TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type

# SSM3K310T

#### High-Speed Switching Applications

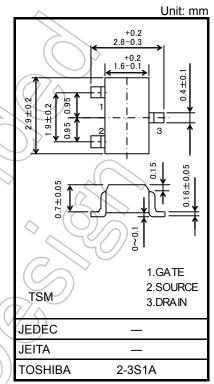
- 1.5 V drive
- Low ON-resistance:  $R_{on} = 66 \text{ m}\Omega \text{ (max)} (@V_{GS} = 1.5 \text{ V})$

 $R_{on} = 28 \text{ m}\Omega \text{ (max)} (@V_{GS} = 4.0 \text{ V})$ 

#### Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V <sub>DS</sub>	20	V	
Gate-Source voltage		V <sub>GSS</sub>	± 10	K1	
Drain current	DC	I <sub>D</sub>	5.0		
	Pulse	I <sub>DP</sub>	10.0	$(// \land)$	
Drain power dissipation		PD (Note 1)	700	m₩	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55~150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).



Weight: 10 mg (typ.)

Note 1: Mounted on an FR4 board. (25.4 mm  $\times$  25.4 mm  $\times$  1.6 t, Cu Pad: 645 mm<sup>2</sup> )

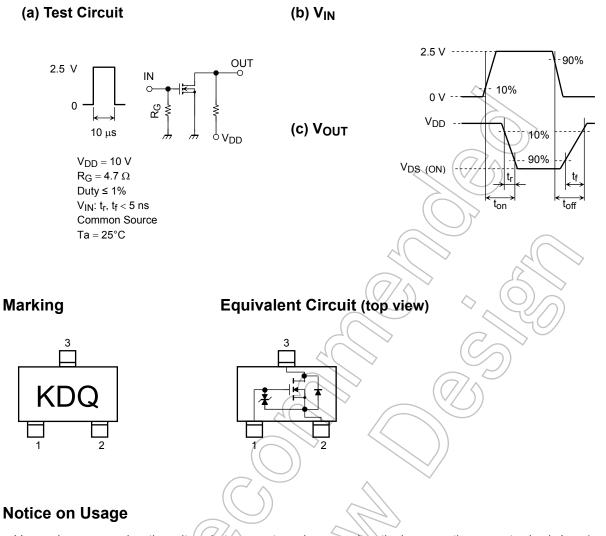
#### Electrical Characteristics (Ta = 25°C)

Characte	eristics	Symbol	Test Condition		Min	Тур.	Max	Unit
Drain-Source breakdown voltage	V (BR) DSS	$I_D = 1 \text{ mA}, V_{GS} = 0$		20	—	_	V	
	V (BR) DSX	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = -10 V		12	_		v	
Drain cutoff current		I <sub>DSS</sub>	$V_{DS} = 20 V, V_{GS} = 0$			_	1	μA
Gate leakage curre	nt	I <sub>GSS</sub>	$V_{GS} = \pm 10 \text{ V}, \text{ V}_{DS} = 0$			_	±1	μA
Gate threshold volt	age	Vth	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 1 mA		0.35	_	1.0	V
Forward transfer ac	dmittance	Y <sub>fs</sub>	$V_{DS} = 3 V, I_D = 4.0 A$ (	Note 2)	14	28	_	S
$\wedge$ (( ))	RDS (ON)	$I_D = 4.0 \text{ A}, V_{GS} = 4.0 \text{ V}$ (	Note 2)	_	19	28	mΩ	
Drain-Source ON-resistance		$I_D = 3.0 \text{ A}, V_{GS} = 2.5 \text{ V}$ (	Note 2)	_	23	32		
		$I_D = 1.0 \text{ A}, V_{GS} = 1.8 \text{ V}$ (	Note 2)	_	28	43		
		$I_D = 0.5 \text{ A}, V_{GS} = 1.5 \text{ V}$ (	Note 2)	_	33	66		
Input capacitance		C <sub>iss</sub>			_	1120	_	
Output capacitance		C <sub>oss</sub>	$V_{DS}=10~V,~V_{GS}=0,~f=1~MHz$		_	180	_	pF
Reverse transfer ca	apacitance	C <sub>rss</sub>			_	160	_	
Total Gate Charge		Qg				14.8		
Gate-Source Charge $Q_{gs}$ $V_{DS}$ = 10 V, $I_{DS}$ = 5.0 A, $V_{GS}$ = 4Gate-Drain Charge $Q_{gd}$		Q <sub>gs</sub>	$V_{DS}$ = 10 V, I <sub>DS</sub> = 5.0 A, V <sub>GS</sub> = 4 V			11.4		nC
				3.4				
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = 10 \text{ V}, \text{ I}_{D} = 2.0 \text{ A},$			21		ns
	Turn-off time	t <sub>off</sub>	$V_{GS}$ = 0 to 2.5 V, $R_{G}$ = 4.7 $\Omega$		—	36	_	
Drain-Source forward voltage		V <sub>DSF</sub>	$I_D = -5.0 \text{ A}, \text{ V}_{GS} = 0 \text{ V}$	(Note 2)		-0.85	-1.2	V

Note 2: Pulse test

Start of commercial production 2006-12

### Switching Time Test Circuit

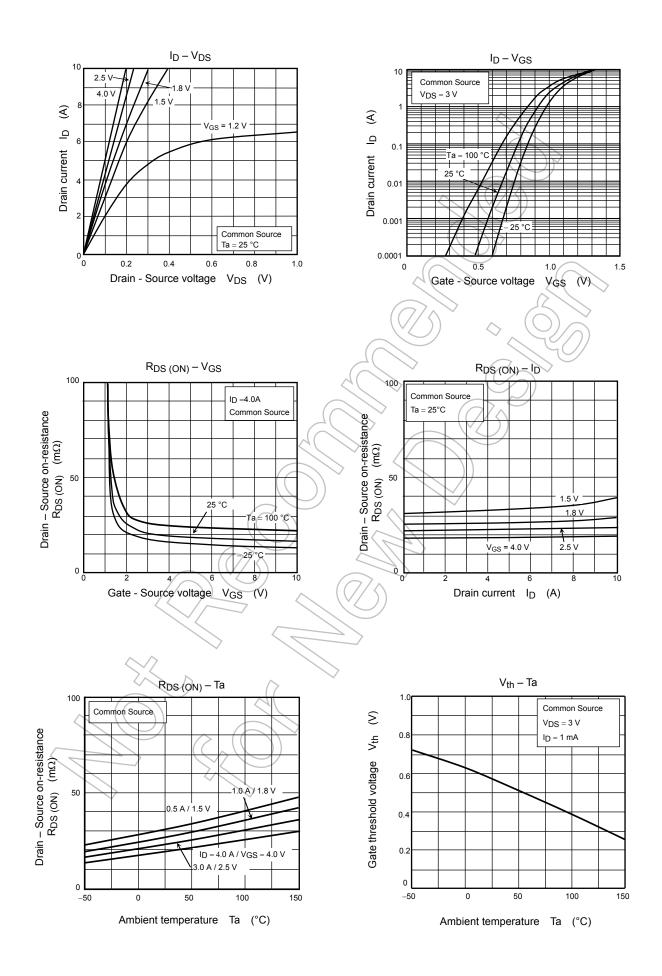


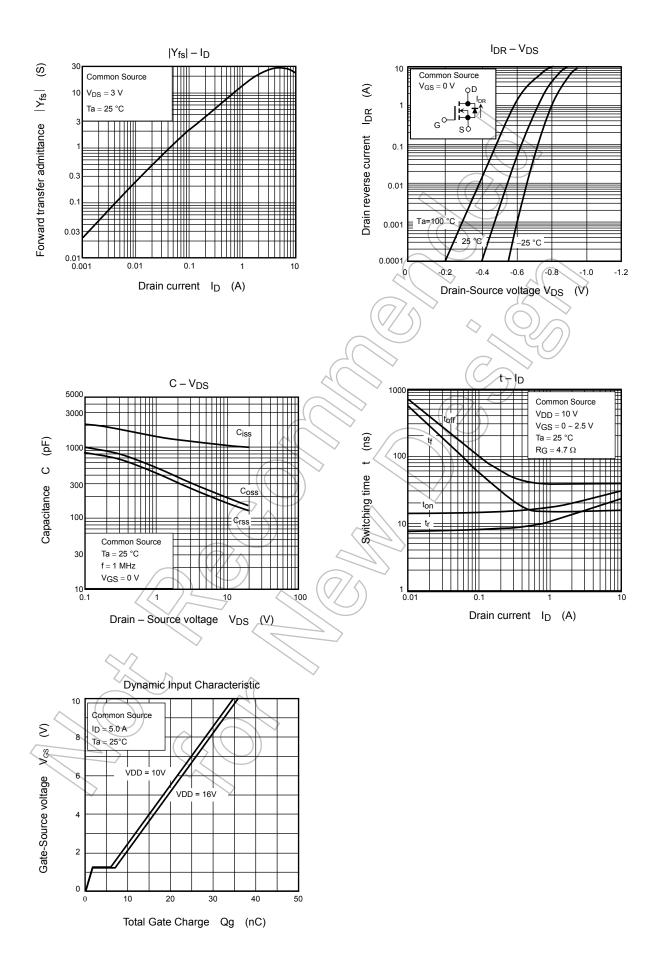
 $V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D = 1$  mA for this product. For normal switching operation,  $V_{GS (on)}$  requires a higher voltage than  $V_{th}$ , and  $V_{GS (off)}$  requires a lower voltage than  $V_{th}$ . (The relationship can be established as follows:  $V_{GS (off)} < V_{th} < V_{GS (on)}$ .)

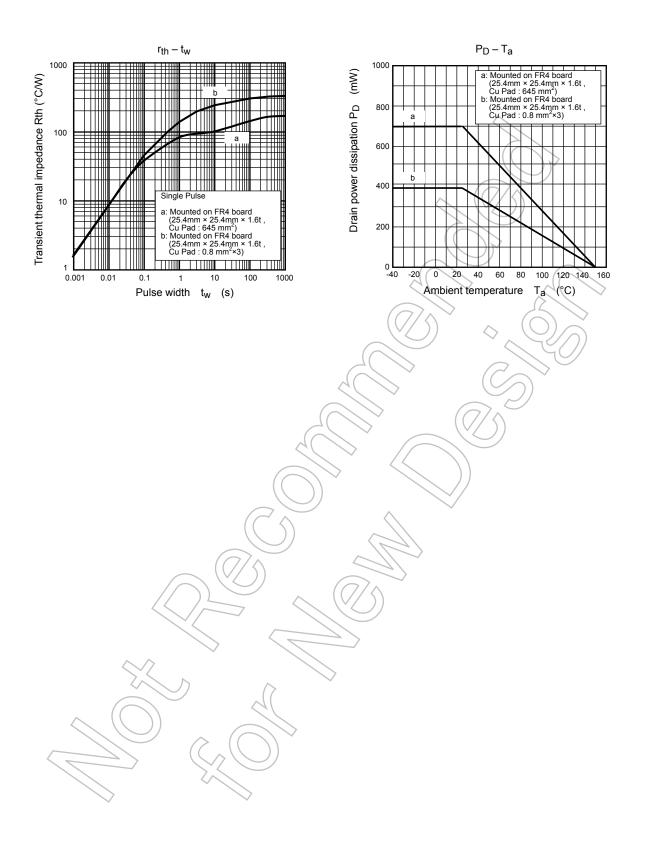
Take this into consideration when using the device.

### Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.







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