Freescale Semiconductor
Data Sheet: Advance Information

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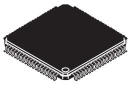
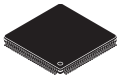
MCF51EM256



80 LQFP
14 mm × 14 mm
917A-03



100 LQFP
14 mm × 14 mm
983-02

MCF51EM256 Series ColdFire Microcontroller

Covers: MCF51EM256
MCF51EM128

The MCF51EM256/128 series microcontrollers are a member of the ColdFire® family of reduced instruction set computing (RISC) microprocessors.

This document provides an overview of these 32-bit microcontrollers, focusing on their highly integrated and diverse feature set.

These microcontrollers are systems-on-chips (SoCs) that are based on the V1 ColdFire core and the following features:

- Operating at processor core speeds up to 50.33 MHz (peripherals operate at half of this speed) at 3.6 V to 2.5 V and 20 MHz at 3.6 V to 1.8 V
- Up to 256 KB of flash memory
- Up to 16 KB of RAM
- Less than 1.3 µA of typical power consumption in battery mode, with MCU supply off
- Ultra-low power independent RTC with calendar features, separate time base, power domain, and 32 bytes of RAM
- A collection of communications peripherals, including UART, IIC and SPI
- Integrated 16-bit SAR analog-to-digital converter
- Programmable delay block (PDB)
- Two analog comparators with selectable interrupt (PRACMP)
- LCD driver
- Three serial communications interface modules (SCI)
- Three serial peripheral interfaces
- Inter-integrated circuit (IIC)
- Two 8-bit and one 16-bit modulo timers (MTIM)
- Two-channel timer/PWM module (TPM)

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

1 MCF51EM256 Series Configurations

1.1 Device Comparison

The MCF51EM256 series is summarized in Table 1.

Table 1. MCF51EM256 Series Features by MCU and Package

Feature	MCF51EM256		MCF51EM128	
Flash size (bytes)	262144		131072	
RAM size (bytes)	16384		8192	
Robust flash update supported	Yes			
Pin quantity	100	80	100	80
PRACMP1 inputs	5	3	5	3
PRACMP2 inputs	5			
ADC modules	4		4	
ADC differential channels[1]	4	2	4	2
ADC single-ended channels	16	12	16	12
DBG	Yes			
ICS	Yes			
IIC	Yes			
IRQ	Yes			
IRTC	Yes			
VREF	Yes			
LCD drivers	44	37	44	37
Rapid GPIO[2]	16	16	16	16
Port I/O[3]	47	40	47	40
Keyboard interface 1	8			
Keyboard interface 2	8			
SCI1	Yes			
SCI2	Yes			
SCI3	Yes			
SPI1 (FIFO)	Yes			
SPI2 (standard)	Yes			
SPI3 (standard)	Yes	No	Yes	No

Table 1. MCF51EM256 Series Features by MCU and Package (continued)

Feature	MCF51EM256	MCF51EM128
MTIM1 (8-bit)	Yes	
MTIM2 (8-bit)	Yes	
MTIM3 (16-it)	Yes	
TPM channels	2	
PDB	Yes	
XOSC1[4]	Yes	
XOSC2[5]	Yes	

[1] Each differential channel is comprised of 2 pin inputs

[2] RGPIO is muxed with standard Port I/O

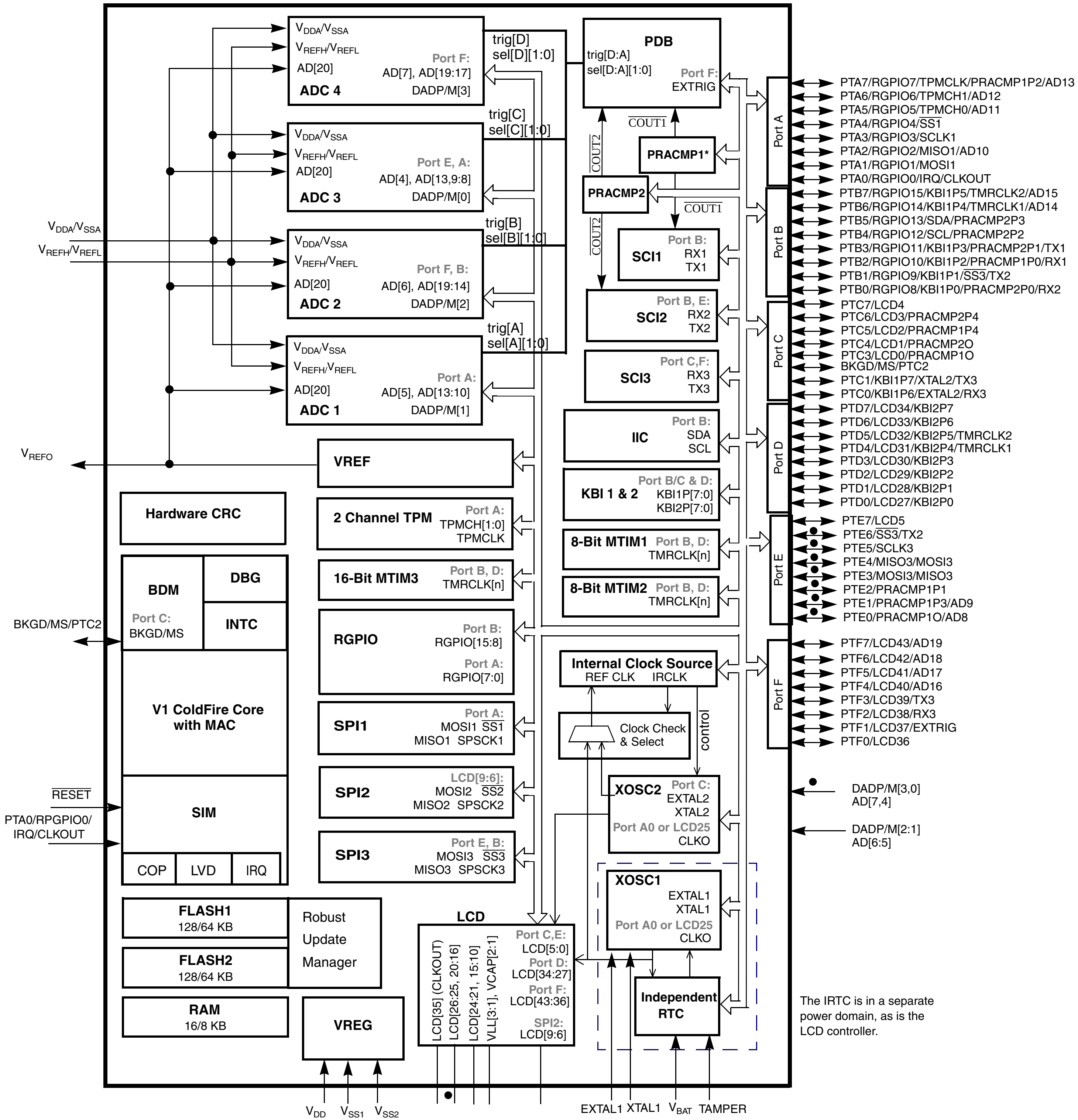
[3] Port I/O count does not include the ouput only PTC2/BKGD/MS.

[4] IRTC crystal input and possible crystal input to the ICS module

[5] Main external crystal input for the ICS module

1.2 Block Diagram

Figure 1 shows the connections between the MCF51EM256 series pins and modules.



[1] Pins with • are not present on 80-pin devices.

[2] PRACMP1 has two less available inputs on the 80-pin devices.

Figure 1. MCF51EM256 Series Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51EM256 series.

Table 2. MCF51EM256 Series Functional Units

Unit	Function
ADC (analog-to-digital converter)	Measures analog voltages at up to 16 bits of resolution. Each ADC has up to four differential and 24 single-ended inputs.
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
CF1 CORE (V1 ColdFire core) with MAC unit	Executes programs, handles interrupts and containes multiply-accumulate hardware (MAC).
PRACMP1, PRACMP2 (comparators)	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (computer operating poperly)	Software watchdog
IRQ (interrupt request)	Single pin high priority interrupt (part of the V1 ColdFire core)
CRC (cyclic Redundancy Check)	High-speed CRC calculation
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
FLASH (flash memory)	Provides storage for program code, constants and variables
IIC (inter-integrated circuits)	Supports standard IIC communications protocol and SMBus
INTC (interrupt controller)	Controls and prioritizes all device interrupts
KBI1 & KBI2	Keyboard Interfaces 1 and 2
LCD	Liquid crystal display driver
LVD (low voltage detect)	Provides an interrupt to the CF1CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event
ICS (internal clock source)	Provides clocking options for the device, including a three frequency-locked loops (FLLs) for multiplying slower reference clock sources
IRTC (independent real-time clock)	The independent real time clock provides an independent time-base with optional interrupt, battery backup and tamper protection
VREF (voltage reference)	The voltage reference output is available for both on and off-chip use
MTIM1, MTIM2 (modulo timers)	8-bit modulo timers with configurable clock inputs and interrupt generation on overflow
MTIM3 (modulo timer)	16-bit modulo timer with configurable clock inputs and interrupt generation on overflow
PDB (programmable delay block)	This timer is optimized for scheduling ADC conversions
RAM (random-access memory)	Provides stack and variable storage
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds and is used to implement GPIO functionality for PTA and PTB.

Table 2. MCF51EM256 Series Functional Units (continued)

Unit	Function
SCI1, SCI2, SCI3(serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SIM (system integration unit)	
SPI1 (FIFO), SPI2, SPI3 (serial peripheral interfaces)	SPI1 has full-complementary drive outputs. SPI2 may be configured with full-complementary drive output via LCD control registers. SPI3 has open drain outputs on SCLK and (MISO or MOSI). These coupled with off-chip pull-up resistors, allow interface to an external 5 V SPI.
TPM (Timer/PWM Module)	Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation
VREG (voltage regulator)	Controls power management across the device
XOSC1 and XOSC2 (crystal oscillators)	These devices incorporate redundant crystal oscillators in separate power domains.One is intended primarily for use by the IRTC, and the other by the CPU and other peripherals.

1.3.1 Feature List

- 32-bit ColdFire V1 central processor unit (CPU)
  - Up to 50.33 MHz ColdFire CPU from 3.6 V to 2.5 V and 20 MHz CPU at 3.6 V to 1.8 V across temperature range of –40 °C to 85 °C
  - ColdFire instruction set revision C (ISA_C) plus MAC
  - 32-bit multiply and accumulate (MAC) optimized for 16×16±32 operations; supports signed or unsigned integer or signed fractional inputs
- On-chip memory
  - MCF51EM256/128 series support two independent flash arrays; read/program/erase over full operating voltage and temperature; allows interrupt processing while programming for robust program updates
  - Random-access memory (RAM)
  - Security circuitry to prevent unathorized access to RAM and Flash contents
- Power-saving modes
  - Two ultra-low power stop modes
  - New low-power run and low-power wait modes
  - Reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Ultra-low power independent real time clock with calendar features (IRTC); runs in all MCU modes; external clock source with trim capabilities; independent voltage source runs IRTC when MCU is powered-down; tamper detection and indicator; battery monitor output to ADC; unaffected by MCU resets
  - Ultra-low power external oscillator that can be used in stop modes to provide accurate clock source to IRTC, ICS and LCD

  - 6 µs typical wakeup time from stop3 mode
- Clock source options
  - Two independent oscillators (XOSC1 and XOSC2) — loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator. XOSC1 nominally supports the independent real time clock, and can be powered by a separate battery backup. XOSC2 is the primary external clock source for the ICS
  - Internal clock source (ICS) — internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference (XOSC1 or XOSC2); precision trimming of internal reference allowing 0.2% resolution and typical 0.5% to –1% deviation over temperature and voltage; supporting CPU frequencies from 4 kHz to 50 MHz
- System protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low voltage detection with reset or interrupt; selectable trip points; seperate low voltage warning with optional interrupt; selectable trip points
  - Illegal opcode and illegal address detection with reset
  - Flash block protection for each array to prevent accidental write/erasure
  - Hardware CRC module to support fast cyclic redundancy checks
- Development support
  - Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection supports same electrical interface used by the S08 family debug modules
  - Real-time debug support with six hardware breakpoints (4 PC, 1 address and 1 data)
  - On-chip trace buffer provides programmable start/stop recording conditions
- Peripherals
  - **ADC16** — 4 analog-to-digital converters; the 100 pin version of the device has 1 dedicated differential channel and 1 dedicated single-ended channel per ADC, along with 3 muxed single-ended channels per ADC. The ADCs have 16-bit resolution, range compare function, 1.7 mV/°C temperature sensor, internal bandgap reference channel, operate in stop3 and are fully functional from 3.6 V to 1.8 V
  - **PDB** — Programmable delay block with 16-bit counter and modulus and 3-bit prescaler; 8 trigger outputs for ADC16 modules (2 per ADC); provides periodic coordination of ADC sampling sequence with programmable sequence completion interrupt
  - **IRTC** — Ultra-low power independent real time clock with calendar features (IRTC); runs in all MCU modes; external clock source with trim capabilities (XOSC1); independent voltage source runs IRTC when MCU is powered-down; tamper detection and indicator; battery monitor output to ADC; unaffected by MCU resets
  - **PRACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to programmable internal reference voltage; operation in stop3
  - **LCD** — up to 288 segments (8 × 36); 160 segments (4 × 40); internal charge pump and option to provide internal reference voltage that can be trimmed for contrast control; flexible

front-plane/backplane pin assignments; operation in all low power modes with blink functionality

  - **SCIx** — Three serial communications interface modules with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; high current drive on Tx on SCI1 and SCI2; wakeup from stop3 on Rx edge. SCI1 and SCI2 Tx pins can be modulated with timer outputs for use with IR interfaces
  - **SPIx**— Two serial peripheral interfaces (SPI2, SPI3) with full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - **SPI16**— Serial peripheral interface (SPI1) with 32-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - **IIC** — Up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
  - **MTIMx** — Two 8-bit and one 16-bit modulo timers with 4-bit prescaler; overflow interrupt; external clock input/pulse accumulator
  - **TPM** — 2-channel Timer/PWM module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator; can be used modulate SCI1 and SCI2 TX pins
- Input/output
  - up to 16 rapid GPIO and 48 standard GPIOs, including 1 output-only pin and 3 open-drain pins.
  - up to 16 keyboard interrupts with selectable polarity
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package options
  - 100-pin LQFP, 80-pin LQFP

1.4 Part Numbers

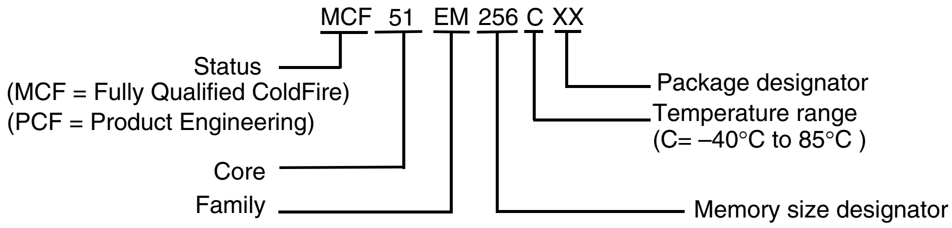


Table 3. Orderable Part Number Summary

Freescale Part Number	Flash / SRAM (KB)	Package	Temperature
MCF51EM256CLL	256/16	100-Pin LQFP	–40°C to 85°C
MCF51EM256CLK	256/16	80-Pin LQFP	–40°C to 85°C
MCF51EM128CLL	128/16	100-Pin LQFP	–40°C to 85°C
MCF51EM128CLK	128/16	80-Pin LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

1.5.1 Pinout: 80-Pin LQFP

Pins not available on the 80-pin LQFP are automatically disabled for reduced current consumption. No user interaction is needed. Software access to the functions on these pins will be ignored

Figure 2 shows the pinout of the 80-pin LQFP.

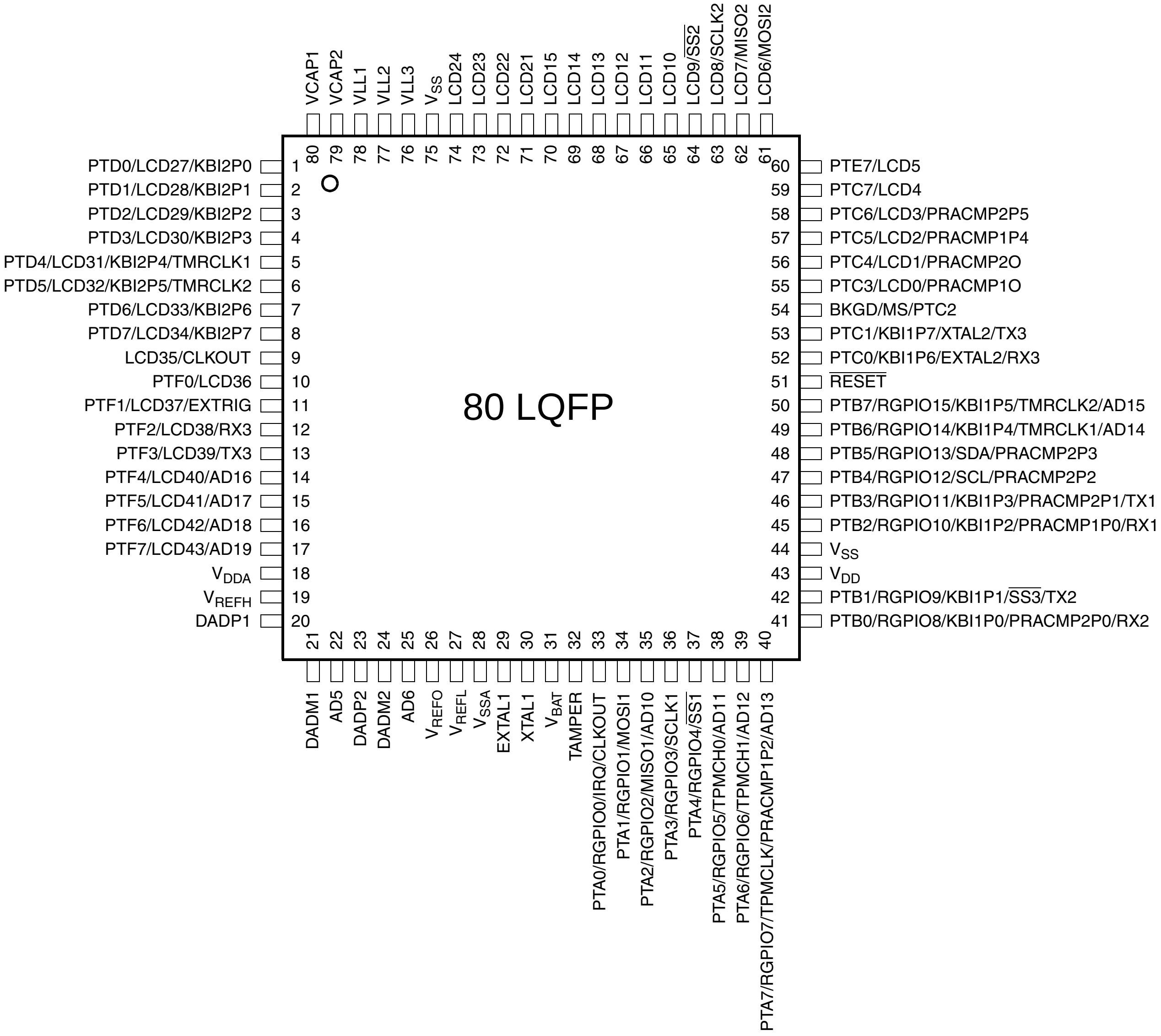


Figure 2. 80-Pin LQFP Pinout

1.5.2 Pinout: 100-Pin LQFP

Figure 3 shows the pinout configuration for the 100-pin LQFP. Pins which are blacked out do not have an equivalent pin on the 80-pin LQFP package.

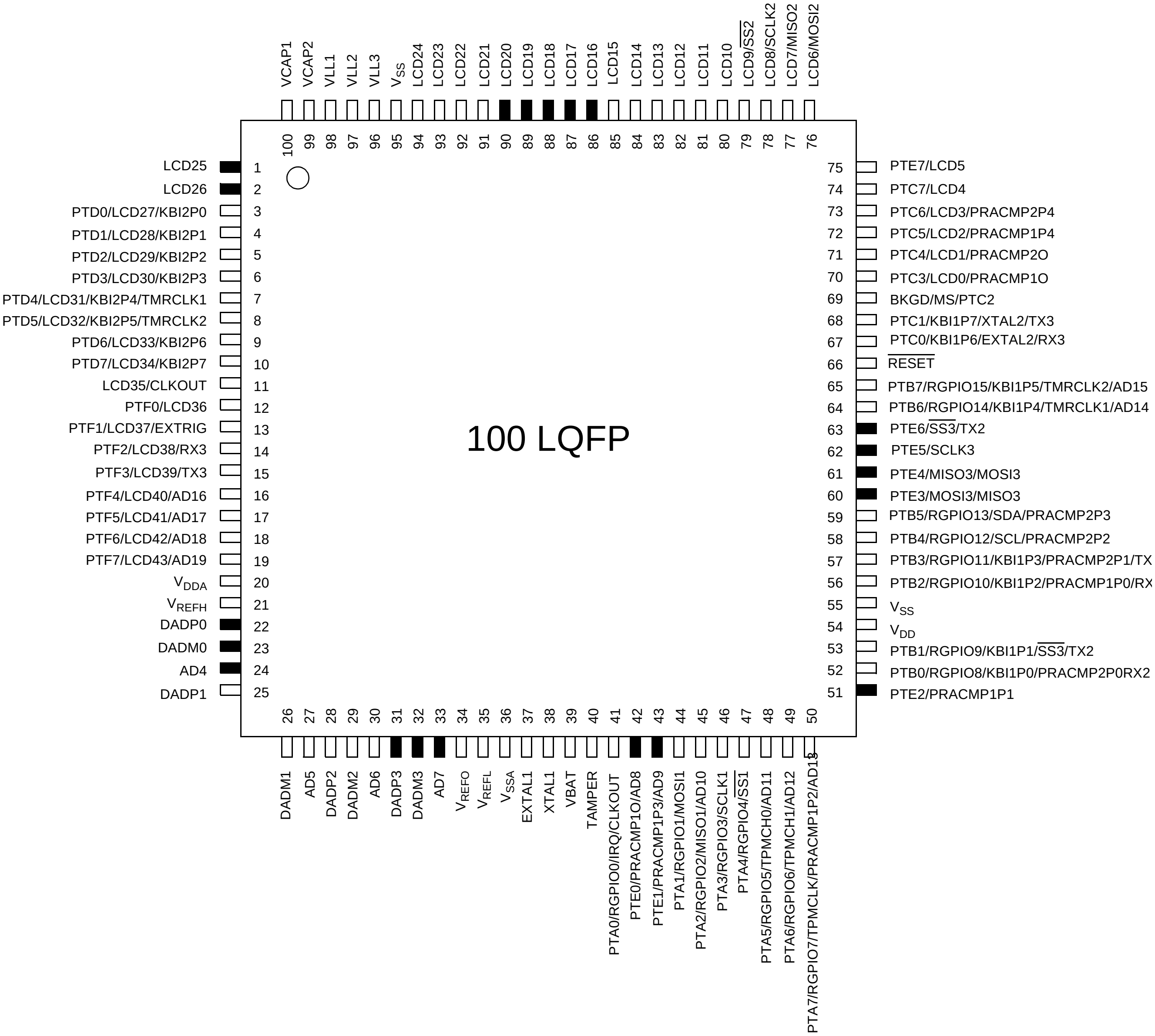


Figure 3. 100-Pin LQFP Pinout

Table 4 shows the package pin assignments.

Table 4. MCF51EM256 Series Package Pin Assignments

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
1	—	LCD25				
2	—	LCD26				
3	1	PTD0	LCD27	KBI2P0		
4	2	PTD1	LCD28	KBI2P1		
5	3	PTD2	LCD29	KBI2P2		
6	4	PTD3	LCD30	KBI2P3		
7	5	PTD4	LCD31	KBI2P4	TMRCLK1	
8	6	PTD5	LCD32	KBI2P5	TMRCLK2	
9	7	PTD6	LCD33	KBI2P6		
10	8	PTD7	LCD34	KBI2P7		
11	9	LCD35	CLKOUT			
12	10	PTF0	LCD36			
13	11	PTF1	LCD37		EXTRIG	
14	12	PTF2	LCD38		RX3	
15	13	PTF3	LCD39		TX3	
16	14	PTF4	LCD40		AD16	
17	15	PTF5	LCD41		AD17	
18	16	PTF6	LCD42		AD18	
19	17	PTF7	LCD43		AD19	
20	18	V_{DDA}				
21	19	V_{REFH}				
22	—	DADP0				
23	—	DADM0				
24	—	AD4				
25	20	DADP1				
26	21	DADM1				
27	22	AD5				
28	23	DADP2				
29	24	DADM2				
30	25	AD6				
31	—	DADP3				
32	—	DADM3				

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
33	—	AD7				
34	26	V_{REFO}				
35	27	V_{REFL}				
36	28	V_{SSA}				
37	29	EXTAL1				
38	30	XTAL1				
39	31	V_{BAT}				
40	32	TAMPER				
41	33	PTA0/RGPIO0	IRQ	CLKOUT		
42	—	PTE0		PRACMP1O	AD8	
43	—	PTE1		PRACMP1P3	AD9	
44	34	PTA1/RGPIO1	MOSI1			RGPIO_ENB is used to select between standard GPIO and RGPIO
45	35	PTA2/RGPIO2	MISO1		AD10	
46	36	PTA3/RGPIO3	SCLK1			
47	37	PTA4/RGPIO4	$\overline{\text{SS1}}$			
48	38	PTA5/RGPIO5	TPMCH0		AD11	
49	39	PTA6/RGPIO6	TPMCH1		AD12	
50	40	PTA7/RGPIO7	TPMCLK	PRACMP1P2	AD13	
51	—	PTE2		PRACMP1P1		
52	41	PTB0/RGPIO8	KBI1P0	PRACMP2P0	RX2	RGPIO_ENB is used to select between standard GPIO and RGPIO
53	42	PTB1/RGPIO9	KBI1P1	$\overline{\text{SS3}}$	TX2	2X Drive Output RGPIO_ENB is used to select between standard GPIO and RGPIO
54	43	V_{DD}				
55	44	V_{SS}				
56	45	PTB2/RGPIO10	KBI1P2	PRACMP1P0	RX1	RGPIO_ENB is used to select between standard GPIO and RGPIO
57	46	PTB3/RGPIO11	KBI1P3	PRACMP2P1	TX1	2X drive output RGPIO_ENB is used to select between standard GPIO and RGPIO

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
58	47	PTB4/RGPIO12	SCL	PRACMP2P2		RGPIO_ENB is used to select between standard GPIO and RGPIO
59	48	PTB5/RGPIO13	SDA	PRACMP2P3		
60	—	PTE3	MOSI3	MISO3		
61	—	PTE4	MISO3	MOSI3		Open Drain
62	—	PTE5	SCLK3			Open Drain
63	—	PTE6	$\overline{\text{SS3}}$	TX2		Open Drain
64	49	PTB6/RGPIO14	KBI1P4	TMRCLK1	AD14	RGPIO_ENB is used to select between standard GPIO and RGPIO
65	50	PTB7/RGPIO15	KBI1P5	TMRCLK2	AD15	
66	51	$\overline{\text{RESET}}$				This pin is an open drain device and has an internal pullup. There is no clamp diode to V_{DD}.
67	52	PTC0	KBI1P6	EXTAL2	RX3	
68	53	PTC1	KBI1P7	XTAL2	TX3	
69	54	BKGD/MS	PTC2			This pin has an internal pullup. PTC2 can only be programmed as an output.
70[1]	55[1]	PTC3	LCD0	PRACMP1O		
71[1]	56[1]	PTC4	LCD1	PRACMP2O		
72[1]	57[1]	PTC5	LCD2		PRACMP1P4	
73[1]	58[1]	PTC6	LCD3		PRACMP2P4	
74[1]	59[1]	PTC7	LCD4			
75[1]	60[1]	PTE7	LCD5			
76[1]	61[1]	LCD6	MOSI2			
77[1]	62[1]	LCD7	MISO2			
78[1]	63[1]	LCD8	SCLK2			
79[1]	64[1]	LCD9	$\overline{\text{SS2}}$			
80	65	LCD10				
81	66	LCD11				
82	67	LCD12				
83	68	LCD13				
84	69	LCD14				
85	70	LCD15				
86	—	LCD16				

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
87	—	LCD17				
88	—	LCD18				
89	—	LCD19				
90	—	LCD20				
91	71	LCD21				
92	72	LCD22				
93	73	LCD23				
94	74	LCD24				
95	75	V_{SS}				
96	76	VLL3				
97	77	VLL2				
98	78	VLL1				
99	79	VCAP2				
100	80	VCAP1				

[1] These pins that are shared with the LCD are open-drain by default if not used as LCD pins. To configure this pins as full complementary drive outputs, you must have the LCD modules bits configured as follow: FCDEN =1, VSUPPLY = 11 and RVEN = 0. The Input levels and internal pullup resistors are referenced to VLL3. Referer to the LCD chapter for further information.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51EM256/128 series microcontrollers, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 4.0	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins except PTB1 and PTB3)[1], [2], [3]	I_D	±25	mA
Instantaneous maximum current Single pin limit (applies to PTB1 and PTB3)[4], [5], [6]	I_D	±50	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

[4] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[5] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[6] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance [1,2,3,4]	θ_{JA}		°C/W
100-pin LQFP			
1s		54	
2s2p		42	
80-pin LQFP			
1s		55	
2s2p		42	

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2] Junction to Ambient Natural Convection

[3] 1s — Single layer board, one signal layer

[4] 2s2p — Four layers board, two signal and two power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Machine Model (MM)	V_{MM}	±200	—	V
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V
4	Latch-up Current at T_A = 85 °C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
1	P	Operating voltage	Digital supply — 50 MHz operation	V_{DD}	2.5	—	3.6	V
			Digital supply[2] — 20 MHz maximum operation	V_{DD}	1.8	—	3.6	
2	P	Analog supply		V_{DDA}	1.8	—	3.6	V
3	D	Battery supply		V_{BAT}	2.2	3	3.3	V
4	P	Bandgap voltage reference[3]		V_{BG}	1.15	1.17	1.18	V
5	C	Output high voltage	PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], low-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -0.6$ mA	V_{OH}	$V_{DD} - 0.5$	—	—	V
	P		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA					
	C		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -3$ mA					
6	C	Output high voltage	PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, low drive strength. VDD ≥ 1.8 V, $I_{Load} = -0.5$ mA	V_{OH}	$V_{DD} - 0.5$	—	—	V
	P		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = -3$ mA					
	C		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = -1$ mA					
7	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	100	mA

Table 10. DC Characteristics (continued)

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
8	C	Output low voltage	PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], low-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 2$ mA	V_{OL}	—	—	0.50	V
	P		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA					
	C		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA					
9	C	Output low voltage	PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, low drive strength. VDD ≥ 1.8 V, $I_{Load} = 0.5$ mA	V_{OL}	—	—	0.50	V
	P		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 2.7$ V, $I_{Load} = 3$ mA					
	C		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 1.8$ V, $I_{Load} = 1$ mA					
10	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	100	mA
11	P	Input high voltage	All digital inputs except tamper_in, $V_{DD} > 2.7$ V	V_{IH}	$0.70 \times V_{DD}$	—	—	V
			All digital inputs except tamper_in, $2.7\text{ V} > V_{DD} \geq 1.8$ V		$0.85 \times V_{DD}$	—	—	
			Tamper_in		1.5	—	—	
12	P	Input low voltage	All digital inputs except tamper_in, $V_{DD} > 2.7$ V	V_{IL}	—	—	$0.35 \times V_{DD}$	V
			all digital inputs except tamper_in, $2.7\text{ V} > V_{DD} \geq 1.8$ V		—	—	$0.3 \times V_{DD}$	
			Tamper_in		—	—	0.5	
13	C	Input hysteresis; all digital inputs		V_{hys}	$0.06 \times V_{DD}$	—	—	mV
14	P	Input leakage current; input only pins[4]		$\lvert I_{In} \rvert$	—	0.1	1	μA
15	P	High Impedance (off-state) leakage current[4]		$\lvert I_{OZ} \rvert$	—	0.1	1	μA
16	P	Internal pullup resistors[5]		R_{PU}	17.5	—	52.5	kΩ
17	P	Internal pulldown resistors[6]		R_{PD}	17.5	—	52.5	kΩ
18	C	Input capacitance; all non-supply pins		C_{In}	—	—	8	pF
19	P	POR rearm voltage		V_{POR}	0.9	1.4	2.0	V
20	D	POR rearm time		t_{POR}	10	—	—	μs
21	P	Low-voltage detection threshold	High range — V_{DD} falling	V_{LVDH}	2.300	2.355	2.410	V
			High range — V_{DD} rising		2.370	2.425	2.480	

Table 10. DC Characteristics (continued)

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
22	C	Low-voltage detection threshold	Low range — V_{DD} falling	V_{LVDL}	1.800	1.845	1.890	V
			Low range — V_{DD} rising		1.870	1.915	1.960	V
23	P	Low-voltage warning threshold	V_{DD} falling, LVWV = 1	V_{LVWH}	2.590	2.655	2.720	V
			V_{DD} rising, LVWV = 1		2.580	2.645	2.710	
24	C	Low-voltage warning	V_{DD} falling, LVWV = 0	V_{LVWL}	2.300	2.355	2.410	V
			V_{DD} rising, LVWV = 0		2.360	2.425	2.490	
25	D	RAM retention voltage		V_{RAM}	—	0.6	1.0	V
26	D	DC injection current[7] [8] [9] [10] (single pin limit), $V_{IN} > V_{DD}$, $V_{IN} < V_{SS}$		I_{IC}	–0.2	—	0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins), $V_{IN} > V_{DD}$, $V_{IN} < V_{SS}$			–5	—	5	mA

[1] Typical values are based on characterization data at 25 °C unless otherwise stated.

[2] Switch to lower frequency when the low-voltage interrupt asserts (V_{LVDH}).

[3] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

[4] Measured with $V_{In} = V_{DD}$ or V_{SS}.

[5] Measured with $V_{In} = V_{SS}$.

[6] Measured with $V_{In} = V_{DD}$.

[7] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[8] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[9] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[10] The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

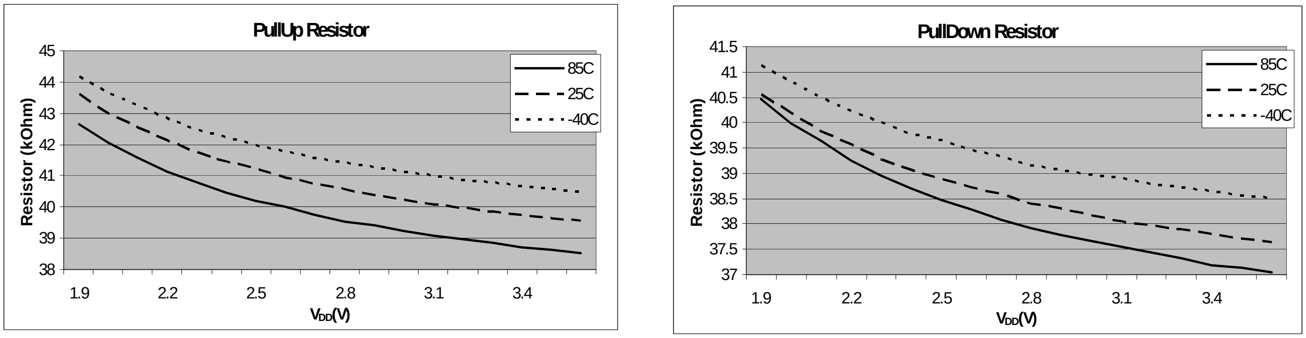


Figure 4. Pullup and Pulldown Typical Resistor Values

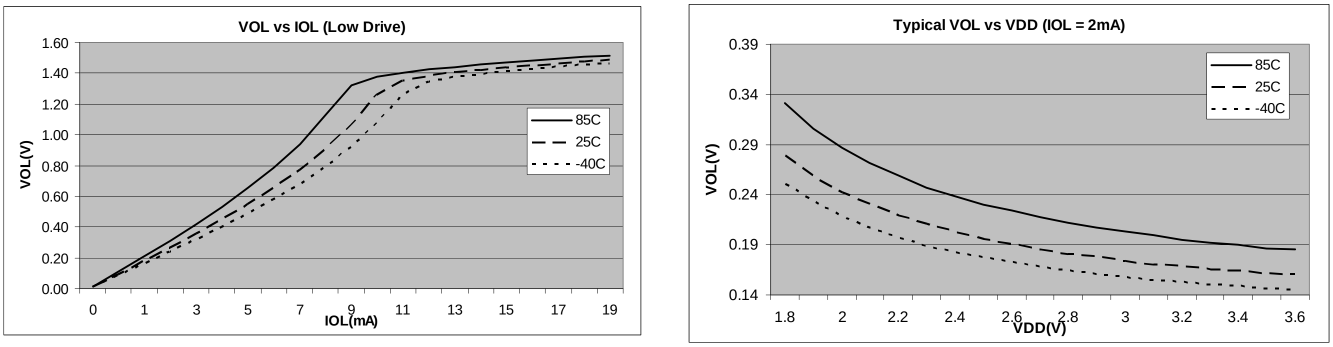


Figure 5. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

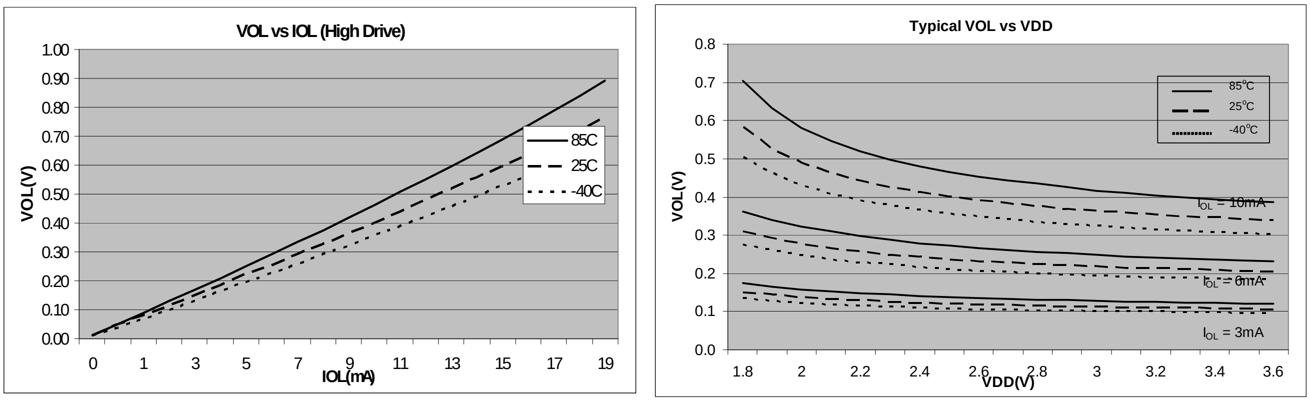


Figure 6. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

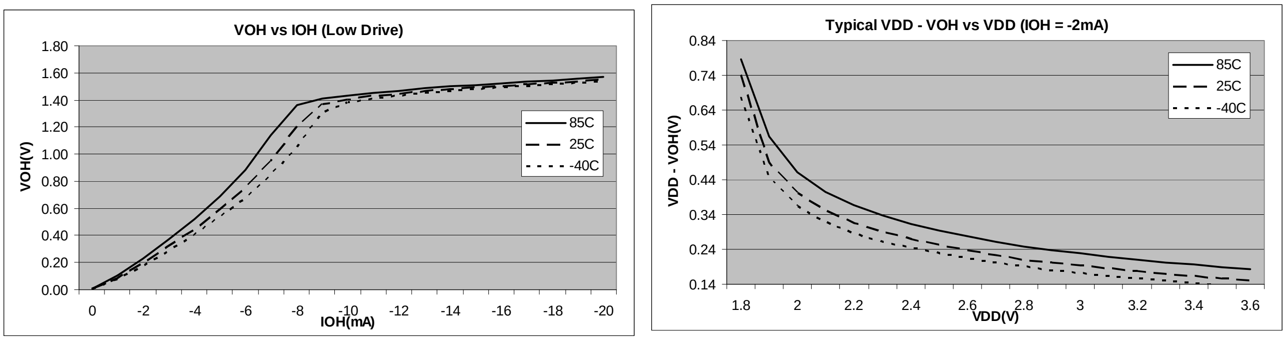


Figure 7. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

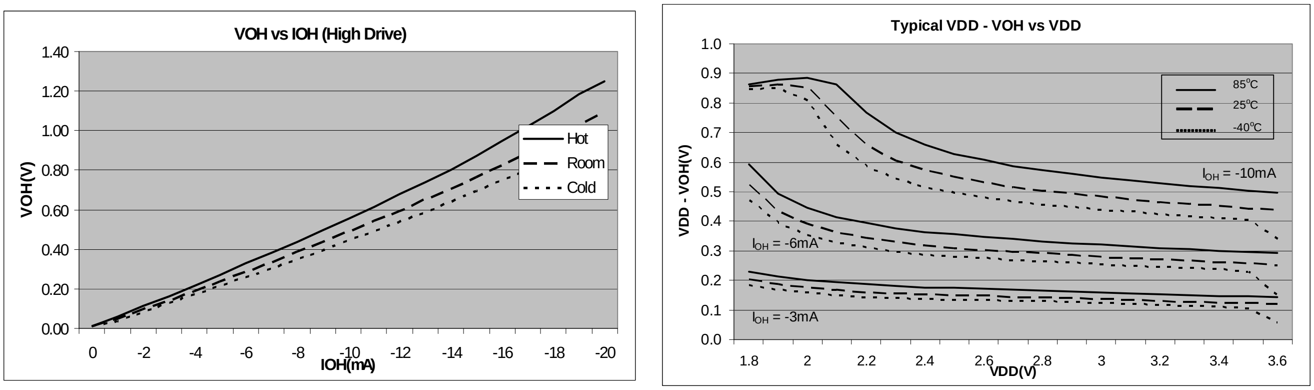


Figure 8. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

2.6 Supply Current Characteristics

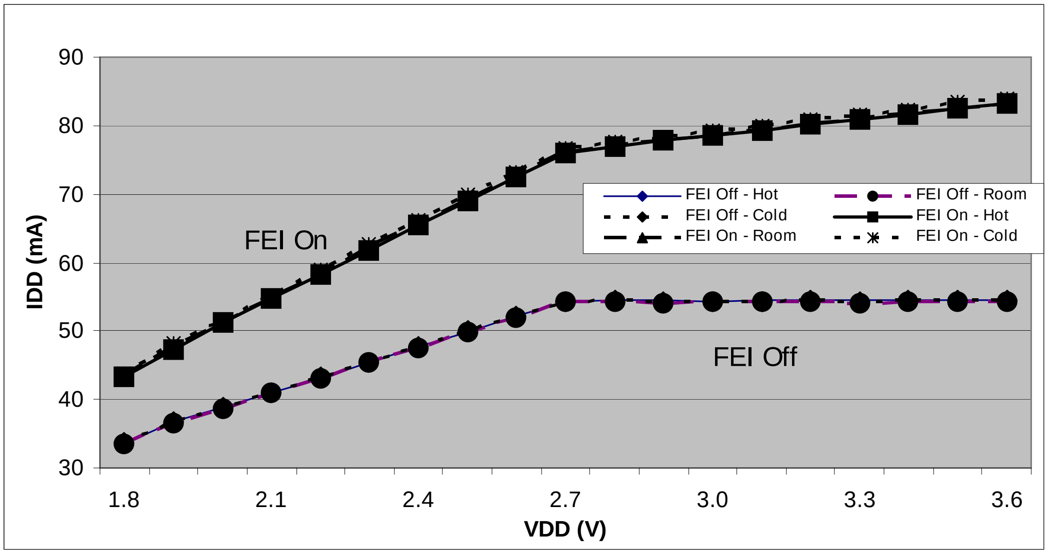


Figure 9. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (All Modules Enabled)

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	25.165 MHz	RI_{DD}	3	66.2	100	mA	–40 to 85°C
	T		20 MHz			55.3	—		
	T		8 MHz			23.9	—		
	T		1 MHz			4.56	—		
2	C	Run supply current FEI mode, all modules off	25.165 MHz	RI_{DD}	3	55.1	56	mA	–40 to 85°C
	T		20 MHz			46.6	—		
	T		8 MHz			19.9	—		
	T		1 MHz			3.92	—		
3	T	Run supply current LPS=0, all modules off	16 kHz FBILP	RI_{DD}	3	239	—	µA	—
	T		16 kHz FBELP			249	—		
4	T	Run supply current LPS = 1, all modules off, running from flash	16 kHz FBELP	RI_{DD}	3	50	—	µA	—
5	C	Wait mode supply current FEI mode, all modules off	25.165 MHz	WI_{DD}	3	51.1	69	mA	–40 to 85°C
	T		20 MHz			42.6	—		
	T		8 MHz			18.8	—		
	T		1			3.69	—		
6	T	Wait mode supply current LPRS = 1, all mods off		WI_{DD}	3	1	—	µA	—
7	P	Stop2 mode supply current		$S2I_{DD}$	3	0.576	30	µA	–40 to 85°C
	C				2		16		
8	P	Stop3 mode supply current		$S3I_{DD}$	3	1.05	45	µA	–40 to 85°C
	C				2		27		
9	T	LVD adder to stop3, stop2 (LVDE = LVDSE = 1)		$S3I_{DDLVD}$	3	120	—	µA	—
10	T	Voltage reference adder to stop3	Low power mode	$S3I_{DDLVD}$	3	90	—	µA	—
			Tight regulation mode			270			
11	T	PRACMP adder to stop3	PRG disabled	$S3I_{DDLVD}$	3	13	—	µA	—
			PRG enabled			29			
12	T	LCD adder to stop3, stop2, VIREG enabled, 1/4 duty cycle, 4x39 configuration for 156 segments, 32Hz frame rate, no LCD glass connected		$S3I_{DDLVD}$	3	1.3	—	µA	—
13	C	Adder to stop3 for oscillator enabled[2] (ERCLKEN =1 and EREFSTEN = 1)		$S3I_{DDOSC}$	3	5		µA	—

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
14	P	IRTC supply current[3,4,5]	$I_{DD\text{-}BAT}$		1.5	5	µA	–40 to 85°C

[1] Typicals are measured at 25 °C.

[2] Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

[3] This is the current consumed when the IRTC is being powered by the V_{BAT}.

[4] The IRTC power source depends on the MCU configuration and V_{DD} voltage level. Refer to reference manual for further information.

[5] The IRTC current consumption includes the IRTC XOSC1.

2.7 Analog Comparator (PRACMP) Electricals

Table 12. PRACMP Electrical Specifications

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{PWR}	1.8	—	3.6	V
2	C	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA
3	C	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA
4	D	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA
5	—	Analog input voltage	VAIN	$V_{SS} - 0.3$	—	V_{DD}	V
6	T	Analog input offset voltage	VAIO	—	5	40	mV
7	T	Analog comparator hysteresis	V_H	3.0	—	20.0	mV
8	D	Analog input leakage current	I_{ALKG}	—	—	1	nA
9	T	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs
10	—	Programmable reference generator input1	$V_{In1}(V_{DD})$	—	V_{DD}	—	V
11	T	Programmable reference generator input2	$V_{In2}(V_{DD25})$	1.8	—	2.75	V
12	D	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs
13	D	Programmable reference generator step size	Vstep	–0.25	0	0.25	LSB
14	P	Programmable reference generator voltage range	V_{prgout}	$V_{In}/32$	—	V_{in}	V

2.8 ADC Characteristics

These specs all assume seperate V_{DDAD} supply for ADC and isolated pad segment for ADC supplies and differential inputs. Spec's should be de-rated for $V_{REFH} = V_{bg}$ condition.

Table 13. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
2		Delta to V_{DD} $(V_{DD}–V_{DDA})^2$	ΔV_{DDA}	–100	0	100	mV	
3	Ground voltage	Delta to V_{SS} $(V_{SS}–V_{SSA})^2$	ΔV_{SSA}	–100	0	100	mV	
4	Ref Voltage High		V_{REFH}	1.15	V_{DDA}	V_{DDA}	V	

Table 13. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
5	Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
6	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
7	Input Capacitance	16-bit modes 8/10/12-bit modes	C_{ADIN}	—	8 4	10 5	pF	
8	Input Resistance		R_{ADIN}	—	2	5	kΩ	
9	Analog Source Resistance	16 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	1 2 5		
11		11/10 bit modes $f_{ADCK} > 8MHz$ $4MHz < f_{ADCK} < 8MHz$ $f_{ADCK} < 4MHz$		— — —	— — —	2 5 10		
12		9/8 bit modes $f_{ADCK} > 8MHz$ $f_{ADCK} < 8MHz$		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	8	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

[1] Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

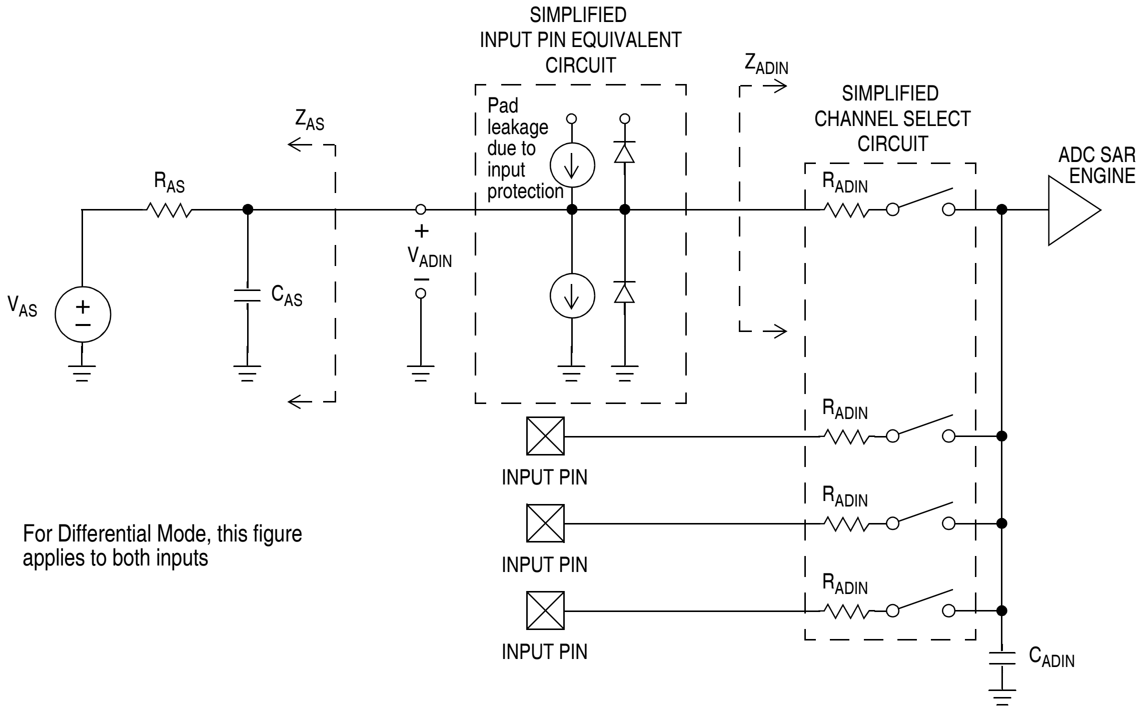


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 8$MHz)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Supply Current	ADLPC = 1, ADHSC = 0	T	I_{DDA}	—	215	—	µA	ADLSMP = 0 ADCO = 1
	ADLPC = 0, ADHSC = 0			—	470	—		
	ADLPC=0, ADHSC=1			—	610	—		
Supply Current	Stop, Reset, Module Off	C	I_{DDA}	—	0.01	—	µA	
ADC Asynchronous Clock Source	ADLPC = 1, ADHSC = 0	P	f_{ADACK}	—	2.4	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC = 0, ADHSC = 0			—	5.2	—		
	ADLPC = 0, ADHSC = 1			—	6.2	—		
Sample Time	See reference manual for sample times							
Conversion Time	See reference manual for conversion times							

Table 14. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+48/-40 +56/-28	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±3.0 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	+5/-3 +5/-3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±16.0 ±20.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.5 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+32/-24 +24/-16	LSB[2]	$V_{ADIN} = V_{SSAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.5 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 14. 16-bit ADC Characteristics full operating range($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 8MHz$)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+10/0 +14/0	+42/-2 +46/-2	LSB[2]	$V_{ADIN} = V_{DDAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±3.5 ±3.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.5 ±1.5		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C	ENOB	12.8 12.7 12.6 12.5 11.9	14.2 13.8 13.6 13.3 12.5	— — — — —	Bits	$F_{in} = F_{sample}/100$
	16 bit single-ended mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	C		— — — — —	TBD TBD TBD TBD TBD	— — — — —		
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	-91.5	-74.3	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	-85.5	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	75.0	92.2	—	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	86.2	—		
Input Leakage Error	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40°C– 25°C	C	m	—	1.646	—	mV/°C	
	25°C– 125°C			—	1.769	—		
Temp Sensor Voltage	25°C	C	V_{TEMP25}	—	701.2	—	mV	

[1] All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDAD}$

[2] Typical values assume $V_{DDAD} = 3.0V$, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[3] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

Table 15. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	T	TUE	— —	±16 ±20	+24/-24 +32/-20	LSB[3]	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.5 ±1.75	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.7 ±0.8	±1.0 ±1.25		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±1 ±1		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±0.75 ±0.75		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	T	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	
	13-bit differential mode 12-bit single-ended mode	T		— —	±1.0 ±1.0	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.5 ±0.5	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.3 ±0.3	±0.5 ±0.5		
Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	$V_{ADIN} = V_{SSAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.0		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		

Table 15. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, ADHSC=1)

Characteristic	Conditions[1]	C	Symb	Min	Typ[2]	Max	Unit	Comment
Full-Scale Error	16-bit differential mode 16-bit single-ended mode	T	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	$V_{ADIN} = V_{DDAD}$
	13-bit differential mode 12-bit single-ended mode	T		— —	±0.7 ±0.7	±2.0 ±2.5		
	11-bit differential mode 10-bit single-ended mode	T		— —	±0.4 ±0.4	±1.0 ±1.0		
	9-bit differential mode 8-bit single-ended mode	T		— —	±0.2 ±0.2	±0.5 ±0.5		
Quantization Error	16 bit modes	D	E_Q	—	-1 to 0	—	LSB[2]	
	≤13 bit modes			—	—	±0.5		
Effective Number of Bits	16 bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1	C	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	$F_{in} = F_{sample}/100$
Signal to Noise plus Distortion	See ENOB		SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB	
Total Harmonic Distortion	16-bit differential mode Avg = 32	C	THD	—	-95.8	-90.4	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	—	—		
Spurious Free Dynamic Range	16-bit differential mode Avg = 32	C	SFDR	91.0	96.5	—	dB	$F_{in} = F_{sample}/100$
	16-bit single-ended mode Avg = 32	D		—	—	—		
Input Leakage Error	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C–25°C	D	m	—	1.646	—	mV/°C	
	25°C–125°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

[1] All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDAD}$

[2] Typical values assume $V_{DDAD} = 3.0$ V, Temp = 25 °C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[3] 1 LSB = $(V_{REFH}–V_{REFL})/2^N$

2.9 External Oscillator (XOSC) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits. XOSC1 operates only in low power low range mode. XOSC2 operates in all the power and range modes.

Table 16. XOSC Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	f_{lo} f_{hi} f_{hi}	32 1 1	— — —	38.4 16 8	kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO = 0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	R_F	— — —	— 10 1	— — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	— 0 100 0 0 0	— — — 0 10 20	kΩ
5	T	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	t_{CSTL} t_{CSTH}	— — — —	600 400 5 15	— — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	50.33 50.33	MHz MHz

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

[2] Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.

[3] See crystal or resonator manufacturer’s recommendation.

[4] Proper PC board layout procedures must be followed to achieve specifications.

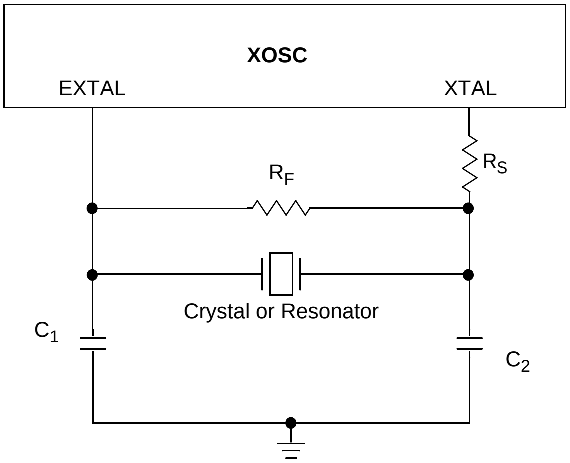


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

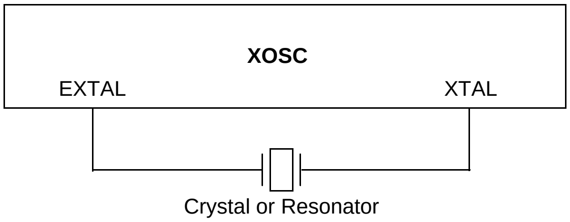


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Gain

2.10 Internal Clock Source (ICS) Characteristics

Table 17. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_u}	16	—	20	MHz
	C		Mid range (DRS = 01)		32	—	40	
	P		High range (DRS = 10)		48	—	60	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
	P		High range (DRS = 10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	%f_{dco}
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	%f_{dco}

Table 17. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time [3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

[2] The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

[3] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[4] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

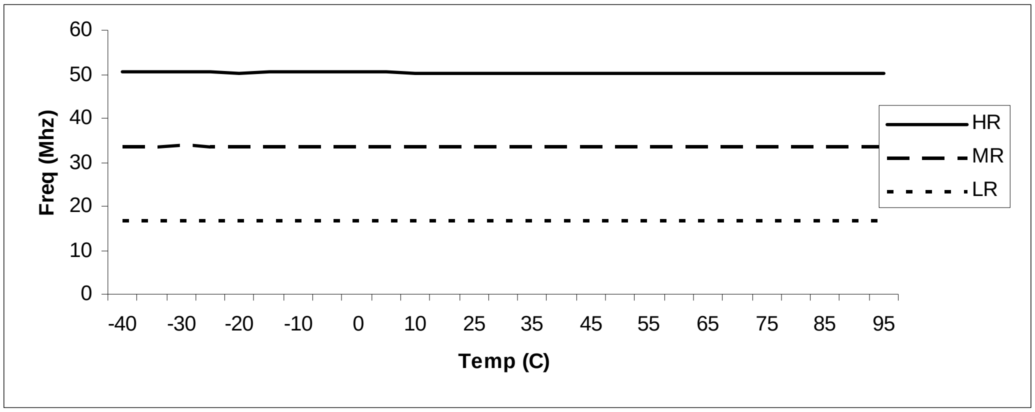


Figure 13. Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 3.0 V)

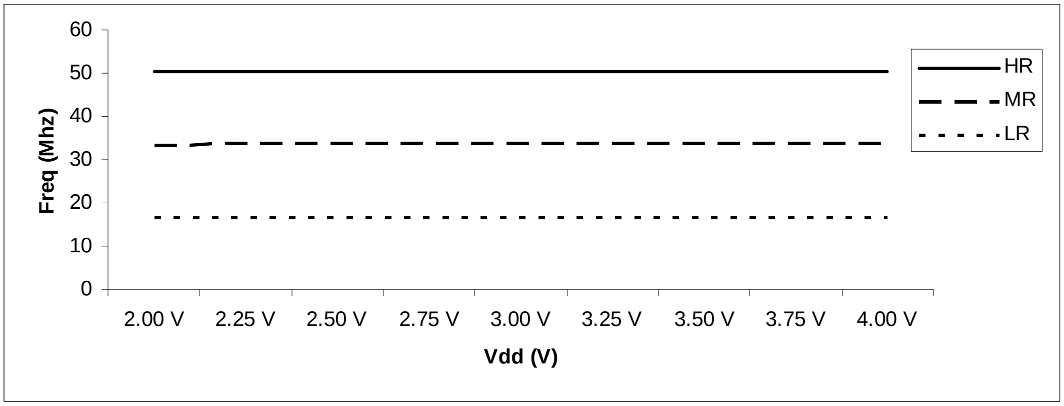


Figure 14. Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 25 °C)

2.11 LCD Specifications

Table 18. LCD Electricals, 3 V Glass

N	C	Characteristic		Symbol	Min	Typical	Max	Unit
1	D	LCD frame frequency		f_{Frame}	28	30	58	Hz
2	D	LCD charge pump capacitance		C_{LCD}		100	100	nF
3	D	LCD bypass capacitance		C_{BYLCD}		100	100	nF
4	D	LCD glass capacitance		C_{glass}		2000	8000	pF
5	D	V_{IREG}	HRefSel = 0	V_{IREG}	.89	1.00	1.15	V
6			HRefSel = 1		1.49	1.67	1.85[1]	
7	D	V_{IREG} trim resolution		Δ_{RTRIM}	1.5			% V_{IREG}
8	D	V_{IREG} ripple	HRefSel = 0		—		0.1	V
			HRefSel = 1				0.15	
9	D	V_{IREG} current adder	RVEN = 1	I_{VIREG}	—	1[2]		µA
10	D	V_{LCD} buffered adder[3]		I_{Buff}	—	1		µA

[1] V_{IREG} Max can not exceed V_{DD} – 0.15 V

[2] 2000 pF Load LCD, frame frequency = 32 Hz

[3] VSUPPLY = 10, BYPASS = 0

2.12 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

2.12.1 Control Timing

Table 19. Control Timing

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	25.165	MHz
2	D	Internal low-power oscillator period	t_{LPO}	700		1300	µs
3	D	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100		—	ns
4	D	Reset low drive	t_{rstdrv}	66 × t_{cyc}		—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500		—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100		—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 × t_{cyc}	—	—	ns
8	D	KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 × t_{cyc}	—	—	ns
9	D	Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0), low drive Slew rate control enabled (PTxSE = 1), low drive Slew rate control disabled (PTxSE = 0), low drive Slew rate control enabled (PTxSE = 1), low drive	t_{Rise}, t_{Fall}	— —	11 35 40 75		ns

---

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

[3] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

[4] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

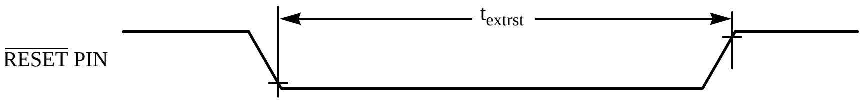


Figure 15. Reset Timing

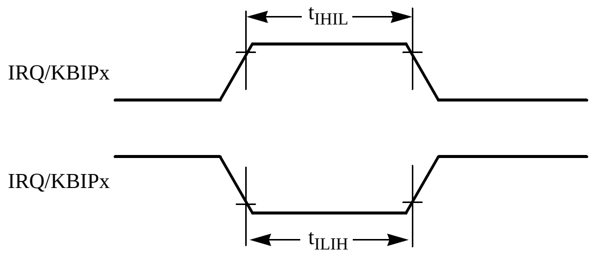


Figure 16. IRQ/KBIPx Timing

2.12.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 20. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

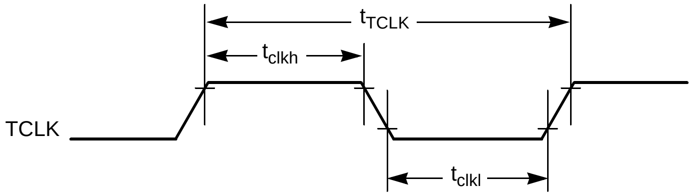


Figure 17. Timer External Clock

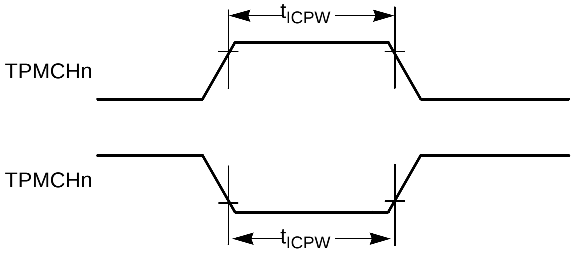


Figure 18. Timer Input Capture Pulse

2.13 VREF Characteristics

Table 21. VREF Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DDAD}	1.80	—	3.60	V
2	—	Operating temperature range	T_{op}	–40	—	105	°C
3	D	Load capability	I_{load}	—	—	10	mA
4	C P	Voltage reference output untrimmed factory trimmed	V_{REFO}	1.070 1.04	— 1.150	1.202 1.17	V V
5	D	Load regulation mode = 10, I_{load} = 1 mA		20	—	100	µV/mA
6	T	Line regulation (power supply rejection) DC AC		±0.1 from room temp voltage –60			mV dB
7	T	Bandgap only (mode = 00)	I_{BG}	—	72	—	µA
8	C	Low power mode (mode = 01)	I_{LP}	—	90	125	µA
9	T	Tight regulation mode (mode =10)	I_{TR}	—	0.27	—	mA

2.14 SPI Characteristics

Table 22 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

Table 22. SPI Electrical Characteristic[1,2]

Num[3]	C	Characteristic[4]	Symbol	Min	Max	Unit
1	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
2	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc}
3	D	Enable lead time Master Slave	t_{Lead}	1/2 —	— —	t_{SPSCK} t_{cyc}
4	D	Enable lag time Master Slave	t_{Lag}	1/2 —	— —	t_{SPSCK} t_{cyc}
5	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$	1024 t_{cyc} —	ns
6	D	Data setup time (inputs) Master Slave	t_{SI}	15 15	— —	ns
7	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns
8	D	Slave access time[5]	t_a	—	1	t_{cyc}
9	D	Slave MISO disable time[6]	t_{dis}	—	1	t_{cyc}
10	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns
11	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns
12	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ —25	ns
13	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ —25	ns

[1] The performance of SPI2 depends on the configuration of power supply of the LCD pins. When the LCD pins are configured with full complementary drive enabled (FCDEN = 1, VSUPPLY = 11 and RVEN = 0), and VLL3 is driven with external VDD, the SPI2 can operate at the max performance as the above table. When the internal LCD charge pump is used to power the LCD pins, the SPI2 is configured with open-drain outputs. Its performance depends on the value of the external pullup resistor implemented, and the max operating frequency must be limited to 1 MHz.

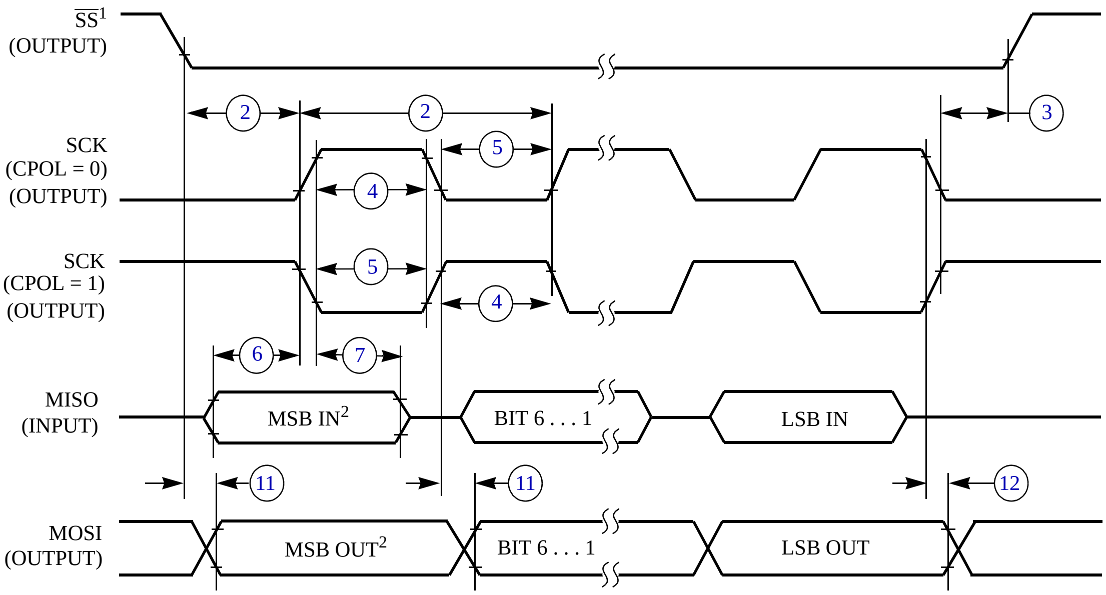
[2] SPI3 has open-drain outputs and its performance depends on the value of the external pullup resistor implemented.

[3] Refer to Figure 19 through Figure 22.

[4] All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

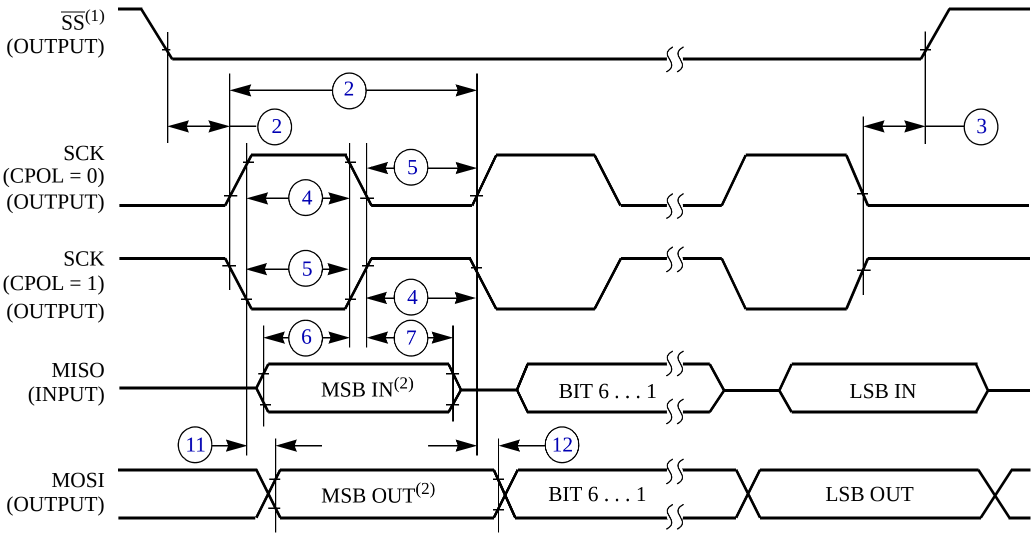
[5] Time to data active from high-impedance state.

[6] Hold time to high-impedance state.



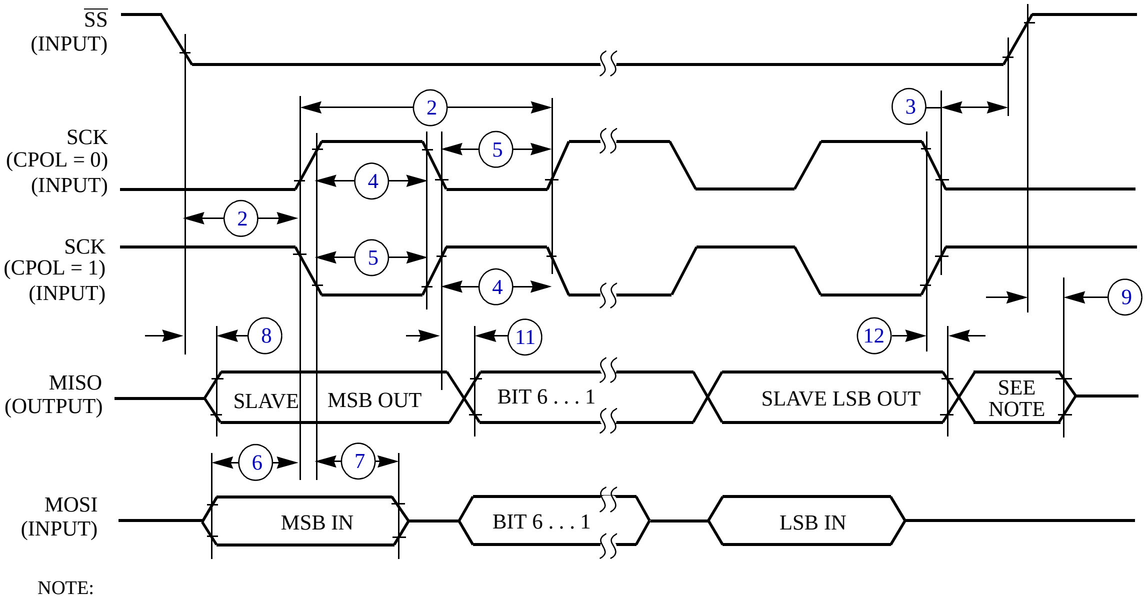
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

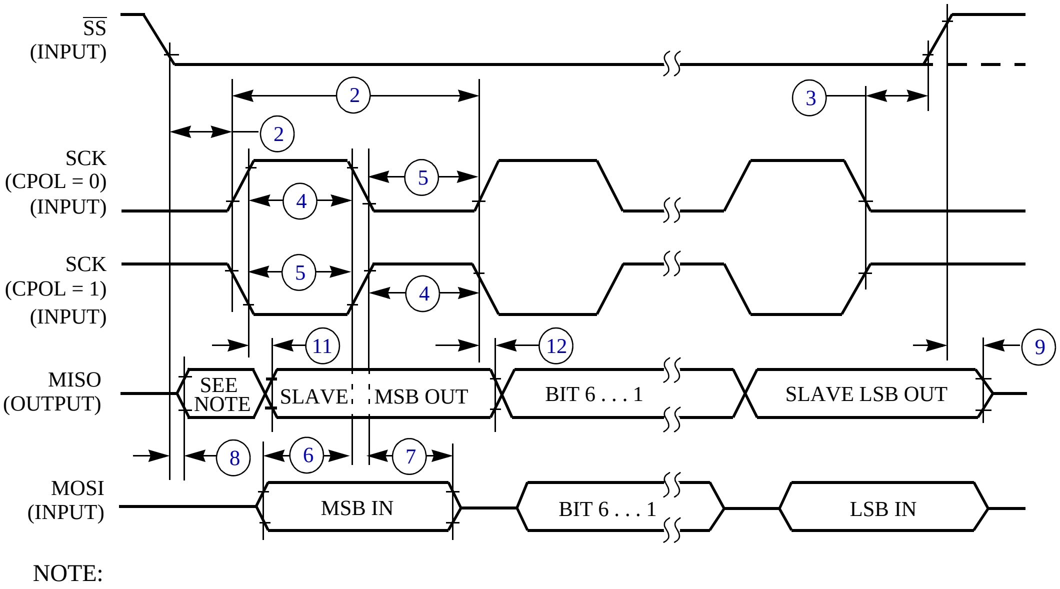
Figure 20. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 21. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 22. SPI Slave Timing (CPHA = 1)

2.15 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MCF51EM256 Series ColdFire Microcontroller Reference Manual*.

Table 23. Flash Characteristics

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8		3.6	V
2	D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
3	D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
4	D	Internal FCLK period ($1/f_{FCLK}$)	t_{Fcyc}	5		6.67	μs
5	P	Longword program time (random location)[2]	t_{prog}		9		t_{Fcyc}
6	P	Longword program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
7	P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
9		Longword program current[3]	R_{IDDBP}	—	9.7	—	mA
10		Page erase current[3]	R_{IDDPE}	—	7.6	—	mA
11	C	Program/erase endurance[4] T_L to T_H = –40 °C to 85 °C T = 25 °C		10,000 —	— 100,000	— —	cycles
12	C	Data retention[5]	t_{D_ret}	15	100	—	years

[1] The frequency of this clock is controlled by a software setting.

[2] These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

[3] The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

[4] **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

[5] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

2.16 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.16.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Mechanical Outline Drawings

3.1 80-pin LQFP Package

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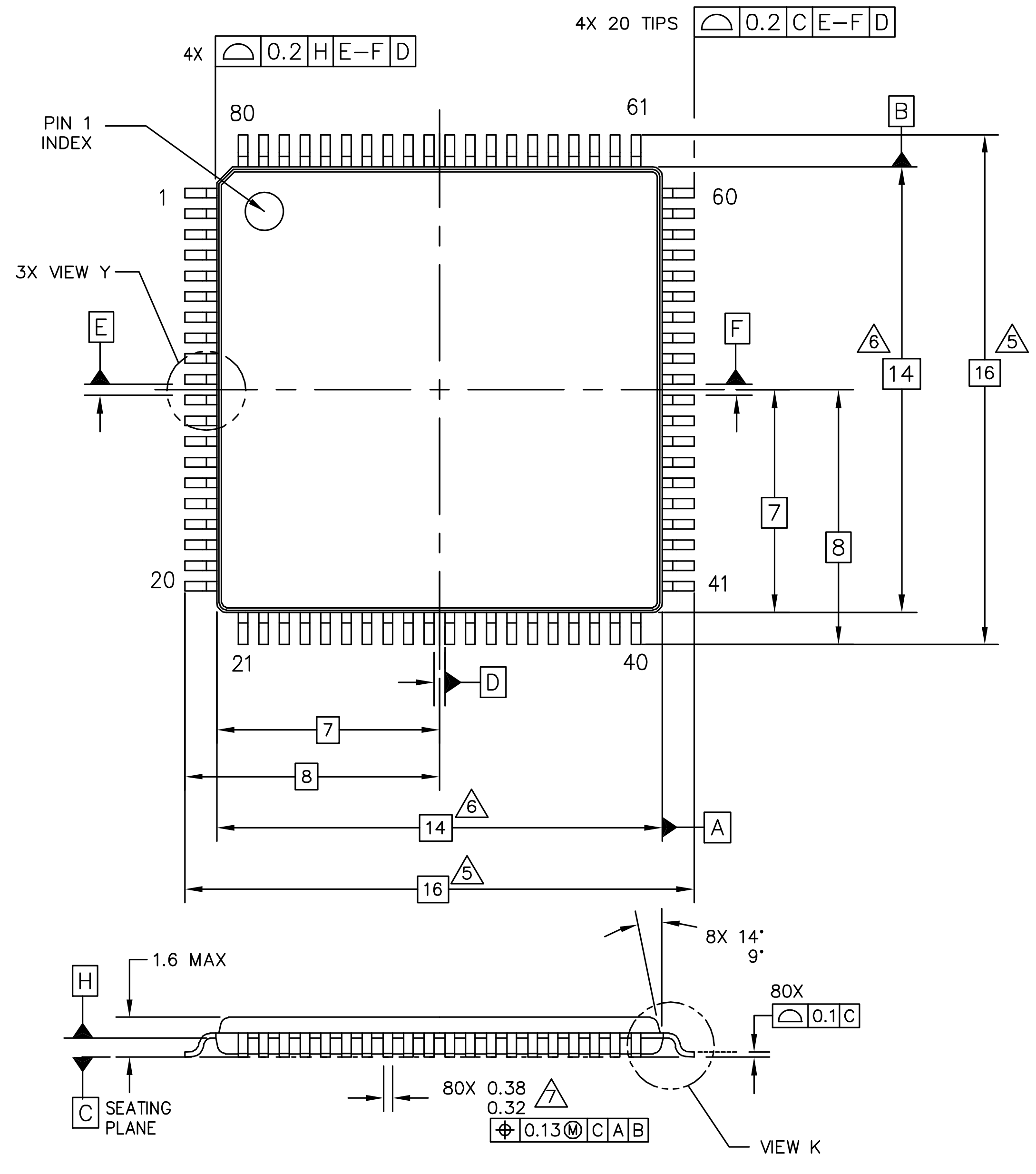

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03
	STANDARD: FREESCALE
	PACKAGE CODE: 8258 — SHEET: 1 OF 4

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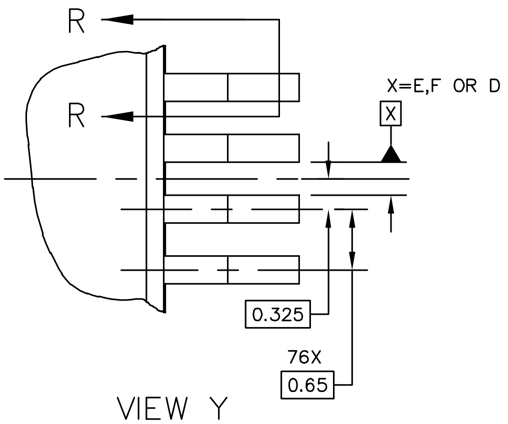
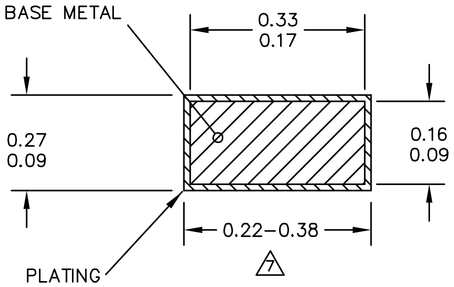
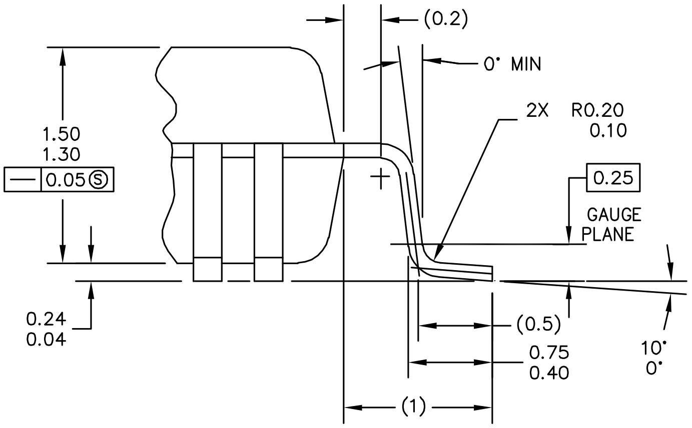


VIEW Y



SECTION R–R
ROTATED 90° CW



VIEW K

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03
	STANDARD: FREESCALE
	PACKAGE CODE: 8258 / SHEET: 2 OF 4

	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION : MILIMETER.

3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.

△5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

△6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 4

3.2 100-pin LQFP Package

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		PAGE: 983
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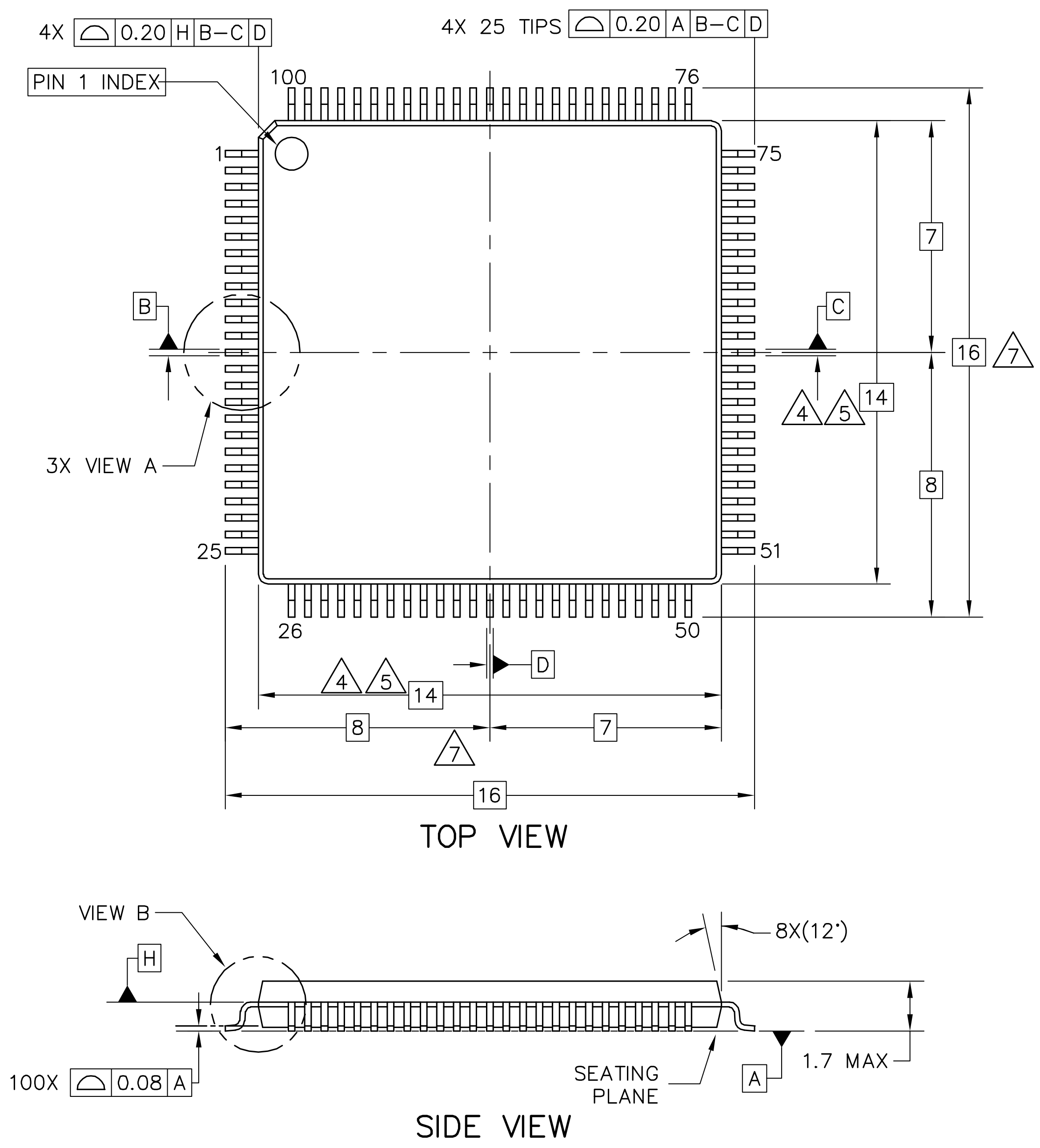
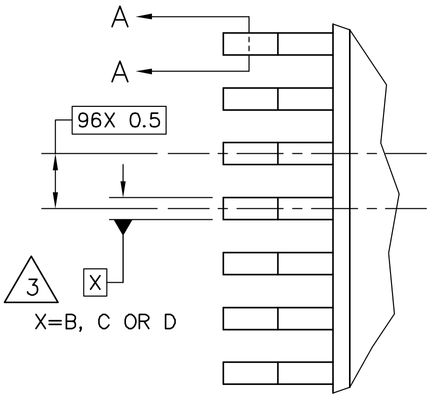
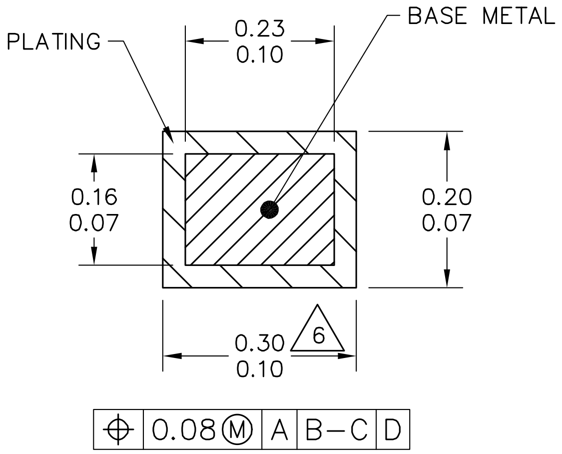


TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 1 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
	DO NOT SCALE THIS DRAWING	REV: H



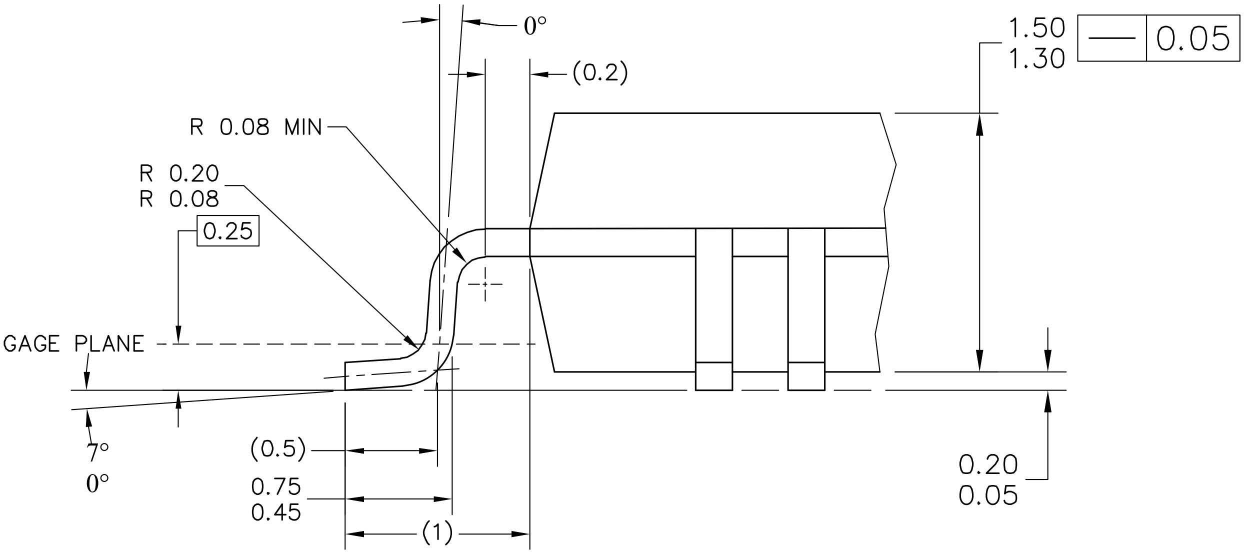
VIEW A



SECTION A–A

ROTATED 90° CW

100 PLACES



VIEW B

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02
	STANDARD: NON–JEDEC
	PACKAGE CODE: 8264 / SHEET: 2 OF 4

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W	
	PAGE:	983
DO NOT SCALE THIS DRAWING	REV:	H

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 3 OF 4

4 Revision History

Table 24. Revision History

Revision	Date	Description
1	10/15/2009	Initial public release.
2	4/29/2010	Updated teh descriptions of SPI in the Table 2. Changed the FSPIx to SPI16 to keep the term in accordance. Updated Figure 4 to Figure 8. Updated WI_{DD}, $S2I_{DD}$, $S3I_{DD}$ in the Table 11. Updated the ADC characteristics in the Table 13 to Table 15. Updated description of XOSC in the Section 2.9, "External Oscillator (XOSC) Characteristics." Updated t_{CSTL} in the Table 16. Updated the the classification of IBG and ITR to T and added Voltage reference output (factory trimmed) in the Table 21. Update SPI data in the Table 22.
3	8/9/2010	Updated the V_{DD} at 20 MHz maximum operation to 3.6 V. Updated the RI_{DD} (at Run supply current FEI mode, all module on), $S2I_{DD}$ and $S3I_{DD}$ at 3 V, $S3I_{DDLVD}$ in the Table 11. Updated ENOB at 16 bit single-ended mode in the Table 14.

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