Document Number: A2I25D025N
Rev. 0, 3/2015

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

The A2I25D025N wideband integrated circuit is designed with on-chip matching that makes it usable from 2100 to 2900 MHz. This multi-stage structure is rated for 26 to 32 V operation and covers all typical cellular base station modulation formats.

- Typical Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 56 mA, $I_{DQ2(A+B)}$ = 136 mA, P_{out} = 3.2 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2300 MHz	32.0	19.0	–46.7
2350 MHz	31.8	19.0	–47.1
2400 MHz	31.7	19.1	–47.5
2496 MHz	31.7	19.3	–47.3
2600 MHz	32.0	19.5	–47.1
2690 MHz	32.5	20.0	–46.8

Features

- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

A2I25D025NR1
A2I25D025GNR1

2100–2900 MHz, 3.2 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

TO-270WB-17 PLASTIC A2I25D025NR1

TO-270WBG-17 PLASTIC A2I25D025GNR1

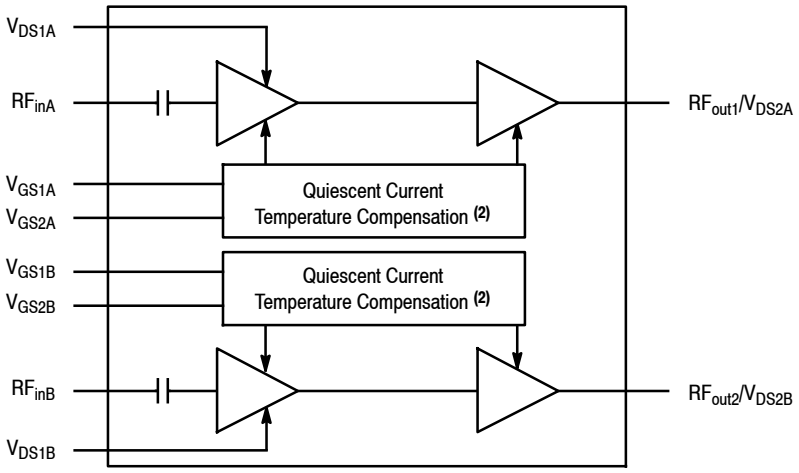
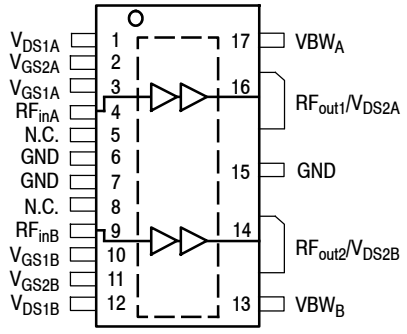


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 3.2 W, 2496 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 56 mA Stage 2, 28 Vdc, $I_{DQ2(A+B)}$ = 136 mA	$R_{\theta JC}$	 6.3 1.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	1B
Machine Model (per EIA/JESD22–A115)	A
Charge Device Model (per JESD22–C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 – Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 – On Characteristics					
Gate Threshold Voltage (4) (V_{DS} = 10 Vdc, I_D = 2.5 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ1(A+B)}$ = 59 mAdc)	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 59 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.6	5.3	6.1	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 16 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ2(A+B)}$ = 157 mAdc)	$V_{GS(Q)}$	—	1.9	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ2(A+B)}$ = 157 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.3	5.0	5.8	Vdc
Drain–Source On–Voltage (1) (V_{GS} = 10 Vdc, I_D = 200 mAdc)	$V_{DS(on)}$	0.1	0.22	1.5	Vdc
Functional Tests (2,3) (In Freescale Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 59 mA, $I_{DQ2(A+B)}$ = 157 mA, P_{out} = 3.2 W Avg., f = 2690 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	30.5	31.9	34.5	dB
Power Added Efficiency	PAE	18.0	19.7	—	%
Load Mismatch (In Freescale Production Test Fixture, 50 ohm system) $I_{DQ1(A+B)}$ = 59 mA, $I_{DQ2(A+B)}$ = 157 mA, f = 2600 MHz					
VSWR 10:1 at 32 Vdc, 36.3 W CW Output Power (3 dB Input Overdrive from 25 W CW Rated Power)	No Device Degradation				
Typical Performance (4) (In Freescale Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 56 mA, $I_{DQ2(A+B)}$ = 136 mA, 2300–2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	24	—	W
P_{out} @ 3 dB Compression Point, CW (5)	P3dB	—	35.5	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300–2690 MHz frequency range.)	Φ	—	–9.0	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	170	—	MHz
Quiescent Current Accuracy over Temperature (6) with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	 — —	 2.43 1.13	 — —	%
Gain Flatness in 390 MHz Bandwidth @ P_{out} = 3.2 W Avg.	G_F	—	0.8	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.036	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I25D025NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13–inch Reel	TO–270WB–17
A2I25D025GNR1		TO–270WBG–17

1. Each side of device measured separately.
2. Part internally input and output matched.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. All data measured in fixture with device soldered to heatsink.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W–CDMA single–carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
6. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1977 or AN1987.

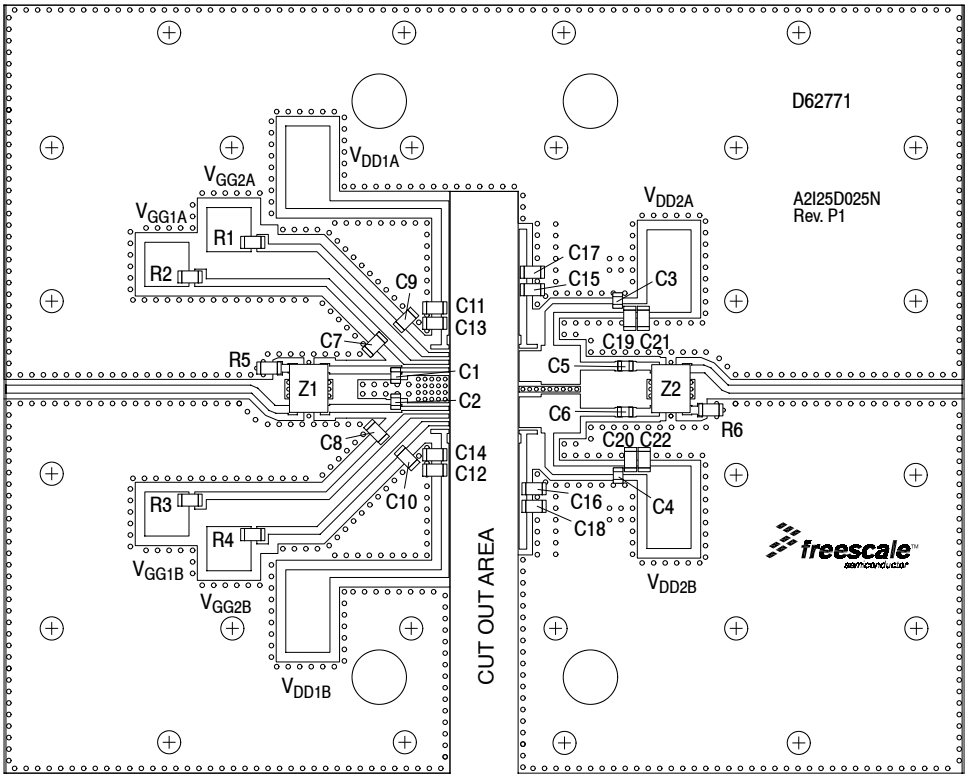
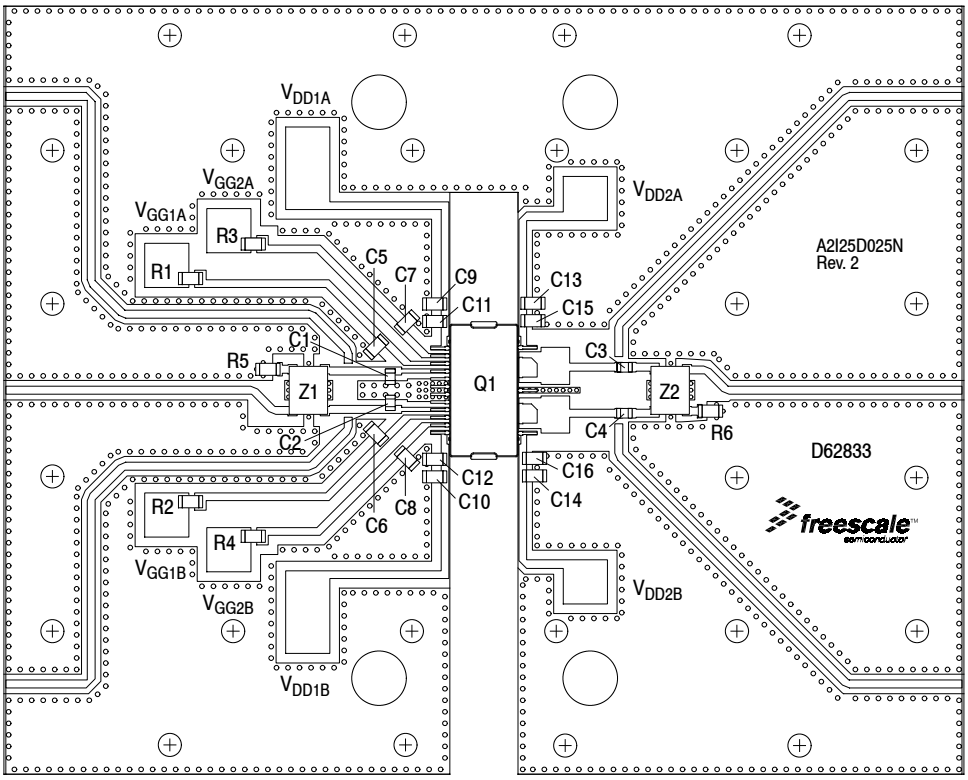


Figure 3. A2I25D025NR1 Production Test Circuit Component Layout

Table 7. A2I25D025NR1 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	0.9 pF Chip Capacitors	ATC600F0R9BT250XT	ATC
C3, C4	15 pF Chip Capacitors	ATC600F150JT250XT	ATC
C5, C6	30 pF Chip Capacitors	ATC600F300JT250XT	ATC
C7, C8, C9, C10, C15, C16, C19, C20	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C11, C12, C17, C18, C21, C22	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C13, C14	1 μF Chip Capacitors	GRM31MR71H105KA88L	Murata
R1, R4	4.7 KΩ Chip Resistors	CRCW12064K70FKEA	Vishay
R2, R3	2.2 kΩ, 1/4 W Chip Resistors	CRCW12062K20FKEA	Vishay
R5, R6	50 Ω, 10 W Chip Resistors	060120A15Z50-2	Anaren
Z1, Z2	2300–2900 MHz Band, 3 dB Hybrid Couplers	X3C26P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D62771	MTL



Note: All data measured in fixture with device soldered to heatsink.

Figure 4. A2I25D025NR1 Characterization Test Circuit Component Layout

Table 8. A2I25D025NR1 Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	0.9 pF Chip Capacitors	ATC600F0R9BT250XT	ATC
C3, C4	20 pF Chip Capacitors	ATC600F200JT250XT	ATC
C5, C6, C7, C8, C15, C16	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C9, C10, C13, C14	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C11, C12	1.0 μF Chip Capacitors	GRM31MR71H105KA88L	Murata
Q1	RF LDMOS Power Amplifier	A2I25D025NR1	Freescale
R1, R2	2.2 kΩ, 1/4 W Chip Resistors	CRCW12062K20FKEA	Vishay
R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
R5, R6	50 Ω, 8 W Chip Resistors	C8A50Z4A	Anaren
Z1, Z2	2300–2900 MHz Band, 3 dB Hybrid Couplers	X3C26P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D62833	MTL

TYPICAL CHARACTERISTICS

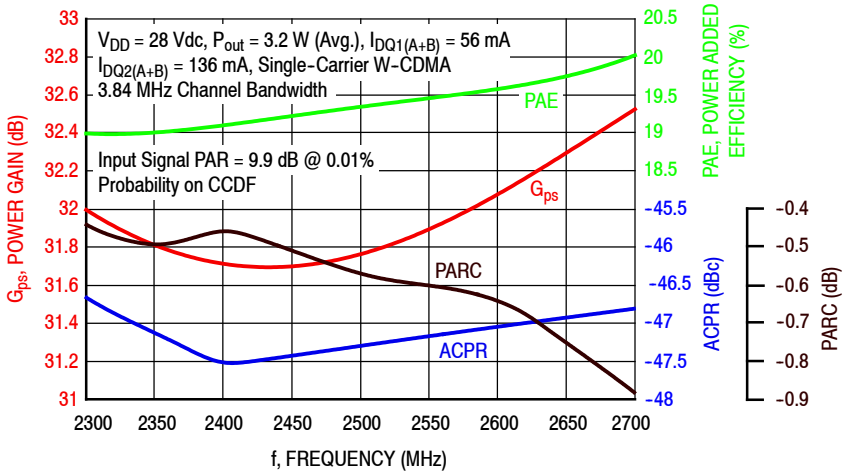


Figure 5. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 3.2 Watts Avg.

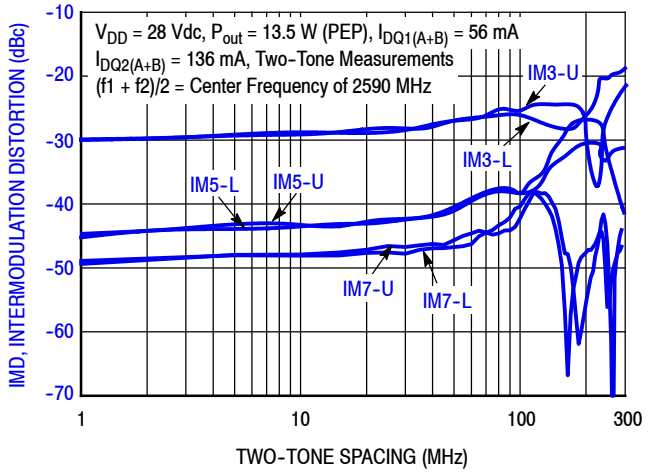


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

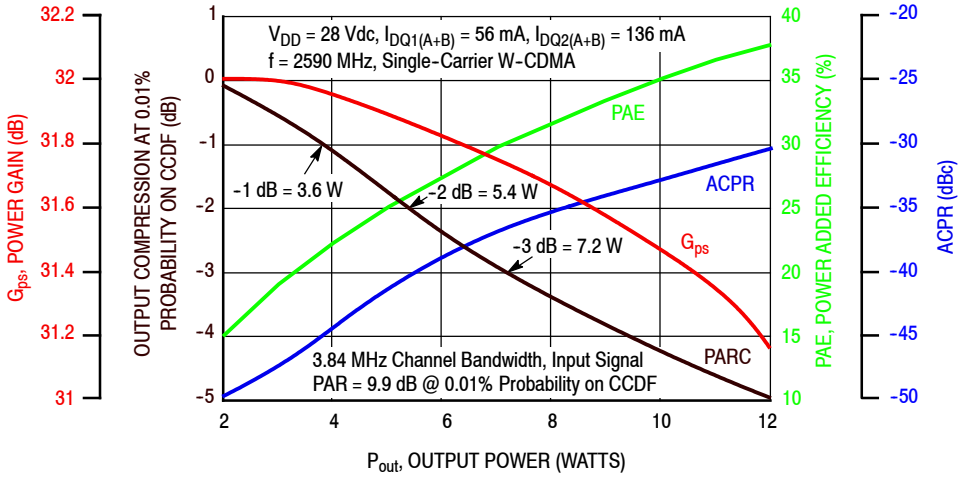


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

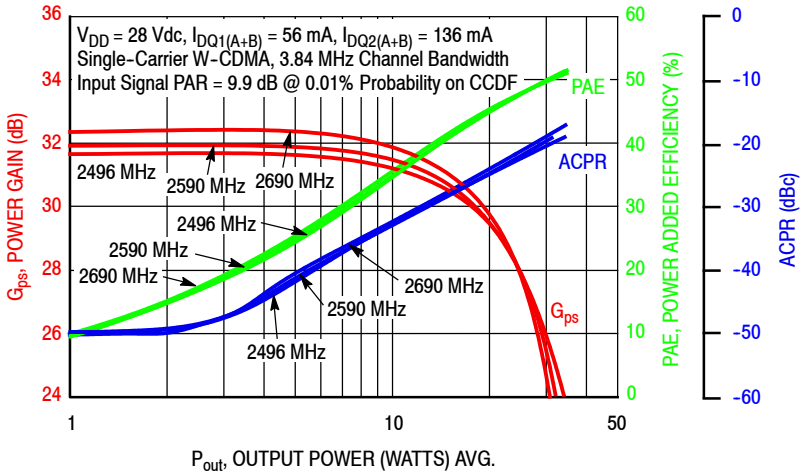


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power — 2496–2690 MHz

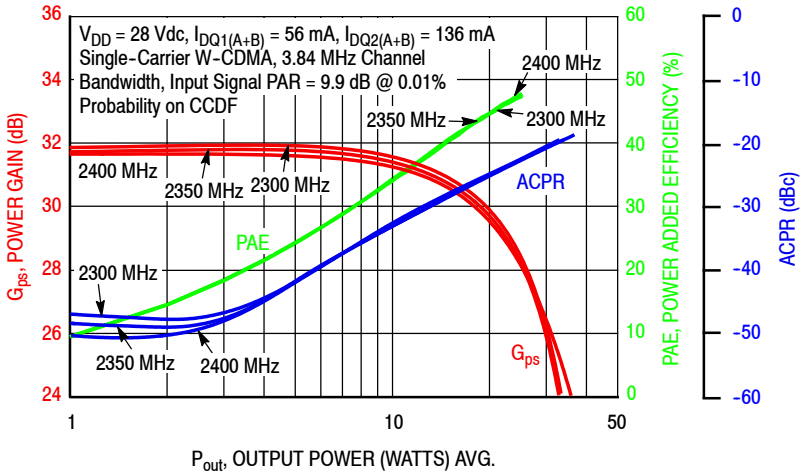
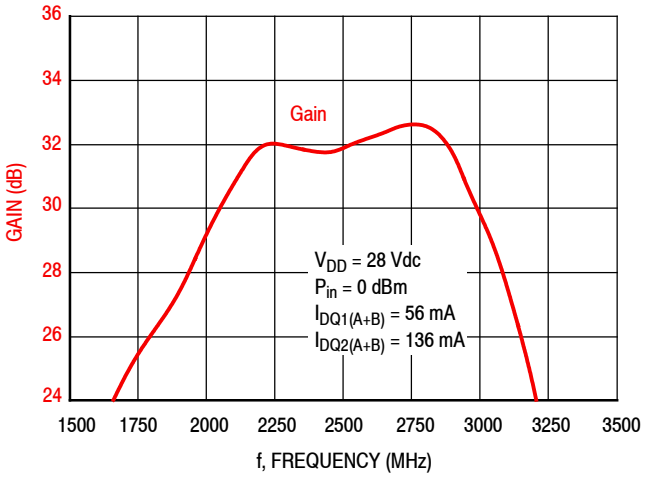


Figure 9. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power — 2300–2400 MHz



Note: Frequency response at band edges limited by hybrid couplers.

Figure 10. Broadband Frequency Response

Table 9. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, $I_{DQ1(A)}$ = 29 mA, $I_{DQ2(A)}$ = 75 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	35.0 + j9.89	36.0 – j13.0	10.4 – j9.63	30.4	42.6	18	59.0	–2
2350	43.2 + j11.9	41.9 – j16.8	10.8 – j11.0	30.5	42.5	18	56.9	–2
2400	45.8 + j23.1	43.5 – j26.0	10.6 – j8.31	30.7	42.3	17	57.2	–3
2496	43.9 + j37.9	40.7 – j37.0	10.1 – j8.37	31.0	42.6	18	60.5	–3
2590	33.1 + j43.7	31.4 – j41.4	9.32 – j9.38	31.0	42.7	19	60.9	–3
2690	29.5 + j41.2	28.0 – j37.3	7.84 – j9.97	30.7	42.7	18	60.8	–4

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	35.0 + j9.89	37.3 – j16.5	9.84 – j10.3	28.2	43.3	21	59.2	–6
2350	43.2 + j11.9	41.5 – j20.9	10.6 – j11.4	28.5	43.2	21	58.3	–7
2400	45.8 + j23.1	41.0 – j29.4	10.6 – j8.89	28.6	43.1	21	58.9	–8
2496	43.9 + j37.9	37.0 – j37.7	10.3 – j9.50	28.8	43.4	22	61.4	–8
2590	33.1 + j43.7	28.2 – j40.5	9.50 – j10.2	28.9	43.5	23	61.3	–8
2690	29.5 + j41.2	25.3 – j35.2	8.12 – j11.0	28.5	43.4	22	61.6	–11

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

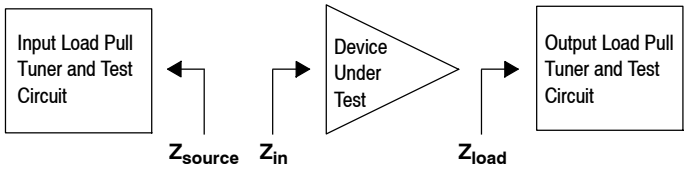


Table 10. Load Pull Performance — Maximum Power Added Efficiency Tuning

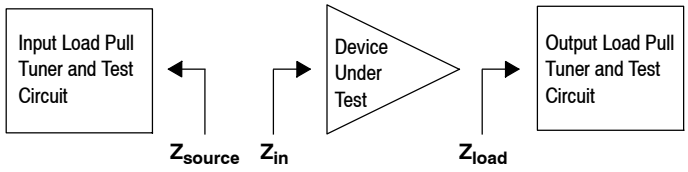
V_{DD} = 28 Vdc, $I_{DQ1(A)}$ = 29 mA, $I_{DQ2(A)}$ = 75 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Power Added Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	35.0 + j9.89	38.0 – j10.9	18.2 – j1.09	31.8	40.8	12	67.0	–6
2350	43.2 + j11.9	45.1 – j14.7	16.1 – j0.71	31.9	40.9	12	64.2	–6
2400	45.8 + j23.1	46.9 – j26.5	14.9 – j0.56	31.9	41.1	13	65.4	–5
2496	43.9 + j37.9	42.8 – j38.7	12.1 – j2.47	31.9	41.6	14	67.5	–6
2590	33.1 + j43.7	32.9 – j44.4	9.72 – j2.39	32.1	41.3	14	68.8	–7
2690	29.5 + j41.2	28.3 – j41.3	7.82 – j4.78	31.8	41.4	14	67.9	–9

			Max Power Added Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
2300	35.0 + j9.89	38.7 – j13.1	17.2 – j2.23	29.7	41.7	15	66.7	–11
2350	43.2 + j11.9	44.6 – j17.7	15.8 – j2.22	29.8	41.9	15	64.7	–9
2400	45.8 + j23.1	45.2 – j28.8	14.2 – j0.88	29.9	41.9	15	65.7	–10
2496	43.9 + j37.9	40.4 – j39.4	11.9 – j2.47	29.9	42.3	17	67.9	–11
2590	33.1 + j43.7	30.3 – j43.9	9.68 – j2.97	30.0	42.1	16	68.5	–12
2690	29.5 + j41.2	25.7 – j39.0	7.97 – j5.65	29.7	42.4	17	67.4	–15

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P1dB - TYPICAL LOAD PULL CONTOURS — 2590 MHz

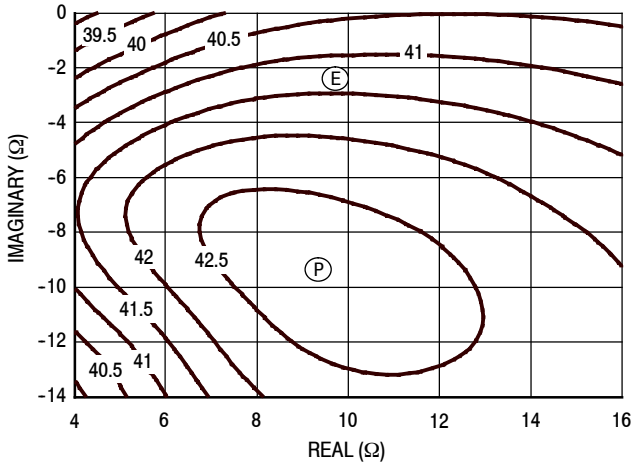


Figure 11. P1dB Load Pull Output Power Contours (dBm)

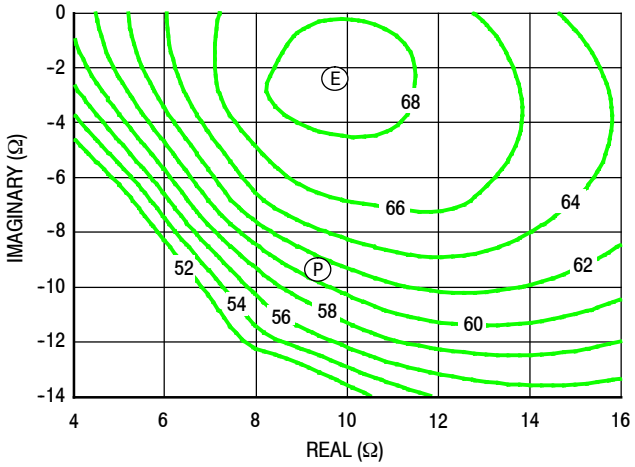


Figure 12. P1dB Load Pull Efficiency Contours (%)

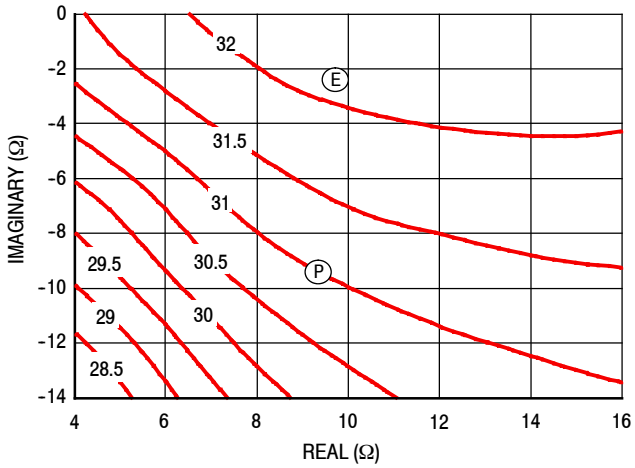


Figure 13. P1dB Load Pull Gain Contours (dB)

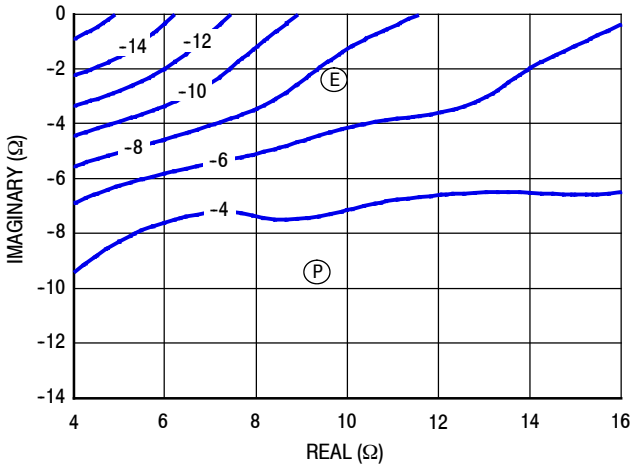


Figure 14. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Power Added Efficiency

Gain

Power Added Efficiency

Linearity

Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2590 MHz

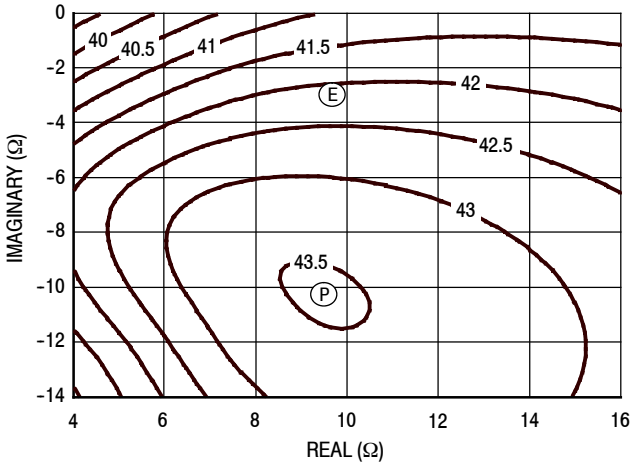


Figure 15. P3dB Load Pull Output Power Contours (dBm)

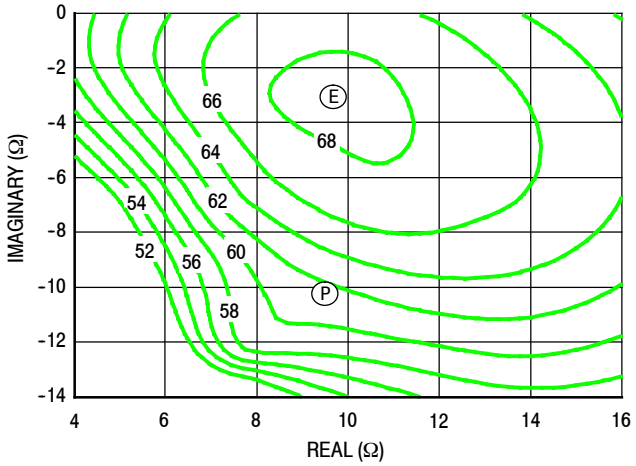


Figure 16. P3dB Load Pull Efficiency Contours (%)

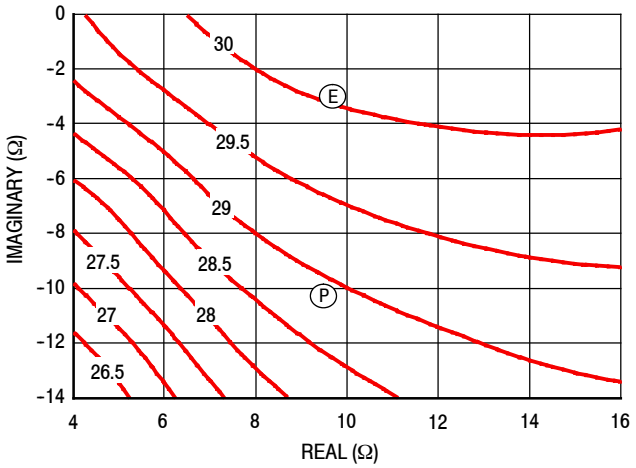


Figure 17. P3dB Load Pull Gain Contours (dB)

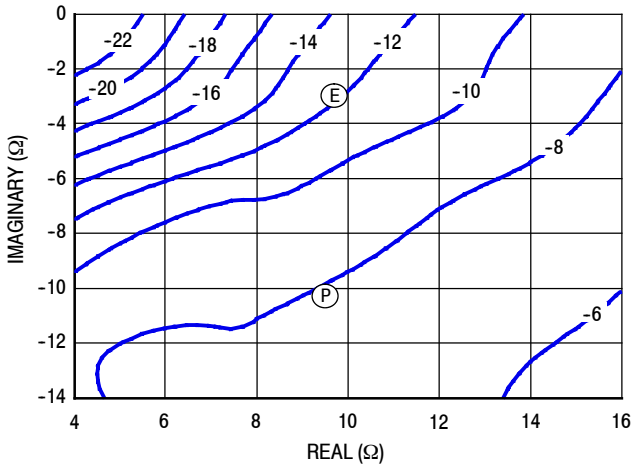
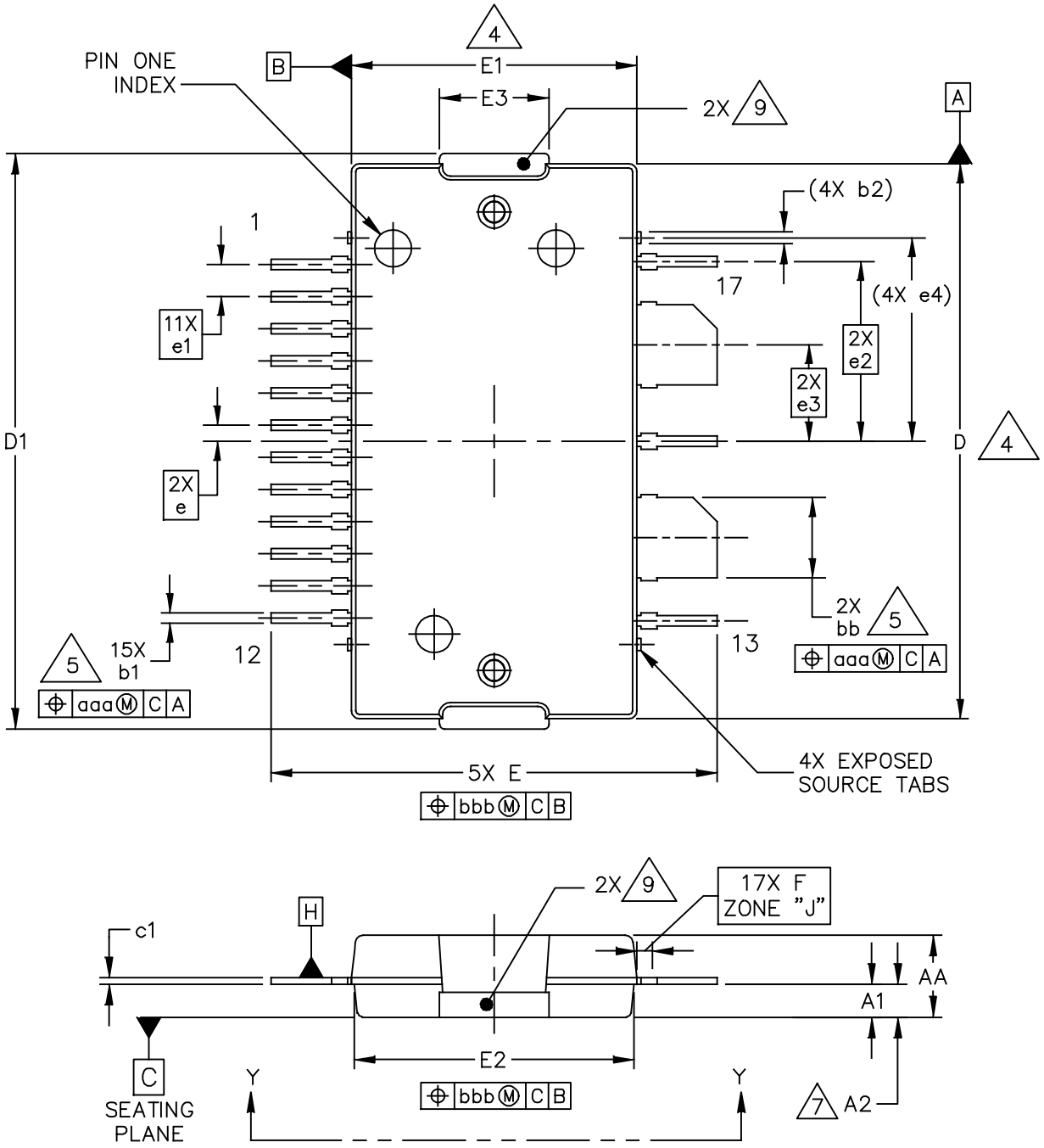


Figure 18. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Power Added Efficiency

Gain
Power Added Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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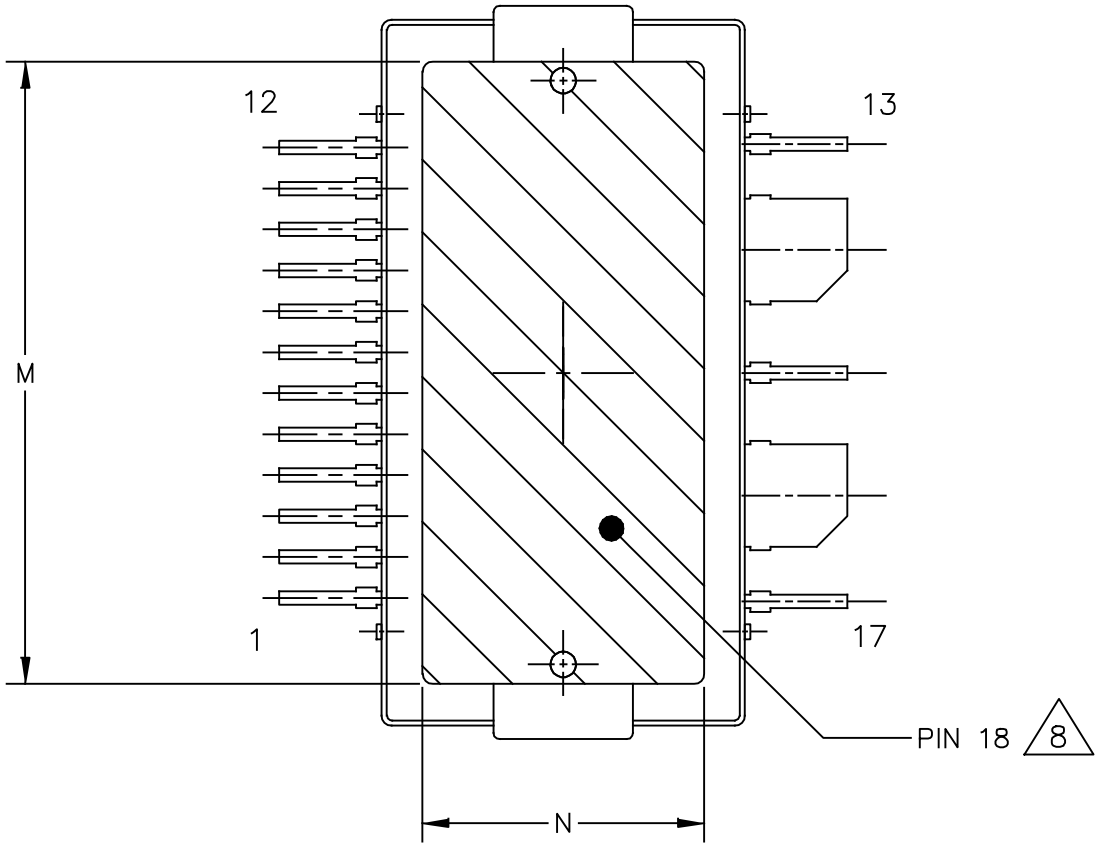

VIEW Y–Y

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

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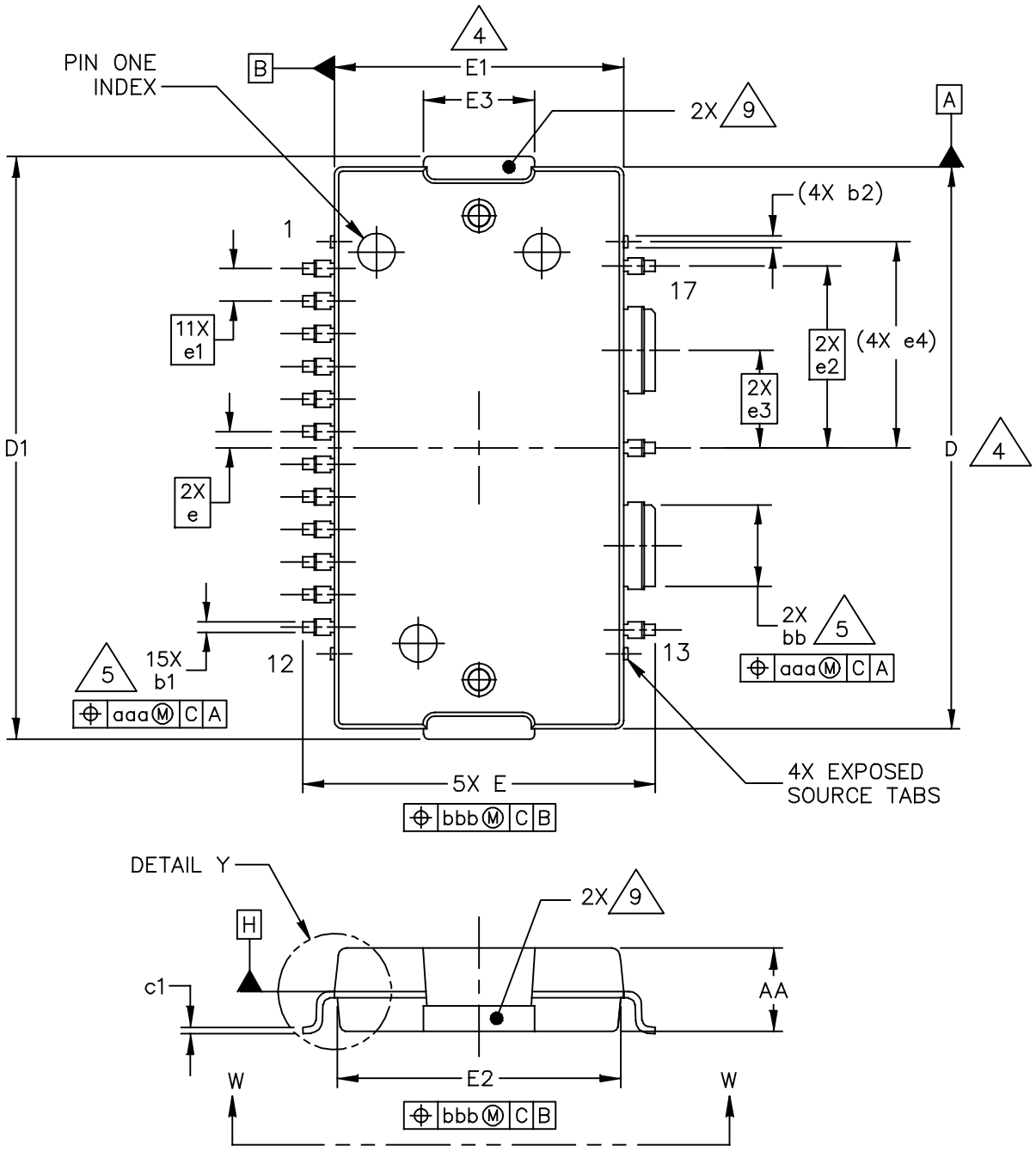

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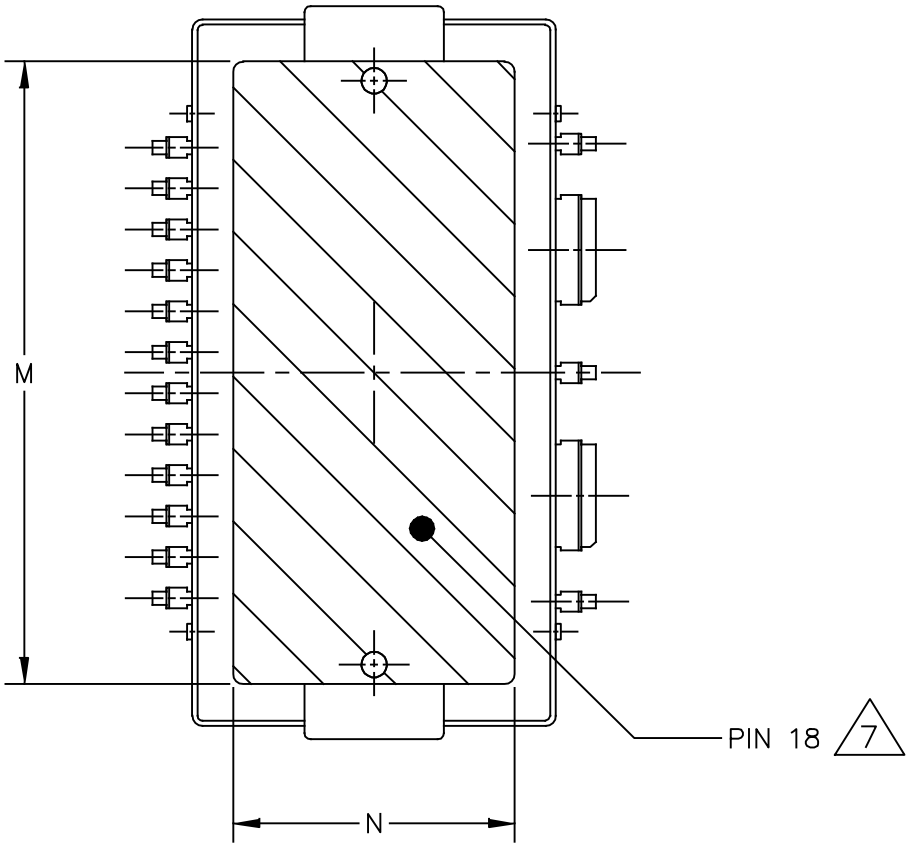
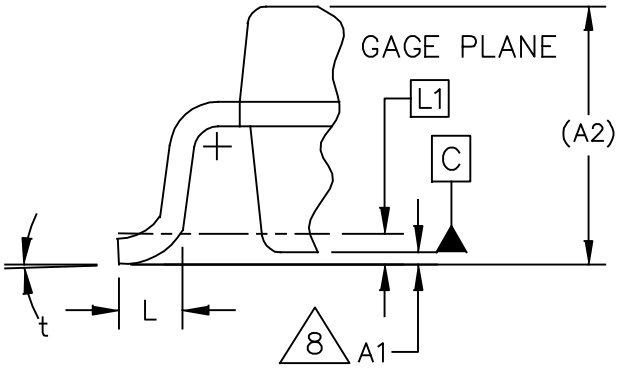


VIEW W–W



DETAIL "Y"

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2015	• Initial release of data sheet

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