LTM4601HV
$5V_{IN}$ to $28V_{IN}$, 12A Step-Down µModule Regulator

DESCRIPTION

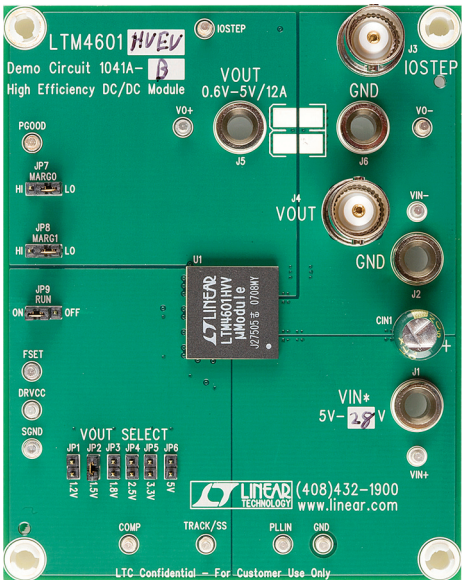
Demonstration circuit DC1041A-B features the LTM®4601HVEV, a 12A high efficiency, high density switch mode step-down converter. The input voltage range is from 4.5V to 28V. The output voltage is jumper selectable for popular voltages from 0.6V to 5V. The PLLIN pin supports synchronizing the µModule® regulator to an external clock. The TRACK/SS pin allows the user to program output ramp-up and ramp-down rates which may coincidentally or ratiometrically track with another supply's output if desired. Output voltage margining of ±5% from the nominal value is available via the margin control pins MARG0 and MARG1. The LTM4601HV data sheet must be read in conjunction with this demo manual prior to working on or modifying demo circuit DC1041A-B.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Input Voltage Range		4.5V to 28V
Output Voltage V_{OUT}	Jumper Selectable (Open for 0.6V)	1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V
Maximum Continuous Output Current	Derating is Necessary for Certain V_{IN}, V_{OUT} and Thermal Conditions	12A DC
Default Operating Frequency		800kHz
External Synchronous Clock Frequency Range	Refer to Data Sheet for Details	560kHz to 1000kHz
Efficiency	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A	83%, See Figure 2

BOARD PHOTO



QUICK START PROCEDURE

Demonstration circuit DC1041A-B is an easy way to evaluate the performance of the LTM4601. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. With the power supply off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0A and power supply voltage within the LTM4601's operating input voltage range.
2. Place jumpers in the following positions for a typical $1.5V_{OUT}$ application:

MARG0	MARG1	RUN	V_{OUT} SELECT
LO	LO	ON	1.5V

3. Turn on the power at the input. The output voltage should be 1.5V ±1%.
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters. Output ripple should be measured at J4 with a BNC cable.
5. For optional load transient test, apply an adjustable pulse signal between IOSTEP (E3) and GND pins. Pulse amplitude sets the current step. The pulse signal should have very small duty cycle (<15%) to limit the thermal stress on the transient load circuit. The output transient current can be monitored at BNC connector J3 (10mV/A).
6. For Margining function test, place jumper MARG0 and MARG1 in the configurations shown in the following table, measure the output voltage at J4.

MARG1	MARG0	ΔV_{OUT}
LO	LO	0
LO	HI	5%
HI	LO	–5%
HI	HI	0

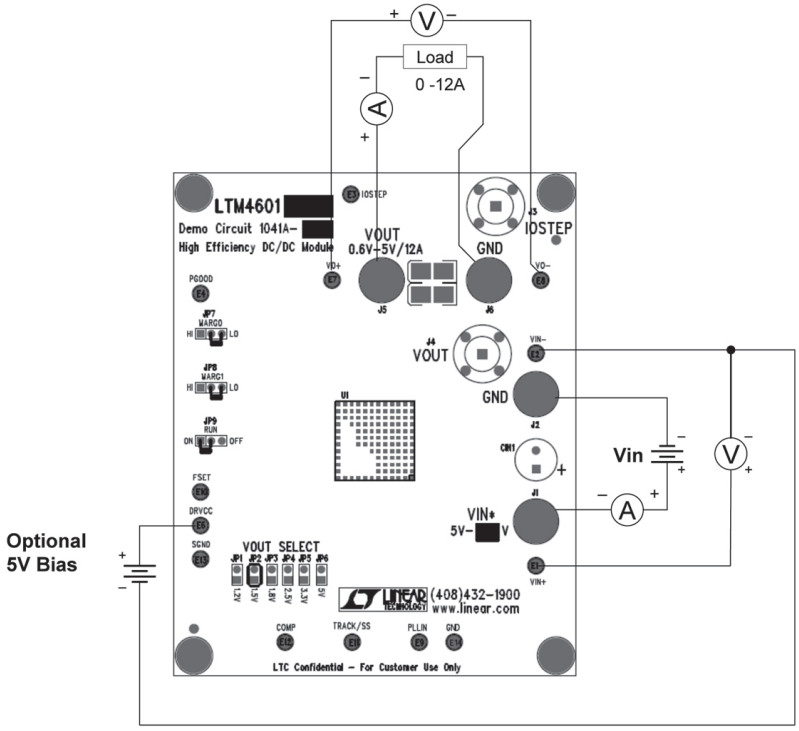


Figure 1. Demo Board Setup

QUICK START PROCEDURE

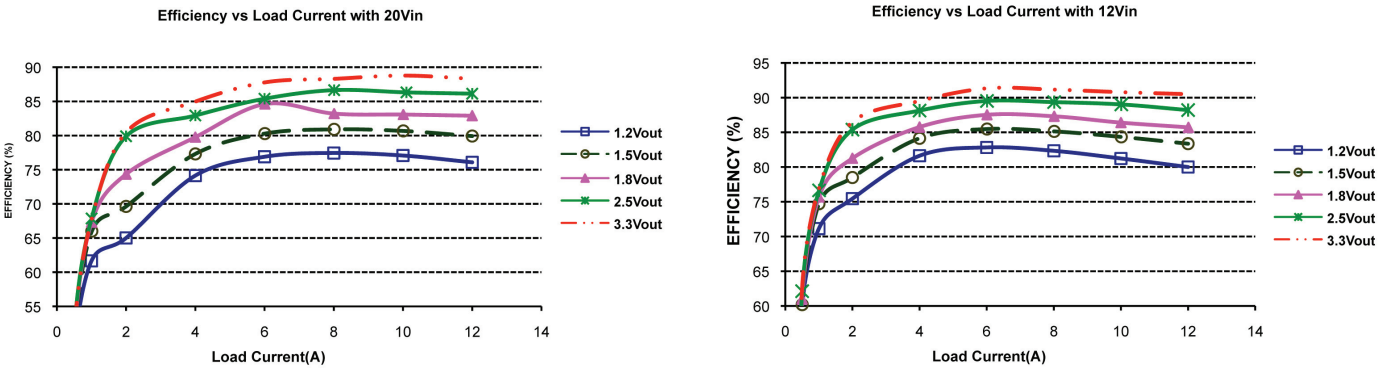
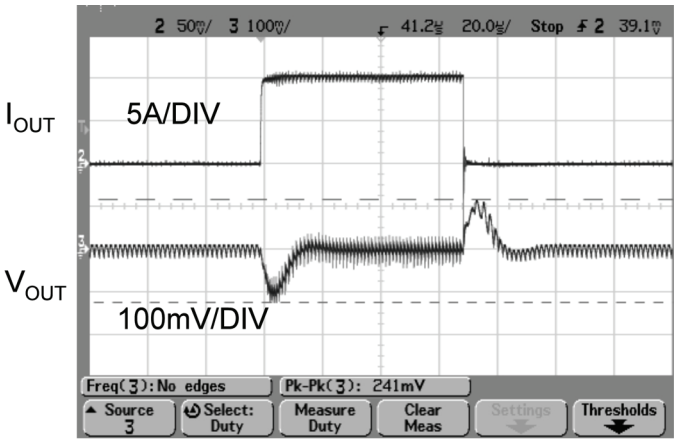


Figure 2. Measured Supply Efficiency with Different V_{IN} and V_{OUT}



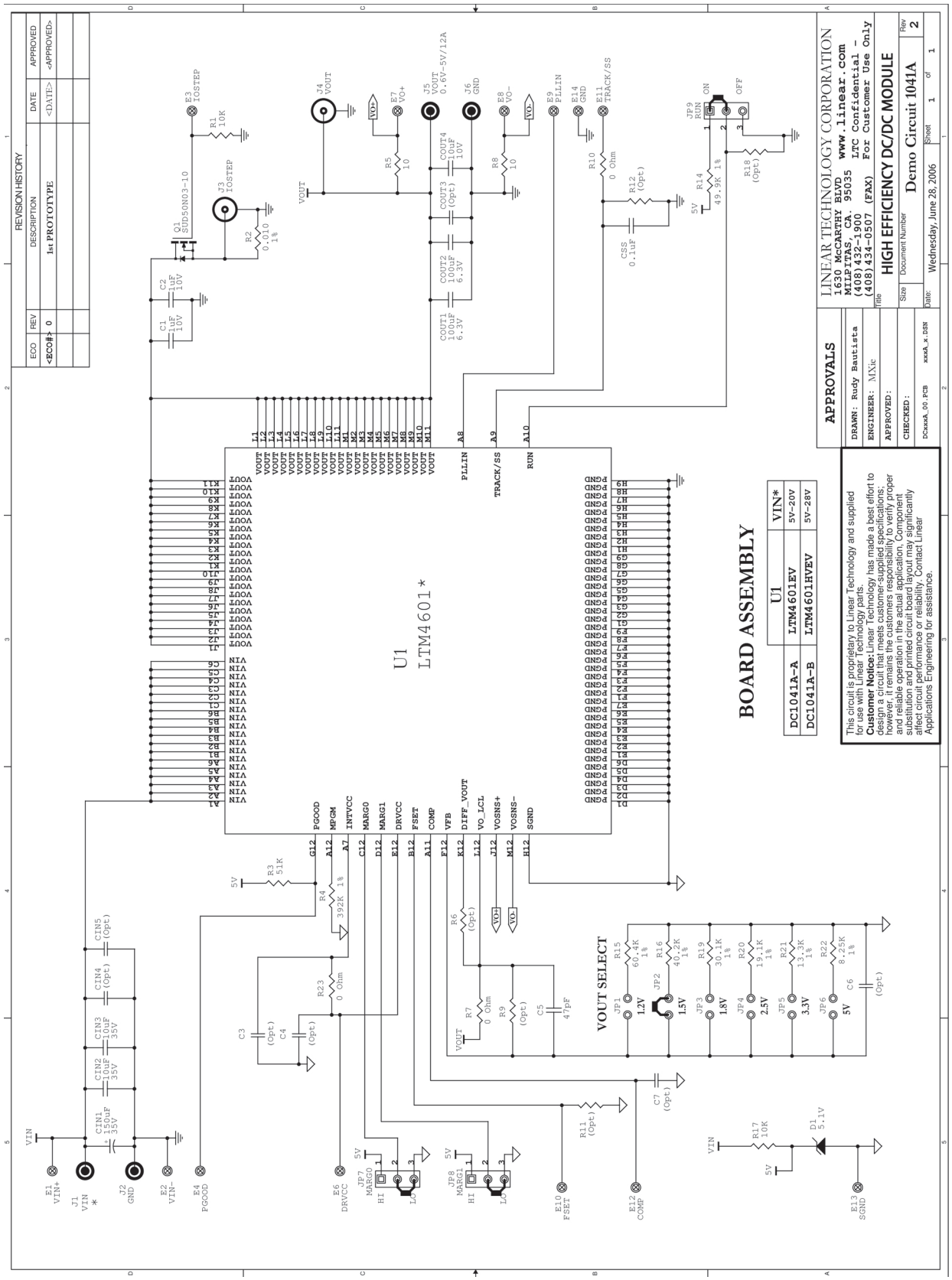
V_{IN} = 12V
V_{OUT} = 1.5V
0A TO 10A LOAD STEP
C_{OUT} = 1 × 22µF CERAMIC, 2 × 100µF CERAMIC, C5 = 47pF

Figure 3. Measured Load Transient Response (0A to 10A Step)

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN1	Cap., Alum 150µF 35V 20%	Sanyo 35ME150WXV (now SUNCON 35ME150WXV)
2	2	CIN2, CIN3	Cap., X7R 10µF 35V 20%	Taiyo Yuden GMK316BJ106ML-T
3	2	COUT1, COUT2	Cap., X5R 100µF 6.3V 20%	Taiyo Yuden JMK432BJ107MU-T
4	1	COUT4	Cap., X5R 10µF 10V 10%	Taiyo Yuden LMK316BJ106KL-T
5	1	CSS	Cap., X7R 0.1µF 16V 20%	AVX 0603YC104MAT2A
6	1	R4	Res., Chip 392k 0.1W 1%	AAC CR16-3923FM
7	2	R8,R5	Res., Chip 10Ω 0.1W 5%	AAC CR16-100JM
8	1	R19	Res., Chip 30.1k 0.06W 1%	AAC CR16-3012FM
9	1	U1	I.C., Volt. Reg.	Linear Technology Corp. LTM4601EV
Additional Demo Board Circuit Components				
1	0	CIN4, CIN5	Cap., 1206 TBD	
2	0	COUT3	Cap., 1210 TBD	
3	0	C3, C4, C5, C6, C7	Cap., 0603 TBD	
4	2	C1, C2	Cap., X5R 1µF 10V 10%	Taiyo Yuden LMK107BJ105KA
5	1	D1	Zener Diode, 5.1V	On Semi. MMBZ5231B
6	1	Q1	MOSFET, N-Channel 30V	Siliconix SUD50N03-10
7	0	R6, R9, R11, R12, R18	Res., 0603 TBD	
8	2	R17, R1	Res., Chip 10k 0.1W 5%	AAC CR16-103JM
9	1	R2	Res., LRC 0.010Ω 0.25W 1%	IRC LRF1206-01-R010-F
10	1	R3	Res., Chip 51k 0.1W 5%	AAC CR16-513JM
11	3	R7, R10, R23	Res/Jumper, Chip 0Ω 1/16W 1A	AAC CJ06-000M
12	1	R14	Res., Chip 49.9k 0.06W 1%	AAC CR16-4992FM
13	1	R15	Res., Chip 60.4k 0.1W 1%	AAC CR16-6042FM
14	1	R16	Res., Chip 40.2k 0.1W 1%	AAC CR16-4022FM
15	1	R20	Res., Chip 19.1k 0.1W 1%	AAC CR16-1912FM
16	1	R21	Res., Chip 13.3k 0.1W 1%	AAC CR16-1332FM
17	1	R22	Res., Chip 8.25k 0.1W 1%	AAC CR16-8251FM

SCHEMATIC DIAGRAM



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