19-3813; Rev 0; 9/05

EVALUATION KIT AVAILABLE

Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

General Description

The MAX5955 and MAX5956 are +1V to +13.2V dual hot-swap controllers with independent on/off control for complete protection of dual-supply systems. They allow the safe insertion and removal of circuit cards into live backplanes. The MAX5955 and MAX5956 operate down to 1V provided one of the inputs is above 2.7V.

The discharged filter capacitors of the circuit card provide low impedance to the live backplane. High inrush currents from the backplane to the circuit card can burn up connectors and components, or momentarily collapse the backplane power supply leading to a system reset. The MAX5955 and MAX5956 hot-swap controllers prevent such problems by gradually ramping up the output voltage and regulating the current to a preset limit when the board is plugged in, allowing the system to stabilize safely. After the startup cycle is completed, two on-chip comparators provide VariableSpeed/BiLevel™ protection against short-circuit and overcurrent faults, as well as immunity against system noise and load transients. In the event of a fault condition, the load is disconnected. The MAX5955B and MAX5956B must be unlatched after a fault, and the MAX5955A and MAX5956A automatically restart after a fault.

The MAX5955 and MAX5956 integrate an on-board charge pump to drive the gates of low-cost, external n-channel MOSFETs. The devices offer integrated features like startup current regulation and current glitch protection to eliminate external timing resistors and capacitors. These devices provide open-drain status outputs, an adjustable startup timer, and adjustable current limits. The MAX5955 provides output undervoltage/overvoltage protection for each channel, while the MAX5956 provides undervoltage/overvoltage monitoring for each channel.

The MAX5955 and MAX5956 are available in a space-saving 16-pin QSOP package.

Applications

Base Station Line Cards

Network Switches, Routers, Hubs

Solid-State Circuit Breakers

RAID

Power-Supply Sequencing

Hot Plug-In Daughter Cards

Portable Computer Device Bays (Docking Stations)

Variable Speed/BiLevel is a trademark of Maxim Integrated Products, Inc.

Features

- **Safe Hot Swap for +1V to +13.2V Power Supplies with V_{IN1} or V_{IN2} ≥ 2.7V**
- **Independent On/Off Control for Each Channel**
- **Internal Charge Pumps Generate n-Channel MOSFET Gate Drives**
- **Inrush Current Regulated at Startup**
- **Circuit-Breaker Function**
- **Adjustable Circuit Breaker/Current-Limit Threshold from 25mV to 100mV**
- **VariableSpeed/BiLevel Circuit Breaker Response**
- **Autoretry or Latched Fault Management**
- **Status Outputs Indicate Fault/Safe Condition**
- **Output Undervoltage and Overvoltage Monitoring or Protection**

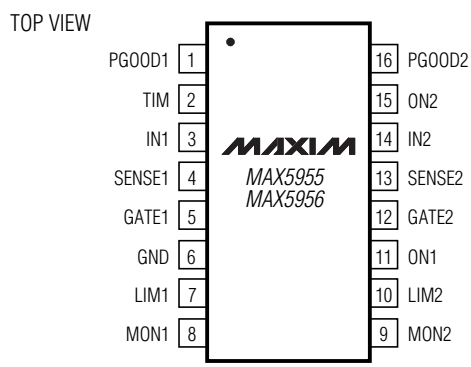
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5955AEEE	-40°C to +85°C	16 QSOP
MAX5955AEEE+	-40°C to +85°C	16 QSOP
MAX5955AUEE	0°C to +85°C	16 QSOP
MAX5955AUEE+	0°C to +85°C	16 QSOP
MAX5955BEEE	-40°C to +85°C	16 QSOP
MAX5955BEEE+	-40°C to +85°C	16 QSOP
MAX5955BUEE	0°C to +85°C	16 QSOP
MAX5955BUEE+	0°C to +85°C	16 QSOP

+Denotes lead-free package.

Ordering Information continued at end of data sheet.
Selector Guide and Typical Operating Circuit appear at end of data sheet.

Pin Configuration



Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

ABSOLUTE MAXIMUM RATINGS

IN_ to GND .....+14V
GATE_ to GND .....-0.3V to ($V_{IN\_}$ + 6.2V)
ON_, PGOOD_, TIM to GND .....-0.3V to the higher of (V_{IN1} + 0.3V) and (V_{IN2} + 0.3V)
SENSE_, MON_, LIM_ to GND .....-0.3V to ($V_{IN\_}$ + 0.3V)
Current into Any Pin .....±50mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range
MAX59_ _ _U_ _ .....0°C to +85°C
MAX59_ _ _E_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN\_}$ = +1V to +13.2V provided at least one supply is higher than +2.7V, V_{ON1} = V_{ON2} = +2.7V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{IN1} = +5V, V_{IN2} = +3.3V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
IN_ Input Voltage Range	V_{IN}	Other V_{IN} ≥ +2.7V		1.0		13.2	V
Supply Current	I_{IN}	I_{IN1} + I_{IN2}, V_{IN1} = +5V, V_{IN2} = +3.3V			1.2	2.3	mA
CURRENT CONTROL							
Slow-Comparator Threshold ($V_{IN\_}$ - $V_{SENSE\_}$) (Note 2)	$V_{SC,TH}$	LIM = GND	T_A = +25°C	22.5	25	27.5	mV
			T_A = -40°C to +85°C	20.5		27.5	
		R_{LIM} = 300kΩ		80	100	130	
Slow-Comparator Response Time (Note 3)	t_{SCD}	1mV overdrive			3		ms
		10mV overdrive			110		µs
Fast-Comparator Threshold ($V_{IN\_}$ - $V_{SENSE\_}$)	$V_{SU,TH}$	During startup			2 x $V_{SC,TH}$		mV
	$V_{FC,TH}$	$V_{IN\_}$ - $V_{SENSE\_}$; normal operation			4 x $V_{SC,TH}$		
Fast-Comparator Response Time ($V_{IN\_}$ - $V_{SENSE\_}$)	t_{FCD}	10mV overdrive, from overload condition			260		ns
SENSE Input Bias Current	$I_{B\ SENSE}$	$V_{SENSE\_}$ = $V_{IN\_}$			0.03	1	µA
MOSFET DRIVER							
Startup Period (Note 4)	t_{START}	R_{TIM} = 100kΩ		6	10.8	16	ms
		R_{TIM} = 4kΩ (minimum value)		0.31	0.45	0.58	
		TIM floating		4	9	17	
Average Gate Current	I_{GATE}	Charging, $V_{GATE\_}$ = +5V, $V_{IN\_}$ = +10V (Note 5)		65	100	130	µA
		Discharging, triggered by a fault or when $V_{ON\_}$ < 0.875V			3		mA
Gate-Drive Voltage	V_{DRIVE}	$V_{GATE\_}$ - $V_{IN\_}$, $I_{GATE\_}$ < 1µA	$V_{IN\_}$ = 3V to 13.2V	4.8	5.4	6.0	V
			$V_{IN\_}$ = 2.7V to 3.0V	4.1	5.0	6.0	
ON_ COMPARATOR							
ON_ Threshold	$V_{ON\_,TH}$	Low to high		0.85	0.875	0.90	V
		Hysteresis			25		mV
ON_ Propagation Delay		10mV overdrive			50		µs

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = +1V to +13.2V provided at least one supply is higher than +2.7V, V_{ON1} = V_{ON2} = +2.7V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{IN1} = +5V, V_{IN2} = +3.3V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ON_ Input Bias Current	I_{BON}	V_{IN1} = V_{IN2} = +13.2V	$V_{ON\_}$ < 4.5V		0.03		µA
			$V_{ON\_}$ > 4.5V		100		
			$V_{ON\_}$ = 4.5V		0.03	1	
ON_ Pulse-Width Low	$t_{UNLATCH}$	To unlatch after a latched fault		100			µs
DIGITAL OUTPUT (PGOOD_)							
Output Leakage Current		$V_{PGOOD\_}$ = 13.2V				1	µA
Output Voltage Low	V_{OL}	I_{SINK} = 1mA				0.4	V
PGOOD_ Delay	t_{PGDLY}	After t_{START}, MON_ = $V_{IN\_}$			0.75		ms
OUTPUT VOLTAGE MONITORS (MON1, MON2)							
MON_ Trip Threshold	V_{MON}	Overvoltage		657	687	707	mV
		Undervoltage		513	543	563	
MON_ Glitch Filter					20		µs
MON_ Input Bias Current		$V_{MON\_}$ = 600mV			0.03		µA
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	V_{UVLO}	Startup is initiated when this threshold is reached by V_{IN1} or V_{IN2}, $V_{ON\_}$ > 0.875V		2.10	2.4	2.67	V
		Hysteresis			100		mV
UVLO Glitch Filter Reset Time		$V_{IN\_}$ toggled below UVLO to unlatch after a fault		100			µs
UVLO to Startup Delay	$t_{D,UVLO}$	$V_{IN\_}$ step from 0 to 2.8V		20	37.5	66	ms
SHUTDOWN LATCH/RESTART							
Autoretry Delay	t_{RETRY}	Delay time to restart after fault shutdown			64 x t_{START}		ms

Note 1: All devices are 100% tested at T_A = +25°C and T_A = +85°C. Limits at T_A = 0°C and -40°C are guaranteed by design.

Note 2: The MAX5955/MAX5956 slow-comparator threshold is adjustable. $V_{SC,TH}$ = R_{LIM} × 0.25µA + 25mV (see the *Typical Operating Characteristics*).

Note 3: The current-limit slow-comparator response time is weighted against the amount of overcurrent; the higher the overcurrent condition, the faster the response time (see the *Typical Operating Characteristics).*

Note 4: The startup period (t_{START}) is the time during which the slow comparator is ignored and the device acts as a current-limiter by regulating the sense current with the fast comparator (see the *Startup Period* section).

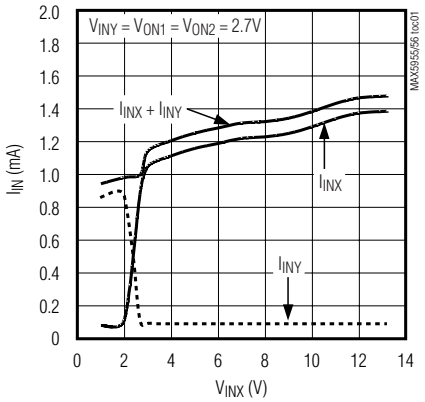
Note 5: The current available at GATE is a function of V_{GATE} (see the *Typical Operating Characteristics*).

Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

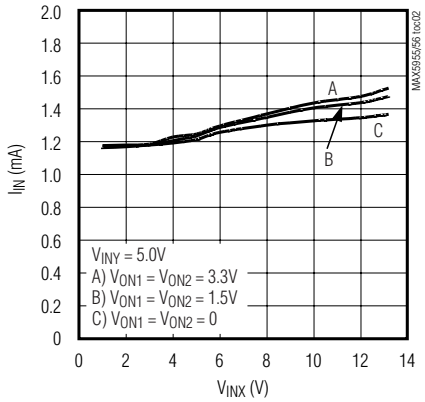
Typical Operating Characteristics

(Typical Operating Circuits, Q1 = Q2 = Fairchild FDB7090L, V_{IN1} = +5V, V_{IN2} = +3.3V, V_{ON1} = V_{ON2} = +2.7V, T_A = +25°C, unless otherwise noted. Channels 1 and 2 are identical in performance. Where characteristics are interchangeable, channels 1 and 2 are referred to as X and Y.)

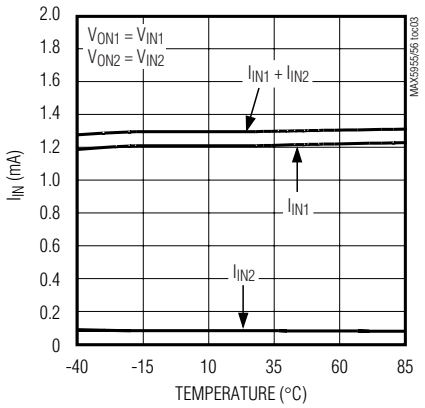
SUPPLY CURRENT vs. SUPPLY VOLTAGE



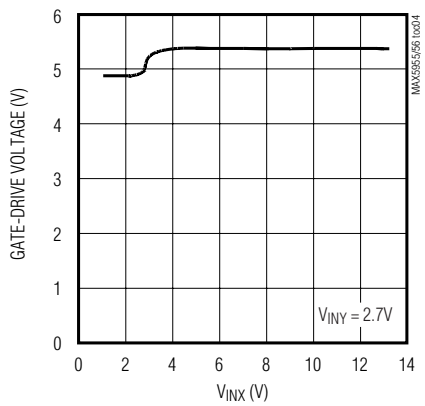
TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



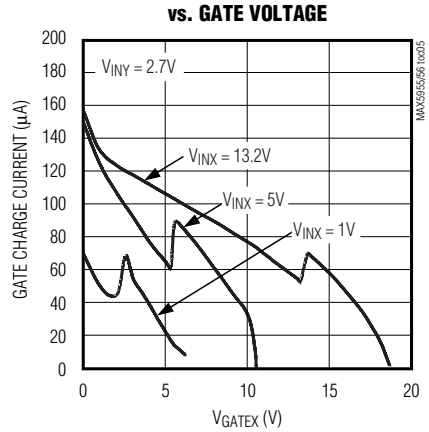
SUPPLY CURRENT vs. TEMPERATURE



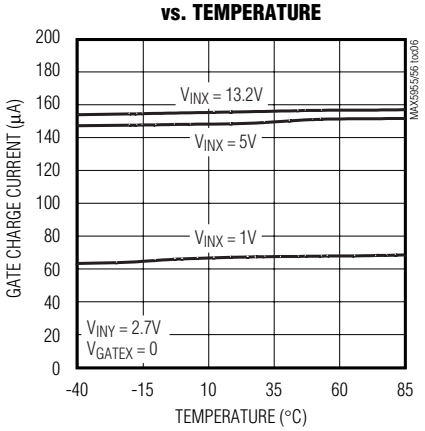
GATE-DRIVE VOLTAGE vs. INPUT VOLTAGE



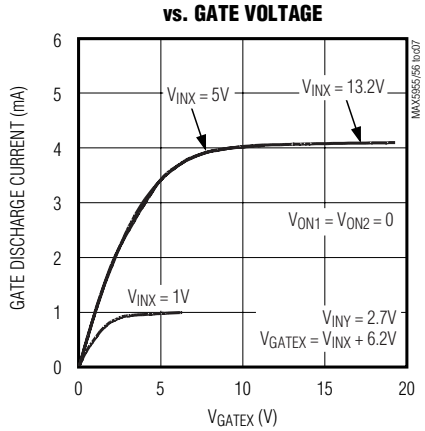
GATE CHARGE CURRENT vs. GATE VOLTAGE



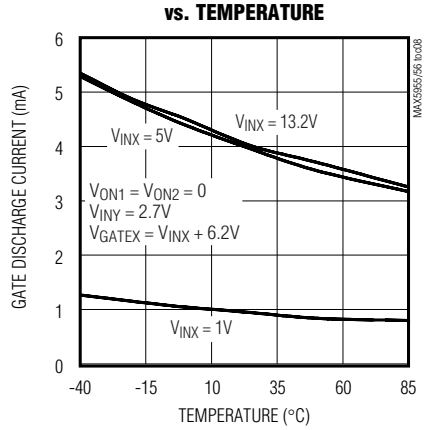
GATE CHARGE CURRENT vs. TEMPERATURE



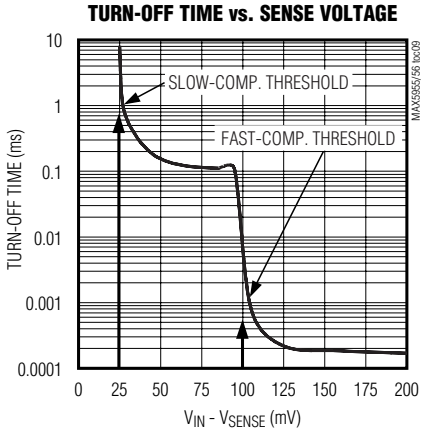
GATE STRONG DISCHARGE CURRENT vs. GATE VOLTAGE



GATE STRONG DISCHARGE CURRENT vs. TEMPERATURE



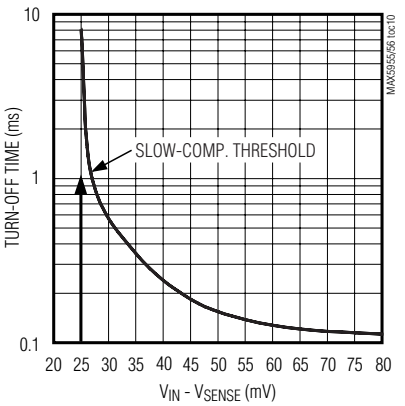
TURN-OFF TIME vs. SENSE VOLTAGE



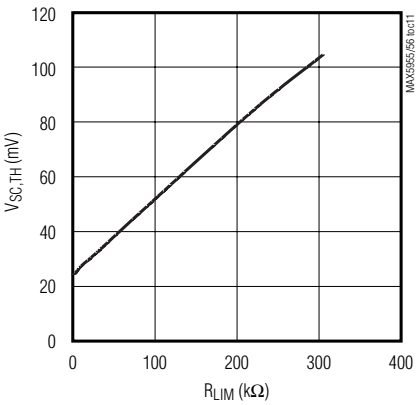
Typical Operating Characteristics (continued)

(Typical Operating Circuits, Q1 = Q2 = Fairchild FDB7090L, V_{IN1} = +5V, V_{IN2} = +3.3V, V_{ON1} = V_{ON2} = +2.7V, T_A = +25°C, unless otherwise noted. Channels 1 and 2 are identical in performance. Where characteristics are interchangeable, channels 1 and 2 are referred to as X and Y.)

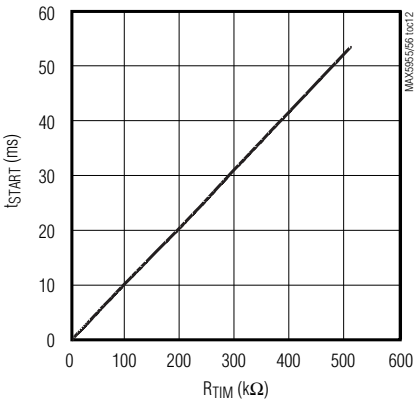
TURN-OFF TIME vs. SENSE VOLTAGE (EXPANDED SCALE)



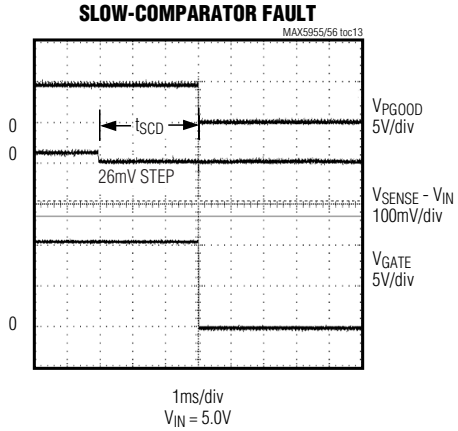
SLOW-COMPARATOR THRESHOLD vs. R_{LIM}



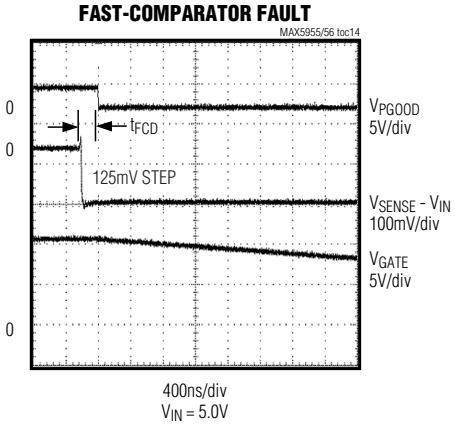
STARTUP PERIOD vs. R_{TIM}



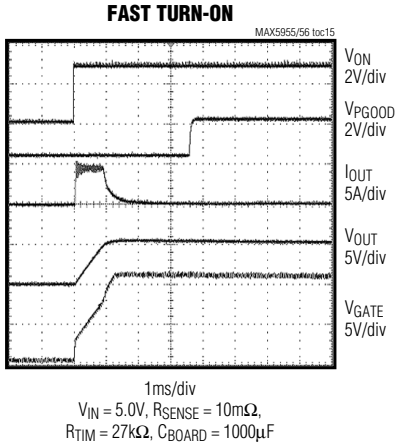
TURN-OFF TIME SLOW-COMPARATOR FAULT



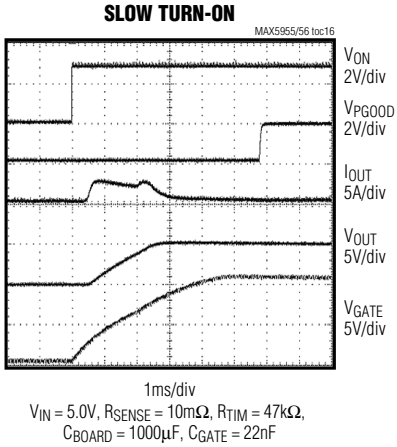
TURN-OFF TIME FAST-COMPARATOR FAULT



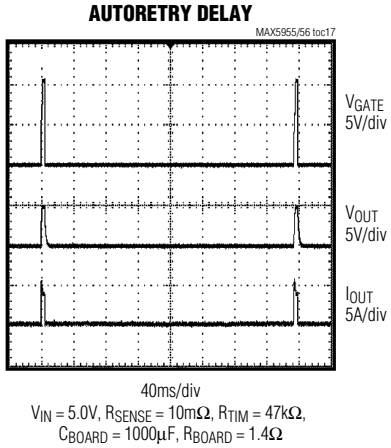
STARTUP WAVEFORMS FAST TURN-ON



STARTUP WAVEFORMS SLOW TURN-ON



AUTORETRY DELAY



Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

Pin Description

PIN	NAME	FUNCTION
1	PGOOD1	Channel 1 Status Output (Open Drain, see the *Absolute Maximum Ratings*). PGOOD1 asserts high when hot swap is successful and channel 1 is within regulation. PGOOD1 asserts low during startup, when ON1 is low, when channel 1 is off, or when channel 1 has any fault condition.
2	TIM	Startup Timer Setting. Connect a resistor from TIM to GND to set the startup period. Leave TIM unconnected for the default startup period of 9ms.
3	IN1	Channel 1 Supply Input. Connect to a supply voltage of 1V to 13.2V.
4	SENSE1	Channel 1 Current-Sense Input. Connect R_{SENSE1} from IN1 to SENSE1. Connect to IN1 to disable circuit breaker function of channel 1.
5	GATE1	Channel 1 Gate-Drive Output. Connect to the gate of an external n-channel MOSFET.
6	GND	Ground
7	LIM1	Channel 1 Current-Limit Setting. Connect a resistor from LIM1 to GND to set the current trip level. Connect to GND for the default 25mV threshold (see the *Slow-Comparator Threshold, R_{LIM}* section).
8	MON1	Channel 1 Output-Voltage Monitor. Window comparator input. Connect through a resistive divider from OUT1 to GND to set the channel 1 overvoltage and undervoltage threshold. Connect to IN1 to disable.
9	MON2	Channel 2 Output-Voltage Monitor. Window comparator input. Connect through a resistive divider from OUT2 to GND to set the channel 2 overvoltage and undervoltage threshold. Connect to IN2 to disable.
10	LIM2	Channel 2 Current-Limit Setting. Connect a resistor from LIM2 to GND to set the current trip level. Connect to GND for the default 25mV threshold (see the *Slow-Comparator Threshold, R_{LIM}* section).
11	ON1	Channel 1 On/Off Control Input. Channel 1 is turned on when $V_{ON1} > 0.875V$.
12	GATE2	Channel 2 Gate-Drive Output. Connect to the gate of an external n-channel MOSFET.
13	SENSE2	Channel 2 Current-Sense Input. Connect R_{SENSE2} from IN2 to SENSE2. Connect to IN2 to disable circuit-breaker function of channel 2.
14	IN2	Channel 2 Supply Input. Connect to a supply voltage of 1V to 13.2V.
15	ON2	Channel 2 On/Off Control Input. Channel 2 is turned on when $V_{ON2} > 0.875V$.
16	PGOOD2	Channel 2 Status Output (Open Drain, see the *Absolute Maximum Ratings*). PGOOD2 asserts high when hot swap is successful and channel 2 is within regulation. PGOOD2 asserts low during startup, when V_{ON2} is low, when channel 2 is off, or when channel 2 has any fault condition.

Detailed Description

The MAX5955 and MAX5956 are circuit breaker ICs for hot-swap applications where a line card is inserted into a live backplane. The MAX5955 and MAX5956 operate down to 1V provided one of the inputs is above 2.7V. Normally, when a line card is plugged into a live backplane, the card's discharged filter capacitors provide low impedance that can momentarily cause the main power supply to collapse. The MAX5955 and MAX5956 reside either on the backplane or on the removable card to provide inrush current limiting and short-circuit protection. This is achieved by using external n-channel MOSFETs, external current-sense resistors, and two on-chip comparators. The startup period and current-limit threshold of the MAX5955/MAX5956 can be adjusted with external resistors. Figure 1 shows the MAX5955/MAX5956 functional diagram.

The MAX5955/MAX5956 pull both PGOODs low and both external FETs off for an overcurrent condition. The MAX5955 also pulls both PGOODs low and both external FETs off (protection) for an undervoltage/overvoltage fault, whereas, the MAX5956 **ONLY** pulls the corresponding fault channel's PGOOD_ low (monitoring). When the overvoltage/undervoltage fault disappears on the MAX5956, the corresponding PGOOD_ automatically goes high impedance.

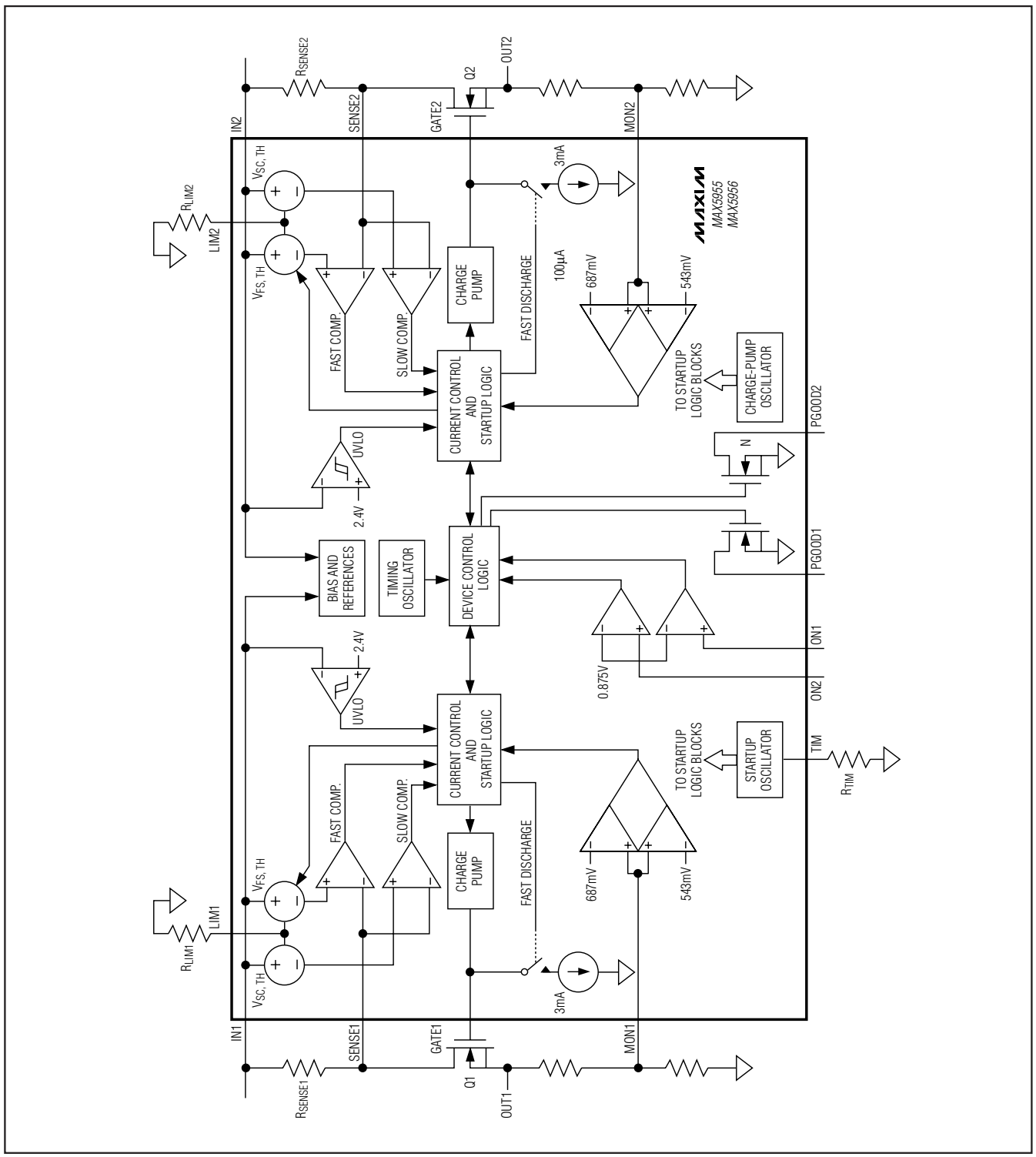


Figure 1. Functional Diagram

Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

Startup Period

R_{TIM} sets the duration of the startup period from 0.45s to 50ms (see the *Setting the Startup Period, RTIM* section). The default startup period is fixed at 9ms when TIM is floating. The startup period begins after the following three conditions are met:

1) V_{IN1} or V_{IN2} exceeds the UVLO threshold (2.4V) for the UVLO to startup delay (37.5ms).
2) V_{ON1} and V_{ON2} exceed the ON threshold (0.875V).
3) The device is not latched or in its autoretry delay (see the *Latched and Autoretry Overcurrent Fault Management* section).

The MAX5955/MAX5956 limit the load current if an overcurrent fault occurs during startup instead of completely turning off the external MOSFETs. The slow comparator is disabled during the startup period and the load current can be limited in two ways:

1) Slowly enhancing the MOSFETs by limiting the MOSFET gate-charging current.
2) Limiting the voltage across the external current-sense resistor.

During the startup period the gate-drive current is limited to 100µA and decreases with the increase of the gate voltage (see the *Typical Operating Characteristics*). This allows the controller to slowly enhance the MOSFETs. If the fast comparator detects an overcurrent, the MAX5955/MAX5956 regulate the gate voltage to ensure that the voltage across the sense resistor does not exceed $V_{SU,TH}$. This effectively regulates the inrush current during startup. Figure 2 shows the startup waveforms. PGOOD_ goes high impedance 0.75ms after the startup period if no fault condition is present.

VariableSpeed/BiLevel Fault Protection

VariableSpeed/BiLevel fault protection incorporates two comparators with different thresholds and response times to monitor the load current (Figure 3). During the startup period, protection is provided by limiting the load current. Protection is provided in normal operation (after the startup period has expired) by discharging both MOSFET gates with a strong 3mA pulldown current in response to a fault condition. After a fault, PGOOD_ is pulled low, the MAX5955B and MAX5956B stay latched off and the MAX5955A and MAX5956A automatically restart.

Slow-Comparator Startup Period

The slow comparator is disabled during the startup period while the external MOSFETs are turning on. Disabling the slow comparator allows the device to ignore the higher-than-normal inrush current charging the board capacitors when a card is first plugged into a live backplane.

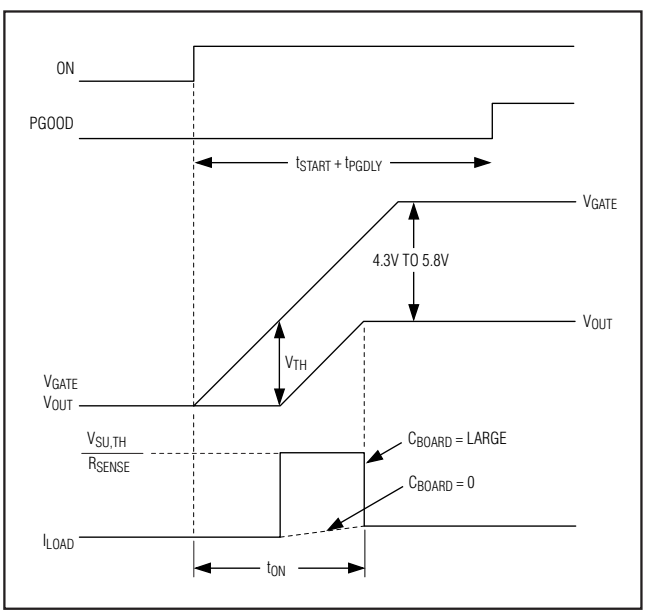


Figure 2. Startup Waveform

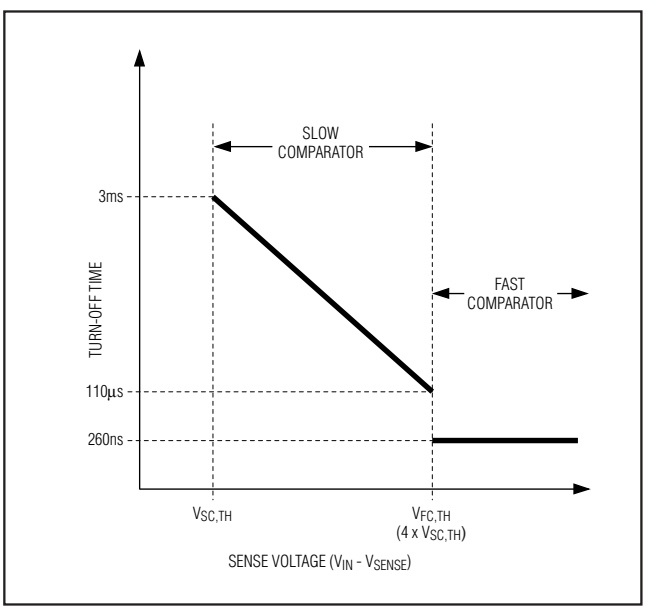


Figure 3. VariableSpeed/BiLevel Response

Slow-Comparator Normal Operation

After the startup period is complete, the slow comparator is enabled and the device enters normal operation. The comparator threshold voltage ($V_{SC,TH}$) is adjustable from 25mV to 100mV. The slow-comparator response time decreases to a minimum of 100µs with a large overdrive voltage. Response time is 3ms for a 1mV overdrive. The variable speed response time allows the MAX5955/MAX5956 to ignore low-amplitude momentary glitches, thus increasing system noise immunity. After an extended overcurrent condition, a fault is generated, both PGOODs are pulled low and the MOSFET gates are discharged with a strong 3mA pulldown current.

Fast-Comparator Startup Period

During the startup period, the fast comparator regulates the gate voltage to ensure that the voltage across the sense resistor does not exceed the startup fast-comparator threshold voltage ($V_{SU,TH}$), $V_{SU,TH}$ is scaled to two times the slow-comparator threshold ($V_{SC,TH}$).

Fast-Comparator Normal Operation

In normal operation, if the load current reaches the fast-comparator threshold, a fault is generated, both PGOODs are pulled low, and the MOSFET gates are discharged with a strong 3mA pulldown current. This happens in the event of a serious current overload or a dead short. The fast-comparator threshold voltage ($V_{FC,TH}$) is scaled to four times the slow-comparator threshold ($V_{SC,TH}$). This comparator has a fast response time of 260ns (Figure 3).

Undervoltage Lockout (UVLO)

The UVLO prevents the MAX5955/MAX5956 from turning on the external MOSFETs until one input voltage exceeds the UVLO threshold (2.4V) for $t_{D,UVLO}$. The MAX5955/MAX5956 use power from the higher input voltage rail for the charge pumps. This allows for more efficient charge-pump operation. The UVLO protects the external MOSFETs from an insufficient gate-drive voltage. $t_{D,UVLO}$ ensures that the board is fully inserted into the backplane and that the input voltages are stable. Any input voltage transient on **both** supplies below the UVLO threshold reinitiates the $t_{D,UVLO}$ and the startup period.

Latched and Autoretry Overcurrent Fault Management

The MAX5955B/MAX5956B latch the external MOSFETs off when an overcurrent fault is detected. Toggling ON_ below 0.875V or one of the supply voltages below/above the UVLO threshold for at least 100µs clears the fault latch and reinitiates the startup period. Similarly, the MAX5955A/MAX5956A turn the external MOSFETs off when an overcurrent fault is detected, then automatically restart after the autoretry delay that is internally set to 64 times t_{START}. During the autoretry delay, toggling ON_ below 0.875V does not clear the fault latch. The autoretry can be overridden, causing the startup period to begin immediately by toggling one of the supply voltages below/above the UVLO threshold. When toggling a supply voltage to clear a fault, remember that the supply voltage must go below and then above the UVLO threshold for at least 100µs regardless of the final value of the supply voltage.

Output Overvoltage/Undervoltage Fault Management

The MAX5955/MAX5956 monitor the output voltages with the MON1 and MON2 window comparator inputs. These voltage monitors are enabled after the startup period. Once enabled, the voltage monitor detects a fault if $V_{MON\_}$ is less than 543mV or greater than 687mV.

When the MAX5955 protection device detects an output overvoltage/undervoltage fault on either MON1 or MON2, both external MOSFET gates are discharged at 3mA and both PGOODs pull low. For the MAX5955A, the part continuously attempts to restart after each autoretry period. The part successfully restarts after the fault is removed and after waiting the autoretry period. For the MAX5955B, the GATEs are latched off until the output voltage fault is removed and the fault latch is cleared by toggling ON_ or by cycling one of the supply voltages above/below the UVLO threshold.

When the MAX5956 monitoring device detects an output overvoltage/undervoltage fault on either MON1 or MON2, neither external MOSFET gates are affected, but the PGOOD_ of the channel experiencing the fault pulls low. Thus the fault is reported on the channel with the problem, but the MAX5956 does not allow an output overvoltage/undervoltage fault to disrupt operation by shutting down the channels. The MAX5956's PGOOD_ output immediately goes high impedance after the output overvoltage/undervoltage fault is removed.

The voltage monitors do not react to output glitches of less than 20µs. A capacitor from MON_ to GND increases the effective glitch filter time. The voltage monitoring function of the MAX5955/MAX5956 can be disabled by connecting V_{IN1} to MON1 and V_{IN2} to MON2.

Status Outputs (PGOOD_)

The status output is an open-drain output that pulls low in response to one of the following conditions:

- Overcurrent fault
- Output undervoltage/overvoltage fault

PGOOD_ goes low when the corresponding channel is forced off (ON_ < 0.875V) (Table 1).

Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

Table 1. Status Output Truth Table

PART	OVERCURRENT FAULT (V_{OUT1})	OVERCURRENT FAULT (V_{OUT2})	OVER/UNDER-VOLTAGE FAULT (V_{OUT1})	OVER/UNDER-VOLTAGE FAULT (V_{OUT2})	PGOOD1/ PGOOD2	GATE1/ GATE2
MAX5955 UV/OV Protection	Yes	X	X	X	Low/Low	Off/Off
	X	Yes	X	X	Low/Low	Off/Off
	X	X	Yes	X	Low/Low	Off/Off
	X	X	X	Yes	Low/Low	Off/Off
MAX5956 UV/OV Monitor	Yes	X	X	X	Low/Low	Off/Off
	X	Yes	X	X	Low/Low	Off/Off
	X	X	Yes	No	Low/High	On/On
	X	X	No	Yes	High/Low	On/On

Applications Information

Component Selection

n-Channel MOSFET

Select the external MOSFETs according to the application's current levels. Table 2 lists some recommended components. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ causes output ripple if there is a pulsating load. Determine the device power rating to accommodate a short-circuit condition on the board at startup and when the device is in automatic-retry mode (see the *MOSFET Thermal Considerations* section).

Using the MAX5955B/MAX5956B in latched mode allows the use of MOSFETs with lower power ratings. A MOSFET typically withstands single-shot pulses with higher dissipation than the specified package rating. Table 3 lists some recommended manufacturers and components.

Table 2. Recommended n-Channel MOSFETs

PART NUMBER	MANUFACTURER	DESCRIPTION
IRF7413	International Rectifier	11mΩ, 8 SO, 30V
IRF7401		22mΩ, 8 SO, 20V
IRL3502S		6mΩ, D2PAK, 20V
MMSF3300	Motorola	20mΩ, 8 SO, 30V
MMSF5N02H		30mΩ, 8 SO, 20V
MTB60N05H		14mΩ, D^2PAK, 50V
FDS6670A	Fairchild	10mΩ, 8 SO, 30V
NDS8426A		13.5mΩ, 8 SO, 20V
FDB8030L		4.5mΩ, D^2PAK, 30V

Sense Resistor

The slow-comparator threshold voltage is adjustable from 25mV to 100mV. Select a sense resistor that causes a drop equal to the slow-comparator threshold voltage at a current level above the maximum normal operating current. Typically, set the overload current at 1.2 to 1.5 times the full load current. The fast-comparator threshold is four times the slow-comparator threshold in normal operating mode. Choose the sense-resistor power rating to be greater than $(I_{OVERLOAD})^2 \times V_{SC,TH}$.

Slow-Comparator Threshold, R_{LIM}

The slow-comparator threshold voltage is adjustable from 25mV to 100mV, allowing designers to fine-tune the current-limit threshold for use with standard-value sense resistors. Low slow-comparator thresholds allow for increased efficiency by reducing the power dissipated by the sense resistor. Furthermore, the low 25mV slow-comparator threshold is beneficial when operating with supply rails down to 1V because it allows a small percentage of the overall output voltage to be used for current sensing. The VariableSpeed/BiLevel fault protection feature offers inherent system immunity against load transients and noise. This allows the slow-comparator threshold to be set close to the maximum normal operating level without experiencing nuisance faults. To adjust the slow-comparator threshold, calculate R_{LIM} as follows:

$$R_{LIM} = \frac{V_{TH} - 25mV}{0.25\mu A}$$

where V_{TH} is the desired slow-comparator threshold voltage.

Table 3. Component Manufacturers

COMPONENT	MANUFACTURER	PHONE	WEBSITE
Sense Resistors	Dale-Vishay	402-564-3131	www.vishay.com
	IRC	704-264-8861	www.irctt.com
MOSFETs	Fairchild	888-522-5372	www.fairchildsemi.com
	International Rectifier	310-233-3331	www.irf.com
	Motorola	602-244-3576	www.mot-sps.com/ppd

Setting the Startup Period, R_{TIM}

The startup period (t_{START}) is adjustable from 0.45ms to 50ms. The adjustable startup period feature allows systems to be customized for MOSFET gate capacitance and board capacitance (C_{BOARD}). The startup period is adjusted with the resistance connected from TIM to GND (R_{TIM}). R_{TIM} must be between 4kΩ and 500kΩ. The startup period has a default value of 9ms when TIM is left floating. Calculate R_{TIM} with the following equation:

$$R_{TIM} = \frac{t_{START}}{128 \times 800pF}$$

where t_{START} is the desired startup period.

Startup Sequence

There are two ways of completing the startup sequence. **Case A** describes a startup sequence that slowly turns on the MOSFETs by limiting the gate charge. **Case B** uses the current-limiting feature and turns on the MOSFETs as fast as possible while still preventing a high inrush current. The output voltage ramp-up time (t_{ON}) is determined by the longer of the two timings, case A and case B. Set the startup timer t_{START} to be longer than t_{ON} to guarantee enough time for the output voltage to settle.

Case A: Slow Turn-On (Without Current Limit)

There are two ways to turn on the MOSFETs without reaching the fast-comparator current limit:

- If the board capacitance (C_{BOARD}) is small, the inrush current is low.
- If the gate capacitance is high, the MOSFETs turn on slowly.

In both cases, the turn-on time is determined only by the charge required to enhance the MOSFET. The small gate-charging current of 100µA effectively limits the output voltage dV/dt. Connecting an external capacitor between GATE and GND extends turn-on time. The time required to charge/discharge a MOSFET is as follows:

$$t = \frac{C_{GATE} \times \Delta V_{GATE} + Q_{GATE}}{I_{GATE}}$$

where:

C_{GATE} is the external gate to ground capacitance (Figure 4).

ΔV_{GATE} is the change in gate voltage.

Q_{GATE} is the MOSFET total gate charge.

I_{GATE} is the gate-charging/discharging current.

In this case, the inrush current depends on the MOSFET gate-to-drain capacitance (C_{rss}) plus any additional capacitance from GATE to GND (C_{GATE}), and on any load current (I_{LOAD}) present during the startup period.

$$I_{INRUSH} = \frac{C_{BOARD}}{C_{rss} + C_{GATE}} \times I_{GATE} + I_{LOAD}$$

Example: Charging and Discharging Times Using the Fairchild FDB7030L MOSFET

If V_{IN1} = 5V then GATE1 charges up to 10.4V (V_{IN1} + V_{DRIVE}); therefore ΔV_{GATE} = 10.4V. The manufacturer's data sheet specifies that the FDB7030L has approximately 60nC of gate charge and C_{rss} = 600pF. The MAX5955/MAX5956 have a 100µA gate-charging current and a 3mA strong discharging current.

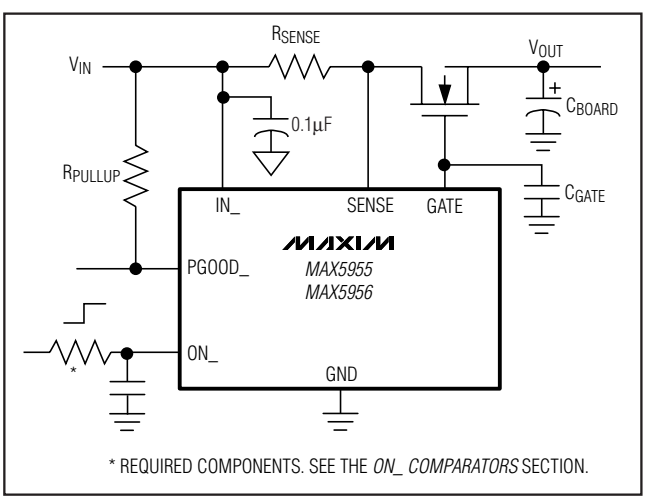


Figure 4. Operating with an External Gate Capacitor

Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

C_{BOARD} = 6µF and the load does not draw any current during the startup period. With no gate capacitor the inrush current, charge, and discharge times are:

$$I_{INRUSH} = \frac{6\mu F}{600pF + 0} \times 100\mu A + 0 = 1A$$

$$t_{CHARGE} = \frac{0 \times 10.4V + 60nC}{100\mu A} = 0.6ms$$

$$t_{DISCHARGE} = \frac{0 \times 10.4V + 60nC}{3mA} = 0.02ms$$

With a 22nF gate capacitor the inrush current, charge, and discharge times are:

$$I_{INRUSH} = \frac{6\mu F}{600pF + 22nF} \times 100\mu A + 0 = 26.5mA$$

$$t_{CHARGE} = \frac{22nF \times 10.4V + 60nC}{100\mu A} = 2.89ms$$

$$t_{DISCHARGE} = \frac{22nF \times 10.4V + 60nC}{3mA} = 0.096ms$$

Case B: Fast Turn-On (with Current Limit)

In applications where the board capacitance (C_{BOARD}) is high, the inrush current causes a voltage drop across R_{SENSE} that exceeds the startup fast-comparator threshold. The fast comparator regulates the voltage across the sense resistor to $V_{SU,TH}$. This effectively regulates the inrush current during startup. In this case, the current charging C_{BOARD} can be considered constant and the turn-on time is:

$$t_{ON} = \frac{C_{BOARD} \times V_{IN} \times R_{SENSE}}{V_{SU,TH}}$$

The maximum inrush current in this case is:

$$I_{INRUSH} = \frac{V_{SU,TH}}{R_{SENSE}}$$

Figure 2 shows the waveforms and timing diagrams for a startup transient with current regulation (see *Typical Operating Characteristics*). **When operating under this condition, an external gate capacitor is not required.**

ON_ Comparators

The ON_ comparators control the on/off function of the MAX5955/MAX5956. ON_ allows independent control over channel 1 and channel 2. Drive ON1 and ON2 high (> 0.875V) to enable channel 1 and channel 2, respectively. Pull ON_ low (< 0.875V) to disable the respective channel. An RC time delay must be added to the ON_ inputs with delay set to at least 20µs. This allows the internal circuits to stabilize after application of a steeply rising $V_{IN\_}$.

Using the MAX5955/MAX5956 on the Backplane

Using the MAX5955/MAX5956 on the backplane allows multiple cards with different input capacitance to be inserted into the same slot even if the card does not have on-board hot-swap protection. The startup period can be triggered if IN_ is connected to ON_ through a trace on the card (Figure 5).

Input Transients

The voltage at IN1 or IN2 must be above the UVLO during inrush and fault conditions. When a short-circuit condition occurs on the board, the fast comparator trips causing the external MOSFET gates to be discharged at 3mA. The main system power supply must be able to sustain a temporary fault current, without dropping below the UVLO threshold of 2.4V, until the external MOSFET is completely off. If the main system power supply collapses below UVLO, the MAX5955/MAX5956 force the device to restart once the supply has recovered. The MOSFET is turned off in a very short time resulting in a high di/dt. The backplane delivering the power to the external card must have low inductance to minimize voltage transients caused by this high di/dt.

MOSFET Thermal Considerations

During normal operation, the external MOSFETs dissipate little power. The MOSFET $R_{DS(ON)}$ is low when the MOSFET is fully enhanced. The power dissipated in normal operation is $P_D = I_{LOAD}^2 \times R_{DS(ON)}$. The most power dissipation occurs during the turn-on and turn-off transients when the MOSFETs are in their linear regions. Take into consideration the worst-case scenario of a continuous short-circuit fault, consider these two cases:

1) The single turn-on with the device latched after a fault (MAX5955B/MAX5956B)
2) The continuous automatic retry after a fault (MAX5955A/MAX5956A)

MOSFET manufacturers typically include the package thermal resistance from junction to ambient ($R_{\theta JA}$) and thermal resistance from junction to case ($R_{\theta JC}$), which determine the startup time and the retry duty cycle ($d = t_{START}/t_{START} + t_{RETRY}$). Calculate the required transient thermal resistance with the following equation:

$$Z_{\theta JA(MAX)} \le \frac{T_{JMAX} - T_A}{V_{IN} \times I_{START}}$$

where $I_{START} = V_{SU,TH} / R_{SENSE}$

Layout Considerations

To take full advantage of the switch response time to an output fault condition, it is important to keep all traces as short as possible and to maximize the high-current trace dimensions to reduce the effect of undesirable parasitic resistance and inductance. Place the MAX5955/MAX5956 close to the card's connector, and a 0.01µF capacitor to GND should be placed as close as possible to each V_{IN} pin. Use a ground plane to minimize impedance and inductance. Minimize the current-sense resistor trace length (< 10mm), and ensure accurate current sensing with Kelvin connections (Figure 6).

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation across the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board (refer to the MAX5956 EV Kit data sheet).

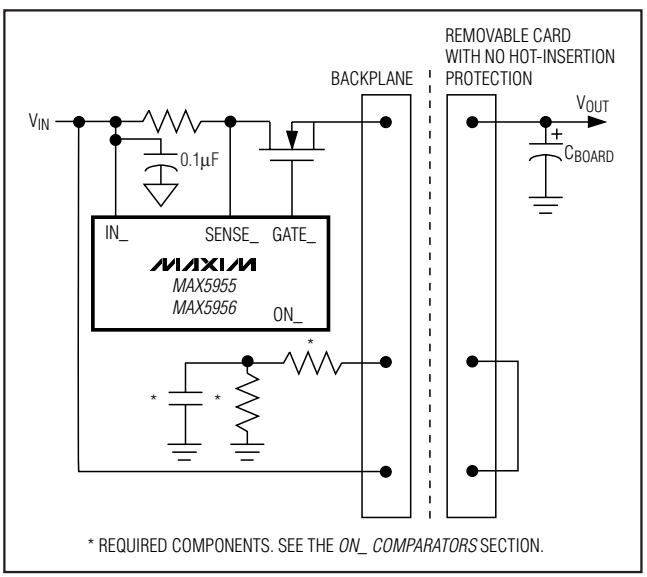


Figure 5. Using the MAX5955/MAX5956 on a Backplane

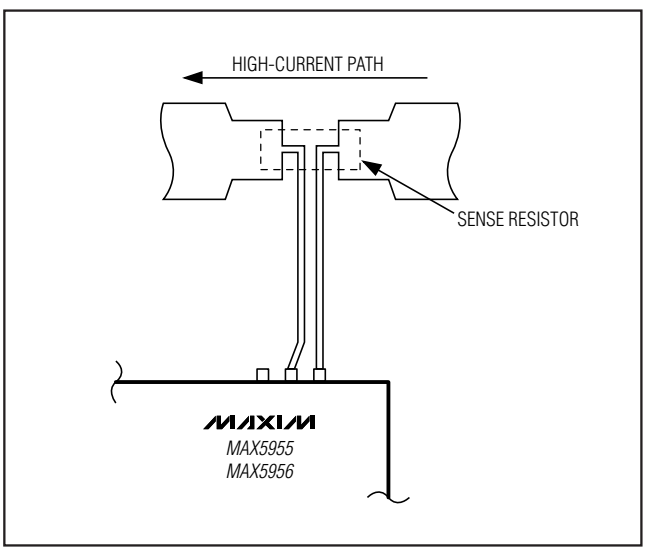


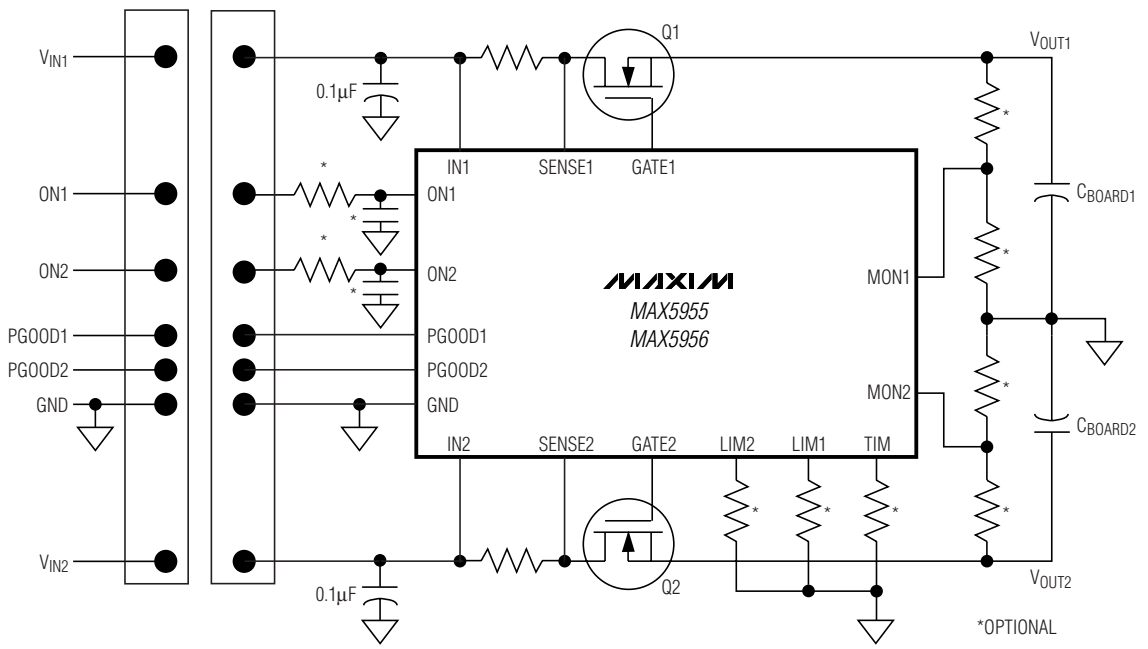
Figure 6. Kelvin Connection for the Current-Sense Resistors

Selector Guide

PART	OUTPUT UNDERVOLTAGE/OVERVOLTAGE PROTECTION/MONITOR	FAULT MANAGEMENT
MAX5955AEEE	Protection	Autoretry
MAX5955AUEE	Protection	Autoretry
MAX5955BEEE	Protection	Latched
MAX5955BUEE	Protection	Latched
MAX5956AEEE	Monitor	Autoretry
MAX5956AUEE	Monitor	Autoretry
MAX5956BEEE	Monitor	Latched
MAX5956BUEE	Monitor	Latched

Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

Typical Operating Circuit



* REQUIRED COMPONENTS. SEE THE *ON_ COMPARATORS* SECTION.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX5956AEEE	-40°C to +85°C	16 QSOP
MAX5956AEEE+	-40°C to +85°C	16 QSOP
MAX5956AUEE	0°C to +85°C	16 QSOP
MAX5956AUEE+	0°C to +85°C	16 QSOP
MAX5956BEEE	-40°C to +85°C	16 QSOP
MAX5956BEEE+	-40°C to +85°C	16 QSOP
MAX5956BUEE	0°C to +85°C	16 QSOP
MAX5956BUEE+	0°C to +85°C	16 QSOP

+Denotes lead-free package.

Chip Information

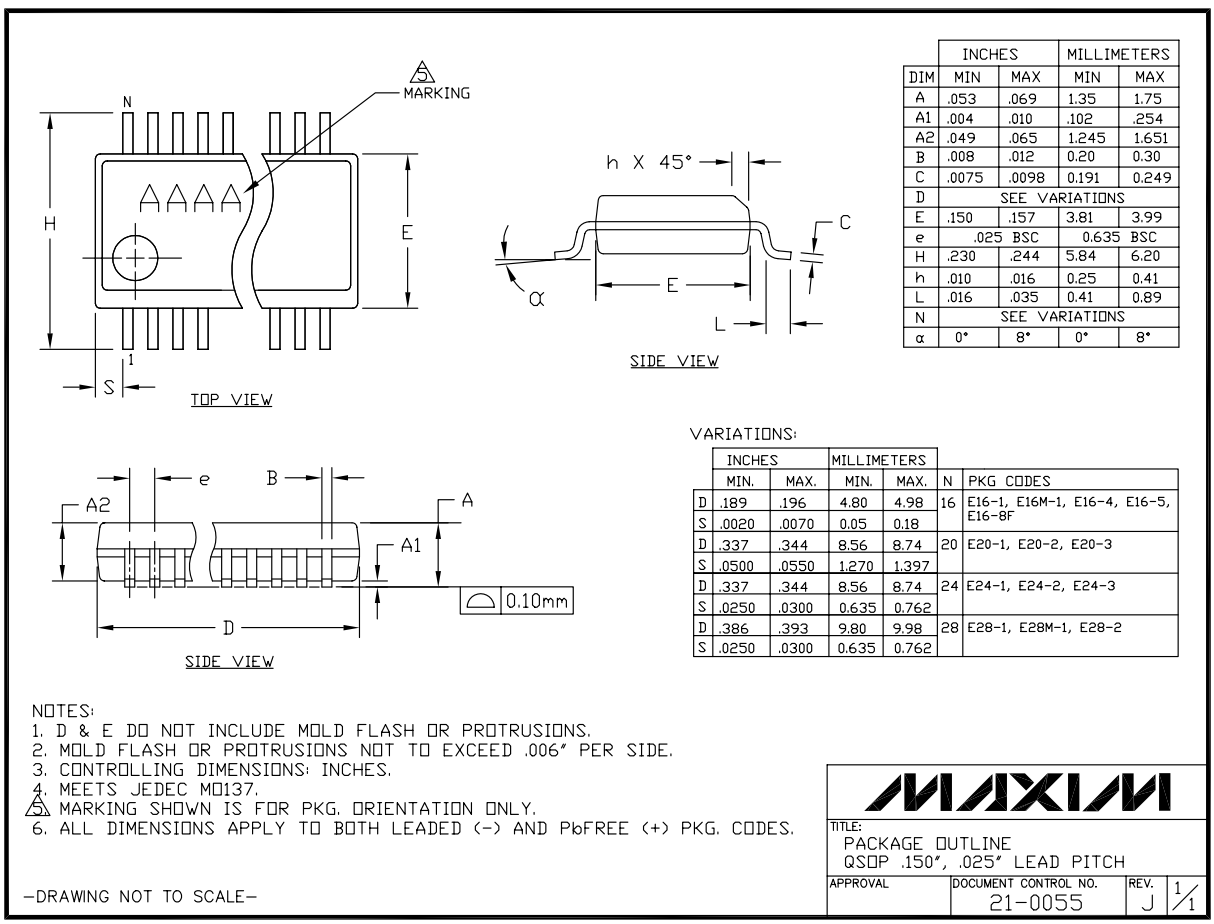
TRANSISTOR COUNT: 3542

PROCESS: BiCMOS

Low-Voltage, Dual Hot-Swap Controllers with Independent On/Off Control

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	PKG CODES
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-4, E16-5, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2, E20-3
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2, E24-3
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	J	1/1