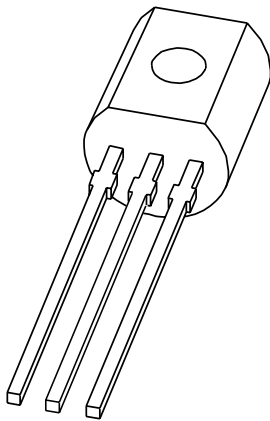


# DATA SHEET



## **MPS3906** PNP switching transistor

Product specification  
Supersedes data of 1999 Apr 12

2004 Oct 27

# PNP switching transistor

# MPS3906

## FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 40 V).

## APPLICATIONS

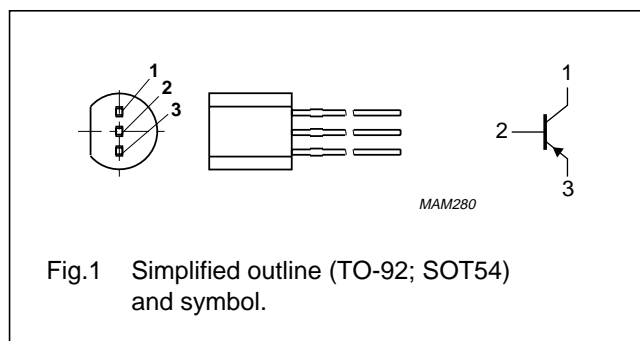
- General purpose switching and amplification.

## DESCRIPTION

PNP transistor in a plastic TO-92; SOT54 package.  
NPN complement: MPS3904.

## PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
MPS3906	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–40	V
$V_{CEO}$	collector-emitter voltage	open base	–	–40	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–100	mA
$I_{CM}$	peak collector current		–	–200	mA
$I_{BM}$	peak base current		–	–200	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	500	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	ambient temperature		–65	+150	°C

## PNP switching transistor

## MPS3906

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	250	K/W

## Note

1. Transistor mounted on an FR4 printed-circuit board.

## CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -30\text{ V}$ ; $I_E = 0\text{ A}$	–	–50	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}$ ; $I_E = 0\text{ A}$	–	–50	nA
$h_{FE}$	DC current gain	$V_{CE} = -1\text{ V}$ ; note 1 $I_C = -0.1\text{ mA}$ $I_C = -1\text{ mA}$ $I_C = -10\text{ mA}$ $I_C = -50\text{ mA}$ $I_C = -100\text{ mA}$	60 80 100 60 30	– – 300 – –	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -10\text{ mA}$ ; $I_B = -1\text{ mA}$ ; note 1	–	–250	mV
		$I_C = -50\text{ mA}$ ; $I_B = -5\text{ mA}$ ; note 1	–	–400	mV
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -10\text{ mA}$ ; $I_B = -1\text{ mA}$ ; note 1	–650	–850	mV
		$I_C = -50\text{ mA}$ ; $I_B = -5\text{ mA}$ ; note 1	–	–950	mV
$C_c$	collector capacitance	$V_{CB} = -5\text{ V}$ ; $I_E = i_e = 0\text{ A}$ ; $f = 100\text{ kHz}$ to $1\text{ MHz}$	–	5	pF
$C_e$	emitter capacitance	$V_{EB} = -0.5\text{ V}$ ; $I_C = i_c = 0\text{ A}$ ; $f = 100\text{ kHz}$ to $1\text{ MHz}$	–	15	pF
$f_T$	transition frequency	$V_{CE} = -20\text{ V}$ ; $I_C = -10\text{ mA}$ ; $f = 100\text{ MHz}$	150	–	MHz
$F$	noise figure	$V_{CE} = -5\text{ V}$ ; $I_C = -100\text{ }\mu\text{A}$ ; $R_S = 1\text{ k}\Omega$ ; $f = 10\text{ Hz}$ to $15.7\text{ kHz}$	–	4	dB

## Switching times (between 10 % and 90 % levels); (see Fig.2)

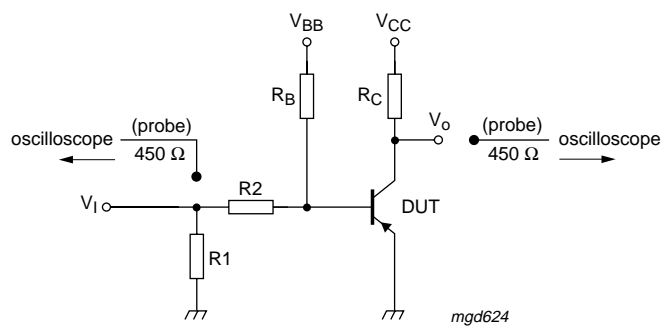
$t_{on}$	turn-on time	$I_{Bon} = -10\text{ mA}$ ; $I_{Boff} = -1\text{ mA}$ ; $I_{Boff} = 1\text{ mA}$ ; $V_{CC} = -3\text{ V}$ ; $V_{BB} = 1.9\text{ V}$	–	100	ns
$t_d$	delay time		–	50	ns
$t_r$	rise time		–	50	ns
$t_{off}$	turn-off time		–	700	ns
$t_s$	storage time		–	600	ns
$t_f$	fall time		–	100	ns

## Note

1. Pulse test:  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 0.02$ .

## PNP switching transistor

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$V_i = -5\text{ V}$ ;  $t_p \geq 4\text{ }\mu\text{s}$ ;  $t_r = t_f \leq 3\text{ ns}$ .

$R_1 = 56\text{ }\Omega$ ;  $R_2 = 2.5\text{ k}\Omega$ ;  $R_B = 3.9\text{ k}\Omega$ ;  $R_C = 270\text{ }\Omega$ .

Oscilloscope: input impedance  $Z_i = 50\text{ }\Omega$ .

Fig.2 Test circuit for switching times.

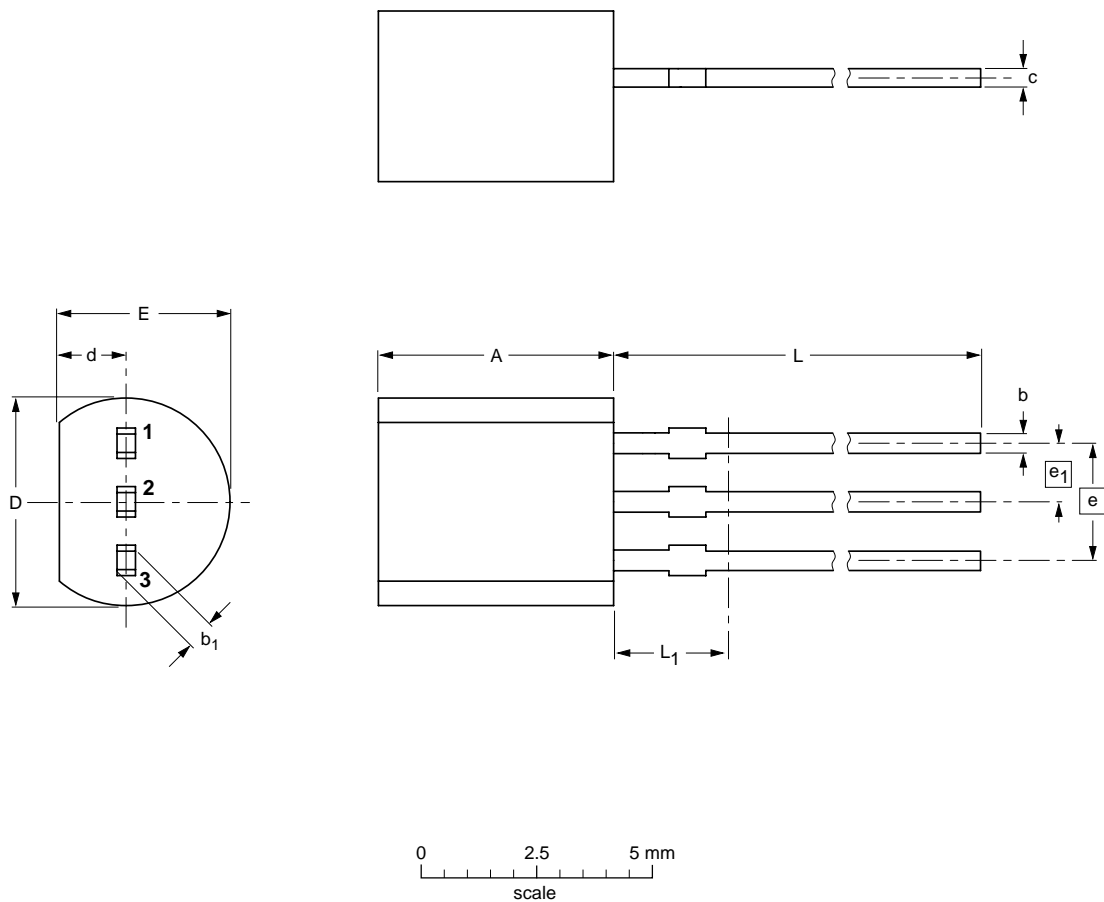
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54




DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			-97-02-28 04-06-28

## PNP switching transistor

MPS3906

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
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