NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL54050IRUZ-T

ISL54501, ISL54502

+1.62V to +5.5V, 5Ω, Single SPST Analog Switches

FN6550
Rev 3.00
May 6, 2013

The Intersil ISL54501 and ISL54502 devices are low ON-resistance, low voltage, bi-directional, single pole/single throw (SPST) analog switches designed to operate from a single +1.62V to +5.5V supply. Targeted applications include battery powered equipment that benefit from low r_{ON} resistance (5Ω), excellent r_{ON} flatness, and fast switching speeds (t_{ON} = 22ns, t_{OFF} = 15ns). The digital logic input is 1.8V CMOS compatible when using a single +3V supply.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This family of parts may be used to switch in additional functionality while reducing ASIC design risk. The ISL54501, ISL54502 are offered in a 6 Ld 1.2mmx1.0mmx0.4mm pitch µTDFN package, alleviating board space limitations.

The ISL54501 has one normally open (NO) switch and ISL54502 has one normally closed (NC) switch.

TABLE 1. FEATURES AT A GLANCE

	ISL54501	ISL54502
NUMBER OF SWITCHES	1	1
SW	NO	NC
1.8V r_{ON}	12Ω	12Ω
1.8V t_{ON}/t_{OFF}	70ns/52ns	70ns/52ns
3V r_{ON}	6.0Ω	6.0Ω
3V t_{ON}/t_{OFF}	30ns/20ns	30ns/20ns
5V r_{ON}	5.0Ω	5.0Ω
5V t_{ON}/t_{OFF}	22ns/15ns	22ns/15ns
Packages	6 Ld µTDFN, 6 Ld SOT-23	

Features

- ON-resistance (r_{ON})
  - V_{CC} = +5.0V 5.0Ω
  - V_{CC} = +3.0V 7.0Ω
  - V_{CC} = +1.8V 13Ω
- r_{ON} Flatness (+4.5V Supply) 1.1Ω
- Single Supply Operation. . . . . +1.62V to +5.5V
- Fast Switching Action (+4.5V Supply)
  - t_{ON} 22ns
  - t_{OFF} 15ns
- ESD HBM Rating 6kV
- 1.8V CMOS Logic Compatible (+3V supply)
- Available in 6 Ld µTDFN and 6 Ld SOT-23 Packages
- Pb-free Available (RoHS compliant)

Applications

- Battery powered, handheld, and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and video switching

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Ordering Information

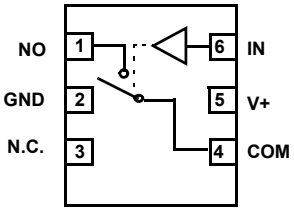
PART NUMBER (Notes 1, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Tape and Reel) (Pb-Free)	PKG. DWG. #
ISL54501IRUZ-T (Note 2)	1	-40 to +85	6 Ld µTDFN	L6.1.2x1.0A
ISL54501IHZ-T (Note 3)	4501	-40 to +85	6 Ld SOT-23	P6.064A
ISL54502IRUZ-T (Note 2)	2	-40 to +85	6 Ld µTDFN	L6.1.2x1.0A
ISL54502IHZ-T (Note 3)	4502	-40 to +85	6 Ld SOT-23	P6.064A

NOTES:

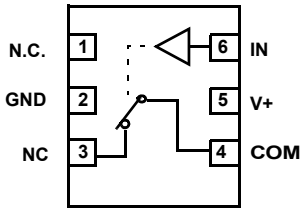
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL54501, ISL54502. For more information on MSL please see techbrief TB363.

Pin Configurations (Note 5)

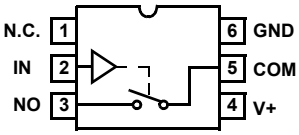
ISL54501
(6 LD UTDFN)
TOP VIEW



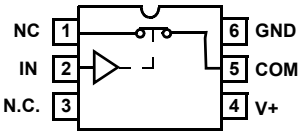
ISL54502
(6 LD UTDFN)
TOP VIEW



ISL54501
(6 LD SOT-23)
TOP VIEW



ISL54502
(6 LD SOT-23)
TOP VIEW



NOTE:
5. Switches Shown for Logic “0” Input.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.62V to +5.5V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Connect

Truth Table

LOGIC	ISL54501	ISL54502
0	Off	On
1	On	Off

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Absolute Maximum Ratings

V+ to GND ..... -0.5 to 6.5V
Input Voltages
NO, NC, IN (Note 6) ..... -0.5V to ((V+) + 0.5V)
Output Voltages
COM (Note 6) ..... -0.5V to ((V+) + 0.5V)
Continuous Current NO, NC, or COM ..... ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) ..... ±600mA
ESD Rating
Human Body Model ..... >6kV
Machine Model ..... >200V
Charged Device Model ..... >2.2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
6 Ld µTDFN Pkg. (Notes 7, 9)	239.2	111.6
6 Ld SOT-23 Pkg. (Note 8, 9)	260	120

Maximum Junction Temperature (Plastic Package) ..... +150°C
Maximum Storage Temperature Range ..... -65°C to +150°C
Pb-free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

V+ (Positive DC Supply Voltage) ..... 1.8V ± 10% to 5.0V ± 10%
Analog Signal Range ..... 0V to V+
V_{IN} (Digital Logic Input Voltage (IN) ..... 0V to V+
Temperature Range ..... -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
9. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.0V, V_{INL} = 0.8V (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 14, see Figure 4)	25	-	4.2	5	Ω
		Full	-	-	6	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Notes 13, 14)	25	-	1.1	1.3	Ω
		Full	-	-	1.5	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0.3V, 5V, V_{NO} or V_{NC} = 5V, 0.3V	25	-25	1.2	25	nA
		Full	-150	-	150	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 0.3V, 5V, or V_{NO} or V_{NC} = 0.3V, 5V, or Floating	25	-30	1.7	30	nA
		Full	-300	-	300	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1, Note 14)	25	-	22	-	ns
		Full	-	23	-	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 1, Note 14)	25	-	15	-	ns
		Full	-	15	-	ns
Break-Before-Make Time Delay, t_D	V+ = 5.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (see Figure 3, Note 14)	Full	-	18	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω, C_L = 1.0nF (see Figure 2)	25	-	16	-	pC
OFF-Isolation	$_L$ = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{P-P}$ (see Figure 3)	25	-	75	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 32Ω	25	-	0.12	-	%
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.01	-	%
-3dB Bandwidth	Signal = 0dBm, R_L = 50Ω	25	-	350	-	MHz
NO or NC OFF Capacitance, C_{OFF}	V+ = 4.5V, f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 5)	25	-	6	-	pF
COM ON Capacitance, $C_{COM(ON)}$	V+ = 4.5V, f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 5)	25	-	12	-	pF

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.0V, V_{INL} = 0.8V (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	**1.62**	-	**5.5**	V
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+	25	-	0.02	**0.1**	µA
		Full	-	0.5	**2.5**	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	**0.8**	V
Input Voltage High, V_{INH}		Full	**2.4**	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	**-0.1**	0.044	**0.1**	µA

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C**.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-Resistance, r_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 14, see Figure 4)	25	-	6.3	**7**	Ω
		Full	-	-	**8**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Notes 13, 14)	25	-	1.8	**2.3**	Ω
		Full	-	-	**2.5**	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 1, Note 8)	25	-	28	-	ns
		Full	-	30	-	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 1, Note 14)	25	-	20	-	ns
		Full	-	30	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω,C_L = 1.0nF (see Figure 2)	25	-	12	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz, V_{COM} = $1V_{P-P}$ (see Figure 3)	25	-	75	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 32Ω	25	-	0.4	-	%
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.053	-	%
-3dB Bandwidth	Signal = 0dBm, R_L = 50Ω	25	-	350	-	MHz
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 5)	25	-	6	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 5)	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 5)	25	-	12	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+	25	-	0.02	-	µA
		Full	-	0.11	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	**0.5**	V
Input Voltage High, V_{INH}		Full	**1.4**	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	**-0.1**	0.049	**0.1**	µA

Electrical Specifications - 1.8V Supply

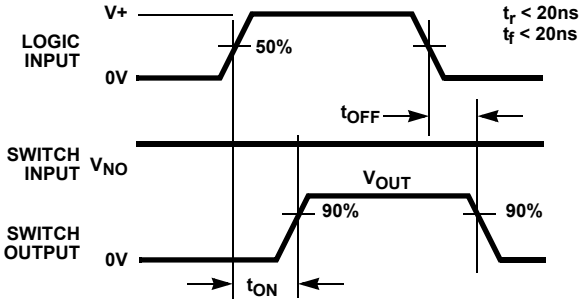
Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1V, V_{INL} = 0.4V (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**0**	-	**V+**	V
ON-Resistance, r_{ON}	V+ = 1.8V, I_{COM} = 10mA, V_{NO} or V_{NC} = 0V to V+ (Note 14, see Figure 4)	25	-	11.9	**12.8**	Ω
		Full	-	-	**13.8**	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 1, Note 14)	25	-	70	-	ns
		Full	-	130	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (see Figure 1, Note 14)	25	-	52	-	ns
		Full	-	100	-	ns
Charge Injection, Q	V_G = V+/2, R_G = 0Ω, C_L = 1.0nF (see Figure 2)	25	-	5.8	-	pC
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	**0.4**	V
Input Voltage High, V_{INH}		Full	**1**	-	-	V

NOTES:

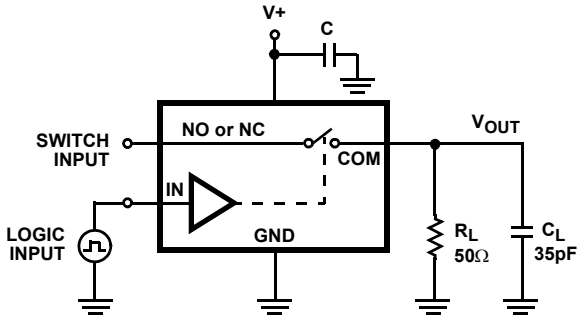
10. V_{IN} = input voltage to perform proper function.
11. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
13. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
14. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

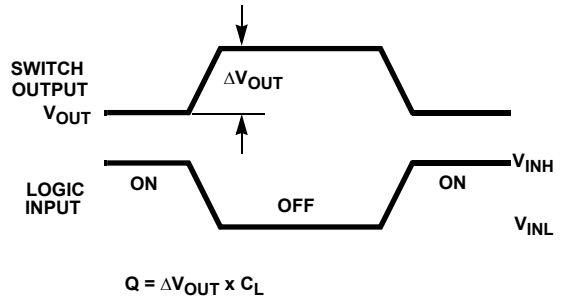


FIGURE 2A. MEASUREMENT POINTS

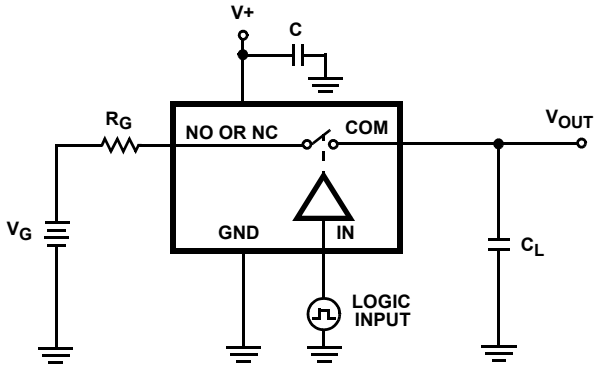


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

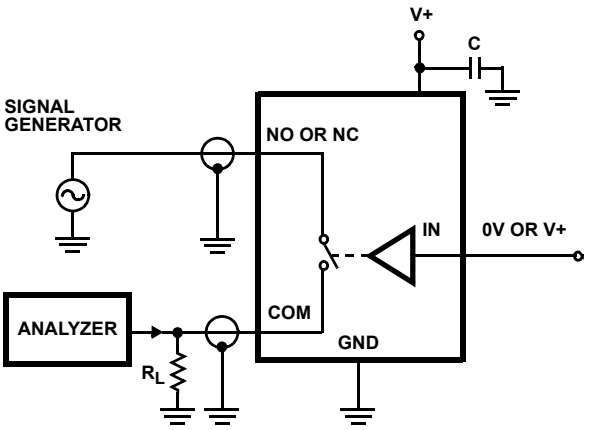


FIGURE 3. OFF ISOLATION TEST CIRCUIT

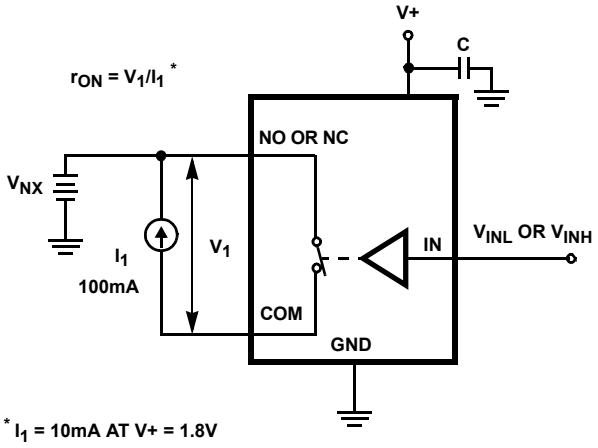


FIGURE 4. r_{ON} TEST CIRCUIT

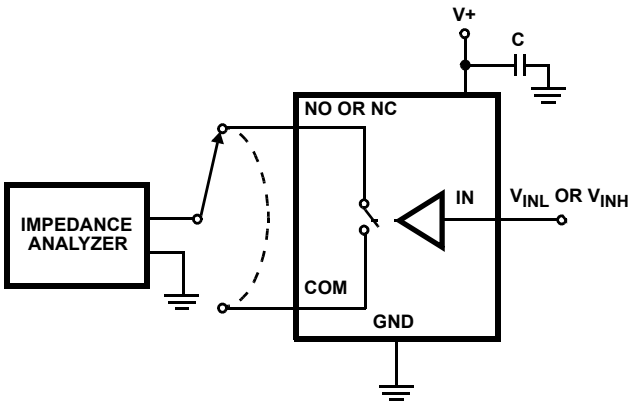


FIGURE 5. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL54501 and ISL54502 are bi-directional, single pole/single throw (SPST) analog switches. They offer precise switching capability from a single 1.62V to 5.5V supply with low ON-resistance and high speed operation. With a single supply of 5V the typical ON-resistance is only 5Ω, with a typical turn-on and turn-off time of: t_{ON} = 22ns, t_{OFF} = 15ns. The devices are especially well suited for portable battery powered equipment due to their low operating supply voltage (1.62V), low power consumption (0.11µW), low leakage currents (300nA max), and tiny µTDFN package.

The ISL54501 is a single normally open (NO) SPST analog switch. The ISL54502 is a single normally closed (NC) SPST analog switch.

External V+ Series Resistor

For improved ESD and latch-up immunity, Intersil recommends adding a 100Ω resistor in series with the V+ power supply pin of the ISL54501, ISL54502 IC (see Figure 6).

During an overvoltage transient event (such as occurs during system level IEC 61000 ESD testing), substrate currents can be generated in the IC that can trigger parasitic SCR structures to turn ON, creating a low impedance path from the V+ power supply to ground. This will result in a significant amount of current flow in the IC, which can potentially create a latch-up state or permanently damage the IC. The external V+ resistor limits the current during this over-stress situation and has been found to prevent latch-up or destructive damage for many over voltage transient events.

Under normal operation the sub-microamp I_{DD} current of the IC produces an insignificant voltage drop across the 100Ω series resistor resulting in no impact to switch operation or performance.

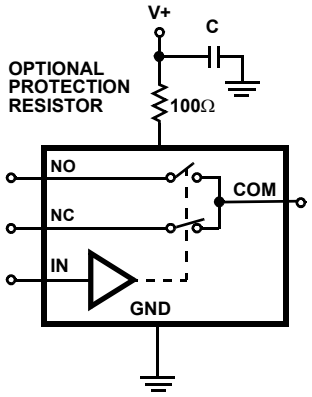


FIGURE 6. V+ SERIES RESISTOR FOR ENHANCED ESD AND LATCH-UP IMMUNITY

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents, which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 7). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 7). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting Schottky diodes to the signal pins (as shown in Figure 9) will shunt the fault current to the supply or to ground, thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current.

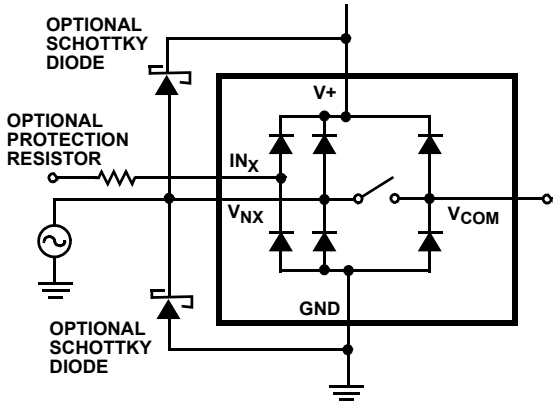


FIGURE 7. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL54501, ISL54502 construction is typical of most single supply CMOS analog switches in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL54501, ISL54502 5.5V maximum supply voltage provides plenty of room for the 10% tolerance of 3.6V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.8V ± 10% but the part will operate with a supply below 1.62V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the "Electrical Specifications" tables starting on page 4 the and "Typical Performance Curves" starting on page 9 for details.

V+ and GND also power the internal logic and level shiftier. The level shiftier converts the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2V to 3.6V (see Figure 14). At 3.6V the V_{IH} level is about 0.98V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, the ISL54501, ISL54502 has a -3dB bandwidth of 350MHz (see Figure 15). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch behaves like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to output. Off isolation is the resistance of this signal feedthrough. Figure 16 details the high off isolation provided by the ISL54501, ISL54502. At 1MHz, off isolation is about 75dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

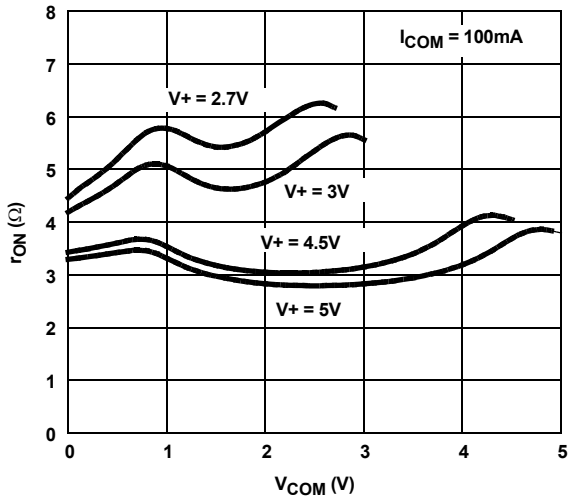


FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

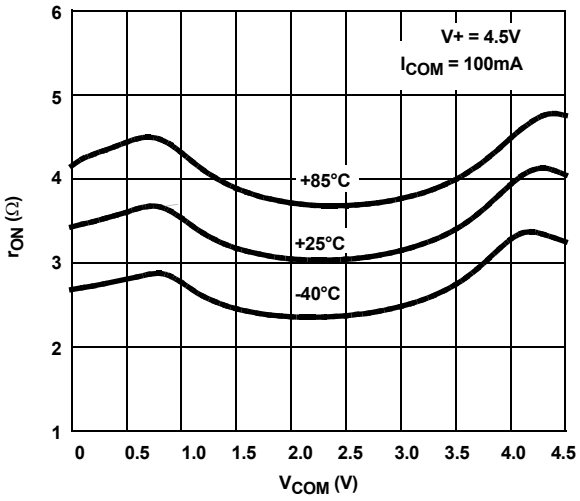


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified (Continued)

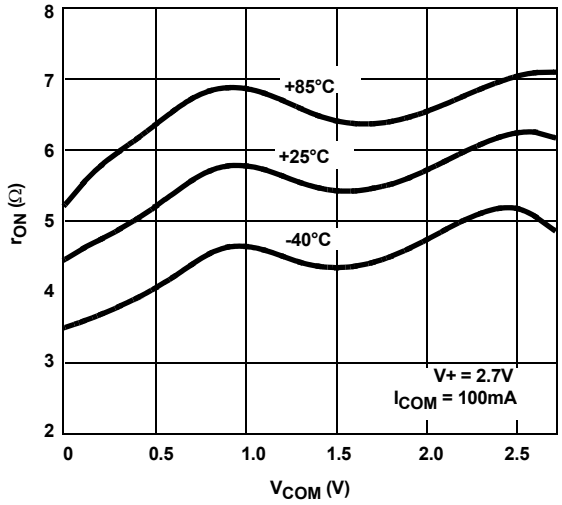


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

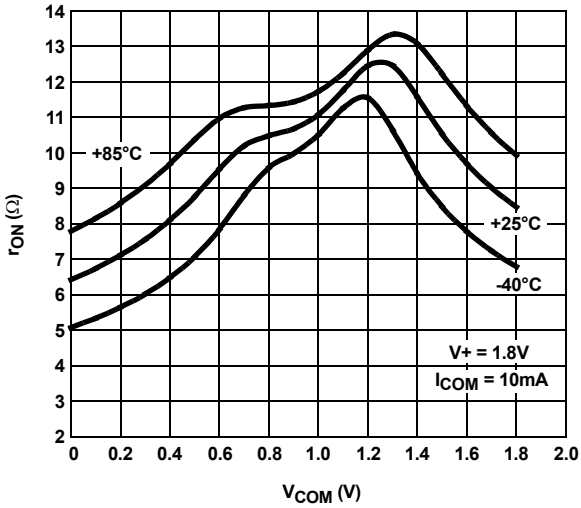


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

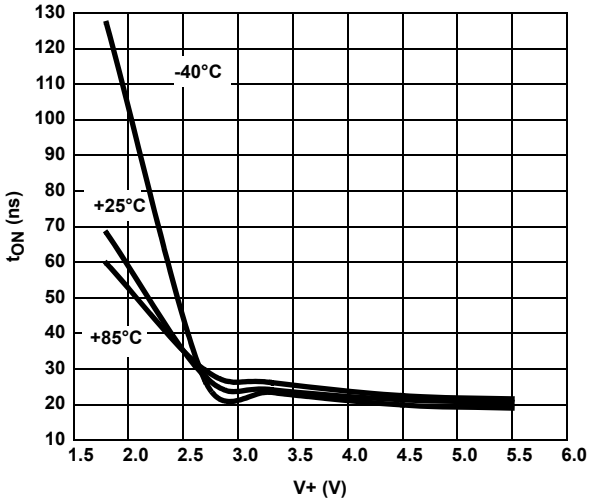


FIGURE 12. TURN-ON TIME vs SUPPLY VOLTAGE

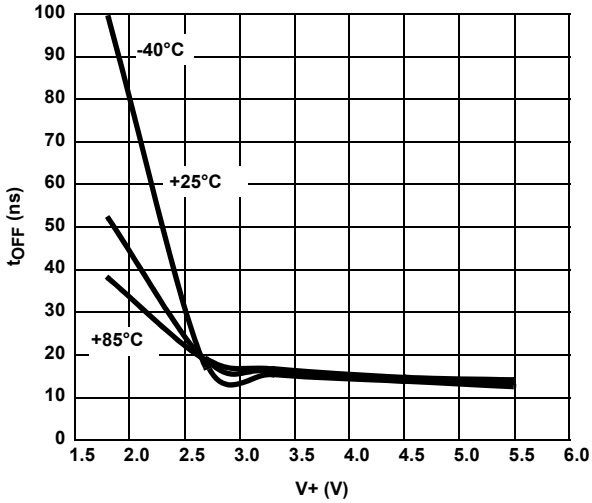


FIGURE 13. TURN-OFF TIME vs SUPPLY VOLTAGE

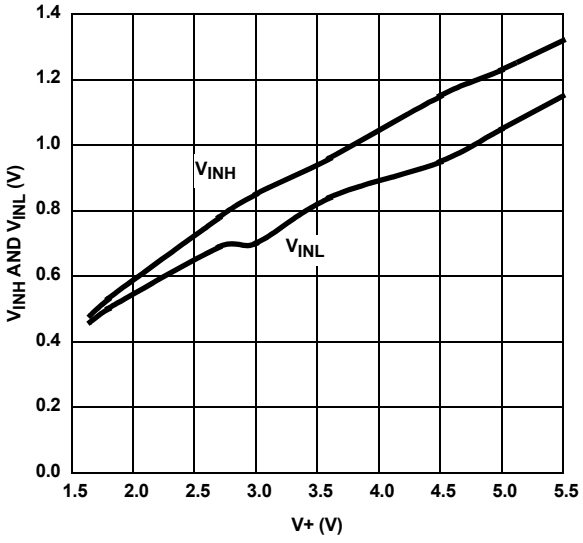


FIGURE 14. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

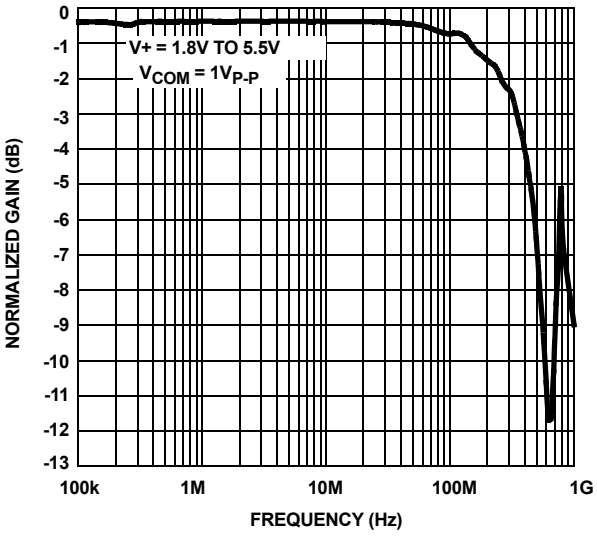


FIGURE 15. FREQUENCY RESPONSE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified (Continued)

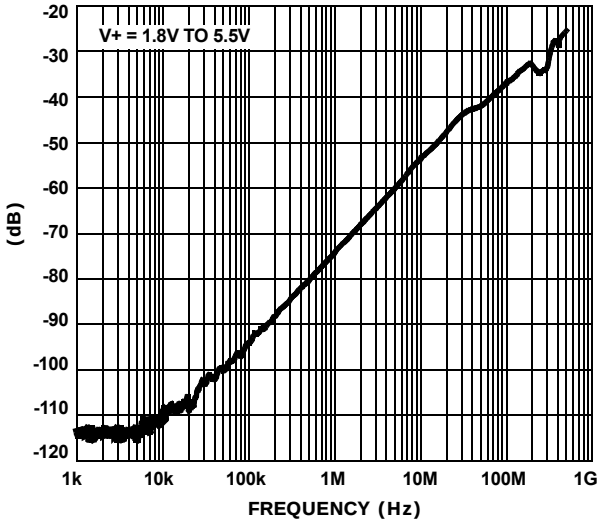


FIGURE 16. OFF ISOLATION

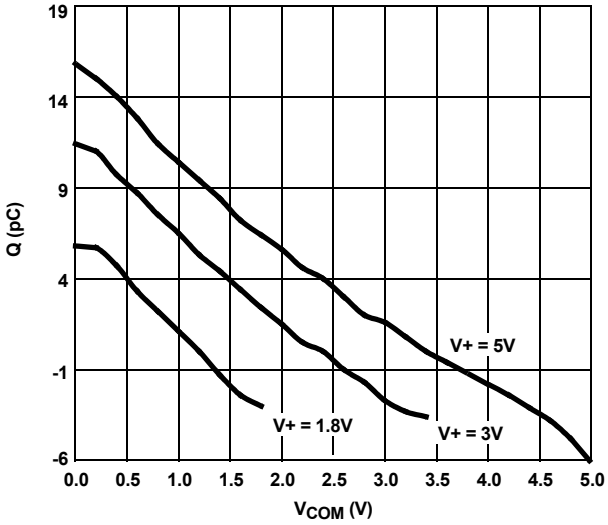


FIGURE 17. CHARGE INJECTION vs SWITCH VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

57

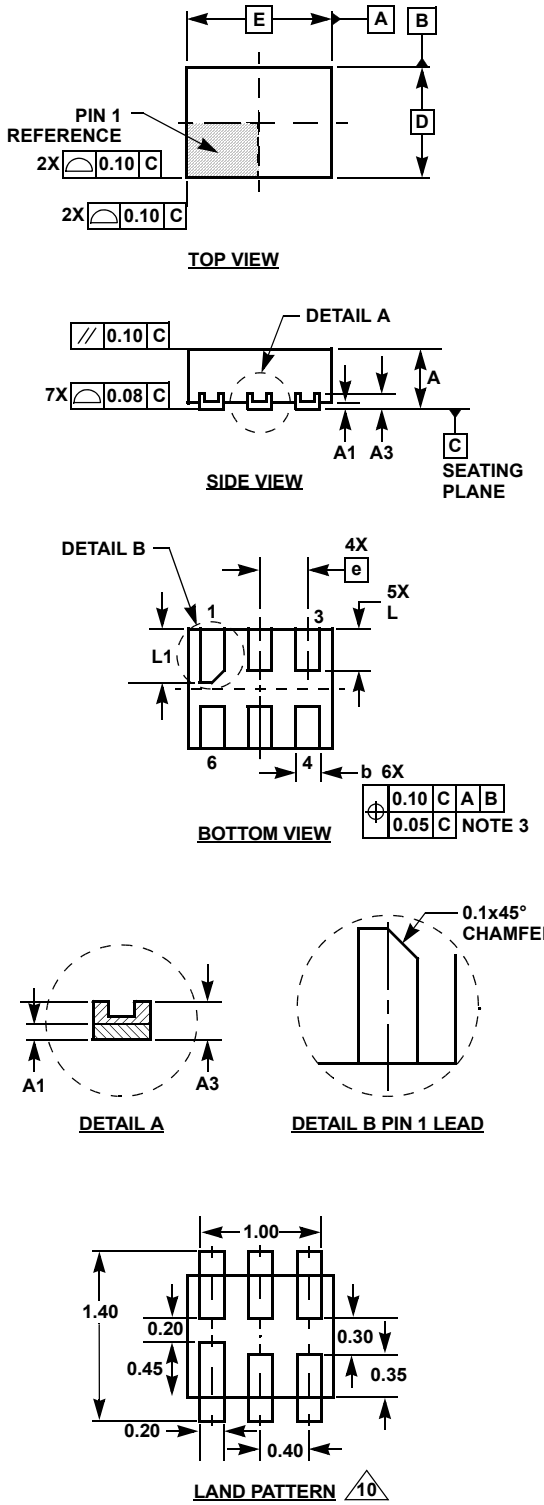
PROCESS:

Submicron CMOS

Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)

L6.1.2x1.0A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE



SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	0.95	1.00	1.05	-
E	1.15	1.20	1.25	-
e		0.40 BSC		-
L	0.30	0.35	0.40	-
L1	0.40	0.45	0.50	-
N		6		2
Ne		3		3
θ	0	-	12	4

Rev. 2 8/06

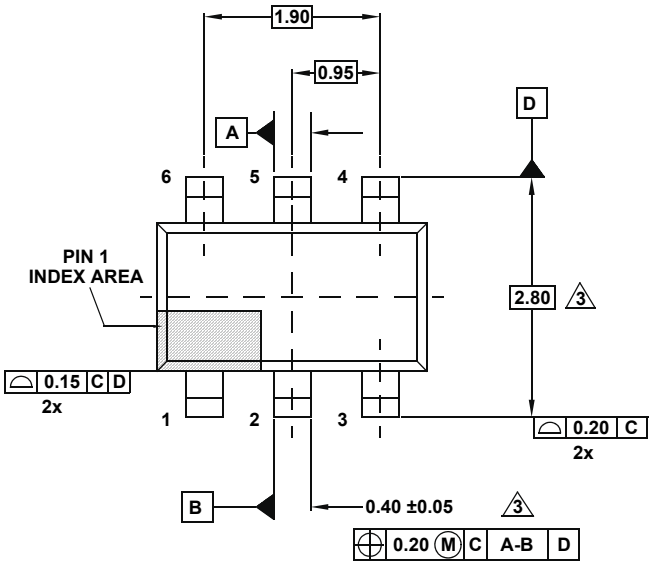
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Ne refers to the number of terminals on E side.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

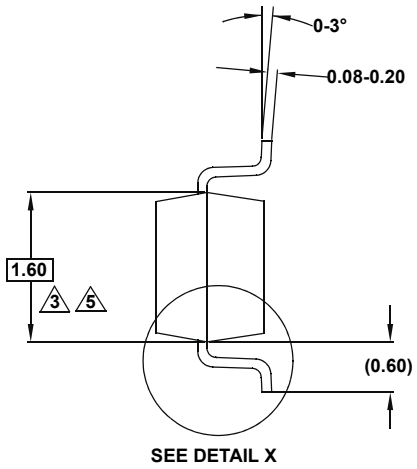
Package Outline Drawing

P6.064A

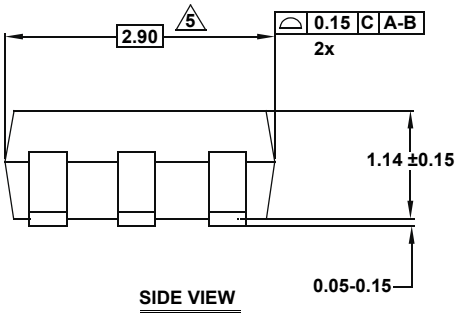
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



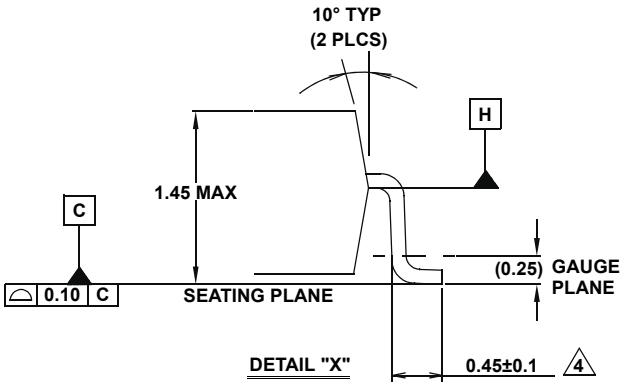
TOP VIEW



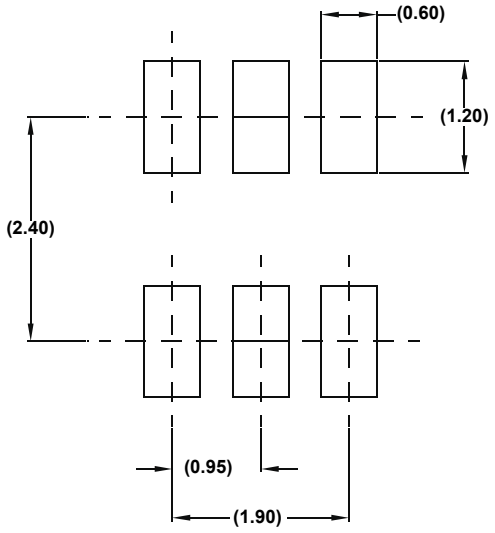
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.