ISL55002

High Supply Voltage 200MHz Unity-Gain Stable Operational Amplifier

FN7497
Rev 4.00
July 27, 2006

The ISL55002 is a high speed, low power, low cost monolithic operational amplifier. The ISL55002 is unity-gain stable and features a 300V/µs slew rate and 200MHz bandwidth while requiring only 8.5mA of supply current per amplifier.

The power supply operating range of the ISL55002 is from ±15V down to ±2.5V. For single-supply operation, the ISL55002 operates from 30V down to 5V.

The ISL55002 also features an extremely wide output voltage swing of -12.75V/+13.4V with V_S = ±15V and R_L = 1kΩ.

At a gain of +1, the ISL55002 has a -3dB bandwidth of 200MHz with a phase margin of 55°. Because of its conventional voltage-feedback topology, the ISL55002 allow the use of reactive or non-linear elements in its feedback network. This versatility combined with low cost and 140mA of output-current drive makes the ISL55002 an ideal choice for price-sensitive applications requiring low power and high speed.

The ISL55002 is available in an 8 Ld SO package and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL55002IB	55002IB	-	8 Ld SO	MDP0027
ISL55002IB-T7	55002IB	7”	8 Ld SO	MDP0027
ISL55002IB-T13	55002IB	13”	8 Ld SO	MDP0027
ISL55002IBZ (See Note)	55002IBZ	-	8 Ld SO (Pb-Free)	MDP0027
ISL55002IBZ-T7 (See Note)	55002IBZ	7”	8 Ld SO (Pb-Free)	MDP0027
ISL55002IBZ-T13 (See Note)	55002IBZ	13”	8 Ld SO (Pb-Free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

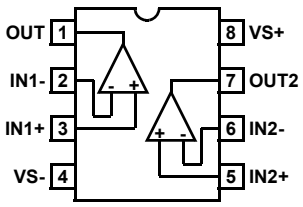
- 200MHz -3dB bandwidth
- Unity-gain stable
- Low supply current: 8.5mA per amplifier
- Wide supply range: ±2.5V to ±15V dual-supply and 5V to 30V single-supply
- High slew rate: 300V/µs
- Fast settling: 75ns to 0.1% for a 10V step
- Wide output voltage swing: -12.75V/+13.4V with V_S = ±15V, R_L = 1kΩ
- Enhanced replacement for EL2244
- Pb-free plus anneal available (RoHS compliant)

Applications

- Video amplifiers
- Single-supply amplifiers
- Active filters/integrators
- High speed sample-and-hold
- High speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- Difference amplifiers

Pinout

ISL55002
(8 LD SO)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S) . . . . . ±16.5V or 33V
Input Voltage (V_{IN}) . . . . . .±V_S
Differential Input Voltage (dV_{IN}) . . . . . .±10V
Continuous Output Current 60mA
Power Dissipation (P_D) . . . . . See Curves
Operating Temperature Range (T_A) . . . . . .-40°C to +85°C
Operating Junction Temperature (T_J) . . . . . .+150°C
Storage Temperature (T_{ST}) . . . . . .-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S = ±15V, A_V = +1, R_L = 1kΩ, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_S = ±15V		1.2	5	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)	-40°C to +85°C		17		µV/°C
I_B	Input Bias Current	V_S = ±15V		0.6	3.5	µA
I_{OS}	Input Offset Current	V_S = ±15V		0.2	2	µA
TCI_{OS}	Average Offset Current Drift (Note 1)			0.2		nA/°C
A_{VOL}	Open-loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1kΩ	12000	21000		V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	75	100		dB
CMRR	Common-mode Rejection Ratio	V_{CM} = ±10V, V_{OUT} = 0V	75	90		dB
CMIR	Common-mode Input Range	V_S = ±15V		13		V
V_{OUT}	Output Voltage Swing	V_O+, R_L = 1kΩ	13.25	13.4		V
		V_O-, R_L = 1kΩ	-12.6	-12.75		V
		V_O+, R_L = 150Ω	9.6	10.7		V
		V_O-, R_L = 150Ω	-8.3	-9.4		V
I_{SC}	Output Short Circuit Current		80	140		mA
I_S	Supply Current (per amplifier)	V_S = ±15V, no load		8.5	9.25	mA
R_{IN}	Input Resistance		2.0	3.2		MΩ
C_{IN}	Input Capacitance	A_V = +1		1		pF
R_{OUT}	Output Resistance	A_V = +1		50		mΩ
PSOR	Power Supply Operating Range	Dual supply	±2.25		±15	V
		Single supply	4.5		30	V

NOTE:

1. Measured from T_{MIN} to T_{MAX}.

AC Electrical Specifications

V_S = ±15V, A_V = +1, R_L = 1kΩ, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth (V_{OUT} = 0.4V_{PP})	V_S = ±15V, A_V = +1		200		MHz
		V_S = ±15V, A_V = -1		50		MHz
		V_S = ±15V, A_V = +2		50		MHz
		V_S = ±15V, A_V = +5		17		MHz
GBWP	Gain Bandwidth Product	V_S = ±15V		70		MHz
PM	Phase Margin	R_L = 1kΩ, C_L = 5pF		55		°
SR	Slew Rate (Note 1)		260	300		V/µs

AC Electrical Specifications V_S = ±15V, A_V = +1, R_L = 1kΩ, T_A = 25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
FPBW	Full-power Bandwidth (Note 2)	V_S = ±15V		9.5		MHz
t_S	Settling to +0.1% (A_V = +1)	V_S = ±15V, 10V step		75		ns
dG	Differential Gain (Note 3)	NTSC/PAL		0.01		%
dP	Differential Phase	NTSC/PAL		0.05		°
eN	Input Noise Voltage	10kHz		12		nV/√Hz
iN	Input Noise Current	10kHz		1.5		pA/√Hz

NOTES:

1. Slew rate is measured on rising edge.
2. For V_S = ±15V, V_{OUT} = $10V_{PP}$, for V_S = ±5V, V_{OUT} = $5V_{PP}$. Full-power bandwidth is based on slew rate measurement using FPBW = SR/(2π * V_{PEAK}).
3. Video performance measured at V_S = ±15V, A_V = +2 with two times normal video level across R_L = 150Ω. This corresponds to standard video levels across a back-terminated 75Ω load. For other values or R_L, see curves.

Typical Performance Curves

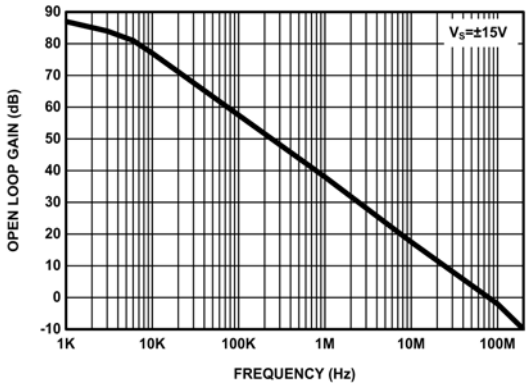


FIGURE 1. OPEN-LOOP GAIN vs FREQUENCY

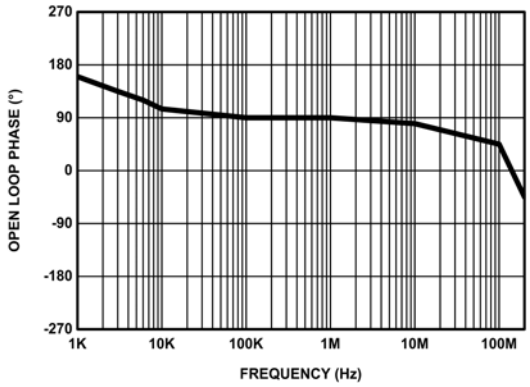


FIGURE 2. OPEN-LOOP PHASE vs FREQUENCY

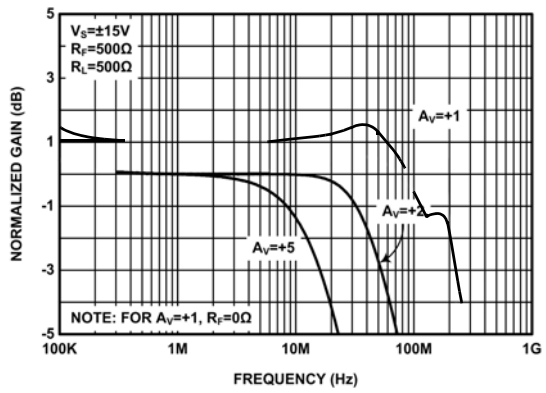


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS NON-INVERTING GAIN SETTINGS

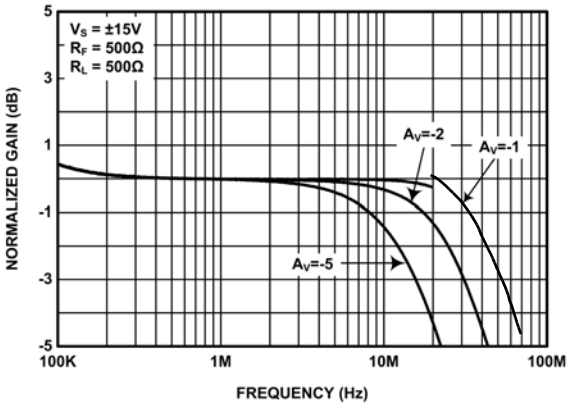


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS INVERTING GAIN SETTINGS

Typical Performance Curves (Continued)

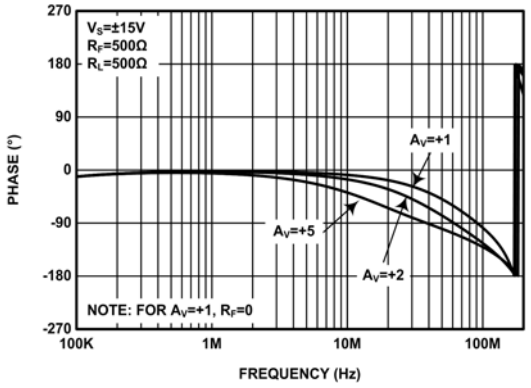


FIGURE 5. PHASE vs FREQUENCY FOR VARIOUS NON-INVERTING GAIN SETTINGS

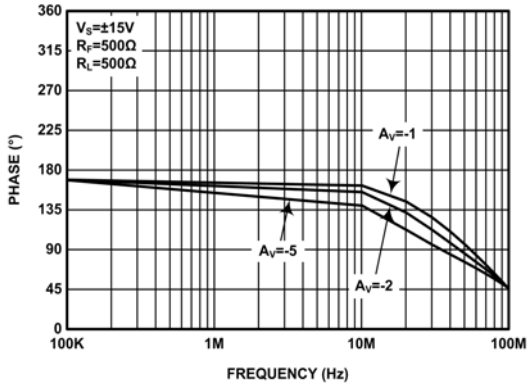


FIGURE 6. PHASE vs FREQUENCY FOR VARIOUS INVERTING GAIN SETTINGS

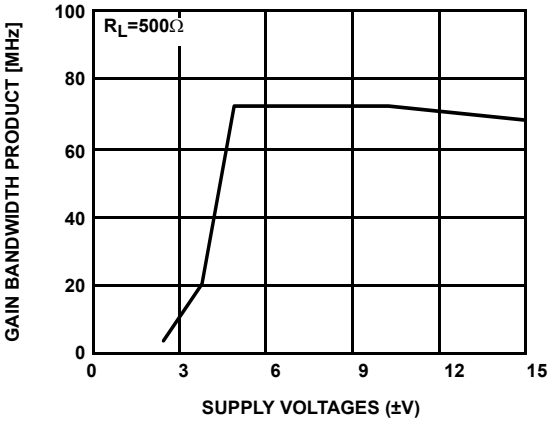


FIGURE 7. GAIN BANDWIDTH PRODUCT vs SUPPLY

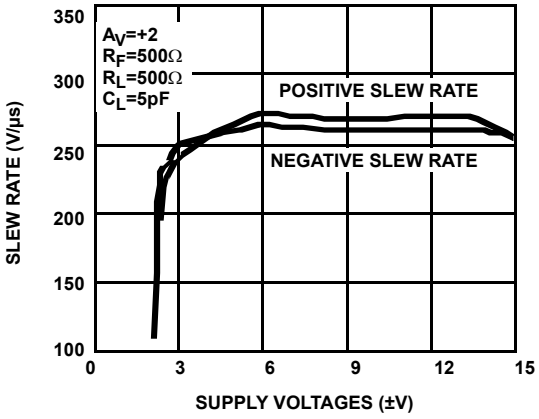


FIGURE 8. SLEW RATE vs SUPPLY

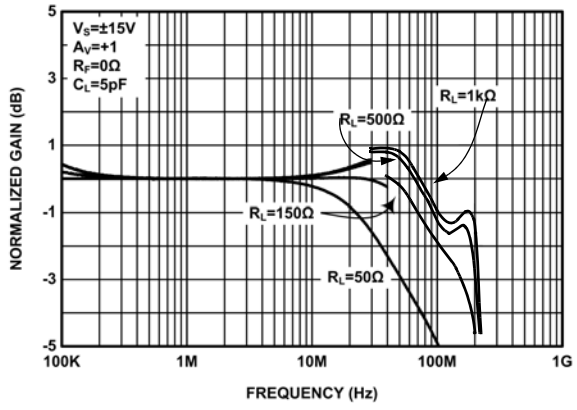


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +1)

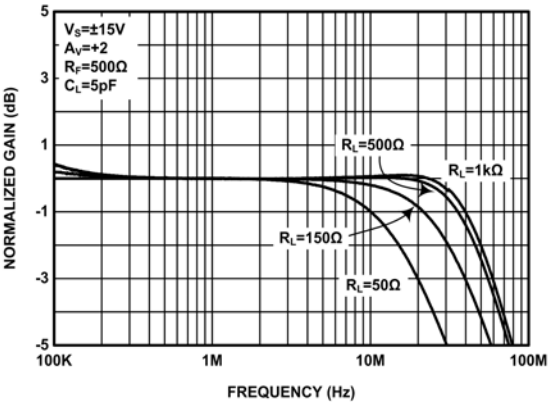


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +2)

Typical Performance Curves (Continued)

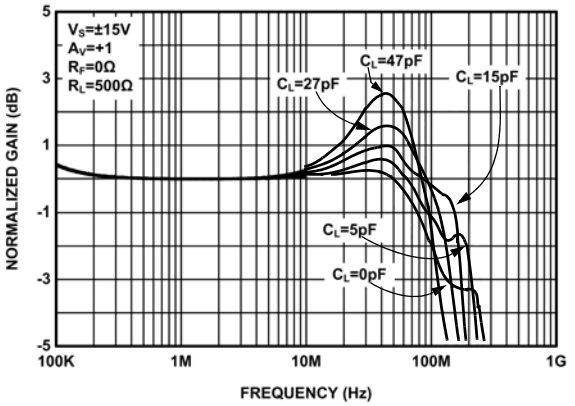


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +1)

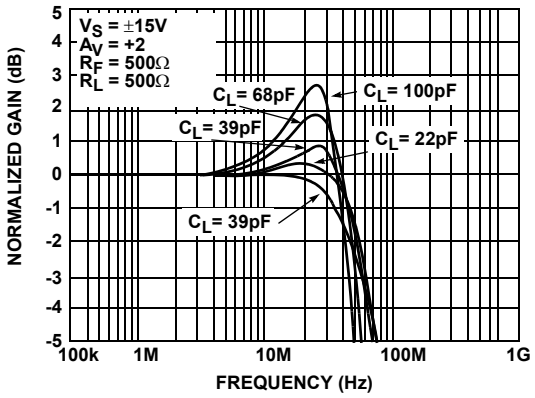


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +2)

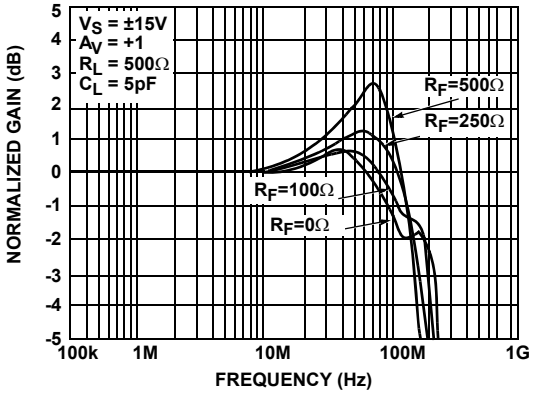


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS $R_{FEEDBACK}$ (A_V = +1)

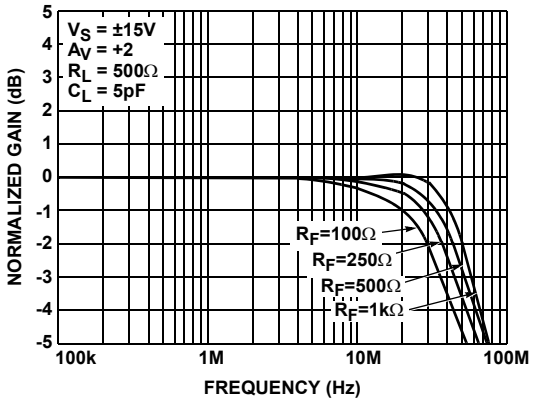


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS $R_{FEEDBACK}$ (A_V = +2)

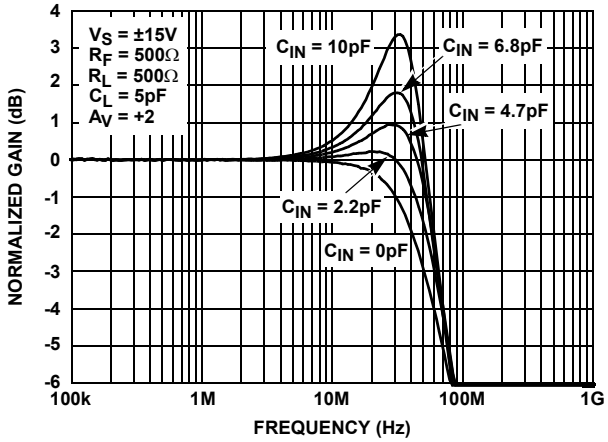


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS INVERTING INPUT CAPACITANCE (C_{IN})

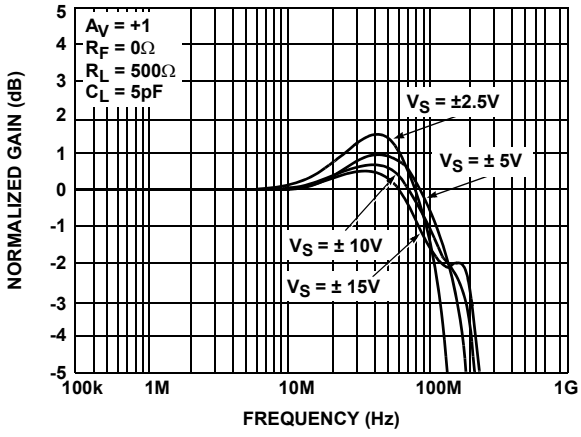


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS SUPPLY SETTINGS

Typical Performance Curves (Continued)

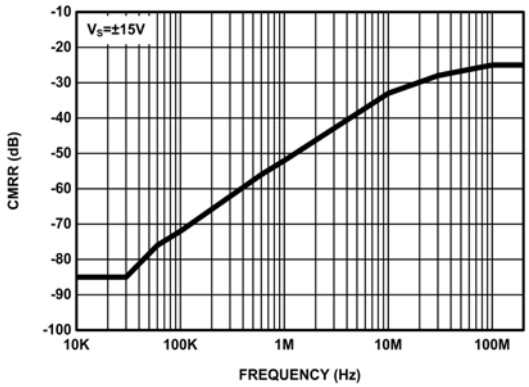


FIGURE 17. COMMON-MODE REJECTION RATIO (CMRR)

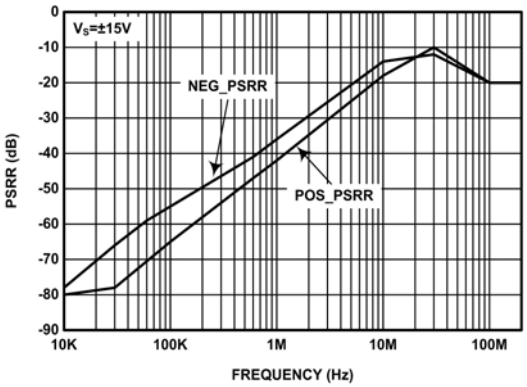


FIGURE 18. POWER SUPPLY REJECTION RATIO (PSRR)

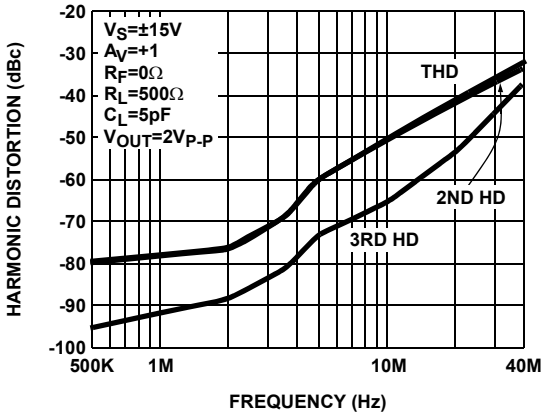


FIGURE 19. HARMONIC DISTORTION vs FREQUENCY (A_V = +1)

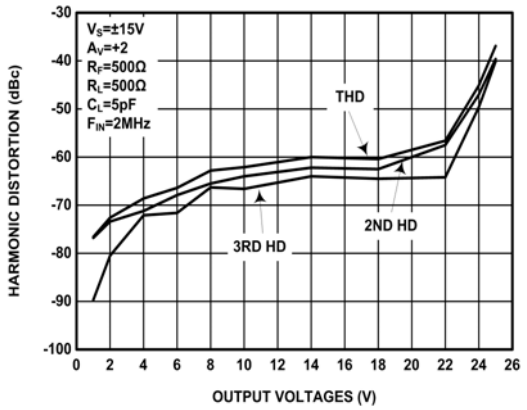


FIGURE 20. HARMONIC DISTORTION vs OUTPUT VOLTAGE (A_V = +2)

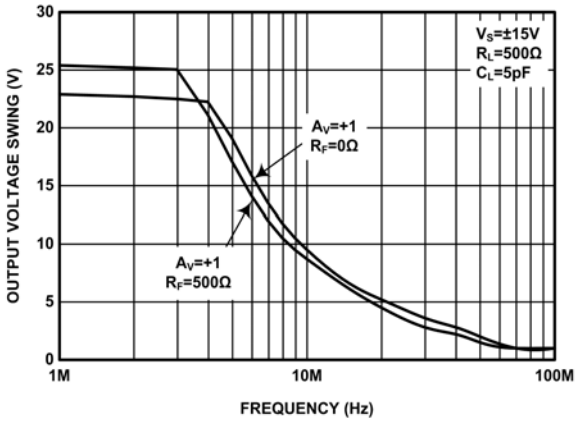


FIGURE 21. OUTPUT SWING vs FREQUENCY FOR VARIOUS GAIN SETTINGS

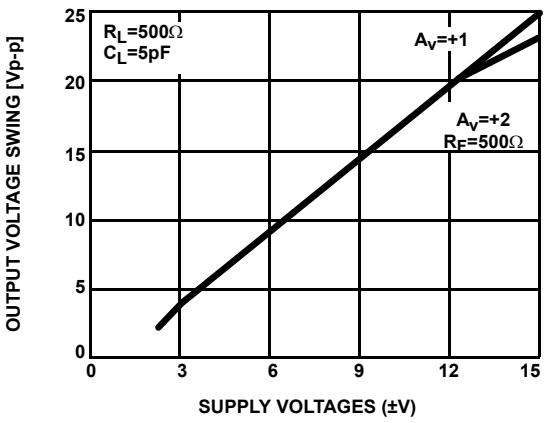


FIGURE 22. OUTPUT SWING vs SUPPLY VOLTAGE FOR VARIOUS GAIN SETTINGS

Typical Performance Curves (Continued)

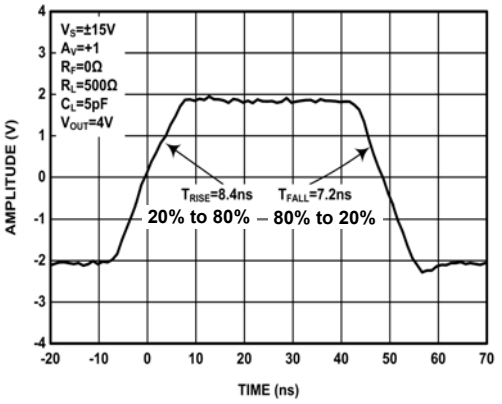


FIGURE 23. LARGE SIGNAL RISE AND FALL TIMES

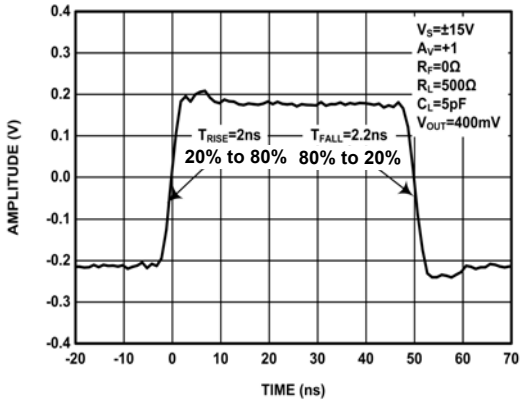


FIGURE 24. SMALL SIGNAL RISE AND FALL TIMES

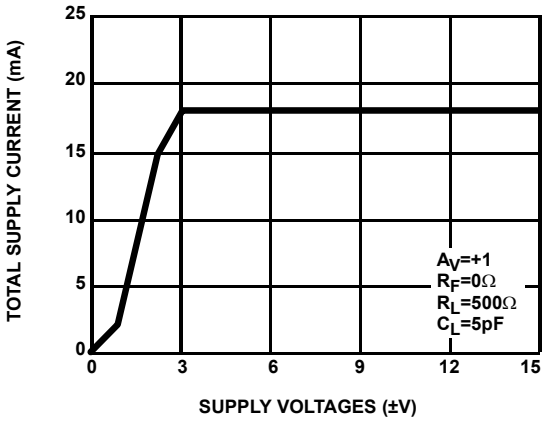


FIGURE 25. SUPPLY CURRENT vs SUPPLY VOLTAGE

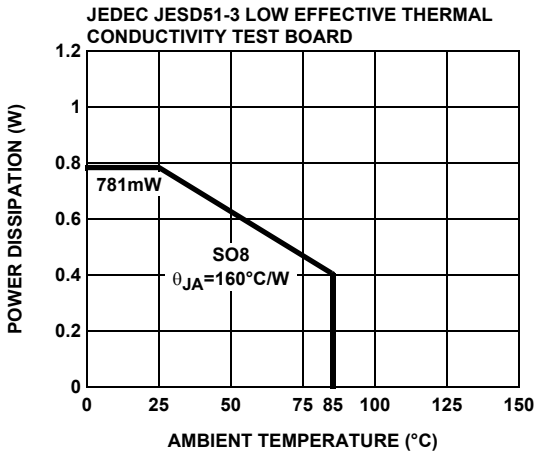


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

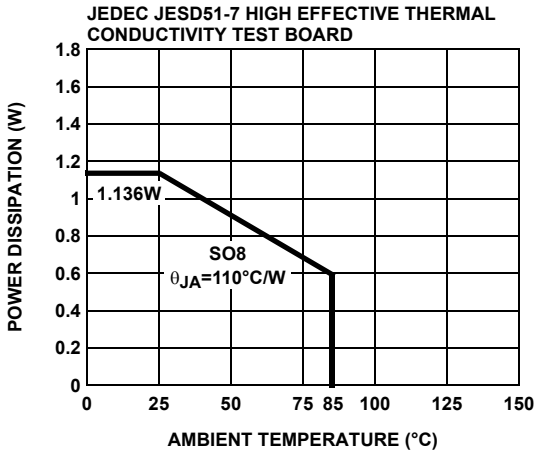


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Product Description

The ISL55002 is a wide bandwidth, low power, and low offset voltage feedback operational amplifier. This device is internally compensated for closed loop gain of +1 or greater. Connected in voltage follower mode and driving a 500Ω load, the -3dB bandwidth is around a 200MHz. Driving a 150Ω load and a gain of 2, the bandwidth is about 90MHz while maintaining a 300V/µs slew rate.

The ISL55002 is designed to operate with supply voltage from +15V to -15V. That means for single supply application, the supply voltage is from 0V to 30V. For split supplies application, the supply voltage is from ±15V. The amplifier has an input common-mode voltage range from 1.5V above the negative supply (V_S- pin) to 1.5V below the positive supply (V_S+ pin). If the input signal is outside the above specified range, it will cause the output signal to be distorted.

The outputs of the ISL55002 can swing from -12.75V to +13.4V for V_S = ±15V. As the load resistance becomes lower, the output swing is lower.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the output pin to the inverting input pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F can't be very big for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico Farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth. For gain of +1, R_F = 0 is optimum. For the gains other than +1, optimum response is obtained with R_F with proper selection of R_F and R_G (see Figures15 and 16 for selection).

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. The dG and dP of this device is about 0.01% and 0.05°, while driving 150Ω at a gain of 2. Driving high impedance loads would give a similar or better dG and dP performance.

Driving Capacitive Loads and Cables

The ISL55002 can drive a 47pF load in parallel with 500Ω with less than 3dB of peaking at gain of +1 and as much as 100pF at a gain of +2 with under 3db of peaking. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with the output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Output Drive Capability

The ISL55002 does not have internal short circuit protection circuitry. It has a typical short circuit current of 140mA. If the output is shorted indefinitely, the power dissipation could easily overheat the die or the current could eventually compromise metal integrity. Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnect. Note that in transient applications, the part is robust.

Short circuit protection can be provided externally with a back match resistor in series with the output placed close as possible to the output pin. In video applications this would be a 75Ω resistor and will provide adequate short circuit protection to the device. Care should still be taken not to stress the device with a short at the output.

Power Dissipation

With the high output drive capability of the ISL55002, it is possible to exceed the 150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

For sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_{OUTi} - V_S) \times I_{LOADi}$$

Where:

- V_S = Supply voltage
- I_{SMAX} = Maximum quiescent supply current
- V_{OUT} = Maximum output voltage of the application
- R_{LOAD} = Load resistance tied to ground
- I_{LOAD} = Load current
- N = number of amplifiers (max = 2)

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

Printed Circuit Board Layout

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Application Circuits

Sallen Key Low Pass Filter

A common and easy to implement filter taking advantage of the wide bandwidth, low offset and low power demands of the ISL55002. A derivation of the transfer function is provided for convenience (See Figure 28).

Sallen Key High Pass Filter

Again this useful filter benefits from the characteristics of the ISL55002. The transfer function is very similar to the low pass so only the results are presented (See Figure 29).

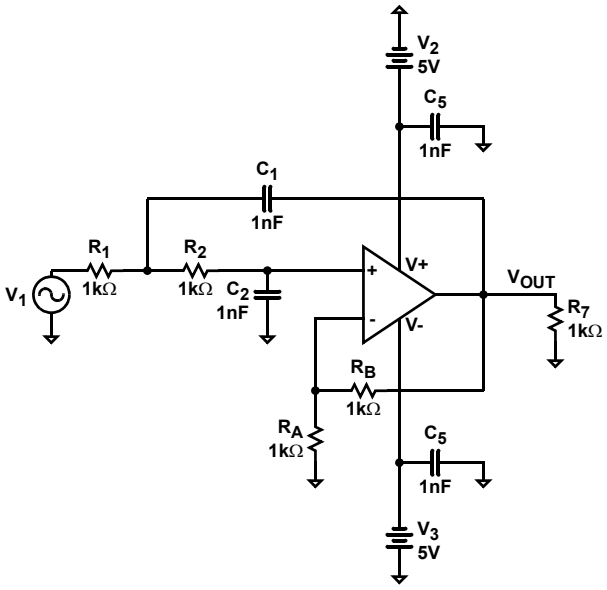


FIGURE 28. SALLEN-KEY LOW PASS FILTER

$$K = 1 + \frac{RB}{RA}$$

$$Vo = K\frac{1}{R2C2s + 1}V1$$

$$\frac{V1 - Vi}{R1}1 + \frac{\frac{Vo}{K - V1}}{R2} + \frac{Vo - Vi}{\frac{1}{C1s}} = 0$$

$$H(s) = \frac{K}{R1C1R2C2s^2 + ((1-K)R1C1 + R1C2 + R21C2)s + 1}$$

$$H(jw) = \frac{1}{1 - w^2R1C1R2C2 + jw((1-K)R1C1 + R1C2 + R2C2)}$$

$$Holp = K$$

$$wo = \frac{1}{\sqrt{R1C1R2C2}}$$

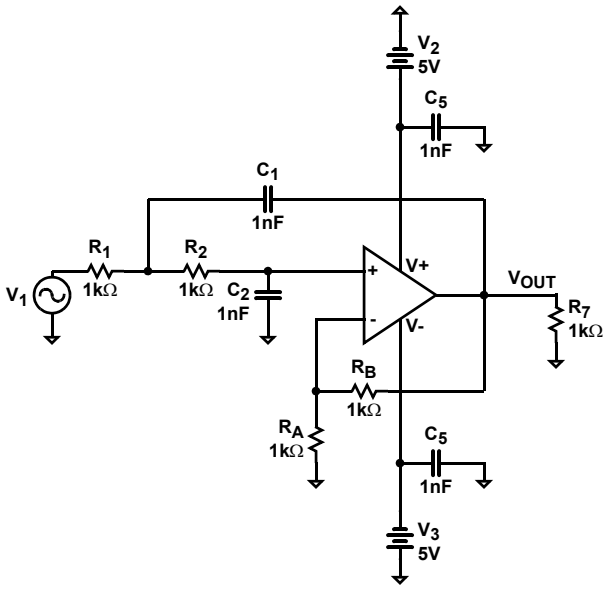
$$Q = \frac{1}{(1-K)\sqrt{\frac{R1C1}{R2C2}} + \sqrt{\frac{R1C2}{R2C1}} + \sqrt{\frac{R2C2}{R1C1}}}$$

$$Holp = K$$

$$wo = \frac{1}{RC}$$

$$Q = \frac{1}{3 - K}$$

Equations simplify if we let all components be equal R=C



$$Holp = K$$

$$wo = \frac{1}{\sqrt{R1C1R2C2}}$$

$$Q = \frac{1}{(1-K)\sqrt{\frac{R1C1}{R2C2}} + \sqrt{\frac{R1C2}{R2C1}} + \sqrt{\frac{R2C2}{R1C1}}}$$

$$Holp = \frac{K}{4-K}$$

$$wo = \frac{\sqrt{2}}{RC}$$

Equations simplify if we let all components be equal R=C

$$Q = \frac{\sqrt{2}}{4-K}$$

FIGURE 29. SALLEN-KEY HIGH PASS FILTER

Differential Output Instrumentation Amplifier

The addition of a third amplifier to the conventional three amplifier instrumentation amplifier introduces the benefits of differential signal realization, specifically the advantage of using common-mode rejection to remove coupled noise and ground potential errors inherent in remote transmission. This configuration also provides enhanced bandwidth, wider output swing and faster slew rate than conventional three amplifier solutions with only the cost of an additional amplifier and few resistors.

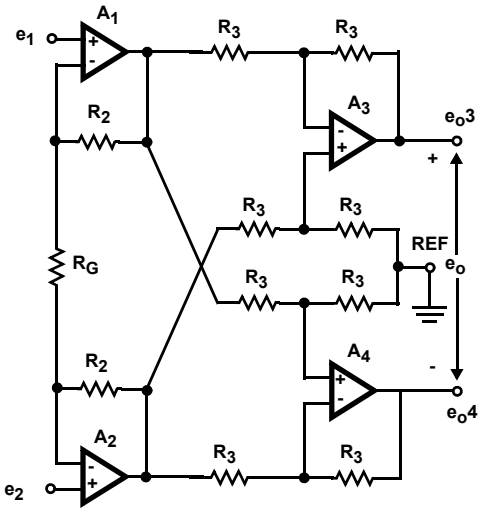


FIGURE 30. DIFFERENTIAL OUTPUT AMPLIFIER

$$e_{o3} = -(1 + 2R_2/R_G)(e_1 - e_2) \qquad e_{o4} = (1 + 2R_2/R_G)(e_1 - e_2)$$

$$e_o = -2(1 + 2R_2/R_G)(e_1 - e_2)$$

$$BW = \frac{2f_{C1,2}}{|A_{Di}|} \qquad A_{Di} = -2(1 + 2R_2/R_G)$$

Strain Gauge

The strain gauge is an ideal application to take advantage of the moderate bandwidth and high accuracy of the ISL55002. The operation of the circuit is very straightforward. As the strain variable component resistor in the balanced bridge is subjected to increasing strain, its resistance changes, resulting in an imbalance in the bridge. A voltage variation from the referenced high accuracy source is generated and translated to the difference amplifier through the buffer stage. This voltage difference as a function of the strain is converted into an output voltage.

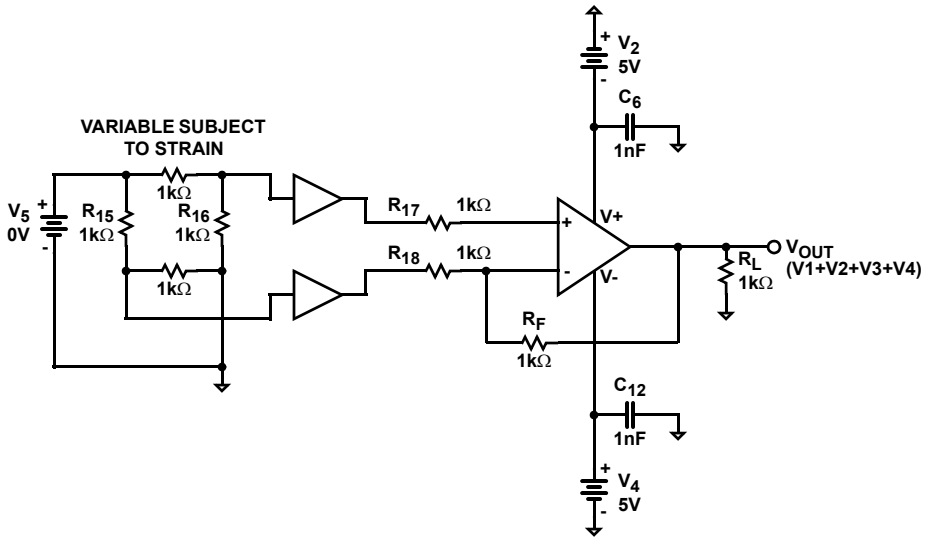
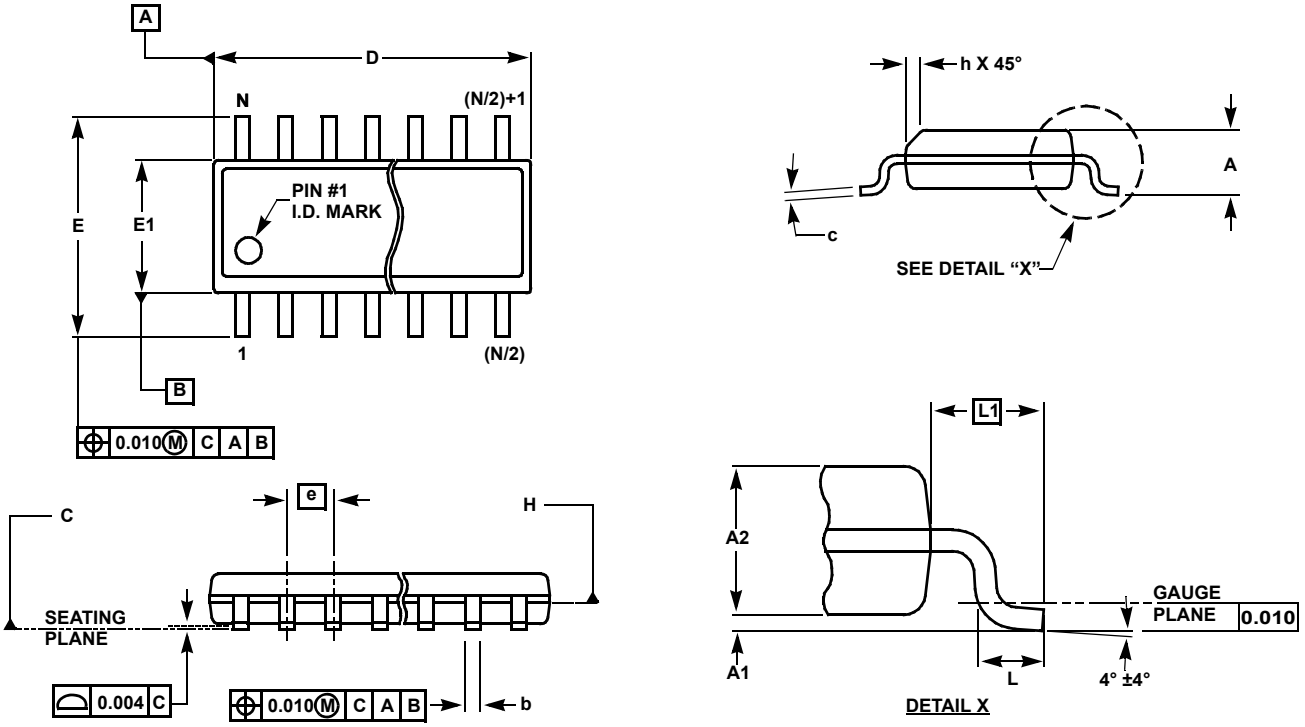


FIGURE 31. STRAIN GAUGE

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994