ISL58328

5V Wide Optical Spectrum Laser Power Monitor IC

FN6329
Rev 2.00
Jul 29, 2013

The ISL58328 photo sensor IC has a wide optical spectral sensitivity from 400nm to 1000nm. It is good for multiple light sources application, such as laser based projectors. ISL58328 has two banks of three sets of gain registers. For a Pico-Projector application, the two banks of gain resistors can be used to monitor bias level and peak level of each wavelength. Bank switching is done by applying a TTL compatible logic signal to HL pin. The three sets of gain registers can be used to adjust optical-to-electrical conversion gain for each RED, GREEN, and BLUE laser or any wavelength in a spectral range for application. The ISL58328 is a single die device that has a photo detector of 0.7mm diameter in the center of the die. Photo current signal is amplified through TIA, fine gain amplifier, and output drivers to convert from current to voltage. The output of ISL58328 can be configured to be either differential or single-ended. Gain changing according to each wavelength is done through 3-wire interface. Registers can be updated in real time while the device is in operation.

The ISL58328 operates from a single +5.0V supply. It is available in a space-saving 9 ball glass top BGA package.

Related Literature

- AN1356, “Serial Bus Specification”
- AN1448, “BD/HD-DVD/DVD/CD PMIC”

Features

- High Sensitivity from 400nm to 1000nm with Patented Technology for Improved Blue Photo Response
- Differential Voltage Output or Single-Ended Output
- Internal Output Reference or External Output Reference
- Single +5V Power Supply
- Serial Interface for Gain Calibration
- Fast Settling Time < 20ns
- Wide Signal Bandwidth > 80MHz
- Wide Signal Gain Dynamic Range > 25dB
- Low Power Consumption
- Low Output Offset < 50mV
- Small 9-Ball Optical Chip Scale Package (OCSP) (2.2mmx2.2mm)
- SPI 3-wire Serial Interface

Applications

- Optical Power Monitoring
- Laser Based Pico-Projectors or Projection TV
- Laser Auto Power Control for Laser Based Application
- White Balance for LED Based LCos and DLP Pico-Projectors

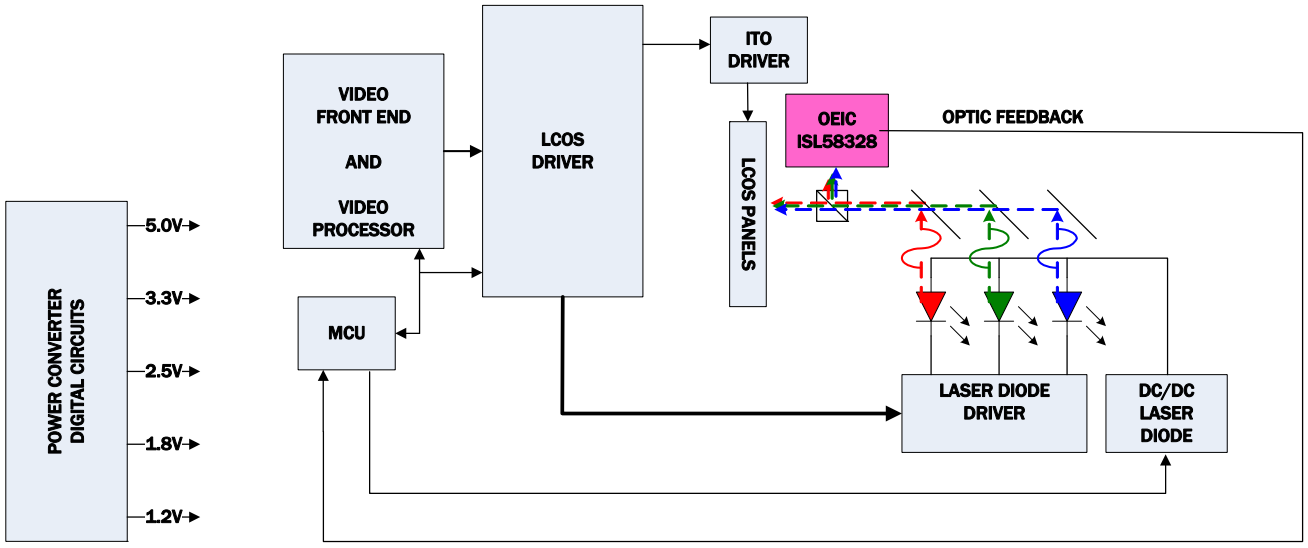
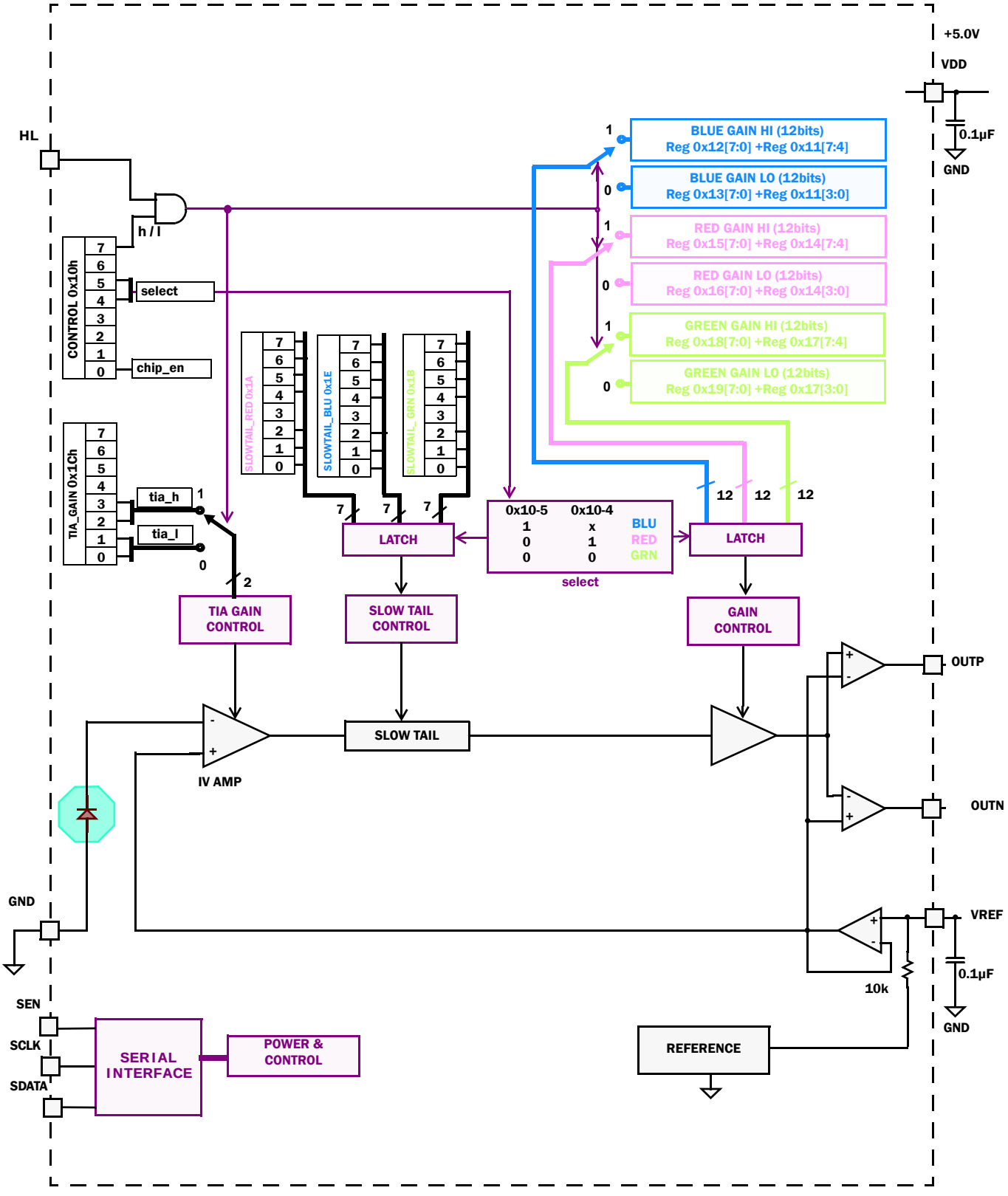


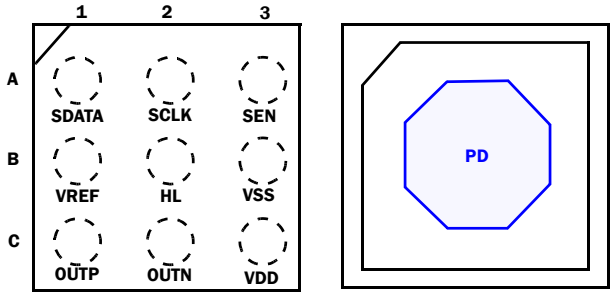
FIGURE 1. APPLICATION BLOCK DIAGRAM

Block Diagram



Pin Configuration

ISL58328
(9 BALL OCSP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
A1	SDATA	Digital I/O	Serial interface data, bi-directional
B1	VREF	Analog Input	Reference voltage input
C1	OUTP	Analog Output	Positive swing analog output
A2	SCLK	Digital Input	Serial interface clock
B2	HL	Digital Input	HIGH/LOW gain mode selection, H = High gain, L = Low Gain. Use in conjunction with Reg 0x10 bit 7. * For hardware switching, Reg 0x10 bit 7 must be set to 1. * For soft switching, this pin must be High.
C2	OUTN	Analog Output	Negative swing analog output
A3	SEN	Digital Input	Serial interface enable
B3	VSS	Power	GND
C3	VDD	Power	+5.0V supply
	PD	Optical input	Photo Diode

Ordering Information

PART NUMBER (Notes 1, 2, 3, 4)	PART MARKING	PACKAGE Tape & Reel (Pb-free)	PKG. DWG. #
ISL58328CIZ-T7	123Z (Backside of Die)	9 Ball OCSP	S3x3.9
ISL58328CIZ-T7A	123Z (Backside of Die)	9 Ball OCSP	S3x3.9
ISL58328CIZ-EVAL	Evaluation Board		

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Please refer to TB478 for solder profile.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL58328. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

Supply Voltage (+5.0V to GND) 6.0V
Maximum CMOS Input/Output 3.6V
Maximum Output Voltage . . . . . V_{SS} - 0.3 to V_{DD} + 0.3
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 2kV
Machine Model (Per EIAJ ED-4701 Method C-111) 200V
Latch Up (Tested per JESD-78) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
9 Ld OCSP (Note 5)	125	NA

Storage Temperature Range . . . . . -25°C to +125°C
Pb-Free Reflow Profile . . . . . 250°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Electrical Specifications

V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{DD}	+5.0V Supply Voltage Range		4.5	5.0	5.5	V
I_{VDD1}	Supply Current	No incident light, in nomal mode		20	25	mA
I_{VDD2}	Supply Current	No incident light, in SLEEP mode			600	µA
V_{OFS}	Output P Offset Referenced to VREF	No incident light	-50	10	+50	mV
V_{REF_i}	Common Mode Output Voltage	Internal VREF generator	1.75	2.10	2.35	V
V_{IL}	CMOS Input LOW	SEN, SDATA, SCLK, and HL pins	0		0.8	V
VI_H	CMOS Input HIGH	SEN, SDATA, SCLK and HL pins	2.4		3.6	V
V_{OL}	CMOS Output LOW	SDATA; I_{LOAD} = 3mA			0.8	V
V_{OH}	CMOS Output HIGH	SDATA; I_{LOAD} = 3mA	2.5			V

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications

V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	Bandwidth OUTP, OUTN (not differential)	-3dB RBW = 30kHz		85		MHz
V_{OUTMAX}	Differential Mode Output Voltage (OUTP) – (OUTN)	Linear output		2.95		V_{P-P}

Sensitivity V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

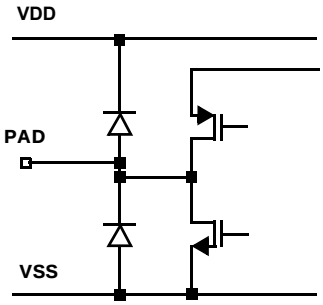
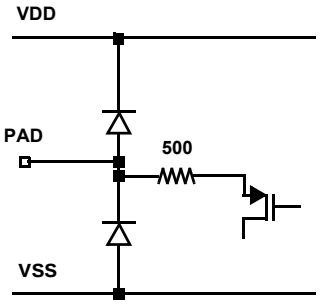
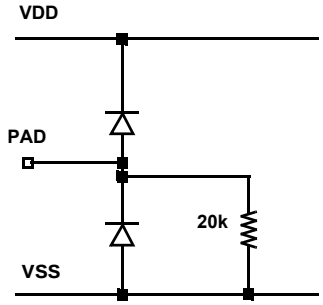
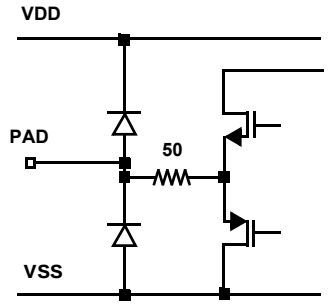
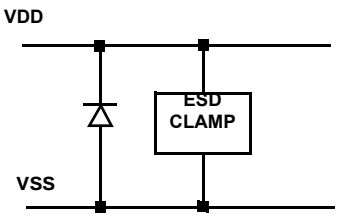
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$Gain_{00}$	TIA Lowest Gain	0dB fine gain adjustment, 7FFh Differential output	350	450	550	mV/µA
$Gain_{01}$	TIA 2nd Lowest Gain	0dB fine gain adjustment, 7FFh Differential output	700	890	1110	mV/µA
$Gain_{10}$	TIA 2nd Highest Gain	0dB fine gain adjustment, 7FFh Differential output	1400	1790	2170	mV/µA
$Gain_{11}$	TIA Highest Gain	0dB fine gain adjustment, 7FFh Differential output	3700	4850	6020	mV/µA
$Gain_{Fine\_MAX}$	Maximum Fine Gain	for both HIGH Gain and LOW Gain channels Compared to 0dB fine gain setting, 7FFh		19		dB
$Gain_{Fine\_MIN}$	Minimum Fine Gain	for both HIGH Gain and LOW Gain channels Compared to 0dB fine gain setting, 7FFh		-5.5		dB
Current to Optical conversion: Optical sensitivity is not tested in production. Gain parameters were obtained using input test currents. Following factors are used to convert current to optical power.						
$I2O_{450nm}$	Current to Optical conversion (450nm)	Bench data; measured on typical devices		0.27		µA/µW
$I2O_{530nm}$	Current to Optical conversion (530nm)	Bench data; measured on typical devices		0.26		µA/µW
$I2O_{640nm}$	Current to Optical conversion (640nm)	Bench data; measured on typical devices		0.38		µA/µW

Serial Interface AC Performance

V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
F_{SER1}	SCLK Operating Range	Deglitch disable(CONTROL[6]=0)			50	MHz
F_{SER2}	SCLK Operating Range	Deglitch enable(CONTROL[6]=1)		2		MHz
t_{EH}	SEN “H” Time		320			ns
t_{EL}	SEN “L” Time		40			ns
t_{ERSR}	SEN Rising Edge to the First SCLK Rising Edge		10			ns
t_{CDS}	SDIO Set Up Time			10		ns
t_{CDH}	SDIO Hold Time			10		ns
t_{SREF}	Last SCLK Rising Edge to SEN Falling Edge		10			ns
t_{CC}	SCLK Cycle Time		20			ns
Duty	SCLK “H” Duty Cycle			50		%
t_{CDD}	SDIO Output Delay			4		ns
t_{EDH}	SDIO Output Hold Time			2		ns
$INPUT_{LEAKAGE}$	Input Leakage for SCLK, SDATA, and SEN pin		-10		10	µA

I/O Pins Equivalent Circuits

PINS	TYPE	EQUIVALENT CIRCUIT
SDATA SCLK SEN	Digital I/O Digital Input Digital Input	
H/L	Digital Input	
VREF	Analog Input	
OUTP OUTN	Analog Output	
VDD	Power	

Application Information

Input Optical Power

The ISL58328 has a photo detector in an octagon shape (shown in PD pattern) with 700µm diameter. It is sensitive from 400nm to 1000nm for light monitoring application, which is a perfect choice for Light Automatic Power control. This wide range of sensitivity also allows the ISL58328 to be used for white balance control in LED systems such as LED based LCoS or DLP pico projectors.

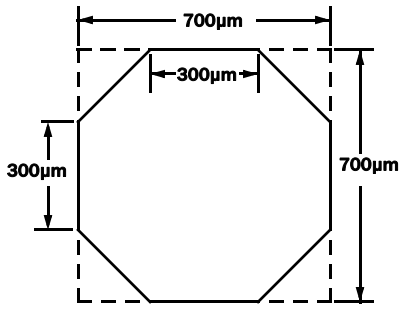
Current generated by the photo detector, is amplified by a trans-impedance amplifier (TIA). The TIA has four feedback resistors. Users can choose which feedback resistor is used for HIGH or LOW gain applications by setting the tia_gain register. Once a proper resistor is selected for the required TIA gain, optical signal is then amplified by the TIA that feeds into the fine gain stage. HIGH gain channel and LOW gain channel TIA gains can be individually set through the TIA register. The HIGH gain and LOW gain channels have the same gain adjustment range (25dB) and can be individually controlled.

In applications where laser power is modulated between 2 power levels, users can choose between HIGH gain channel for the low power level and LOW gain channel for the high power. It can provide the best resolution when power is low and not saturate the amplifier circuit when power is high. If users don't need to monitor two power levels, there is no need to switch between HIGH gain channel and LOW gain channel.The selection of HIGH gain or LOW gain signal path can be done with fast hardware switching or by setting register bit "h/l". When changing HIGH Gain or LOW Gain signal paths by hardware switching, "h/l" bit (Reg 0x10 bit [7]) needs to be "1". When changing it with register (soft switching), HL pin needs to be driven by digital HIGH because HL and "h/l" are AND for TIA gain control. Regardless of channel gain settings, the dynamic range of TIA is determined by the photo detector sensitivity with respect to wavelength. For example in 445nm application when TIA = 01b gain is selected, the maximum input optical power is limited to 2mW for blue light laser; but this limitation is reduced to 1.45mW with 638nm laser. This is because the photo detector has higher optical-to-electrical conversion efficiency to longer wavelength. Higher than the maximum input limitation, the TIA or whole device will still be working but it may yield distorted output and a long fall time, increasing the time that the circuit used to recover from saturation.

TABLE 1. MAXIMUM INPUT POWER vs TIA RESISTOR

TIA_Gain (tia_h/tia_l)	(445nm) mW	(638nm) mW	(532nm) mW
00b	5.0	3.65	5.30
01b	2.5	1.82	2.65
10b	1.25	0.91	1.33
11b	0.44	0.32	0.47

Detector Pattern



Gain Control

The ISL58328 channel gain is set through a 12-bit DAC, separated into 2 registers. Each wavelength has two 12-bit gain registers, one for HIGH gain application and the other for LOW gain application. The selection of HIGH gain or LOW Gain is done by fast hardware switching through HL pin or "h/l" register bit. All gain registers of HIGH Gain and LOW Gain channels are capable of update at anytime through the serial interface. The 12-bit gain registers provides total 25dB of adjustment range, +19dB to -5.5dB reference to fine gain setting 7FFh. All settings will be reset to default at power-on. Users need to load gain settings after ISL58328 is powered up. Overall differential output signal gain can be obtained by using Equations 1 through 3:

Blue Laser Diode(445nm)

$$\text{Gain}\ (\text{mV}/\mu\text{W}) = \frac{1.88 \times \text{TIA}}{256 + \text{Code}} \quad \text{(EQ. 1)}$$

Red Laser Diode (638nm)

$$\text{Gain}\ (\text{mV}/\mu\text{W}) = \frac{2.57 \times \text{TIA}}{256 + \text{Code}} \quad \text{(EQ. 2)}$$

Green Laser Diode(530nm)

$$\text{Gain}\ (\text{mV}/\mu\text{W}) = \frac{1.76 \times \text{TIA}}{256 + \text{Code}} \quad \text{(EQ. 3)}$$

Where: Code is 12 bits gain code in decimal (0 ~ 4095)

TABLE 2.

tia_h, tia_l SETTINGS	TIA FACTOR IN EQUATION
00b	500
01b	1000
10b	2000
11b	5400

Output Configuration

The ISL58328 has two differential outputs: OUTP is a positive and OUTN is a negative swing output. OUTP and OUTN outputs are referenced to VREF. VREF can be externally supplied or internally generated 2.1V. With respect to the input optical signal, OUTP swings up from reference voltage and OUTN swings down from reference voltage. Both OUTP and OUTN have the same linear output dynamic range up to 1.4V swing from reference voltage. When using external reference voltage, users need to adjust gain registers to set proper channel gain to prevent output saturation. To use ISL58328 as a single-ended output, users can take either OUTP or OUTN signal and load another output with equivalent resistor and capacitor load to keep both outputs with the same load condition. However, it won't be an issue to leave another output floating. When using ISL58328 as a single-ended output device, external reference voltage is necessary because the VREF pin doesn't have strong driving capability. It is not recommended to use VREF as a reference source to drive other devices. To obtain the best signal quality at the input of the AFE or video processor, it is recommended to keep OUTP and OUTN traces in parallel and to keep them with same length, same width, and route. If output signals from ISL58328 need to travel through a flex cable to AFE or video processor, to match with the impedance of flex cable, a 50Ω serial termination resistor close to OUTP and OUTN output pins may be necessary; thus the best value should be determined according to the actual application.

Slow Tail Compensation

Photons at longer wavelength will penetrate deeper into the photo detector structure than shorter wavelengths. It takes longer for electron-hole pairs to become photo current and results in a longer tail for the pulse output, called slow tail. Longer wavelength light such as 638nm or IR has more visible slow tail effect than blue laser. To minimize the slow tail effect, ISL58328 has incorporated Intersil's proprietary slow tail compensation technology. There are three registers for slow tail compensation adjustment for each wavelength (such as 638nm, 532nm, and 445nm). The slow tail compensation function is not limited to the specific wavelength listed previously; it is used in conjunction with the selected fine gain registers. Users can disable slow tail compensation by setting Bit 7 (MSB) of the register to "0". This function can also be used to improve the quality of pulse output waveforms due to impedance mismatch from OEIC outputs to the flex connector. One example is to improve Tr/Tf or to minimize overshoot.

Layout Consideration

When using differential output, layout OUTP and OUTN traces next to each other and ground traces should be placed to other side of OUTP and OUTN traces. When using single-ended, layout reference trace needs to be next to output signal trace and layout a ground trace at the other side ofthe output. For best result, dual layer flex with signal on one side and ground plane on other side is a must.

Reference Voltage

The ISL58328 has a reference voltage generator intended to generate 2.1V reference voltage for all circuit blocks. Output is biased at internal reference voltage automatically when VREF pin is left floating. When a DC voltage is applied to VREF pin, OUTP and OUTN will be biased at external reference automatically. External reference is limited to a range from 1.5V to 2.5V. Using voltage outside of this range will yield distorted outputs. When using external reference voltage, good decoupling is very important to prevent noise coupling into VREF. A 0.1µF ceramic capacitor placed as close to VREF pin as possible is recommended to decouple VREF to ground.

Power Supply Decoupling

Due to the current being switched rapidly at OUTP and OUTN, it is important to ensure that the power supply is well decoupled to ground. During output switching, the V_{DD} undergoes severe current transients, thus every effort should be made to decouple the V_{DD} as close to the package as possible.

Without proper power supply decoupling there could make poor rise/fall times, overshoot, and poor settling response.

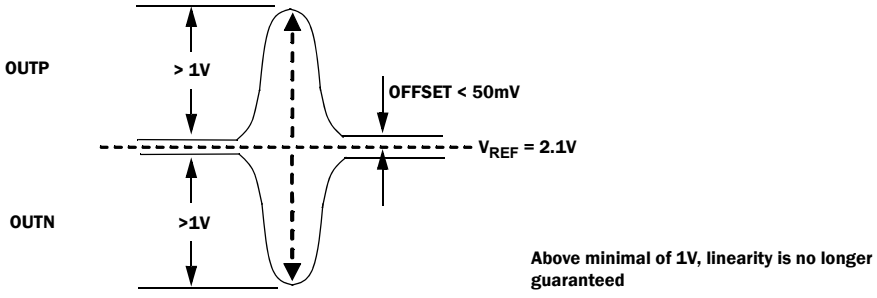


FIGURE 2. OUTP/OUTN

Sensitivity Curves

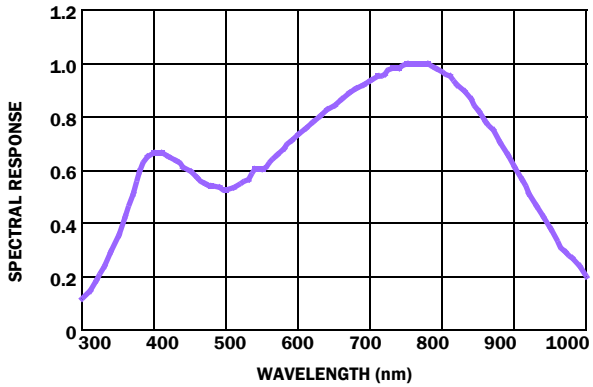


FIGURE 3. NORMALIZED SPECTRAL RESPONSE vs WAVELENGTH

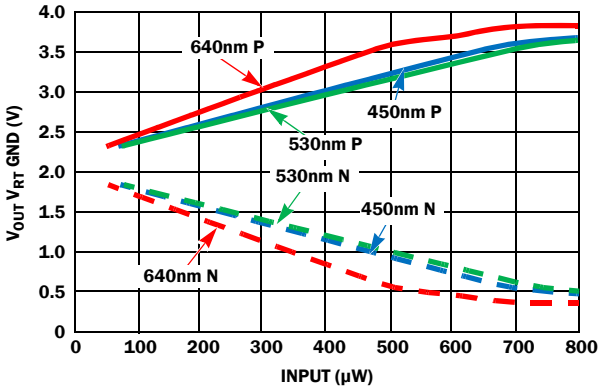


FIGURE 4. OPTICAL POWER INPUT vs OUTPUT (RED LED 620nm; GREEN LED 532nm; BLUE LED 460nm)

Register Map

ADDR	NAME	b7	b6	b5	b4	b3	b2	b1	b0	DEFAULT	ACCESS
00h	ID0	DEVICE ID								28h	R
01h	ID1	DEVICE OPTION				DEVICE VERSION				E0h	R
02h	ID2	reserved								00h	R
03h	DSR	DEVICE SELECT REGISTER (DSR)								43h	RW
04h		reserved for multi-chip protocol									
05h		reserved for multi-chip protocol									
06h		reserved for multi-chip protocol									
07h		reserved for multi-chip protocol									
08h		reserved for multi-chip protocol									
09h		reserved for multi-chip protocol									
0Ah		reserved for multi-chip protocol									
0Bh		reserved for multi-chip protocol									
0Ch		reserved for multi-chip protocol									
0Dh		reserved for multi-chip protocol									
0Eh		reserved for multi-chip protocol									
0Fh		reserved for multi-chip protocol									
10h	CONTROL	h/l	deglitch	blue	red/green	test_en	x	x	chip_en	46h	RW
11h	B _GAIN0	blue_h[3: 0]				blue_l[3:0]				FFh	RW
12h	B_H_GAIN	blue_h[11:4]								7Fh	RW
13h	B_L_GAIN	blue_l[11:4]								7Fh	RW
14h	R_GAIN0	red_h[3:0]				red_l[3:0]				FFh	RW
15h	R_H_GAIN	red_h[11:4]								7Fh	RW
16h	R_L_GAIN	red_l[11:4]								7Fh	RW
17h	GREEN_GAIN0	green_h[3:0]				green_l[3:0]				FFh	RW
18h	GREEN_H_GAIN	green_h[11:4]								7Fh	RW
19h	GREEN_L_GAIN	green_l[11:4]								7Fh	RW

Register Map (Continued)

ADDR	NAME	b7	b6	b5	b4	b3	b2	b1	b0	DEFAULT	ACCESS
1Ah	ST_RED	st_en_red	st_time_red[2:0]			x	st_mag_red[2:0]			00h	RW
1Bh	ST_GREEN	st_en_green	st_time_green[2:0]			x	st_mag_green[2:0]			00h	RW
1Ch	TIA_GAIN	x	x	x	x	tia_h[1:0]			tia_l[1:0]	00h	RW
1Dh		reserved									
1Eh	ST_BLUE	st_en_blue	st_time_blue[2:0]			x	st_mag_blue[2:0]			00h	RW

Note: All gain registers in this table can be used for any wavelength in spectral range from 390nm to 1000nm, not limited to wavelengths specified.

Register Description

TABLE 3. ID0 (addr = 00h)

REGISTER	DESCRIPTION
ID0	Device ID, read only, code = 28h

TABLE 4. ID1 (addr = 01h)

REGISTER	DESCRIPTION
DEVICE OPTION	Device option code, read only, code = E0h
DEVICE VERSION	Device version code, read only, code = 0h

TABLE 5. DSR (addr = 03h)

REGISTER	DESCRIPTION
DSR (Note 7)	Device selection code, used for Intersil universal Serial Interface protocol, code = 43h

NOTE:

7. DSR register is to allow multiple devices to share same the SPI interface. Each device on the SPI interface bus has its own DSR value, like a device address in I^2C protocol. Master sends DSR to the SPI bus, only one device with a matched DSR will response to the following commands and data, remaining devices on the bus will ignore commands and data; pull the interface to Hi-Z. For more information please contact Intersil for Universal Serial Interface Specification document.

TABLE 6. CONTROL (addr = 10h)

REGISTER	DESCRIPTION
h/l Bit [7]	HIGH gain or LOW Gain channels selection. Used in conjunction with HL pin. 1b: HIGH Gain channel 0b: LOW Gain channel Default: 0b
deglitch Bit [6]	1b: Enable serial interface deglitch function 0b: Disable serial interface deglitch function Default: 0b
blue Bit [5]	1b: Device works in blue mode (regardless of red/green bit setting) 0b: Device works in either RED or GREEN mode, depends on red/green register bit setting Default: 0b
red/green Bit [4]	0b: GREEN 1b: RED Default: 0b (GREEN mode)
test_en Bit [3]	To enable a chip test function (for Intersil internal use only) 1b: Enable test function 0b: Disable test function Default: 0b
chip_en Bit [0]	To enable or disable ISL58328. When disabled all outputs are in Hi-Z 1b: enable 0b: disable (SLEEP mode)

TABLE 7. B_GAIN0 (addr = 11h)

REGISTER	DESCRIPTION
blue_h[3: 0] Bits [7:4]	Lower 4 bits of blue light HIGH Gain channel fine gain control
blue_l[3: 0] Bits [3:0]	Lower 4 bits of blue light LOW Gain channel fine gain control

TABLE 8. B_H_GAIN (addr = 12h)

REGISTER	DESCRIPTION
blue_h[11:4] Bits [7:0]	High 8 bits of blue light HIGH Gain channel fine gain control

TABLE 9. B_L_GAIN (addr = 13h)

REGISTER	DESCRIPTION
blue_l[11:4] Bits [7:0]	High 8 bits of blue light LOW Gain channel fine gain control

TABLE 10. RED_GAIN0 (addr = 14h)

REGISTER	DESCRIPTION
red_h[3: 0] Bits [7:4]	Lower 4 bits of red light HIGH Gain channel fine gain control
red_l[3: 0] Bits [3:0]	Lower 4 bits of red light LOW Gain channel fine gain control

TABLE 11. RED_H_GAIN (addr = 15h)

REGISTER	DESCRIPTION
red_h[11:4] Bits [7:0]	High 8 bits of red light HIGH Gain channel fine gain control

TABLE 12. RED_L_GAIN (addr = 16h)

REGISTER	DESCRIPTION
red_l[11:4] Bits [7:0]	High 8 bits of red light LOW Gain channel fine gain control

TABLE 13. GREEN_GAIN0 (addr = 17h)

REGISTER	DESCRIPTION
green_h[3:0] Bits [7:4]	Lower 4 bits of green light HIGH Gain channel fine gain control
green_l[3:0] Bits [3:0]	Lower 4 bits of green light LOW Gain channel fine gain control

TABLE 14. GREEN_H_GAIN (addr = 18h)

REGISTER	DESCRIPTION
green_h[11:4] Bits [7:0]	High 8 bits of green light HIGH Gain channel fine gain control

TABLE 15. GREEN_L_GAIN (addr = 19h)

REGISTER	DESCRIPTION
green_l[11:4] Bits [7:0]	High 8 bits of green light LOW Gain channel fine gain control

TABLE 16. ST_RED (addr = 1Ah)

REGISTER	DESCRIPTION
st_en_red Bit [7]	Red light slow tail compensation control 1b: enable 0b: disable (when disable, st_time_red and st_mag_red are reset to 000b)
st_time_red Bits [6:4]	Red light slow tail compensation time constant control
st_mag_red Bits [2:0]	Red light slow tail compensation magnitude control

TABLE 17. ST_GREEN (addr = 1Bh)

REGISTER	DESCRIPTION
st_en_green Bit [7]	Green light slow tail compensation control 1b: enable 0b: disable (when disabled, st_time_green and st_mag_green are reset to 000b)
st_time_green Bits [6:4]	Green light slow tail compensation time constant control
st_mag_green Bits [2:0]	Green light slow tail compensation magnitude control

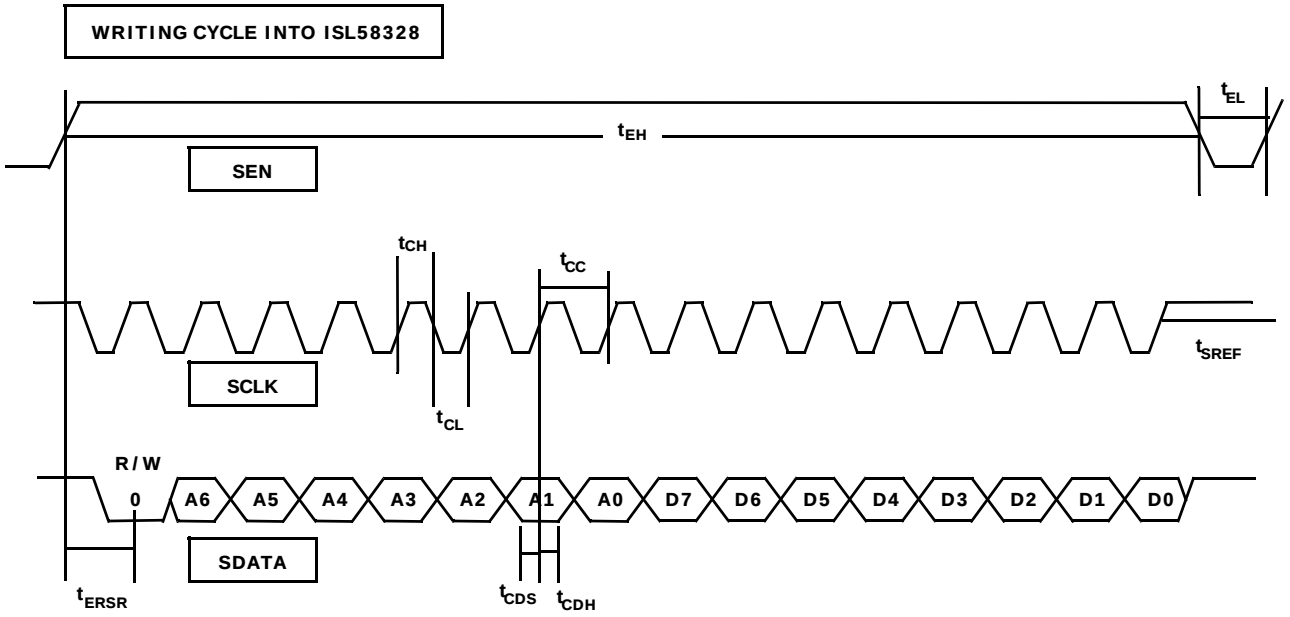
TABLE 18. TIA_GAIN (addr = 1Ch)

REGISTER	DESCRIPTION
tia_l[1:0] Bits [3:2]	TIA gain selection in HIGH Gain channel application 00b: Lowest gain 01b: 2nd lowest gain 10b: 2nd highest gain 11b: Highest gain
tia_h[1:0] Bits [1:0]	TIA gain selection in LOW Gain channel application 00b: Lowest gain 01b: 2nd lowest gain 10b: 2nd highest gain 11b: Highest gain

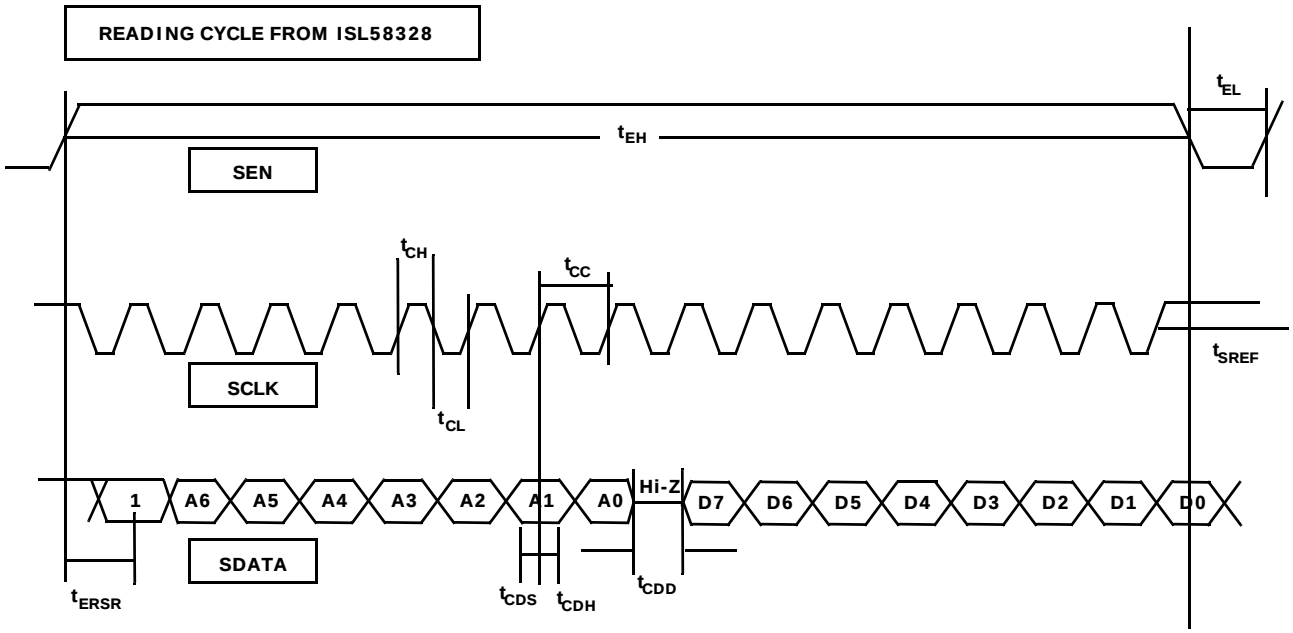
TABLE 19. ST_BLUE (addr = 1Eh)

REGISTER	DESCRIPTION
st_en_blue Bit [7]	Blue light slow tail compensation control 1b: enable 0b: disable (when disable, st_time_blue and st_mag_blue are reset to 000b)
st_time_blue Bits [6:4]	Blue light slow tail compensation time constant control
st_mag_blue Bits [2:0]	Blue light slow tail compensation magnitude control

Serial Interface Protocol



R/W BIT, ADDRESS BITS, AND DATA BITS ARE CLOCKED INTO ISL58328 AT RISING EDGE OF SCLK.



R/W BIT AND ADDRESS BITS ARE CLOCKED INTO ISL58328 AT RISING EDGE OF SCLK.
DATA BITS ARE CLOCKED OUT FROM ISL58328 AT FALLING EDGE OF SCLK.
THE LAST BIT (D0) OF DATA IS CLOCKED BY THE FALLING EDGE OF SEN.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 29, 2013	FN6329.2	Change Products information verbiage to About Intersil.
February 21, 2012	FN6329.1	Added ISL58328CIZ-T7A to “Ordering Information” on page 3.
December 8, 2010	FN6329.0	Initial Release

About Intersil

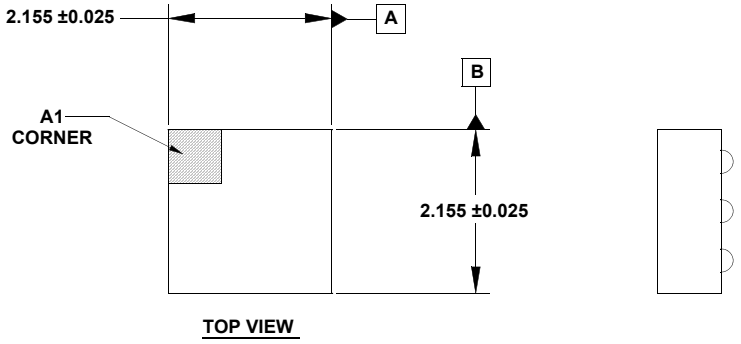
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

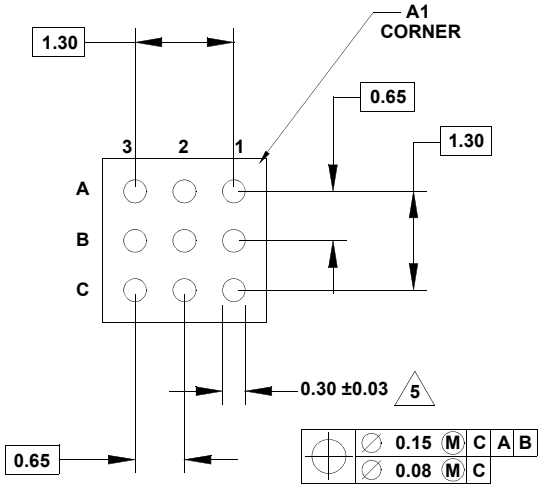
Package Outline Drawing

S3x3.9

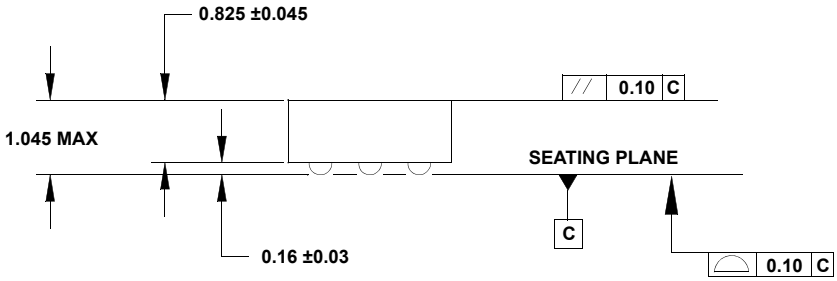
3X3 ARRAY 9 BUMP OPTICAL CHIP SCALE PACKAGE (OCSP)
Rev 7, 10/10



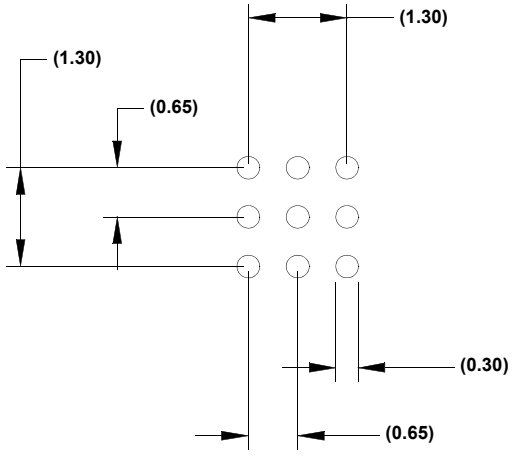
TOP VIEW



BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference only.
2. Dimensioning and tolerancing conform to ASME Y 14.5M-1994
3. Primary datum C and seating plane are defined by the spherical crowns of the contact balls.
4. Pin "A1" is marked on the top and bottom side adjacent to the A1 ball.

5. Dimension is measured at the maximum ball diameter.