MICROCHIP

AT24C08D

I²C-Compatible (2-Wire) Serial EEPROM 8-Kbit (1,024 x 8)

Features

- Low-Voltage Operation:
  - Vcc = 1.7V to 3.6V
- Internally Organized as 1,024 x 8 (8K)
- Industrial Temperature Range -40°C to +85°C
- I^2C-Compatible (2-Wire) Serial Interface:
  - 100 kHz Standard mode, 1.7V to 3.6V
  - 400 kHz Fast mode, 1.7V to 3.6V
  - 1 MHz Fast Mode Plus (FM+), 2.5V to 3.6V
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Write-Protect Pin for Full Array Hardware Data Protection (except WLCSP)
- Ultra Low Active Current (1 mA maximum) and Standby Current (0.8 μA maximum)
- 16-Byte Page Write Mode:
  - Partial page writes allowed
- Random and Sequential Read Modes
- Self-Timed Write Cycle within 5 ms Maximum
- ESD Protection > 4,000V
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green Package Options (Lead-free/Halide-free/RoHS compliant)
- Die Sale Options: Wafer Form and Bumped Wafers

Packages

- 8-Lead PDIP[(1)], 8-Lead SOIC, 5-Lead SOT23, 8-Lead TSSOP, 8-Pad UDFN, 8-Ball VFBGA and 4-Ball WLCSP

Note:

1. Contact Microchip Sales for the availability of this package.

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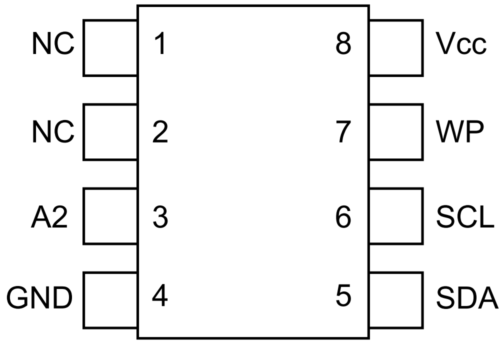
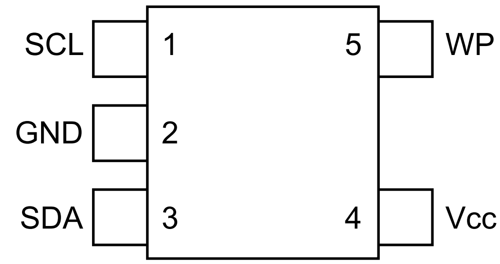
1. Package Types (not to scale)

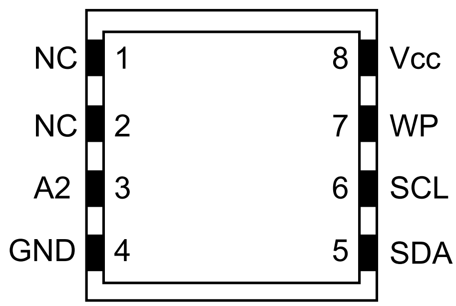
8-lead PDIP/SOIC/TSSOP
(Top View)



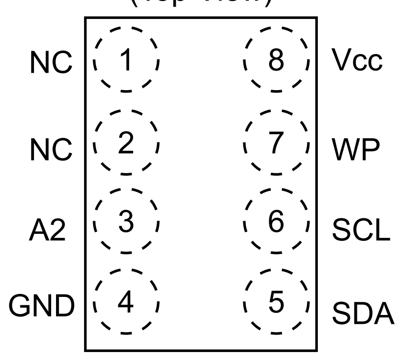
5-lead SOT23[(2)]
(Top View)



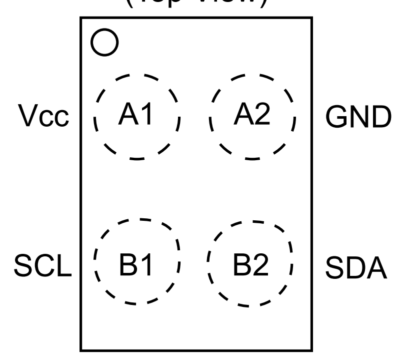
8-pad UDFN
(Top View)



8-ball VFBGA
(Top View)



4-ball WLCSP[(1)]
(Top View)



Note:

1. Since the WLCSP has no WP pin, the write protection feature is not offered on the WLCSP. Refer to 6.1 Device Addressing for details about addressing the WLCSP version of the device.
2. Refer to 6.1 Device Addressing for details about addressing the SOT23 version of the device.

2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead PDIP	8-Lead SOIC	8-Lead TSSOP	5-Lead SOT23	8-Pad UDFN(1)	8Ball VFBGA	4-Ball WLCSP	Function
NC	1	1	1	—	1	1	—	No Connect
NC	2	2	2	—	2	2	—	No Connect
A2(2)	3	3	3	—	3	3	—	Device Address Input
GND	4	4	4	2	4	4	A2	Ground
SDA	5	5	5	3	5	5	B2	Serial Data
SCL	6	6	6	1	6	6	B1	Serial Clock
WP(2)	7	7	7	5	7	7	—	Write-Protect
V_{CC}	8	8	8	4	8	8	A1	Device Power Supply

Note:
1. The exposed pad on the this package can be connected to GND or left floating.
2. If the A2 or WP pins are not driven, they are internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Microchip recommends connecting these pins to a known state whenever possible.

2.1 Device Address Input (A2)

The A2 pin is a device address input that is hard-wired (directly to GND or to V_{CC}) for compatibility with other AT24C devices. When the pin is hard-wired, as many as two devices may be addressed on a single bus system. A device is selected when a corresponding hardware and software match is true. If the pin is left floating, the A2 pin will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the address pin to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

2.2 Ground

The ground reference for the power supply. GND should be connected to the system ground.

2.3 Serial Data (SDA)

The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 10 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

2.4 Serial Clock (SCL)

The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled high using an external pull-up resistor.

2.5 Write-Protect (WP)

The write-protect input, when connected to GND, allows normal write operations. When the WP pin is connected directly to V_{CC}, all write operations to the protected memory are inhibited.

If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the WP pin to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

Table 2-2. Write-Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full Array
At GND	Normal Write Operations

2.6 Device Power Supply

The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

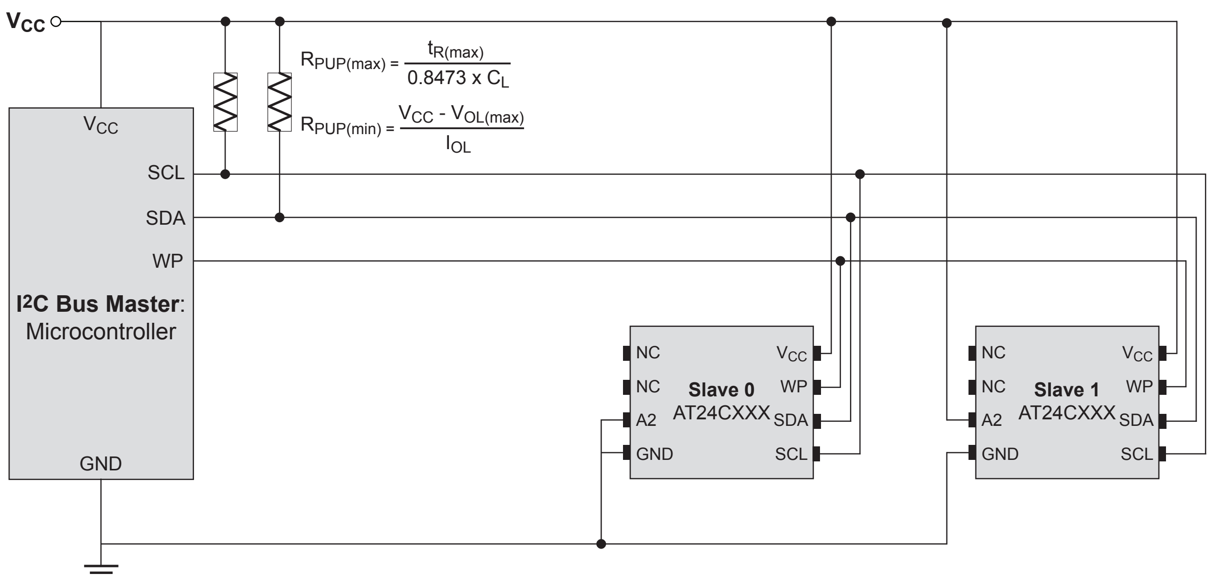
3. Description

The AT24C08D provides 8,192 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 1,024 words of 8 bits each. This device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The device is available in space-saving 8-lead SOIC, 8-lead TSSOP, 8-pad UDFN, 8-lead PDIP[1], 5-lead SOT23, 8-ball VFBGA and 4-ball WLCSP packages. All packages operate from 1.7V to 3.6V.

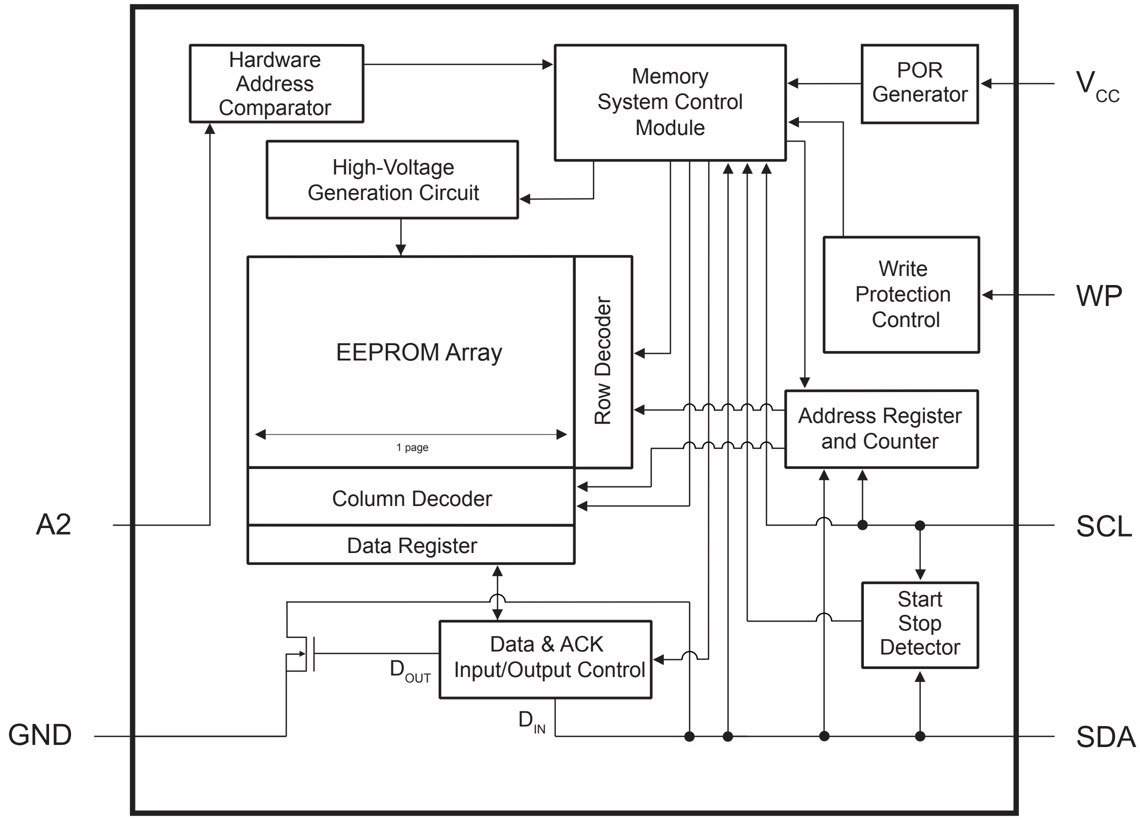
Note:

1. Contact Microchip Sales for the availability of this package.

3.1 System Configuration Using 2-Wire Serial EEPROMs



3.2 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
V_{CC}	4.1V
Voltage on any pin with respect to ground	-0.6V to +4.1V
DC output current	5.0 mA
ESD protection	>4 kV

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT24C08D		
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low Voltage Grade	1.7V to 3.6V

4.3 DC Characteristics

Table 4-2. DC Characteristics

Parameter	Symbol	Minimum	Typical[(1)]	Maximum	Units	Test Conditions
Supply Voltage	V_{CC}	1.7	—	3.6	V	
Supply Current	I_{CC1}	—	0.08	0.3	mA	V_{CC} = 1.8V[(2)], Read at 400 kHz
		—	0.15	0.5	mA	V_{CC} = 3.6V, Read at 1 MHz
Supply Current	I_{CC2}	—	0.20	1.0	mA	V_{CC} = 3.6V, Write at 1 MHz
Standby Current	I_{SB}	—	0.08	0.4	µA	V_{CC} = 1.8V[(2)], V_{IN} = V_{CC} or GND
		—	0.10	0.8	µA	V_{CC} = 3.6V, V_{IN} = V_{CC} or GND

Parameter	Symbol	Minimum	Typical(1)	Maximum	Units	Test Conditions
Input Leakage Current	I_{LI}	—	0.10	3.0	µA	$V_{IN} = V_{CC}$ or GND
Output Leakage Current	I_{LO}	—	0.05	3.0	µA	$V_{OUT} = V_{CC}$ or GND
Input Low Level	V_{IL}	-0.6	—	V_{CC} x 0.3	V	Note 2
Input High Level	V_{IH}	V_{CC} x 0.7	—	V_{CC} + 0.5	V	Note 2
Output Low Level	V_{OL1}	—	—	0.2	V	V_{CC} = 1.8V, I_{OL} = 0.15 mA
Output Low Level	V_{OL2}	—	—	0.4	V	V_{CC} = 3.0V, I_{OL} = 2.1 mA

Note:

1. Typical values characterized at T_A = +25°C unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.

4.4 AC Characteristics

Table 4-3. AC Characteristics(1)

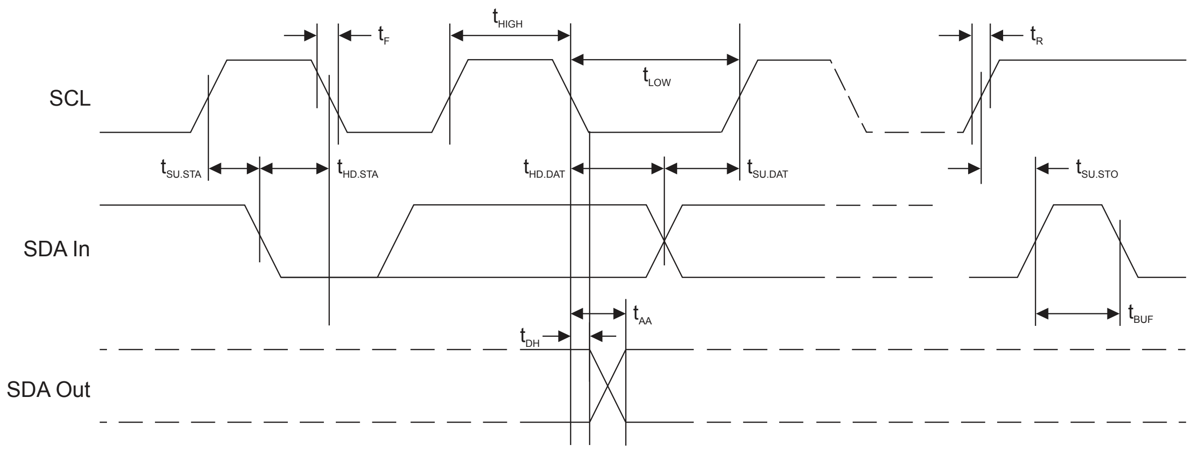
Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Units
		V_{CC} = 1.7V to 3.6V		V_{CC} = 1.7V to 3.6V		V_{CC} = 2.5V to 3.6V		
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency, SCL	f_{SCL}	—	100	—	400	—	1000	kHz
Clock Pulse Width Low	t_{LOW}	4,700	—	1,300	—	500	—	ns
Clock Pulse Width High	t_{HIGH}	4,000	—	600	—	400	—	ns
Input Filter Spike Suppression (SCL,SDA)(2)	t_I	—	100	—	100	—	100	ns
Clock Low to Data Out Valid	t_{AA}	—	4,500	—	900	—	450	ns
Bus Free Time between Stop and Start(2)	t_{BUF}	4,700	—	1,300	—	500	—	ns

Parameter	Symbol	Standard Mode V_{CC} = 1.7V to 3.6V		Fast Mode V_{CC} = 1.7V to 3.6V		Fast Mode Plus V_{CC} = 2.5V to 3.6V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Start Hold Time	$t_{HD.STA}$	4,000	—	600	—	250	—	ns
Start Set-up Time	$t_{SU.STA}$	4,700	—	600	—	250	—	ns
Data In Hold Time	$t_{HD.DAT}$	0	—	0	—	0	—	ns
Data In Set-up Time	$t_{SU.DAT}$	200	—	100	—	100	—	ns
Inputs Rise Time(2)	t_R	—	1,000	—	300	—	100	ns
Inputs Fall Time(2)	t_F	—	300	—	300	—	100	ns
Stop Set-up Time	$t_{SU.STO}$	4,700	—	600	—	250	—	ns
Write-Protect Setup Time	$t_{SU.WP}$	4,000	—	600	—	100	—	ns
Write-Protect Hold Time	$t_{HD.WP}$	4,000	—	600	—	400	—	ns
Data Out Hold Time	t_{DH}	100	—	50	—	50	—	ns
Write Cycle Time	t_{WR}	—	5	—	5	—	5	ms

Note:

1. AC measurement conditions:
   - C_L: 100 pF
   - R_{PUP} (SDA bus line pull-up resistor to V_{CC}): 1.3 kΩ (1000 kHz), 4 kΩ (400 kHz), 10 kΩ (100 kHz)
   - Input pulse voltages: 0.3 x V_{CC} to 0.7 x V_{CC}
   - Input rise and fall times: ≤50 ns
   - Input and output timing reference voltages: 0.5 x V_{CC}
2. These parameters are determined through product characterization and are not 100% tested in production.

Figure 4-1. Bus Timing



4.5 Electrical Specifications

4.5.1 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT24C08D should monotonically rise from GND to the minimum V_{CC} level, as specified in Table 4-1, with a slew rate no faster than 0.1 V/µs.

4.5.1.1 Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT24C08D includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus master must wait at least t_{PUP} before sending the first command to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-up Conditions[1]

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands.	100	—	µs
V_{POR}	Power-on Reset Threshold Voltage.	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles.	1	—	ms

Note:

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT24C08D drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

4.5.2 Pin Capacitance

Table 4-5. Pin Capacitance[(1)]

Symbol	Test Condition	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A2, SCL)	6	pF	V_{IN} = 0V

Note:

1. This parameter is characterized but is not 100% tested in production.

4.5.3 EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance[(1)]	T_A = 25°C, V_{CC} (min.) < V_{CC} < V_{CC} (max.) Byte or Page Write mode	1,000,000	—	Write Cycles
Data Retention[(1)]	T_A = 55°C	100	—	Years

Note:

1. Performance is determined through characterization and the qualification process.

5. Device Operation and Communication

The AT24C08D operates as a slave device and utilizes a simple I^2C-compatible 2-wire digital serial interface to communicate with a host controller, commonly referred to as the bus master. The master initiates and controls all read and write operations to the slave devices on the serial bus, and both the master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the master, while the bidirectional SDA pin is used to receive command and data information from the master as well as to send data back to the master. Data is always latched into the AT24C08D on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant bit (MSb) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the master. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic-high state at the same time.

5.1 Clock and Data Transition Requirements

The SDA pin is an open-drain terminal and therefore must be pulled high with an external pull-up resistor. SCL is an input pin which can either be driven high or pulled high using an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below. The relationship of the AC timing parameters with respect to SCL and SDA for the AT24C08D are shown in the timing waveform in Figure 4-1. The AC timing characteristics and specifications are outlined in 4.4 AC Characteristics.

5.2 Start and Stop Conditions

5.2.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable logic '1' state and will bring the device out of Standby mode. The master uses a Start condition to initiate any data transfer sequence; therefore, every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Refer to Figure 5-1 for more details.

5.2.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic '1' state.

The master can use the Stop condition to end a data transfer sequence with the AT24C08D which will subsequently return to Standby mode. The master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the master will perform another operation. Refer to Figure 5-1 for more details.

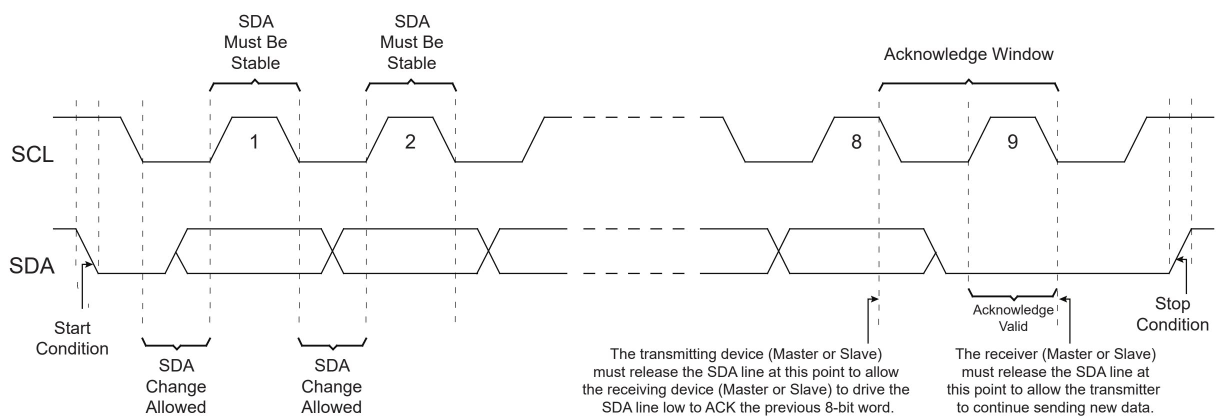
5.3 Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the transmitting device that it has successfully received the data byte by responding with what is known as an Acknowledge (ACK). An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a logic '0' during the entire high period of the ninth clock cycle.

When the AT24C08D is transmitting data to the master, the master can indicate that it is done receiving data and wants to end the operation by sending a logic '1' response to the AT24C08D instead of an ACK response during the ninth clock cycle. This is known as a No-Acknowledge (NACK) and is accomplished by the master sending a logic '1' during the ninth clock cycle, at which point the AT24C08D will release the SDA line so the master can then generate a Stop condition.

The transmitting device, which can be the bus master or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a logic '0' to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram has been provided in Figure 5-1 to better illustrate these requirements.

Figure 5-1. Start Condition, Data Transitions, Stop Condition and Acknowledge



5.4 Standby Mode

The AT24C08D features a low-power Standby mode which is enabled when any one of the following occurs:

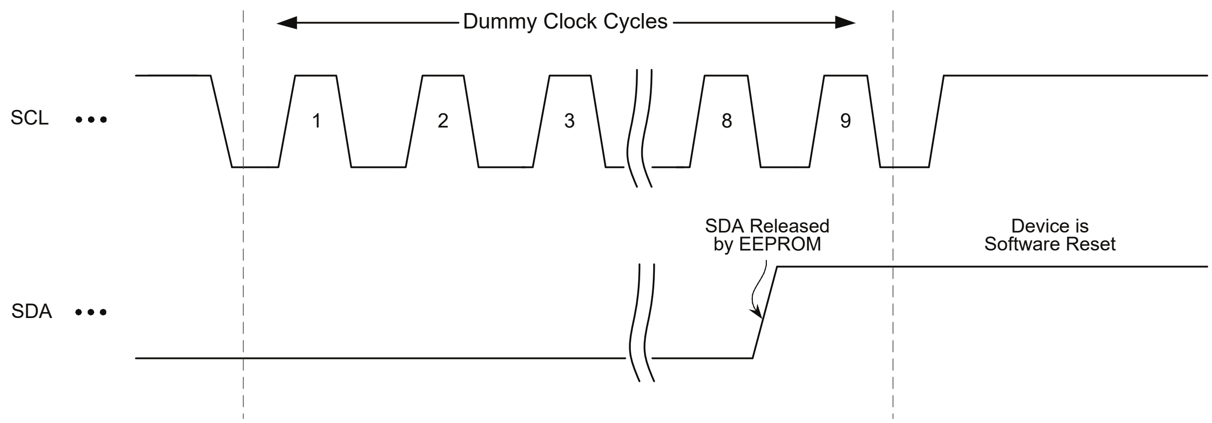
- A valid power-up sequence is performed (see 4.5.1 Power-Up Requirements and Reset Behavior).
- A Stop condition is received by the device unless it initiates an internal write cycle (see 7. Write Operations).
- At the completion of an internal write cycle (see 7. Write Operations).
- An unsuccessful match of the device type identifier or hardware address in the device address byte occurs (see 6.1 Device Addressing).

- The bus master does not ACK the receipt of data read out from the device; instead it sends a NACK response (see Section 8. Read Operations).

5.5 Software Reset

After an interruption in protocol, power loss or system Reset, any 2-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The software Reset sequence should not take more than nine dummy clock cycles. Once the software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition followed by the protocol. Refer to Figure 5-2 for an illustration.

Figure 5-2. Software Reset



In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see 4.5.1 Power-Up Requirements and Reset Behavior).

6. Memory Organization

The AT24C08D is internally organized as 64 pages of 16 bytes each.

6.1 Device Addressing

Accessing the device requires an 8-bit device address byte following a Start condition to enable the device for a read or write operation. Since multiple slave devices can reside on the serial bus, each slave device must have its own unique address so the master can access each device independently.

The Most Significant four bits of the device address byte is referred to as the device type identifier. The device type identifier '1010' (Ah) is required in bits 7 through 4 of the device address byte (see Table 6-1).

Following the 4-bit device type identifier is the hardware slave address bit, A2. This bit can be used to expand the address space by allowing up to two Serial EEPROM devices on the same bus. The A2 value must correlate with the voltage level on the corresponding hardwired device address input pin A2. The A2 pin uses an internal proprietary circuit that automatically biases it to a logic '0' state if the pin is allowed to float. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once the pin is biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Microchip recommends connecting the A2 pin to a known state whenever possible.

When using the SOT23 and WLCSP packages, the A2 pin is not accessible and is left floating. The previously mentioned automatic pull-down circuit will set this pin to a logic '0' state. As a result, to properly communicate with the device in the SOT23 and WLCSP packages, the A2 software bit must always be set to logic '0' for any operation.

Following the A2 hardware slave address bit are bits A9 and A8 (bit 2 and bit 1 of the device address byte), which are the two Most Significant bits of the memory array word address. Refer to Table 6-1 to review these bit positions.

The eighth bit (bit 0) of the device address byte is the Read/Write Select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon the successful comparison of the device address byte, the AT24C08D will return an ACK. If a valid comparison is not made, the device will NACK.

Table 6-1. Device Address Byte

Package	Device Type Identifier				Hardware Slave Address Bit	Most Significant Bits of the Word Address		R/$\overline{W}$ Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOIC, TSSOP, UDFN, PDIP, VFBGA	1	0	1	0	A2	A9	A8	R/$\overline{W}$
SOT23, WLCSP	1	0	1	0	0	A9	A8	R/$\overline{W}$

For all operations except the current address read, a word address byte must be transmitted to the device immediately following the device address byte. The word address byte consists of the remaining eight bits of the 10-bit memory array word address, and is used to specify which byte location in the EEPROM to start reading or writing. Refer to Table 6-2 to review these bit positions.

Table 6-2. Word Address Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A7	A6	A5	A4	A3	A2	A1	A0

7. Write Operations

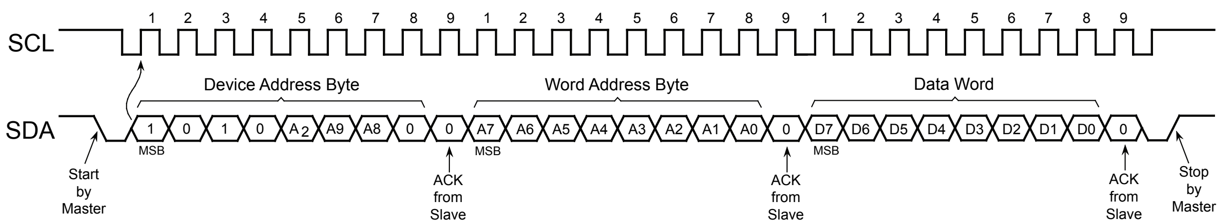
All write operations for the AT24C08D begin with the master sending a Start condition, followed by a device address byte with the R/$\overline{W}$ bit set to logic '0', and then by the word address byte. The data value(s) to be written to the device immediately follow the word address byte.

7.1 Byte Write

The AT24C08D supports the writing of a single 8-bit byte. Selecting a data word in the AT24C08D requires a 10-bit word address.

Upon receipt of the proper device address and the word address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an ACK. The addressing device, such as a bus master, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within t_{WR}, while the data word is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete.

Figure 7-1. Byte Write



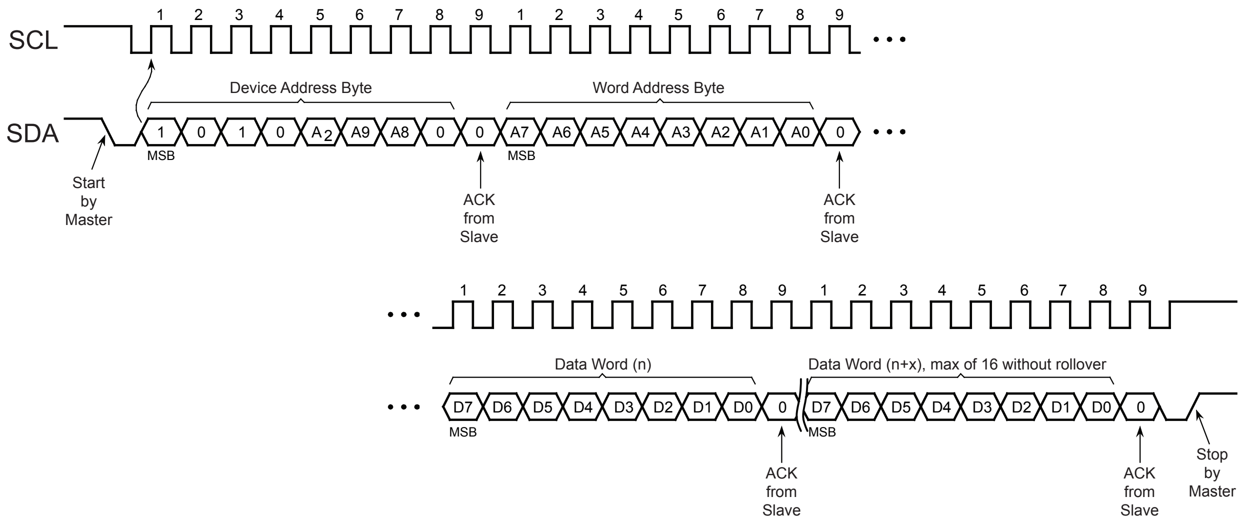
7.2 Page Write

A page write operation allows up to 16 bytes to be written in the same write cycle, provided all bytes are in the same row of the memory array (where address bits A9 through A4 are the same). Partial page writes of less than 16 bytes are also allowed.

A page write is initiated the same way as a byte write, but the bus master does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus master can transmit up to fifteen additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written has been sent to the device, the bus master must issue a Stop condition (see Figure 7-2) at which time the internally self-timed write cycle will begin.

The lower four bits of the word address are internally incremented following the receipt of each data word. The higher order address bits are not incremented and retain the memory page row location. Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will roll-over to the beginning of the same page. Nevertheless, creating a roll-over event should be avoided as previously loaded data in the page could become unintentionally altered.

Figure 7-2. Page Write

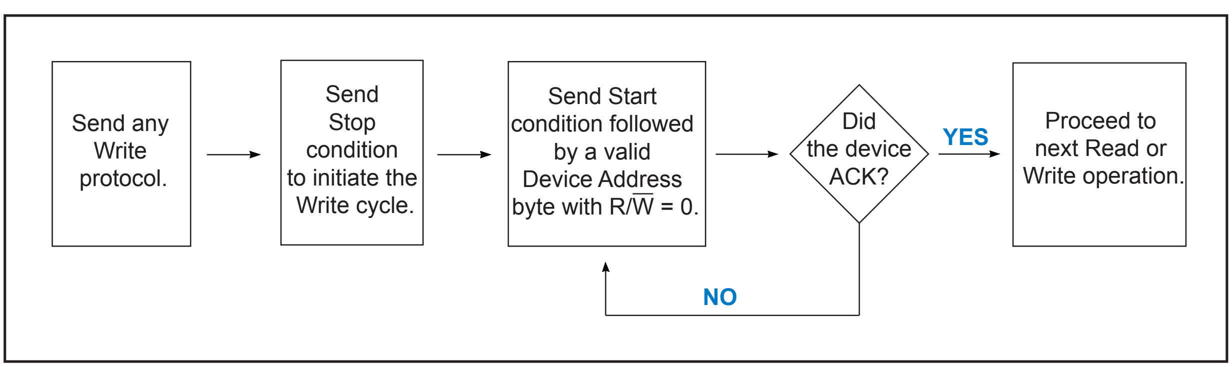


7.3 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time-sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}). This method allows the application to know immediately when the Serial EEPROM write cycle has completed, so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid device address byte with the R/$\overline{W}$ bit set at logic '0'. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new read or write operation to be immediately initiated. A flowchart has been included below in Figure 7-3 to better illustrate this technique.

Figure 7-3. Acknowledge Polling Flow Chart

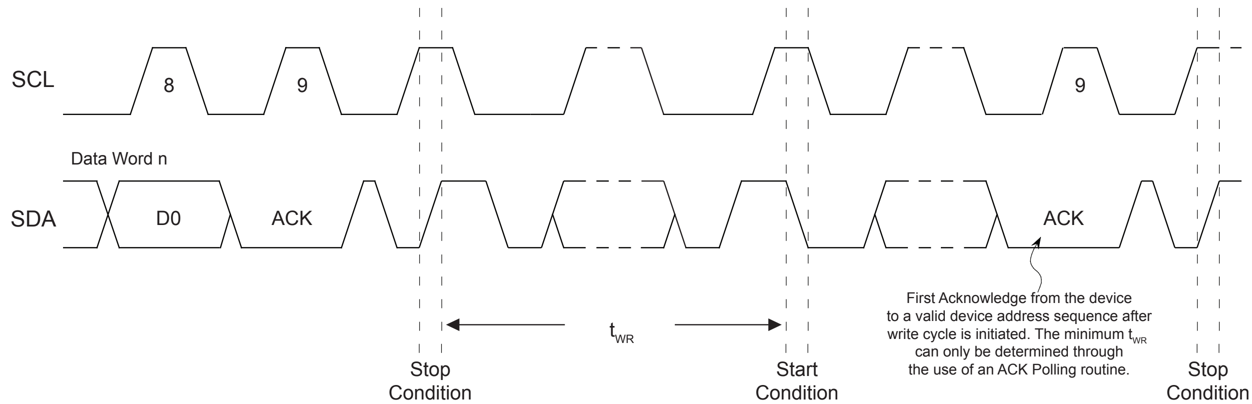


7.4 Write Cycle Timing

The length of the self-timed write cycle (t_{WR}) is defined as the amount of time from the Stop condition that begins the internal write cycle to the Start condition of the first device address byte sent to the AT24C08D that it subsequently responds to with an ACK. Figure 7-4 has been included to show this measurement.

During the internally self-timed write cycle, any attempts to read from or write to the memory array will not be processed.

Figure 7-4. Write Cycle Timing



7.5 Write Protection

The AT24C08D utilizes a hardware data protection scheme that allows the user to write-protect the entire memory contents when the WP pin is at V_{CC} (or a valid V_{IH}). No write protection will be set if the WP pin is at GND or left floating. The 4-ball WLCSP version of the device does not include any write protection features.

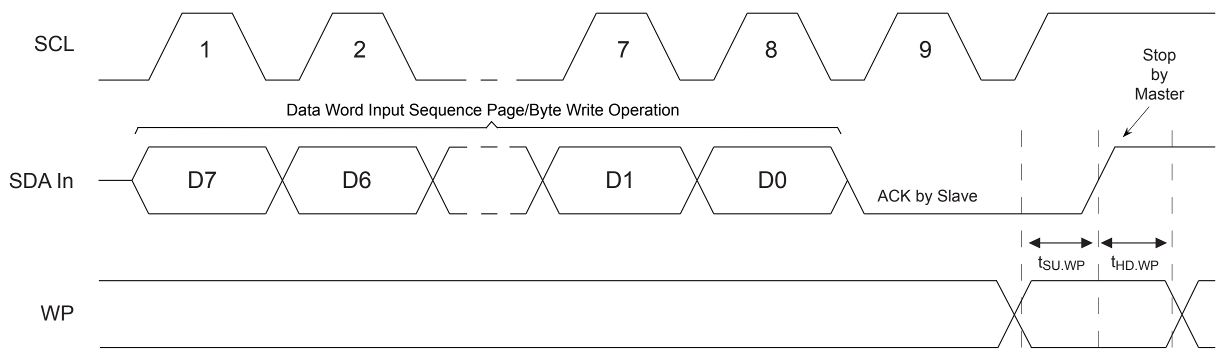
Table 7-1. AT24C08D Write-Protect Behavior

WP Pin Voltage	Part of the Array Protected
V_{CC}	Full Array
GND	None — Write Protection Not Enabled

The status of the WP pin is sampled at the Stop condition for every byte write or page write operation prior to the start of an internally self-timed write cycle. Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle. The WP pin state must be valid with respect to the associated setup ($t_{SU.WP}$) and hold ($t_{HD.WP}$) timing as shown in Figure 7-5 below. The WP setup time is the amount of time that the WP state must be stable before the Stop condition is issued. The WP hold time is the amount of time after the Stop condition that the WP pin must remain stable.

If an attempt is made to write to the device while the WP pin has been asserted, the device will acknowledge the device address, word address and data bytes, but no write cycle will occur when the Stop condition is issued. The device will immediately be ready to accept a new read or write command.

Figure 7-5. Write-Protect Setup and Hold Timing



8. Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write Select bit in the device address byte must be a logic '1'. There are three read operations:

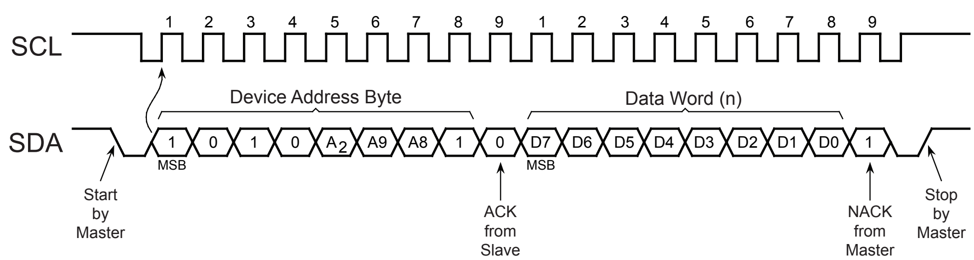
- Current Address Read
- Random Address Read
- Sequential Read

8.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V_{CC} is maintained to the part. The address roll-over during a read is from the last byte of the last page to the first byte of the first page of the memory.

A current address read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of read operations will be terminated if the bus master does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

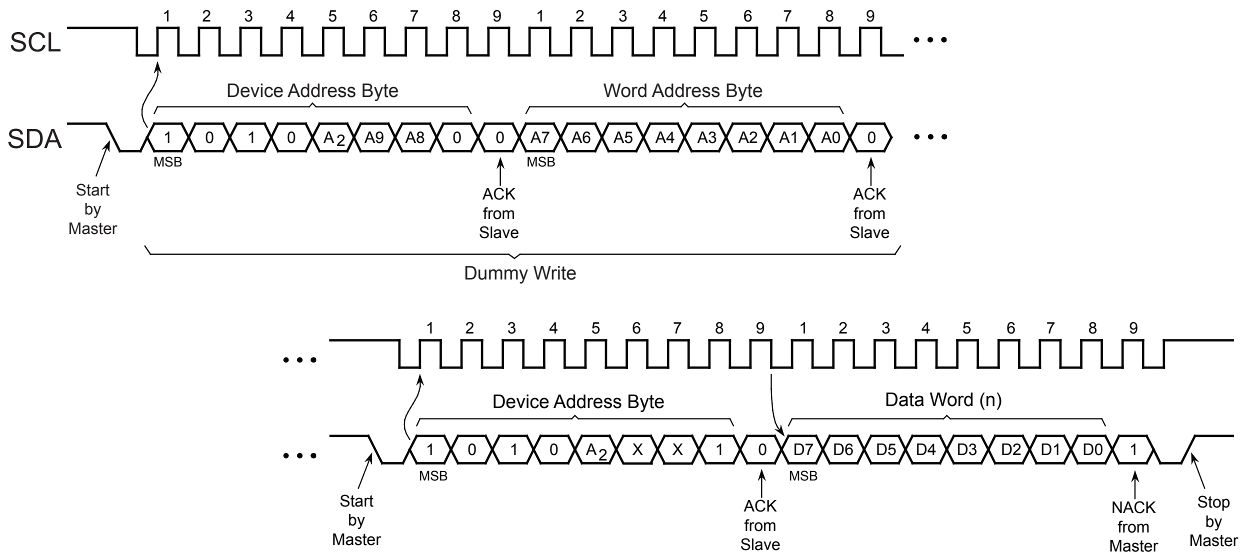
Figure 8-1. Current Address Read



8.2 Random Read

A random read begins in the same way as a byte write operation does to load in a new data word address. This is known as a "dummy write" sequence; however, the data byte and the Stop condition of the byte write must be omitted to prevent the part from entering an internal write cycle. Once the device address and word address are clocked in and acknowledged by the EEPROM, the bus master must generate another Start condition. The bus master now initiates a current address read by sending a Start condition, followed by a valid device address byte with the R/$\overline{W}$ bit set to logic '1'. In this second device address byte, the bit positions usually reserved for the Most Significant bits of the word address (bit 2 and 1) are "don't care" bits since the address that will be read from is determined only by what was sent in the dummy write portion of the sequence. The EEPROM will ACK the device address and serially clock out the data word on the SDA line. All types of read operations will be terminated if the bus master does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

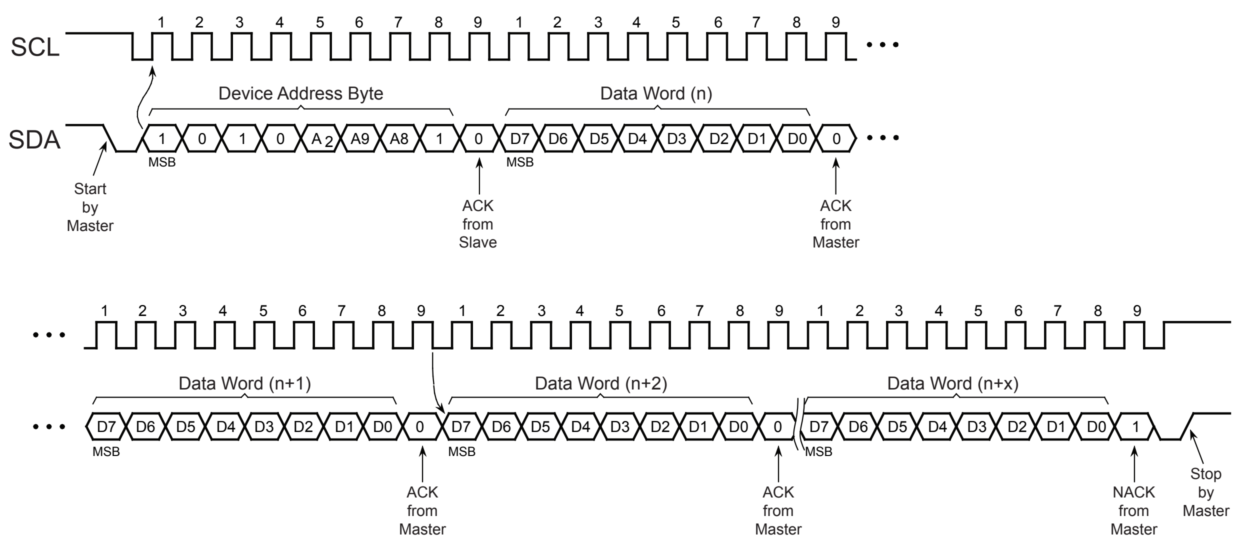
Figure 8-2. Random Read



8.3 Sequential Read

Sequential reads are initiated by either a current address read or a random read. After the bus master receives a data word, it responds with an Acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out sequential data words. When the maximum memory address is reached, the data word address will roll-over and the sequential read will continue from the beginning of the memory array. All types of read operations will be terminated if the bus master does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

Figure 8-3. Sequential Read



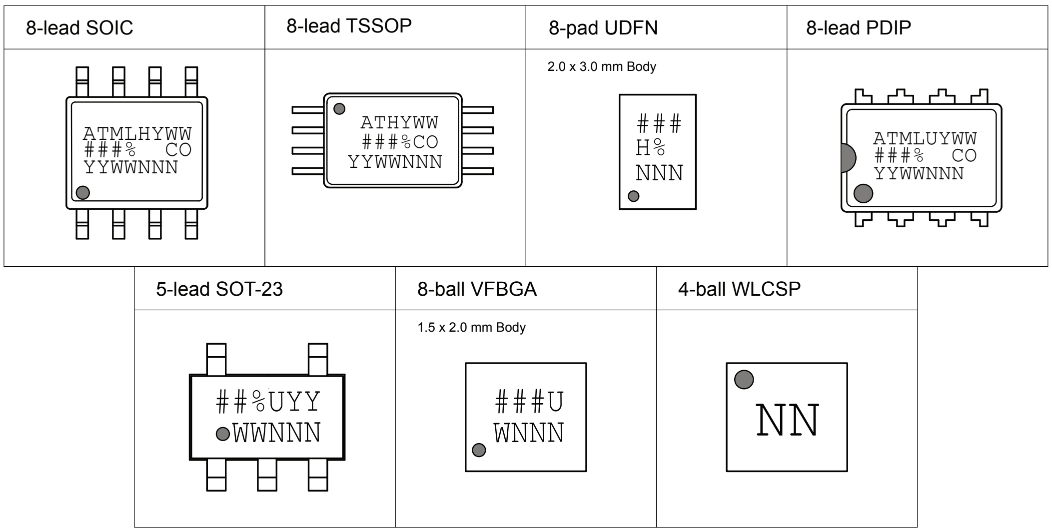
9. Device Default Condition from Microchip

The AT24C08D is delivered with the EEPROM array set to logic '1', resulting in FFh data in all locations.

10. Packaging Information

10.1 Package Marking Information

AT24C08D: Package Marking Information



Note 1: ● designates pin 1
Note 2: Package drawings are not to scale
Note 3: For SOT23 package with date codes before 7B, the bottom line (YMXX) is marked on the bottom side and there is no Country of Assembly (@) mark on the top line.

Catalog Number Truncation	
AT24C08D	Truncation Code ###: 08D / ##: 8D

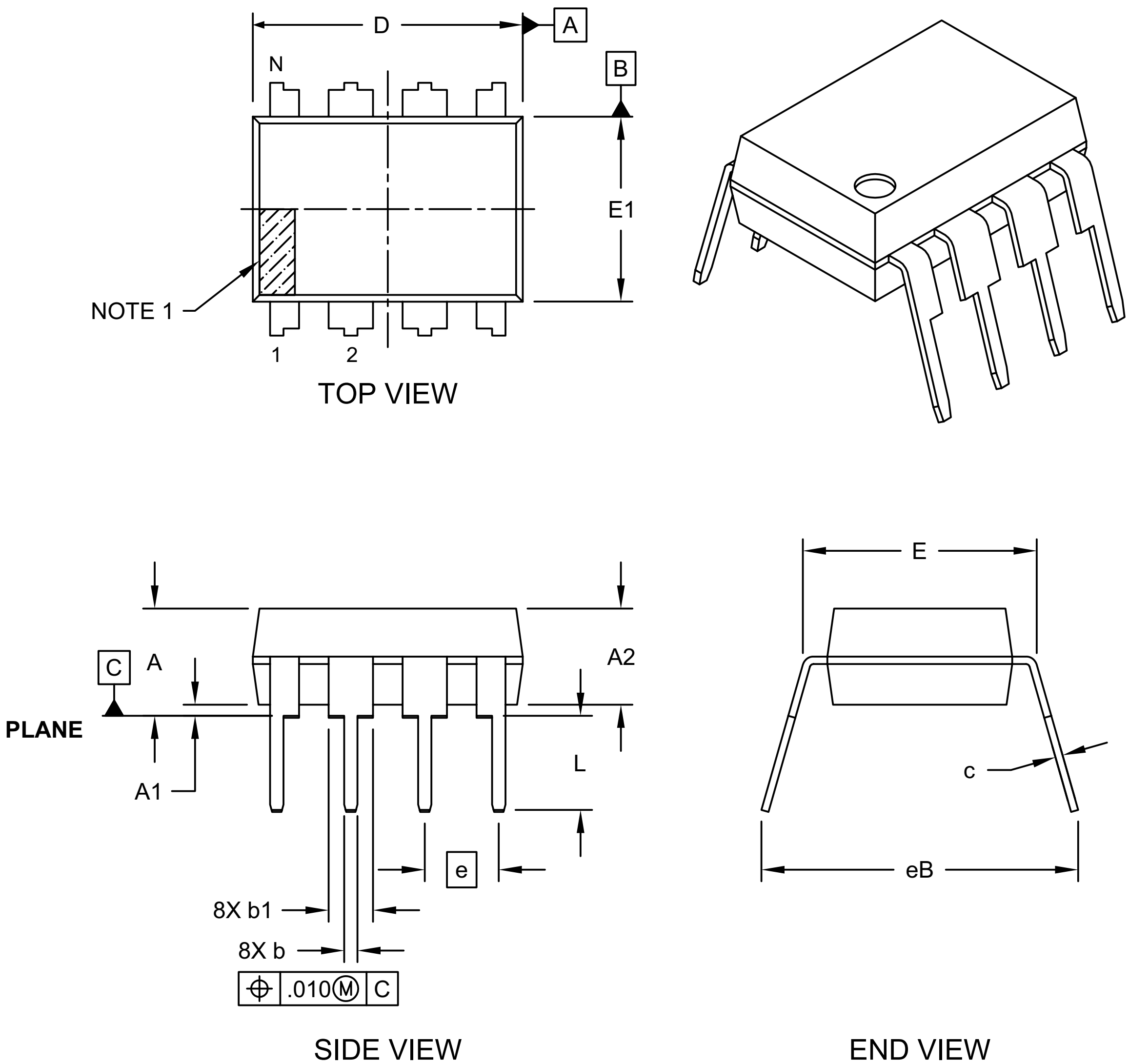
Date Codes					**Voltages**
YY = Year		Y = Year		WW = Work Week of Assembly	% = Minimum Voltage
16: 2016	20: 2020	6: 2016	0: 2020	02: Week 2	M: 1.7V min
17: 2017	21: 2021	7: 2017	1: 2021	04: Week 4	
18: 2018	22: 2022	8: 2018	2: 2022	...	
19: 2019	23: 2023	9: 2019	3: 2023	52: Week 52	

Country of Origin	**Device Grade**	**Atmel Truncation**
CO = Country of Origin	H or U: Industrial Grade	AT: Atmel ATM: Atmel ATML: Atmel

Trace Code
NNN = Alphanumeric Trace Code (2 Characters for Small Packages)

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

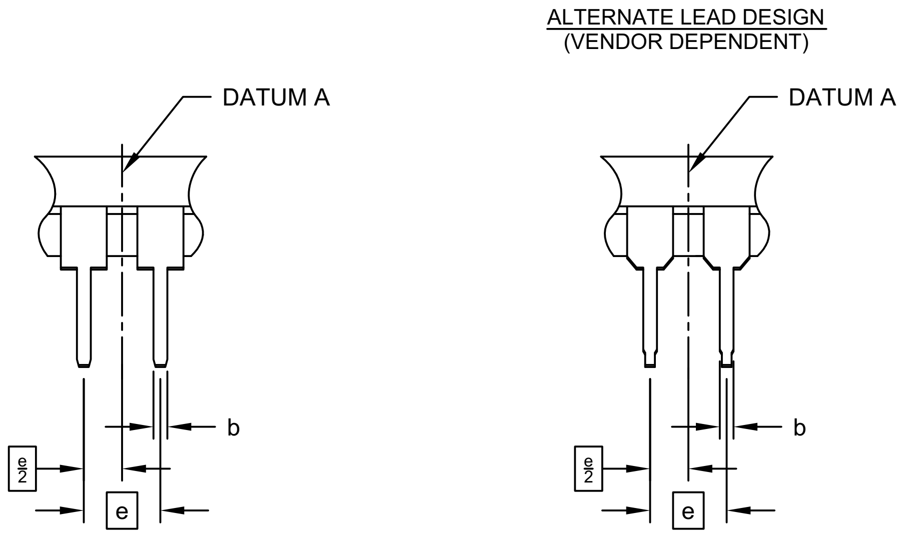
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

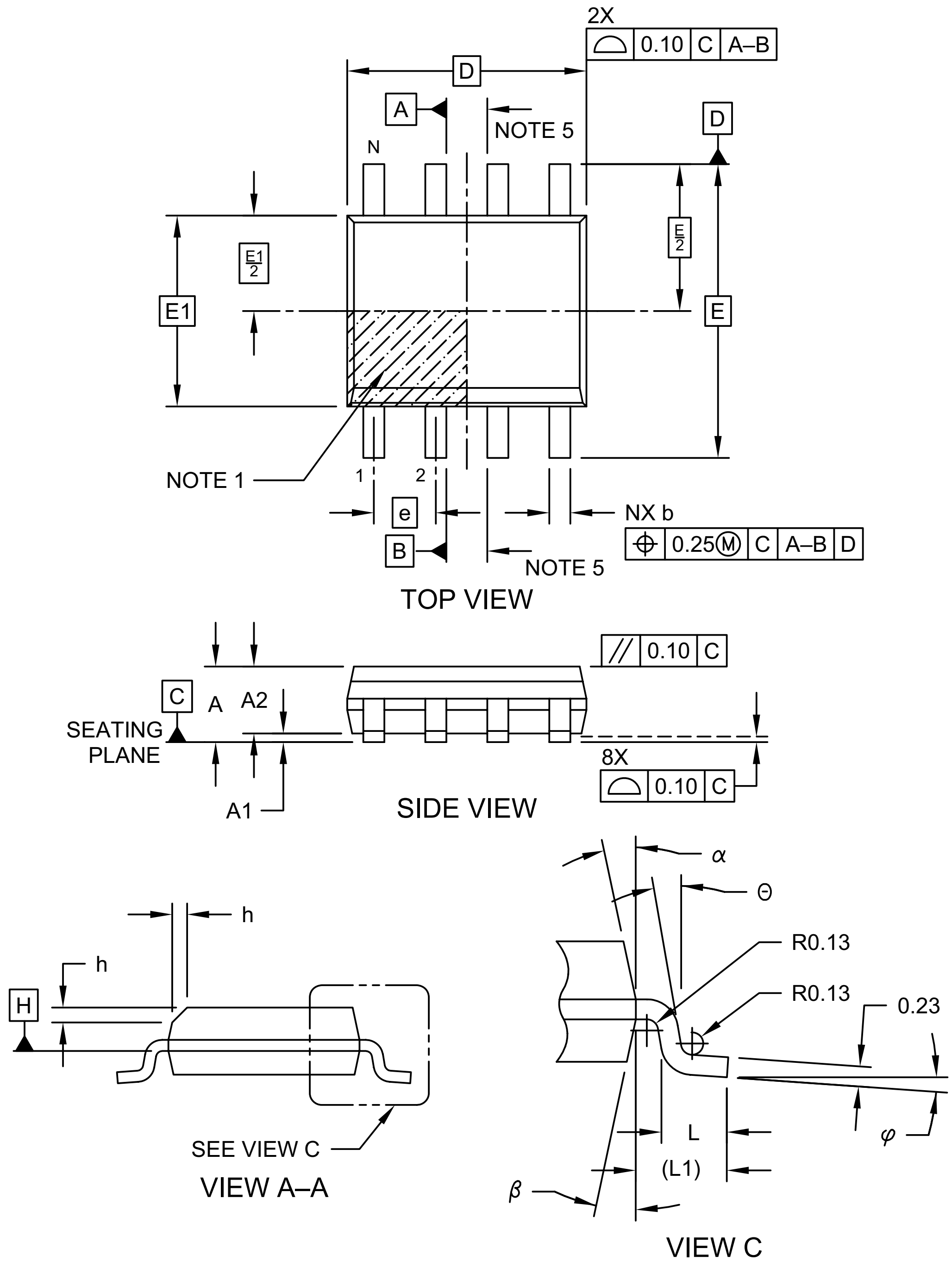
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

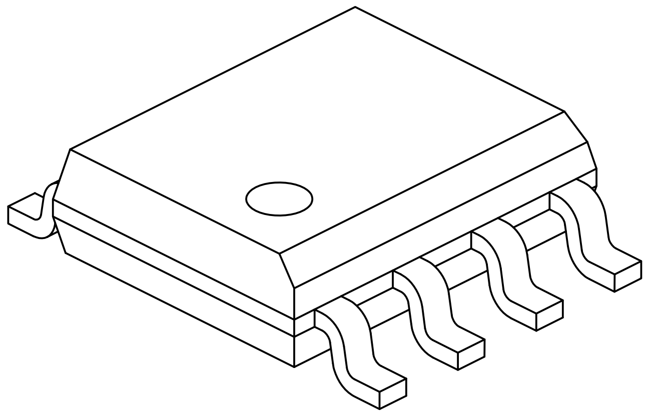
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

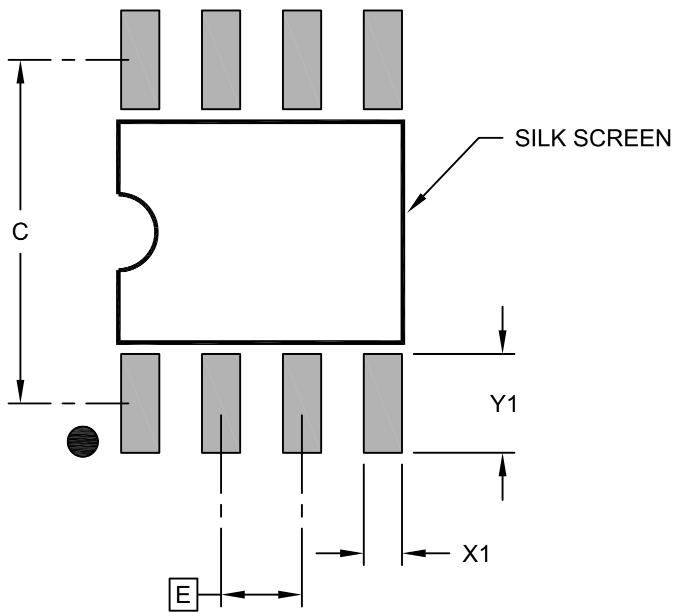
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

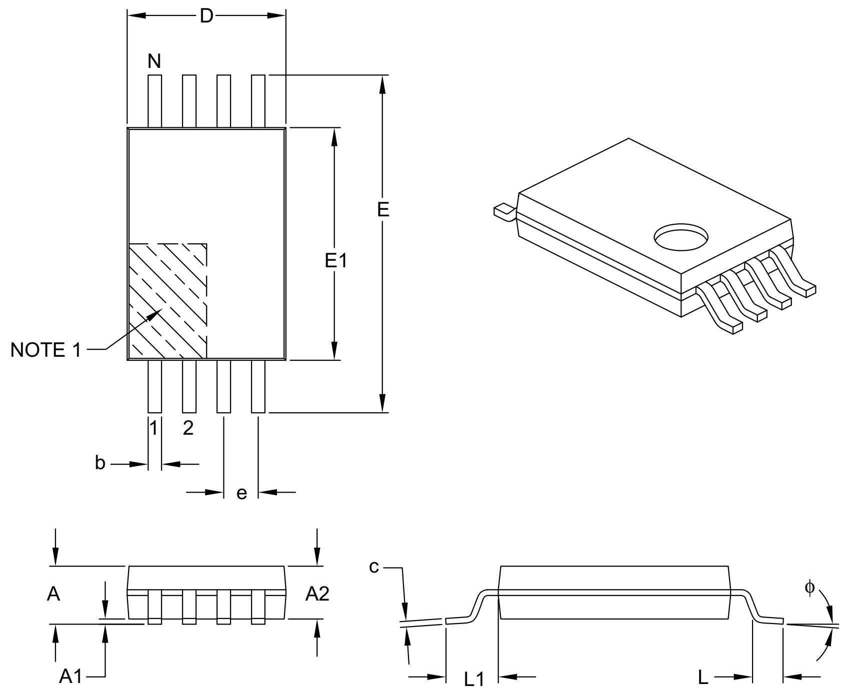
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

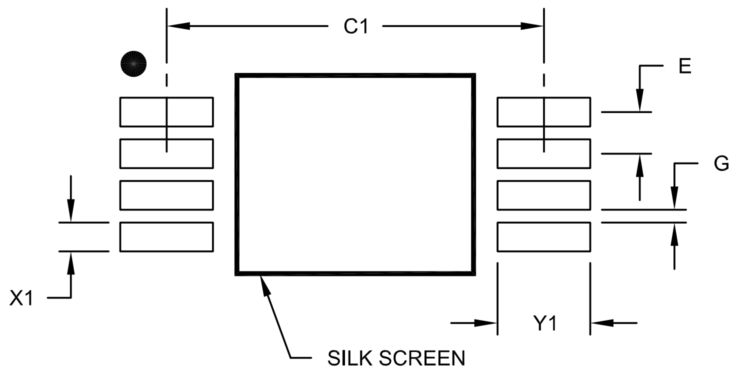
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

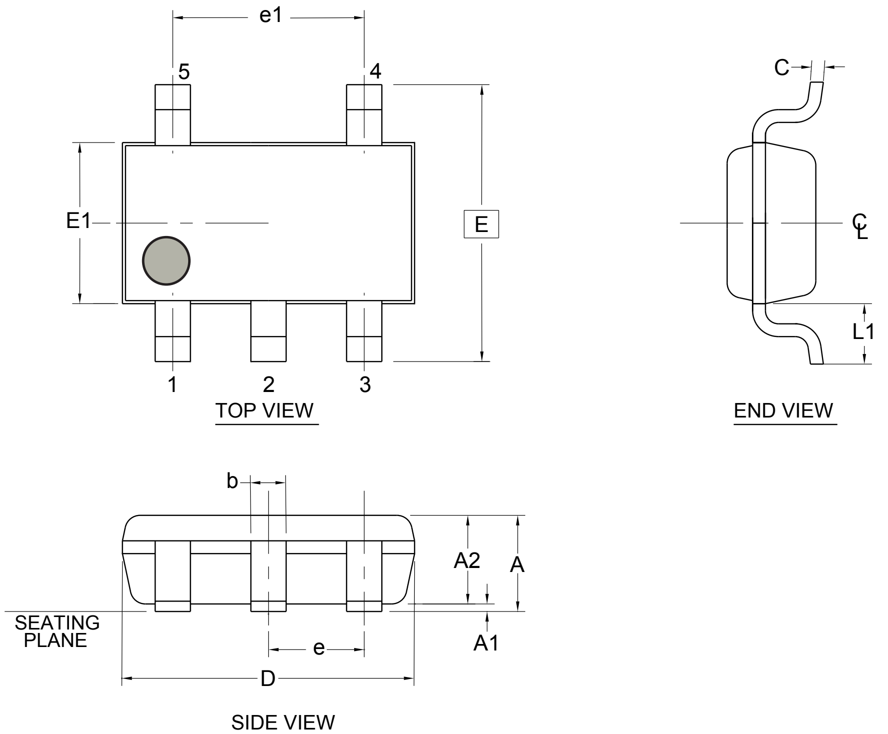
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A



1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.00	
A1	0.00	—	0.10	
A2	0.70	0.90	1.00	
c	0.08	—	0.20	3
D		2.90 BSC		1,2
E		2.80 BSC		1,2
E1		1.60 BSC		1,2
L1		0.60 REF		
e		0.95 BSC		
e1		1.90 BSC		
b	0.30	—	0.50	3,4

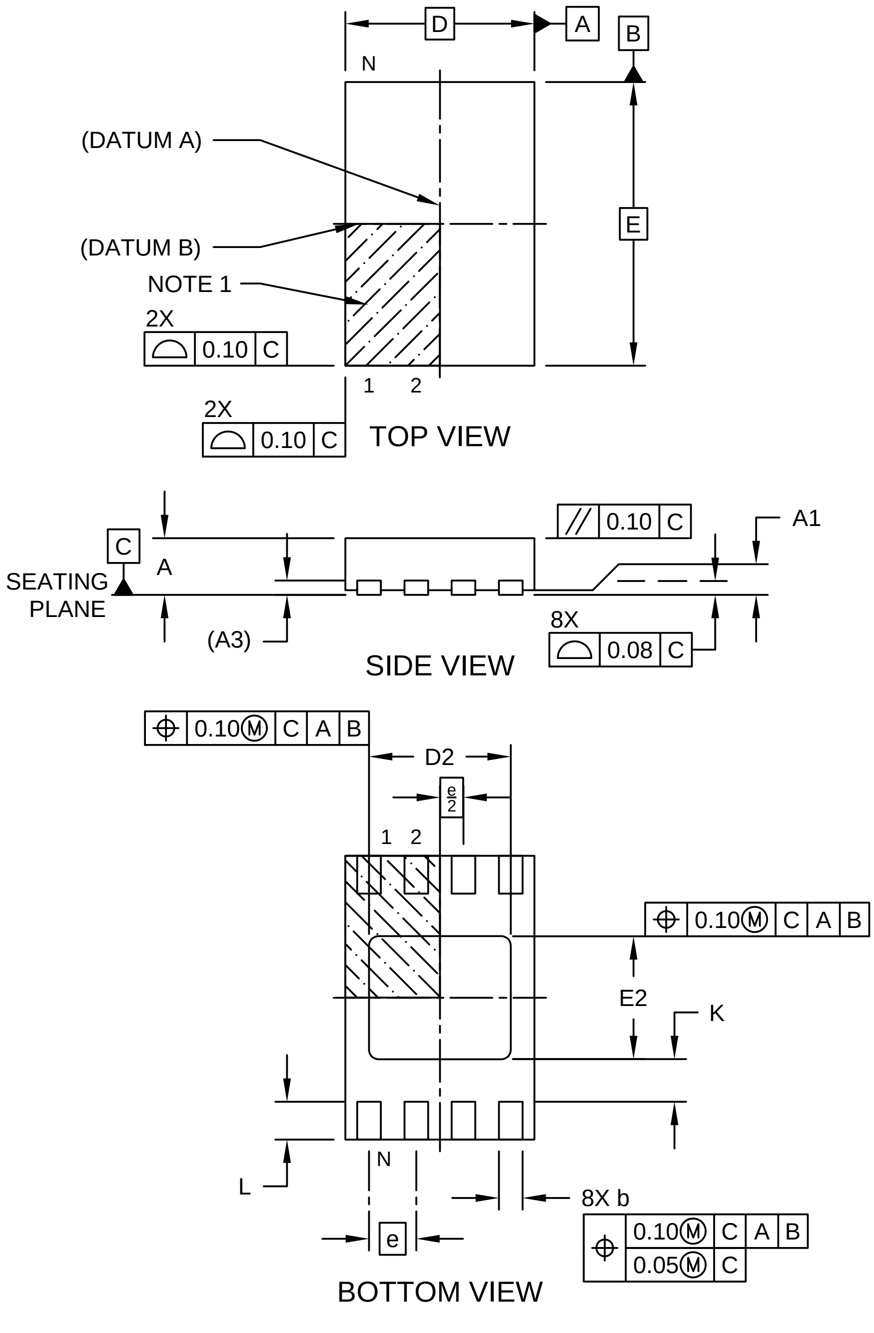
2/2/16

	TITLE	GPC	DRAWING NO.	REV.
	5TS1, 5-lead 1.60mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	TSZ	5TS1	E

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

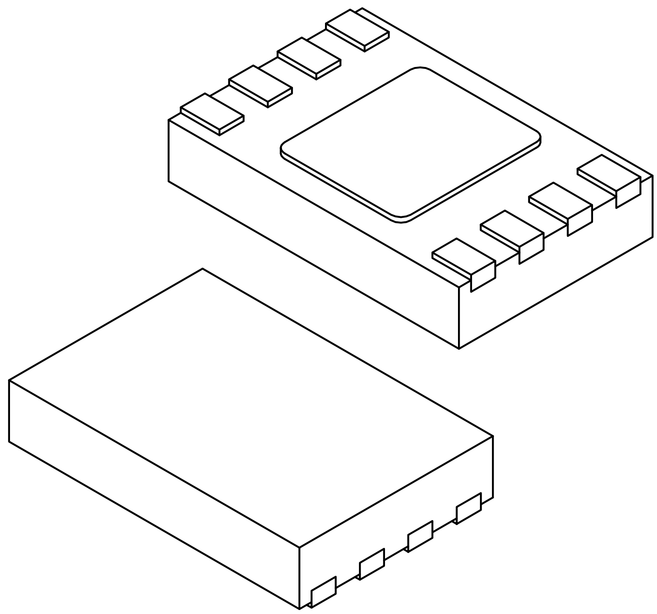
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21355-Q4B Rev A Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

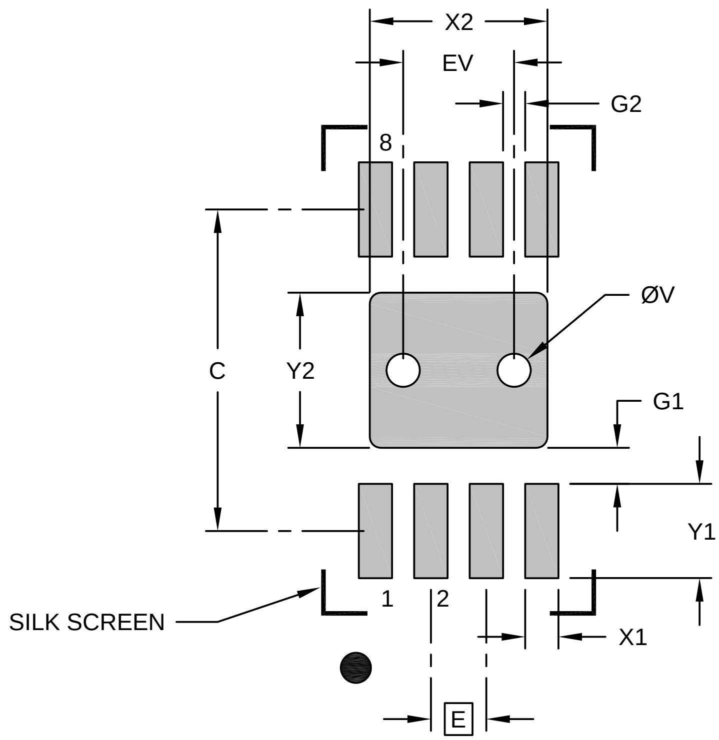
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev A Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



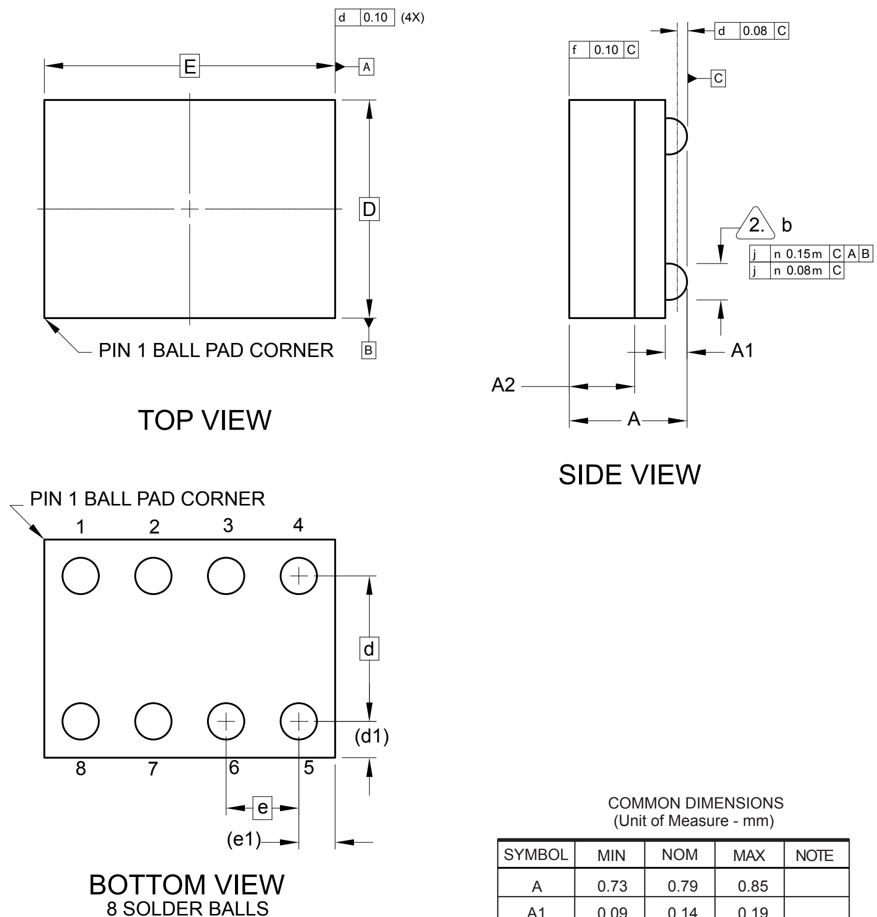
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.33		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-21355-Q4B Rev A



Notes:

1. This drawing is for general information only.
2. Dimension ‘b’ is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

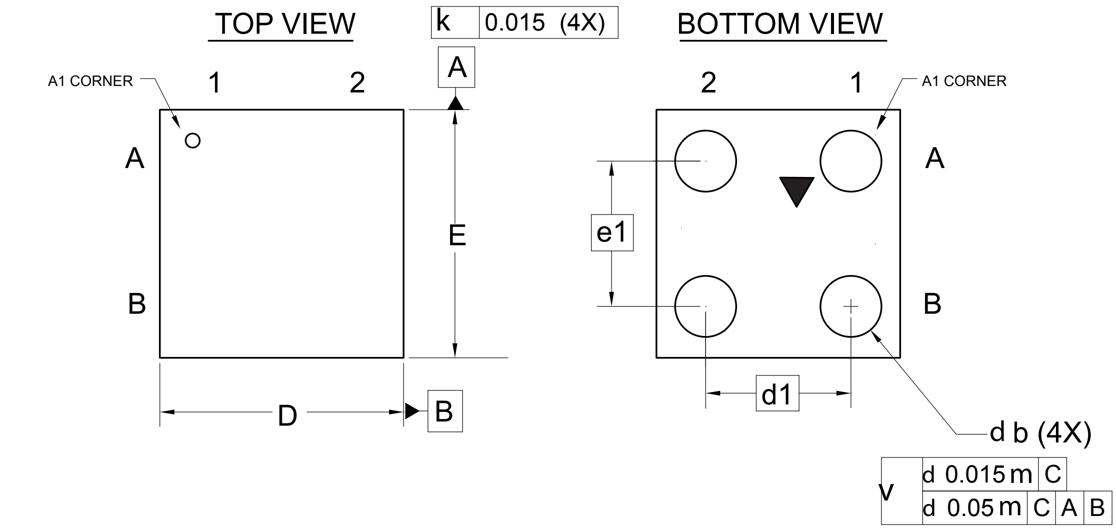
COMMON DIMENSIONS
(Unit of Measure - mm)

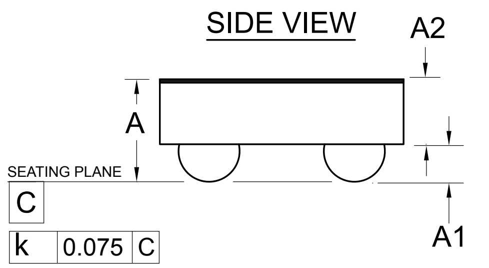
SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D		1.50 BSC		
E		2.0 BSC		
e		0.50 BSC		
e1		0.25 REF		
d		1.00 BSC		
d1		0.25 REF		

7/1/14

	TITLE	GPC	DRAWING NO.	REV.
	8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GXU	8U3-1	G

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.





PIN ASSIGNMENT MATRIX

	1	2
A	V_{CC}	GND
B	SCL	SDA

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.260	0.295	0.330	
A1	—	0.080	—	
A2	—	0.215	—	3
D	Contact Microchip for Details			
d1	0.400 BSC			
E	Contact Microchip for Details			
e1	0.400 BSC			
b	—	0.162	—	

Note: 1. Dimensions are NOT to scale.
2. Solder ball composition is 95.5Sn-4.0Ag-0.5Cu.
3. Product offered with Back Side Coating (BSC)

8/28/15

TITLE	GPC	DRAWING NO.	REV.
4U-4, 4-ball 2x2 Array, 0.40mm Pitch Wafer Level Chip Scale Package (WLCSP) with BSC	GEG	4U-4	F

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

11. Revision History

Atmel Document 8880 Revision A (February 2014)
Initial release of this document.

Atmel Document 8880 Revision B (April 2014)
Grammatical corrections, corrected standby current from 1 μA to 0.8 μA in the features list, and refined sections “Current Address Read”, “Random Read”, “Sequential Read”, and “Device Reset”. Updated data sheet status from preliminary to complete release.

Atmel Document 8880 Revision C (January 2015)
Added 100 kHz timing set for reference, the UDFN extended quantity option, and the figure for “System Configuration Using 2-Wire Serial EEPROMs”. Updated the package outline drawings and the ordering information section.

Atmel Document 8880 Revision D (April 2015)
Added part number AT24C08D-UUM1B-T to the ordering information section. Updated the 8S1 package drawing.

Atmel Document 8880 Revision E (January 2016)
Updated the 8MA2 and 4U-4 package drawings.

Atmel Document 8880 Revision F (December 2016)
Part marking SOT23:
- Moved backside mark (YMXX) to front side line2.
- Added @ = Country of Assembly

Atmel Document 8880 Revision G (January 2017)
Updated Power On Requirements and Reset Behavior section

Revision A (June 2018)
Updated to the Microchip template. Microchip DS20006022 replaces Atmel document 8800. Updated Part Marking Information. Updated the "Software Reset" section. Added ESD rating. Removed lead finish designation. Updated trace code format in package markings. Updated section content throughout for clarification. Updated the 5TS1 SOT23 and 8U3-1 VFBGA package drawings. Updated the PDIP, SOIC, TSSOP and UDFN package drawings to Microchip format.

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A T 2 4 C 0 8 D - S S H M x x - T

Product Family
24C = Standard I²C-compatible Serial EEPROM

Device Density
08 = 8 Kilobit

Device Revision

Shipping Carrier Option
T = Tape and Reel, Standard Quantity Option
E = Tape and Reel, Extended Quantity Option
B = Bulk (Tubes)

Product Variation
xx = Applies to select packages only.

Operating Voltage
M = 1.7V to 3.6V

Device Grade or Wafer/Die Thickness
H or U = Industrial Temperature Range (-40°C to +85°C)
11 = 11mil Wafer Thickness

Package Option
SS = SOIC
X = TSSOP
MA = 2.0mm x 3.0mm UDFN
P = PDIP
ST = SOT23
C = VFBGA
U = WLCSP
WWU= Wafer Unsawn

Examples

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT24C08D-PUM	PDIP	P	P	Bulk (Tubes)	Industrial Temperature (-40°C to 85°C)
AT24C08D-SSHM-T	SOIC	SN	SS	Tape and Reel	
AT24C08D-STUM-T	SOT23	5TS1	ST	Tape and Reel	
AT24C08D-XHM-B	TSSOP	ST	X	Bulk (Tubes)	
AT24C08D-MAHM-T	UDFN	Q4B	MA	Tape and Reel	
AT24C08D-MAHM-E	UDFN	Q4B	MA	Extended Qty. Tape and Reel	
AT24C08D-CUM-T	VFBGA	8U3-1	C	Tape and Reel	
AT24C08D-UUM0B-T	WLCSP	4U-4	U	Tape and Reel	

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