Evaluation Board for LTC1564 Digitally Controlled Antialiasing Filter and 4-Bit P.G.A.

DESCRIPTION

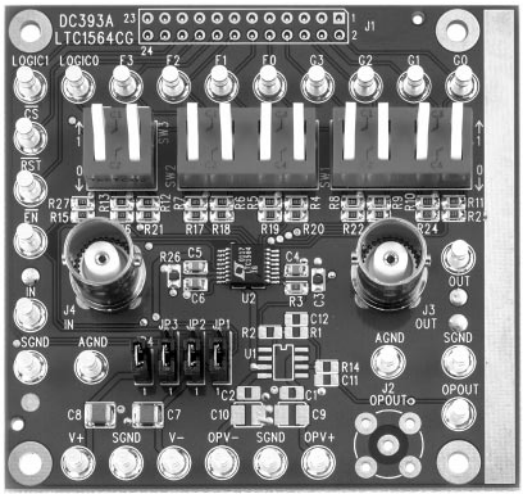
This demonstration circuit allows the user to evaluate the LTC®1564 digitally controlled antialiasing filter. The cutoff frequency (f_C) and passband gain are fully programmable while the shape of the lowpass response is fixed. A latching digital interface stores f_C and gain settings or it can be bypassed for control directly from the pins through either the on-board toggle switches or using the optional connector to control the pins externally. The LTC1564 operates from 2.7V to 10V total supply voltage (single or split supplies) and comes in a 16 pin surface mount SSOP. This board demonstrates proper layout, bypassing and optional buffering to achieve best performance. Applications include DSP antialiasing and reconstruction filtering, communications and instruments with high dynamic range, up to 20 bits, and sampling rates to 300+ kilosamples per second.

Some key features of this demo circuit include:

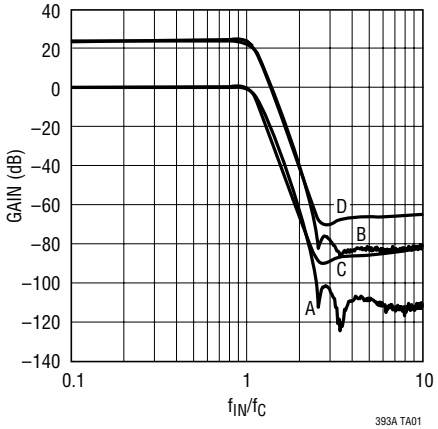
- 4-bit digitally controlled 8th order lowpass filter
- f_C = 10kHz to 150kHz in 10kHz steps
- 4-bit digitally controlled programmable gain amplifier
- G = 1 to 16 in 1V/V steps
- 100dB attenuation at 2.5 • f_C
- Rail-to-rail input and output range
- Miniature 16-Pin SSOP package

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Demo Circuit

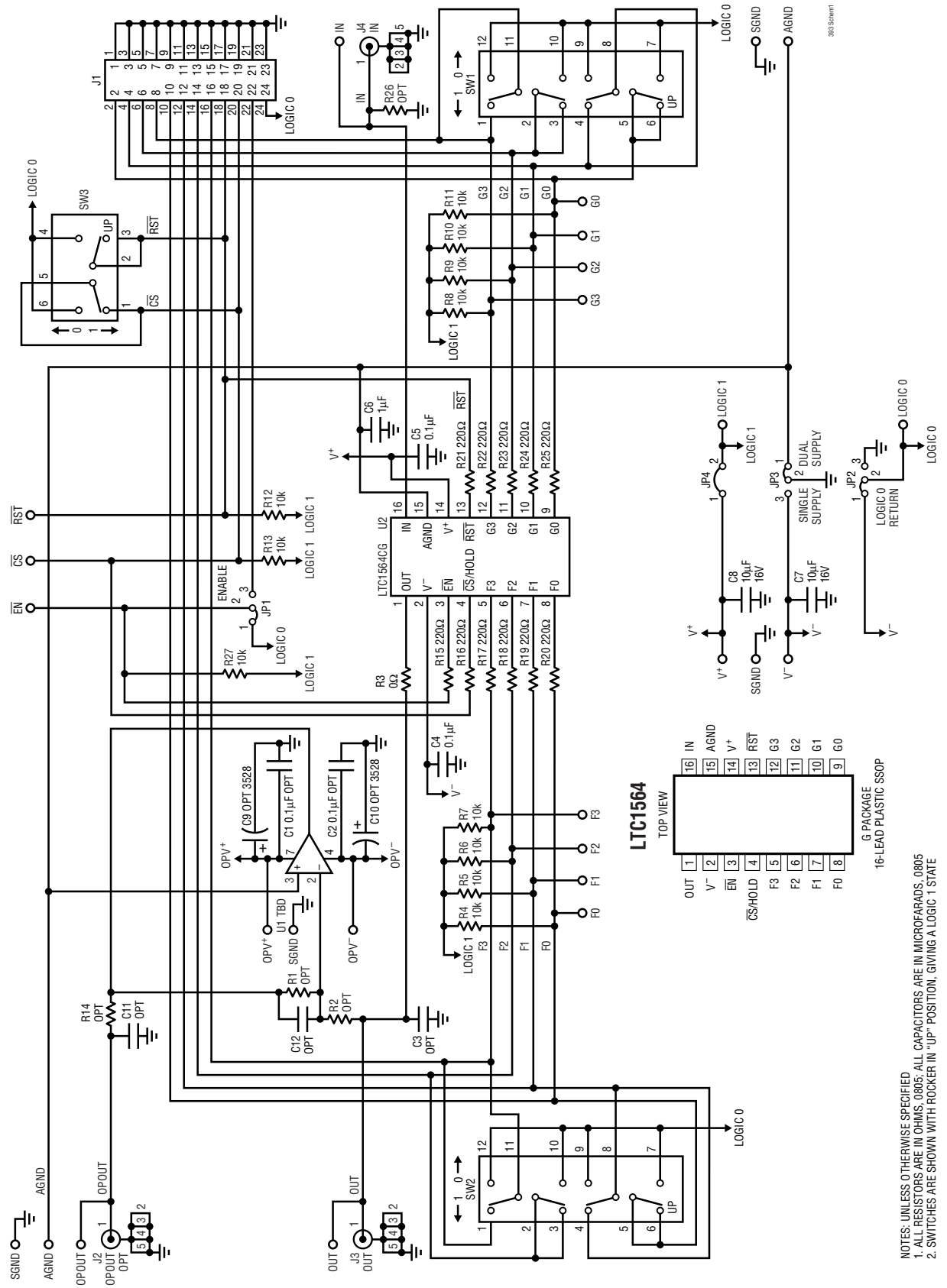


Frequency Response



A: f_C = 10kHz, GAIN = 1, V_{IN} = 1V_{RMS}
B: f_C = 10kHz, GAIN = 16, V_{IN} = 62.5mV_{RMS}
C: f_C = 150kHz, GAIN = 1, V_{IN} = 1V_{RMS}
D: f_C = 150kHz, GAIN = 16, V_{IN} = 62.5mV_{RMS}

PACKAGE AND SCHEMATIC DIAGRAM



PARTS LIST

REFERENCE	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
(2) AGND, (3) SGND, F0–F3, G0–G3, IN, OUT, CS, RST, EN, V^+, V^-, LOGIC 0, LOGIC 1, OPV^+, OPV^-, OPOUT	25	2501-2	1-Pin Terminal Turret, 0.094"	MILL-MAX	(516) 922-6000
C1–C3, C9–C12	Optional	TBD	Capacitor	TBD	
C4, C5	2	0805ZC104MAT1A	0.1µF 10V X7R Capacitor	AVX	(843) 946-0362
C6	1	0805ZC105MAT1A	1µF 10V X7R Capacitor	AVX	(843) 946-0362
C7, C8	2	EMK325BJ106MN	10µF 16V, 20% 1210 XR5 Capacitor	Taiyo Yuden	(408) 573-4150
J1	Optional	TBD	Header	TBD	
J2	Optional	TBD	BNC	TBD	
J3, J4	2	112404	BNC	Connex	(805) 378-6464
JP1, JP2, JP3	3	3801S-3G2	Header, 3 Pins 1 Row 0.1"cc	Comm Con	(626) 301-4200
JP4	1	3801S-2G2	Header, 2 Pins 1 Row 0.1"cc	Comm Con	(626) 301-4200
JP1–JP4	4	CCIJ230-G	Shunts for JP1–JP4 , 0.1"cc	Comm Con	(626) 301-4200
R1, R2, R14, R26	Optional	TBD	Resistor	TBD	
R3	1	CJ10-000M	0Ω 1/16W 5% Resistor	AAC	(800) 508-1521
R4–R13, R27	11	CR10-103JM	10k 1/16W 5% Resistor	AAC	(800) 508-1521
R15–R25	11	CR10-221JM	220Ω 1/16W 5% Resistor	AAC	(714) 255-9186
SW1, SW2	2	76STC04	Switch SPDT-4 FORM C	Gray Hill	(708) 354-1040
SW3	1	76STC02	Switch SPDT-2 FORM C	Gray Hill	(708) 354-1040
U1	Optional	TBD	IC	TBD	
U2	1	LTC1564CGN	IC	LTC	(408) 432-1900

OPERATION

Demo Board Operation and Connection Hints

When using the DC393 demo board, the following steps should be taken to ensure proper operation for evaluating the LTC1564. This demo board was designed for either single or dual supply operation.

The LTC1564 has only three analog pins: input, output and a half-supply reference voltage point, AGND. The other pins are digital controls and power supply.

Step 1: Check the JP1 Jumper Setting. This jumper is the digital chip enable input for the LTC1564. Install the jumper between Pins 1 and 2 for normal operation ($\overline{EN}$ = 0) or between pins 2 and 3 ($\overline{EN}$ = 1) for shutdown mode with reduced supply current. The active circuitry in the LTC1564 shuts off and its output assumes a high impedance state. If F and G bits are latched ($\overline{CS}$/HOLD = 1) during the shutdown state, the latch will retain its contents.

Step 2: Check the JP2 Jumper Setting. The LTC1564's CMOS-level inputs accept CMOS logic levels, either rail-to-rail or, alternatively, 0V and 5V when the part is operated from ±5V supplies. Jumper JP2 sets the logic 0 level to either SGND or V^-. Install the jumper between Pins 1 and 2 for logic 0 = V^- or between Pins 2 and 3 for logic 0 = SGND.

Step 3: Check the JP3 Jumper Setting. Used for selecting single or dual power supply operation. Install the jumper between Pins 1 and 2 for dual supply or between Pins 2 and 3 for single supply.

OPERATION

Step 4: Check the JP4 Jumper Setting. This jumper when installed connects the 10k pull-up resistors to V^+ for all digital inputs of the LTC1564.

Step 5: Check the SW1 Switch Positions. The four switches labeled G3, G2, G1, G0 create a 4-bit binary word for the LTC1564's digital gain control ("G Code") inputs. G3 is the most significant bit (MSB). These switches program the LTC1564's passband gain through the internal latch, which passes the bits directly when the $\overline{CS}$/HOLD input is at logic 0. When $\overline{CS}$/HOLD changes to logic 1, the G switches cease to have effect and the latch retains the previous input values. This gain control is linear in amplitude: nominal passband gain of the LTC1564 is the binary value of the G code plus one, as shown in Table 1.

Step 6: Check the SW2 Switch Positions. The four switches labeled F3, F2, F1, F0 create a 4-bit binary word for the LTC1564's digital frequency control ("F Code") inputs. F3 is the most significant bit (MSB). These switches program the LTC1564's cutoff frequency f_C through the internal latch, which passes the bits directly when the $\overline{CS}$/HOLD input is at logic 0. When $\overline{CS}$/HOLD changes to logic 1, the F pins cease to have effect and the latch holds the previous values. The F code control is the filter's cutoff frequency f_C in 10kHz steps up to 150kHz, as summarized in Table 2. Thus f_C is proportional to the binary value of the F code.

The frequency setting ("F") and gain setting ("G") are each four-bit codes entered through the F and G digital input pins (Table 3). Also, setting the F code to 0000 engages a "mute" state where the filter remains fully powered but the input pin is disconnected inside the LTC1564 and output noise becomes even lower than in normal filter operation.

Step 7: Check the SW3 Switch Positions. The $\overline{CS}$/HOLD switch is the digital enable input for the internal latch holding F and G bits. Logic 0 makes the latch transparent so that the F and G switches directly control the filter's cutoff frequency and gain. Logic 1 holds the last values of these switches prior to the transition. The $\overline{RST}$ switch is the digital asynchronous reset input for the internal F and G latches. Logic 0 at any time will reset these latches to zero.

Table 1. Programming the LTC1564 Gain

G3	G2	G1	G0 (AT OUTPUT OF INTERNAL LATCH)	NOMINAL PASSBAND GAIN (V/V)	(dB)	MAXIMUM INPUT SIGNAL LEVEL (V_{P-P}) DUAL 5V	SINGLE 5V	SINGLE 3V	NOMINAL INPUT IMPEDANCE (k)
0	0	0	0	1	0	10	5	3	10
0	0	0	1	2	6	5	2.5	1.5	5
0	0	1	0	3	9.5	3.33	1.67	1	3.33
0	0	1	1	4	12	2.5	1.25	0.75	2.5
0	1	0	0	5	14	2	1	0.6	2
0	1	0	1	6	15.6	1.67	0.83	0.5	1.67
0	1	1	0	7	16.9	1.43	0.71	0.43	1.43
0	1	1	1	8	18.1	1.25	0.63	0.38	1.25
1	0	0	0	9	19.1	1.1	0.56	0.33	1.11
1	0	0	1	10	20	1	0.5	0.3	1
1	0	1	0	11	20.8	0.91	0.45	0.27	0.91
1	0	1	1	12	21.6	0.83	0.42	0.25	0.83
1	1	0	0	13	22.3	0.77	0.38	0.23	0.77
1	1	0	1	14	22.9	0.71	0.36	0.21	0.71
1	1	1	0	15	23.5	0.67	0.33	0.2	0.66
1	1	1	1	16	24.1	0.63	0.31	0.19	0.63

OPERATION

Step 8: Connecting Power Supply Lines. Electrically clean supplies and a low impedance ground are important for the high dynamic range and high stopband suppression available from the LTC1564. Low noise linear power supplies are recommended. Switching supplies can be used with sufficient filtering to prevent switching noise coupling into the signal path, reducing dynamic range.

Step 9: Input Connection. Connect the input signal to the IN BNC connector. The input of the LTC1564 is connected directly to the IN BNC with an optional R26 shunt resistor connected to SGND. Table 1 shows how the maximum input signal level is inversely proportional to the gain of the filter for different supplies.

Step 10: Output Connection. Connect your monitoring device (oscilloscope, network analyzer, etc.) to the OUT BNC connector. The output of the LTC1564 is designed to drive nominal load of 5kΩ and 50pf. Change the series resistor R3 from 0Ω to 500Ω for capacitances greater than 50pf. Consult the LTC1564 data sheet for more details on output loading issues.

Table 2. Programming the LTC1564 Cutoff Frequency

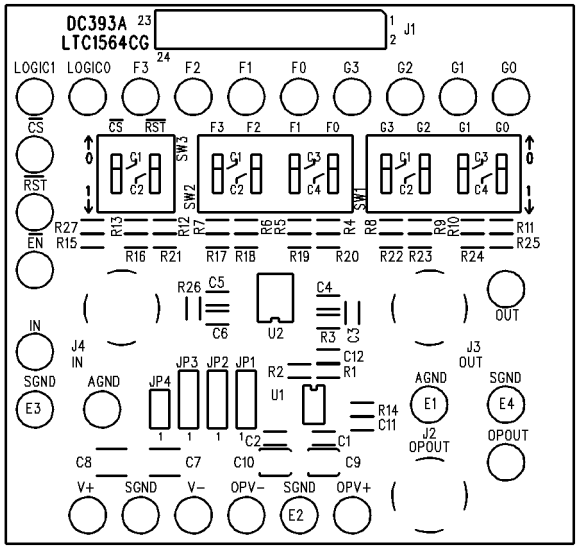
F3 (AT OUTPUT OF INTERNAL LATCH)	F2	F1	F0	NOMINAL f_C (CUTOFF FREQUENCY)
0	0	0	0	0 (Mute State)
0	0	0	1	10kHz
0	0	1	0	20kHz
0	0	1	1	30kHz
0	1	0	0	40kHz
0	1	0	1	50kHz
0	1	1	0	60kHz
0	1	1	1	70kHz
1	0	0	0	80kHz
1	0	0	1	90kHz
1	0	1	0	100kHz
1	0	1	1	110kHz
1	1	0	0	120kHz
1	1	0	1	130kHz
1	1	1	0	140kHz
1	1	1	1	150kHz

Table 3. LTC1564 Digital Controls and Modes

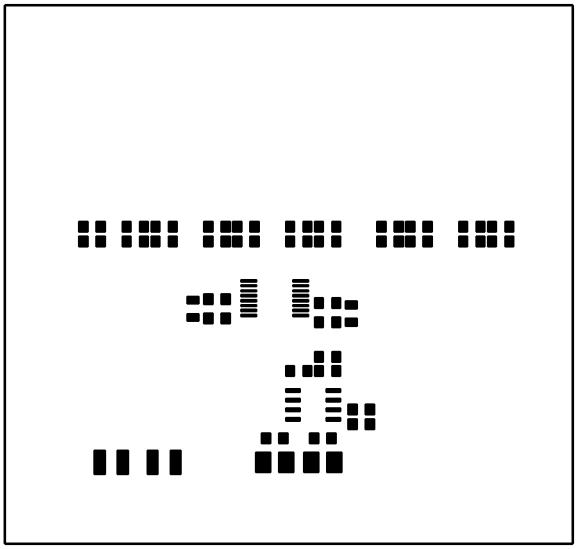
$\overline{EN}$	$\overline{RST}$	$\overline{CS}$/HOLD	F 3	F 2	F I	F 0	G 3	G 2	G 1	G 0	FUNCTION
1	1	1	X	X	X	X	X	X	X	X	Shutdown Mode. Filter Disabled. Latch Holds F and G Inputs Present when Last $\overline{CS}$/HOLD = 0
1	1	0	X	X	X	X	X	X	X	X	Shutdown Mode. Filter Disabled. Latch Accepts F and G Inputs
1	0	X	X	X	X	X	X	X	X	X	Shutdown Mode. Filter Disabled. Latch Contents (F and G) Reset to All Zeros
0	1	0	0	0	0	0	X	X	X	X	Mute Mode. Reduced Noise
0	0	X	X	X	X	X	X	X	X	X	Mute Mode. Reduced Noise Latch Contents (F and G) Reset to All Zeros
0	1	1	Other Than 0 0 0 0				X	X	X	X	Normal Filtering Operation. Latch Holds F and G Inputs Present when Last $\overline{CS}$/HOLD = 0
0	1	0	Other Than 0 0 0 0				X	X	X	X	Normal Filtering Operation. Filter Responds Directly to F and G Input Pins

X = Don't Care

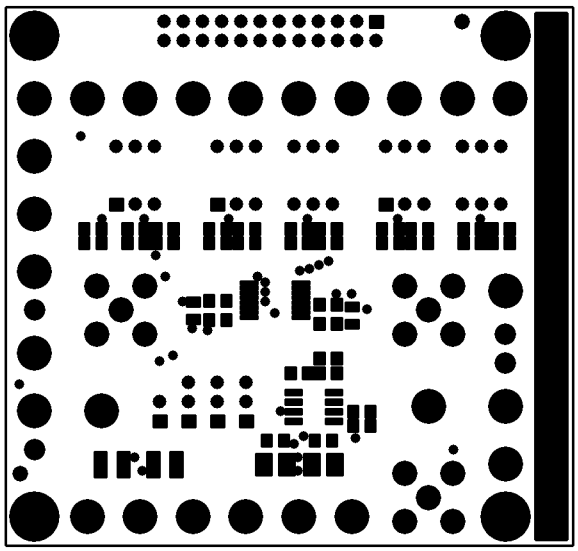
PCB LAYOUT AND FILM



Top Silkscreen

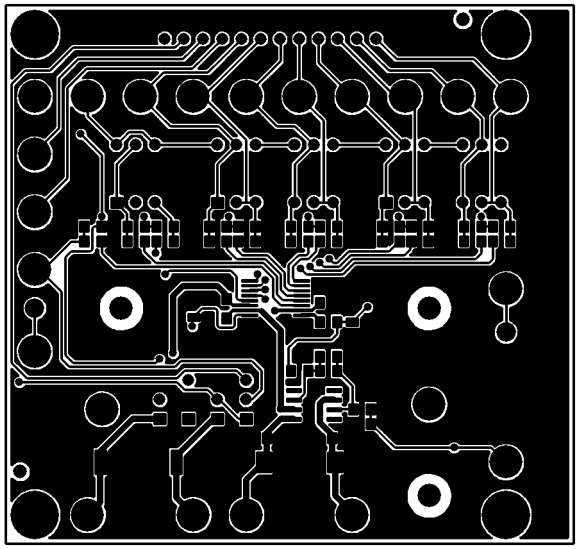


Top Solder Paste

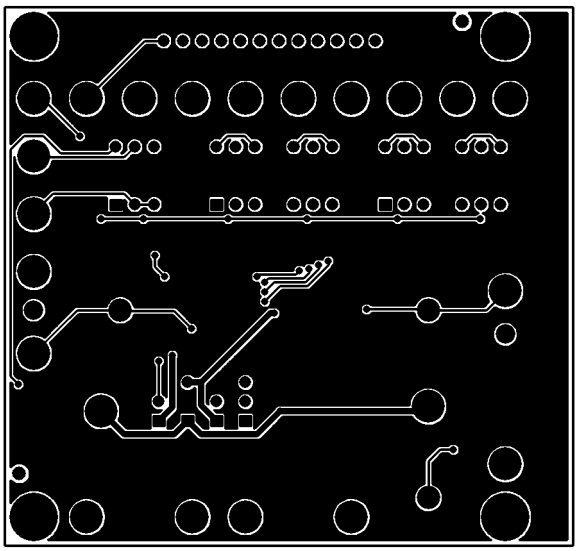


Top Solder Mask

PCB LAYOUT AND FILM

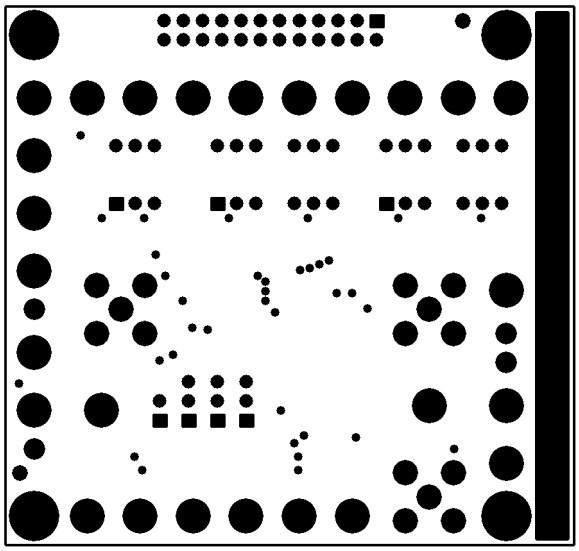


Top Layer

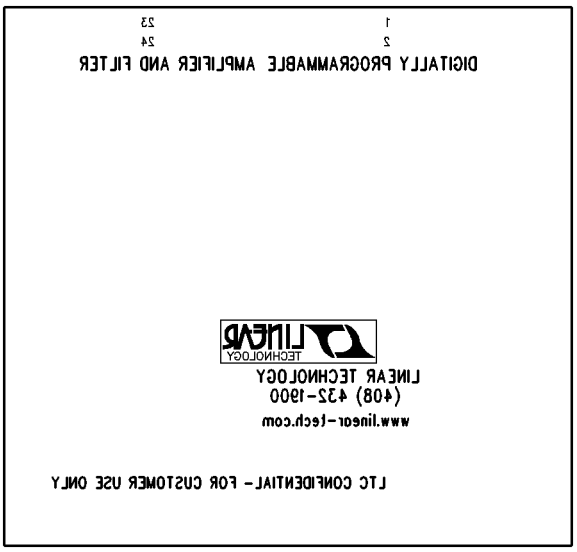


Bottom Layer

PCB LAYOUT AND FILM

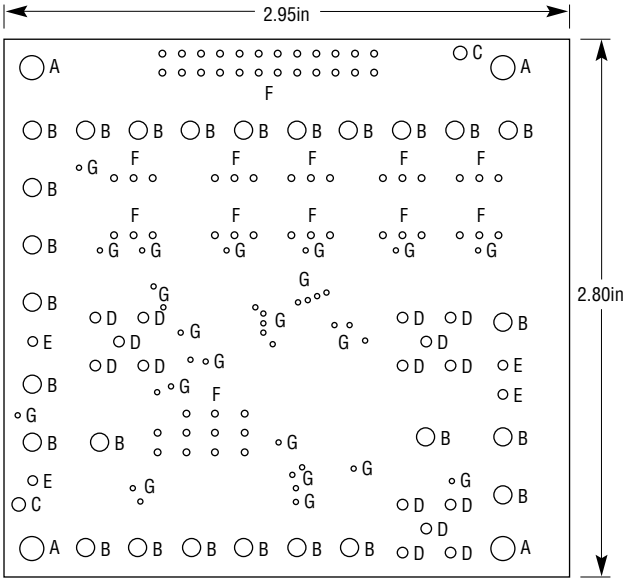


Bottom Solder Mask



Bottom Silkscreen

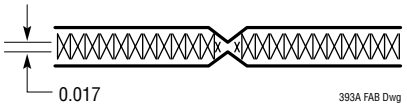
PC FAB DRAWING



HOLE CHART

SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.125	4	YES
B	0.094	26	YES
C	0.070	2	NO
D	0.055	15	YES
E	0.050	4	YES
F	0.035	65	YES
G	0.020	36	YES
TOTAL HOLES		152	

NOTES: UNLESS OTHERWISE SPECIFIED
1. MATERIAL: FR4 OR EQUIVALENT EPOXY, 2 OZ COPPER CLAD
THICKNESS 0.062 ±0.006 TOTAL OF 2 LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.015 MAX COPPER PLATE
ELECTRODEPOSITED TIN-LEAD COMPOSITION
BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK: BOTH SIDES USING LPI OR EQUIVALENT
4. SILKSCREEN: USING WHITE NONCONDUCTIVE EPOXY INK
5. UNUSED SMD COMPONENTS SHOULD BE FREE OF SOLDER
6. FILL UP ALL VIAS WITH SOLDER
7. SCORING



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