Integrated Dual RF Receivers

Data Sheet

ADRV9008-1

FEATURES

Dual receivers
Maximum receiver bandwidth: 200 MHz
Fully integrated, fractional-N, RF synthesizers
Fully integrated clock synthesizer
Multichip phase synchronization for RF LO and baseband clocks
JESD204B datapath interface
Tuning range (center frequency): 75 MHz to 6000 MHz

APPLICATIONS

3G/4G/5G FDD, macrocell base stations
Wideband active antenna systems
Massive multiple input, multiple output (MIMO)
Phased array radar
Electronic warfare
Military communications
Portable test equipment

GENERAL DESCRIPTION

The ADRV9008-1 is a highly integrated, dual radio frequency (RF), agile receiver offering integrated synthesizers and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption required by 3G/4G/5G macrocell, frequency division duplex (FDD), base station applications.

The receive path consists of two independent, wide bandwidth, direct conversion receivers with state-of-the-art dynamic range. The complete receive subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, eliminating the need for these functions in the digital baseband. RF front-end control and several auxiliary functions, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose input/outputs (GPIOs) for the power amplifier (PA), are also integrated.

In addition to automatic gain control (AGC), the ADRV9008-1 also features flexible external gain control modes, allowing dynamic gain control.

The received signals are digitized with a set of four, high dynamic range, continuous time, sigma-delta (Σ-Δ) ADCs that provide inherent antialiasing. The combination of the direct conversion architecture (which does not suffer from out of band image mixing) and the lack of aliasing reduces the requirements of the RF filters compared to the requirements of traditional intermediate frequency (IF) receivers.

The fully integrated phase-locked loop (PLL) provides high performance, low power, fractional-N, RF synthesis for the receiver signal paths. An additional synthesizer generates the clocks needed for the converters, digital circuits, and serial interface. A multichip synchronization mechanism synchronizes the phase of the RF local oscillator (LO) and baseband clocks between multiple ADRV9008-1 chips. The ADRV9008-1 features the isolation that high performance base station applications require. All voltage controlled oscillators (VCOs) and loop filter components are integrated.

The high speed JESD204B interface supports up to 12.288 Gbps lane rates, resulting in a single lane per receiver in the widest bandwidth mode. The interface also supports interleaved mode for lower bandwidths, reducing the total number of high speed data interface lanes to one. Both fixed and floating point data formats are supported. The floating point format allows internal AGC to be invisible to the demodulator device.

The core of the ADRV9008-1 can be powered directly from 1.3 V and 1.8 V regulators and is controlled via a standard 4-wire serial port. Comprehensive power-down modes are included to minimize power consumption during normal use. The ADRV9008-1 is packaged in a 12 mm × 12 mm, 196-ball chip scale ball grid array (CSP_BGA).

Rev. 0 **Document Feedback**

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REVISION HISTORY

9/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

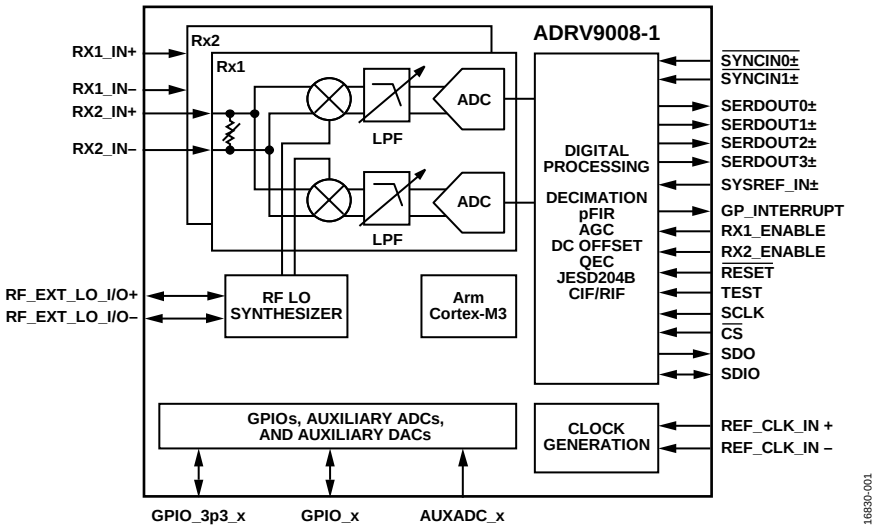


Figure 1.

SPECIFICATIONS

Electrical characteristics at VDDA1P3[1] = 1.3 V, VDDD1P3_DIG = 1.3 V, T_J = full operating temperature range, and LO frequency (f_{LO}) = 1800 MHz, unless otherwise noted. The specifications in Table 1 are not de-embedded. Refer to the Typical Performance Characteristics section for input/output circuit path loss. The device configuration profile for the 75 MHz to 525 MHz frequency range is as follows: receiver = 50 MHz bandwidth (inphase quadrature (I/Q) rate = 61.44 MHz), JESD204B rate = 9.8304 GSPS, and device clock = 245.76 MHz. Unless otherwise specified, the device configuration for all other frequency ranges is as follows: receiver = 200 MHz bandwidth (I/Q rate = 245.76 MHz), JESD204B rate = 9.8304 GSPS, and device clock = 245.76 MHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVERS						
Center Frequency		75		6000	MHz	
Gain Range			30		dB	
Analog Gain Step			0.5		dB	Attenuator steps from 0 dB to 6 dB
			1		dB	Attenuator steps from 6 dB to 30 dB
Bandwidth Ripple			±0.5		dB	200 MHz bandwidth, compensated by programmable finite impulse response (FIR) filter
			±0.2		dB	Any 20 MHz bandwidth span, compensated by programmable FIR filter
Receiver (Rx) Bandwidth				200	MHz	
Receiver Alias Band Rejection		80			dB	Due to digital filters
Maximum Useable Input Level	P_{HIGH}					0 dB attenuation, increases decibel for decibel with attenuation, continuous wave (CW) = 1800 MHz, corresponds to −1 dBFS at ADC
			−11		dBm	75 MHz < f ≤ 3000 MHz
			−10.2		dBm	3000 MHz < f ≤ 4800 MHz
			−9.5		dBm	4800 MHz < f ≤ 6000 MHz
Noise Figure	NF					0 dB attenuation, at receiver port
			11.5		dB	75 MHz < f ≤ 600 MHz
			12		dB	600 MHz < f ≤ 3000 MHz
			13		dB	3000 MHz < f ≤ 4800 MHz
			15.2		dB	4800 MHz < f ≤ 6000 MHz
Ripple			1.8		dB	At band edge maximum bandwidth mode
Input Third-Order Intercept Point	IIP3					
Difference Product			12		dBm	75 MHz < f ≤ 600 MHz, (P_{HIGH} − 12) dB per tone; 600 MHz < f ≤ 6000 MHz, (P_{HIGH} − 10) dB per tone; two tones near band edge
Sum Product			12		dBm	75 MHz < f ≤ 600 MHz, (P_{HIGH} − 12) dB per tone; 600 MHz < f ≤ 6000 MHz, (P_{HIGH} − 10) dB per tone; two tones at bandwidth/6 offset from the LO
Third-Order Harmonic Distortion	HD3					75 MHz < f ≤ 600 MHz, (P_{HIGH} − 6) dB; 600 MHz < f ≤ 6000 MHz, (P_{HIGH} − 4) dB; CW tone at bandwidth/6 offset from the LO
			−65		dBc	75 MHz < f ≤ 600 MHz
			−66		dBc	600 MHz < f ≤ 4800 MHz
			−62		dBc	4800 MHz < f ≤ 6000 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Second-Order Input Intermodulation Intercept Point	IIP2		62		dBm	75 MHz < f ≤ 600 MHz, (P_{HIGH} − 12) dB per tone; 600 MHz < f ≤ 6000 MHz, (P_{HIGH} − 10) dB per tone; 0 dB attenuation, complex
Image Rejection			75		dB	QEC active, within 200 MHz receiver bandwidth
Input Impedance			100		Ω	Differential (see Figure 168)
Receiver to Receiver Isolation			77		dB	75 MHz < f ≤ 600 MHz
			65		dB	600 MHz < f ≤ 4800 MHz
			61		dB	4800 MHz < f ≤ 6000 MHz
Receiver Band Spurs Referenced to RF Input at Maximum Gain			−95		dBm	No more than one spur at this level per 10 MHz of receiver bandwidth
Receiver LO Leakage at Receiver Input at Maximum Gain						Leakage decreases decibel for decibel with attenuation for first 12 dB
			−70		dBm	75 MHz < f ≤ 600 MHz
			−70		dBm	600 MHz < f ≤ 3000 MHz
			−65		dBm	3000 MHz < f ≤ 6000 MHz
LO SYNTHESIZER						
LO Frequency Step			2.3		Hz	1.5 GHz to 2.8 GHz, 76.8 MHz phase frequency detector (PFD) frequency
LO Spur			−85		dBc	Excludes integer boundary spurs
Integrated Phase Noise						2 kHz to 18 MHz
75 MHz LO			0.014		°rms	Narrow PLL loop bandwidth (50 kHz)
1900 MHz LO			0.2		°rms	Narrow PLL loop bandwidth (50 kHz)
3800 MHz LO			0.36		°rms	Wide PLL loop bandwidth (300 kHz)
5900 MHz LO			0.54		°rms	Wide PLL loop bandwidth (300 kHz)
Spot Phase Noise						
75 MHz LO						Narrow PLL loop bandwidth
10 kHz Offset			−126.5		dBc/Hz	
100 kHz Offset			−132.8		dBc/Hz	
1 MHz Offset			−150.1		dBc/Hz	
10 MHz Offset			−150.7		dBc/Hz	
1900 MHz LO						Narrow PLL loop bandwidth
100 kHz Offset			−100		dBc/Hz	
200 kHz Offset			−115		dBc/Hz	
400 kHz Offset			−120		dBc/Hz	
600 kHz Offset			−129		dBc/Hz	
800 kHz Offset			−132		dBc/Hz	
1.2 MHz Offset			−135		dBc/Hz	
1.8 MHz Offset			−140		dBc/Hz	
6 MHz Offset			−150		dBc/Hz	
10 MHz Offset			−153		dBc/Hz	
3800 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−104		dBc/Hz	
1.2 MHz Offset			−125		dBc/Hz	
10 MHz Offset			−145		dBc/Hz	
5900 MHz LO						Wide PLL loop bandwidth
100 kHz Offset			−99		dBc/Hz	
1.2 MHz Offset			−119.7		dBc/Hz	
10 MHz Offset			−135.4		dBc/Hz	
LO PHASE SYNCHRONIZATION						Change in LO delay per temperature change
Phase Deviation			1.6		ps/°C	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL LO INPUT						
Input Frequency	f_{EXTLO}	300		8000	MHz	Input frequency must be 2× the desired LO frequency
Input Signal Power		0		12	dBm	50 Ω matching at the source
			3		dBm	f_{EXTLO} ≤ 2 GHz, add 0.5 dBm/GHz above 2 GHz
			6		dBm	f_{EXTLO} = 8 GHz
External LO Input Signal Differential						To ensure adequate QEC
Phase Error				3.6	ps	
Amplitude Error				1	dB	
Duty Cycle Error				2	%	
Even Order Harmonics				−50	dBc	
CLOCK SYNTHESIZER						
Integrated Phase Noise						1 kHz to 100 MHz
1966.08 MHz LO			0.4		°rms	PLL optimized for close in phase noise
Spot Phase Noise						
1966.08 MHz						
100 kHz Offset			−109		dBc/Hz	
1 MHz Offset			−129		dBc/Hz	
10 MHz Offset			−149		dBc/Hz	
REFERENCE CLOCK (REF_CLK_IN±)						
Frequency Range		10		1000	MHz	
Signal Level		0.3		2.0	V p-p	AC-coupled, common-mode voltage (V_{CM}) = 618 mV, use <1 V p-p input clock for best spurious performance
AUXILIARY CONVERTERS						
ADC						
Resolution			12		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			VDDA_3P3 − 0.05		V	
DAC						
Resolution			10		Bits	Includes four offset levels
Output Voltage						
Minimum			0.7		V	1 V V_{REF}
Maximum			VDDA_3P3 − 0.3		V	2.5 V V_{REF}
Output Drive Capability			10		mA	
DIGITAL SPECIFICATIONS (CMOS): SERIAL PERIPHERAL INTERFACE (SPI), GPIO_x						
Logic Inputs						
Input Voltage						
High Level		VDD_INTERFACE × 0.8		VDD_INTERFACE	V	
Low Level		0		VDD_INTERFACE × 0.2	V	
Input Current						
High Level		−10		+10	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDD_INTERFACE × 0.8			V	
Low Level				VDD_INTERFACE × 0.2	V	
Drive Capability			3		mA	
DIGITAL SPECIFICATIONS (CMOS): GPIO_3p3_x						
Logic Inputs						
Input Voltage						
High Level		VDDA_3P3 × 0.8		VDDA_3P3	V	
Low Level		0		VDDA_3P3 × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDDA_3P3 × 0.8			V	
Low Level				VDDA_3P3 × 0.2	V	
Drive Capability			4		mA	
DIGITAL SPECIFICATIONS, LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS)						
Logic Inputs (SYSREF_IN±, SYNCINx±)						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled
SPI TIMING						See the UG-1295 for more information
SCLK Period	t_{CP}	20			ns	
SCLK Pulse Width	t_{MP}	10			ns	
$\overline{CS}$ Setup to First SCLK Rising Edge	t_{SC}	3			ns	
Last SCLK Falling Edge to $\overline{CS}$ Hold	t_{HC}	0			ns	
SDIO Data Input Setup to SCLK	t_S	2			ns	
SDIO Data Input Hold to SCLK	t_H	0			ns	
SCLK Rising Edge to Output Data Delay (3-Wire Mode or 4-Wire Mode)	t_{CO}	3		8	ns	
Bus Turnaround Time, Read After Baseband Processor (BBP) Drives Last Address Bit	t_{HZM}	t_H		t_{CO}	ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Bus Turnaround Time, Read After ADRV9008-1 Drives Last Data Bit	t_{HZS}	0		t_{CO}	ns	
JESD204B DATA OUTPUT TIMING						AC-coupled
Unit Interval	UI	81.38		320	ps	
Data Rate Per Channel (NRZ)		3125		12288	Mbps	
Rise Time	t_R	24	39.5		ps	20% to 80% in 100 Ω load
Fall Time	t_F	24	39.4		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled
Differential Output Voltage	V_{DIFF}	360	600	770	mV	
Short-Circuit Current	I_{DSHORT}	−100		+100	mA	
Differential Termination Impedance		80	94.2	120	Ω	
Total Jitter			15.13		ps	Bit error rate (BER) = 10^{-15}
Uncorrelated Bounded High Probability Jitter	UBHPJ		0.56		ps	
Duty Cycle Distortion	DCD		0.369		ps	
SYSREF_IN± Setup Time to REF_CLK_IN±		2.5			ns	See Figure 2
SYSREF_IN± Hold Time to REF_CLK_IN±		−1.5			ns	See Figure 2
Latency	t_{LAT_FRM}					REF_CLK_IN± = 245.76 MHz
			89.4		Clock cycles	Receiver bandwidth = 200 MHz, IQ rate = 245.76 MHz, lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1
			364.18		ns	

[1] VDDA1P3 refers to all analog 1.3 V supplies, including VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_SER, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_VCO_LDO, VDDA1P3_AUX_SYNTH, and VDDA1P3_AUX_VCO_LDO.

CURRENT AND POWER CONSUMPTION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CHARACTERISTICS					
VDDA1P3[1] Analog Supply	1.267	1.3	1.33	V	
VDDD1P3_DIG Supply	1.267	1.3	1.33	V	
VDDA1P8_AN Supply	1.71	1.8	1.89	V	
VDDA1P8_BB Supply	1.71	1.8	1.89	V	
VDD_INTERFACE Supply	1.71	1.8	2.625	V	CMOS and LVDS supply, 1.8 V to 2.5 V nominal range
VDDA_3P3 Supply	3.135	3.3	3.465	V	
POSITIVE SUPPLY CURRENT					LO at 2600 MHz
200 MHz Receiver Bandwidth					Two receivers enabled
VDDA1P3[1] Analog Supply		1645		mA	
VDDD1P3_DIG Supply		984		mA	Receiver QEC active
VDDA1P8_AN Supply		0.4		mA	
VDDA1P8_BB Supply		68		mA	
VDD_INTERFACE Supply		8		mA	
VDDA_3P3 Supply		3		mA	No Auxiliary DAC x or AUXADC_x enabled (if enabled, AUXADC_x adds 2.7 mA, and each Auxiliary DAC x adds 1.5 mA)
Total Power Dissipation		3.57		W	Typical supply voltages, receiver QEC active

[1] VDDA1P3 refers to all analog 1.3 V supplies, including VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_SER, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_VCO_LDO, VDDA1P3_AUX_SYNTH, and VDDA1P3_AUX_VCO_LDO.

TIMING DIAGRAMS

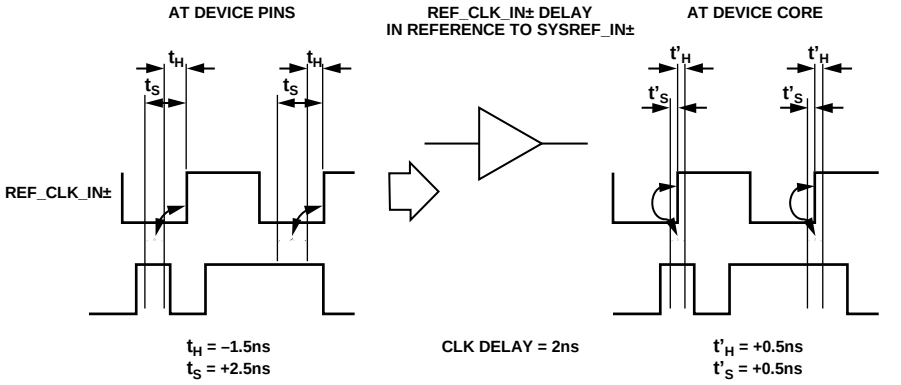


Figure 2. SYSREF_IN± Setup and Hold Timing

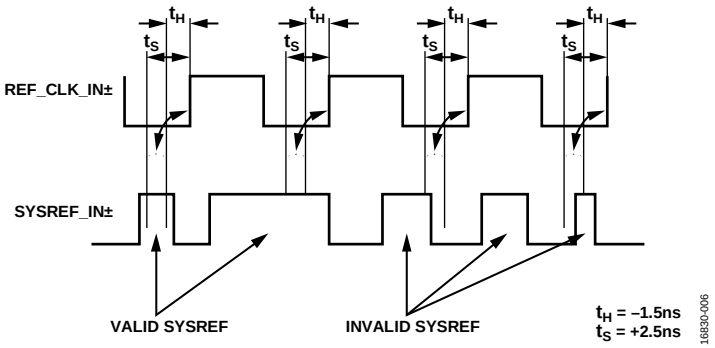


Figure 3. SYSREF_IN± Setup and Hold Timing Examples, Relative to Device Clock

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDDA1P3[1] to VSSA	−0.3 V to +1.4 V
VDDD1P3_DIG to VSSD	−0.3 V to +1.4 V
VDD_INTERFACE to VSSA	−0.3 V to +3.0 V
VDDA_3P3 to VSSA	−0.3 V to +3.9 V
VDD_INTERFACE Logic Inputs and Outputs to VSSD	−0.3 V to VDD_INTERFACE + 0.3 V
JESD204B Logic Outputs to VSSA	−0.3 V to VDDA1P3_SER
Input Current to Any Pin Except Supplies	±10 mA
Maximum Input Power into RF Port	23 dBm (peak)
Maximum Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C

[1] VDDA1P3 refers to all analog 1.3 V supplies, including VDDA1P3_RF_SYNTH, VDDA1P3_BB, VDDA1P3_RX_RF, VDDA1P3_RX, VDDA1P3_RF_VCO_LDO, VDDA1P3_RF_LO, VDDA1P3_CLOCK_SYNTH, VDDA1P3_CLOCK_SYNTH, and VDDA1P3_CLOCK_VCO_LDO.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The ADRV9008-1 reflow profile is in accordance with the JEDEC JESD204B criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL MANAGEMENT

The ADRV9008-1 is a high power device that can dissipate over 3 W depending on the user application and configuration. Because of the power dissipation, the ADRV9008-1 uses an exposed die package to provide the customer with the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly. Figure 4 shows the profile view of the device mounted to a user printed circuit board (PCB) and a heat sink (typically the aluminum case) to keep the junction (exposed die) below the maximum junction temperature shown in Table 3. The device is designed for a lifetime of 10 years when operating at the maximum junction temperature.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance data for the ADRV9008-1 mounted on both a JEDEC 2S2P test board and a 10-layer Analog Devices, Inc., evaluation board is listed in Table 4. Do not exceed the absolute maximum junction temperature rating in Table 3. Ten-layer PCB entries refer to the 10-layer Analog Devices evaluation board, which more accurately reflects the PCB used in customer applications.

Table 4. Thermal Resistance[1, 2]

Package Type	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-196-13	21.1	0.04	4.9	0.3	4.9	°C/W

[1] For the θ_{JC} test, 100 µm thermal interface material (TIM) is used. TIM is assumed to have 3.6 thermal conductivity watts/(meter × Kelvin).
[2] Using enhanced heat removal techniques such as PCB, heat sink, and airflow improves the thermal resistance values.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

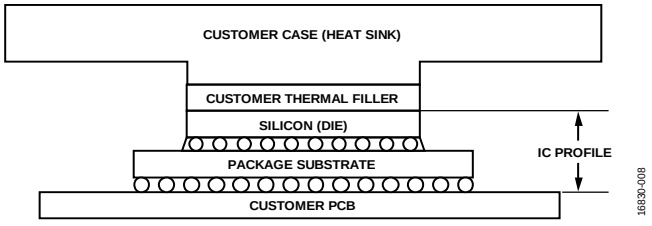


Figure 4. Typical Thermal Management Solution

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

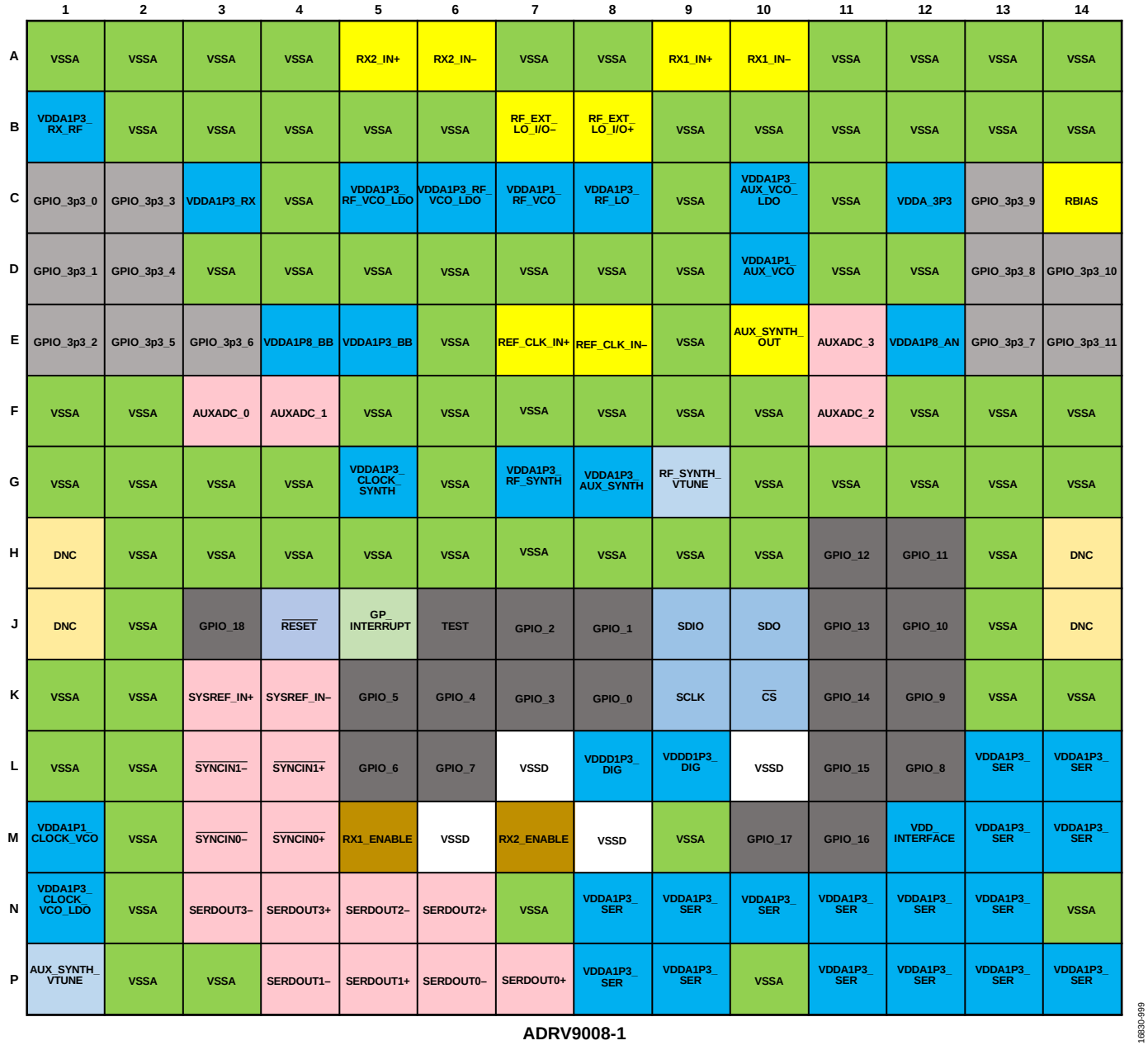


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Type	Mnemonic	Description
A1 to A4, A7, A8, A11 to A14, B2 to B6, B9 to B14, C4, C9, C11, D3 to D9, D11, D12, E6, E9, F1, F2, F5 to F10, F12 to F14, G1 to G4, G6, G10 to G14, H2 to H10, H13, J2, J13, K1, K2, K13, K14, L1, L2, M2, M9, N2, N7, N14, P2, P3, P10	Input	VSSA	Analog Supply Voltage (V_{SS}).

Pin No.	Type	Mnemonic	Description
A5, A6	Input	RX2_IN+, RX2_IN−	Differential Input for Receiver 1. When unused, connect these pins to ground.
A9, A10	Input	RX1_IN+, RX1_IN−	Differential Input for Receiver 2. When unused, connect these pins to ground.
B1	Input	VDDA1P3_RX_RF	Receiver Mixer Supply.
B7, B8	Input	RF_EXT_LO_I/O−, RF_EXT_LO_I/O+	Differential External LO Input/Output. If these pins are used for external LO, the input frequency must be 2× the desired carrier frequency. When unused, do not connect these pins.
C1	Input/ output	GPIO_3p3_0	GPIO Pin Referenced to 3.3 V Supply. The alternate function is Auxiliary DAC 4. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
C2	Input/ output	GPIO_3p3_3	GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
C3	Input	VDDA1P3_RX	1.3 V Supply for Receiver Baseband Circuits, Transimpedance Amplifier (TIA), Baseband Filters, and Auxiliary DACs.
C5, C6	Input	VDDA1P3_RF_VCO_LDO	RF VCO Low Dropout (LDO) Supply Inputs. Connect Pin C5 to Pin C6. Use a separate trace to a common supply point.
C7	Input	VDDA1P1_RF_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF.
C8	Input	VDDA1P3_RF_LO	1.3 V LO Generator for RF Synthesizer. This pin is sensitive to aggressors.
C10	Input	VDDA1P3_AUX_VCO_LDO	1.3 V Supply.
C12	Input	VDDA_3P3	General-Purpose Output Pull-Up Voltage and Auxiliary DAC Supply Voltage.
C13	Input/ output	GPIO_3p3_9	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 9. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
C14	Input/ output	RBIAS	Bias Resistor. Tie this pin to ground using a 14.3 kΩ resistor. This pin generates an internal current based on an external 1% resistor.
D1	Input/ output	GPIO_3p3_1	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 5. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
D2	Input/ output	GPIO_3p3_4	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 6. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
D10	Input	VDDA1P1_AUX_VCO	1.1 V VCO Supply. Decouple with 1 µF.
D13	Input/ output	GPIO_3p3_8	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.

Pin No.	Type	Mnemonic	Description
D14	Input/ output	GPIO_3p3_10	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
E1	Input/ output	GPIO_3p3_2	GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
E2	Input/ output	GPIO_3p3_5	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 7. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
E3	Input/ output	GPIO_3p3_6	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 8. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
E4	Input	VDDA1P8_BB	1.8 V Supply for the ADC and DAC.
E5	Input	VDDA1P3_BB	1.3 V Supply for the ADC, DAC, and Auxiliary ADCs.
E7, E8	Input	REF_CLK_IN+, REF_CLK_IN–	Device Clock Differential Input.
E10	Output	AUX_SYNTH_OUT	Auxiliary PLL Output. When unused, do not connect this pin.
E11, F3, F4, F11	Input	AUXADC_0 to AUXADC_3	Auxiliary ADC Input. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
E12	Input	VDDA1P8_AN	1.8 V Bias Supply for Analog Circuitry.
E13	Input/ output	GPIO_3p3_7	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 2. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as an output, and driven low.
E14	Input/ output	GPIO_3p3_11	GPIO Pin Referenced to 3.3 V Supply. The alternative function is Auxiliary DAC 3. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or this pin can be left floating, programmed as outputs, and driven low.
G5	Input	VDDA1P3_CLOCK_SYNTH	1.3 V Supply Input for Clock Synthesizer. Use a separate trace on the PCB back to a common supply point.
G7	Input	VDDA1P3_RF_SYNTH	1.3 V RF Synthesizer Supply Input. This pin is sensitive to aggressors.
G8	Input	VDDA1P3_AUX_SYNTH	1.3 V Auxiliary Synthesizer Supply Input.
G9	Output	RF_SYNTH_VTUNE	RF Synthesizer V_{TUNE} Output.
H1, J1, H14, J14	DNC[1]	DNC	Do Not Connect. Do not connect these pins.
H11	Input/ output	GPIO_12	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
H12	Input/ output	GPIO_11	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.

Pin No.	Type	Mnemonic	Description
J3	Input/ output	GPIO_18	Digital GPIO, 1.8 V to 2.5 V. The joint test action group (JTAG) function is test clock (TCLK). Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
J4	Input	$\overline{\text{RESET}}$	Active Low Chip Reset.
J5	Output	GP_INTERRUPT	General-Purpose Digital Interrupt Output Signal. When unused, do not connect this pin.
J6	Input	TEST	Pin Used for JTAG Boundary Scan. When unused, connect this pin to ground.
J7	Input/ output	GPIO_2	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
J8	Input/ output	GPIO_1	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
J9	Input/ output	SDIO	Serial Data Input in 4-Wire Mode or Input/Output in 3-Wire Mode.
J10	Output	SDO	Serial Data Output. In SPI 3-Wire mode, do not connect this pin.
J11	Input/ output	GPIO_13	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
J12	Input/ output	GPIO_10	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
K3, K4	Input	SYSREF_IN+, SYSREF_IN−	LVDS Input.
K5	Input/ output	GPIO_5	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is test data output (TDO). Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
K6	Input/ output	GPIO_4	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is test rest ($\overline{\text{TRST}}$). Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
K7	Input/ output	GPIO_3	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
K8	Input/ output	GPIO_0	Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
K9	Input	SCLK	Serial Data Bus Clock.
K10	Input	$\overline{\text{CS}}$	Serial Data Bus Chip Select, Active Low.

Pin No.	Type	Mnemonic	Description
K11	Input/ output	GPIO_14	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
K12	Input/ output	GPIO_9	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
L3, L4	Input	$\overline{\text{SYNCIN1}}$–, $\overline{\text{SYNCIN1}}$+	LVDS Input. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
L5	Input/ output	GPIO_6	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is test data input (TDI). Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
L6	Input/ output	GPIO_7	Digital GPIO, 1.8 V to 2.5 V. The JTAG function is test mode select input (TMS). Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
L7, L10, M6, M8	Input	VSSD	Digital V_{SS}.
L8, L9	Input	VDDD1P3_DIG	1.3 V Digital Core. Connect Pin L8 to Pin L9. Use a separate trace to a common supply point.
L11	Input/ output	GPIO_15	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
L12	Input/ output	GPIO_8	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
L13, L14, M13, M14, N8 to N13, P8, P9, P11 to P14	Input	VDDA1P3_SER	1.3 V Supply for JESD204B Serializer.
M1	Input	VDDA1P1_CLOCK_VCO	1.1 V VCO Supply. Decouple this pin with 1 µF.
M3, M4	Input	$\overline{\text{SYNCIN0}}$–, $\overline{\text{SYNCIN0}}$+	JESD204B Receiver Channel 0. These pins form the synchronization signal associated with receiver channel data on the JESD204B interface. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.
M5	Input	RX1_ENABLE	Receiver 1 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect directly to ground.
M7	Input	RX2_ENABLE	Receiver 2 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect directly to ground.
M10	Input/ output	GPIO_17	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
M11	Input/ output	GPIO_16	Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor to safeguard against misconfiguration, or it can be left floating, programmed as an output, and driven low.
M12	Input	VDD_INTERFACE	Input/Output Interface Supply, 1.8 V to 2.5 V.
N1	Input	VDDA1P3_CLOCK_VCO_LDO	1.3 V Supply. Use a separate trace to a common supply point.

Pin No.	Type	Mnemonic	Description
N3, N4	Output	SERDOUT3−, SERDOUT3+	RF Current Mode Logic (CML) Differential Output 3. When unused, do not connect these pins.
N5, N6	Output	SERDOUT2−, SERDOUT2+	RF CML Differential Output 2. When unused, do not connect these pins.
P1	Output	AUX_SYNTH_VTUNE	Auxiliary Synthesizer V_{TUNE} Output.
P4, P5	Output	SERDOUT1−, SERDOUT1+	RF CML Differential Output 1. When unused, do not connect these pins.
P6, P7	Output	SERDOUT0−, SERDOUT0+	RF CML Differential Output 0. When unused, do not connect these pins.

[1] DNC means do not connect.

TYPICAL PERFORMANCE CHARACTERISTICS

The temperature settings refer to the die temperature.

75 MHz TO 525 MHz BAND

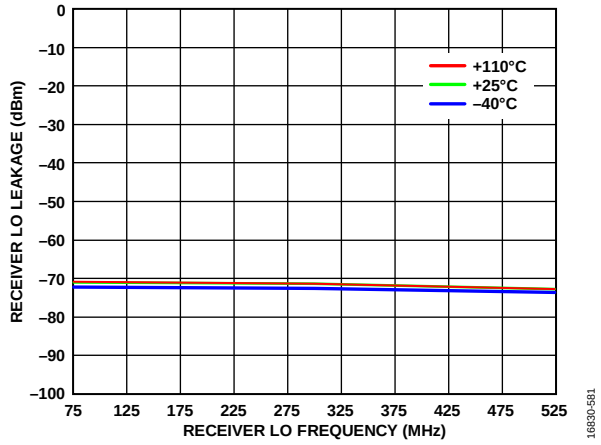


Figure 6. Receiver LO Leakage vs. Receiver LO Frequency, 75 MHz, 300 MHz, 525 MHz; Receiver Attenuation = 0 dB, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS

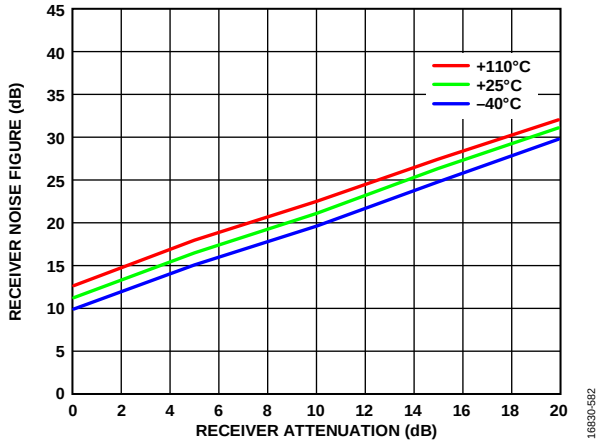


Figure 7. Receiver Noise Figure vs. Receiver Attenuation, LO = 75 MHz, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = 1 MHz to 25 MHz

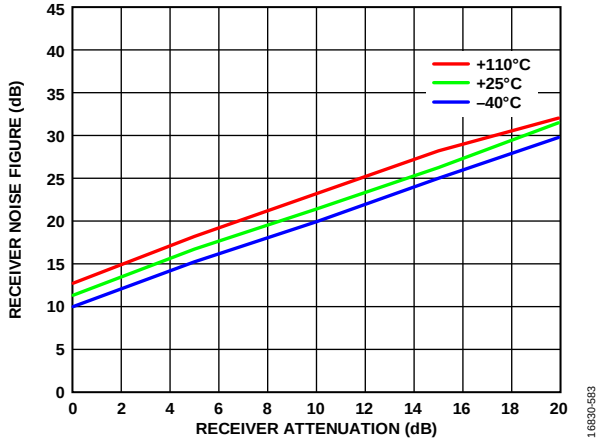


Figure 8. Receiver Noise Figure vs. Receiver Attenuation, LO = 300 MHz, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = 1 MHz to 25 MHz

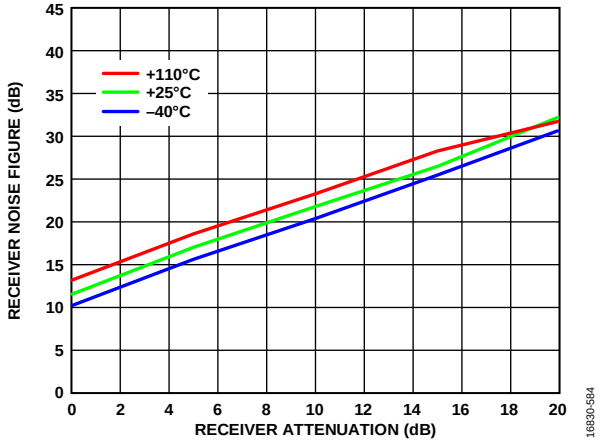


Figure 9. Receiver Noise Figure vs. Receiver Attenuation, LO = 525 MHz, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = 1 MHz to 25 MHz

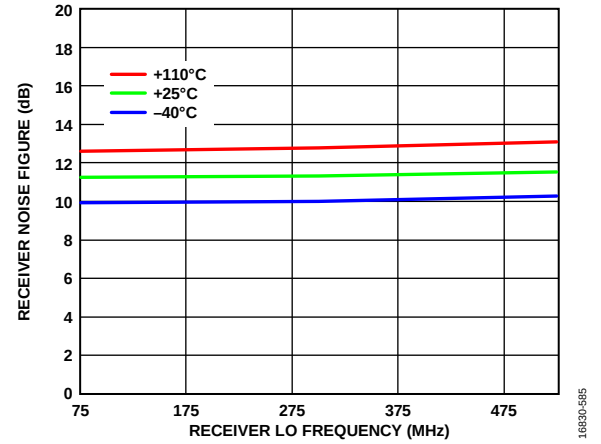


Figure 10. Receiver Noise Figure vs. Receiver LO Frequency, Receiver Attenuation = 0 dB, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = ±25 MHz

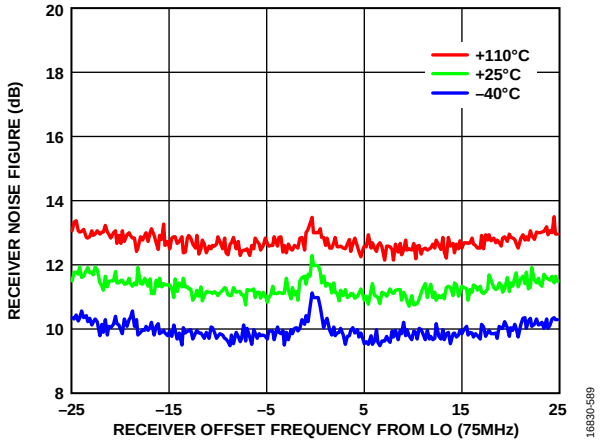


Figure 11. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 75 MHz

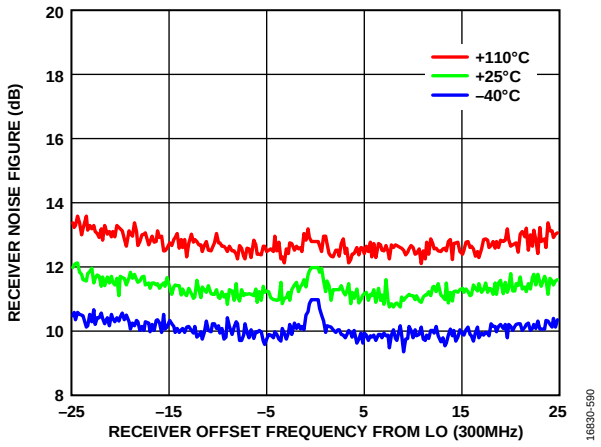


Figure 12. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 300 MHz

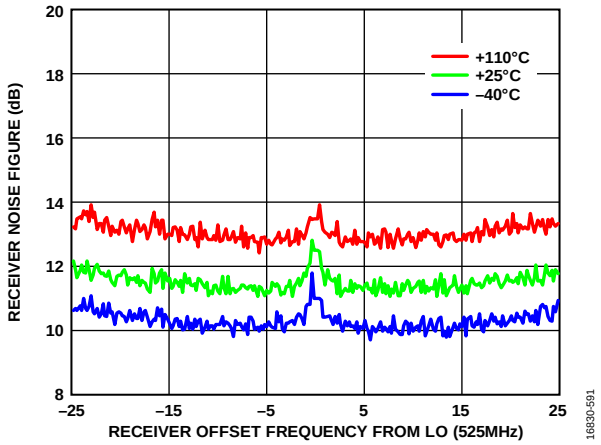


Figure 13. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 525 MHz

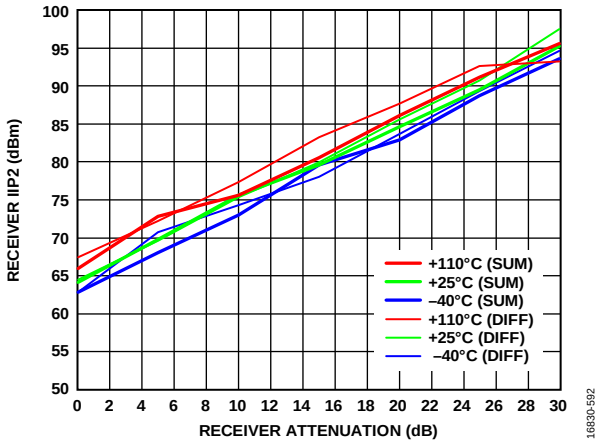


Figure 14. Receiver IIP2 vs. Receiver Attenuation, LO = 75 MHz, Tones Placed at 82.5 MHz and 83.5 MHz, −23.5 dBm Plus Attenuation

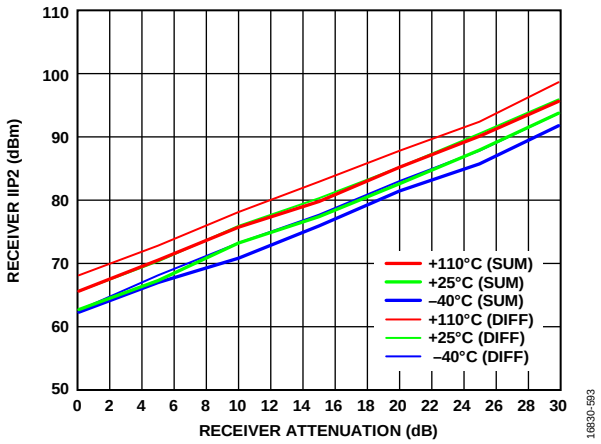


Figure 15. Receiver IIP2 vs. Receiver Attenuation, LO = 300 MHz, Tones Placed at 310 MHz and 311 MHz, −23.5 dBm Plus Attenuation

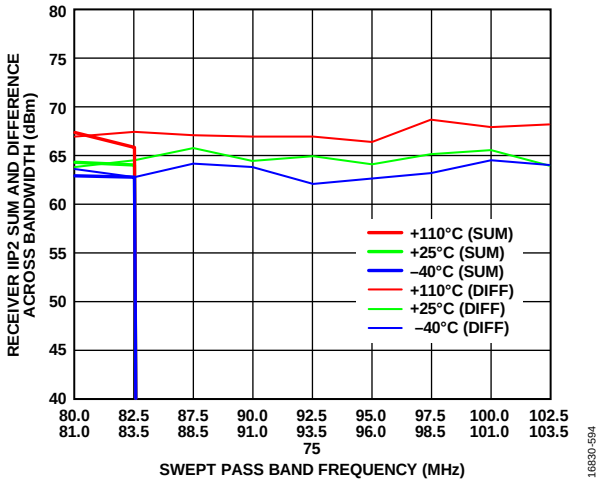


Figure 16. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 75 MHz, 10 Tone Pairs, −23.5 dBm Each

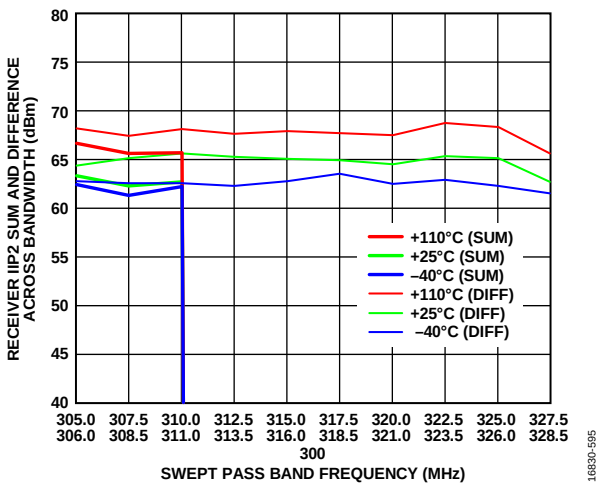


Figure 17. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 300 MHz, 10 Tone pairs, −23.5 dBm Each

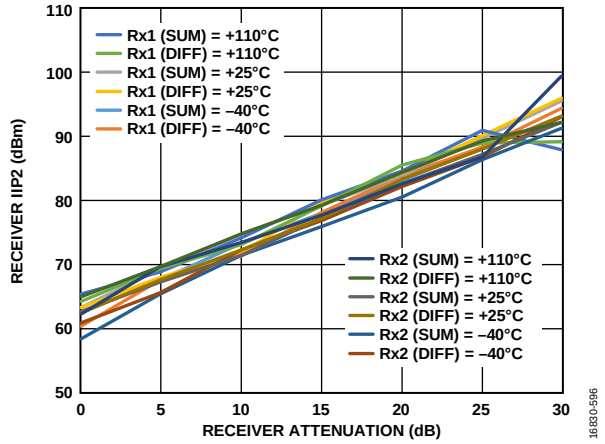


Figure 18. Receiver IIP2 vs. Receiver Attenuation, LO = 75 MHz, Tones Placed at 77 MHz and 97 MHz, –23.5 dBm Plus Attenuation

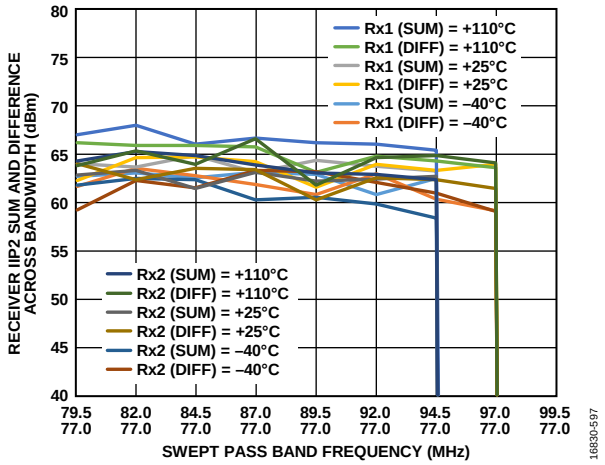


Figure 19. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 75 MHz, Tone 1 = 77 MHz, Tone 2 Swept, –23.5 dBm Each

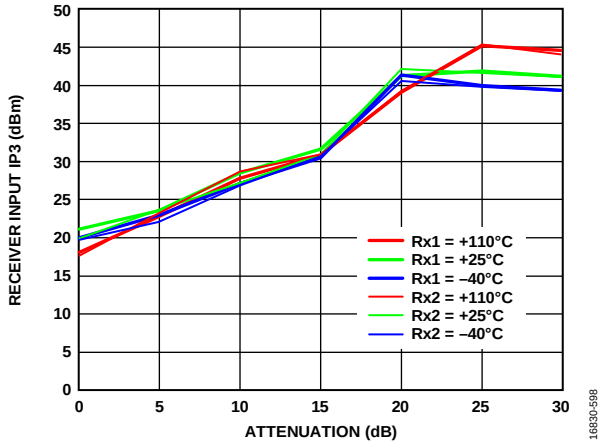


Figure 20. Receiver IIP3 vs. Attenuation, LO = 300 MHz, Tone 1 = 325 MHz, Tone 2 = 326 MHz, –21 dBm Plus Attenuation

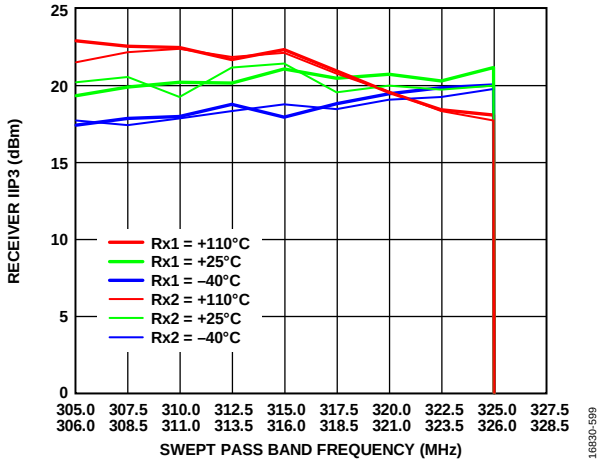


Figure 21. Receiver IIP3, Receiver Attenuation = 0 dB, LO = 300 MHz, Tone 2 = Tone 1 + 1 MHz, –21 dBm Each, Swept Across Pass Band

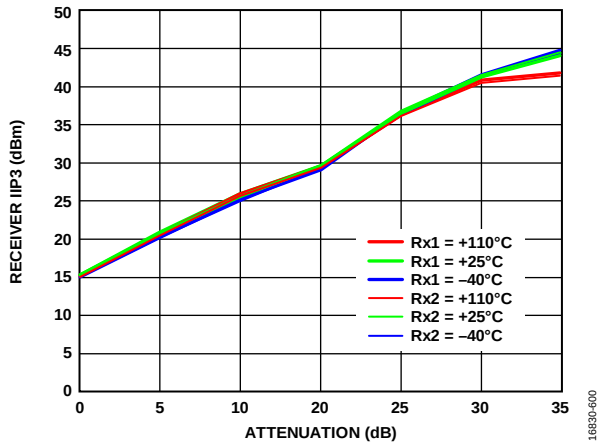


Figure 22. Receiver IIP3 vs. Attenuation, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = 322 MHz, –19 dBm Plus Attenuation

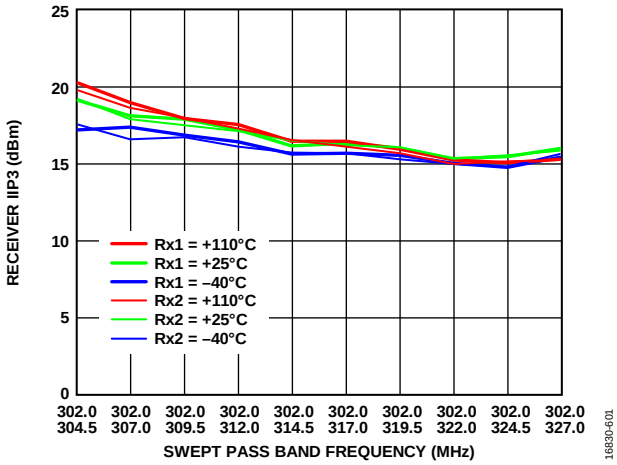


Figure 23. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 Swept Across Pass Band, –19 dBm Each

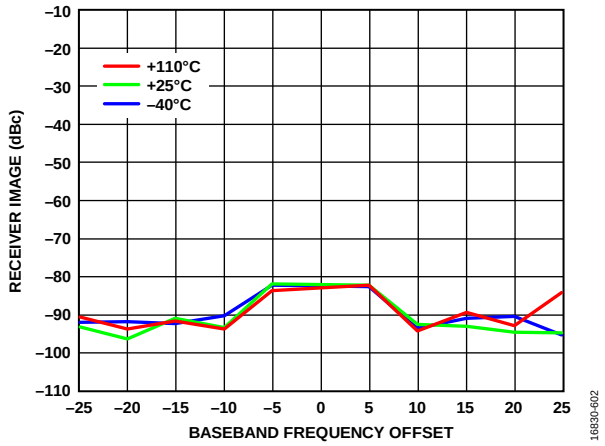


Figure 24. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 50 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 75 MHz

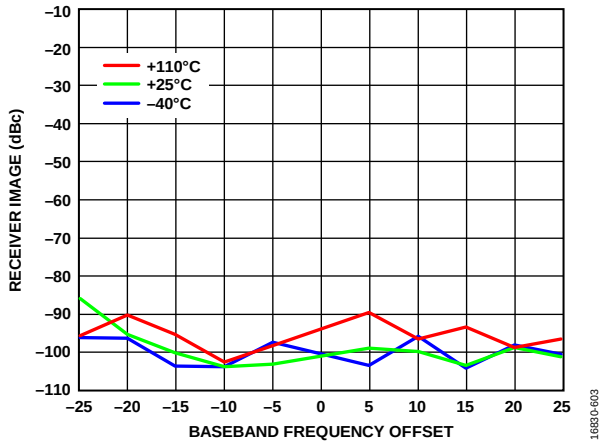


Figure 25. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 50 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 300 MHz

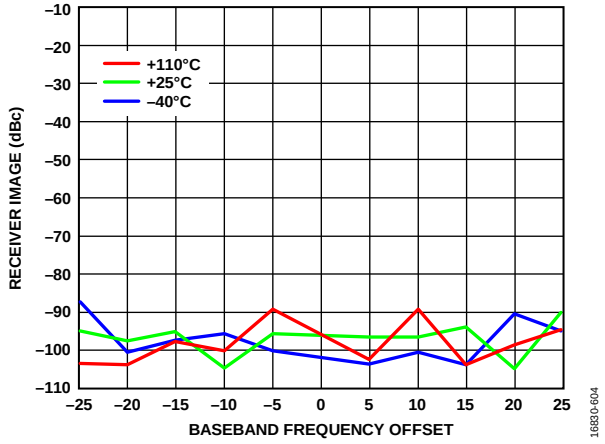


Figure 26. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 50 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 525 MHz

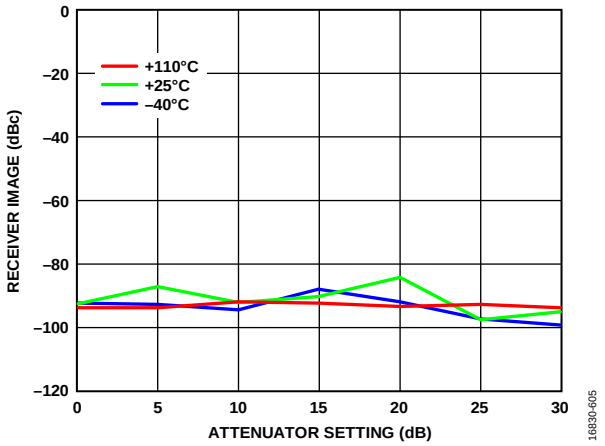


Figure 27. Receiver Image vs. Attenuator Setting, RF Bandwidth = 25 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 75 MHz, Baseband Frequency = 25 MHz

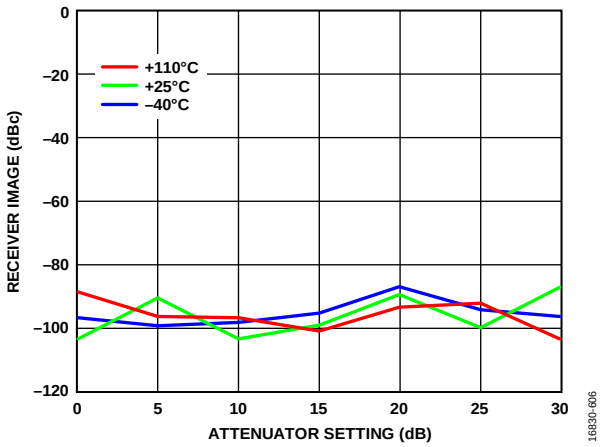


Figure 28. Receiver Image vs. Attenuator Setting, RF Bandwidth = 25 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 325 MHz, Baseband Frequency = 25 MHz

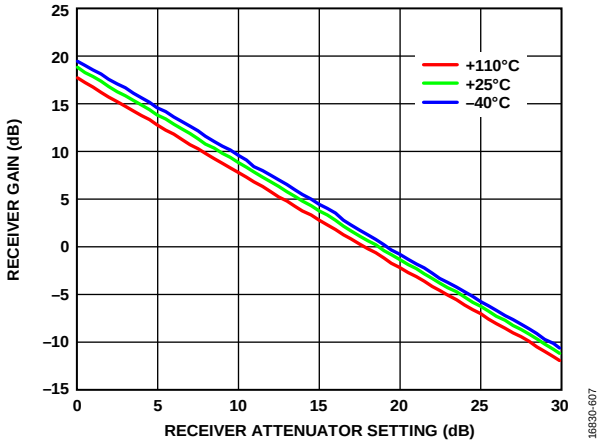


Figure 29. Receiver Gain vs. Receiver Attenuator Setting, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, LO = 75 MHz

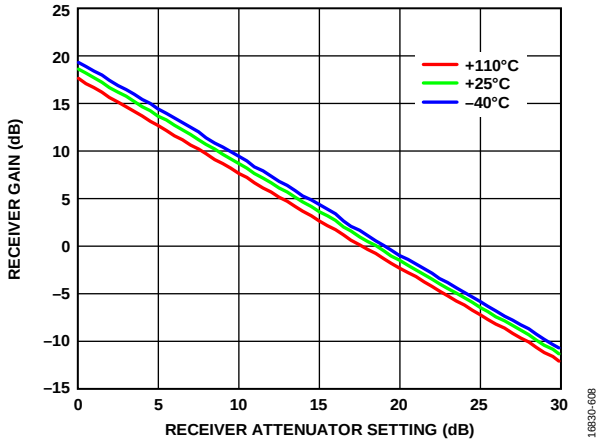


Figure 30. Receiver Gain vs. Receiver Attenuator Setting, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, LO = 325 MHz

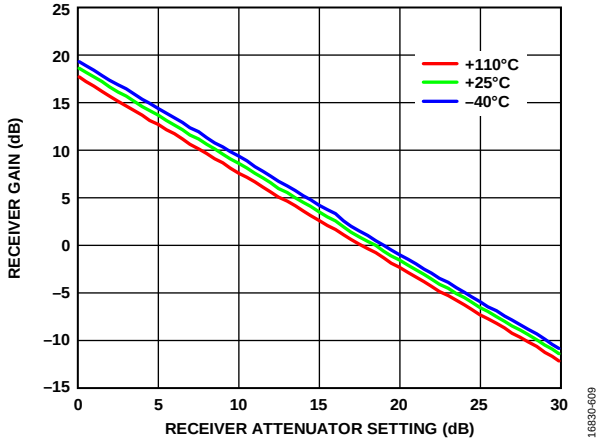


Figure 31. Receiver Gain vs. Receiver Attenuator Setting, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, LO = 525 MHz

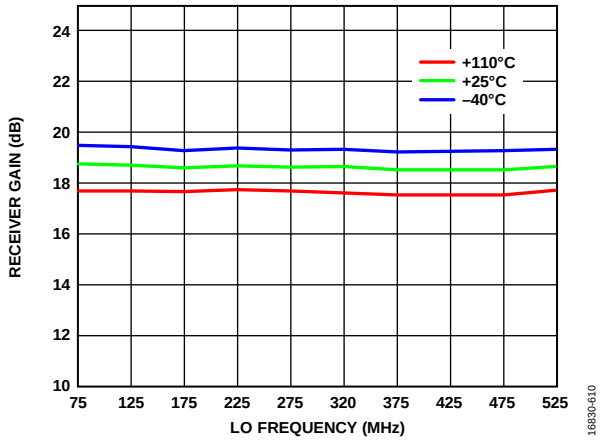


Figure 32. Receiver Gain vs. LO Frequency, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS

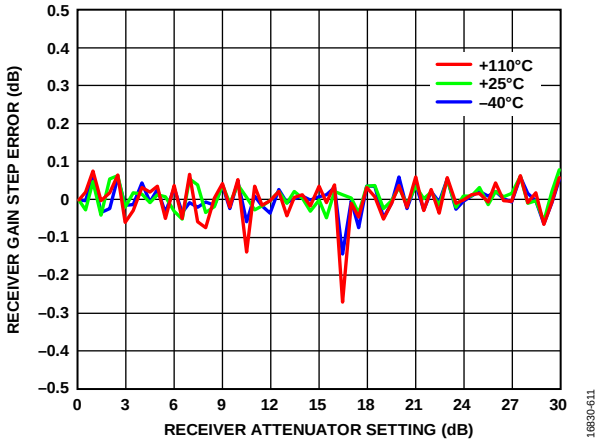


Figure 33. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 75 MHz

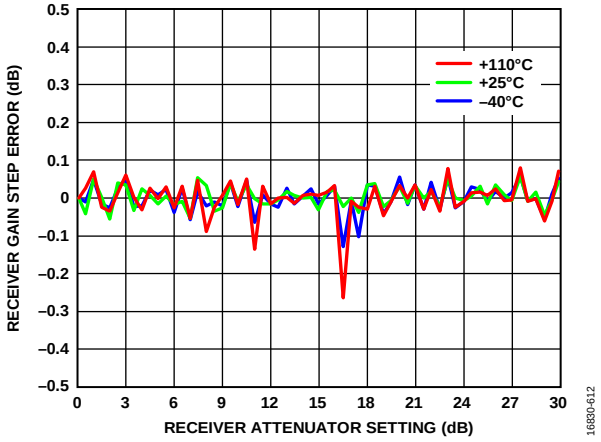


Figure 34. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 325 MHz

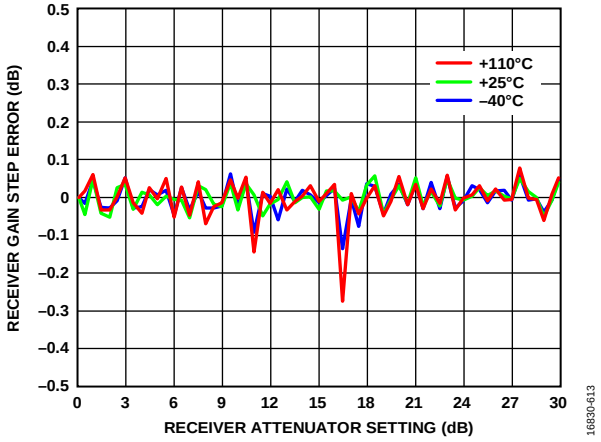


Figure 35. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 525 MHz

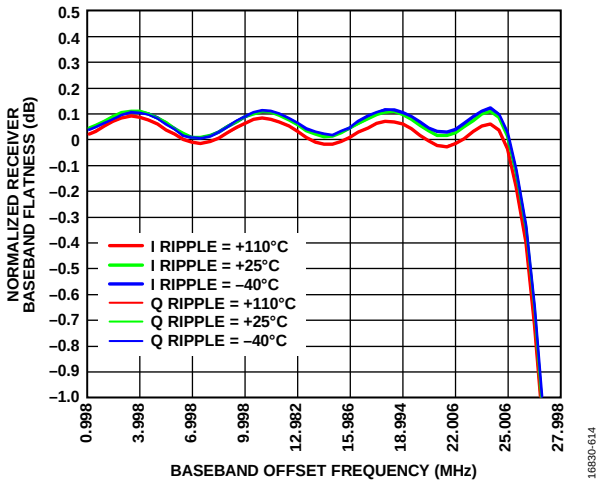


Figure 36. Normalized Receiver Baseband Flatness vs. Baseband Offset Frequency (Receiver Flatness), LO = 75 MHz

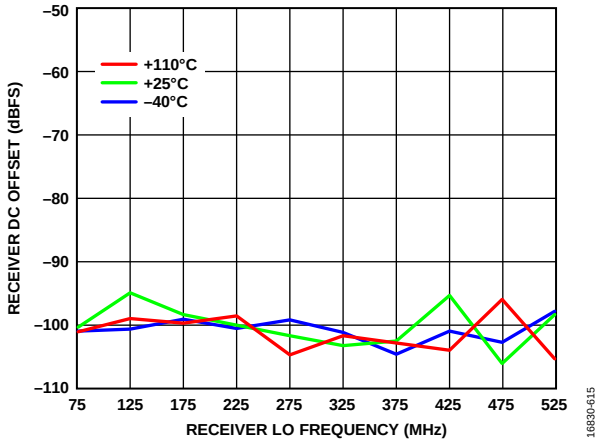


Figure 37. Receiver DC Offset vs. Receiver LO Frequency

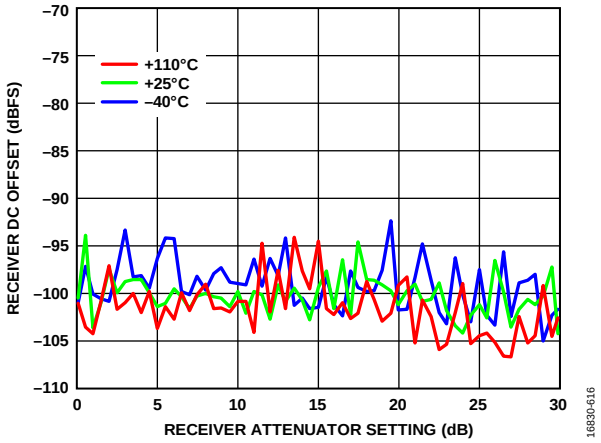


Figure 38. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 75 MHz

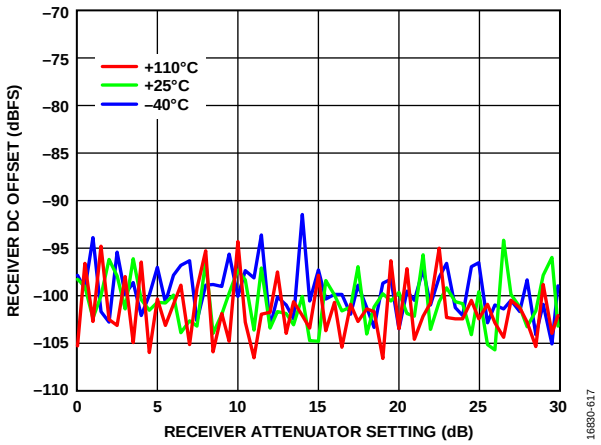


Figure 39. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 525 MHz

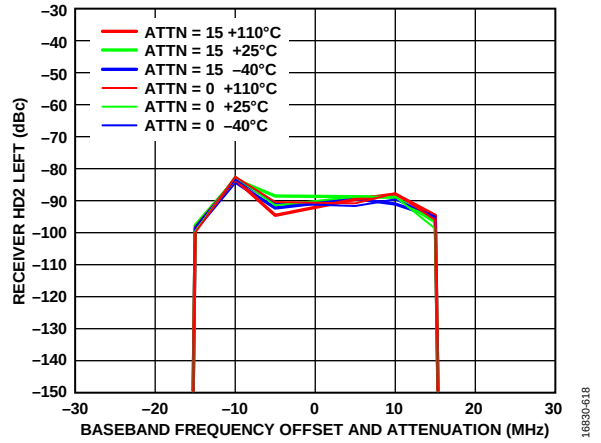


Figure 40. Receiver Second-Order Harmonic Distortion (HD2) Left vs. Baseband Frequency Offset and Attenuation, Tone Level = –21 dBm at Attenuation = 0 dB, X-Axis Is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product is 2× Baseband Frequency), HD2 Canceller Disabled, LO = 75MHz

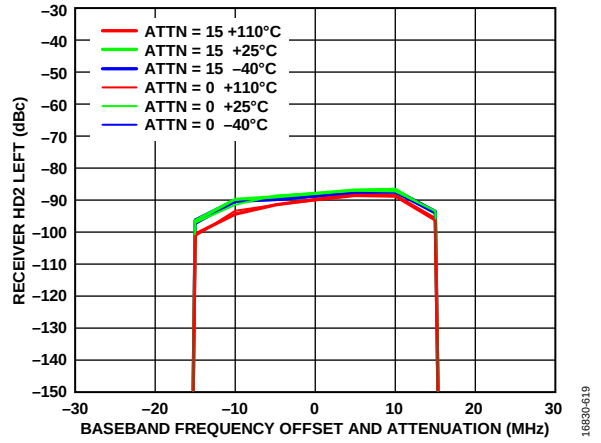


Figure 41. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation, Tone Level –21 dBm at Attenuation = 0 dB, X-Axis Is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product Is 2× Baseband Frequency), HD2 Canceller Disabled, LO = 300 MHz

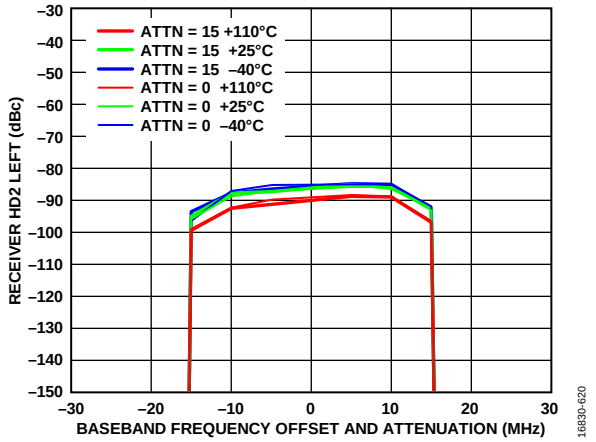


Figure 42. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation, Tone Level –21 dBm at Attenuation = 0 dB, X-Axis Is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product Is 2× Baseband Frequency), HD2 Canceller Disabled, LO = 525 MHz

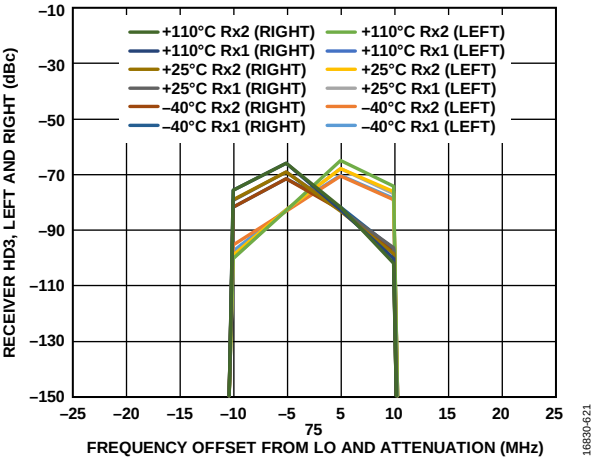


Figure 43. Receiver HD3, Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level = –16 dBm at Attenuation = 0 dB, LO = 75 MHz

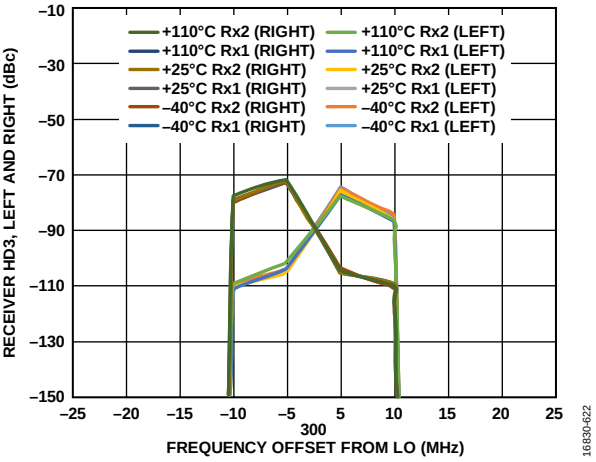


Figure 44. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level –17 dBm at Attenuation = 0 dB, LO = 300 MHz

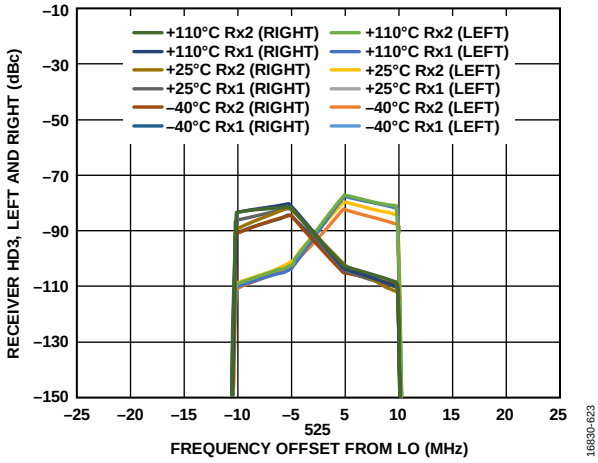


Figure 45. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level –17 dBm at Attenuation = 0 dB, LO = 525 MHz

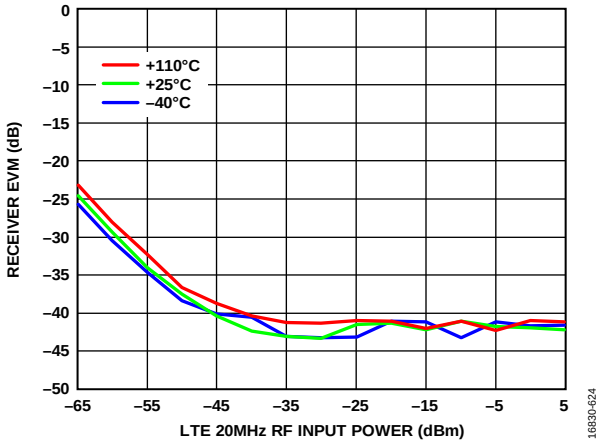


Figure 46. Receiver Error Vector Magnitude (EVM) vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 75 MHz, Default AGC Settings

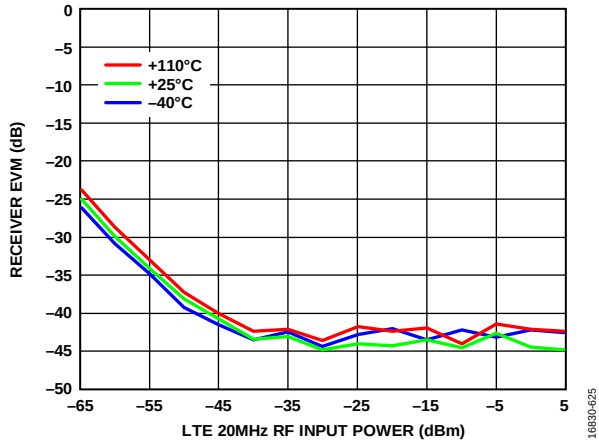


Figure 47. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 300 MHz, Default AGC Settings

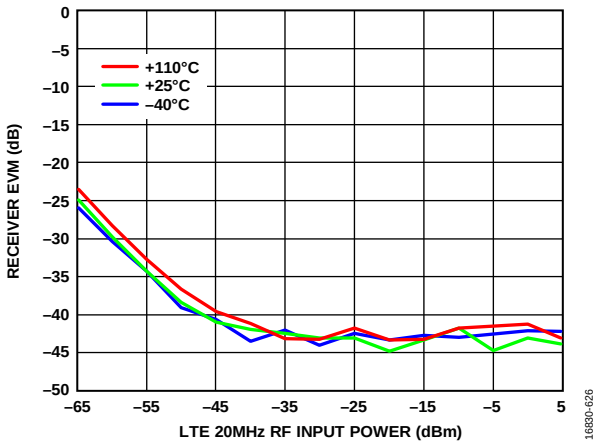


Figure 48. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 525 MHz, Default AGC Settings

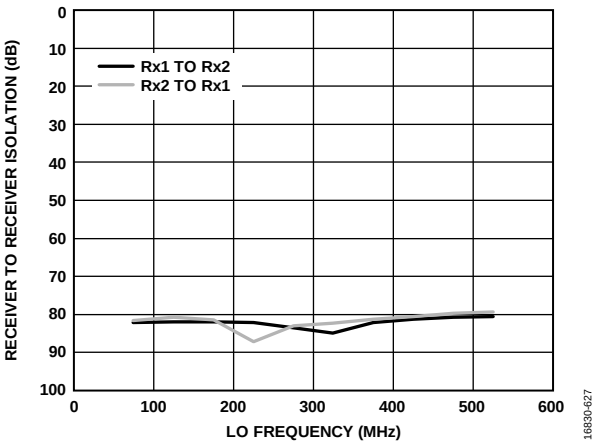


Figure 49. Receiver to Receiver Isolation vs. LO Frequency, Baseband Frequency = 10 MHz

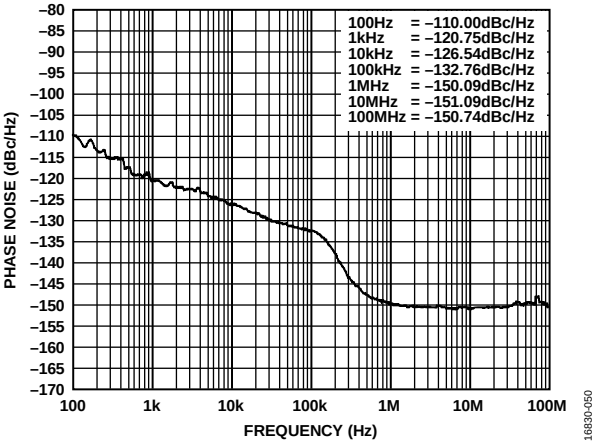


Figure 50. LO Phase Noise vs. Frequency Offset, LO = 75 MHz, PLL Loop Bandwidth = 50 kHz

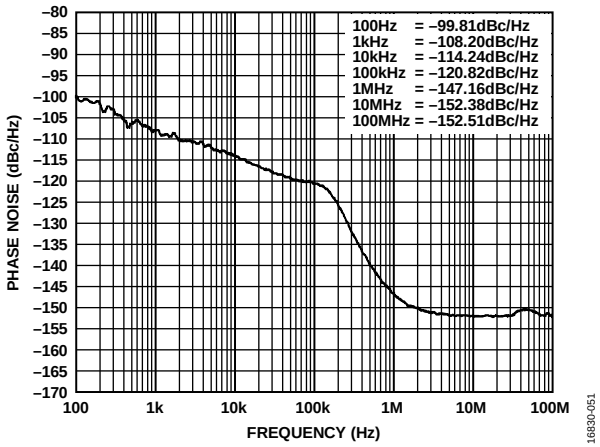


Figure 51. LO Phase Noise vs. Frequency Offset, LO = 300 MHz, PLL Loop Bandwidth = 50 kHz

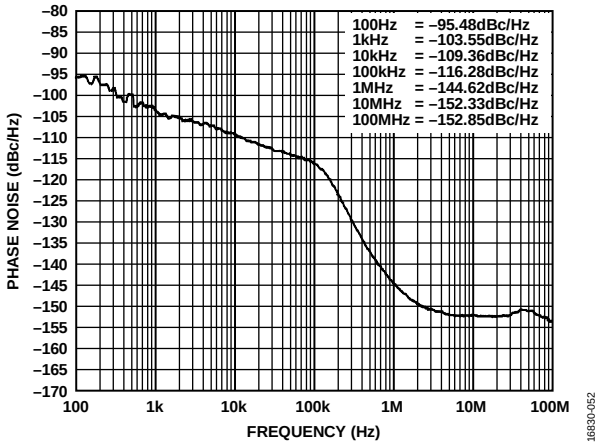


Figure 52. LO Phase Noise vs. Frequency Offset, LO = 525 MHz, PLL Loop Bandwidth = 50 kHz

650 MHz TO 3000 MHz BAND

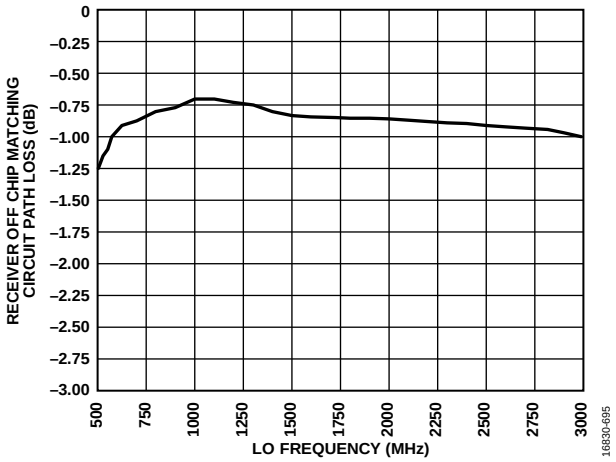


Figure 53. Receiver Off Chip Matching Circuit Path Loss vs. LO Frequency, Can Be Used for De-Embedding Performance Data

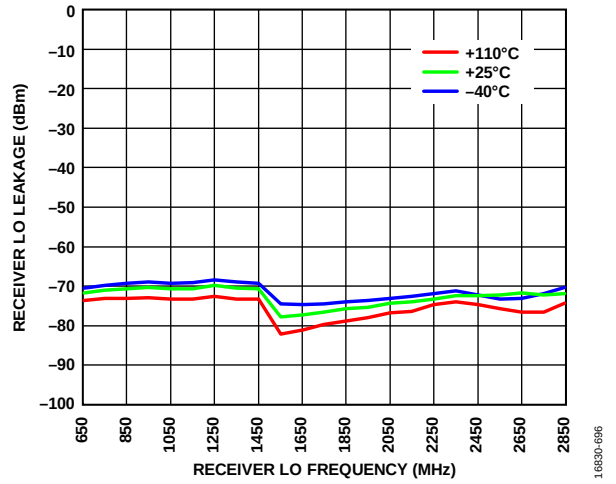


Figure 54. Receiver LO Leakage vs. Receiver LO Frequency, Receiver Attenuation = 0 dB, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS

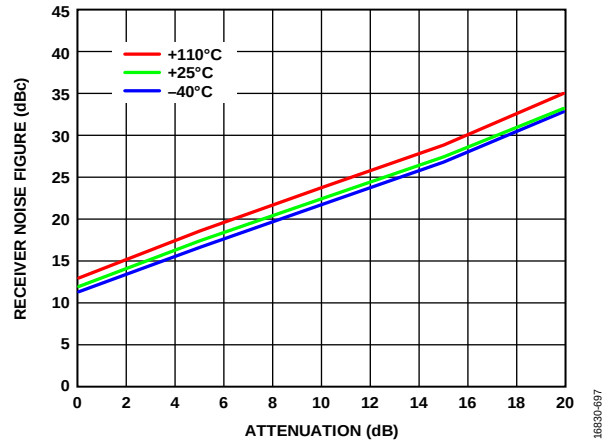


Figure 55. Receiver Noise Figure vs. Attenuation, LO = 650 MHz, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

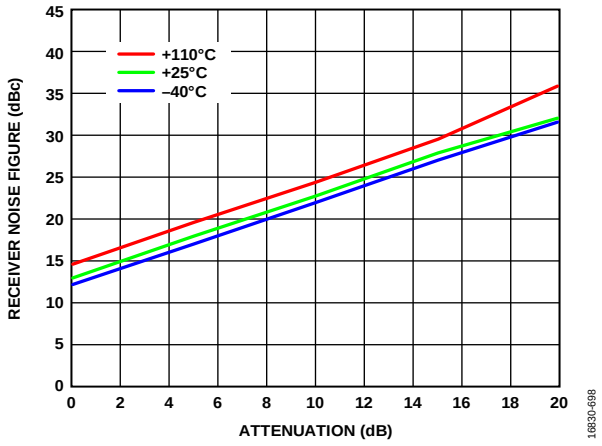


Figure 56. Receiver Noise Figure vs. Attenuation, LO = 1850 MHz, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

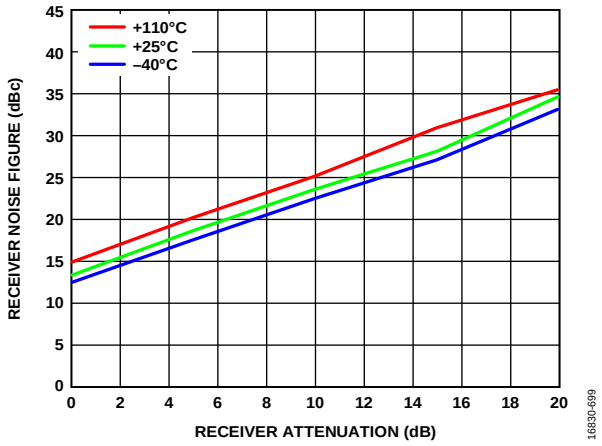


Figure 57. Receiver Noise Figure vs. Receiver Attenuation, 2850 MHz LO, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

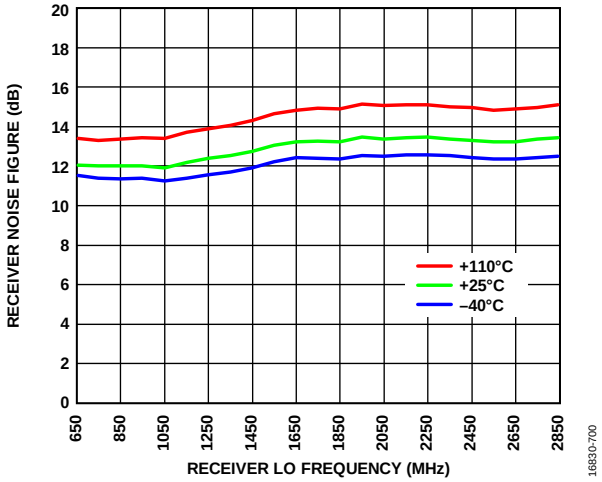


Figure 58. Receiver Noise Figure vs. Receiver LO Frequency, Receiver Attenuation = 0 dB, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth = ±100 MHz

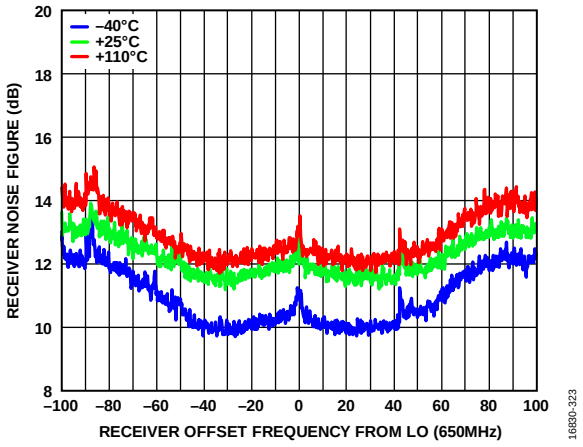


Figure 59. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 650 MHz

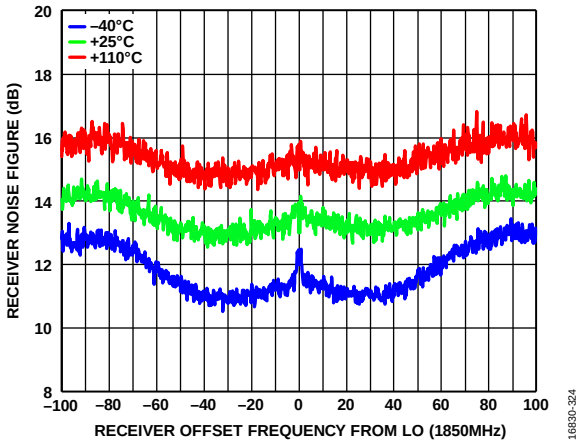


Figure 60. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 1850 MHz

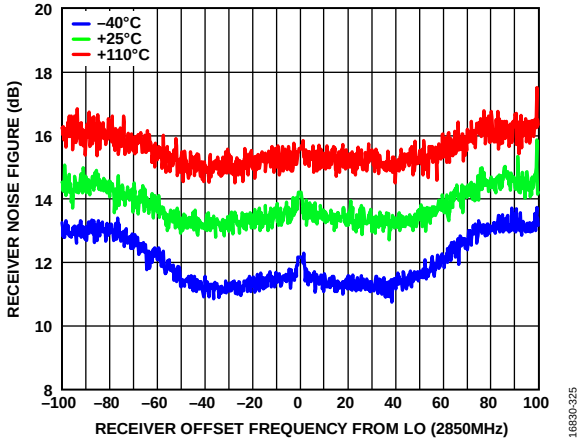


Figure 61. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 2850 MHz

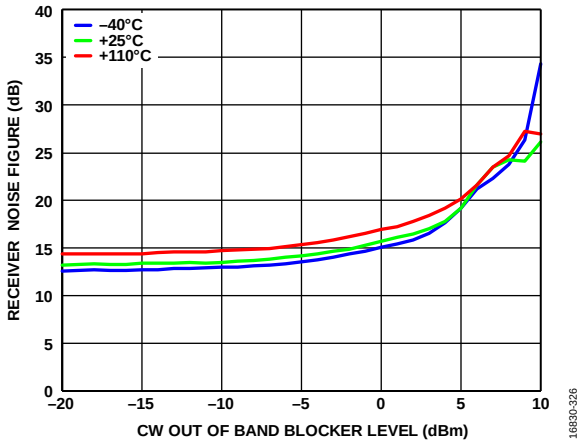


Figure 62. Receiver Noise Figure vs. CW Out of Band Blocker Level, LO = 1685 MHz, Blocker = 2085 MHz

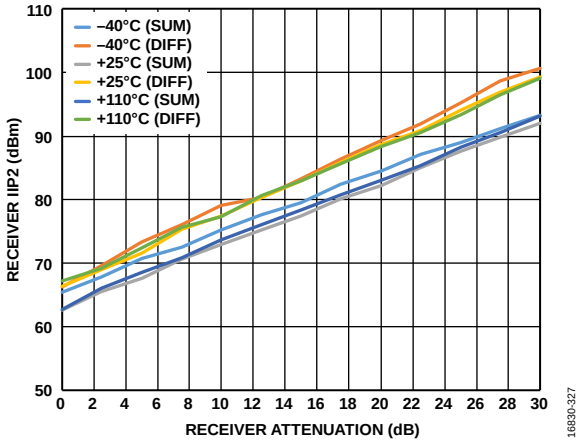


Figure 63. Receiver IIP2 vs. Receiver Attenuation, LO = 1800 MHz, Tones Placed at 1845 MHz and 1846 MHz, –21 dBm Each at Attenuation = 0 dB

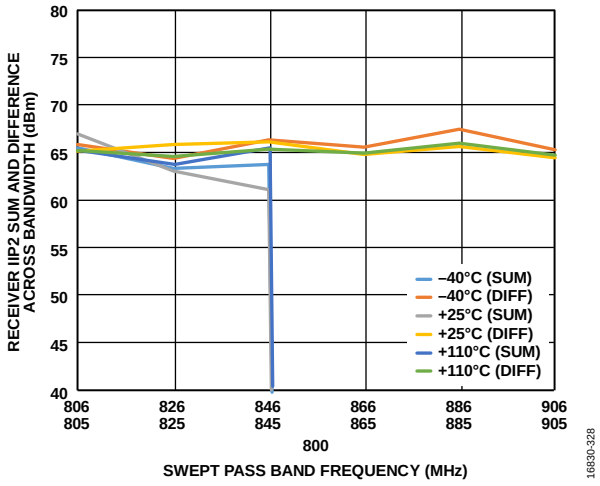


Figure 64. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 800 MHz, Six Tone Pairs, –21 dBm Each

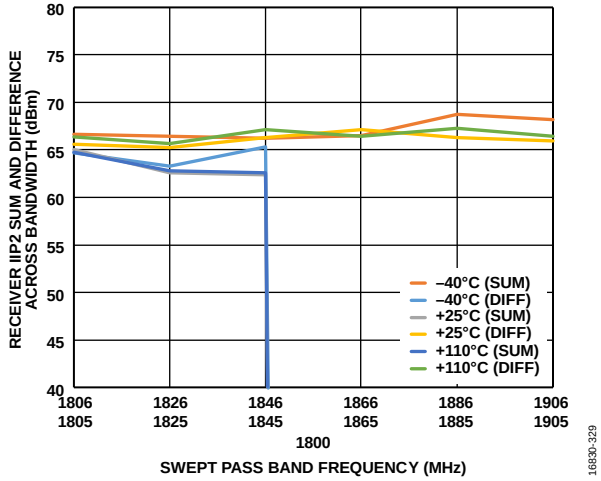


Figure 65. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 1800 MHz, Six Tone Pairs, –21 dBm Each

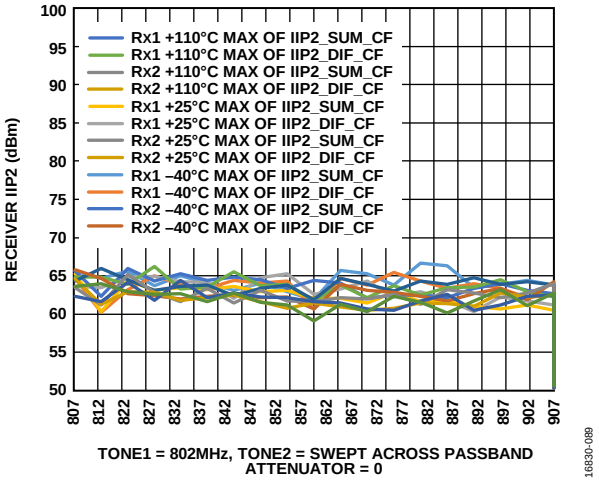


Figure 68. Receiver IIP2 Sum and Difference Across Bandwidth, Receiver Attenuation = 0 dB, LO = 800 MHz, Tone 1 = 802 MHz, Tone 2 Swept, –21 dBm Each, IIP2_SUM_CF and IIP2_DIF_CF Indicate Sum and Difference Products

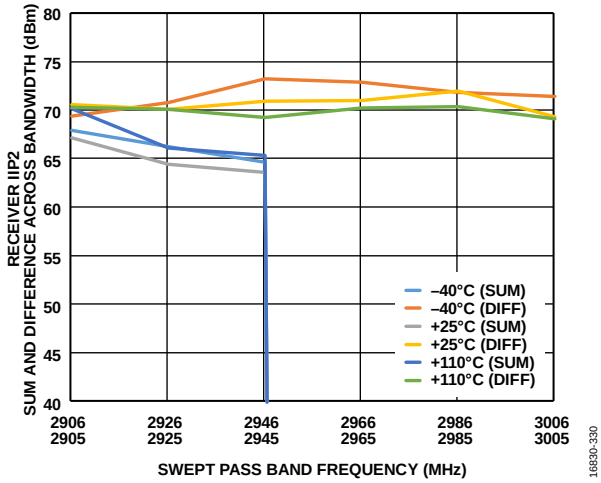


Figure 66. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 2900 MHz, Six Tone Pairs, –21 dBm Each

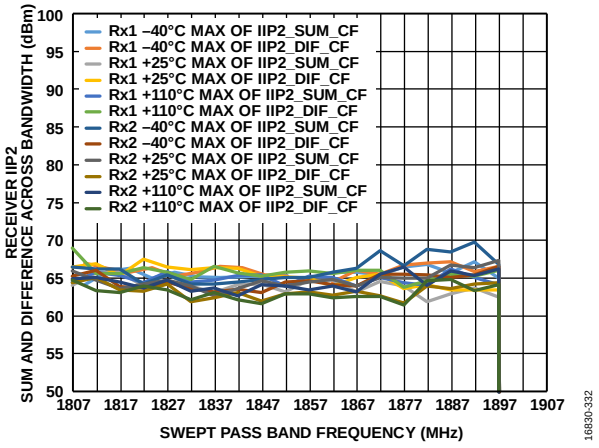


Figure 69. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 Swept, –21 dBm Each, IIP2_SUM_CF and IIP2_DIF_CF Indicate Sum and Difference Products

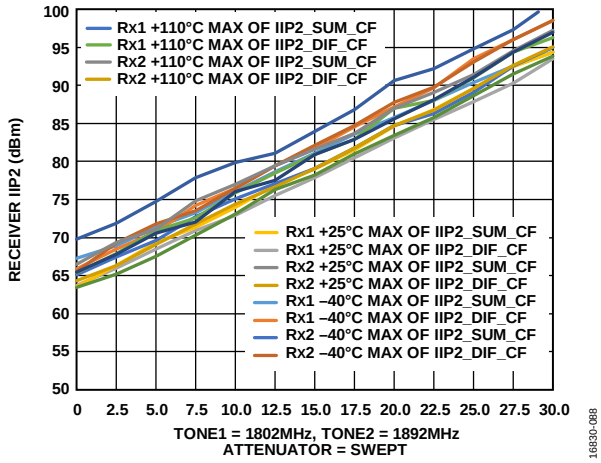


Figure 67. Receiver IIP2, LO = 1800 MHz, Tones Placed at 1802 MHz and 1892 MHz, –21 dBm Each at Attenuation = 0 dB, IIP2_SUM_CF and IIP2_DIF_CF Indicate Sum and Difference Products

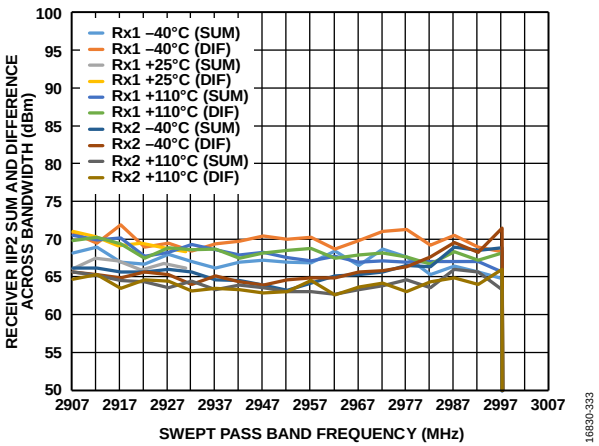


Figure 70. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 2900 MHz, Tone 1 = 2902 MHz, Tone 2 Swept, –21 dBm Each

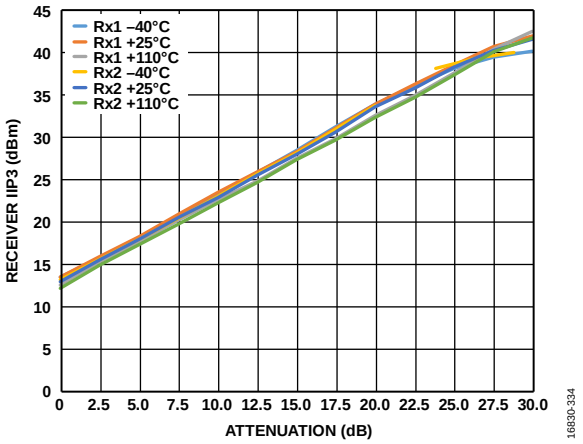


Figure 71. Receiver IIP3 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1890 MHz, Tone 2 = 1891 MHz, −21 dBm Each at Attenuation = 0 dB

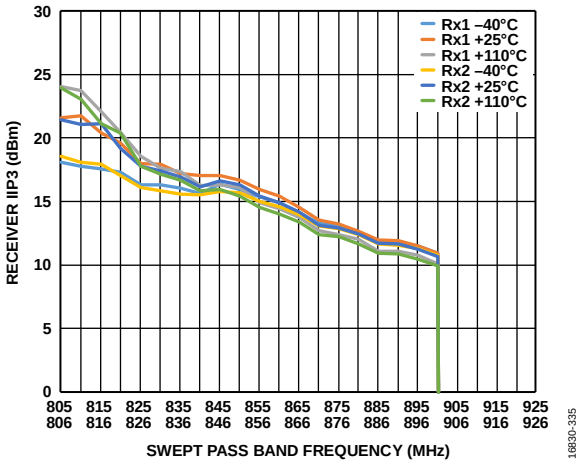


Figure 72. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 800 MHz, Tone 2 = Tone 1 + 1 MHz, −21 dBm Each, Swept Across Pass Band

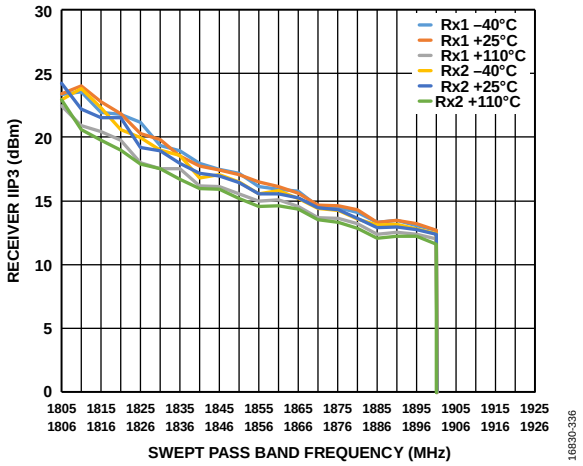


Figure 73. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 1800 MHz, Tone 2 = Tone 1 + 1 MHz, −21 dBm Each, Swept Across Pass Band

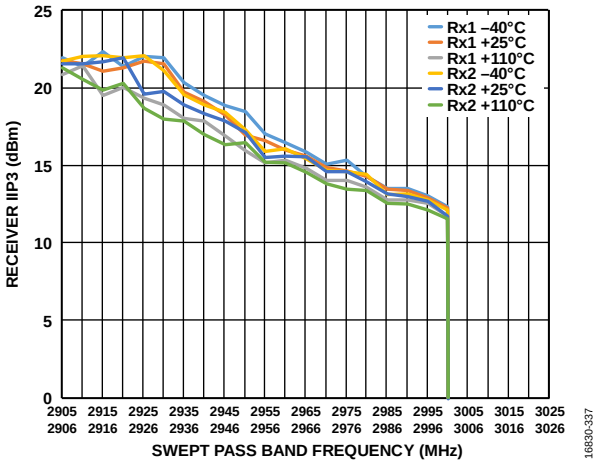


Figure 74. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 2900 MHz, Tone 2 = Tone 1 + 1 MHz, −21 dBm Each, Swept Across Pass Band

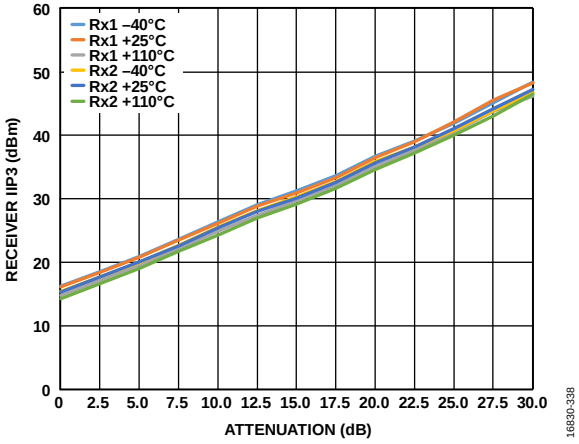


Figure 75. Receiver IIP3 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = 1892 MHz, −21 dBm Each at Attenuation = 0 dB

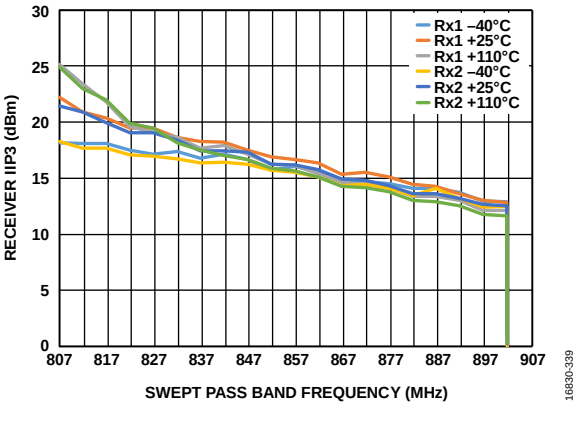


Figure 76. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 800 MHz, Tone 1 = 802 MHz, Tone 2 Swept Across Pass Band, −21 dBm Each

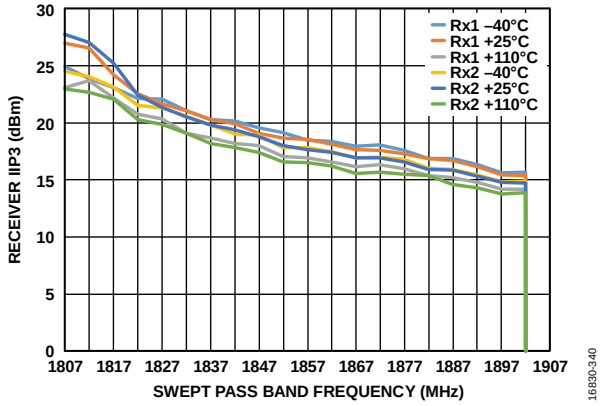


Figure 77. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 Swept Across Pass Band, –21 dBm Each

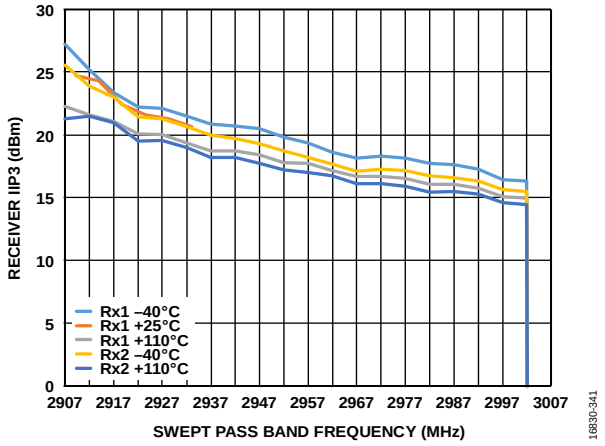


Figure 78. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 2900 MHz, Tone 1 = 2902 MHz, Tone 2 Swept Across Pass Band, –21 dBm Each

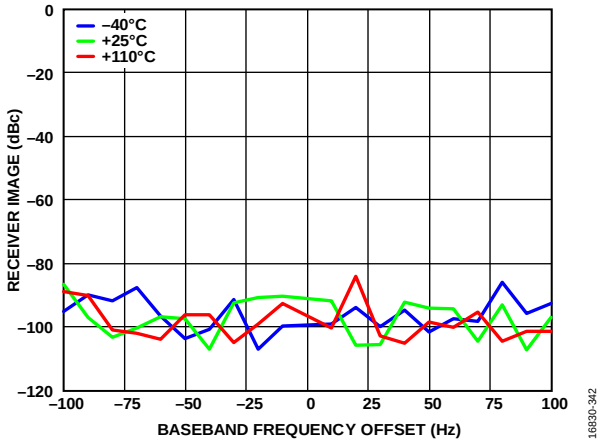


Figure 79. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, 200 MHz RF Bandwidth, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 650 MHz

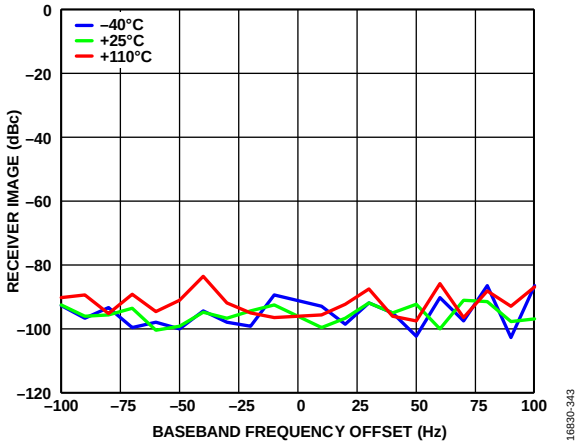


Figure 80. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 1850 MHz

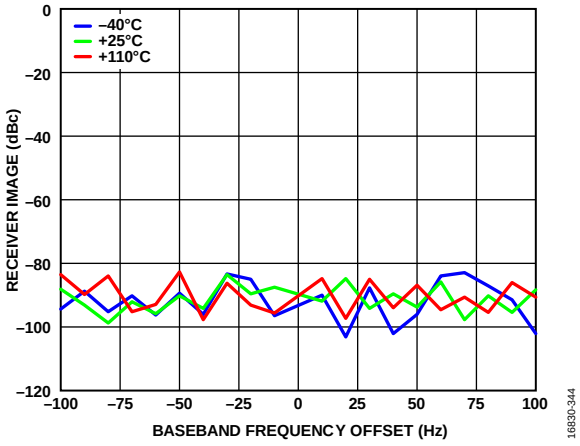


Figure 81. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 2850 MHz

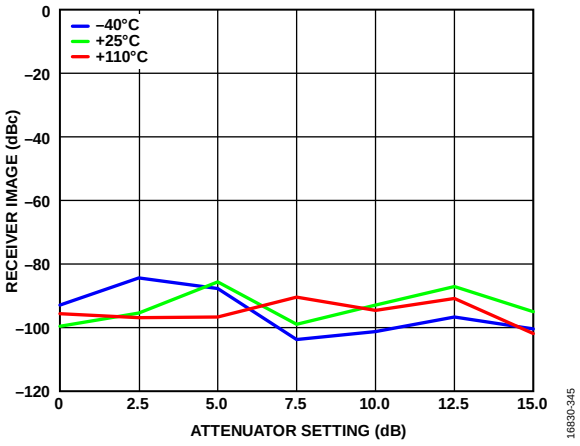


Figure 82. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 1850 MHz

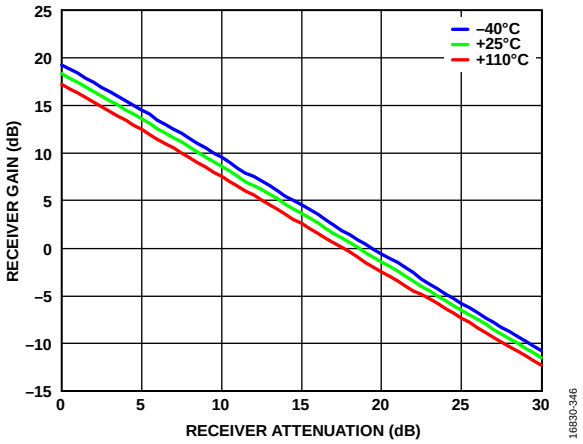


Figure 83. Receiver Gain vs. Receiver Attenuation, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS, LO = 1850 MHz

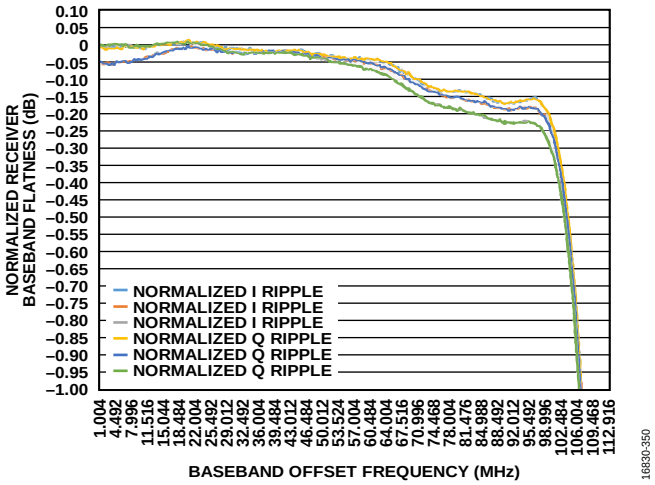


Figure 86. Normalized Receiver Baseband Flatness vs. Baseband Offset Frequency, LO = 2600 MHz

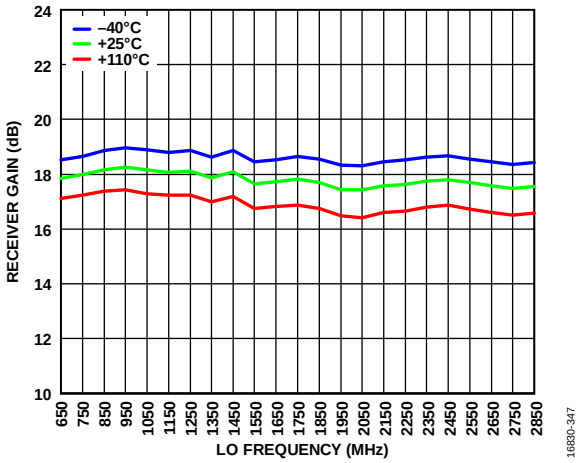


Figure 84. Receiver Gain vs. LO Frequency, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS

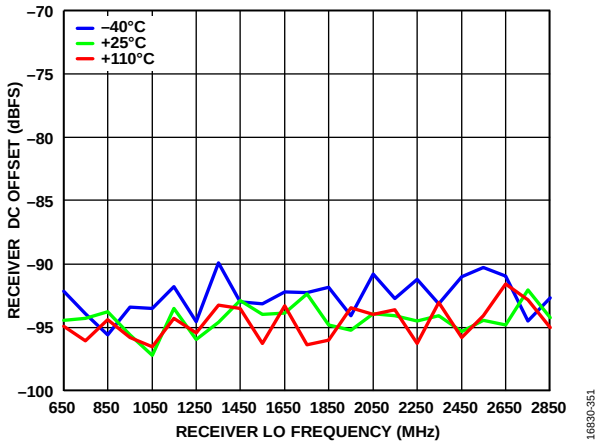


Figure 87. Receiver DC Offset vs. Receiver LO Frequency

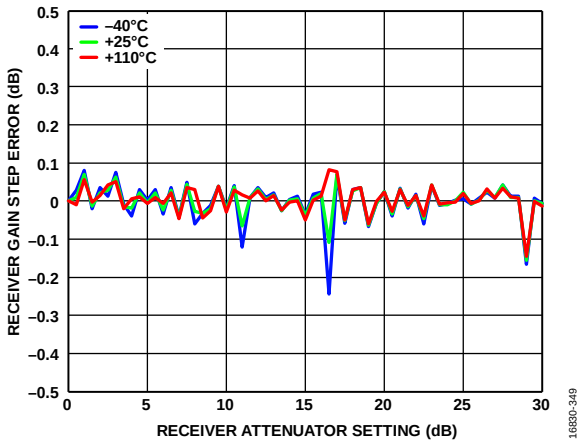


Figure 85. Receiver Gain Step Error vs. Receiver Attenuator Setting over Temperature

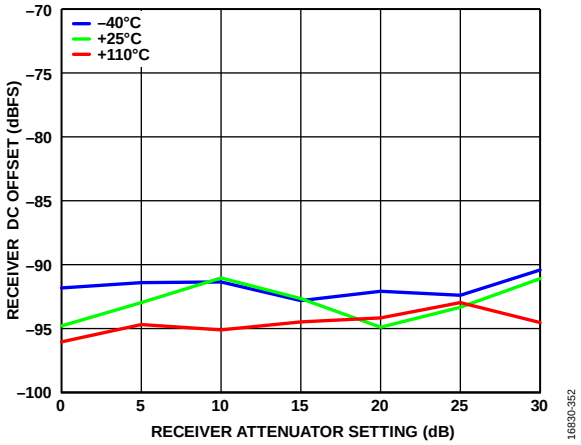


Figure 88. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 1850 MHz

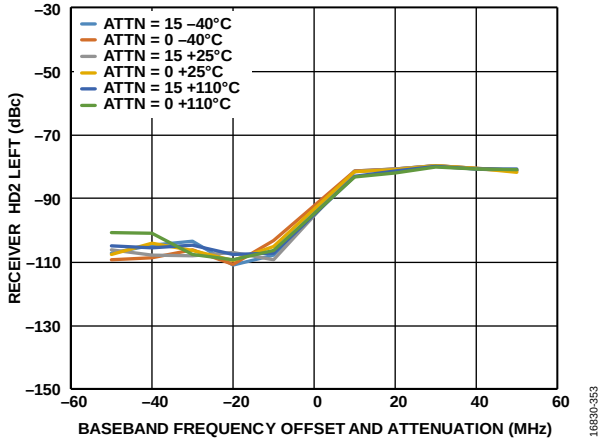


Figure 89. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation, Tone Level = −15 dBm at Attenuation = 0 dB, HD2 Correction Configured for Low-Side Optimization, X-Axis = Baseband Frequency Offset of Fundamental Tone and Not the Frequency of the HD2 Product (HD2 Product = 2× Baseband Frequency), LO = 650 MHz

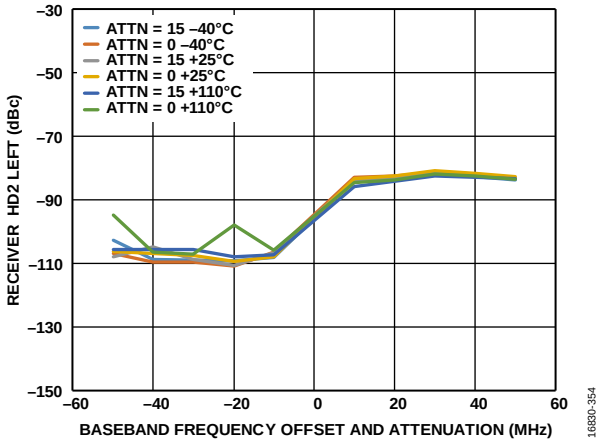


Figure 90. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation, Tone Level = −15 dBm at Attenuation = 0 dB, HD2 Correction Configured for Low-Side Optimization, X-Axis = Baseband Frequency Offset of the Fundamental Tone and Not the Frequency of the HD2 Product (HD2 Product = 2× the Baseband Frequency), LO = 1850 MHz

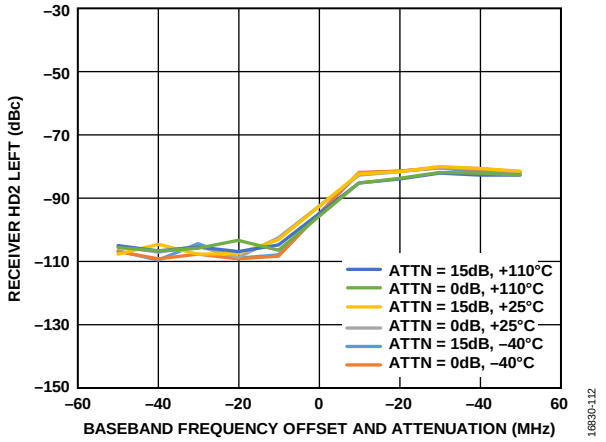


Figure 91. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation, Tone Level = −15 dBm at Attenuation = 0 dB, HD2 Correction Configured for Low-Side Optimization, X-Axis = Baseband Frequency Offset of the Fundamental Tone and Not the Frequency of the HD2 Product (HD2 Product = 2× the Baseband Frequency), LO = 2850 MHz

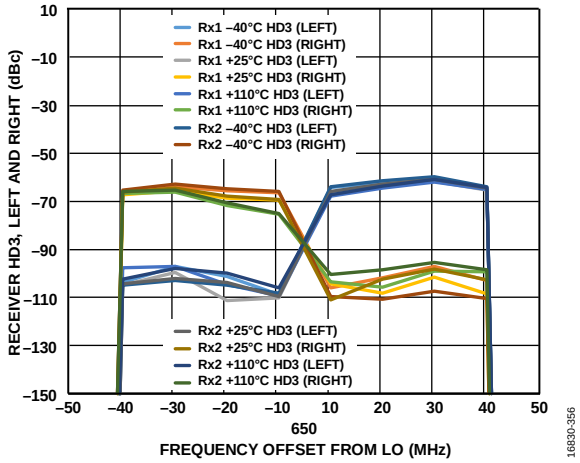


Figure 92. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = −15 dBm at Attenuation = 0 dB, LO = 650 MHz

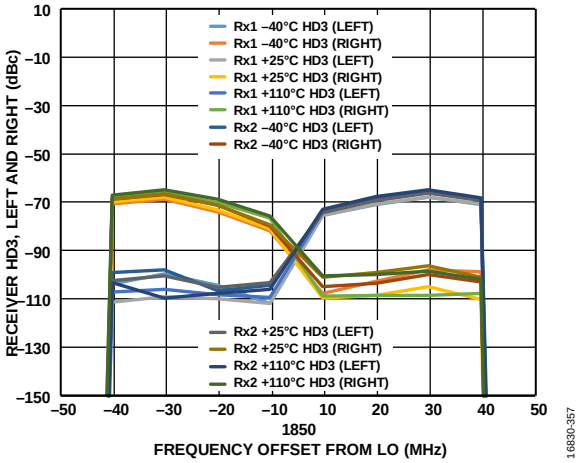


Figure 93. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = −15 dBm at Attenuation = 0 dB, LO = 1850 MHz

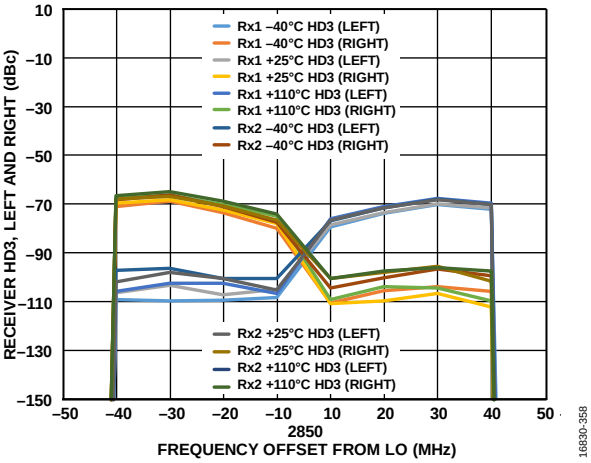


Figure 94. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = −15 dBm at Attenuation = 0 dB, LO = 2850 MHz

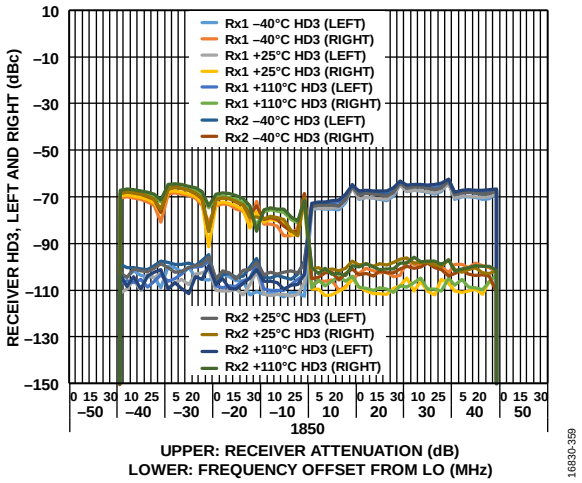


Figure 95. Receiver HD3, Left and Right vs. Receiver Attenuation and Frequency Offset from LO, Baseband Tone Held Constant, Tone Level Increased 1 for 1 as Attenuator is Swept from 0 dB to 30 dB, HD3 Right (High Side): Tone on Same Side as HD3 Product; HD3 Left (Low Side): Tone on Opposite Side as HD3 Product, CW Signal, LO = 1850 MHz, Tone Level = −15 dBm at Attenuation = 0 dB

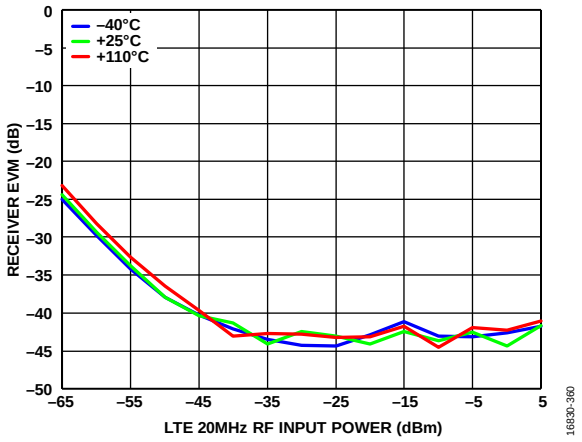


Figure 96. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 600 MHz

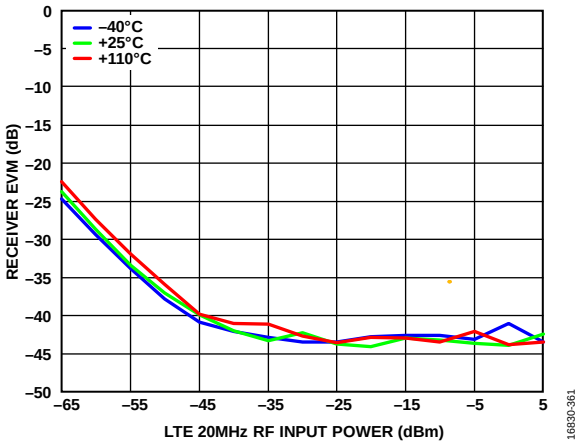


Figure 97. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 1800 MHz

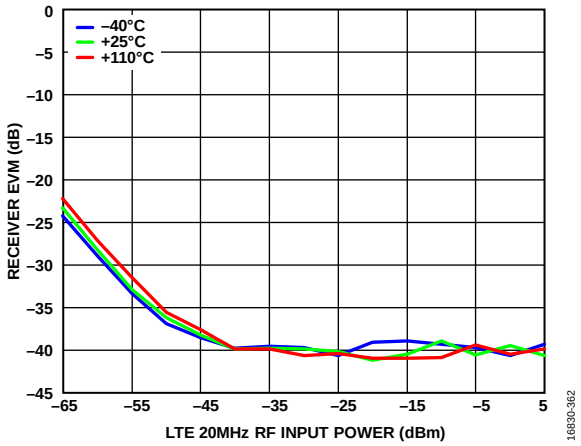


Figure 98. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 2700 MHz

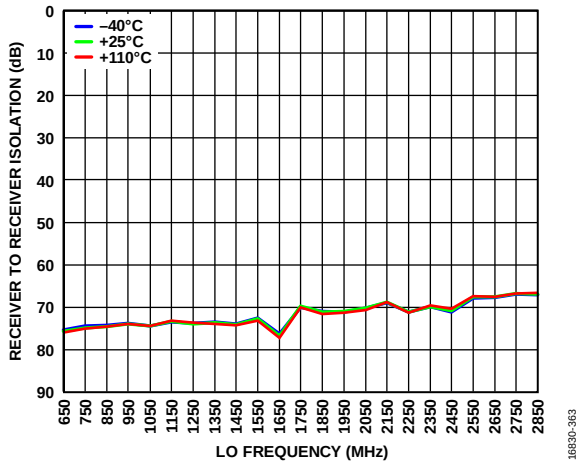


Figure 99. Receiver to Receiver Isolation (dB) vs. LO Frequency (MHz)

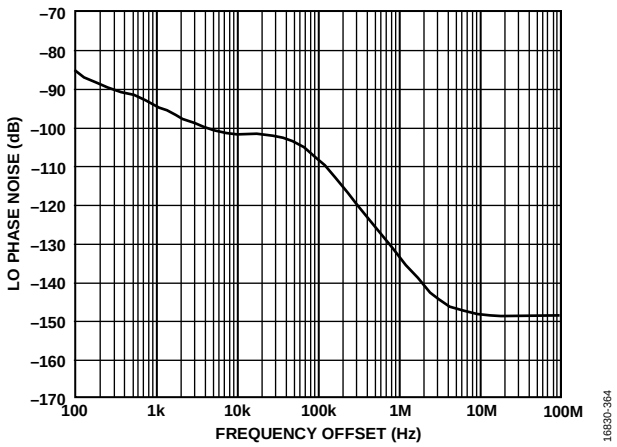


Figure 100. LO Phase Noise vs. Frequency Offset, LO = 1900 MHz, Spectrum Analyzer Limits Far Out Noise

3400 MHz TO 4800 MHz BAND

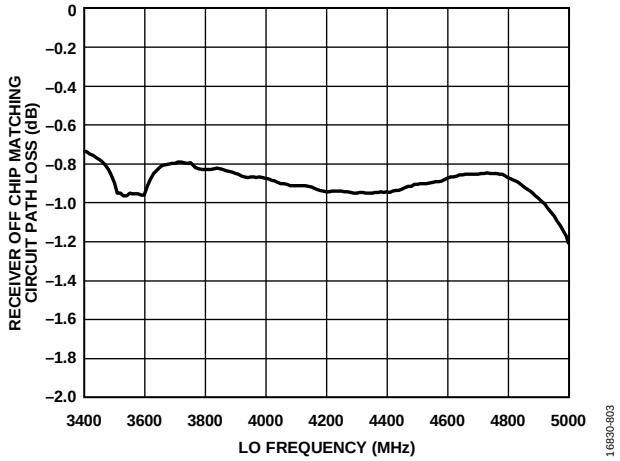


Figure 101. Receiver Off Chip Matching Circuit Path Loss vs. LO Frequency (Simulation), Can Be Used for De-Embedding Performance Data

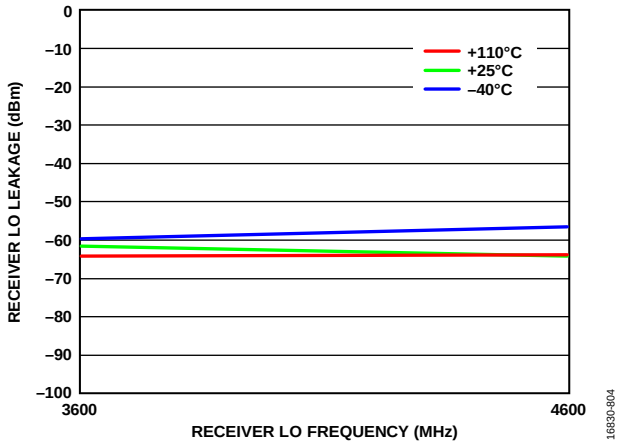


Figure 102. Receiver LO Leakage from 3600 MHz to 4600 MHz, 0 dB Receiver Attenuation, 200 MHz RF Bandwidth, 245.76 MSPS Sample Rate

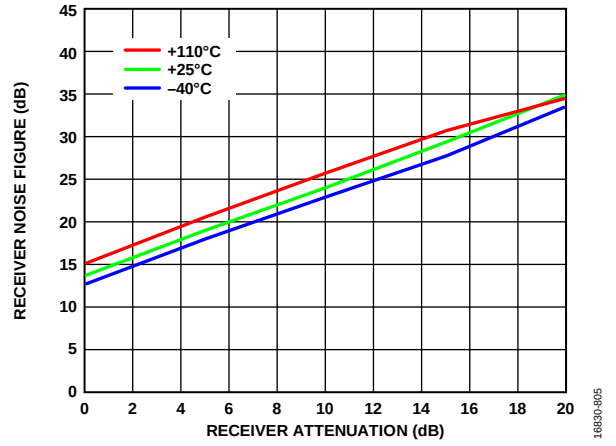


Figure 103. Receiver Noise Figure vs. Receiver Attenuation, LO = 3600 MHz, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

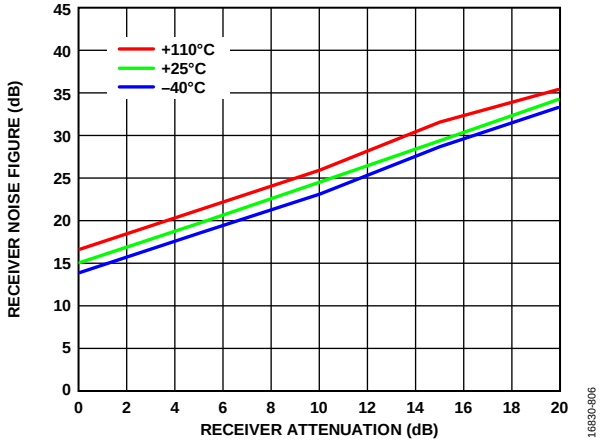


Figure 104. Receiver Noise Figure vs. Receiver Attenuation, LO = 4600 MHz, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

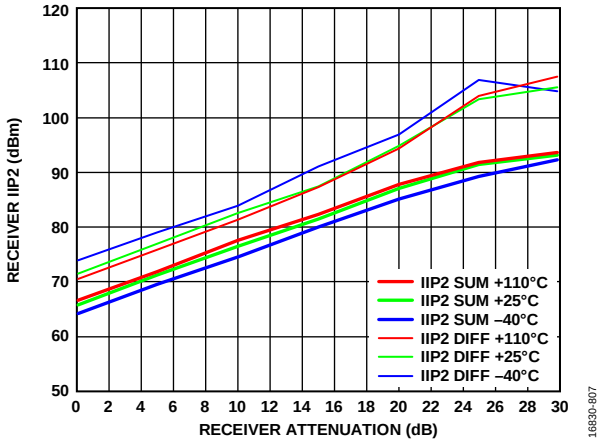


Figure 105. Receiver IIP2 vs. Receiver Attenuation, LO = 3600 MHz, Tones Placed at 3645 MHz and 3646 MHz, –21 dBm Plus Attenuation

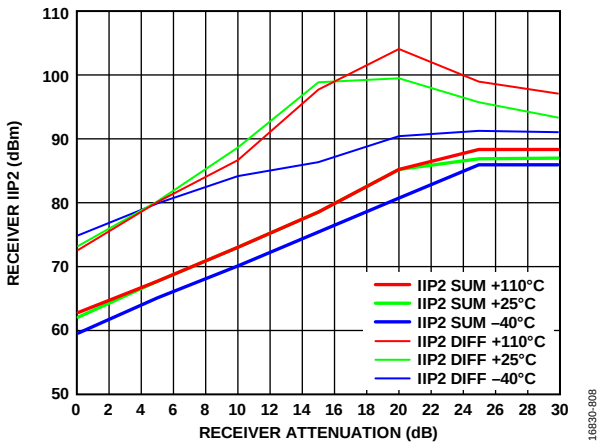


Figure 106. Receiver IIP2 vs. Receiver Attenuation, LO = 4600 MHz, Tones Placed at 4645 MHz and 4646 MHz, –21 dBm Plus Attenuation

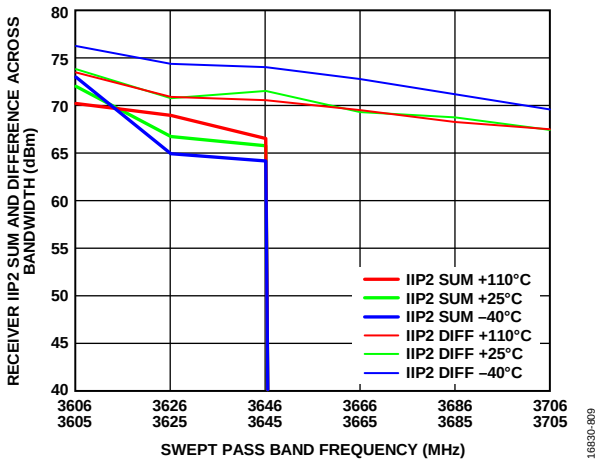


Figure 107. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 3600 MHz, Six Tone Pairs, –21 dBm Plus Attenuation Each

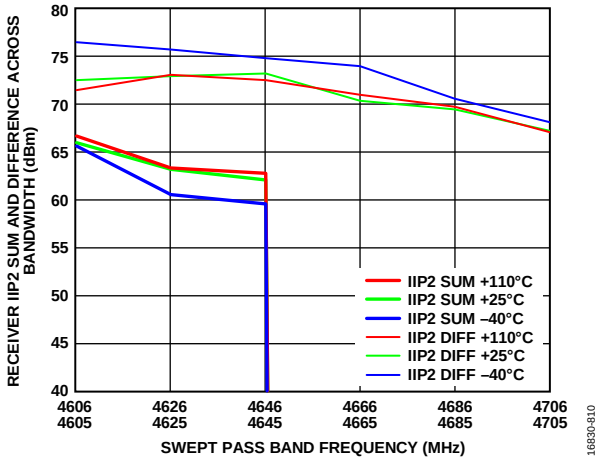


Figure 108. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 4600 MHz, Six Tone Pairs, –21 dBm Each

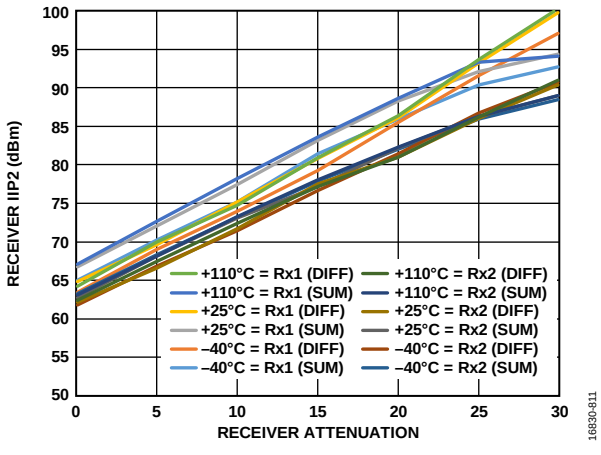


Figure 109. Receiver IIP2 vs. Receiver Attenuation, LO = 3600 MHz, Tone 1 = 4602 MHz and Tone 2 = 4692 MHz, –21 dBm Plus Attenuation

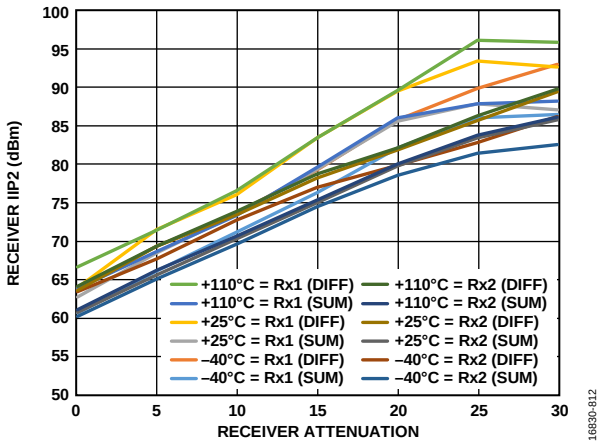


Figure 110. Receiver IIP2 vs. Receiver Attenuation, LO = 4600 MHz, Tones Placed at 4602 MHz and 4692 MHz, –21 dBm Plus Attenuation

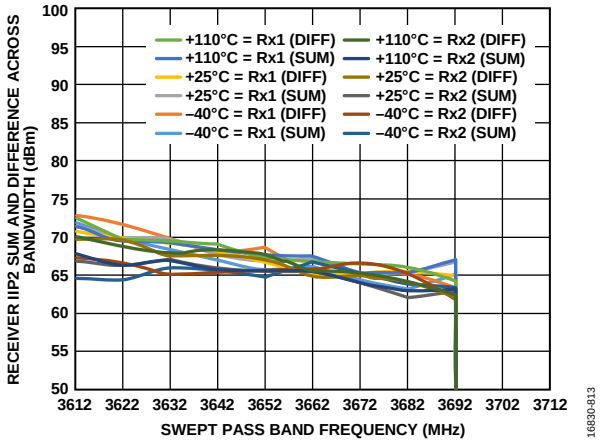


Figure 111. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 Swept, –21 dBm Each

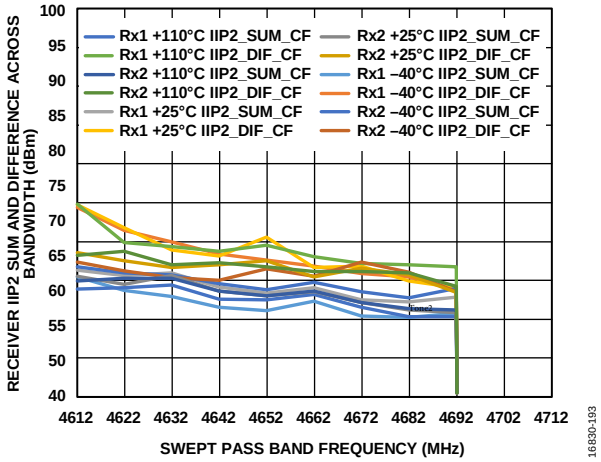


Figure 112. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 Swept, –21 dBm Each, IIP2_SUM_CF and IIP2_DIF_CF Indicate Sum and Difference Products

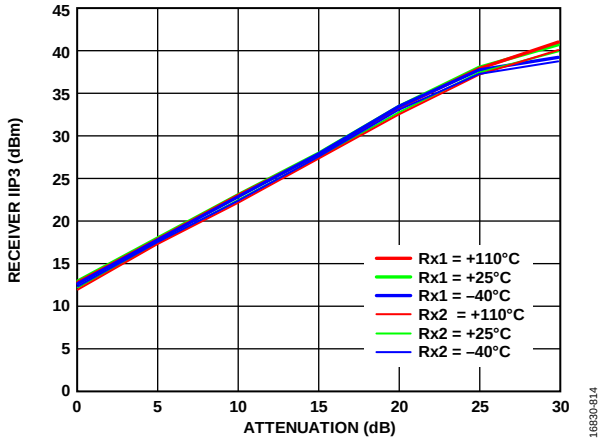


Figure 113. Receiver IIP3 vs. Attenuation, LO = 3600 MHz, Tone 1 = 3695 MHz, Tone 2 = 3696 MHz, −21 dBm Plus Attenuation

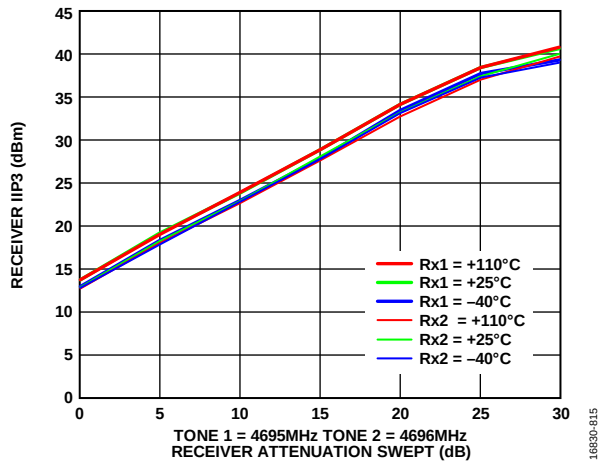


Figure 114. Receiver IIP3 vs. Receiver Attenuation Swept, LO = 4600 MHz, Tone 1 = 4695 MHz, Tone 2 = 4696 MHz, −21 dBm Plus Attenuation

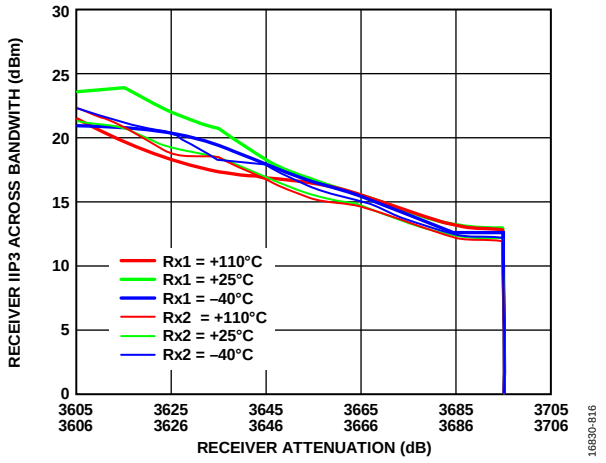


Figure 115. Receiver IIP3 Across Bandwidth, Receiver Attenuation = 0 dB, LO = 3600 MHz, Tone 2 = Tone 1 + 1 MHz, −21 dBm Each, Swept Across Pass Band

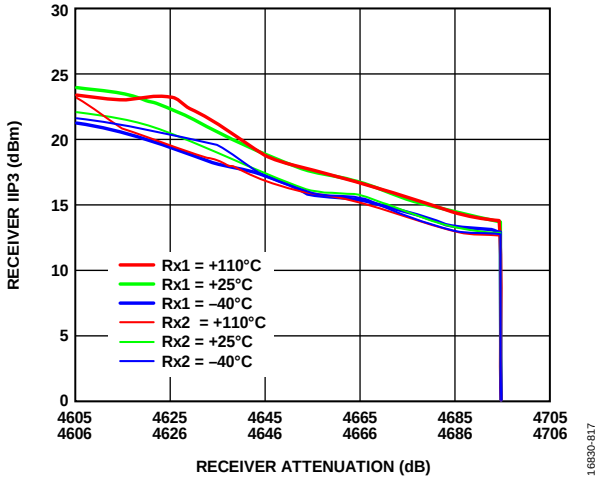


Figure 116. Receiver IIP3 vs. Receiver Attenuation, Receiver Attenuation = 0 dB, LO = 4600 MHz, Tone 2 = Tone 1 + 1 MHz, −21 dBm Each, Swept Across Pass Band

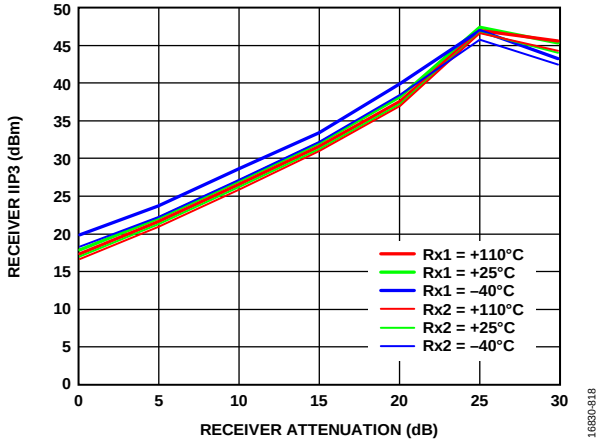


Figure 117. Receiver IIP3 vs. Receiver Attenuation, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = 3692 MHz, −21 dBm Plus Attenuation

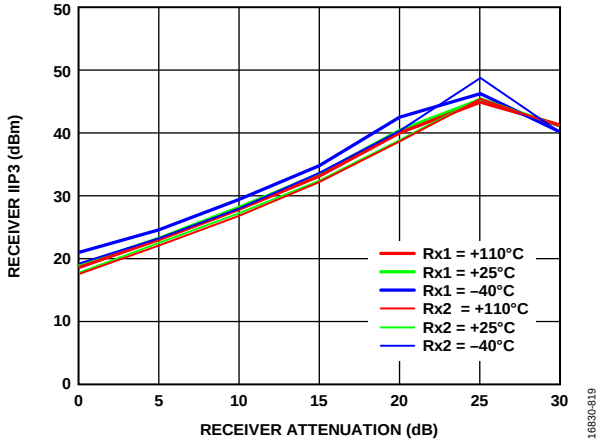


Figure 118. Receiver IIP3 vs. Receiver Attenuation, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = 4692 MHz, −21 dBm Plus Attenuation

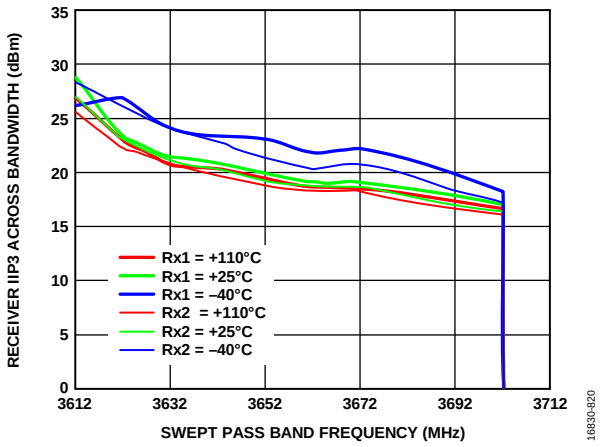


Figure 119. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 Swept Across Pass Band, −21 dBm Each

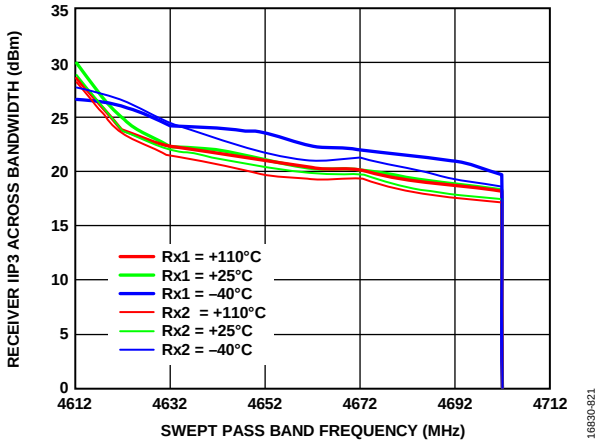


Figure 120. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 Swept Across Pass Band, −21 dBm Each

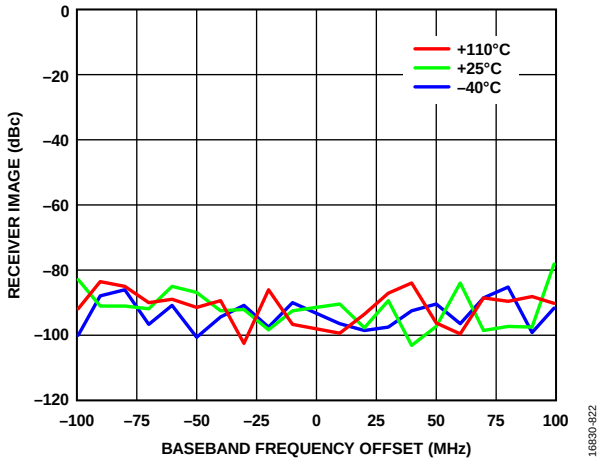


Figure 121. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 3600 MHz

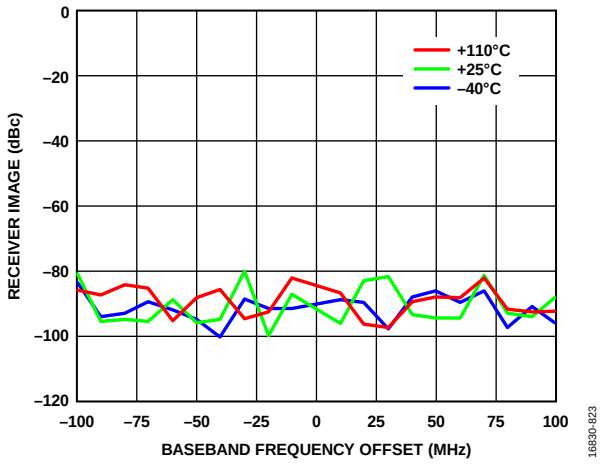


Figure 122. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 4600 MHz

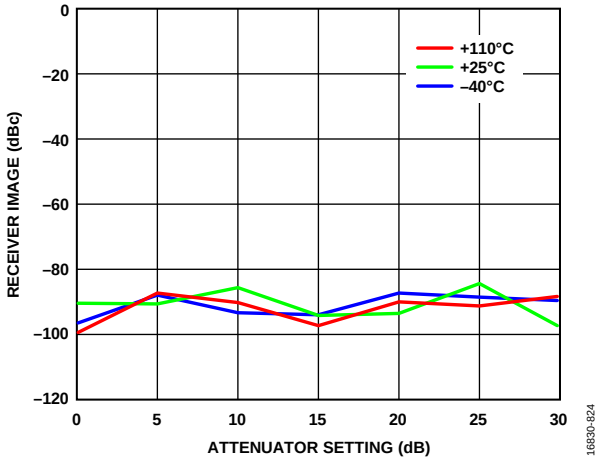


Figure 123. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 3600 MHz, Baseband Frequency= 10 MHz

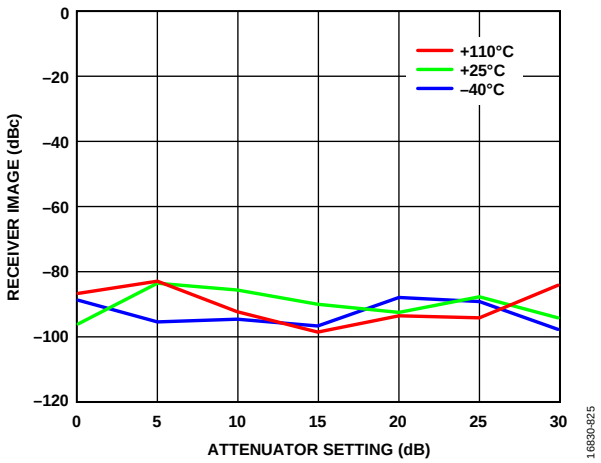


Figure 124. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 4600 MHz, Baseband Frequency = 10 MHz

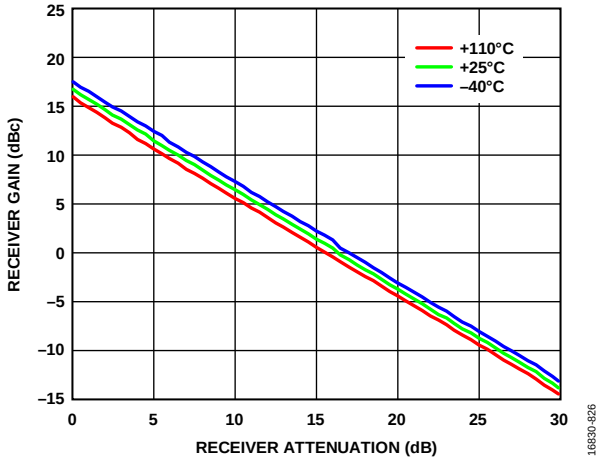


Figure 125. Receiver Gain vs. Receiver Attenuation, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS, LO = 3600 MHz

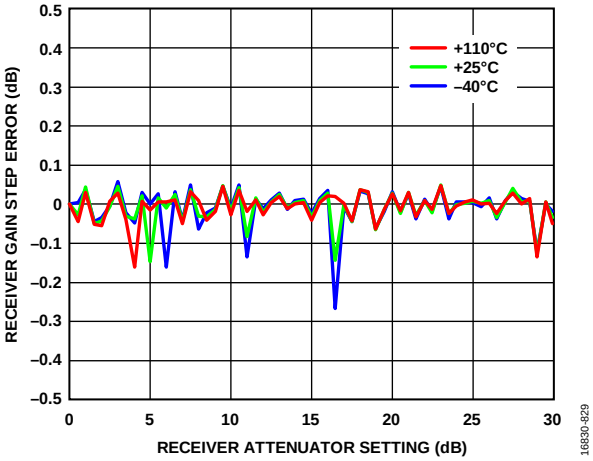


Figure 128. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 3600 MHz

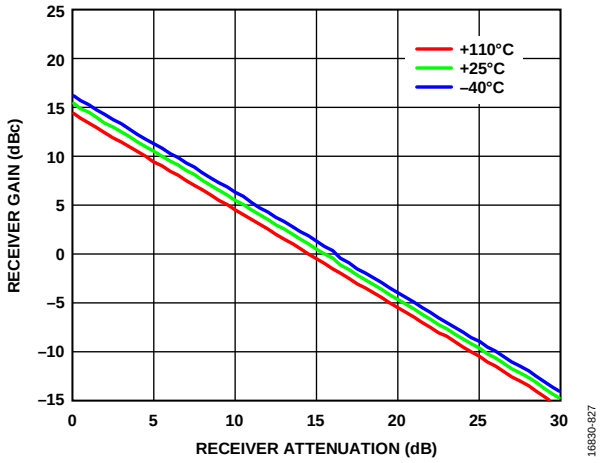


Figure 126. Receiver Gain vs. Receiver Attenuation, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS, LO = 4600 MHz

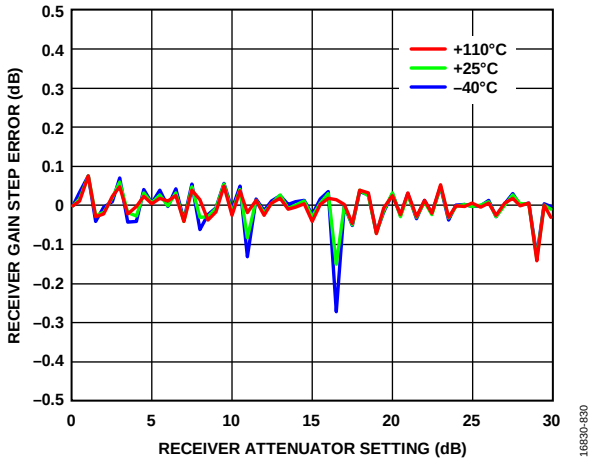


Figure 129. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 4600 MHz

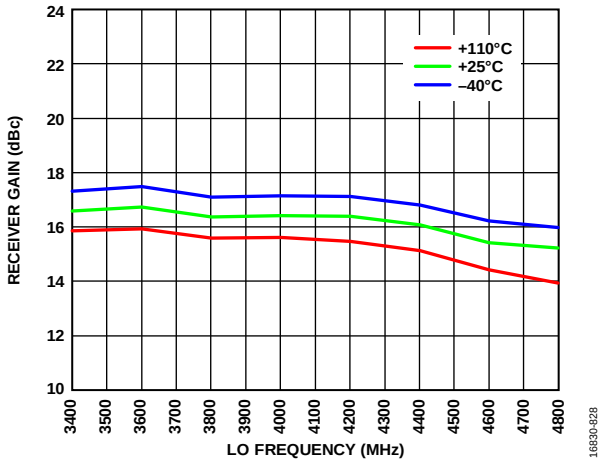


Figure 127. Receiver Gain vs. LO Frequency, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS

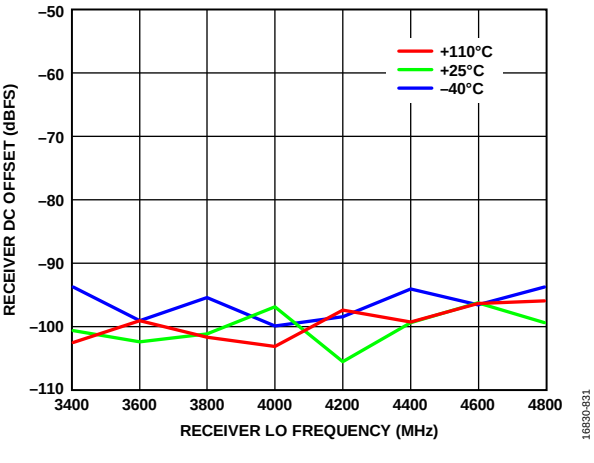


Figure 130. Receiver DC Offset vs. Receiver LO Frequency

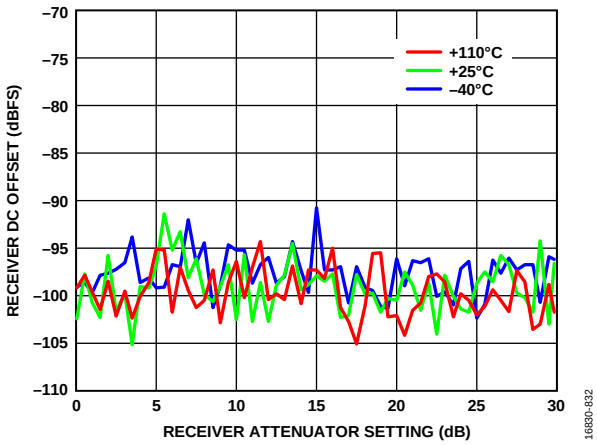


Figure 131. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 3600 MHz

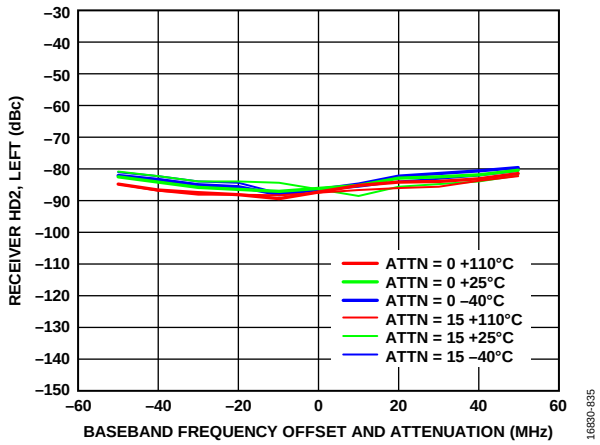


Figure 134. Receiver HD2, Left vs. Baseband Frequency Offset and Attenuation, Tone Level = −15 dBm at Attenuation = 0 dB, X-Axis = Baseband Frequency Offset of the Fundamental Tone, Not the Frequency of the HD2 Product (HD2 Product = 2× the Baseband Frequency), HD2 Canceller Disabled, LO = 4600 MHz

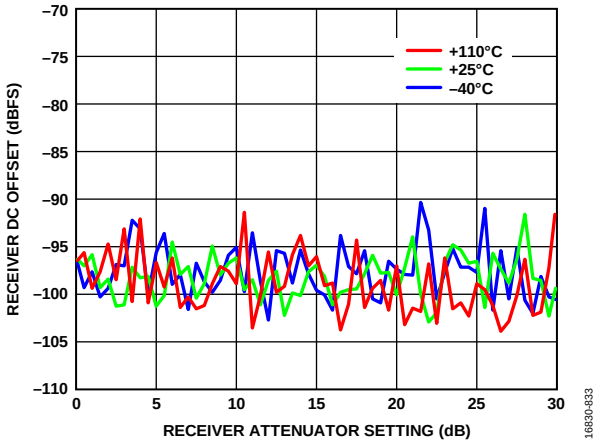


Figure 132. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 4600 MHz

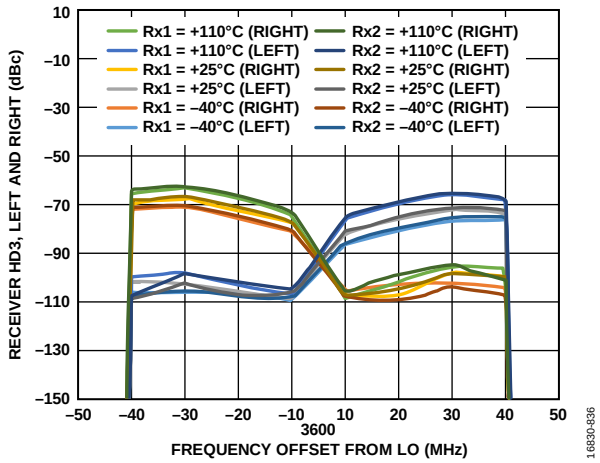


Figure 135. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = −15 dBm at Attenuation = 0 dB, LO = 3600 MHz

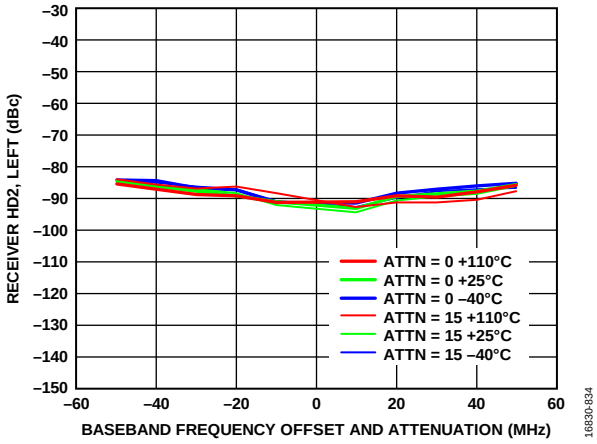


Figure 133. Receiver HD2, Left vs. Baseband Frequency Offset and Attenuation, Tone Level = −15 dBm at Attenuation = 0 dB, X-Axis = Baseband Frequency Offset of the Fundamental Tone Not the Frequency of the HD2 Product (HD2 Product = 2× the Baseband Frequency), HD2 Canceller Disabled, LO = 3600 MHz

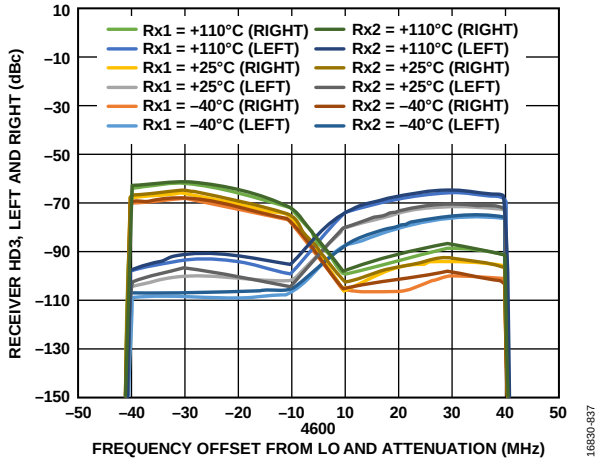


Figure 136. Receiver HD3, Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level = −15 dBm at Attenuation = 0 dB, LO = 4600 MHz

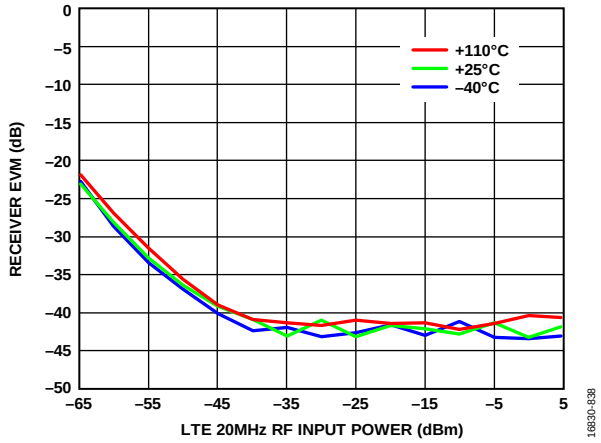


Figure 137. Receiver EVM vs. LTE 20 MHz RF Input Power, RF Signal = LTE 20 MHz, LO = 3600 MHz, Default AGC Settings

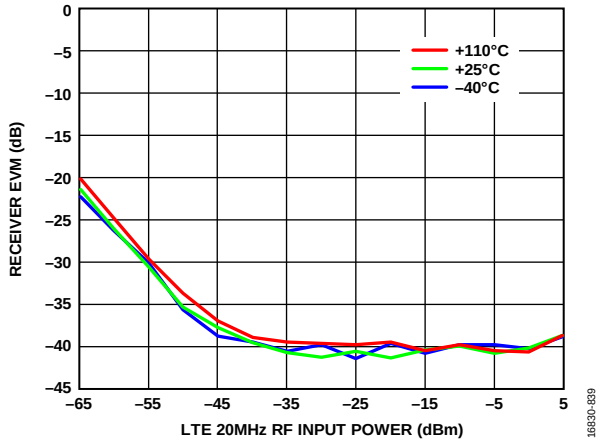


Figure 138. Receiver EVM vs. LTE 20 MHz RF Input Power, RF Signal = LTE 20 MHz, LO = 4600 MHz, Default AGC Settings

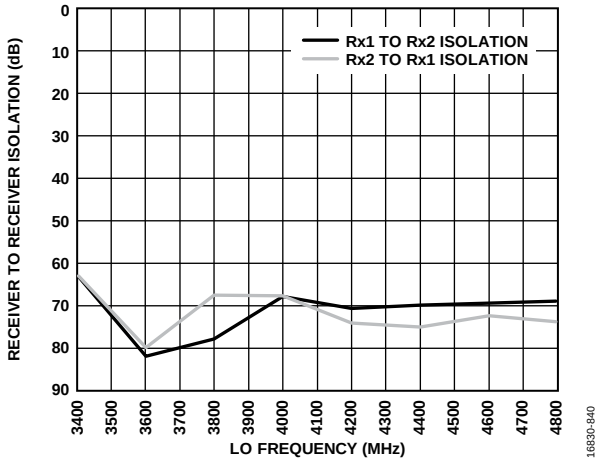


Figure 139. Receiver to Receiver Isolation vs. LO Frequency

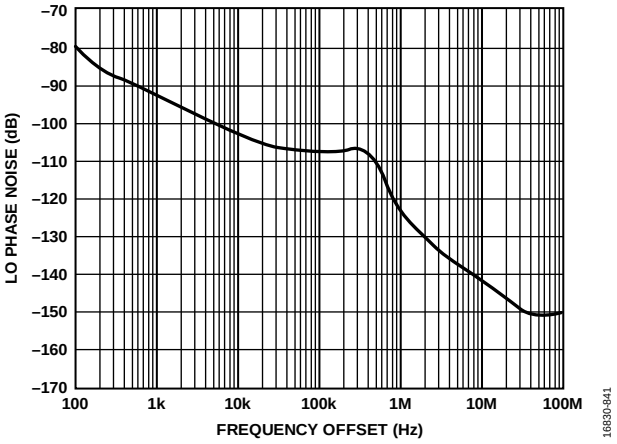


Figure 140. LO Phase Noise vs. Frequency Offset, LO = 3800 MHz, PLL Loop Bandwidth = 300 kHz, Spectrum Analyzer Limits Far Out Noise

5100 MHz TO 5900 MHz BAND

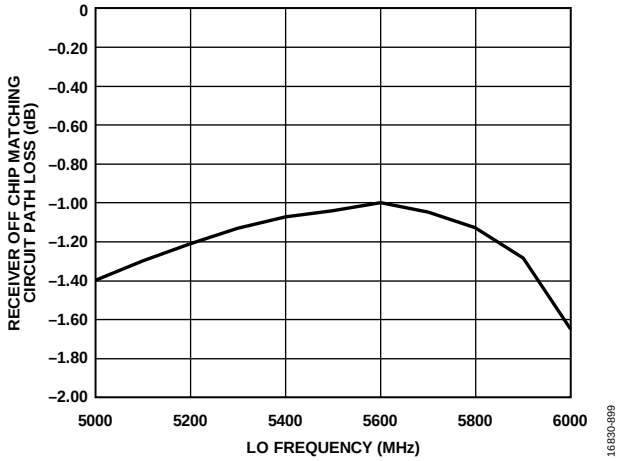


Figure 141. Receiver Off Chip Matching Circuit Path Loss vs. LO Frequency (Simulation), Can Be Used for De-Embedding Performance Data

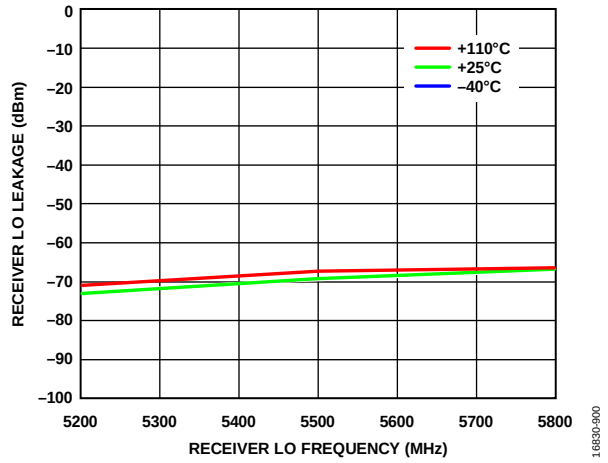


Figure 142. Receiver LO Leakage vs. Receiver LO Frequency, 5200 MHz, 5500 MHz, and 5800 MHz, Receiver Attenuation = 0 dB, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS

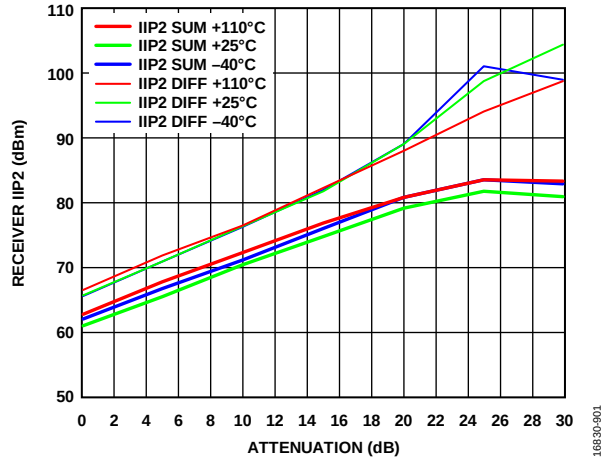


Figure 143. Receiver IIP2 vs. Attenuation, LO = 5800 MHz, Tones Placed at 5845 MHz and 5846 MHz, –21 dBm Plus Attenuation

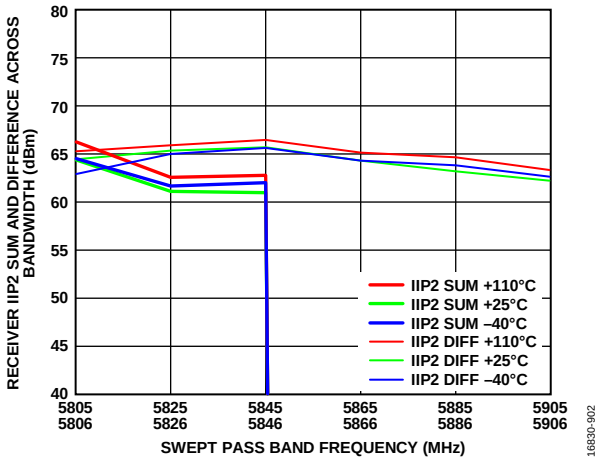


Figure 144. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Six Tone Pairs, –21 dBm Plus Attenuation Each

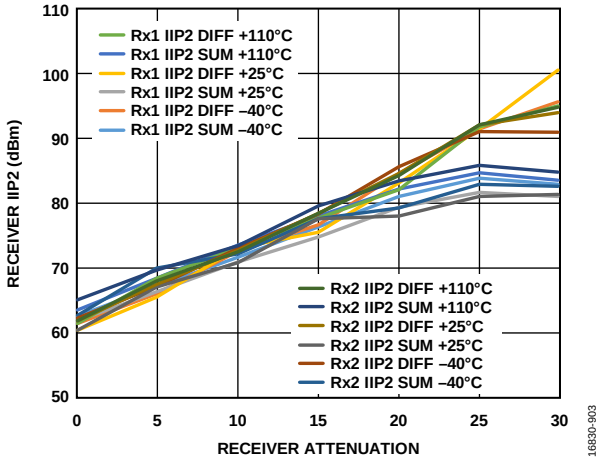


Figure 145. Receiver IIP2 vs. Receiver Attenuation, LO = 5800 MHz, Tones Placed at 5802 MHz and 5892 MHz, –21 dBm Plus Attenuation

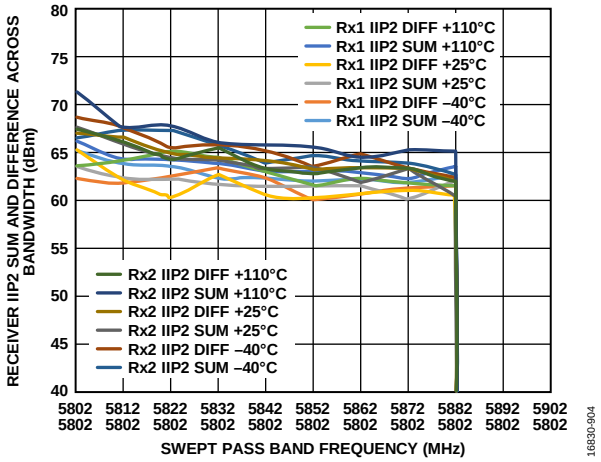


Figure 146. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Tone 1 = 5802 MHz, Tone 2 Swept, –21 dBm Each

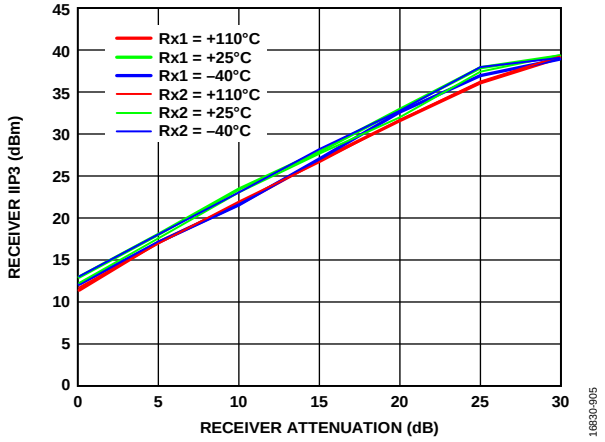


Figure 147. Receiver IIP3 vs. Receiver Attenuation, LO = 5800 MHz, Tone 1 = 5895 MHz, Tone 2 = 5896 MHz, −21 dBm Plus Attenuation

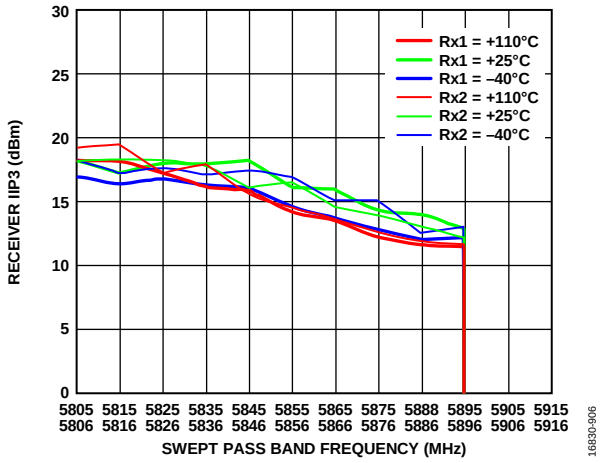


Figure 148. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Tone 2 = Tone 1 + 1 MHz, −21 dBm Each, Swept Across Pass Band

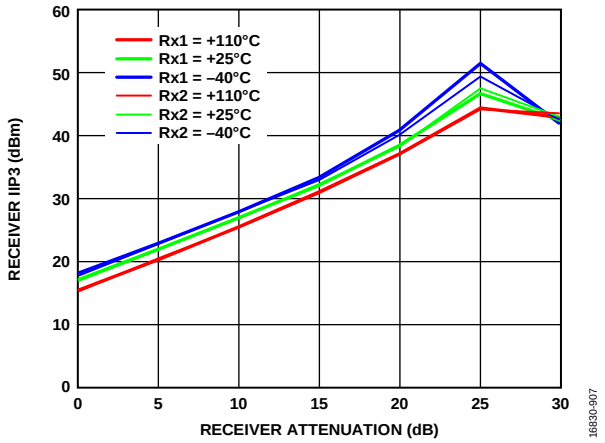


Figure 149. Receiver IIP3 vs. Receiver Attenuation, LO = 5800 MHz, Tone 1 = 5802 MHz, Tone 2 = 5892 MHz, −21 dBm Plus Attenuation

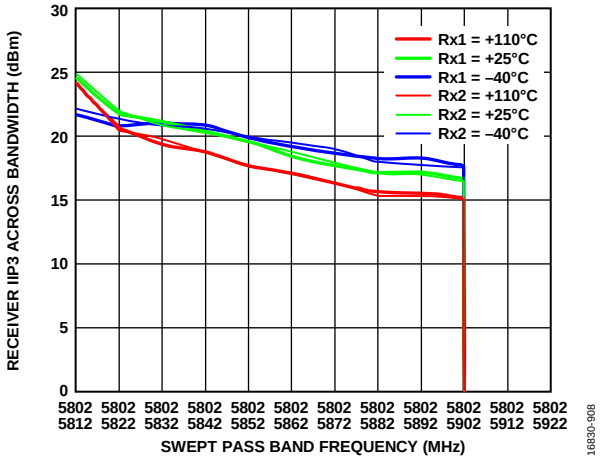


Figure 150. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Tone 1 = 5802 MHz, Tone 2 Swept Across Pass Band, −21 dBm Each

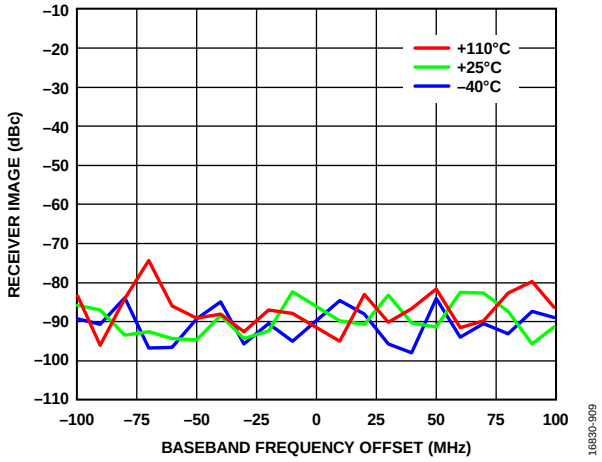


Figure 151. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5200 MHz

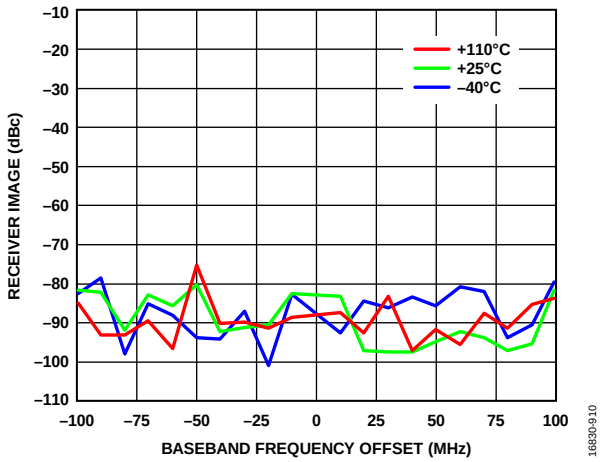


Figure 152. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5900 MHz

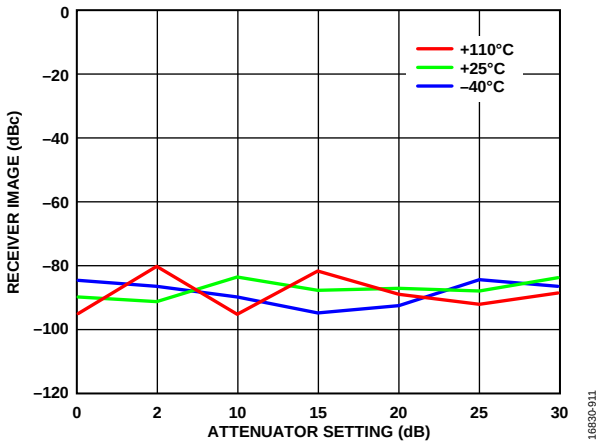


Figure 153. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5200 MHz, Baseband Frequency = 10 MHz

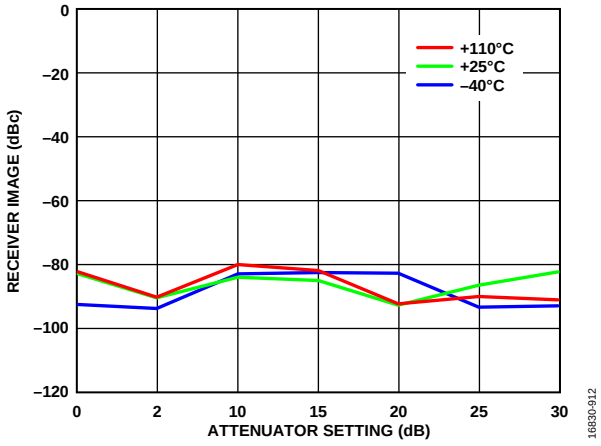


Figure 154. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5900MHz, Baseband Frequency = 10 MHz

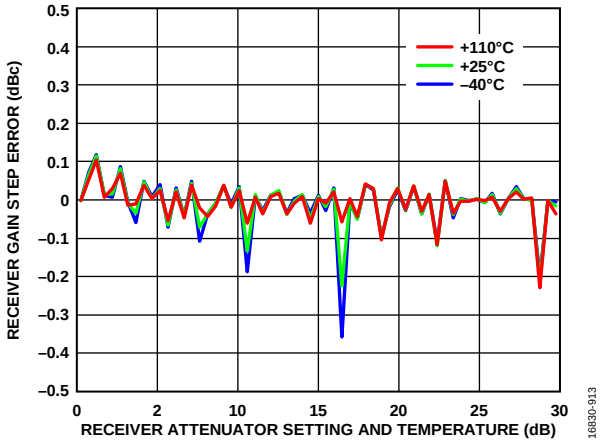


Figure 155. Receiver Gain Step Error vs. Receiver Attenuator Setting and Temperature, LO = 5200 MHz

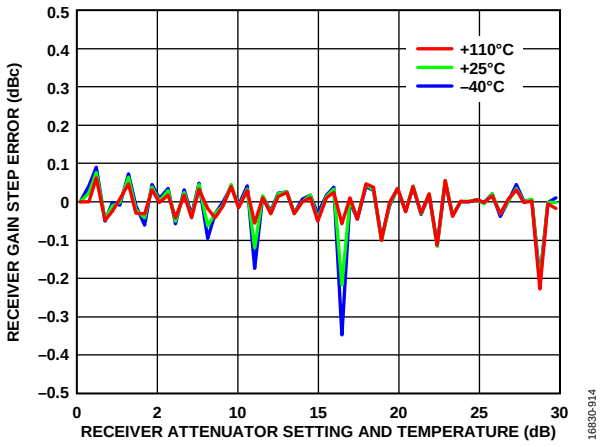


Figure 156. Receiver Gain Step Error vs. Receiver Attenuator Setting and Temperature, LO = 5600 MHz

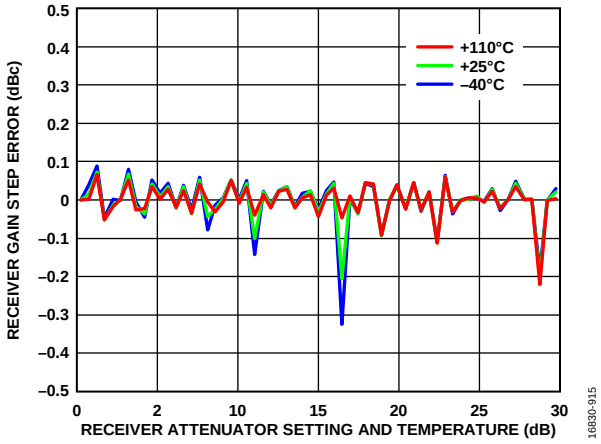


Figure 157. Receiver Gain Step Error vs. Receiver Attenuator Setting and Temperature, LO = 6000 MHz

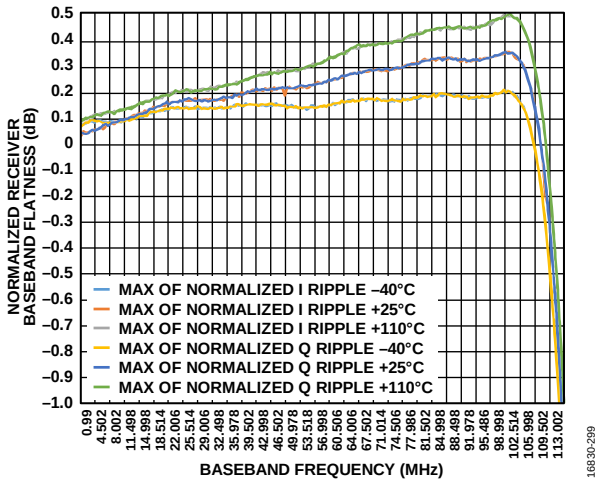


Figure 158. Normalized Receiver Baseband Flatness vs. Baseband Frequency (Receiver Flatness)

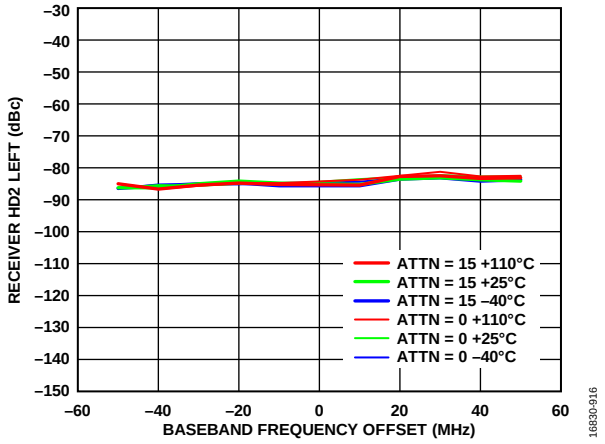


Figure 159. Receiver HD2 Left vs. Baseband Frequency Offset, Tone Level = −15 dBm at Attenuation = 0 dB, X-Axis = Baseband Frequency Offset of the Fundamental Tone Not the Frequency of the HD2 Product (HD2 Product = 2× the Baseband Frequency), HD2 Canceller Disabled, LO = 5200 MHz

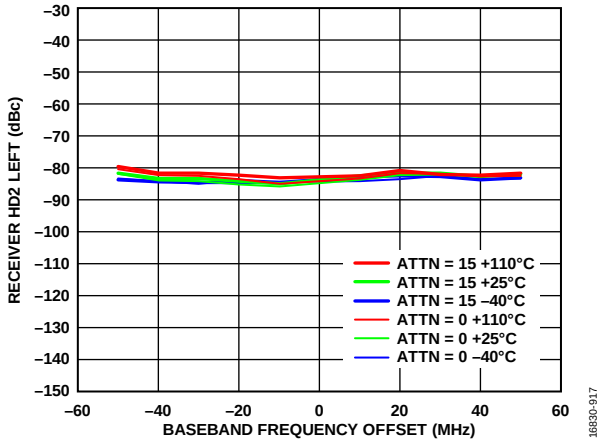


Figure 160. Receiver HD2 Left vs. Baseband Frequency Offset, Tone Level = −15 dBm at Attenuation = 0 dB, X-Axis = Baseband Frequency Offset of the Fundamental Tone Not the Frequency of the HD2 Product (HD2 Product = 2× the Baseband Frequency), HD2 Canceller Disabled, LO = 5900 MHz

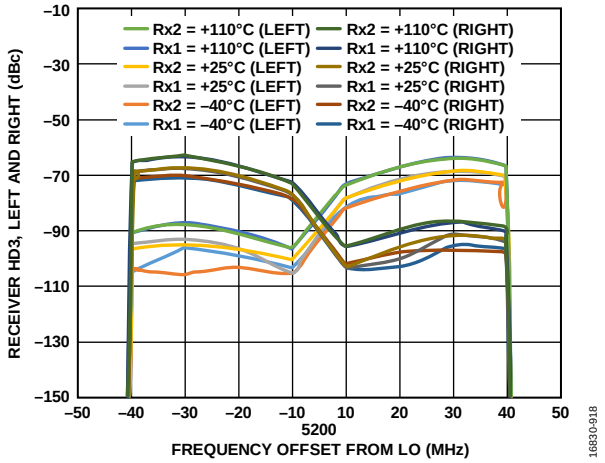


Figure 161. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = −15 dBm at Attenuation = 0 dB, LO = 5200 MHz

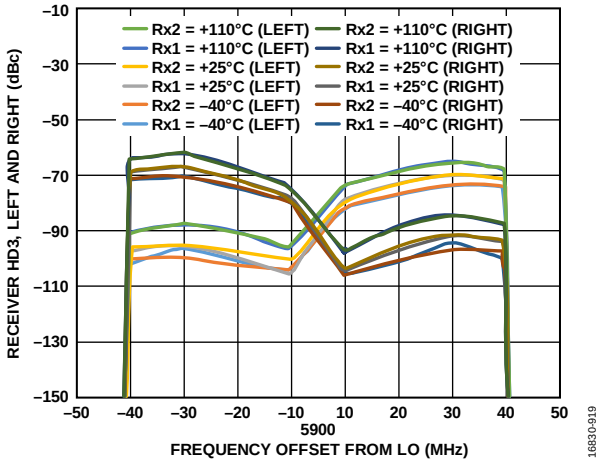


Figure 162. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = −15 dBm at Attenuation = 0 dB, LO = 5900 MHz

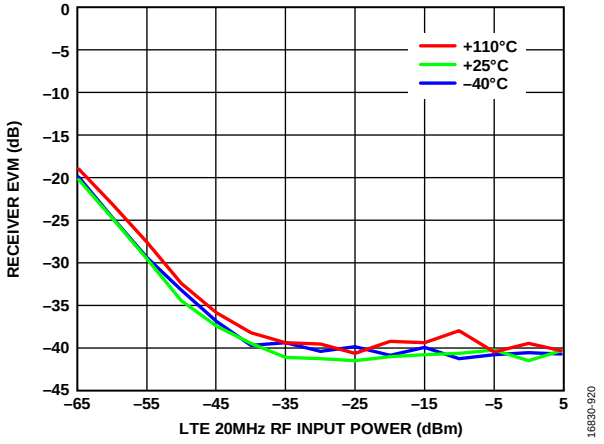


Figure 163. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 5200 MHz, Default AGC Settings

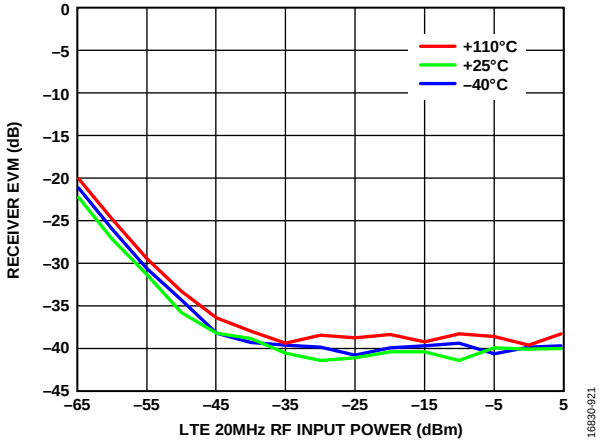


Figure 164. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 5500 MHz, Default AGC Settings

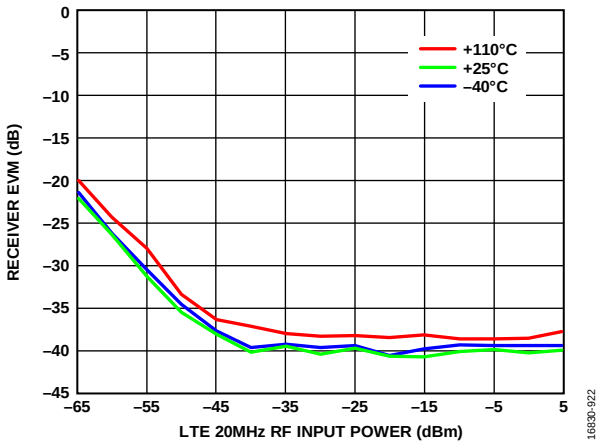


Figure 165. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 5800 MHz, Default AGC Settings

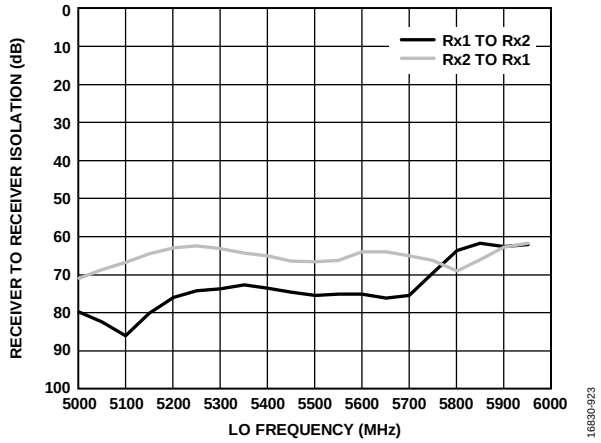


Figure 166. Receiver to Receiver Isolation vs. LO Frequency

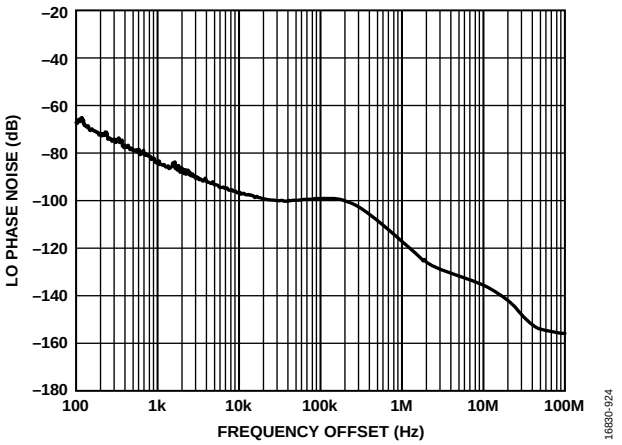


Figure 167. LO Phase Noise vs. Frequency Offset, LO = 5900 MHz, PLL Loop Bandwidth > 300 kHz, Spectrum Analyzer Limits Far Out Noise

RECEIVER INPUT IMPEDANCE

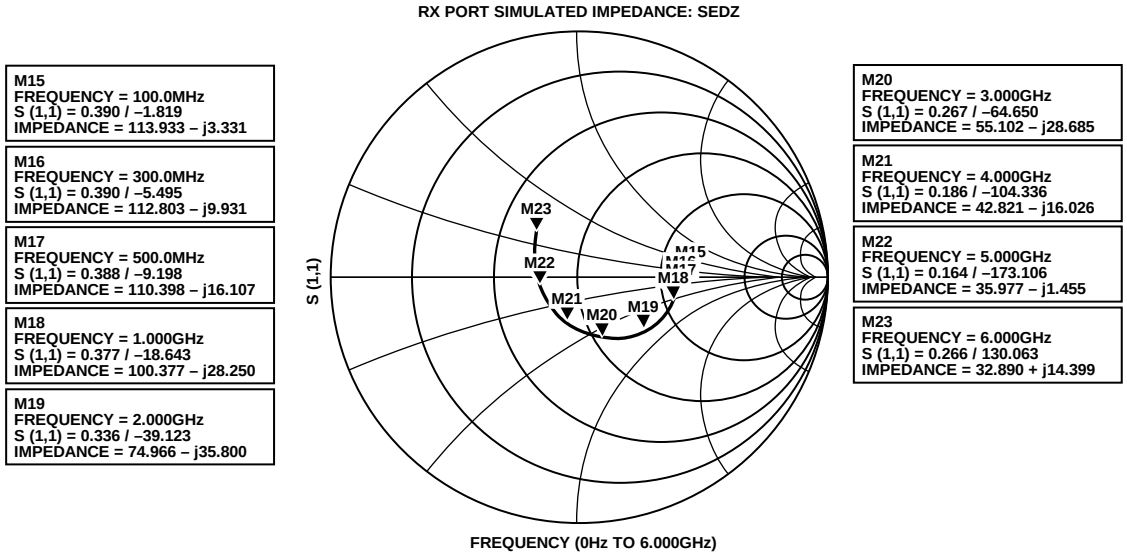


Figure 168. Receiver Input Impedance, Series Equivalent Differential Impedance (SEDZ)

TERMINOLOGY

Large Signal Bandwidth

Large signal bandwidth, otherwise known as instantaneous bandwidth or signal bandwidth, is the bandwidth over which there are large signals. For example, for Band 42 LTE, the large signal bandwidth is 200 MHz.

Occupied Bandwidth

Occupied bandwidth is the total bandwidth of the active signals. For example, three 20 MHz carriers have a 60 MHz occupied bandwidth, regardless of the placement of the carriers within the large signal bandwidth.

Backoff

Backoff is the difference (in dB) between full-scale signal power and the rms signal power.

P_{HIGH}

P_{HIGH} is the largest signal that can be applied without overloading the ADC for the receiver input. This input level results in slightly less than full scale at the digital output because of the nature of the continuous-time, Σ-Δ ADCs, which, for example, exhibit a soft overload in contrast to the hard clipping of pipeline ADCs.

THEORY OF OPERATION

The ADRV9008-1 is a highly integrated, RF, agile receiver subsystem capable of configuration for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide all receiver functions in a single device. Programmability allows the receiver to be adapted for use in many TDD and 3G/4G/5G cellular standards. The ADRV9008-1 contains two high speed links each for the receiver chain. These links are JESD204B, Subclass 1 compliant.

The ADRV9008-1 also provides tracking correction of dc offset QEC errors to maintain high performance under varying temperatures and input signal conditions. The device also includes test modes that allow system designers to debug designs during prototyping and optimize radio configurations.

RECEIVERS

The ADRV9008-1 receivers contain all the blocks necessary to receive RF signals and convert them to digital data used by a BBP. Each receiver can be configured as a direct conversion system that supports up to a 200 MHz bandwidth. Each receiver contains a programmable attenuator stage and matched I and Q mixers that downconvert received signals to baseband for digitization.

Achieve gain control by using the on-chip AGC or by allowing the BBP to make gain adjustments in a manual gain control mode. Optimize performance by mapping each gain control setting to specific attenuation levels at each adjustable gain block in the receiver signal path. Additionally, each channel contains independent receive signal strength indicator (RSSI) measurement capability, dc offset tracking, and all circuitry necessary for self calibration.

The receivers include ADCs and adjustable sample rates that produce data streams from the received signals. The signals can be conditioned further by a series of decimation filters and a programmable FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

CLOCK INPUT

The ADRV9008-1 requires a differential clock connected to the REF_CLK_IN_x pins. The frequency of the clock input must be between 10 MHz and 1000 MHz, and the frequency must have low phase noise because this signal generates the RF LO and internal sampling clocks.

SYNTHESIZERS

RF PLL

The ADRV9008-1 contains a fractional-N PLL to generate the RF LO for the signal paths. The PLL incorporates an internal VCO and loop filter, requiring no external components. The LOs on multiple chips can be phase synchronized to support active antenna systems and beam forming applications.

Clock PLL

The ADRV9008-1 contains a PLL synthesizer that generates all the baseband related clock signals and serialization/deserialization (SERDES) clocks. This PLL is programmed based on the data rate and sample rate requirements of the system.

SPI

The ADRV9008-1 uses an SPI interface to communicate with the BBP. This interface can be configured as a 4-wire interface with a dedicated receiver port and transmitter port. The interface can also be configured as a 3-wire interface with a bidirectional data communications port. This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first five bits set the bus direction and the number of bytes to transfer. The next 11 bits set the address where the data is written. The final eight bits are the data transferred to the specific register address.

Read commands follow a similar format with the exception that the first 16 bits are transferred on the SDIO pin and the final eight bits are read from the ADRV9008-1, either on the SDO pin in 4-wire mode or on the SDIO pin in 3-wire mode.

JTAG BOUNDARY SCAN

The ADRV9008-1 provides support for the JTAG boundary scan. There are five dual-function pins associated with the JTAG interface. These pins, listed in Figure 5, are used to access the on-chip test access port. To enable the JTAG functionality, set the GPIO_3 pin through the GPIO_0 pin to 1001 and pull the TEST pin high.

POWER SUPPLY SEQUENCE

The ADRV9008-1 requires a specific power-up sequence to avoid undesired power-up currents. In the optimal power-up sequence, the VDDD1P3_DIG supply and the VDDA1P3_x supply (VDDA1P3_x includes all 1.3 V domains) power up together first. If these supplies cannot be powered up simultaneously, then the VDDD1P3_DIG supply must power up first. Power up the VDDA_3P3 supply, the VDDA1P8_x supply, and the VDDA1P3_SER supply after powering up the 1.3 V supplies. The VDD_INTERFACE supply can be powered up at any time. No device damage occurs if this sequence is not followed, but failing to follow this sequence may result in higher than expected power-up currents. Toggle the RESET signal after the power stabilizes, prior to configuration. The power-down sequence is not critical. If a power-down sequence is followed, remove the VDDD1P3_DIG supply last to avoid any back biasing of the digital control lines.

GPIO_x PINS

The ADRV9008-1 provides nineteen 1.8 V to 2.5 V GPIO signals that can be configured for numerous functions. When configured as outputs, certain pins can provide real-time signal information to the BBP, allowing the BBP to determine receiver performance. A pointer register selects the information that is output to these pins. Signals used for manual gain mode, calibration flags, state machine states, and various receiver parameters are among the outputs that can be monitored on these pins. Additionally, certain pins can be configured as inputs and used for various functions, such as setting the receiver gain in real time.

Twelve 3.3 V GPIO_x pins are also included on the device. These pins provide control signals to external components.

AUXILIARY CONVERTERS

AUXADC_x

The ADRV9008-1 contains an auxiliary ADC that is multiplexed to four input pins (AUXADC_x). The auxiliary ADC is 12 bits with an input voltage range of 0.05 V to VDDA_3P3 − 0.05 V. When enabled, the auxiliary ADC is free running. The SPI reads provide the last value latched at the ADC output. The auxiliary ADC can also be multiplexed to a built in, diode-based temperature sensor.

Auxiliary DAC x

The ADRV9008-1 contains 10 identical auxiliary DACs that can be used for bias or other system functionality. The auxiliary DACs are 10 bits, have an output voltage range of approximately 0.7 V to VDDA_3P3 − 0.3 V, and have a current drive of 10 mA.

JESD204B DATA INTERFACE

The digital data interface for the ADRV9008-1 uses JEDEC JESD204B Subclass 1. The serial interface operates at speeds of up to 12.288 Gbps. The benefits of the JESD204B interface include a reduction in required board area for data interface routing, resulting in smaller total system size. Four high speed serial lanes are provided for the receiver. The ADRV9008-1 supports single-lane and dual-lane interfaces and supports fixed and floating point data formats for receiver.

Table 6. Example Receiver Interface Rates (Other Output Rates, Bandwidths, and JESD204B Lanes Also Supported)

		Single-Channel Operation		Dual-Channel Operation	
Bandwidth (MHz)	Output Rate (MSPS)	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes
80	122.88	4915.2	1	9830.4	1
100	153.6	6144	1	12288	1
100	245.76	9830.4	1	9830.4	2
200	245.76	9830.4	1	9830.4	2
200	245.76	4915.2	2	4915.2	4

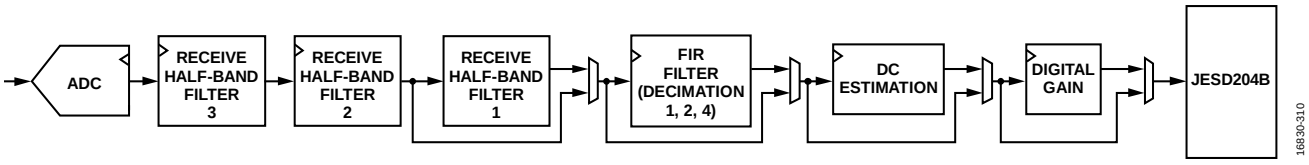


Figure 169. Receiver Datapath Filter Implementation

APPLICATIONS INFORMATION

PCB LAYOUT AND POWER SUPPLY RECOMMENDATIONS

Overview

The ADRV9008-1 is a highly integrated, RF, agile receiver with significant signal conditioning integrated on one chip. Due to the increased complexity of the device and its high pin count, careful PCB layout is important to achieve optimal performance. This data sheet provides a checklist of issues to look for and guidelines on how to optimize the PCB to mitigate performance issues. The goal of this data sheet is to help achieve optimal performance of the ADRV9008-1 while reducing board layout effort. This data sheet assumes that the reader is an experienced analog and RF engineer with an understanding of RF PCB layout and RF transmission lines. This data sheet discusses the following issues and provides guidelines for system designers to achieve optimal performance of the ADRV9008-1:

- PCB material and stackup selection
- Fanout and trace space layout guidelines
- Component placement and routing guidelines
- RF and JESD204B transmission line layout
- Isolation techniques used on the ADRV9008-1W/PCBZ
- Power management considerations
- Unused pin instructions

PCB MATERIAL AND STACKUP SELECTION

Figure 170 shows the PCB stackup used for the ADRV9008-1W/PCBZ. Table 7 and Table 8 list the single-ended and differential impedance for the stackup shown in Figure 170. The dielectric material used on the top and the bottom layers is 8 mil Rogers 4350B. The remaining dielectric layers are FR4-370 HR. The board design uses the Rogers laminate for the top and the bottom layers for the low loss tangent at high frequencies. The ground planes under the Rogers laminate (Layer 2 and Layer 13) are the reference planes for the transmission lines routed on the outer surfaces. These layers are solid copper planes without any splits under the RF traces. Layer 2 and Layer 13 are crucial to maintaining the RF signal integrity and, ultimately, the ADRV9008-1 performance. Layer 3 and Layer 12 are used to route power supply domains. To keep the RF section of the ADRV9008-1 isolated from the fast transients of the digital section, the JESD204B interface lines are routed on Layer 5 and Layer 10. These layers have impedance control set to a 100 Ω differential. The remaining digital lines from ADRV9008-1 are routed on Inner Layer 7 and Inner Layer 8. RF traces on the outer layers must be a controlled impedance for optimal performance of the device. The inner layers in this board use 0.5 ounce copper or 1 ounce copper. The outer layers use 1.5 ounce copper so that the RF traces are less prone to pealing. Ground planes on this board are full copper floods with no splits except for vias, through-hole components, and isolation structures. The ground planes must route entirely to the edge of the PCB under the Surface-Mount Type A (SMA) connectors to maintain signal launch integrity. Power planes can be pulled back from the board edge to decrease the risk of shorting from the board edge.

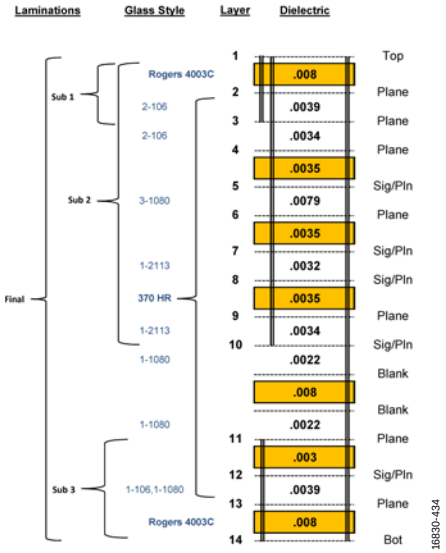


Figure 170. ADRV9008-1W/PCBZ Trace Impedance and Stackup

Table 7. Evaluation Board Single-Ended Impedance and Stackup[1]

Layer	Board Copper (%)	Starting Copper (oz.)	Finished Copper (oz.)	Single-Ended Impedance	Designed Trace Single-Ended (Inches)	Finished Trace Single-Ended (Inches)	Calculated Impedance (Ω)	Single-Ended Reference Layers
1	N/A	0.5	1.71	50 Ω ±10%	0.0155	0.0135	49.97	2
2	65	1	1	N/A	N/A	N/A	N/A	N/A
3	50	0.5	1	N/A	N/A	N/A	N/A	N/A
4	65	1	1	N/A	N/A	N/A	N/A	N/A
5	50	0.5	0.5	50 Ω ±10%	0.0045	0.0042	49.79	4, 6
6	65	1	1	N/A	N/A	N/A	N/A	N/A
7	50	0.5	0.5	50 Ω ±10%	0.0049	0.0039	50.05	6, 9
8	50	0.5	0.5	50 Ω ±10%	0.0049	0.0039	50.05	6, 9
9	65	1	1	N/A	N/A	N/A	N/A	N/A
10	50	0.5	1	50 Ω ±10%	0.0045	0.0039	49.88	9, 11
11	65	0.5	1	N/A	N/A	N/A	N/A	N/A
12	50	1	1	N/A	N/A	N/A	N/A	N/A
13	65	1	1	N/A	N/A	N/A	N/A	N/A
14		0.5	1.64	50 Ω ±10%	0.0155	0.0135	49.97	13

[1] N/A means not applicable.

Table 8. Evaluation Board Differential Impedance and Stackup[1]

Layer	Differential Impedance	Designed Trace (Inches)	Gap Differential for Designed Trace (Inches)	Finished Trace (Inches)	Gap Differential for Finished Trace (Inches)	Calculated Impedance (Ω)	Differential Reference Layers
1	100 Ω ± 10%	0.008	0.006	0.007	0.007	99.55	2
	50 Ω ± 10%	0.0032	0.004	0.0304	0.0056	50.11	2
2	N/A[1]	N/A	N/A	N/A	N/A	N/A	N/A
3	N/A	N/A	N/A	N/A	N/A	N/A	N/A
4	N/A	N/A	N/A	N/A	N/A	N/A	N/A
5	100 Ω ±10%	0.0036	0.0064	0.0034	0.0065	99.95	4, 6
6	N/A	N/A	N/A	N/A	N/A	N/A	N/A
7	100 Ω ±10%	0.0036	0.0064	0.0034	0.0066	100.51	6, 9
8	100 Ω ±10%	0.0038	0.0062	0.0034	0.0066	100.51	6, 9
9	N/A	N/A	N/A	N/A	N/A	N/A	N/A
10	100 Ω ±10%	0.0036	0.0064	0.003	0.007	100.80	9, 11
11	N/A	N/A	N/A	N/A	N/A	N/A	N/A
12	N/A	N/A	N/A	N/A	N/A	N/A	N/A
13	100 Ω ±10%	0.008	0.006	0.007	0.007	99.55	13
14	50 Ω ±10%	0.032	N/A	0.004	N/A	50.11	13

[1] N/A means not applicable.

FANOUT AND TRACE SPACE GUIDELINES

The ADRV9008-1 uses a 196-ball chip scale ball grid array (CSP_BGA), 12 mm × 12 mm package. The pitch between the pins is 0.8 mm. This small pitch makes it impractical to route all signals on a single layer. RF pins are placed on the outer edges of the ADRV9008-1 package. The location of the pins helps route the critical signals without a fanout via. Each digital signal is routed from the BGA pad using a 4.5 mil trace. The trace is connected to the BGA using a via in the pad structure. The signals are buried in the inner layers of the board for routing to other parts of the system.

The JESD204B interface signals are routed on two signal layers that use impedance control (Layer 5 and Layer 10). The spacing between the BGA pads is 17.5 mil. After the signal is on the inner layers, a 3.6 mil trace (50 Ω) connects the JESD204B signal to the field programmable gate array (FPGA) mezzanine card (FMC) connector. The recommended BGA land pad size is 15 mil.

Figure 171 shows the fanout scheme of the ADRV9008-1W/PCBZ. As mentioned before, the ADRV9008-1W/PCBZ uses a via in the pad technique. This routing approach can be used for the ADRV9008-1 if there are no issues with manufacturing capabilities.

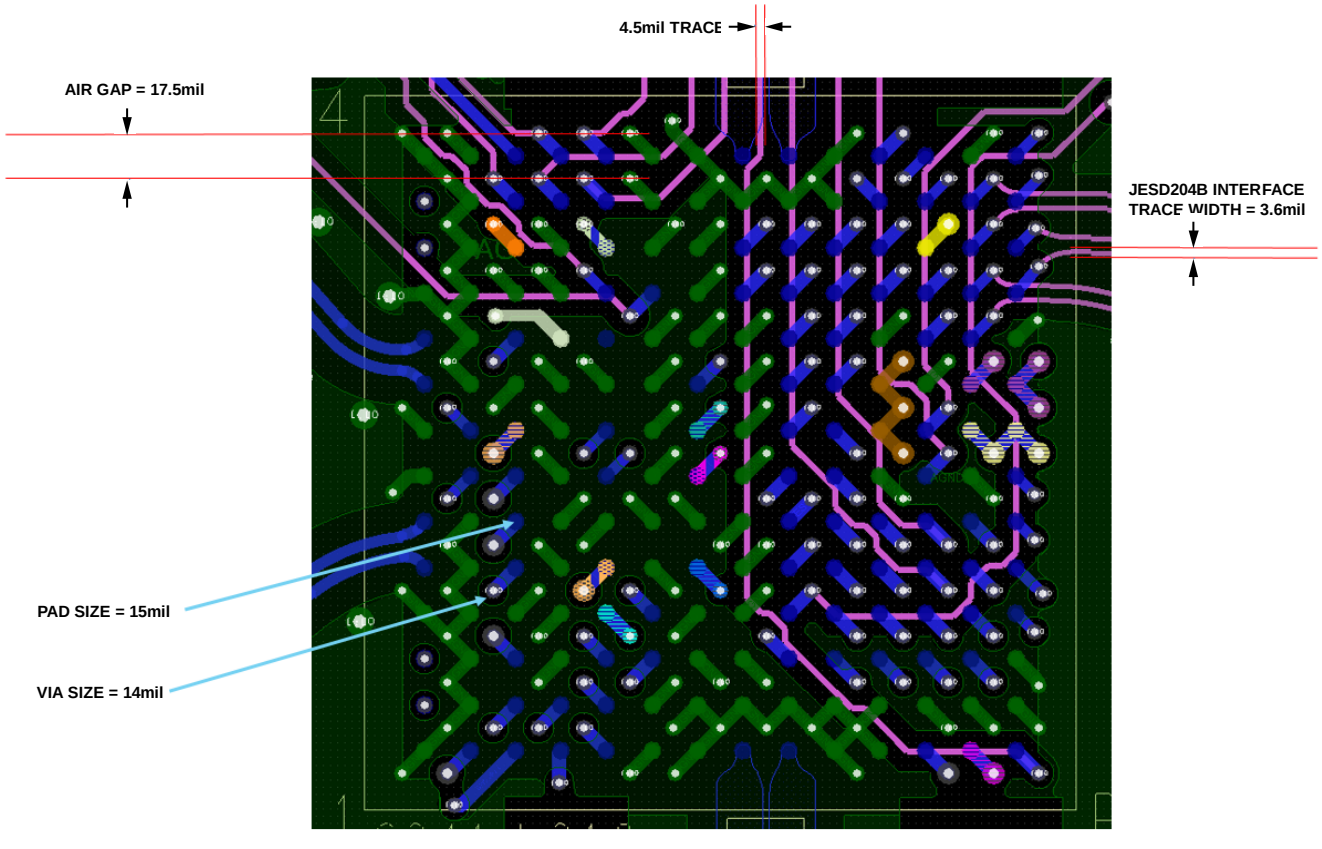


Figure 171. Trace Fanout Scheme on the ADRV9008-1W/PCBZ (PCB Layer Top and Layer 5 Enabled)

COMPONENT PLACEMENT AND ROUTING GUIDELINES

The ADRV9008-1 receiver requires few external components to function, but those that are used require careful placement and routing to optimize performance. This section provides a checklist for properly placing and routing critical signals and components.

Signals with Highest Routing Priority

RF lines and JESD204B interface signals are the signals that are most critical and must be routed with the highest priority.

Figure 170 shows the general directions in which each of the signals must be routed so that they can be properly isolated from noisy signals.

The receiver baluns and the matching circuits affect the overall RF performance of the ADRV9008-1 receiver. Make every effort to optimize the component selection and placement to avoid performance degradation. The RF Routing Guidelines section describes proper matching circuit placement and routing in more detail. Refer to the RF Port Interface Information section for more information.

To achieve the desired level of isolation between RF signal paths, use the technique described in the Isolation Techniques Used on the ADRV9008-1W/PCBZ section in customer designs.

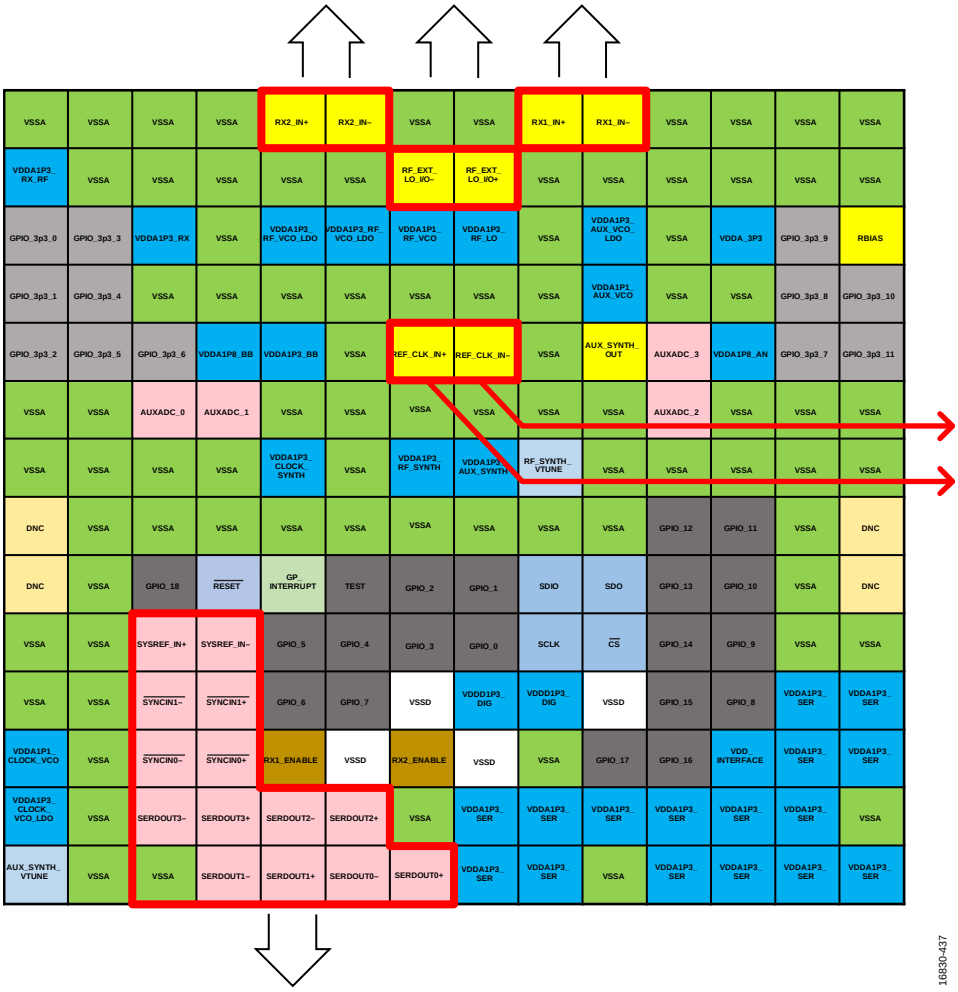


Figure 172. RF Input/Output, REF_CLK_IN±, and JESD204B Signal Routing Guidelines

Figure 173 shows placement for ac coupling capacitors and a 100 Ω termination resistor near the ADRV9008-1 REF_CLK_IN± pins. Shield the traces with ground flooding that is surrounded with vias staggered along the edge of the trace pair. The trace pair creates a shielded channel that shields the reference clock from any interference from other signals. Refer to the ADRV9008-1W/PCBZ layout and board support files included with the evaluation board software for exact details.

Route the JESD204B interface at the beginning of the PCB design and with the same priority as the RF signals.

The JESD204B Trace Routing Recommendations section outlines recommendations for JESD204B interface routing. Provide appropriate isolation between interface differential pairs. The Isolation Between JESD204B Lines section provides guidelines for optimizing isolation.

The RF_EXT_LO_I/O– pin (B7) and RF_EXT_LO_I/O+ pin (B8) on the ADRV9008-1 are internally dc biased. If an external LO is used, connect the LO to the device via ac coupling capacitors.

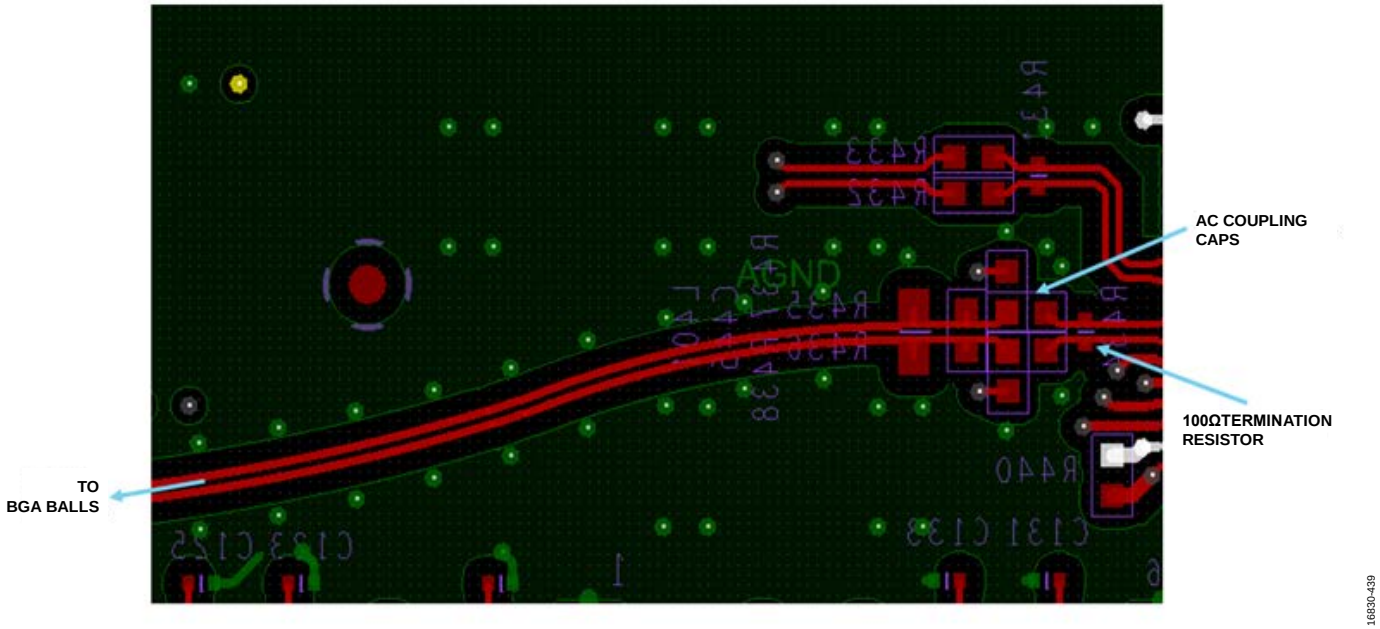


Figure 173. REF_CLK_IN± Routing Recommendation

Signals with Second Routing Priority

Power supply quality has a direct impact on overall system performance. To achieve optimal performance, follow recommendations for ADRV9008-1 power supply routing. The following recommendations outline how to route different power domains that can be connected together directly and to the same supply, but are separated by a 0 Ω placeholder resistor or ferrite bead.

When the recommendation is to use a trace to connect power to a particular domain, ensure that this trace is surrounded by ground.

Figure 174 shows an example of such traces routed on the ADRV9008-1W/PCBZ on Layer 12. Each trace is separated from any other signal by the ground plane and vias. Separating the traces from other signals is essential to providing necessary isolation between the ADRV9008-1 power domains.

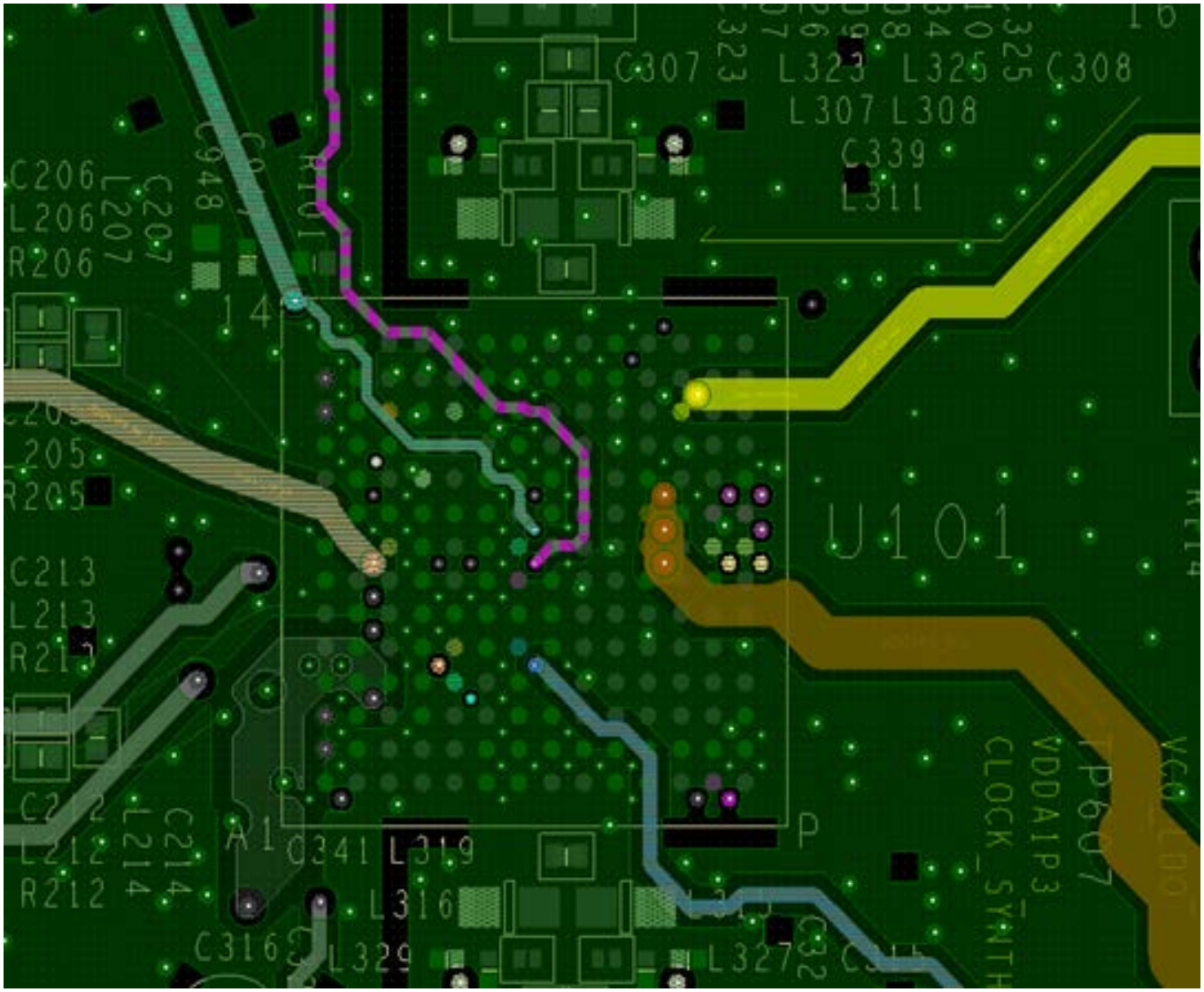


Figure 174. Layout Example of Power Supply Domains Routed with Ground Shielding (Layer 12 to Power)

Each power supply pin requires a 0.1 µF bypass capacitor near the pin at a minimum. Place the ground side of the bypass capacitor so that ground currents flow away from other power pins and the bypass capacitors.

For domains shown in Figure 175, like the domains powered through a 0 Ω placeholder resistor or ferrite bead (FB), place the 0 Ω placeholder resistors or ferrite beads further away from the device. Space 0 Ω placeholder resistors or ferrite beads apart from each other to ensure the electric fields on the ferrite beads do not influence each other. Figure 176 shows an example of how the ferrite beads, reservoir capacitors, and decoupling capacitors are placed. The recommendation is to connect a ferrite bead between a power plane and the ADRV9008-1 at a distance away from the device. The ferrite bead and the reservoir capacitor provide stable voltage to the ADRV9008-1 during operation by isolating the pin or pins that the network is connected to from the power plane. Then, shield this trace with ground and provide power to the power pins on the ADRV9008-1. Place a 100 nF capacitor near the power supply pin with the ground side of the bypass capacitor placed so that ground currents flow away from other power pins and the bypass capacitors.

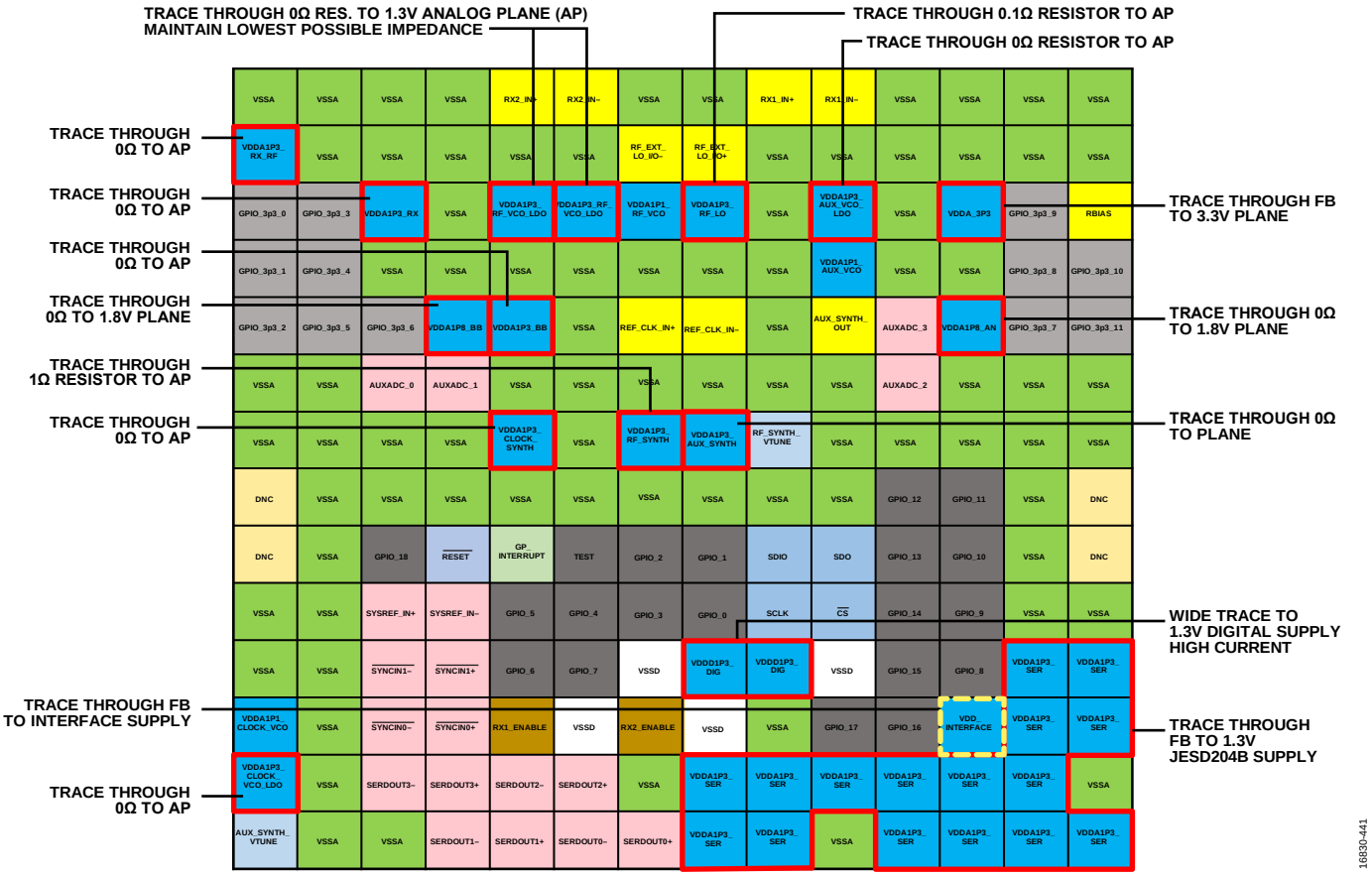


Figure 175. Power Supply Domains Interconnection Guidelines

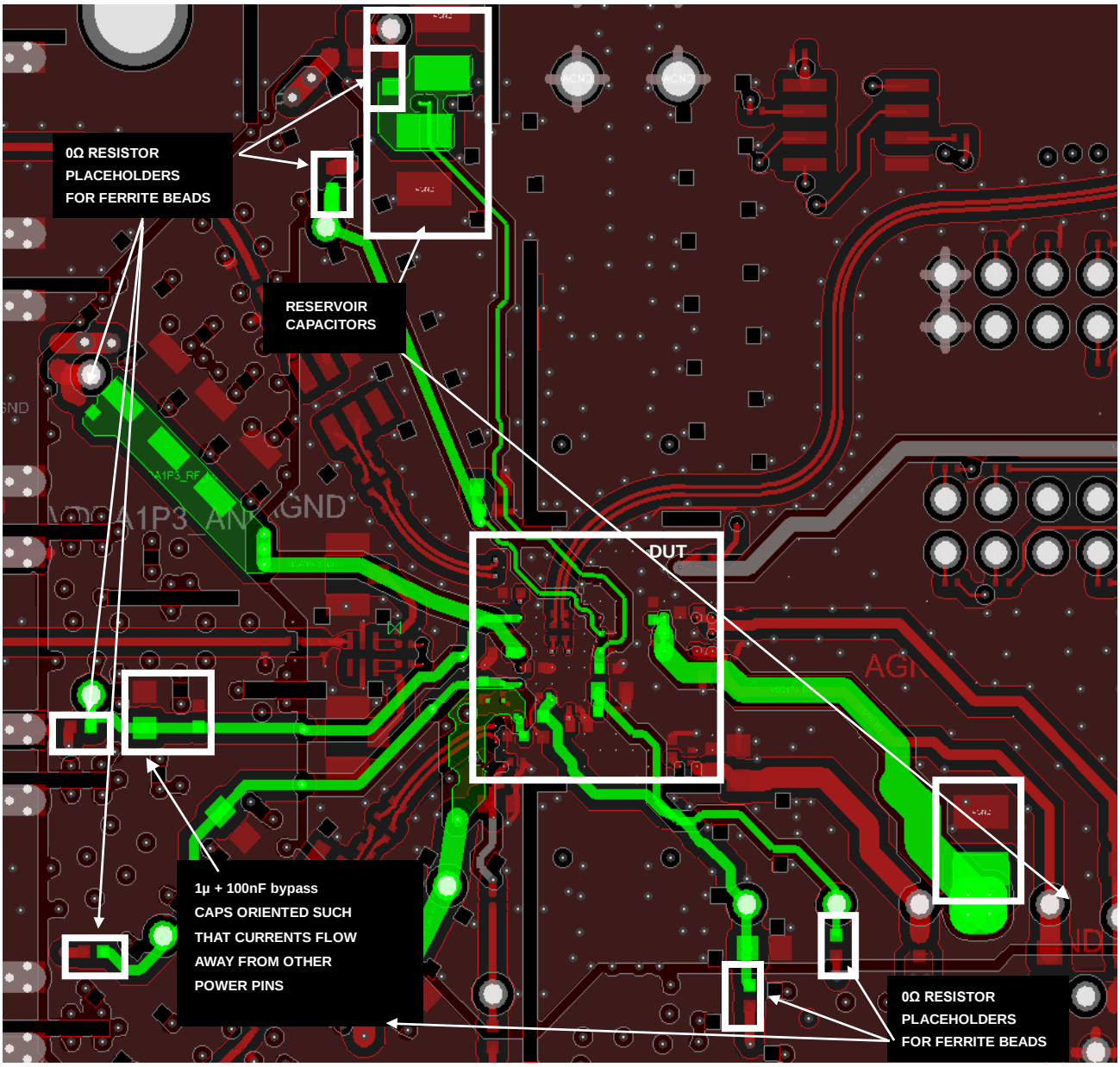


Figure 176. Placement Example of 0 Ω Resistor Placeholders for Ferrite Beads, Reservoir and Bypass Capacitors on the ADRV9008-1W/PCBZ (Layer 12 to Power and Bottom)

Signals with Lowest Routing Priority

As a last step while designing the PCB layout, route the signals shown in Figure 177. The following list outlines the recommended order of signal routing:

1. Use ceramic 1 µF bypass capacitors at the VDDA1P1_RF_VCO, VDDA1P1_AUX_VCO, and VDDA1P1_CLOCK_VCO pins. Place these pins as close as possible to the ADRV9008-1 device with the ground side of the bypass capacitor placed so that ground currents flow away from other power pins and the bypass capacitors, if possible.
2. Connect a 14.3 kΩ resistor to the RBIAS pin (C14). This resistor must have a 1% tolerance.
3. Pull the TEST pin (J6) to ground for normal operation. The device supports JTAG boundary scan, and this pin is used to access that function. Refer to the JTAG Boundary Scan section for JTAG boundary scan information.
4. Pull the $\overline{\text{RESET}}$ pin (J4) high with a 10 kΩ resistor to VDD_INTERFACE for normal operation. To reset the device, drive the $\overline{\text{RESET}}$ pin low.

When routing analog signals such as GPIO_3p3_x or AUXADC_x, it is recommended to route the signals away from the digital section (Row H through Row P). Do not cross the analog section of the ADRV9008-1, highlighted by a red dotted line in Figure 177, by any digital signal routing.

When routing digital signals from Row H and below, it is important to route the signals away from the analog section (Row A through Row G). Do not cross the analog section of the ADRV9008-1, highlighted by a red dotted line in Figure 177, by any digital signal routing.

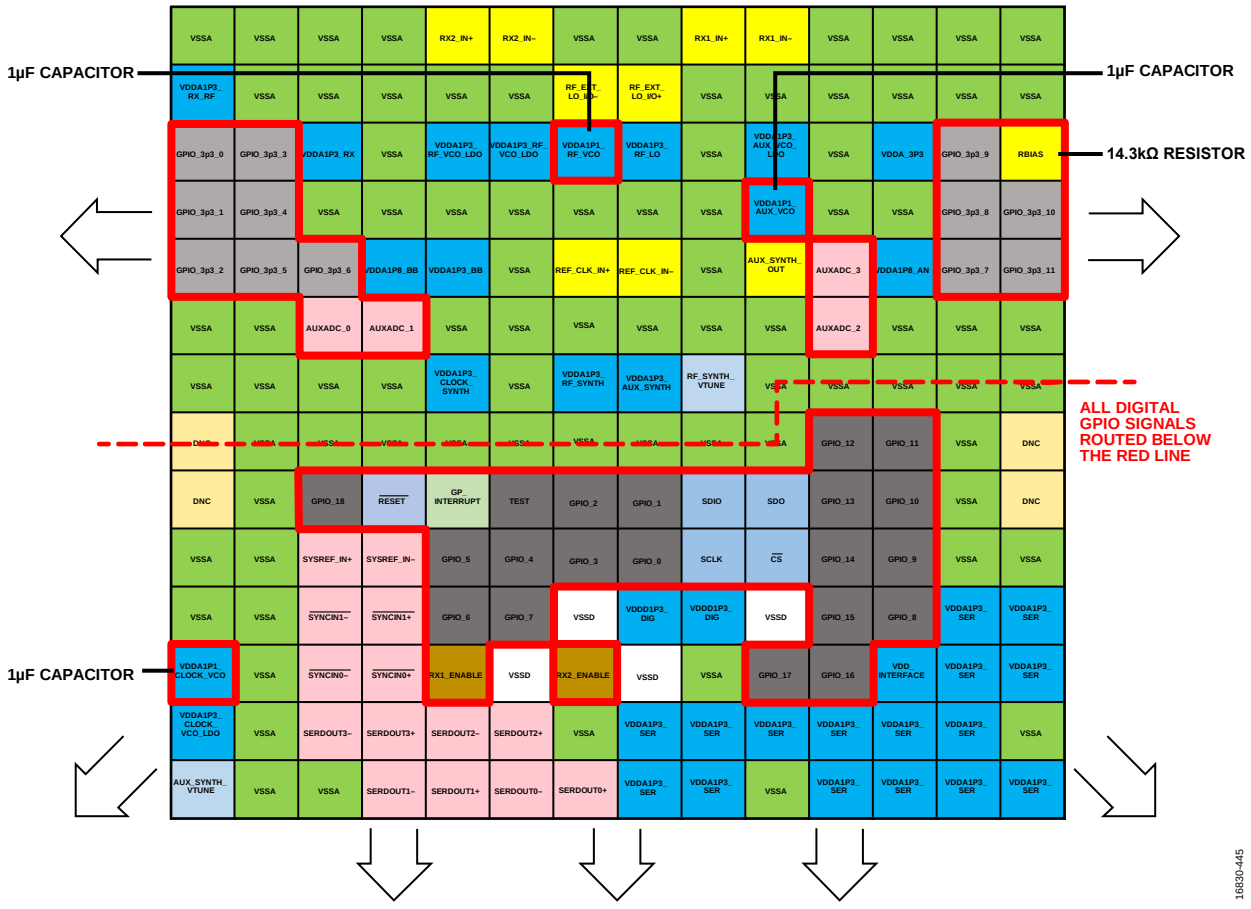


Figure 177. AUXADC_x, Analog, and Digital GPIO Signals Routing Guidelines

RF AND JESD204B TRANSMISSION LINE LAYOUT

RF Routing Guidelines

The ADRV9008-1W/PCBZ uses microstrip type lines for receiver traces. In general, Analog Devices does not recommend using vias to route RF traces unless a direct line route is not possible. Differential lines from the balun to the receiver pins must be as short as possible. Keep the length of the single-ended transmission line short to minimize the effects of parasitic coupling. It is important to note that these traces are the most critical when optimizing performance and are, therefore, routed before any other routing. These traces have the highest priority if trade-offs are needed.

Figure 178 shows pi matching networks on the single-ended side of the baluns. The receiver front end is dc biased internally. Therefore, the differential side of the balun is ac-coupled. The system designer can optimize the RF performance with a proper selection of the balun, matching components, and ac coupling capacitors. The external LO traces and the REF_CLK_IN± traces may also require matching components to ensure optimal performance.

All the RF signals mentioned previously must have a solid ground reference under each trace. Do not run any of the critical traces over a section of the reference plane that is discontinuous. The ground flood on the reference layer must extend all the way to the edge of the board. This flood length ensures signal integrity for the SMA launch when an edge launch connector is used.

Refer to the RF Port Interface Information section for more information on RF matching recommendations for the ADRV9008-1.

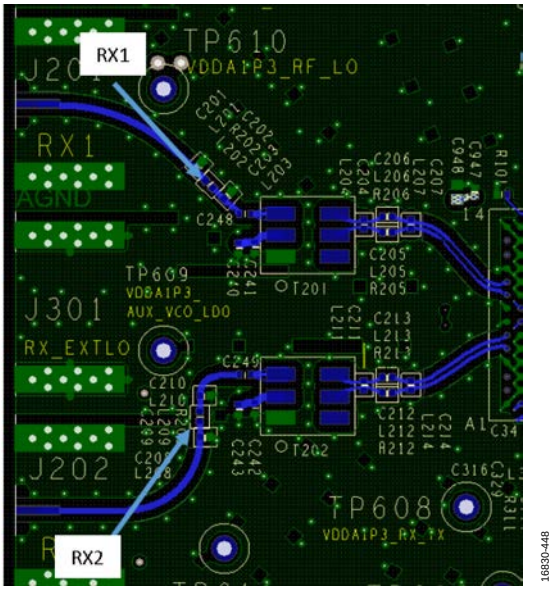


Figure 178. Pi Network Matching Components Available on Different RF Nets

JESD204B Trace Routing Recommendations

The ADRV9008-1 receiver uses the JESD204B, high speed serial interface. To ensure optimal performance of this interface, keep the differential traces as short as possible by placing the ADRV9008-1 as close as possible to the FPGA or BBP, and route the traces directly between the devices. Use a PCB material with a low dielectric constant (< 4) to minimize loss. For distances greater than 6 inches, use a premium PCB material, such as RO4350B or RO4003C.

Routing Recommendations

Route the differential pairs on a single plane using a solid ground plane as a reference on the layers above and/or below these traces.

All JESD204B lane traces must be impedance controlled to achieve 50 Ω to ground. It is recommended that the differential pair be coplanar and loosely coupled. An example of a typical configuration is 5 mil trace width and 15 mil edge to edge spacing, with the trace width maximized as shown in Figure 179.

Match trace widths with pin and ball widths as closely as possible while maintaining impedance control. If possible, use 1 oz. copper trace widths of at least 8 mil (200 µm). The coupling capacitor pad size must match JESD204B lane trace widths as closely as possible. If trace width does not match pad size, use a smooth transition between different widths.

The pad area for all connector and passive component choices must be minimized due to a capacitive plate effect that leads to problems with signal integrity.

Reference planes for impedance controlled signals must not be segmented or broken for the entire length of a trace.

The REF_CLK_IN± signal trace and the SYSREF signal trace are impedance controlled for character impedance (Z_O) = 50 Ω.

Stripline Transmission Lines vs. Microstrip Transmission Lines

Stripline trasmission lines have less signal loss and emit less electromagnetic interference than microstrip trasmission lines. However, stripline trasmission lines require the use of vias that add line inductance, increasing the difficulty of controlling the impedance.

Microstrip trasmission lines are easier to implement if the component placement and density allow routing on the top layer. Microstrip trasmission lines make controlling the impedance easier.

If the top layer of the PCB is used by other circuits or signals, or if the advantages of stripline are more desirable over the advantages of microstrip, follow these recommendations:

- Minimize the number of vias.
- Use blind vias where possible to eliminate via stub effects, and use micro vias to minimize via inductance.
- When using standard vias, use a maximum via length to minimize the stub size. For example, on an 8-layer board, use Layer 7 for the stripline pair.
- Place a pair of ground vias near each via pair to minimize the impedance discontinuity.

Route the JESD204B lines on the top side of the board as a differential 100 Ω pair (microstrip). For the ADRV9008-1W/PCBZ, the JESD204B differential signals are routed on inner layers of the board (Layer 5 and Layer 10) as differential 100 Ω pairs (stripline). To minimize potential coupling, these signals are placed on an inner layer using a via embedded in the component footprint pad where the ball connects to the PCB. The ac coupling capacitors (100 nF) on these signals are placed near the connector and away from the chip to minimize coupling. The JESD204B interface can operate at frequencies of up to 12 GHz. Ensure that signal integrity from the chip to the connector is maintained.

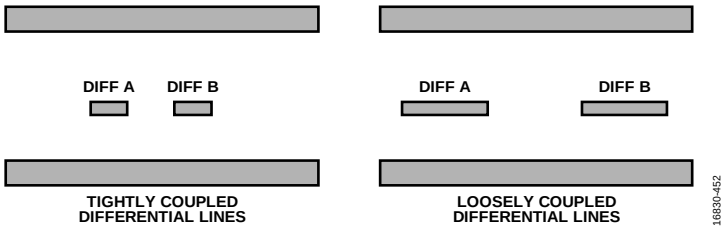


Figure 179. Routing JESD204B, Diff A and Diff B Correspond to Differential Positive Signals or Negative Signals (One Differential Pair)

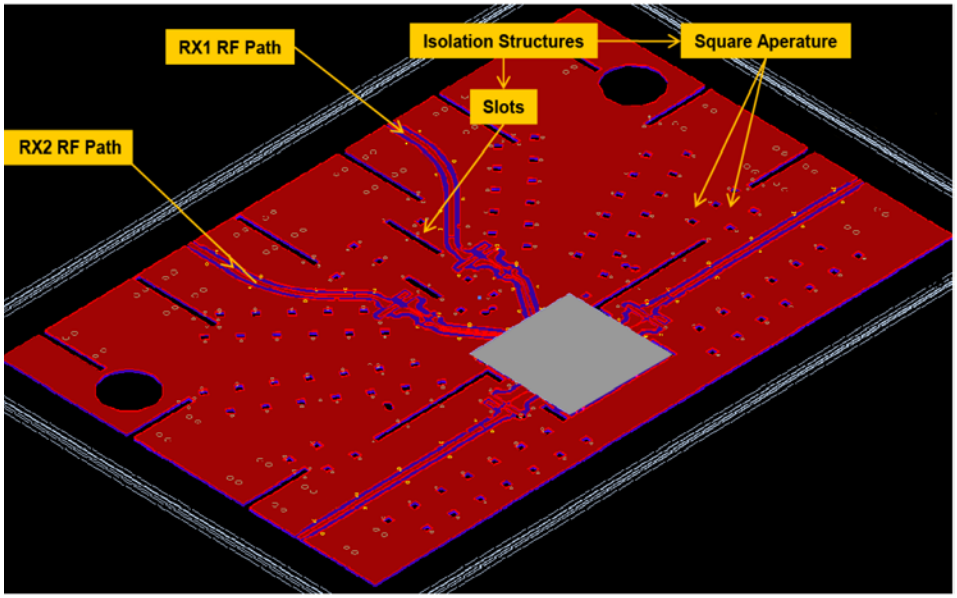


Figure 180. Isolation Structures on the ADRV9008-1W-PCBZ

ISOLATION TECHNIQUES USED ON THE ADRV9008-1W/PCBZ

Isolation Goals

Significant isolation challenges were overcome in designing the ADRV9008-1W/PCBZ. The following isolation requirement is used to accurately evaluate the ADRV9008-1 receiver performance: receiver to receiver, 65 dB out to 6 GHz.

To meet these isolation goals with significant margin, isolation structures are introduced.

Figure 180 shows the isolation structures used on the ADRV9008-1W/PCBZ. These structures consist of a combination of slots and square apertures. These structures are present on every copper layer of the PCB stack. The advantage of using square apertures is that signals can be routed between the openings without affecting the isolation benefits of the array of apertures. When using these isolation structures, make sure to place ground vias around the slots and apertures.

Figure 181 outlines the methodology used on the ADRV9008-1W/PCBZ. When using slots, ground vias must be placed at the ends of the slots and along the sides of the slots. When using square apertures, at least one single ground via must be placed adjacent to each square. These vias must be through-hole vias from the top to the bottom layer. The function of these vias is to steer return current to the ground planes near the apertures.

For accurate slot spacing and square apertures layout, use simulation software when designing a PCB for the ADRV9008-1 receivers. Spacing between square apertures must be no more than 1/10 of a wavelength. Calculate the wavelength using Equation 1:

$$Wavelength\ (\text{m}) = \frac{300}{Frequency\ (\text{MHz}) \times \sqrt{E_R}} \quad (1)$$

where E_R is the dielectric constant of the isolator material. For RO4003C material, microstrip structure (+ air) E_R = 2.8. For FR4-370HR material, stripline structure E_R = 4.1.

For example, if the maximum RF signal frequency is 6 GHz, and E_R = 2.8 for RO4003C material, microstrip structure (+ air), the minimum wavelength is approximately 29.8 mm.

To follow the 1/10 wavelength spacing rule, square aperture spacing must be 2.98 mm or less.

Isolation Between JESD204B Lines

The JESD204B interface uses eight line pairs that can operate at speeds of up to 12 GHz. When configuring the PCB layout, ensure that these lines are routed according to the rules outlined in the JESD204B Trace Routing Recommendations section. In addition, use isolation techniques to prevent crosstalk between different JESD204B lane pairs.

Figure 182 shows a technique used on the ADRV9008-1W/PCBZ that involves via fencing. Placing ground vias around each JESD204B pair provides isolation and decreases crosstalk. The spacing between vias is 1.2 mm.

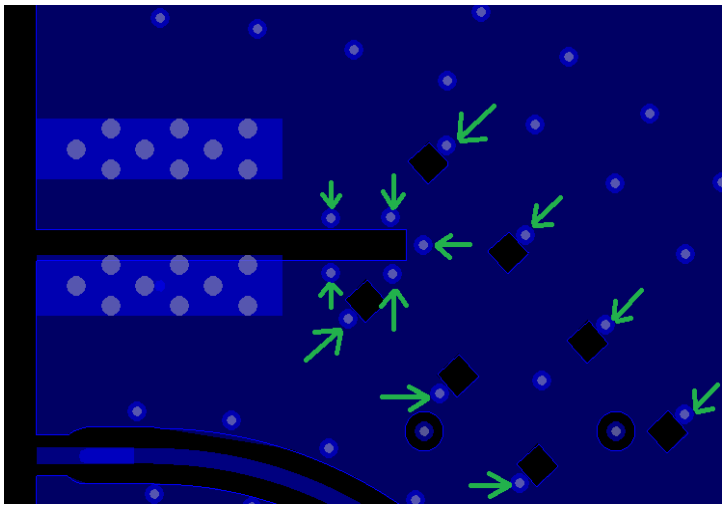


Figure 181. Current Steering Vias Placed Next to Isolation Structures

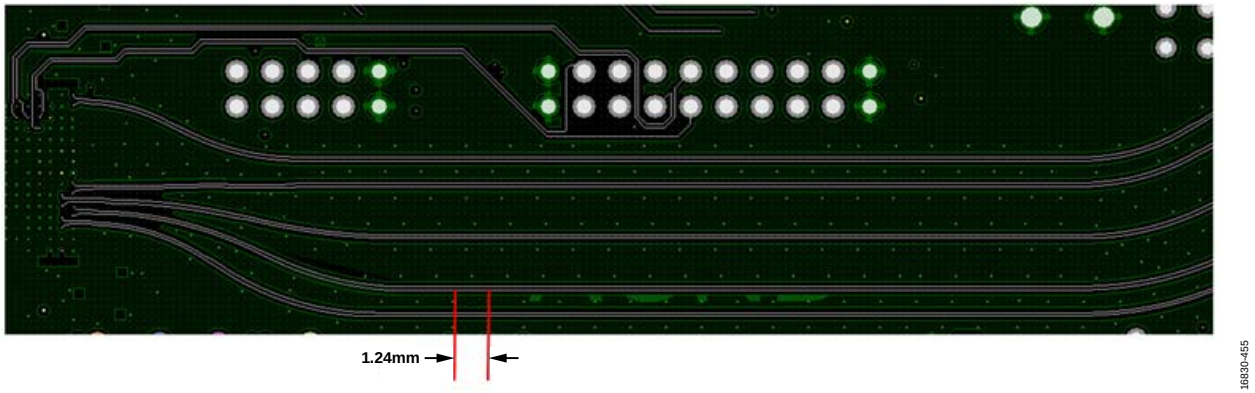


Figure 182. Via Fencing Around JESD204B Lines, PCB Layer 10

Figure 182 shows the rule provided in Equation 1. JESD204B lines are routed on Layer 5 and Layer 10 so that the lines use stripline structures. The dielectric material used in the inner layers of the ADRV9008-1W/PCBZ PCB is FR4-370HR.

For accurate spacing of the JESD204B fencing vias, use layout simulation software. Input the following data into Equation 1 to calculate the wavelength and square aperture spacing:

- Maximum JESD204B signal frequency is approximately 12 GHz.
- For FR4-370HR material, stripline structure, E_R = 4.1, the minimum wavelength is approximately 12.4 mm.

To follow the 1/10 wavelength spacing rule, spacing between vias must be 1.24 mm or less. The minimum spacing recommendation according to transmission line theory is 1/4 wavelength.

RF PORT INTERFACE INFORMATION

This section details the RF receiver interfaces for optimal device performance. This section also includes data for the anticipated ADRV9008-1 RF port impedance values and examples of impedance matching networks used in the evaluation platform. This section also provides information on board layout techniques and balun selection guidelines.

The ADRV9008-1 is a highly integrated receiver device. External impedance matching networks are required on the receiver port to achieve performance levels indicated in the Specifications section.

Analog Devices recommends the use of simulation tools in the design and optimization of impedance matching networks. To achieve the closest match between computer simulated results and measured results, accurate models of the board environment, SMD components (including baluns and filters), and ADRV9008-1 port impedances are required.

RF Port Impedance Data

This section provides the port impedance data for the receivers in the ADRV9008-1 integrated receiver. Note the following:

- Z_O is defined as 50 Ω.
- The ADRV9008-1 ball pads are the reference plane for this data.
- Single-ended mode port impedance data is not available. However, a rough assessment is possible by taking the differential mode port impedance data and dividing both the real and imaginary components by 2.

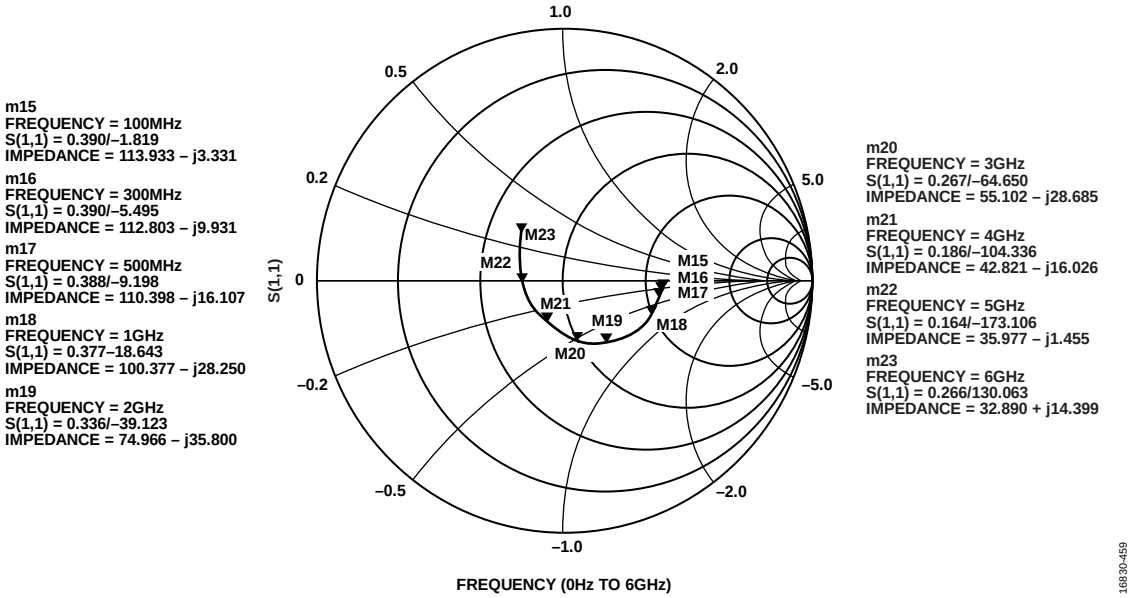


Figure 183. Receiver 1 and Receiver 2 SEDZ and Parallel Equivalent Differential Impedance (PEDZ) Data

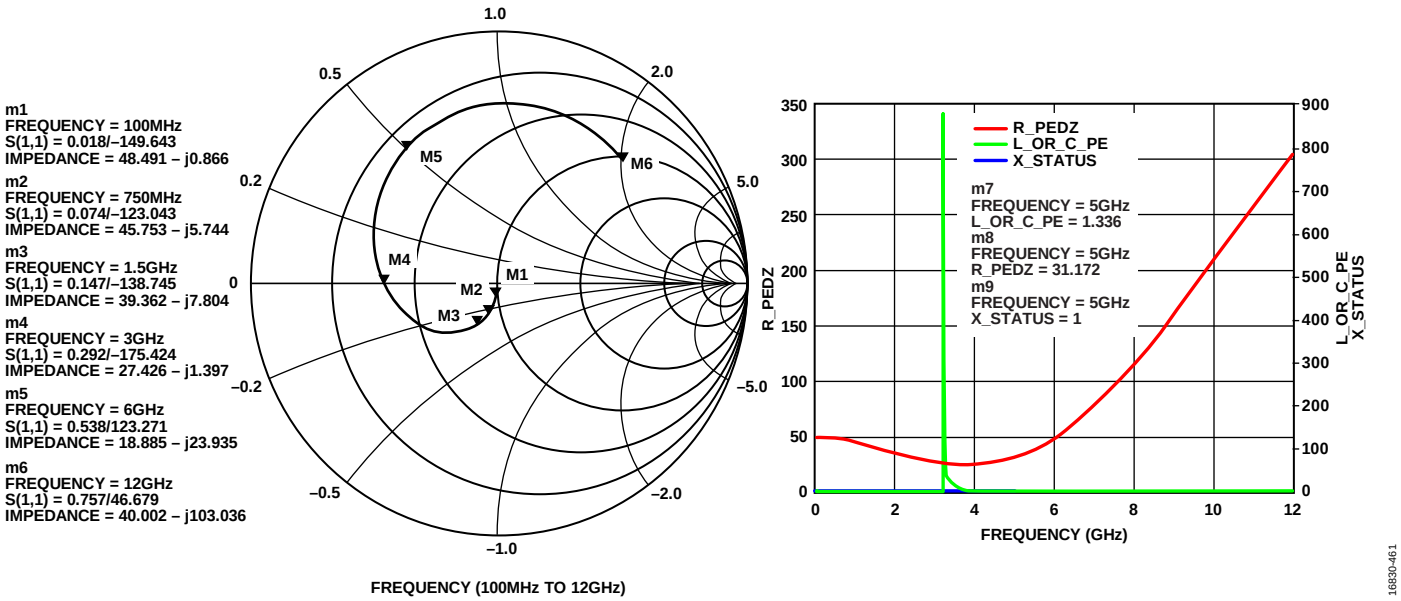


Figure 184. RF_EXT_LO_I/O± SEDZ and PEDZ Data

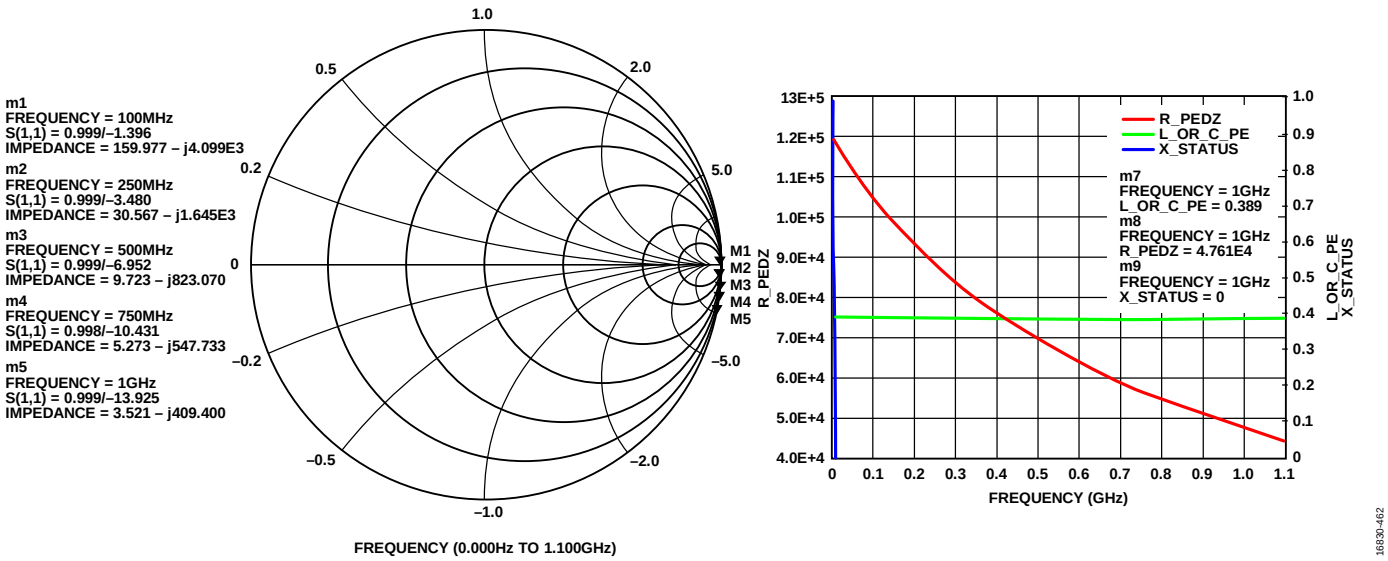


Figure 185. REF_CLK_IN± SEDZ and PEDZ Data—On Average, the Real Part of Parallel Equivalent Differential Impedance (R_P) = ~70 kΩ

Advanced Design System (ADS) Setup Using the DataAccessComponent and SEDZ File

Analog Devices supplies the port impedance as an **.s1p** file that can be downloaded from the ADRV9008-1 product page. This format allows simple interfacing to the ADS by using the data access component. In Figure 186, Term1 is the single-ended input or output, and Term2 is the differential input or output RF port on the ADRV9008-1. The pi on the single-ended side and the differential pi configuration on the differential side allow maximum flexibility in designing matching circuits. The pi configuration is suggested for all design layouts because the pi configuration can step the impedance up or down as needed with appropriate component population.

The mechanics of setting up a simulation for impedance measurement and impedance matching is as follows:

1. The data access component block reads the RF port **.s1p** file. This file is the device RF port reflection coefficient.
2. The two equations convert the RF port reflection coefficient to a complex impedance. The result is the RX_SEDZ variable.
3. The RF port calculated complex impedance (RX_SEDZ) is used to define the Term2 impedance.
4. Term2 is used in a differential mode, and Term1 is used in a single-ended mode.

Setting up the simulation this way allows one to measure the input reflection (S11), output reflection (S22), and through reflection (S21) of the three port system without complex math operations within the display page.

For the highest accuracy, the electromagnetic momentum (EM) modeling result of the PCB artwork and S parameters (S11, S22, and S21) of the matching components and balun must be used in the simulations.

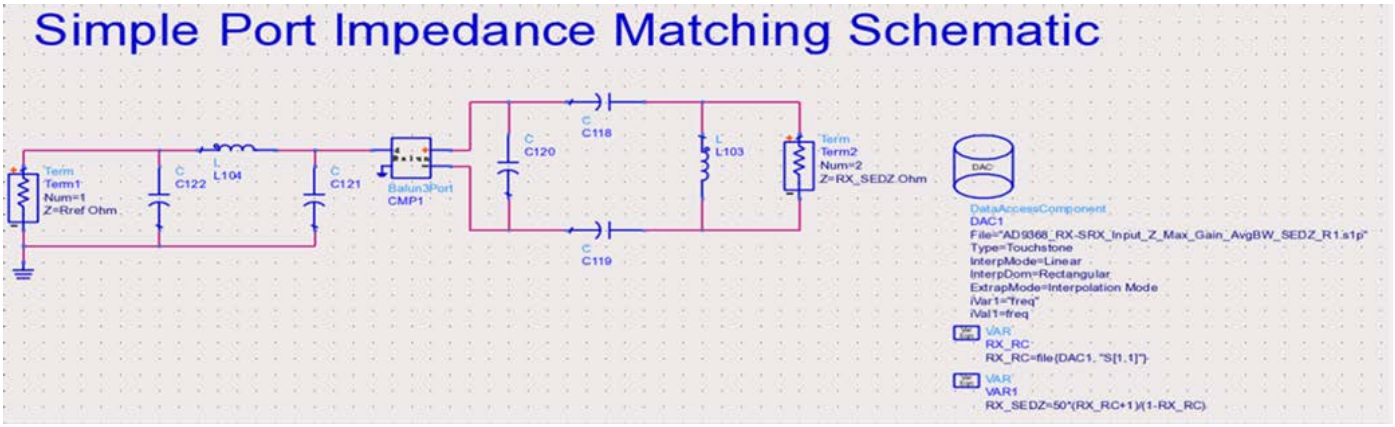


*Figure 186 Simulation Setup in ADS with SEDZ **.s1p** Files and DataAccessComponent*

General Receiver Path Interface

The ADRV9008-1 receivers can support up to a 200 MHz bandwidth.

The ADRV9008-1 receivers support a wide range of operation frequencies. In the case of the receiver channels, the differential signals interface to an integrated mixer. The mixer input pins have a dc bias of approximately 0.7 V and may need to be ac-coupled, depending on the common-mode voltage level of the external circuit.

Important considerations for the receiver port interface are as follows:

- The device to be interfaced (filter, balun, transmit/receive (T/R) switch, external low noise amplifier (LNA), external PA, and so on).
- The receiver maximum safe input power is 23 dBm (peak).
- The receiver optimum dc bias voltage is 0.7 V bias to ground.
- The board design (reference planes, transmission lines, impedance matching, and so on).

Figure 187 and Figure 188 show possible differential receiver port interface circuits. The options in Figure 187 and Figure 188 are valid for all receiver inputs operating in differential mode, though only the Receiver 1 signal names are indicated. Impedance matching may be necessary to obtain data sheet performance levels.

Given wide RF bandwidth applications, SMD balun devices function well. Decent loss and differential balance are available in a relatively small (0603, 0805) package.

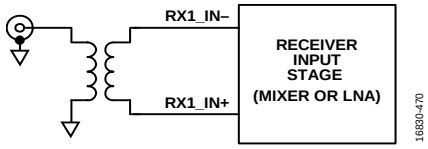


Figure 187. Differential Receiver Interface Using a Transformer

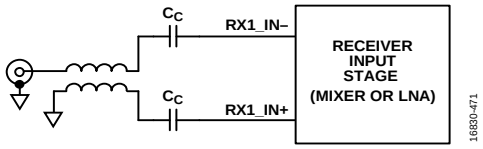


Figure 188. Differential Receiver Interface Using a Transmission Line Balun

Impedance Matching Network Examples

Impedance matching networks are required to achieve the ADRV9008-1 data sheet performance levels. This section provides a description of the matching network topology and components used on the ADRV9008-1W/PCBZ.

Device models, board models, and balun and SMD component models are required to build an accurate system level simulation. The board layout model can be obtained from an EM simulator. The balun and SMD component models can be obtained from the device vendors or built locally. Contact Analog Devices applications engineering for ADRV9008-1 modeling details.

The impedance matching network provided in this section is not evaluated in terms of mean time to failure (MTTF) in high volume production. Consult with component vendors for long-term reliability concerns. Consult with balun vendors to determine appropriate conditions for dc biasing.

Figure 190 shows three elements in parallel marked do not install (DNI). However, only one set of SMD component pads is placed on the board. For example, the R202, L202, and C202 components only have one set of SMD pads for one SMD component. Figure 190 shows that, in a generic port impedance matching network, the shunt or series elements may be a resistor, inductor, or capacitor.

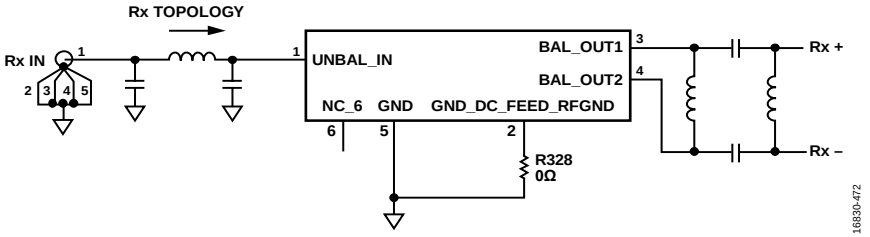


Figure 189. Impedance Matching Topology

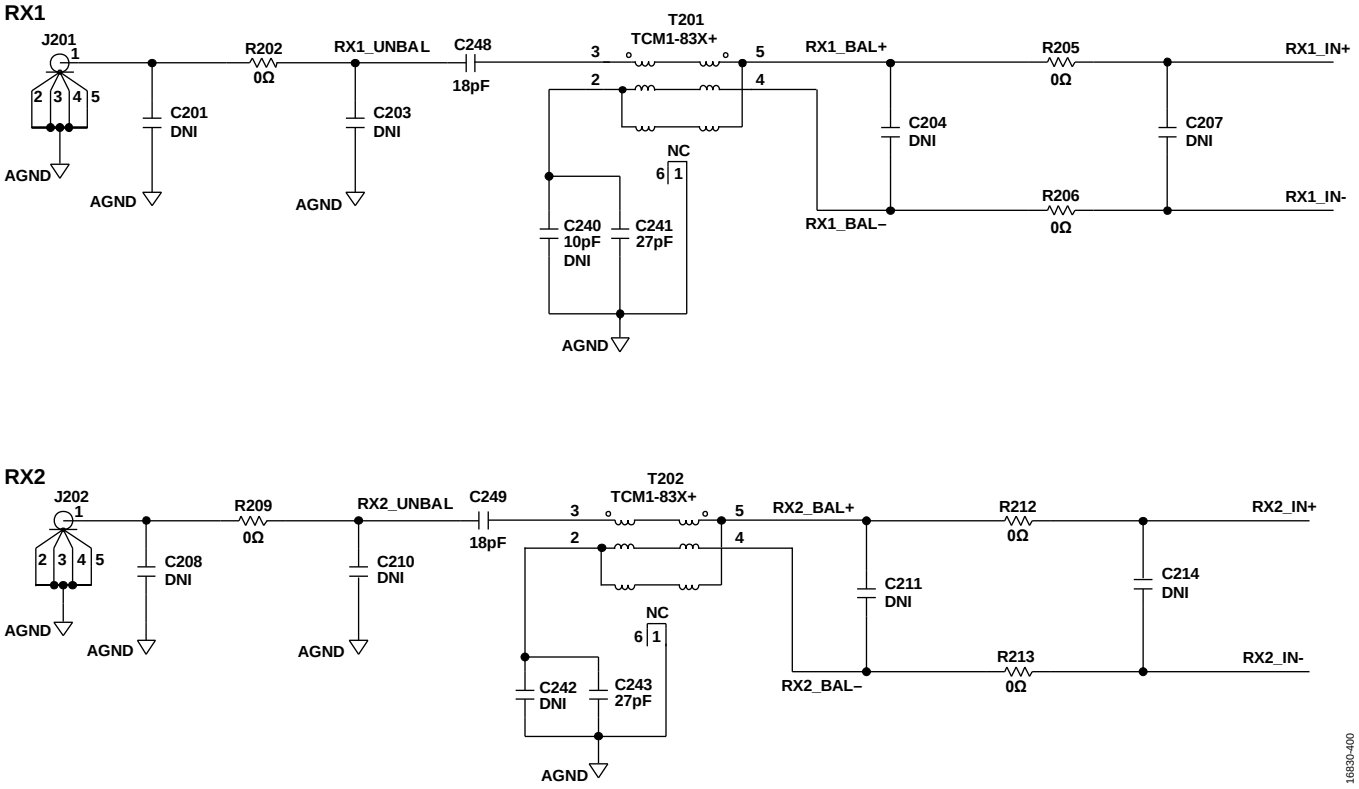


Figure 190. Receiver 1 (RX1) and Receiver 2 (RX2) Generic Matching Network Topology

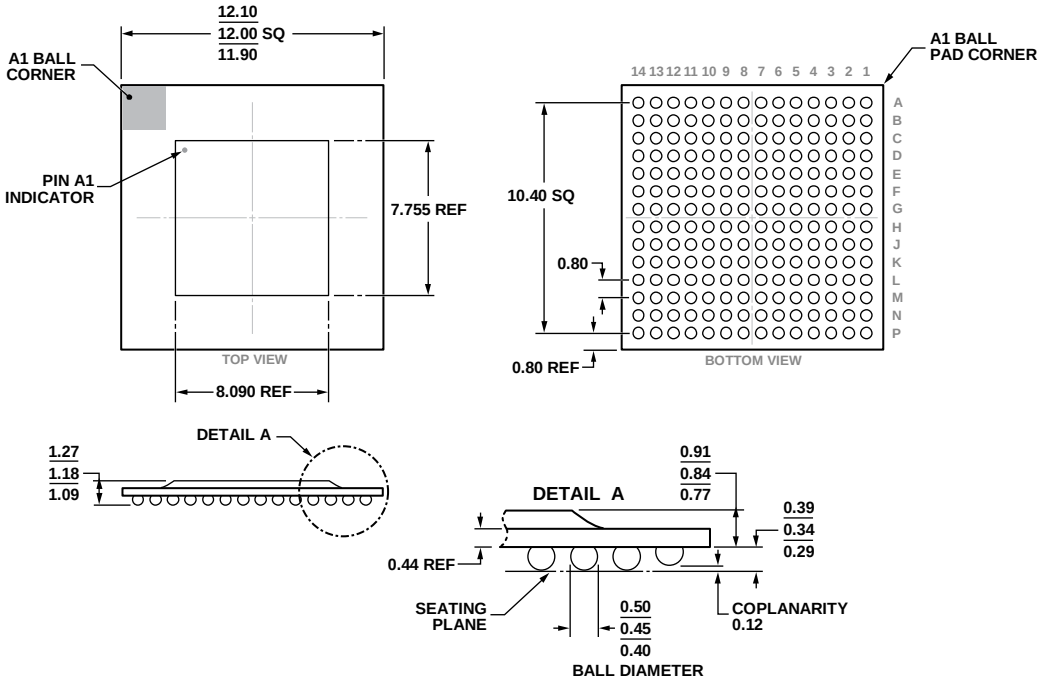
Table 9 and shows the selected balun and component values used for three matching network sets. Refer to the ADRV9008-1 schematics for a wideband matching example that operates across the entire device frequency range with somewhat reduced performance.

The RF matching used in the ADRV9008-1W/PCBZ allows the ADRV9008-1 to operate across the entire chip frequency range with slightly reduced performance.

Table 9. Receiver 1 and Receiver 2 Evaluation Board Matching Components for Frequency Band 75 MHz to 6000 MHz

Component	Value
C201, C208	Do not install (DNI)
R202, R209	0 Ω
C203, C210	DNI
C248, C249	18 pF
C204, C211	DNI
R205/R206, R212/R213	0 Ω
C207, C214	DNI
T201, T202	Mini circuits TMC1-83X+

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-GGAB-1.

Figure 191. 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-196-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
ADRV9008BBCZ-1	−40°C to +85°C	196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-196-13
ADRV9008BBCZ-1REEL	−40°C to +85°C	196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-196-13
ADRV9008-1W/PCBZ		Pb-Free Evaluation Board, 75 MHz to 6000 MHz	

[1] Z = RoHS Compliant Part.
[2] See the Thermal Management section.