EV-AD7768-1FMCZ User Guide
UG-1260

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Evaluating the AD7768-1 24-Bit, 256 kSPS, Sigma-Delta ADC with Power Scaling

FEATURES

Full featured evaluation board for the AD7768-1
PC control in conjunction with EVAL-SDP-CH1Z
PC software control and data analysis
Time and frequency domain
Standalone hardware capability

EQUIPMENT NEEDED

EVAL-SDP-CH1Z system demonstration platform
DC/ac signal source (audio precision or similar high performance signal source)
PC running Windows 7, Windows 8, or Windows 10 with USB 2.0 port

EVALUATION KIT CONTENTS

EV-AD7768-1FMCZ evaluation board

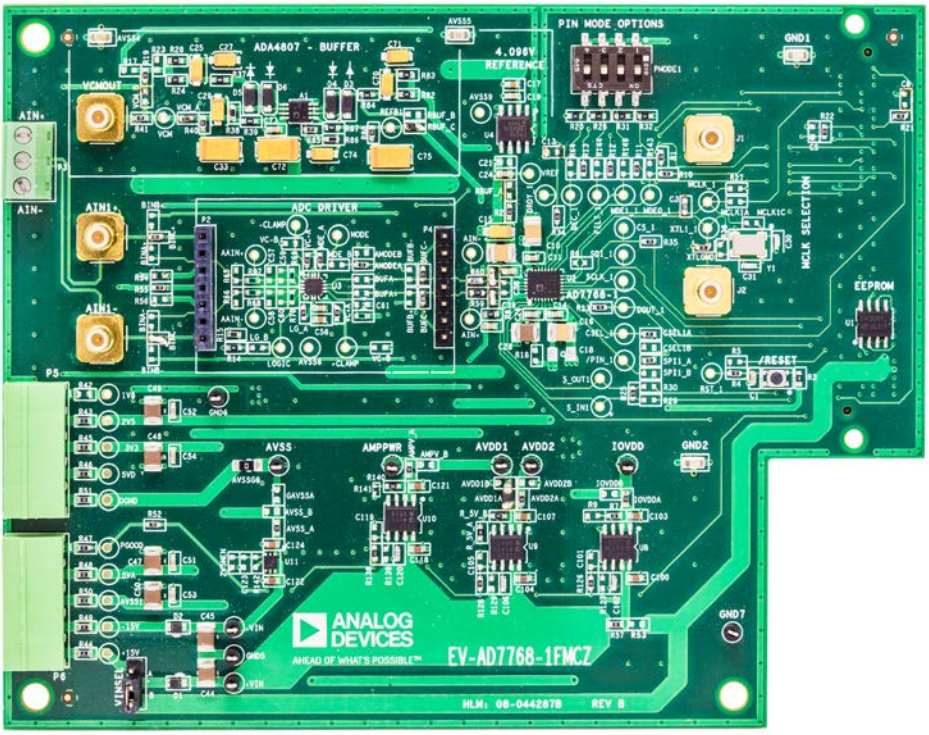
GENERAL DESCRIPTION

The EV-AD7768-1FMCZ evaluation kit features the AD7768-1 24-bit, 256 kSPS analog-to-digital converter (ADC). The EV-AD7768-1FMCZ board connects to the USB port of the PC via the EVAL-SDP-CH1Z motherboard. By default, power is supplied from the EVAL-SDP-CH1Z supply, which is regulated to 5 V and 3.3 V to supply the AD7768-1 and support components.

The EV-AD7768-1FMCZ software fully configures the AD7768-1 device register functionality and provides dc and ac time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The EV-AD7768-1FMCZ is an evaluation board that allows the user to evaluate the features of the ADC. The user PC software executable controls the AD7768-1 over USB through the system demonstration platform (EVAL-SDP-CH1Z).

EVALUATION BOARD PHOTOGRAPH



16666-001

Figure 1.

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REVISION HISTORY

4/2018—Revision 0: Initial Version

QUICK START GUIDE

To begin using the evaluation board, take the following steps:

1. Ensure the EVAL-SDP-CH1Z system demonstration platform board is disconnected from the PC. Install the AD7768-1 evaluation board software. Restart the PC after the software installation is complete. For complete software installation instructions, see the Software Installation Procedures section.
2. Connect the EVAL-SDP-CH1Z system demonstration platform board to the unpowered EV-AD7768-1FMCZ evaluation board. The J4 connector of the EVAL-SDP-CH1Z system demonstration platform board connects to the receiving socket, P1, on the AD7768-1FMCZ printed circuit board (PCB).
3. Ensure the evaluation boards are connected firmly together by screwing them together.
    a. Ensure the VINSEL link is set to Position B; this provides power to the AD7768-1 evaluation board from the EVAL-SDP-CH1Z.
4. Connect the 12 V dc supply to the EVAL-SDP-CH1Z system demonstration platform board and then connect to the PC using the supplied USB cable. Choose to automatically search for the drivers for the EVAL-SDP-CH1Z if prompted by the operating system.
5. Launch the EV-AD7768-1FMCZ software from the **Analog Devices** subfolder in the **Programs** menu.

To power off, first close the software. Then press the reset button on the EVAL-SDP-CH1Z before disconnecting the power or USB.

ANALOG INPUTS AND FRONT-END CIRCUIT

The AIN1+ and AIN− analog inputs are accessible through either the Subminiature Version B connectors (SMBs) or the terminal blocks (see Figure 2).

The default connections on the evaluation board are set as follows:

- Connect from the input terminals through the driver amplifier.
- Analog inputs from an external source are biased to a common mode using the on-board common-mode voltage (VCM). VCM defaults to (AVDD1 − AVSS)/2, which equates to 2.5 V on the EV-AD7768-1FMCZ.
- For the ADR4540, a 4.096 V low noise reference is used by default, allowing an absolute input range of 0 V to 4.096 V on each input.
- The driver amplifier is not terminated at the inputs for any particular source impedance.

Figure 2. Analog Inputs

EVALUATION BOARD HARDWARE

HARDWARE LINK OPTIONS

The default link options are listed in Table 1. The power input to the evaluation board can be taken from the SDP-H1 or from the P5 connector or P6 connector. The default option takes 12 V of power from the EVAL-SDP-CH1Z, which is passed to the ADP7118 on-board low dropout regulators (LDOs).

Table 1. Default Link and Solder Link Options

Name	Link No.	Default Link Option	Description
GPIO0		R10	GPIO0 connection; DEC_1 test point
	R1		R1 selects the driver amplifier power mode
	R10		R10 selects the general purpose input/output (GPIO) connection to the SDP-H1 board
	R143		R143 selects the pin mode switch for power mode selection
GPIO1		R11	GPIO1 connection; Filt_1 test point
	R11		R11 selects the GPIO connection to the SDP-H1 board
	R149		R149 selects the pin mode switch for power mode selection
GPIO2		R12	GPIO2 connection; MDE1_1 test point
	R12		R12 selects the GPIO connection to the SDP-H1 board
	R144		R144 selects the pin mode switch for filter selection
GPIO3		R13	GPIO3 connection; MDE0_1 test point
	R13		R13 selects the GPIO connection to the SDP-H1 board
	R64		R64 selects the pin mode switch for decimation rate control
$\overline{\text{PIN}}$/SPI		SPI1_A	Selects pin or serial peripheral interface (SPI) mode on the AD7768-1
	SPI1_A		SPI1_A ties Pin 6 to the IOVDD voltage level, selecting SPI control
	SPI1_B		SPI1_B ties Pin 6 to GND, selecting pin mode control
MCLK		MCLK1A	Selects the source of the AD7768-1 master clock
	MCLK1A		MCLK1A selects the 16 MHz clock from the SDP-H1 board
	MCLK1C		MCLK1C selects the 16.384 MHz crystal (XTAL), Y1
			If none of the above are shorted with 0 Ω links, then an external clock can be applied on J1; in other words, remove all 0 Ω links to use an external MCLK applied on J1
CLK_SEL		CSEL1A	Selects the clock source for $\overline{\text{PIN}}$ control mode
	CSEL1A		CSEL1A ties Pin 8 to GND, selecting a complementary metal oxide semiconductor (CMOS) clock option in pin mode
	CSEL1B		CSEL1B ties Pin 8 to IOVDD, enabling the XTAL excitation circuitry in pin mode
XTL1		XTLGND	Set up for XTAL1 (Pin 13)
	R36		R36 inserted for XTAL operation
	XTLGND		XTLGND inserted for normal CMOS clock operation
$\overline{\text{SYNC\_IN}}$		R25	Sets up the synchronization mechanism for the AD7768-1
	R25		R25 shorts SYNC_OUT to SYNC_IN, meaning the AD7768-1 SYNC pulse does not need occur synchronous to the MCLK edge; SPI or start (GPIO) SYNC pulses can be used
	R29		R29 inserted allows a sync connection from the SDP-H1 connector
Voltage Input Select	VINSEL	B	Selects the input to the LDOs
	A		A selects the power input from Connector P6
	B		B selects 12 V from the SDP-H1 board
IOVDD		IOVDDA	Selects the IOVDD source
	IOVDDA		IOVDDA selects the ADP7118ARDZ-3.3 LDO
	IOVDDB		IOVDDB selects the external IOVDD source on Connector P5
AVDD1		AVDD1A	Selects the AVDD1 source
	AVDD1A		AVDD1A selects the 5 V LDO output
	AVDD1B		AVDD1B selects the external AVDD1 source on Connector P6

Name	Link No.	Default Link Option	Description
AVDD2		AVDD2A	Selects the AVDD2 source
	AVDD2A		AVDD2A selects the 5 V LDO output
	AVDD2B		AVDD2B selects the external AVDD2 source on Connector P5
AVSS		AVSS_A	Selects the AVSS voltage reference
	AVSS_A		AVSS_A selects the −2.5 V output from the ADP7182 −2.5 V LDO
	AVSS_B		AVSS_B selects the external AVSS source on Connector P6
	AVSSGX	AVSSG6	AVSSG6 shorts AVSS and DGND by default; it can be shorted in numerous locations around the board
AMP V_S+		AMPV_A	Selects the amplifier and reference voltage supplies
	AMPV_A		AMPV_A uses the 7 V output from the on-board adjustable 7 V LDO
	AMPV_B		AMPV_B uses the 5 V output from the on-board 5 V LDO
ADC Driver Input		BIN1A+/BIN1A−	Selects the input to the ADC driver amplifier
	BIN1A+/ BIN1A−		BIN1A+/BIN1A− connect the analog inputs to the ADC driver
	BIN1B+/ BIN1B−		BIN1B+/BIN1B− bypass the driver amplifier
	BIN1C+/ BIN1C−		BIN1C+/BIN1C− select the amplifier mezzanine card option for evaluating different driver amplifiers
ADC Driver Output		BUF1A+/BUF1A−	Routes the output to the ADC driver amplifier
	BUF1A+/ BUF1A−		BUF1A+/BUF1A− connect the driver amplifier output to the AD7768-1
	BUF1B+/ BUF1B−		BUF1B+/BUF1B− bypass the driver amplifier for a direct connection to the AD7768-1
	BUF1C+/ BUF1C−		BUF1C+/BUF1C− select the output of the amplifier mezzanine card for evaluating driver amplifiers
VCM Selection		VCM_A	Selects the path for the VCM signal to the driver amplifiers
	VCM_A		VCM_A selects a buffered and filtered VCM signal
	VCM_B		VCM_B takes the VCM straight from the AD7768-1, unbuffered
Reference Buffer		RBUF_C	Selects the path for the ADR4540 reference
	RBUF_A		RBUF_A routes the reference directly to the ADC, unbuffered
	RBUF_B		RBUF_B routes the reference directly to the ADC through large filtering capacitors and is unbuffered to the ADC
	RBUF_C		RBUF_C routes the reference to the ADC through the ADA4807-2 buffer

On-Board Connectors

Table 2 provides information about the external on-board connectors on the EV-AD7768-1FMCZ.

Table 2. On-Board Connectors

Connector	Function
P1	Connects all digital signals to the SDP-H1 board
P5/P6	External power connections
P3	DC analog inputs
AIN1+/AIN1−	SMB analog inputs for ac signals
VCMOUT	VCM output from the ADA4807-2 buffer
J1	SMB connector for the external MCLK
J2	SMB connector for the low voltage differential signaling (LVDS) clock on the XTAL1 pin

POWER SUPPLIES

The evaluation board requires an external power supply—either a bench top supply or the 12 V output from the EVAL-SDP-CH1Z. VINSEL selects which source to use. Select Position A on VINSEL to power the board externally through P6. Select Position B on VINSEL to power the EV-AD7768-1FMCZ using the SDP-H1 board.

Linear regulators generate the required power supply levels from the input voltage selected on VINSEL. The ADP7118 regulators (U8, U9, and U10) supply 5 V to AVDD1 and AVDD2, 7 V to the ADC driver amplifier, ADR4540, ADA4807-2 (reference and reference buffer, respectively), and the 3.3 V ADP7118 for IOVDD.

Each supply is decoupled at the point where it enters the board and again at the point where it connects to each device.

EVALUATION BOARD SETUP PROCEDURES

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP board as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and the EVAL-SDP-CH1Z to the USB port of the PC to ensure the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Board

Connect the EVAL-SDP-CH1Z to P1 on the EV-AD7768-1FMCZ board. Screw the two boards together

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

The EV-AD7768-1FMCZ evaluation kit includes a link to the software to be installed on your PC before you begin using the evaluation board. Download the software at www.analog.com/EV-AD7768-1FMCZ.

There are two parts to the installation: the AD7768-1 evaluation board software installation and the EVAL-SDP-CH1Z system demonstration platform board drivers installation.

Installing the AD7768-1 Evaluation Board Software

To install the AD7768-1 evaluation board software, take the following steps:

1. The EVAL-AD7768FMCZ evaluation software requires the .NET 3.5 framework to operate correctly. Ensure the correct .NET framework is installed before continuing with the installation. Check if the .NET 3.5 framework is installed by taking the following steps:
   a. In the Windows **Control Panel**, go to **Programs** > **Programs and Features**.
   b. Select the **Turn Windows Features on or off** section. This selection lists the features currently installed. Select **.NET Framework 3.5 (includes .NET 2.0 and 3.0)**. Figure 3 shows this dialog box as it appears in Windows 10.

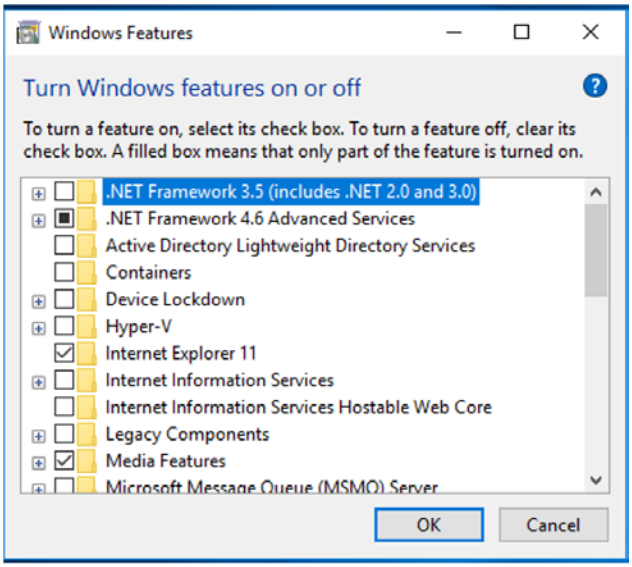

Figure 3. Turning Windows Features On or Off

   c. After selecting the checkbox and clicking **OK**, the dialog box shown in Figure 4 appears. An internet connection is needed for this step. Select **Download files from Windows Update**.

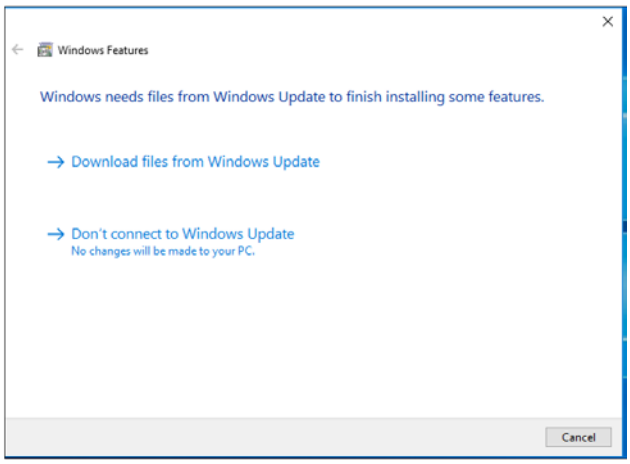

Figure 4. Prompt to Download Windows Updates

2. Disconnect the EVAL-SDP-CH1Z system demonstration platform board from the USB port of the PC, and run the executable.
3. Double click the setup.exe file to begin the evaluation board software installation. The software is installed to the following default location: **C:\Program Files\Analog Devices\AD7768-1**.
4. A dialog box appears asking for permission to allow the program to make changes to the computer (see Figure 5). Click **Yes**.

Figure 5. Granting Permission for the Program to Make Changes.

5. Select the location to install the software, and then click **Next**. Figure 6 shows the default locations, which are displayed when the window opens; select another location by clicking **Browse**.

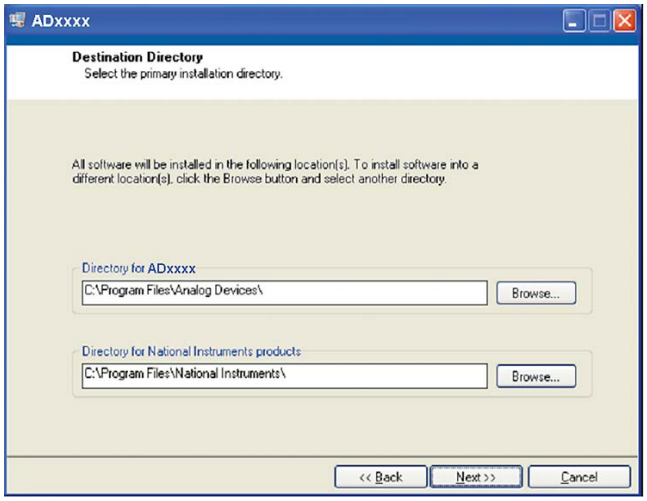

Figure 6. Selecting the Location for Software Installation

6. A license agreement appears. Read the agreement, and then select **I accept the License Agreement** and click **Next** (see Figure 7).

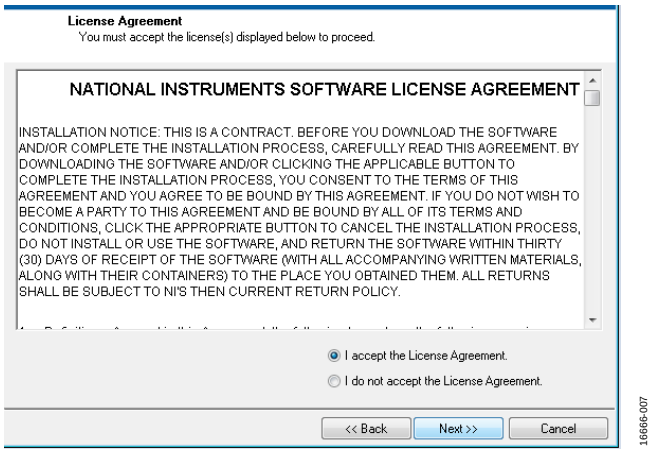

Figure 7. Accepting the License Agreement

7. A summary of the installation is displayed (see Figure 8). Click **Next** to continue.

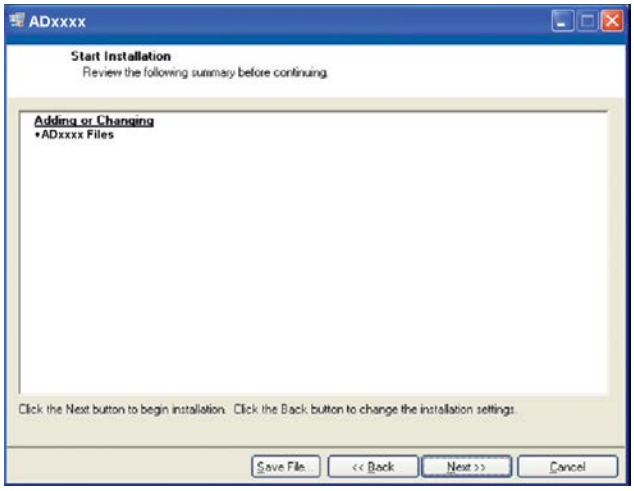

Figure 8. Reviewing a Summary of the Installation

8. A dialog box indicates when the installation is complete (see Figure 9). Click **Next**.

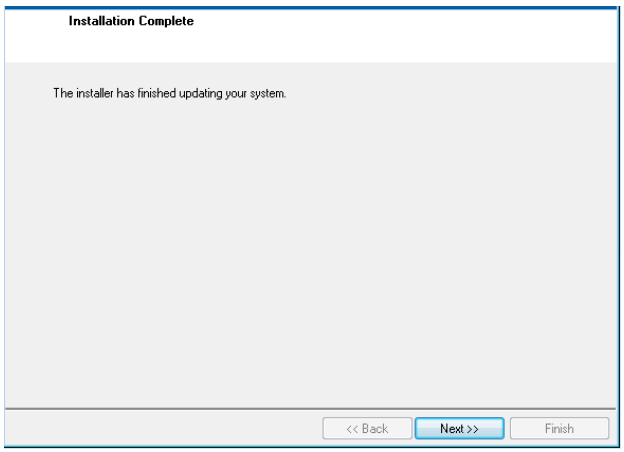

Figure 9. Indicating When the Installation is Complete

Installing the EVAL-SDP-CH1Z System Demonstration Platform Board Drivers

After the installation of the evaluation software is complete, a welcome window displays the installation information for the EVAL-SDP-CH1Z system demonstration platform board drivers.

To install the EVAL-SDP-CH1Z system demonstration platform board drivers, take the following steps:

1. With the EVAL-SDP-CH1Z system demonstration platform board still disconnected from the USB port of the PC, ensure that all other applications are closed, and then click **Next** (see Figure 10).

Figure 10. Beginning the Drivers Installation

2. Select the location to install the drivers and click **Next** (see Figure 11).

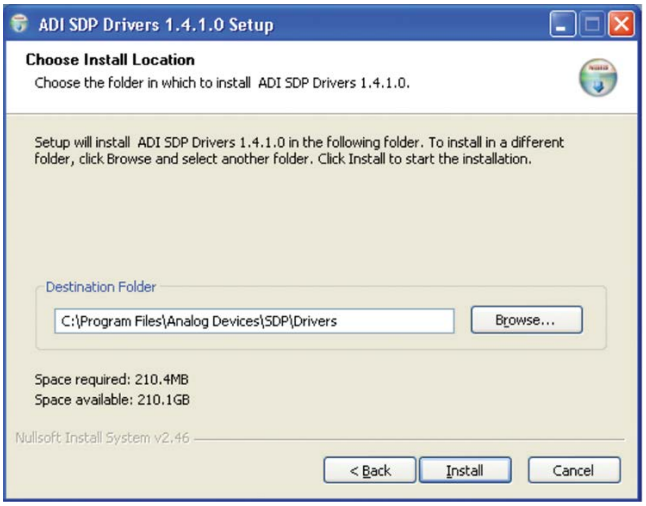

Figure 11. Selecting the Location for the Drivers Installation

3. Click **Install** (see Figure 12).

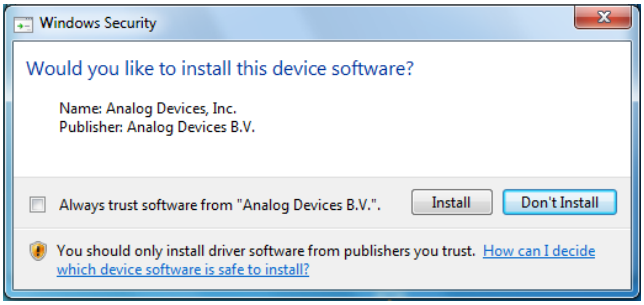

Figure 12. Granting Permission to Install Drivers

4. To complete the driver installation, click **Finish**, which closes the installation wizard (see Figure 13).

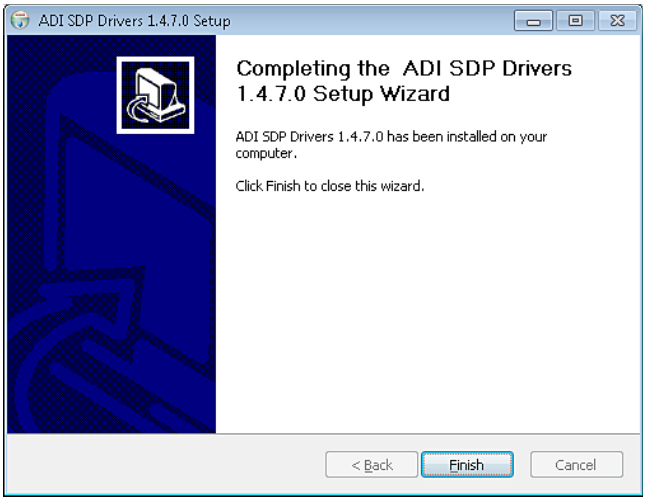

Figure 13. Completing the Drivers Setup Wizard

5. Before using the evaluation board, restart the computer (see Figure 14).

Figure 14. Restarting Your Computer

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Evaluation Board Software section and the Evaluation Board Hardware section, set up the system for data capture as follows:

1. Run the **Found New Hardware Wizard** after the EVAL-SDP-CH1Z system demonstration platform board is plugged into the PC. If using Windows XP, the user may need to search for the EVAL-SDP-CH1Z drivers. Automatically search for the drivers for the EVAL-SDP-CH1Z system demonstration platform board if prompted by the operating system.
2. Check that the evaluation board is connecting to the PC correctly using the **Device Manager** of the PC. Access the **Device Manager** as follows:
    a. Right click **My Computer** and then click **Manage**.
    b. A dialog box appears asking for permission to allow the program to make changes to the computer. Click **Yes**.
    c. The **Computer Management** window appears. Click **Device Manager** from the list of **System Tools** (see Figure 15).
    d. If the EVAL-SDP-CH1Z system demonstration platform board appears under **ADI Development Tools**, the driver software is installed and the evaluation board is connecting to the PC correctly.

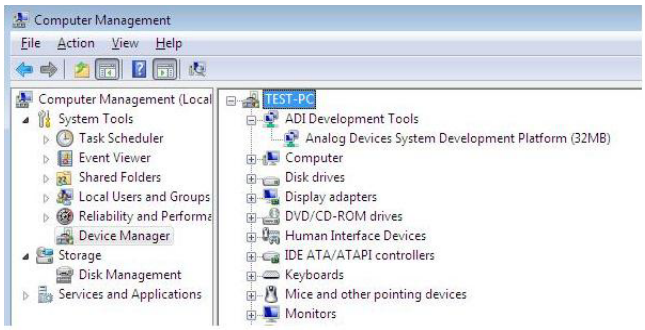

Figure 15. Checking That the Evaluation Board Is Connected to the PC Correctly

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, take the following steps to launch the AD7768-1 software:

1. From the **Start** menu, select **Programs** > **Analog Devices** > **AD7768-1 Evaluation Software**. The main window of the software then displays.
2. If the AD7768-1 evaluation system is not connected to the USB port via the EVAL-SDP-CH1Z when the software is launched, a connectivity error displays (see Figure 16). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Refresh**, and then follow the on screen instructions.

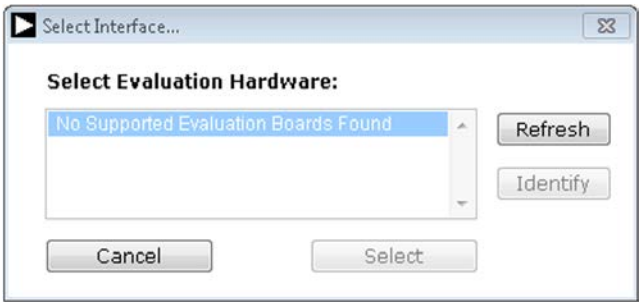

Figure 16. Connectivity Error Alert

SOFTWARE OPERATION

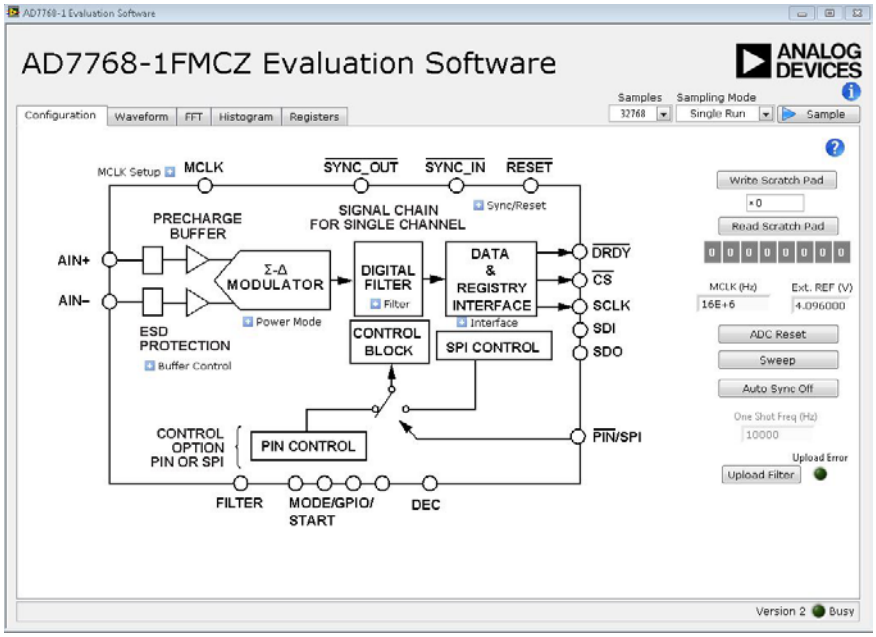

Figure 17. ***Configuration*** *Tab*

Overview of the Main Window

The main window contains the significant control buttons and analysis indicators of the evaluation software.

Configuration Tab and AD7768-1 Block Diagram

The **Configuration** tab is the tab displayed by default when the software first opens (see Figure 17). An overview of the AD7768-1 block diagram is shown, along with buttons that open pop up menus for quick configuration of the device.

The **Waveform** tab (see Figure 19) displays captured waveform data. This tab also contains options to save the resulting data and shows the header data output from the conversion results if the header data output is enabled.

The **FFT** tab (see Figure 22) and **Histogram** tab (see Figure 23) show a more in depth analysis of the output data. This data can be saved to a file.

Use the **Registers** tab to change the configuration of the AD7768-1 (see Figure 24).

Sample Button

Click **Sample** to start ADC sampling; results are reported in the **Waveform**, **FFT**, and **Histogram** tabs. The mode of operation can be set using the **Sampling Mode** button; the mode can be continuous sampling or a single run. Continuous sampling mode operates similarly to automating the sample button, rather than taking a stream of continuous data.

Number of Samples

The number of samples per channel is variable and can be changed using the **Samples** control.

MCLK

The **MCLK (Hz)** control in the **Configuration** tab must match the frequency of the ADC clock source. It is set to 16 MHz by default.

V_{REF}

The **Ext. REF (V)** control in the **Configuration** tab must match the reference voltage of the ADC. This control is set to 4.096 V by default to match the ADR4540 output on the evaluation board.

ADC Reset

Clicking **ADC Reset** in the **Configuration** tab sends a reset command to the ADC via the SPI and resets the device to its default configuration.

Status Indicator and Busy light

The status bar at the bottom of the screen indicates the current state of the AD7768-1 software. The **Busy** indicator illuminates when the software is busy performing an action. Do not carry out any actions when this indicator is lit.

Pop Up Buttons

The pop up buttons allow quick configuration of the EV-AD7768-1FMCZ. The pop up buttons allow quick configuration by the user of the more common register settings. Figure 18 shows the pop up menu for the power mode selection. The register section allows configuration of the full suite of available registers.

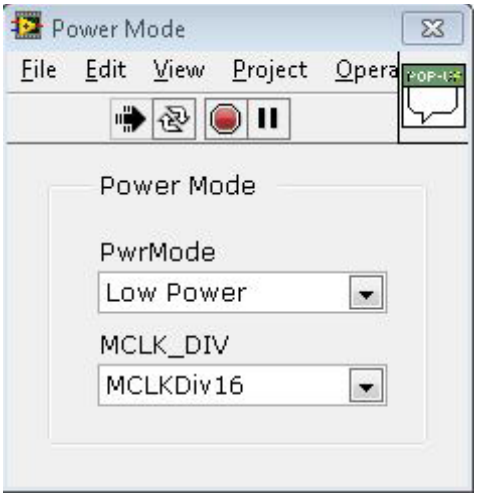

*Figure 18. Pop Up Button Menu for **Power Mode** Selection*

Waveform Tab

The **Waveform** tab displays a time domain graph of the sampled data. Controls beneath the graph allow zooming and panning. Amplitude information is given beneath the graph for the analysis channel selected.

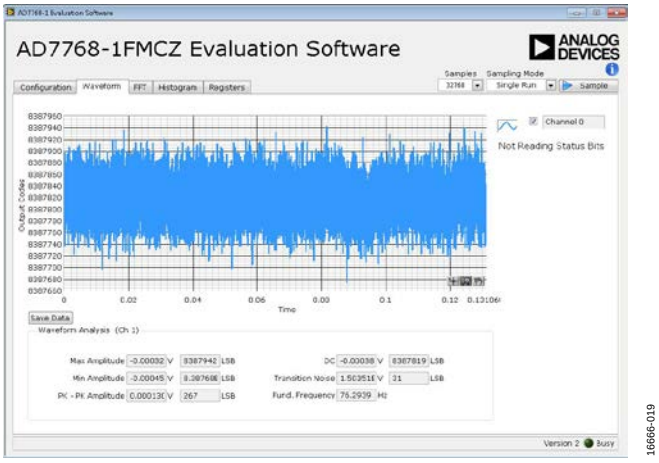

*Figure 19. **Waveform** Tab*

If postprocessing of the waveform data is required, each of the plots in the AD7768-1 evaluation software can be exported, as shown in Figure 20. Right click on the graph and select the options shown in Figure 20. It is also possible to manipulate the data as shown in Figure 21. The controls for zoom, zoom to fit, and so on are located in the bottom right corner of each graph.

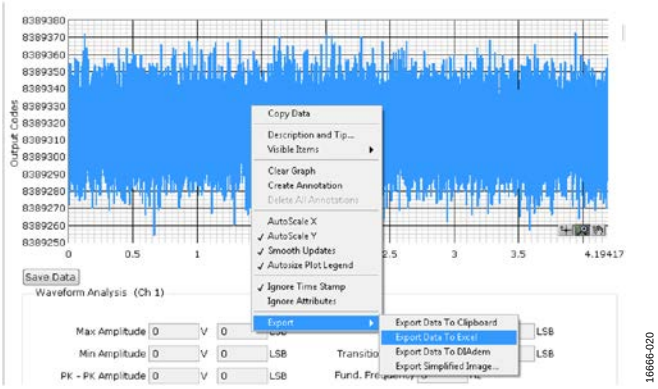

Figure 20. Exporting Data from a Graph

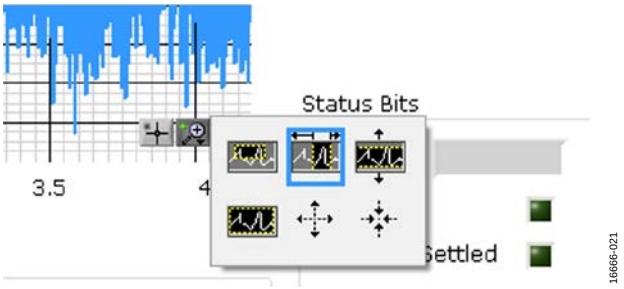

Figure 21. Graph Manipulation

FFT Tab

The **FFT** tab shows a frequency domain graph of the sampled data. Controls beneath the graph allow zooming and panning and control over amplitude and frequency scaling. Frequency and amplitude information is given beneath the graph for the selected analysis channel.

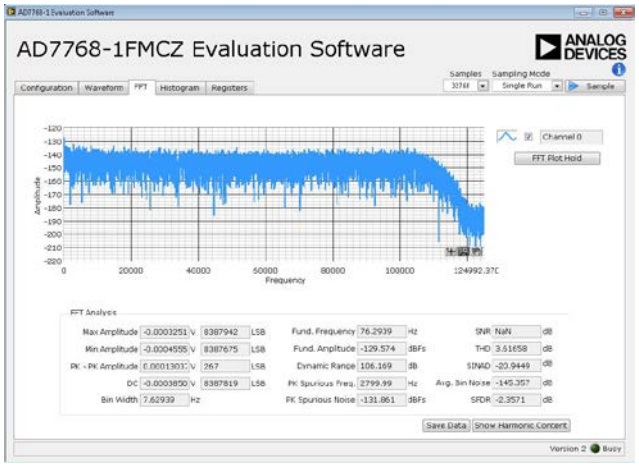

*Figure 22. **FFT** Tab*

Histogram Tab

The **Histogram** tab shows a histogram of the sampled data. Controls beneath the graph allow zooming, panning, and control over amplitude scaling. Amplitude information is given beneath the graph for the selected analysis channel.

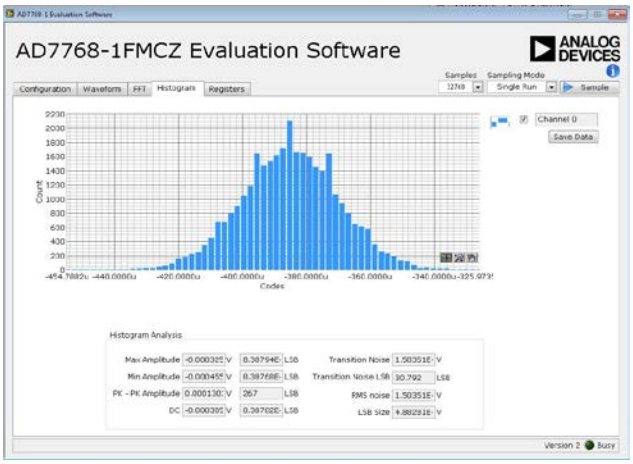

*Figure 23. **Histogram** Tab*

Registers Tab

The **Registers** tab allows precise control of the AD7768-1 registers, allowing them to be read back and written to. The registers are grouped together and can be altered in a number of ways, as shown in Figure 24. The register to be written to can be selected from the register map, located on the left hand side of the **Registers** tab. Individual register bits can be changed from the register section, or the entire register can also be written to by writing the required hexadecimal value. Dropdown options can be selected from the **Bitfields** section, or the entire bitfield can be written to with a hexadecimal value.

A particular register configuration can be saved to be loaded again at a later time.

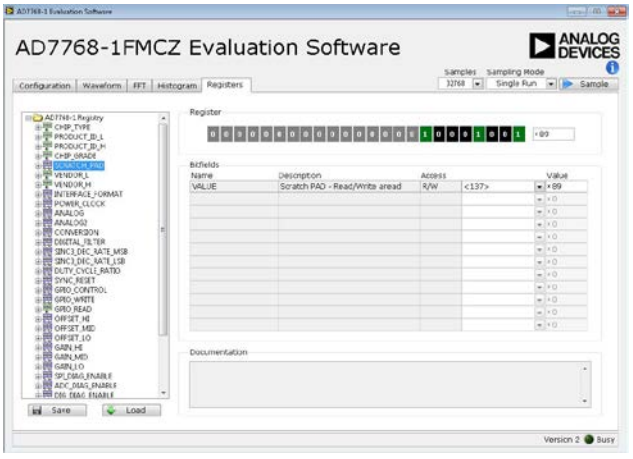

*Figure 24. **Registers** Tab*

Scratch Pad

The scratch pad shown in Figure 25 is located on the **Configuration** tab. The scratch pad can verify that read and write operations are functioning correctly from the AD7768-1 graphic user interface (GUI) to the AD7768-1 device on the EV-AD7768-1FMCZ. The same scratch pad is also located in the **Register** tab, Register Address 0x0A.

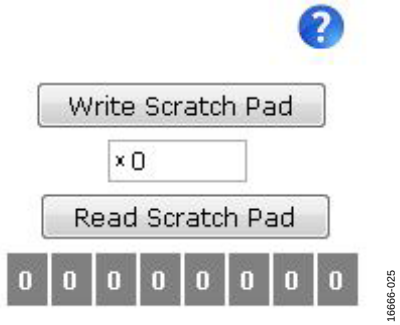

Figure 25. Scratch Pad for Register Read/Write Debug

Sweep

To aid in evaluation of the AD7768-1, a sweep function automatically steps through one of two options selectable by the user. The first sweep option performs fast Fourier transform (FFT) analysis on decimation rates from 32 to 1024 on each of the three power modes.

The second sweep option performs FFT analysis on each combination of an analog input precharge buffer and a reference buffer.

The data saved to the file in both cases includes root mean squared (RMS) noise, dynamic range, signal-to-noise ratio (SNR), and total harmonic distortion (THD). The button to start a sweep is located on the **Configuration** tab, as shown in Figure 27.

Figure 26. Available Sweep Options

Auto Sync Off

After each configuration change of the AD7768-1, a synchronization pulse is required, as per the data sheet. By default, the EV-AD7768-1FMCZ software provides this pulse over the SPI (SYNC_IN is shorted to SYNC_OUT on the evaluation board) each time the **Sample** button is pressed. This automatic SYNC operation can be prevented by pressing the **Auto Sync Off** button as shown in Figure 27; this is needed if evaluating the device in one shot mode, for example, or if a very slow output data rate (ODR) is selected, in which case the user may wish to manually issue a synchronization pulse to capture only fully settled data.

One Shot Mode

In one shot mode, the AD7768-1 operates similar to a successive approximation register (SAR) in that the output data rate is set by the frequency of a pulse applied on the SYNC_IN input. To enable this mode, set the CONV_MODE bitfield in the conversion register, Address 0x18, to continuous one shot. This setting enables the user to enter the one shot mode, which calculates the time base on the evaluation software plots. **Auto Sync Off** is also selected in this mode.

Digital Filter Upload

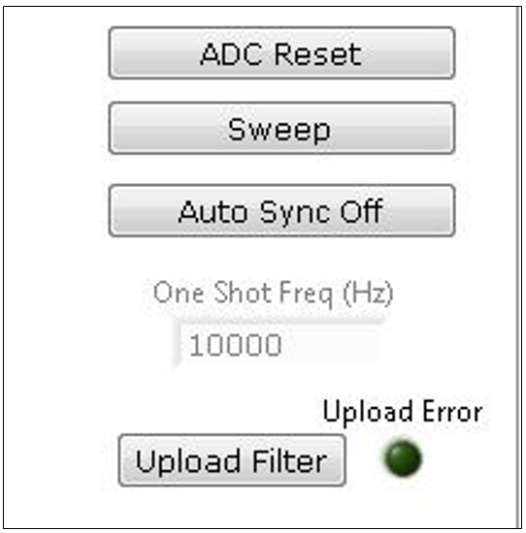

*Figure 27. Filter Upload Option on the Main **Configuration** Tab*

There is an option to upload a customized digital filter to the AD7768-1. This option replaces the default wideband filter coefficients with coefficients customized for a specific filter response. Consult the AD7768-1 data sheet for details on designing custom filters for upload to the AD7768-1.

Pressing the **Upload Filter** button allows the user to upload a set of 56 coefficients to the AD7768-1. The file format used for this upload must be a .csv file. The format of data must match that of the example files supplied with this software. Example files are named **AD7768-1_Low_Ripple.csv** and **AD7768-1 _simple_average.csv**

Choosing the upload filter option automatically sets the device in fast power mode and selects the wideband filter option. After each upload, the AD7768-1 software reads back all 56 coefficients and checks these against the coefficients in the selected file. If there is any difference, this error is flagged in the upload error indicator. After the reset button is pressed, or if the AD7768-1 is powered off, the default wideband coefficients are loaded into the device again. The customized coefficients must be loaded each time the device is powered on or reset, if required.

Press the **FFT Plot Hold** button in the **FFT** tab to check that the filter upload was successful and that the filter characteristics are as expected. This action holds the highest amplitude value in each frequency bin for as long as the **FFT Plot Hold** button is selected.

Status Bits

If the status bits are enabled in the register map, the status bits for the conversion are displayed in the **Waveform** tab as shown in Figure 28. The status bits can be output by writing a 1 to Bit 4 of the INTERFACE_FORMAT register, Address 0x14.

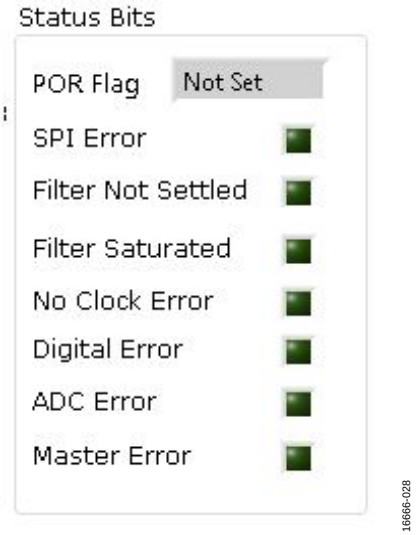

Figure 28. Status Bits

Exiting the Software

To exit the software, click the red **X** at the top right hand corner of the main window. Press the reset button on the EV-AD7768-1FMCZ before the EVAL-SDP-CH1Z is powered off.

Example Data Capture

In this example, a sample is taken and analyzed with the AD7768-1 software. The conditions required for operation are median mode, decimation × 128, with a wideband filter.

1. Start the AD7768-1 software. Wait for the **Busy** indicator to turn off. The software sets the power mode to fast and the filter to wideband on power-up.
2. Ensure that **MCLK (Hz)** and **Ext. REF (V)** are set to match the clock frequency and reference voltage supplied to the chip (by default, the values are 16 MHz and 4.096 V, respectively).
3. Set the number of samples per channel to 32,768 (default).
4. Configure the registers as required using the **Registers** tab. The POWER_CLOCK register is set to 0x33 and the DIGITAL_FILTER register is set to 0x42.
5. Click **Sample** to take a reading. Wait for the **Busy** indicator to turn off.
6. The sampled data is now present in the data capture tabs (**Waveform**, **FFT**, and **Histogram** tabs). Change between each of these tabs to view the results.
7. These settings give a dynamic range of approximately 114 dB, which can be seen on the FFT Analysis section of the **FFT** tab.
8. To export the raw data for further analysis, click on the **Waveform** tab. Right click the graph. Select **Export** > **Export Data To Excel**. The data can then be post processed in Microsoft Excel or passed to other analysis tools.

Example $\overline{\text{PIN}}$ Control

In this example, the steps required to set the device into $\overline{\text{PIN}}$ control mode with an externally applied MCLK are detailed. The $\overline{\text{PIN}}$ control settings are low power mode, wideband, low ripple filter, and decimation by 64. $\overline{\text{PIN}}$ control is only available in the LFCSP package.

To set the device into $\overline{\text{PIN}}$ control mode, take the following steps:

1. Change the 0 Ω $\overline{\text{PIN}}$/SPI link from SPI1_A to SPI1_B; this changes Pin 6 from high to low, therefore selecting $\overline{\text{PIN}}$ control mode.
2. Change the following solder links on the AD7768-1 evaluation board: move R13 to R64, move R12 to R144, move R11 to R149, and move R1 to R143.
3. On the PMODE1 switch, 1001 must to be written to GPIO0 to GPIO3. To perform this setting, select the following options: set Switch 1 to the on position, set Switch 2 to the off position, set Switch 3 to the off position, and set Switch 4 to the on position.
4. Remove the 0 Ω link on MCLK1A. Add a 50 Ω resistor (or other) to Position C3 to terminate the external clock correctly.
5. Set the MCLK frequency on the **Configuration** tab (see Figure 17). The output data rate (ODR) is set using a combination of the AD7768-1 MCLK and decimation rate. In $\overline{\text{PIN}}$ control mode, the registers are not used to configure the part. The register map settings of the EV-AD7768-1FMCZ software are no longer automatically updated to reflect the settings of the device.