Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

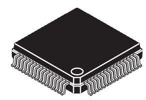
Freescale Semiconductor
Data Sheet: Technical Data

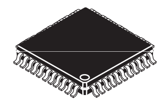
Document Number: MC9S08LL16
Rev. 7, 1/2013

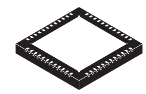
An Energy Efficient Solution by Freescale

MC9S08LL16 Series

Covers: MC9S08LL16 and MC9S08LL8


64-LQFP
Case 840F


48-LQFP
Case 932


48-QFN
1314

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20-MHz CPU at 3.6V to 1.8V across temperature range of -40°C to 85°C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Dual Array FLASH read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and FLASH contents
- Power-Saving Modes
  - Two low power stop modes
  - Reduced power wait mode
  - Low power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents.
  - Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
  - 6 usec typical wake up time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1MHz to 10 MHz.
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-Voltage Warning with interrupt
  - Low-Voltage Detection with reset or interrupt
  - Illegal opcode and illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — 4x28 or 8x24 LCD driver with internal charge pump and option to provide an internally regulated LCD reference that can be trimmed for contrast control.
  - **ADC** — 8-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
  - **ACMP** — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
  - **SPI**— Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
  - **IIC** — IIC with up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
  - **TPMx** — Two 2-channel (TPM1 and TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel;
  - **TOD**— (Time Of Day) 8-bit quarter second counter with match register; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components.
- Input/Output
  - 38 GPIOs, 2 output-only pins
  - 8 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.
- Package Options
  - 64-LQFP, 48-LQFP and 48-QFN

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	9/2008	Initial Release.
2	10/2008	Updated electrical characteristics.
3	01/2009	Corrected 48-Pin QFN/LQFP pinouts for pins 29, 30, 32, and 32 in Figure 3. Extracted Stop Mode Adders from the Supply Current table and created a Separate table for the data (See Table 10). Added missing power consumption parameters in Supply Current Characteristics (Table 9).
4	07/21/2009	Completed all the TBDs. Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}, I_{DDAD} to I_{DDA}. Corrected the data in the Table 8, and added $\|I_{InT}\|$. Completed the Figure in the Section 3.6, "DC Characteristics." Corrected RI_{DD} in FEI mode with all modules on, WI_{DD} at 8 MHz, FEI mode with all modules off, $S2I_{DD}$, $S3I_{DD}$; added $ApS3I_{DD}$ in the Table 9. Corrected E_{TUE}, DNL, INL, E_{ZS}, E_{FS}, E_Q, and E_{IL} in the Table 18.
5	10/13/2009	Updated R_{PU}/R_{PD} data in the Table 8. Added Figure 5.
6	10/27/2010	Changed the Max. of R_{PU}/R_{PD} at PTA[4:5], PTD[0:77] and PTE[0:7] to 69.5 kΩ in the Table 8.
7	1/23/2013	Updated $\|I_{In}\|$ in the Table 8.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08LL16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 Devices in the MC9S08LL16 Series

Table 1 summarizes the feature set available in the MC9S08LL16 series of MCUs.

Table 1. MC9S08LL16 Series Features by MCU and Package

Feature	MC9S08LL16		MC9S08LL8
Package	64-pin LQFP	48-pin QFN/LQFP	48-pin QFN/LQFP
FLASH	16,384 (Dual 8K Arrays)		10,240 (8K and 2K arrays)
RAM	2080	2080	2080
ACMP	yes	yes	yes
ADC	8-ch	8-ch	8-ch
IIC	yes	yes	yes
IRQ	yes	yes	yes
KBI	8	8	8
SCI	yes	yes	yes
SPI	yes	yes	yes
TPM1	2-ch	2-ch	2-ch
TPM2	2-ch	-	-
TOD	Yes	Yes	Yes
LCD	8x24 4x28	8x16 4x20	8x16 4x20
I/O pins[1]	38	31	31

[1] I/O does not include two output-only port pins.

The block diagram in Figure 1 shows the structure of the MC9S08LL16 series MCU.

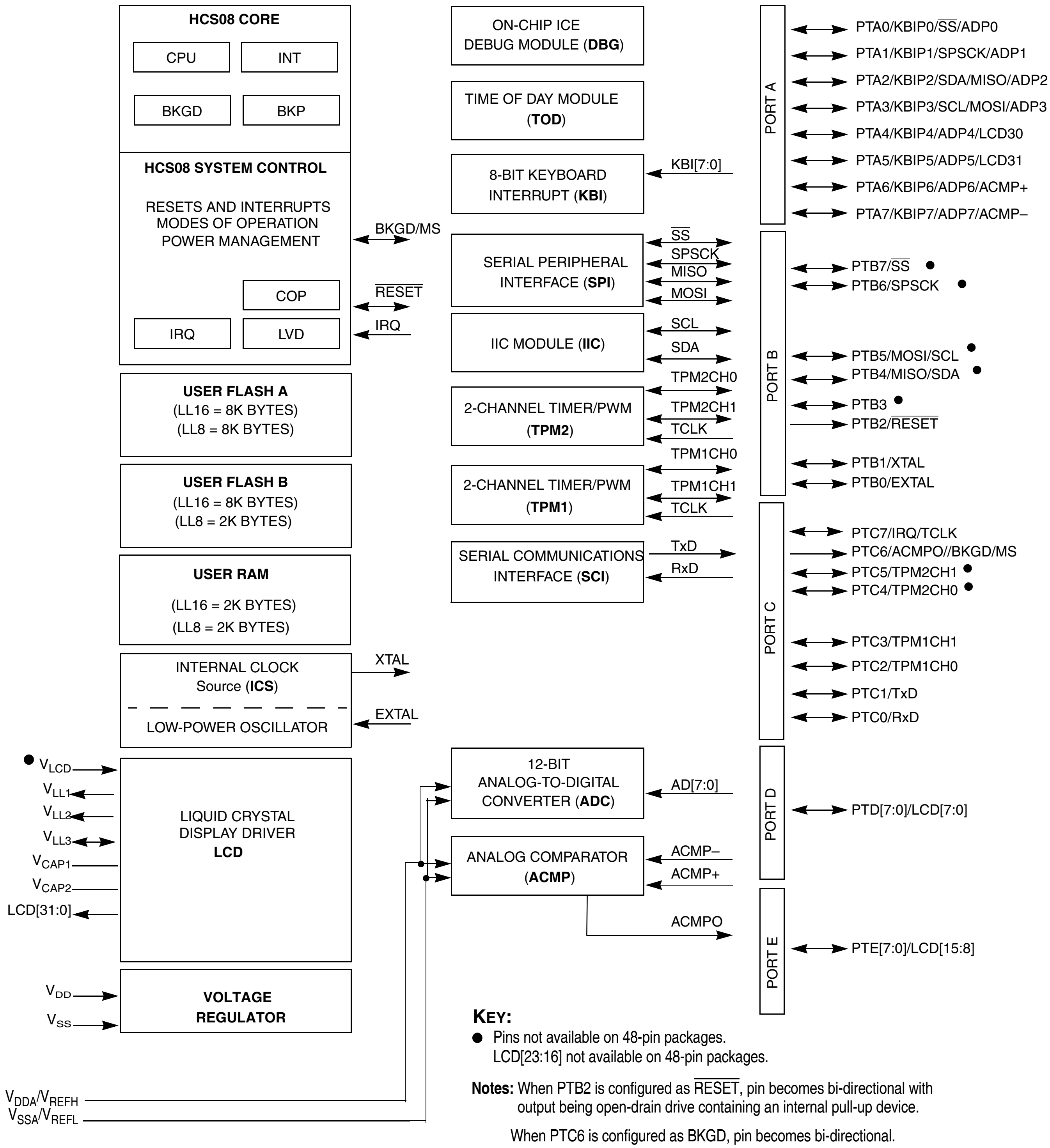
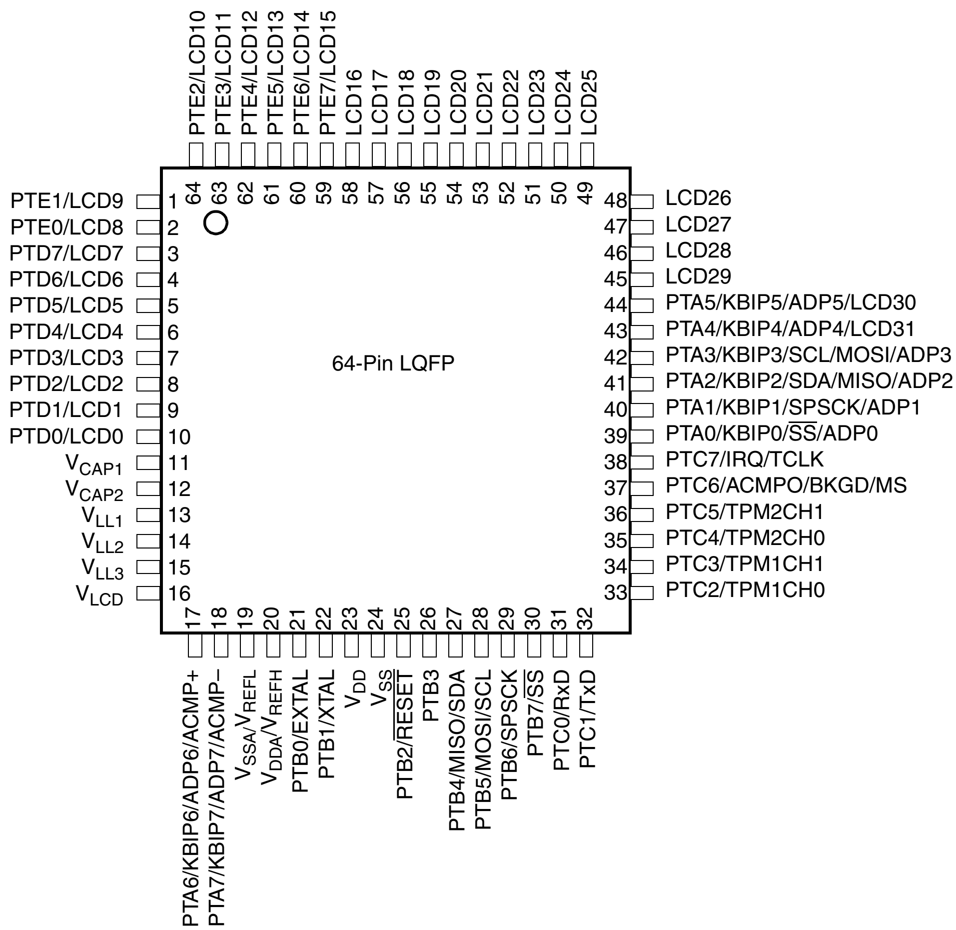


Figure 1. MC9S08LL16 Series Block Diagram

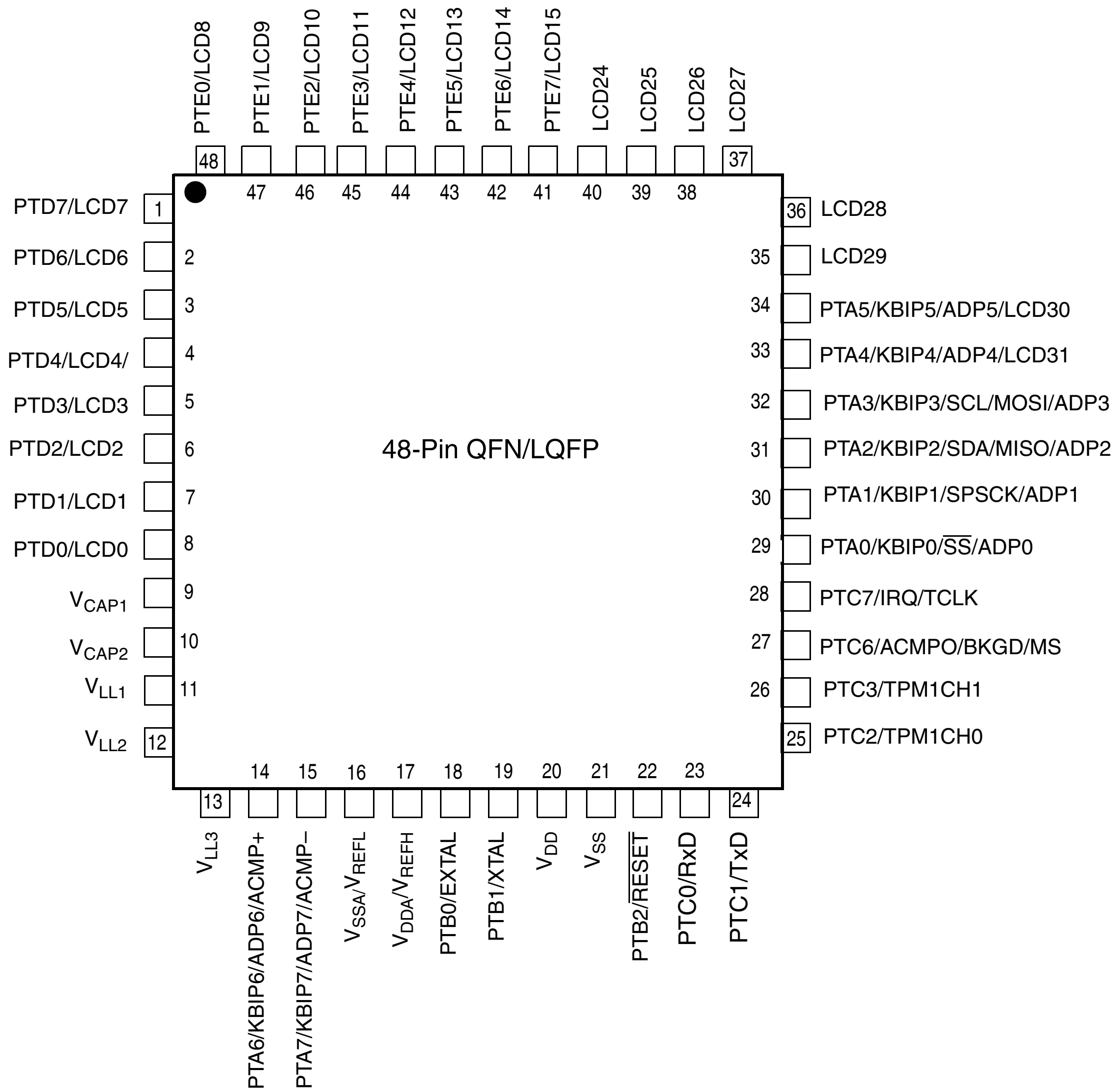
2 Pin Assignments

This section shows the pin assignments for the MC9S08LL16 series devices.



Note: V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Figure 2. MC9S08LL16 Series in 64-pin LQFP Package



Note: V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}

Figure 3. MC9S08LL16 Series in 48-Pin QFN/LQFP Packages

Table 2. Pin Availability by Package Pin-Count

		<-- Lowest **Priority** --> Highest				
64	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
1	47	PTE1	LCD9			
2	48	PTE0	LCD8			
3	1	PTD7	LCD7			
4	2	PTD6	LCD6			
5	3	PTD5	LCD5			
6	4	PTD4	LCD4			
7	5	PTD3	LCD3			
8	6	PTD2	LCD2			
9	7	PTD1	LCD1			
10	8	PTD0	LCD0			
11	9		V_{cap1}			
12	10		V_{cap2}			
13	11		V_{LL1}			
14	12		V_{LL2}			
15	13		V_{LL3}			
16	—		V_{LCD}			
17	14	PTA6	KBIP6	ADP6	ACMP+	
18	15	PTA7	KBIP7	ADP7	ACMP–	
19	16				V_{SSA}	
					V_{REFL}	
20	17				V_{REFH}	
					V_{DDA}	
21	18	PTB0		EXTAL		
22	19	PTB1		XTAL		
23	20				V_{DD}	
24	21				V_{SS}	
25	22	PTB2	$\overline{\text{RESET}}$			
26	—	PTB3				
27	—	PTB4	—	MISO	SDA	
28	—	PTB5	—	MOSI	SCL	
29	—	PTB6	—	SPSCK		
30	—	PTB7	—	$\overline{\text{SS}}$		
31	23	PTC0		RxD		
32	24	PTC1		TxD		
33	25	PTC2		TPM1CH0		
34	26	PTC3		TPM1CH1		
35	—	PTC4		TPM2CH0		
36	—	PTC5		TPM2CH1		
37	27	PTC6	ACMPO	BKGD	MS	
38	28	PTC7		IRQ	TCLK	
39	29	PTA0	KBIP0	—	$\overline{\text{SS}}$	ADP0

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
64	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
40	30	PTA1	KBIP1	—	SPSCK	ADP1
41	31	PTA2	KBIP2	SDA	MISO	ADP2
42	32	PTA3	KBIP3	SCL	MOSI	ADP3
43	33	PTA4	KBIP4	ADP4	LCD31	
44	34	PTA5	KBIP5	ADP5	LCD30	
45	35		LCD29			
46	36		LCD28			
47	37		LCD27			
48	38		LCD26			
49	39		LCD25			
50	40		LCD24			
51	—		LCD23			
52	—		LCD22			
53	—		LCD21			
54	—		LCD20			
55			LCD19			
56			LCD18			
57			LCD17			
58			LCD16			
59	41	PTE7	LCD15			
60	42	PTE6	LCD14			
61	43	PTE5	LCD13			
62	44	PTE4	LCD12			
63	45	PTE3	LCD11			
64	46	PTE2	LCD10			

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08LL16 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature		T_{JM}	95	°C
Thermal resistance Single-layer board				
	64-pin LQFP	θ_{JA}	72	°C/W
	48-pin QFN		84	
	48-pin LQFP		81	
Thermal resistance Four-layer board				
	64-pin LQFP	θ_{JA}	54	°C/W
	48-pin QFN		30	
	48-pin LQFP		57	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 3-1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 3-2}$$

Solving Equation 3-1 and Equation 3-2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 3-1 and Equation 3-2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating voltage				1.8		3.6	V
2	C	Output high voltage	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P		PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8 V I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage	PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P		PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8 V I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current	Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V I_{Load} = 0.6 mA	—	—	0.5	V
	P		PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 1.8 V I_{Load} = 3 mA	—	—	0.5	
6	C	Output low voltage	PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OL}	V_{DD} > 1.8 V I_{Load} = 0.5 mA	—	—	0.5	V
	P		PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V I_{Load} = 3 mA	—	—	0.5	
	C				V_{DD} > 1.8 V I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current	Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage	all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 × V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 × V_{DD}	—	—	
9	P	Input low voltage	all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C				V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis	all digital inputs	V_{hys}		0.06 × V_{DD}	—	—	mV

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
11	P	Input leakage current	all input only pins except for LCD only pins (LCD 16-29)	$\lvert I_{In} \rvert$	$V_{In} = V_{DD}$	—	0.025	1	μA
					$V_{In} = V_{SS}$	—	0.025	1	μA
			LCD only pins (LCD 16-29)		$V_{In} = V_{DD}$	—	100	150	μA
					$V_{In} = V_{SS}$	—	0.025	1	μA
12	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\lvert I_{OZ} \rvert$	$V_{In} = V_{DD}$ or V_{SS}	—	0.025	1	μA
13	P	Total leakage current[3]	Total leakage current for all pins	$\lvert I_{InT} \rvert$	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
14	P	Pullup, pulldown resistors when enabled	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7]	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ
	P		PTA[4:5], PTD[0:7], PTE[0:7]					69.5	
15	D	DC injection current [4, 5, 6]	Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
16	C	Input capacitance, all pins		C_{In}		—	—	8	pF
17	C	RAM retention voltage		V_{RAM}		—	0.6	1.0	V
18	C	POR re-arm voltage[7]		V_{POR}		0.9	1.4	2.0	V
19	D	POR re-arm time		t_{POR}		10	—	—	μs
20	P	Low-voltage detection threshold		V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V
21	P	Low-voltage warning threshold		V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.2	V
22	P	Low-voltage inhibit reset/recover hysteresis		V_{hys}		—	80	—	mV
23	P	Bandgap voltage reference[8]		V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 All I/O pins except for LCD pins in open drain mode.

3 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

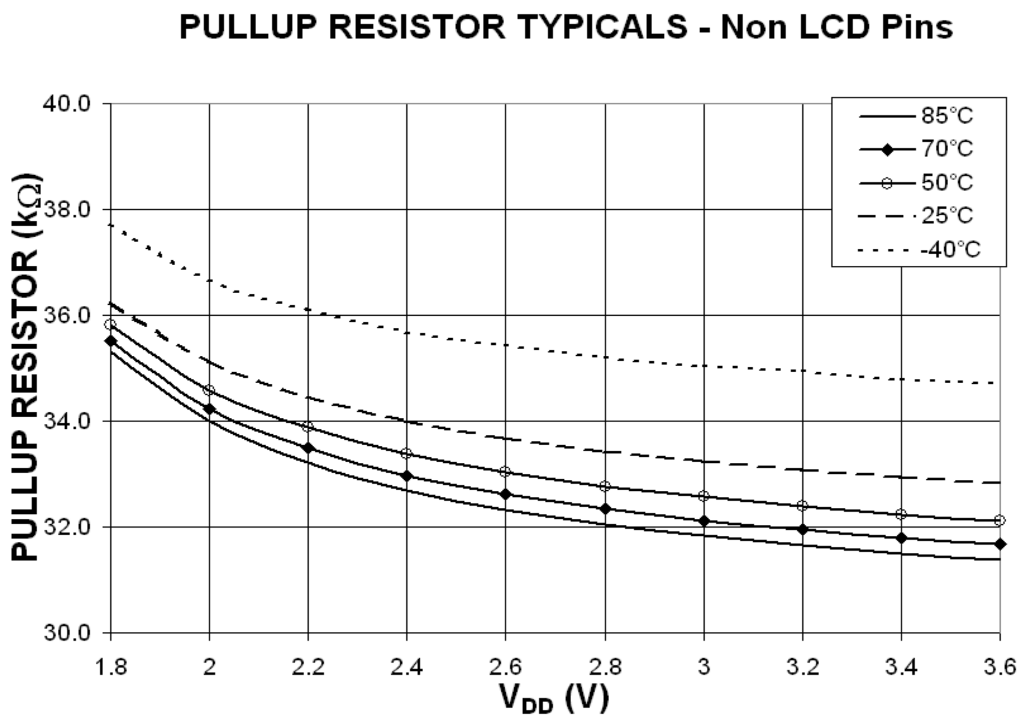
4 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 POR will occur below the minimum voltage.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C.



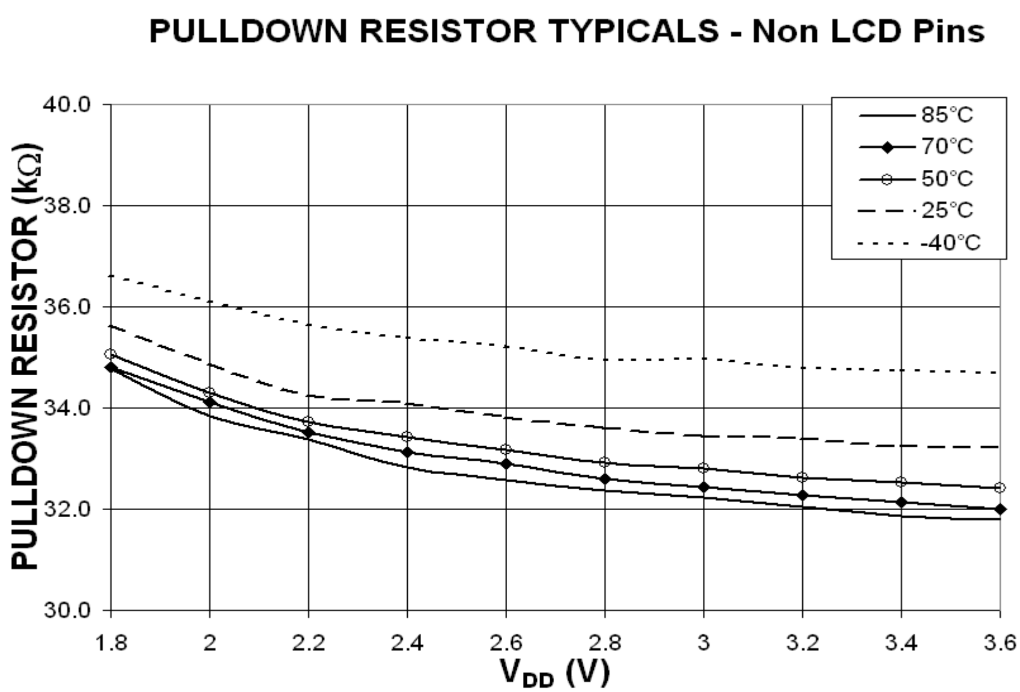


Figure 4. Non-LCD pins I/O Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

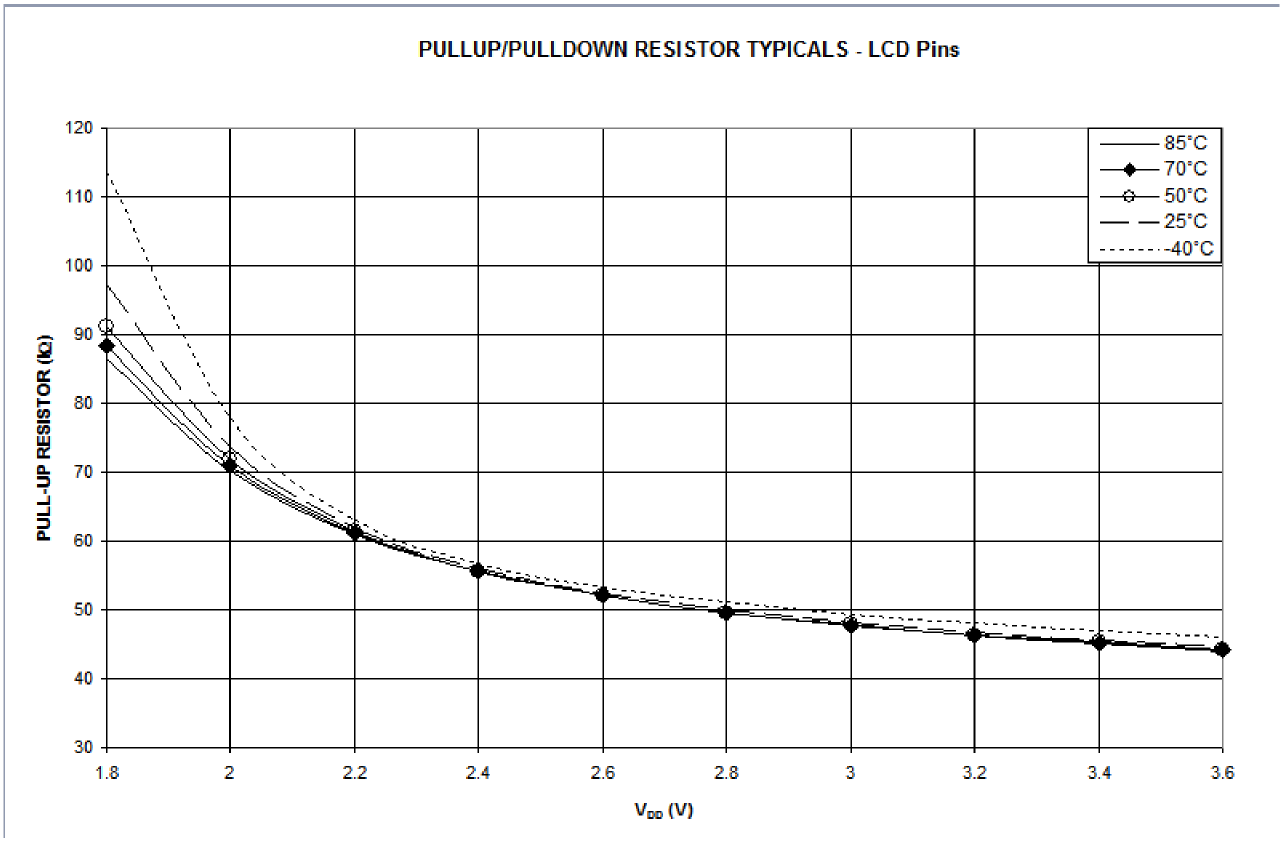


Figure 5. LCD/GPIO Pins I/O Pullup/Pulldown Typical Resistor Values

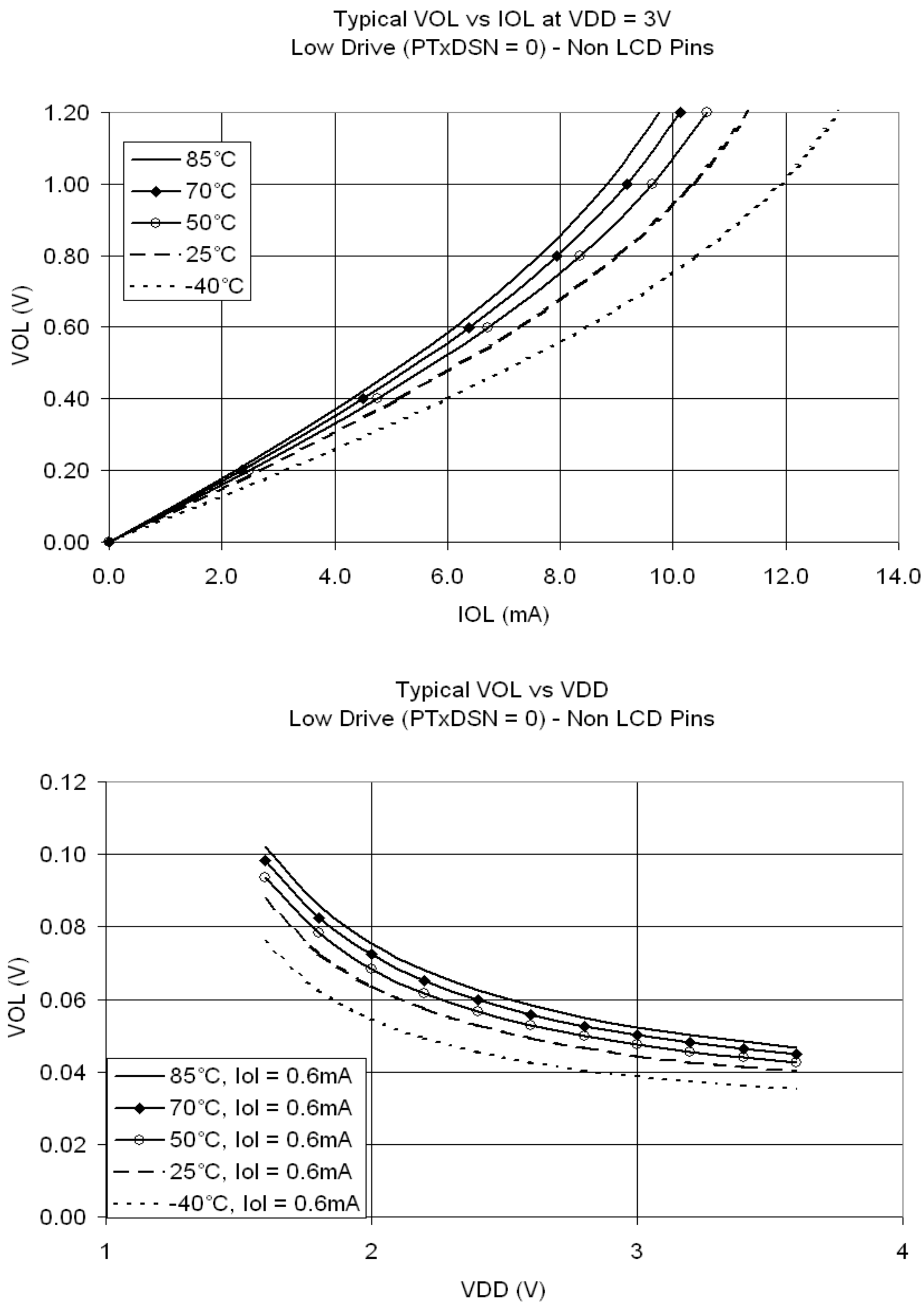
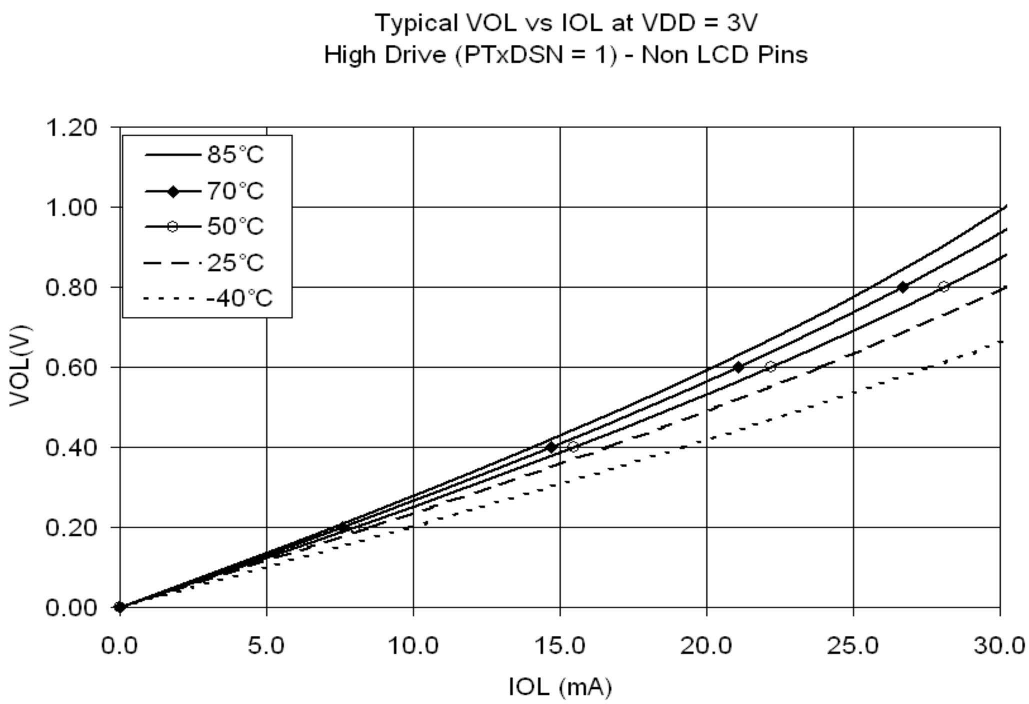


Figure 6. Typical Low-Side Driver (Sink) Characteristics (Non-LCD pins) — Low Drive (PTxDSn = 0)



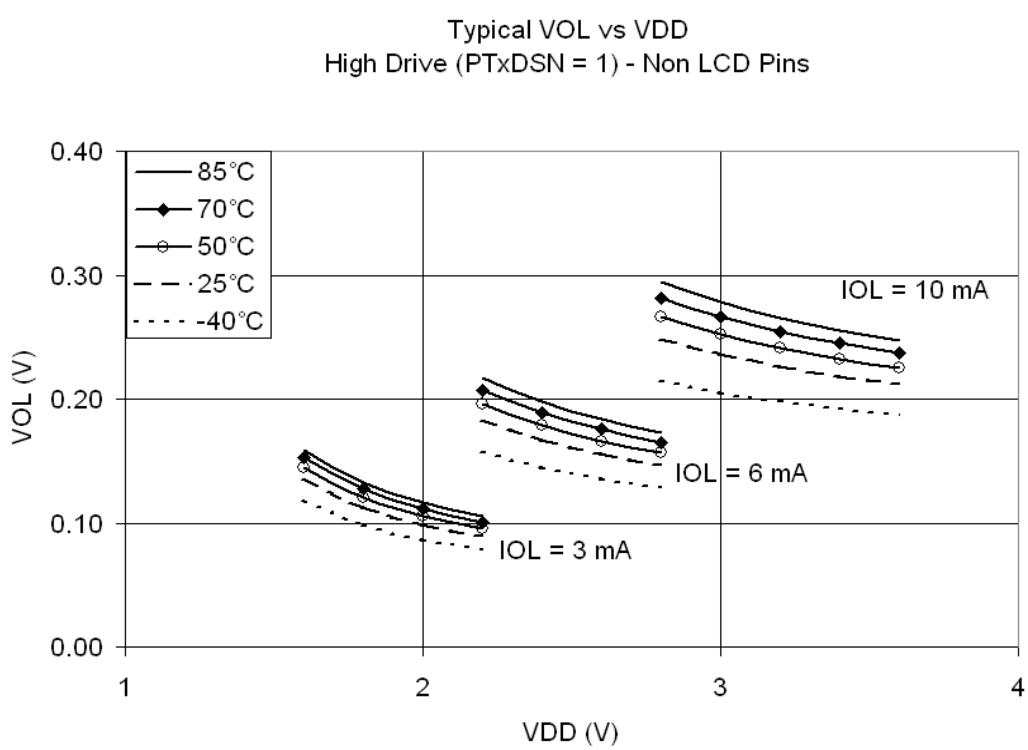
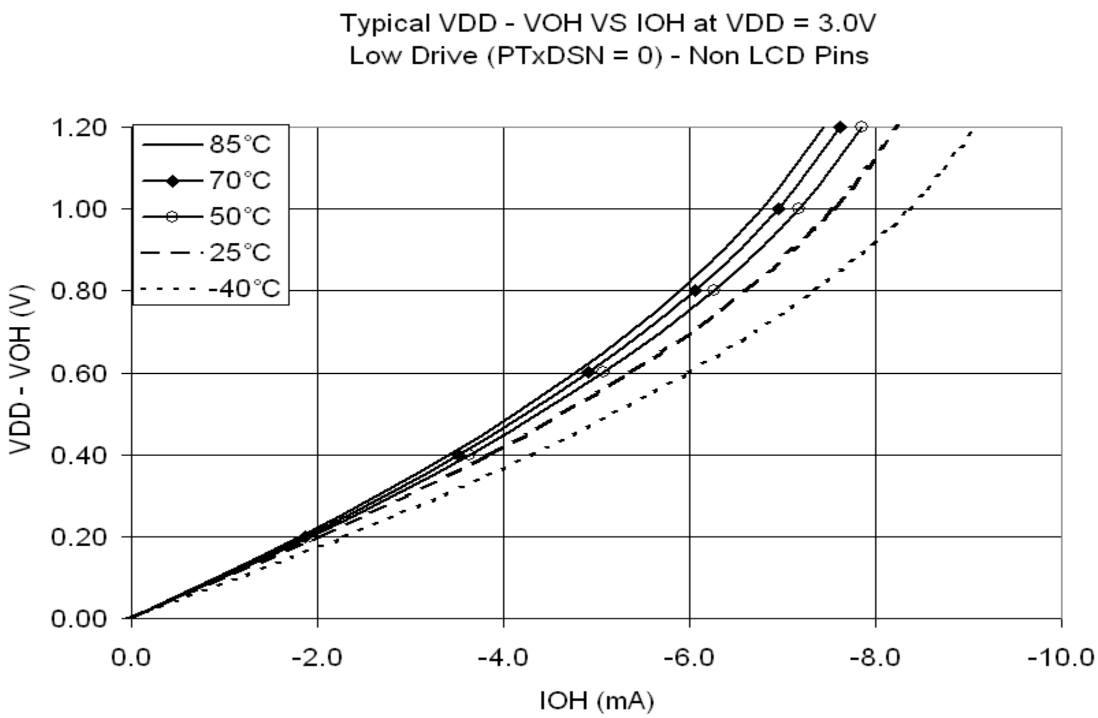


Figure 7. Typical Low-Side Driver (Sink) Characteristics(Non-LCD pins) — High Drive (PTxDSn = 1)



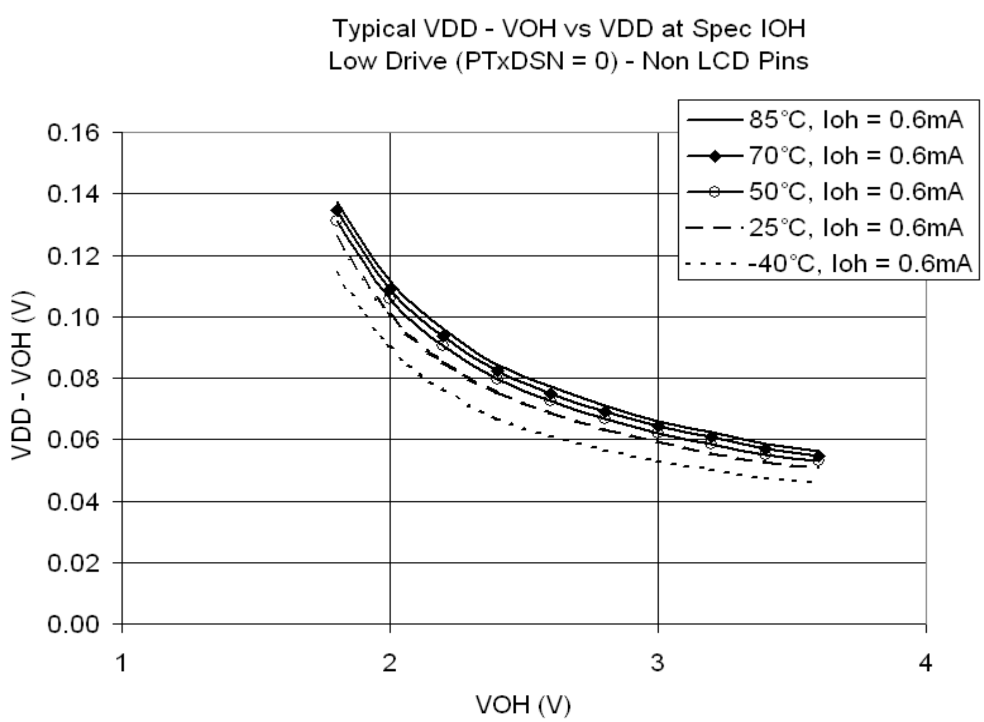


Figure 8. Typical High-Side (Source) Characteristics (Non-LCD Pins) — Low Drive (PTxDSn = 0)

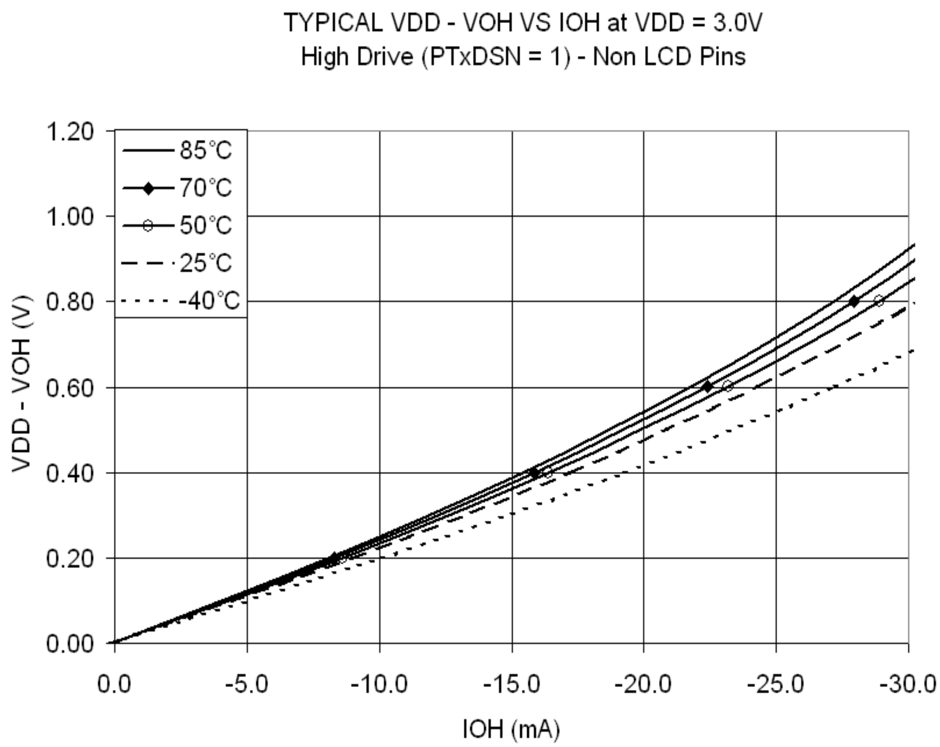
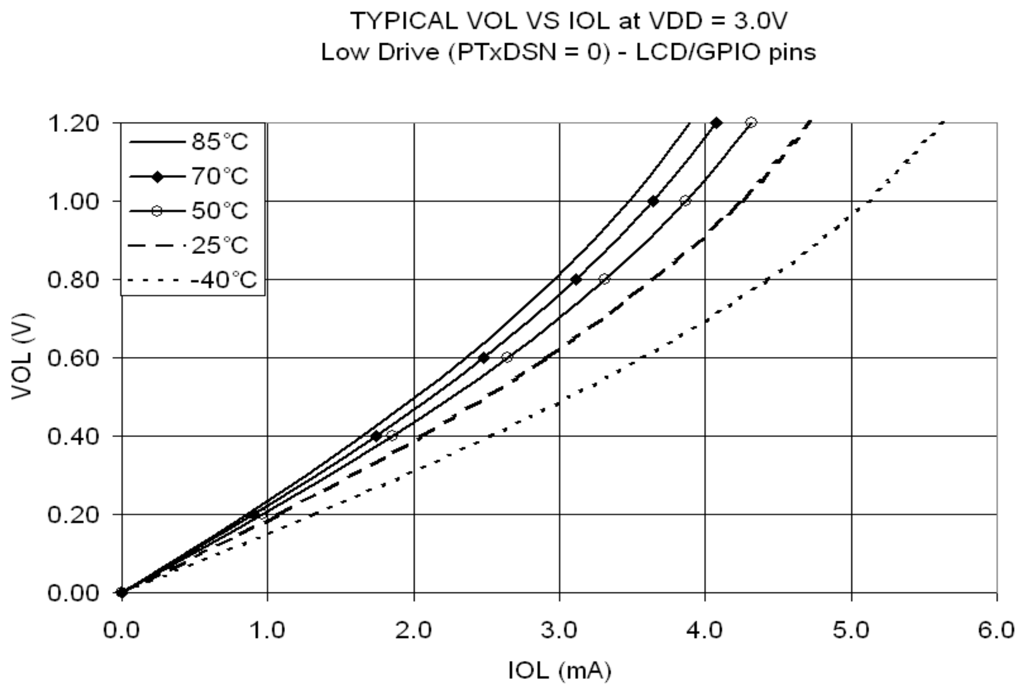


Figure 9. Typical High-Side (Source) Characteristics(Non-LCD Pins) — High Drive (PTxDSn = 1)



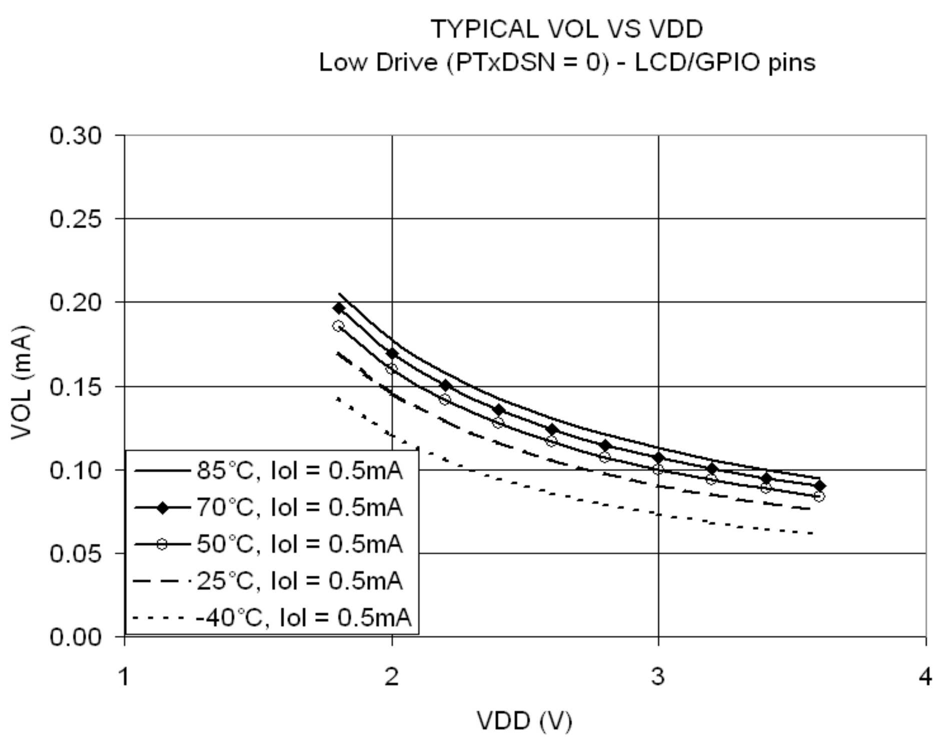


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — Low Drive (PTxDSn = 0)

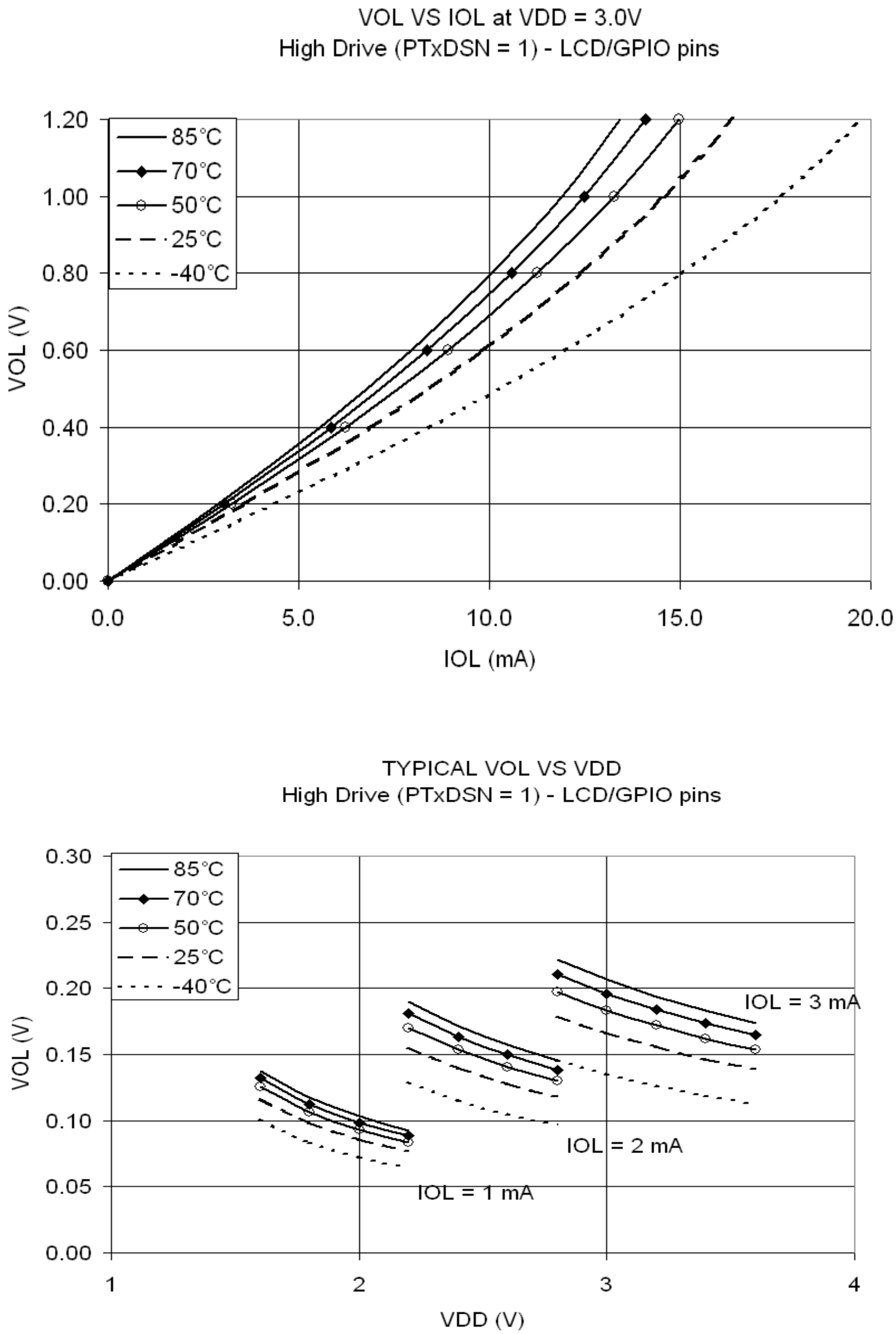
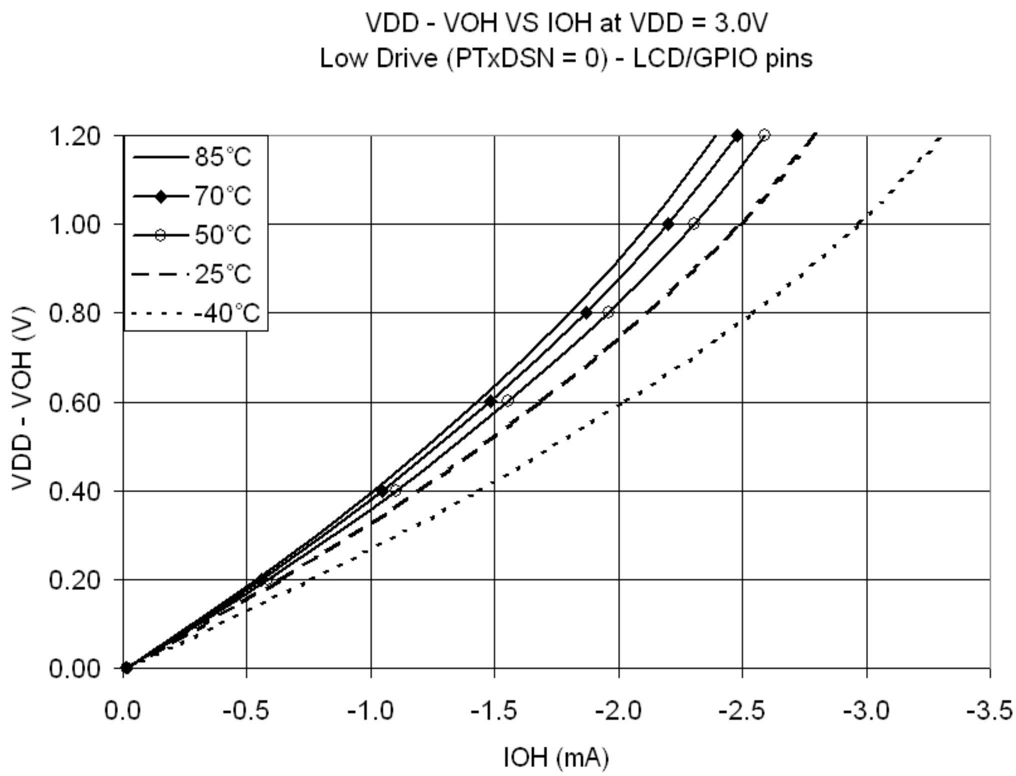


Figure 11. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO Pins) — High Drive (PTxDSn = 1)



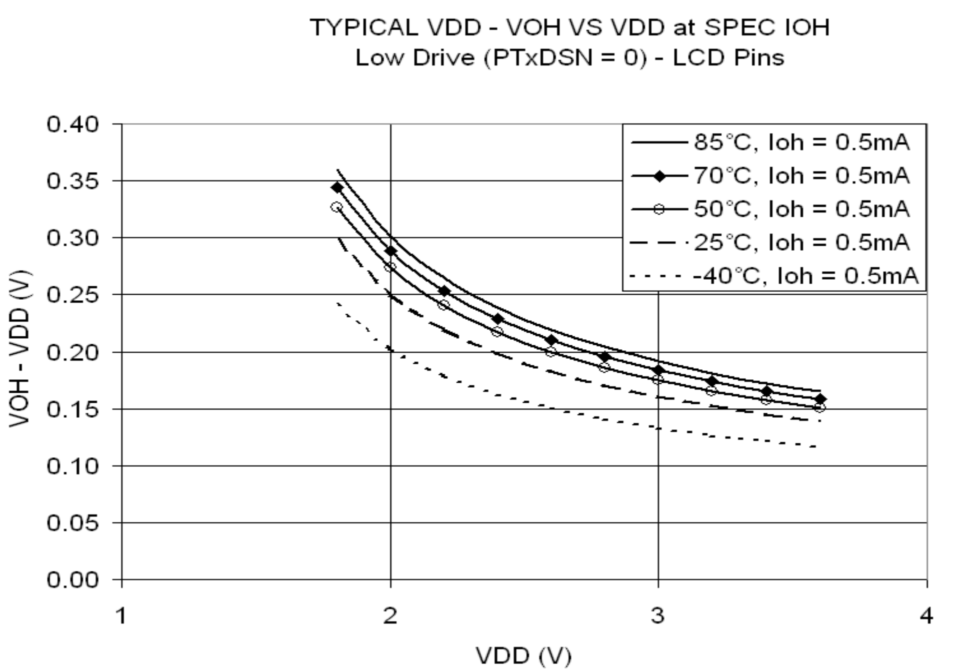
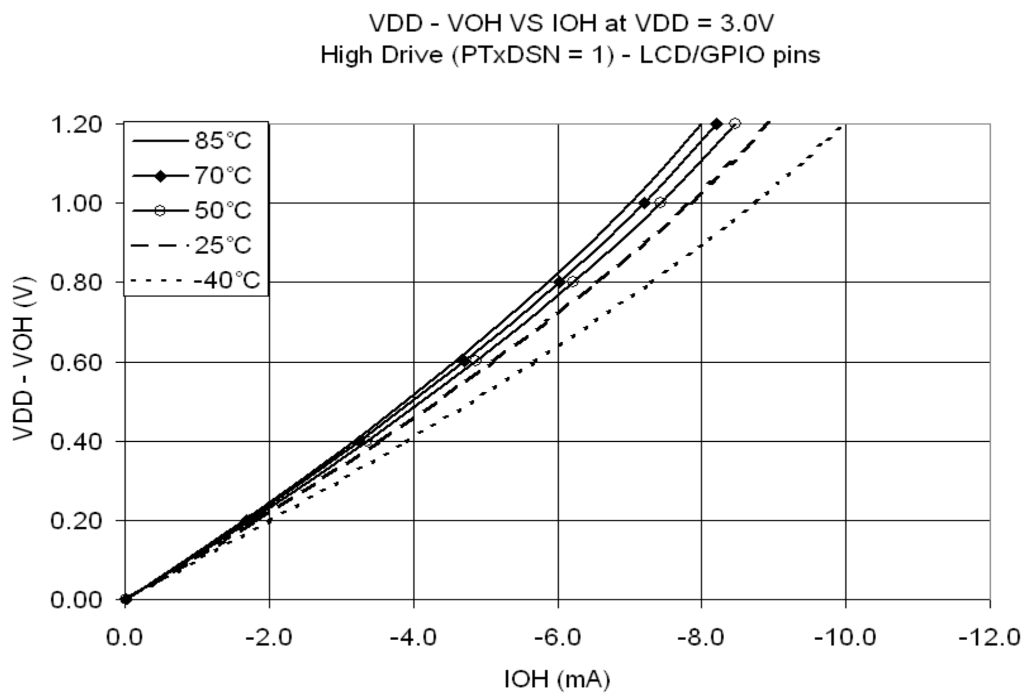


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — Low Drive (PTxDSn = 0)



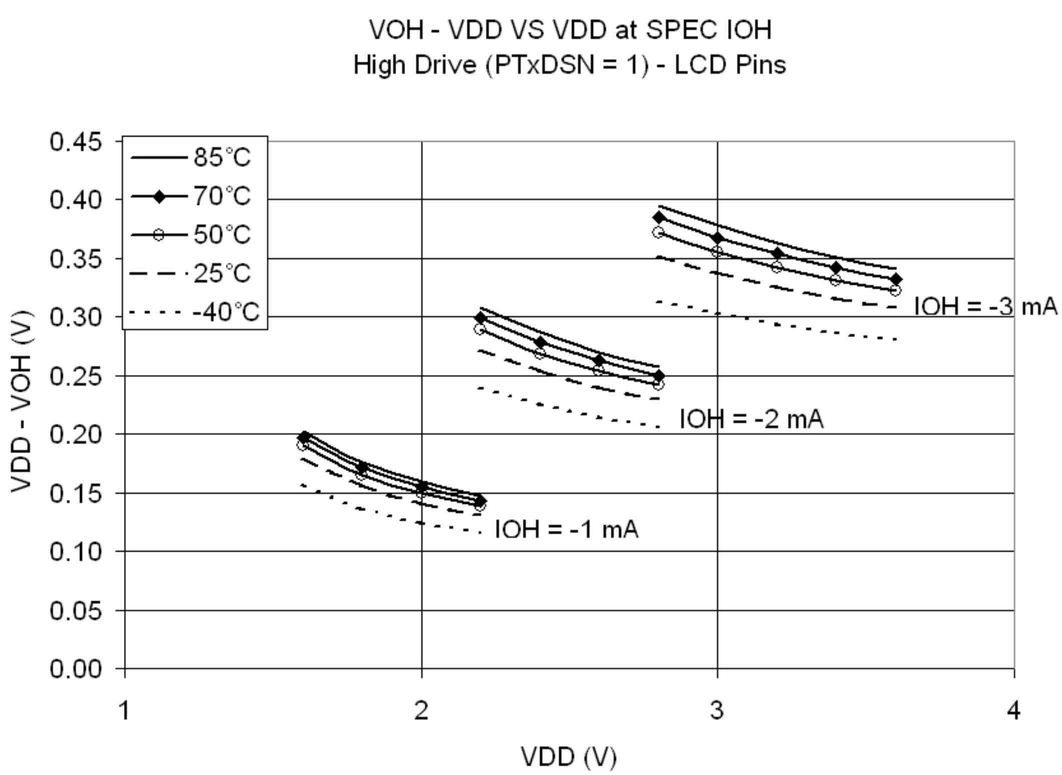


Figure 13. Typical High-Side (Source) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	8 MHz	3	4.2	5.7	mA	–40 to 85 °C
	T			1 MHz		1	1.52		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	10 MHz	3	3.60	—	mA	–40 to 85 °C
	T			1 MHz		0.50	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3	165	—	μA	–40 to 85 °C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off; running from Flash	RI_{DD}	16 kHz FBILP	3	77	—	μA	–40 to 85 °C
	T			16 kHz FBELP		21	—		
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	77	—	μA	–40 to 85 °C
	T			16 kHz FBELP		7.3	—		
6	P	Wait mode supply current FEI mode, all modules off	WI_{DD}	8 MHz	3	1.4	3.5	mA	–40 to 85 °C
	C			1 MHz		0.8	1.15		
7	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBELP	3	1.3	—	μA	–40 to 85 °C
8	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	350	930	nA	–40 to 25 °C
						1000	—		50 °C
						2500	4000		70 °C
						5100	—		85 °C
	C			n/a	2	250	—		–40 to 25 °C
						2000	—		70 °C
						4000	—		85 °C
9	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	400	1030	nA	–40 to 25 °C
						1300	—		50 °C
						4000	6000		70 °C
						8000	—		85 °C
	C			n/a	2	350	—		–40 to 25 °C
						3000	—		70 °C
						6000	—		85 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
10	C	Application Stop3 mode supply current[2]	$ApS3I_{DD}$	n/a	3	6.1	—	µA	25 °C
11	C	Application Stop3 mode supply current[2]	$ApS3I_{DD}$	n/a	3	7.5	—	µA	50 °C

1 Typical values are measured at 25 °C. Characterized, not tested.

2 32 kHz crystal enabled in low power mode. TOD module enabled. V_{IREG} enabled for 3 V LCD glass 500pf 8x24 LCD glass at 32 Hz frame rate with LCD Charge pump clock set to low setting and every other segment "on."

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				–40	25	70	85	
1	T	LPO		100	100	150	175	nA
2	T	ERREFSTEN	RANGE = HGO = 0	250	360	400	460	nA
3	T	IREFSTEN[1]		63	70	77	81	µA
4	T	TOD	Does not include clock source current	50	50	75	100	nA
5	T	LVD[1]	LVDSE = 1	110	110	112	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	12	12	20	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	95	101	120	µA
8	T	LCD	VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 Segments, 32Hz frame rate, No LCD glass connected.	1	1	4.2	12	µA

1 Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Refer to Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	f_{lo} f_{hi} f_{hi}	32 1 1	— — —	38.4 16 8	kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	— — —	— 10 1	— — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	— 100 0 0 0 0	— — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	t_{CSTL} t_{CSTH}	— — — —	600 400 5 15	— — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.
[2] Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.
[3] See crystal or resonator manufacturer's recommendation.
[4] Proper PC board layout procedures must be followed to achieve specifications.

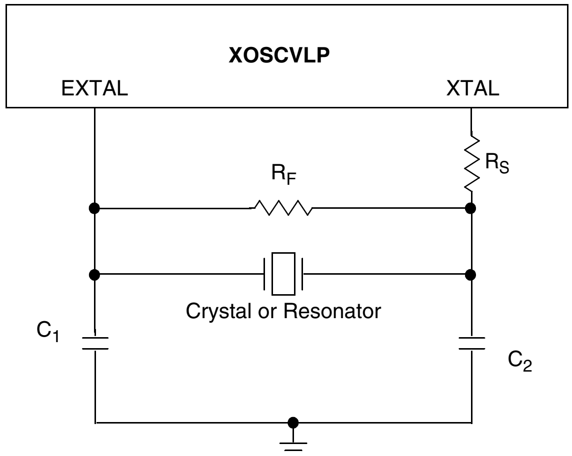


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

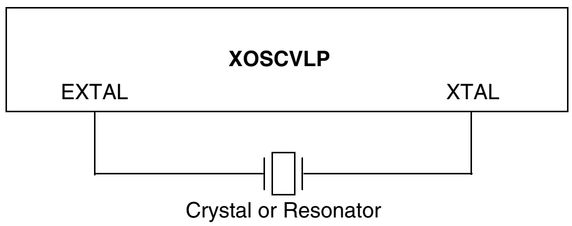


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - trimmed	f_{int_t}	31.25	—	39.063	kHz
3	T	Internal reference start-up time	t_{IRST}	—	—	6	μs
4	P	DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
5	P	DCO output frequency range - trimmed	f_{dco_t}	16	—	20	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	C	Total deviation from trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 –1.0	±2	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time [2]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

[2] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[3] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

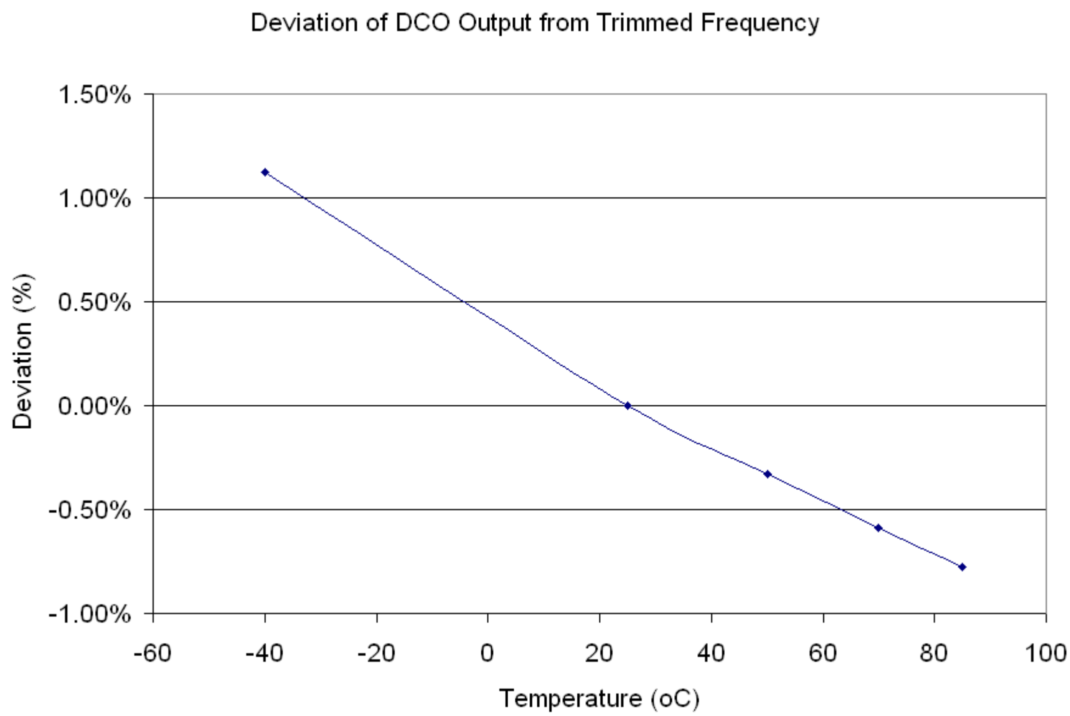


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage Regulator Recovery time	t_{VRR}	—	6	10	us

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.
2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.
6 Except for LCD pins in Open Drain mode.

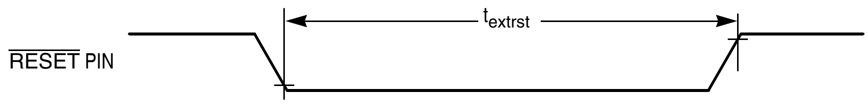


Figure 17. Reset Timing

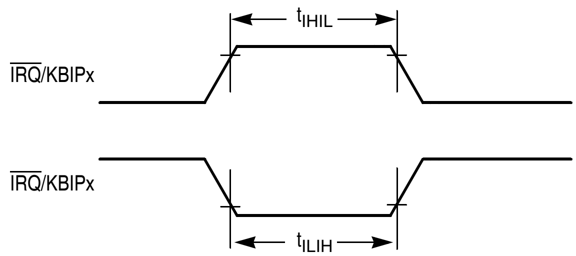


Figure 18. $\overline{IRQ}$/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TP Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

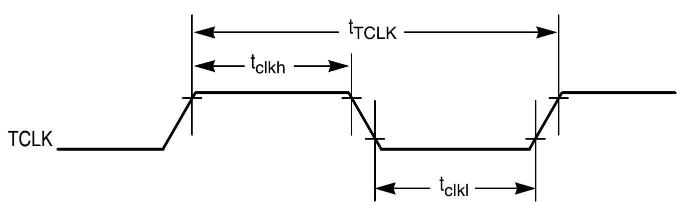


Figure 19. Timer External Clock

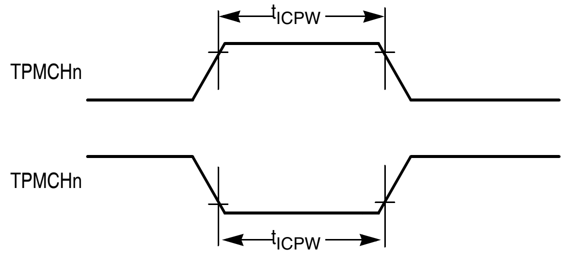


Figure 20. Timer Input Capture Pulse

3.10.3 SPI Timing

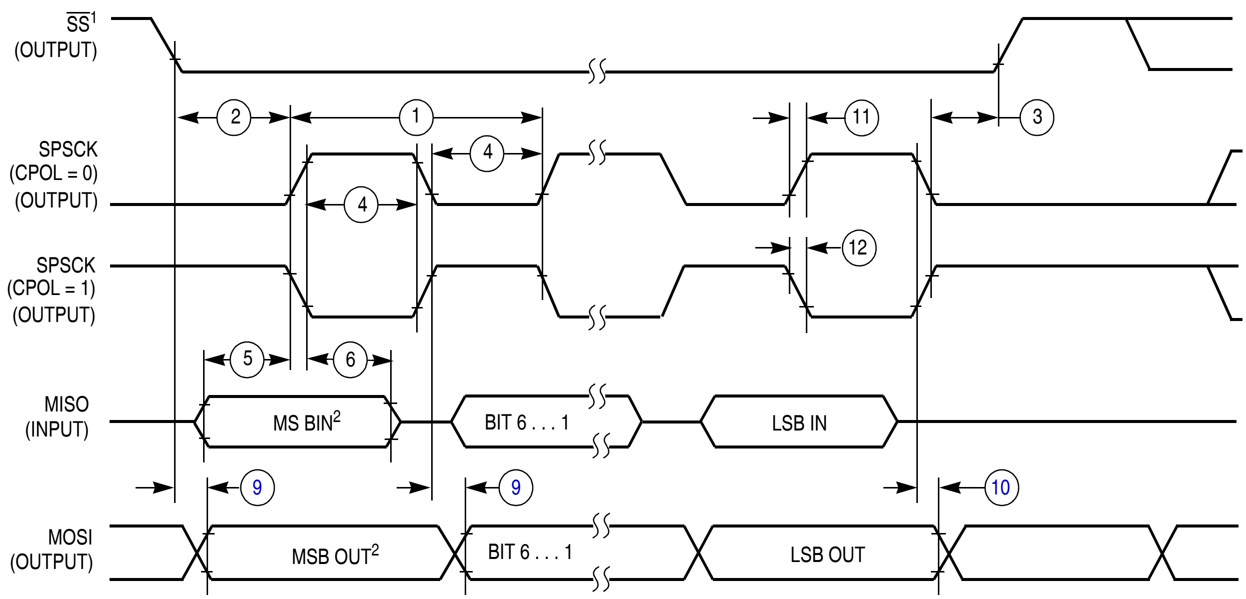
Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns

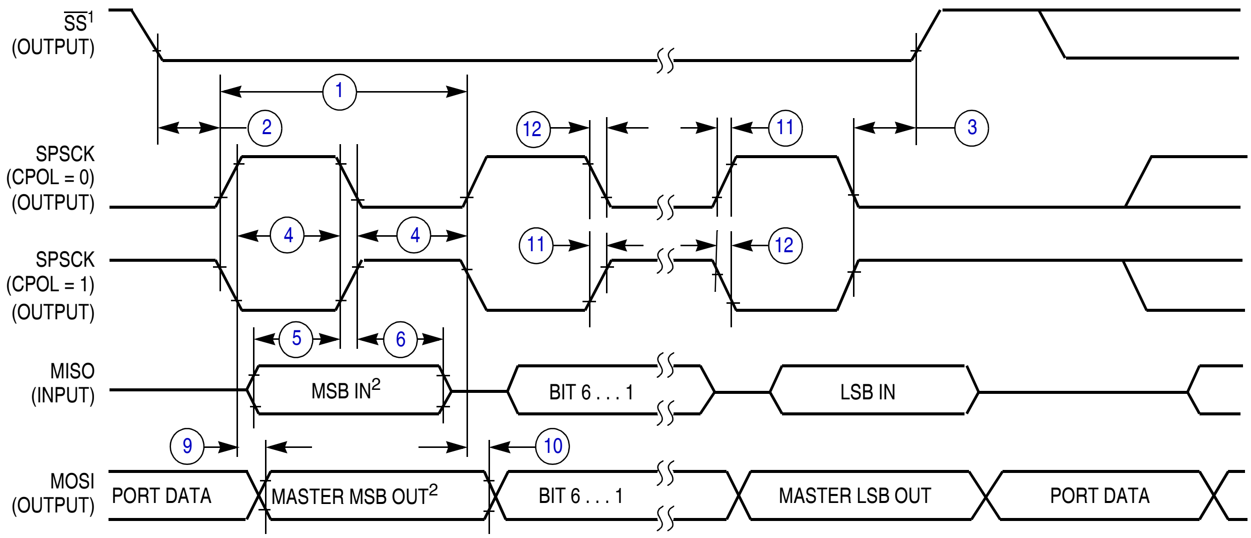
Table 15. SPI Timing (continued)

No.	C	Function	Symbol	Min	Max	Unit
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



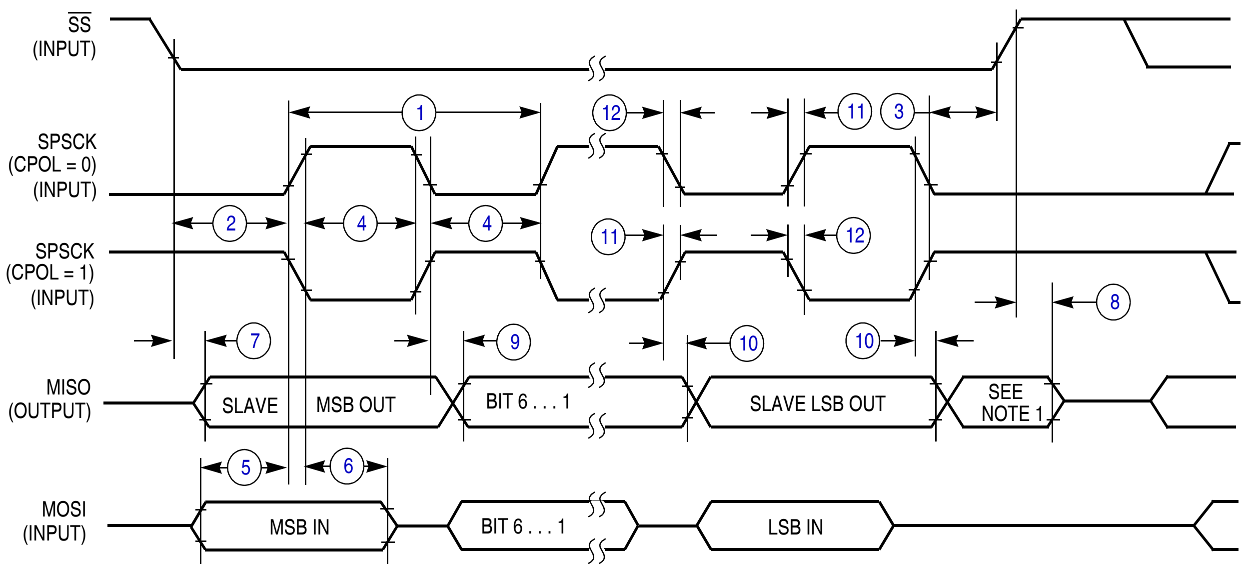
NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)



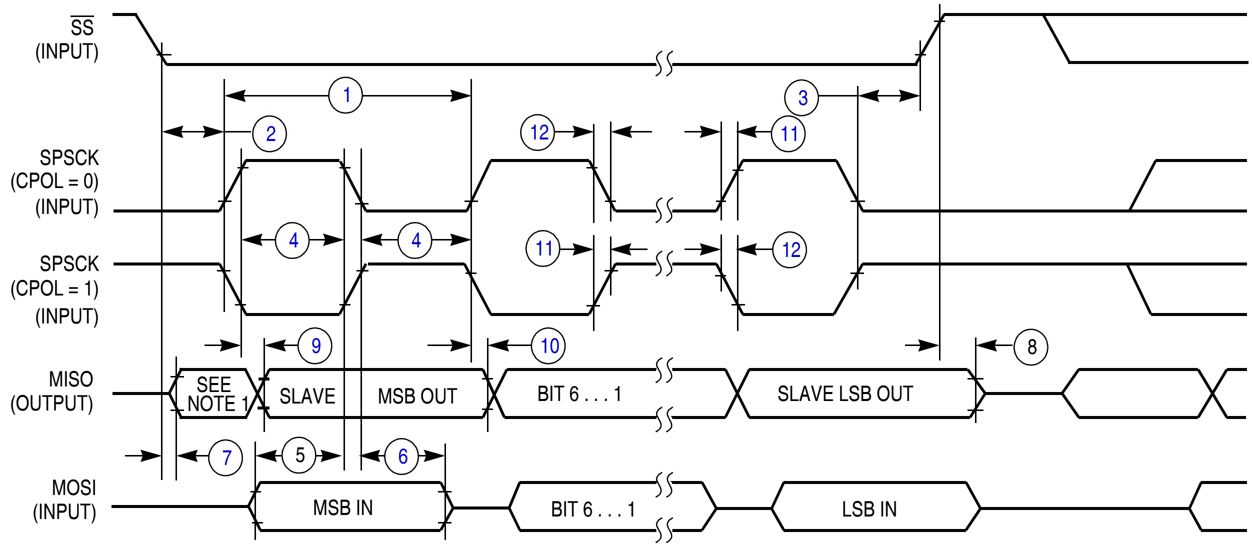
NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)



NOTE:
1. Not defined but normally MSB of character just received.

Figure 23. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received.

Figure 24. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
C	Supply current (active)	I_{DDAC}	—	20	35	μA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}		20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 17. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
	Delta to V_{DD} $(V_{DD}-V_{DDA})^2$	ΔV_{DDA}	–100	0	100	mV	
Ground voltage	Delta to V_{SS} $(V_{SS}-V_{SSA})^2$	ΔV_{SSA}	–100	0	100	mV	

Table 17. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Ref Voltage High		V_{REFH}	1.8	V_{DDA}	V_{DDA}	V	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	5	7	kΩ	
Analog Source Resistance	12-bit mode $f_{ADCK} > 4MHz$ $f_{ADCK} < 4MHz$	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode $f_{ADCK} > 4MHz$ $f_{ADCK} < 4MHz$		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

[1] Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

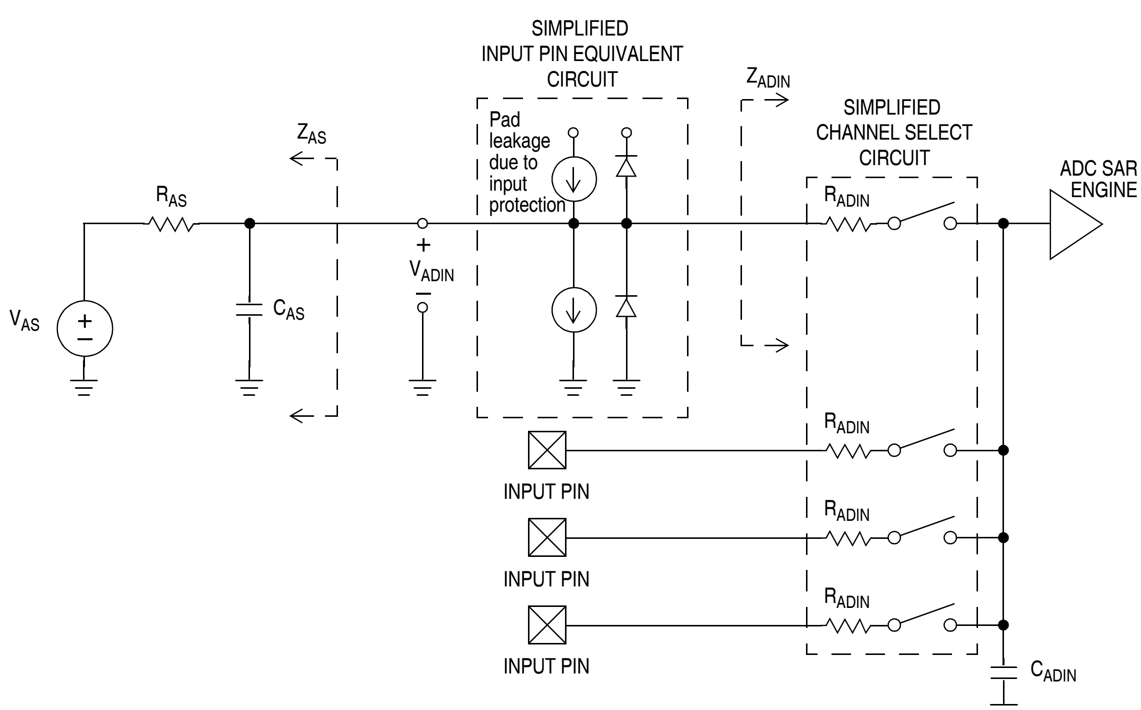


Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC=1 ADLSMP=1 ADCO=1		I_{DDA}	—	120	—	µA	
T	Supply Current ADLPC=1 ADLSMP=0 ADCO=1		I_{DDA}	—	200	—	µA	
T	Supply Current ADLPC=0 ADLSMP=1 ADCO=1		I_{DDA}	—	290	—	µA	
P	Supply Current ADLPC=0 ADLSMP=0 ADCO=1		I_{DDA}	—	0.53	1	mA	
P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
C		Low Power (ADLPC=1)		1.25	2	3.3		
P	Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See ADC chapter in the LL16 Reference Manual for conversion time variances
C		Long Sample (ADLSMP=1)		—	40	—		
P	Sample Time	Short Sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
C		Long Sample (ADLSMP=1)		—	23.5	—		
T	Total Unadjusted Error	12-bit mode, 3.6>VDDA>2.7V	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
		12-bit mode, 2.7>VDDA>1.8V		—	–1 to 3	–3.0 to 6.0		
P		10-bit mode		—	±1	±2.5		
T		8-bit mode		—	±0.5	±1.0		
T	Differential Non-Linearity	12-bit mode	DNL	—	±1	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
T		8-bit mode[3]		—	±0.3	±0.5		
T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	–2.5 to 1.0	LSB[2]	
P		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		

Table 18. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Zero-Scale Error	12-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
P		10-bit mode		—	±0.5	±1.5		
T		8-bit mode		—	±0.5	±0.5		
T	Full-Scale Error	12-bit mode	E_{FS}	—	±1	–3.5 to 1.0	LSB[2]	$V_{ADIN} = V_{DDA}$
P		10-bit mode		—	±0.5	±1		
T		8-bit mode		—	±0.5	±0.5		
D	Quantization Error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		
D	Input Leakage Error	12-bit mode	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		
D	Temp Sensor Slope	–40 °C to 25 °C	m	—	1.646	—	mV/°C	
		25 °C to 85 °C		—	1.769	—		
D	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} – V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

3.13 LCD Specifications

Table 19. LCD Electricals, 3 V Glass

C	Characteristic		Symbol	Min	Typ	Max	Unit
D	LCD Supply Voltage		V_{LCD}	0.9	1.5	1.8	V
D	LCD Frame Frequency		f_{Frame}	28	30	58	Hz
D	LCD Charge Pump Capacitance		C_{LCD}		100	100	nF
D	LCD Bypass Capacitance		C_{BYLCD}		100	100	nF
D	LCD Glass Capacitance		C_{glass}		2000	8000	pF
D	V_{IREG}	HRefSel = 0	V_{IREG}	.89	1.00	1.15	V
		HRefSel = 1		1.49	1.67	1.85[1]	
D	V_{IREG} TRIM Resolution		Δ_{RTRIM}	1.5			% V_{IREG}
D	V_{IREG} Ripple	HRefSel = 0				0.1	V
		HRefSel = 1				0.15	
D	V_{LCD} Buffered Adder[2]		I_{Buff}		1		µA

[1] V_{IREG} Max can not exceed V_{DD} – 0.15 V

[2] VSUPPLY = 10, BYPASS = 0

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 20. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{prog/erase}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	μs
P	Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
D	Byte program current[3]	RI_{DDBP}	—	4	—	mA
D	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 Typical endurance for FLASH was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.15.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 21. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 3.3 V T_A = 25 °C package type 64-pin LQFP	0.15 – 50 MHz	32 kHz crystal 10 MHz bus	–7	dBμV
			50 – 150 MHz		–9	
			150 – 500 MHz		–6	
			500 – 1000 MHz		–6	
			IEC Level		N	—
			SAE Level		1	—

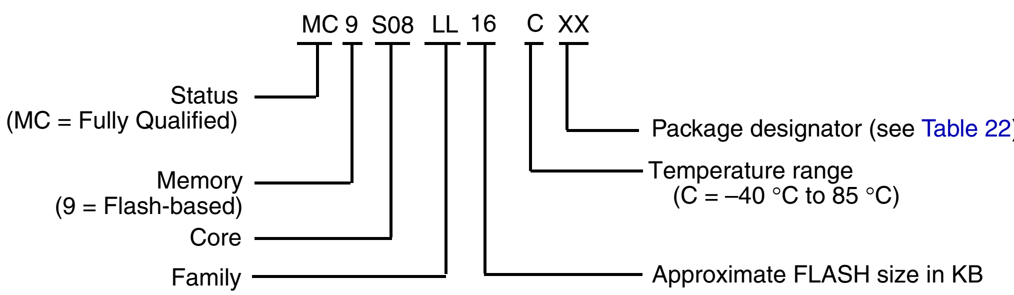
[1] Data based on qualification test results.

4 Ordering Information

This section contains the ordering information and the device numbering system for the MC9S08LL16 Series.

4.1 Device Numbering System

Example of the device numbering system:



5 Package Information and Mechanical Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08LL16 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 22) in the “Enter Keyword” search box at the top of the page.

Table 22. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A
48	Quad Flat No-Leads	QFN	GT	1314	98ARH99048A

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