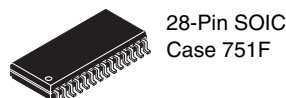
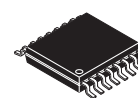
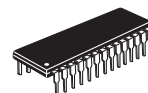


MC9S08SE8


28-Pin SOIC
Case 751F

16-Pin TSSOP
Case 948F-01

28-Pin PDIP
Case 710-02

MC9S08SE8 Series

Covers: MC9S08SE8
MC9S08SE4

Features:

- 8-Bit HCS08 Central Processor Unit (CPU)
 - 20 MHz HCS08 CPU (central processor unit)
 - 10 MHz internal bus frequency
 - HC08 instruction set with added BGND
 - Support for up to 32 interrupt/reset sources
- On-Chip Memory
 - Up to 8 KB of on-chip in-circuit programmable flash memory with block protection and security options
 - Up to 512 bytes of on-chip RAM
- Power-Saving Modes
 - Wait plus two stops
- Clock Source Options
 - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 10 MHz.
- System Protection
 - Optional computer operating properly (COP) reset with option to run from independent 1 kHz internal clock source or the bus clock
 - Low voltage detection
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- Development Support
 - Single-wire background debug interface
 - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
 - **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
 - **ADC** — 10-channel, 10-bit resolution; 2.5 μ s conversion time; automatic compare function; 1.7 mV/ $^{\circ}$ C temperature sensor; internal bandgap reference channel; runs in stop3
 - **TPMx** — One 2-channel (TPM1) and one 1-channel (TPM2) 16-bit timer/pulse-width modulator (TPM) modules; selectable input capture, output compare, and edge-aligned PWM capability on each channel; timer module may be configured for buffered, centered PWM (CPWM) on all channels
 - **KBI** — 8-pin keyboard interrupt module
 - **RTC** — Real-time counter with binary- or decimal-based prescaler
- Input/Output
 - Software selectable pullups on ports when used as inputs
 - Software selectable slew rate control on ports when used as outputs
 - Software selectable drive strength on ports when used as outputs
 - Master reset pin and power-on reset (POR)
 - Internal pullup on $\overline{\text{RESET}}$, IRQ, and BKGD/MS pins to reduce customer system cost
- Package Options
 - 28-pin PDIP
 - 28-pin SOIC
 - 16-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to: freescale.com

The following revision history table summarizes changes contained in this document.

| Revision | Date | Description of Changes |
|----------|-----------|--|
| 1 | 10/8/2008 | Initial public released. |
| 2 | 1/16/2009 | In Table 8 , added the Max. of S2I _{DD} and S3I _{DD} in 0–105 °C; changed the Max. of S2I _{DD} and S3I _{DD} in 0–85 °C; changed the typical of S2I _{DD} and S3I _{DD} ; changed the S23I _{DDRTI} to P. |
| 3 | 4/7/2009 | Added I _{OZTOT} in the Table 7 . Changed V _{DDAD} to V _{DDA} , V _{SSAD} to V _{SSA} . Updated Table 9 , Table 10 , Table 11 , and Table 12 . Updated Figure 13 and Figure 14 . |
| 4 | 4/10/2015 | Updated Table 9 . |

Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9S08SE8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9S08SE8 series MCUs.

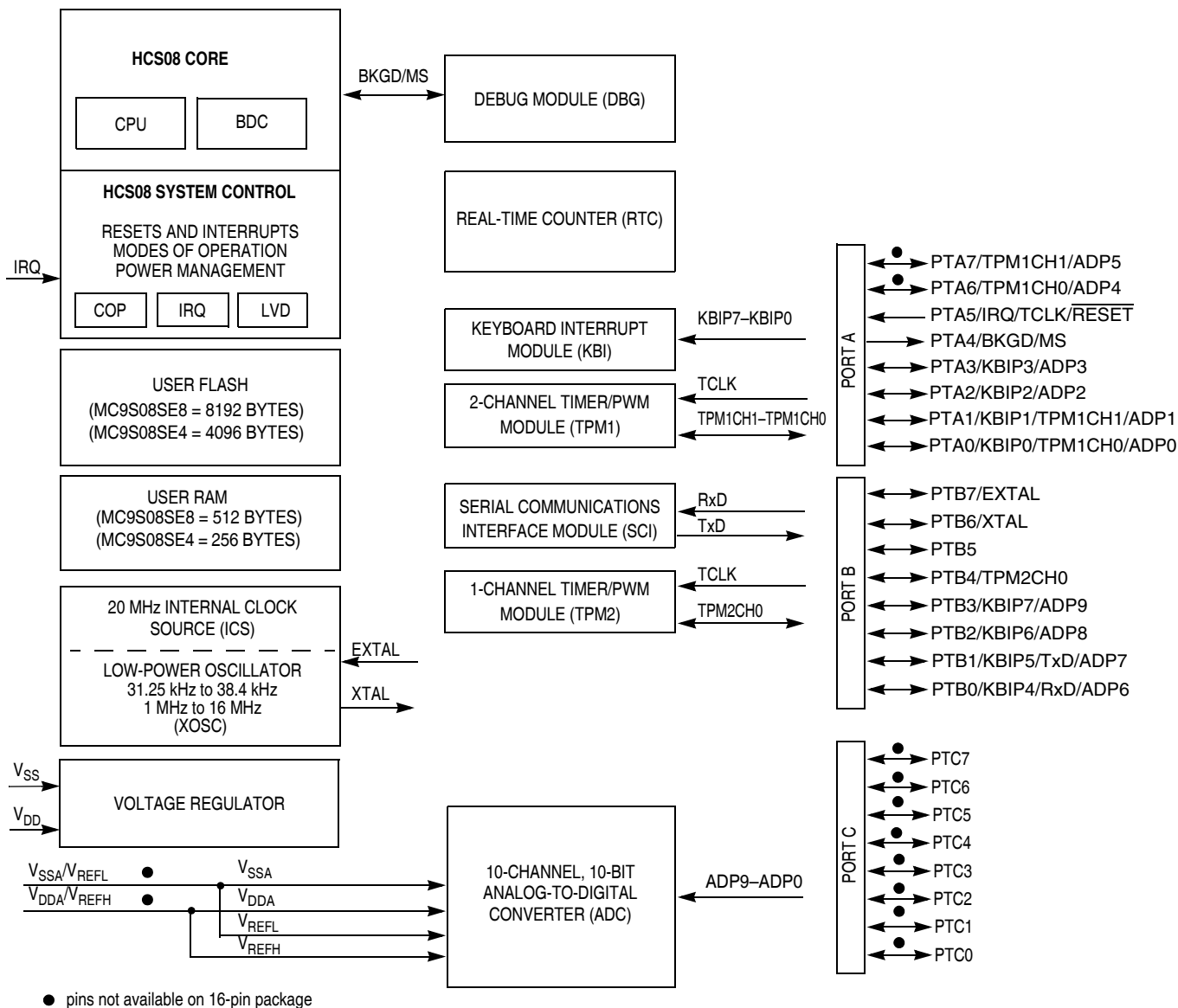


Figure 1. MC9S08SE8 Series Block Diagram

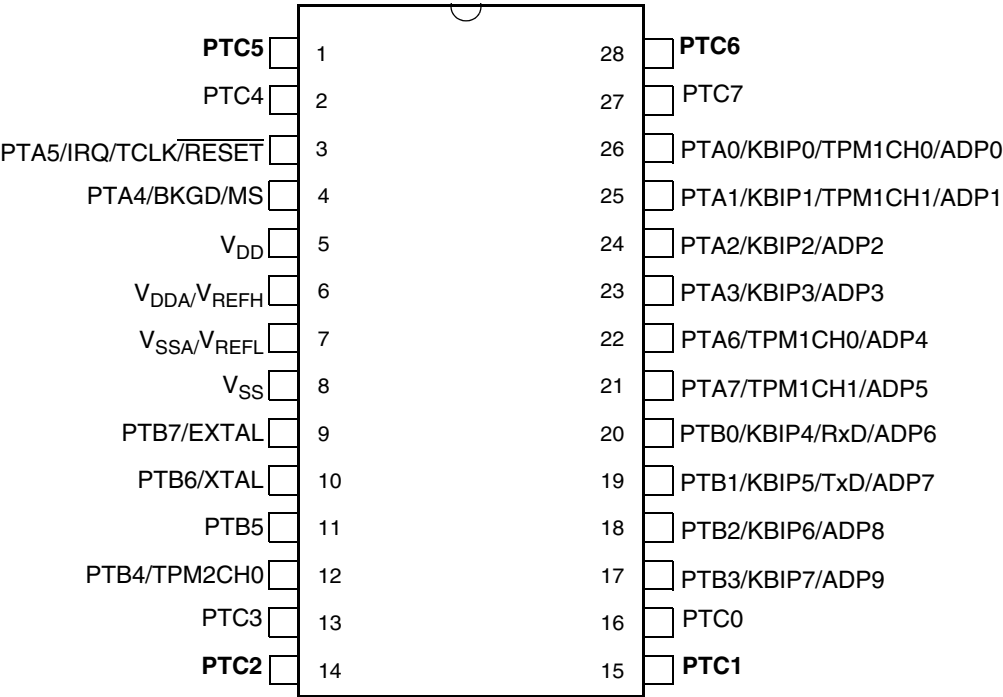
2 Pin Assignments

This chapter shows the pin assignments in the packages available for the MC9S08SE8 series.

Table 1. Pin Availability by Package Pin-Count

| Pin Number (Package) | | <-- Lowest Priority --> Highest | | | |
|-------------------------|---------------|---------------------------------|-------|----------------------|-------------------|
| 28 (SOIC/PDIP) | 16 (TSSOP) | Port Pin | Alt 1 | Alt 2 | Alt 3 |
| 1 | — | PTC5 | | | |
| 2 | — | PTC4 | | | |
| 3 | 1 | PTA5 | IRQ | TCLK | RESET |
| 4 | 2 | PTA4 | | BKGD | MS |
| 5 | 3 | | | | V _{DD} |
| 6 | — | | | V _{DDA} | V _{REFH} |
| 7 | — | | | V _{SSA} | V _{REFL} |
| 8 | 4 | | | | V _{SS} |
| 9 | 5 | PTB7 | EXTAL | | |
| 10 | 6 | PTB6 | XTAL | | |
| 11 | 7 | PTB5 | | | |
| 12 | 8 | PTB4 | | TPM2CH0 | |
| 13 | — | PTC3 | | | |
| 14 | — | PTC2 | | | |
| 15 | — | PTC1 | | | |
| 16 | — | PTC0 | | | |
| 17 | 9 | PTB3 | KBIP7 | | ADP9 |
| 18 | 10 | PTB2 | KBIP6 | | ADP8 |
| 19 | 11 | PTB1 | KBIP5 | TxD | ADP7 |
| 20 | 12 | PTB0 | KBIP4 | RxD | ADP6 |
| 21 | — | PTA7 | | TPM1CH1 ¹ | ADP5 |
| 22 | — | PTA6 | | TPM1CH0 ¹ | ADP4 |
| 23 | 13 | PTA3 | KBIP3 | | ADP3 |
| 24 | 14 | PTA2 | KBIP2 | | ADP2 |
| 25 | 15 | PTA1 | KBIP1 | TPM1CH1 ¹ | ADP1 |
| 26 | 16 | PTA0 | KBIP0 | TPM1CH0 ¹ | ADP0 |
| 27 | — | PTC7 | | | |
| 28 | — | PTC6 | | | |

¹ TPM1 pins can be remapped to PTA7, PTA6 and PTA1,PTA0



Pins in **bold** are lost in the next lower pin count package.

Figure 2. MC9S08SE8 Series in 28-Pin PDIP/SOIC Package

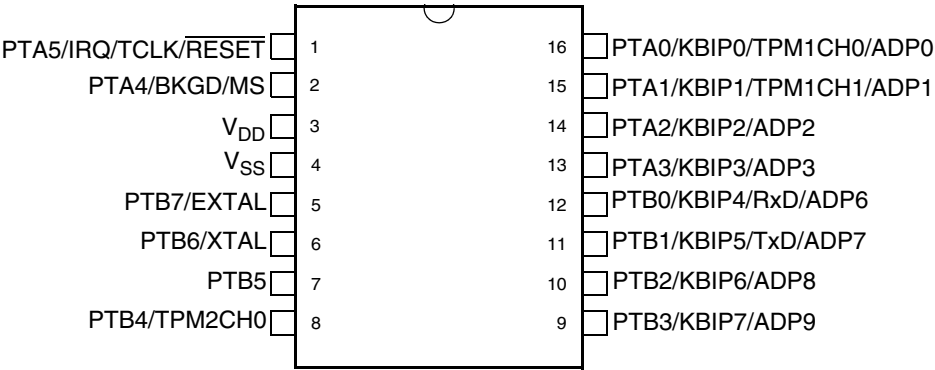


Figure 3. MC9S08SE8 in 16-Pin TSSOP Package

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

| | |
|---|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|-----------|------------------------|------|
| Supply voltage | V_{DD} | -0.3 to 5.8 | V |
| Maximum current into V_{DD} | I_{DD} | 120 | mA |
| Digital input voltage | V_{In} | -0.3 to $V_{DD} + 0.3$ | V |
| Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3} | I_D | ±25 | mA |
| Storage temperature range | T_{stg} | -55 to 150 | °C |

- ¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.
- ² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .
- ³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

| Rating | | Symbol | Value | Unit |
|--|--------------|---------------|----------------|------|
| Operating temperature range (packaged) | C | T_A | T_L to T_H | °C |
| | V | | -40 to 85 | |
| | M | | -40 to 105 | |
| | M | | -40 to 125 | |
| Maximum junction temperature | | T_{JM} | 135 | °C |
| Thermal resistance single-layer board | 28-pin SOIC | θ_{JA} | 70 | °C/W |
| | 28-pin PDIP | | 68 | |
| | 16-pin TSSOP | | 129 | |
| Thermal resistance four-layer board | 28-pin SOIC | | 48 | °C/W |
| | 28-pin PDIP | | 49 | |
| | 16-pin TSSOP | | 85 | |

Electrical Characteristics

The average chip-junction temperature (T_J) in $^{\circ}\text{C}$ can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

Where:

T_A = Ambient temperature, $^{\circ}\text{C}$

θ_{JA} = Package thermal resistance, junction-to-ambient, $^{\circ}\text{C}/\text{W}$

$P_D = P_{\text{int}} + P_{\text{I/O}}$

$P_{\text{int}} = I_{\text{DD}} \times V_{\text{DD}}$, Watts — chip internal power

$P_{\text{I/O}}$ = Power dissipation on input and output pins — user-determined

For most applications, $P_{\text{I/O}} \ll P_{\text{int}}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{\text{I/O}}$ is neglected) is:

$$P_D = K \div (T_J + 273^{\circ}\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^{\circ}\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

3.4 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|--------------------------|--------|-------|----------|
| Human body | Series resistance | R1 | 1500 | Ω |
| | Storage capacitance | C | 100 | pF |
| | Number of pulses per pin | — | 3 | — |
| Machine | Series resistance | R1 | 0 | Ω |
| | Storage capacitance | C | 200 | pF |
| | Number of pulses per pin | — | 3 | — |

Table 5. ESD and Latch-up Test Conditions (continued)

| Model | Description | Symbol | Value | Unit |
|----------|-----------------------------|--------|-------|------|
| Latch-up | Minimum input voltage limit | — | –2.5 | V |
| | Maximum input voltage limit | — | 7.5 | V |

Table 6. ESD and Latch-up Protection Characteristics

| No. | Rating ¹ | Symbol | Min | Max | Unit |
|-----|---|-----------|-------|-----|------|
| 1 | Human body model (HBM) | V_{HBM} | ±2000 | — | V |
| 2 | Machine model (MM) | V_{MM} | ±200 | — | V |
| 3 | Charge device model (CDM) | V_{CDM} | ±500 | — | V |
| 4 | Latch-up current at $T_A = 125\text{ °C}$ | I_{LAT} | ±100 | — | mA |

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.5 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

| Num | C | Parameter | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|-----------|--|----------------------|------------------|------|
| 1 | — | Operating voltage | — | 2.7 | — | 5.5 | V |
| 2 | P | Output high voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = -2\text{ mA}$ 3 V, $I_{Load} = -0.6\text{ mA}$ 5 V, $I_{Load} = -0.4\text{ mA}$ 3 V, $I_{Load} = -0.24\text{ mA}$ | V_{OH} | $V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$ | — — — — | — — — — | V |
| | | Output high voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = -10\text{ mA}$ 3 V, $I_{Load} = -3\text{ mA}$ 5 V, $I_{Load} = -2\text{ mA}$ 3 V, $I_{Load} = -0.4\text{ mA}$ | | $V_{DD} - 1.5$ $V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$ | — — — — | — — — — | |
| 3 | P | Output low voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = 2\text{ mA}$ 3 V, $I_{Load} = 0.6\text{ mA}$ 5 V, $I_{Load} = 0.4\text{ mA}$ 3 V, $I_{Load} = 0.24\text{ mA}$ | V_{OL} | 1.5 1.5 0.8 0.8 | — — — — | — — — — | V |
| | | Output low voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = 10\text{ mA}$ 3 V, $I_{Load} = 3\text{ mA}$ 5 V, $I_{Load} = 2\text{ mA}$ 3 V, $I_{Load} = 0.4\text{ mA}$ | | 1.5 1.5 0.8 0.8 | — — — — | — — — — | |
| 4 | P | Output high current — Max total I_{OH} for all ports 5 V 3 V | I_{OHT} | — — | — — | 100 60 | mA |

Table 7. DC Characteristics (continued)

| Num | C | Parameter | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|---------------|----------------------|----------------------|----------------------|------------|
| 5 | P | Output low current — Max total I_{OL} for all ports 5 V 3 V | I_{OLT} | — — | — — | 100 60 | mA |
| 6 | P | Input high voltage; all digital inputs | V_{IH} | $0.65 \times V_{DD}$ | — | — | V |
| 7 | P | Input low voltage; all digital inputs | V_{IL} | — | — | $0.35 \times V_{DD}$ | |
| 8 | P | Input hysteresis; all digital inputs | V_{hys} | $0.06 \times V_{DD}$ | — | — | mV |
| 9 | C | Input leakage current; input only pins ² | $ I_{In} $ | — | 0.1 | 1 | μA |
| 10 | P | High impedance (off-state) leakage current ² | $ I_{OZ} $ | — | 0.1 | 1 | μA |
| 11 | C | Total leakage combined for all inputs and Hi-Z pins — All input only and I/O ² | $ I_{OZTOT} $ | — | — | 2 | μA |
| 12 | P | Internal pullup resistors ³ | R_{PU} | 20 | 45 | 65 | k Ω |
| 13 | P | Internal pulldown resistors ⁴ | R_{PD} | 20 | 45 | 65 | k Ω |
| 14 | D | DC injection current ^{5, 6, 7} $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins | I_{IC} | –0.2 –5 | — — | 0.2 5 | mA |
| 15 | C | Input capacitance; all non-supply pins | C_{In} | — | — | 8 | pF |
| 16 | C | RAM retention voltage | V_{RAM} | 0.6 | 1.0 | — | V |
| 17 | P | POR re-arm voltage ⁸ | V_{POR} | 0.9 | 1.4 | 2.0 | V |
| 18 | D | POR re-arm time | t_{POR} | 10 | — | — | μs |
| 19 | P | Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising | V_{LVD1} | 3.9 4.0 | 4.0 4.1 | 4.1 4.2 | V |
| 20 | P | Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising | V_{LVD0} | 2.48 2.54 | 2.56 2.62 | 2.64 2.70 | V |
| 21 | C | Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising | V_{LVW3} | 4.5 4.6 | 4.6 4.7 | 4.7 4.8 | V |
| 22 | P | Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising | V_{LVW2} | 4.2 4.3 | 4.3 4.4 | 4.4 4.5 | V |
| 23 | P | Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising | V_{LVW1} | 2.84 2.90 | 2.92 2.98 | 3.00 3.06 | V |
| 24 | C | Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising | V_{LVW0} | 2.66 2.72 | 2.74 2.80 | 2.82 2.88 | V |

Table 7. DC Characteristics (continued)

| Num | C | Parameter | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|-----------|--------|----------------------|--------|------|
| 25 | T | Low-voltage inhibit reset/recover hysteresis 5 V 3 V | V_{hys} | — — | 100 60 | — — | mV |
| 26 | P | Bandgap voltage reference ⁹ | V_{BG} | 1.18 | 1.20 | 1.21 | V |

¹ Typical values are measured at 25 °C. Characterized, not tested.

² Measured with $V_{In} = V_{DD}$ or V_{SS} .

³ Measured with $V_{In} = V_{SS}$.

⁴ Measured with $V_{In} = V_{DD}$.

⁵ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁶ Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁷ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁸ Maximum is highest voltage that POR is guaranteed.

⁹ Factory trimmed at $V_{DD} = 5.0$ V, Temp = 25 °C.

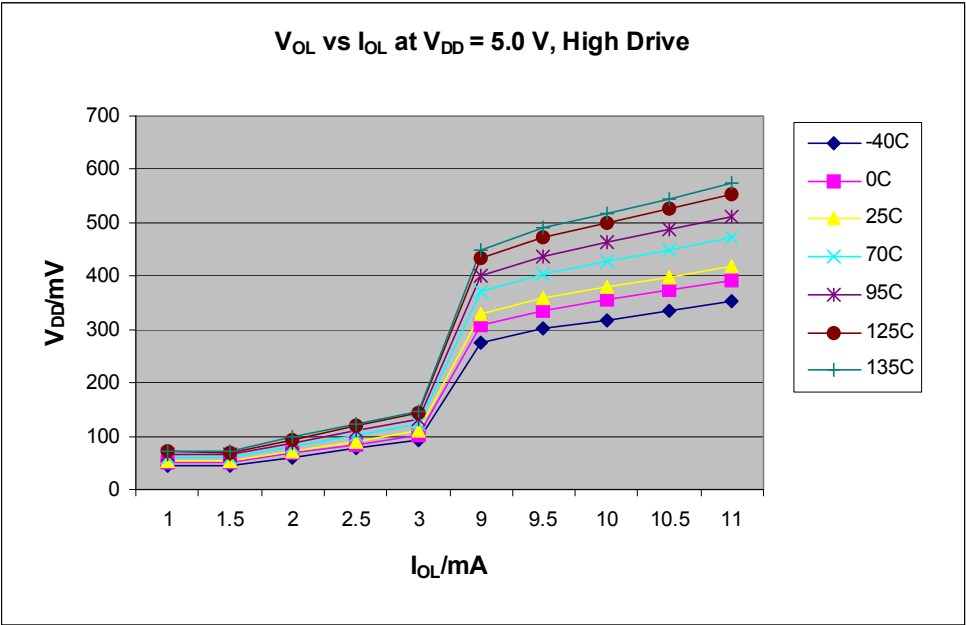


Figure 4. Typical V_{OL} vs. I_{OL} for High Drive Enabled Pad ($V_{DD} = 5$ V)

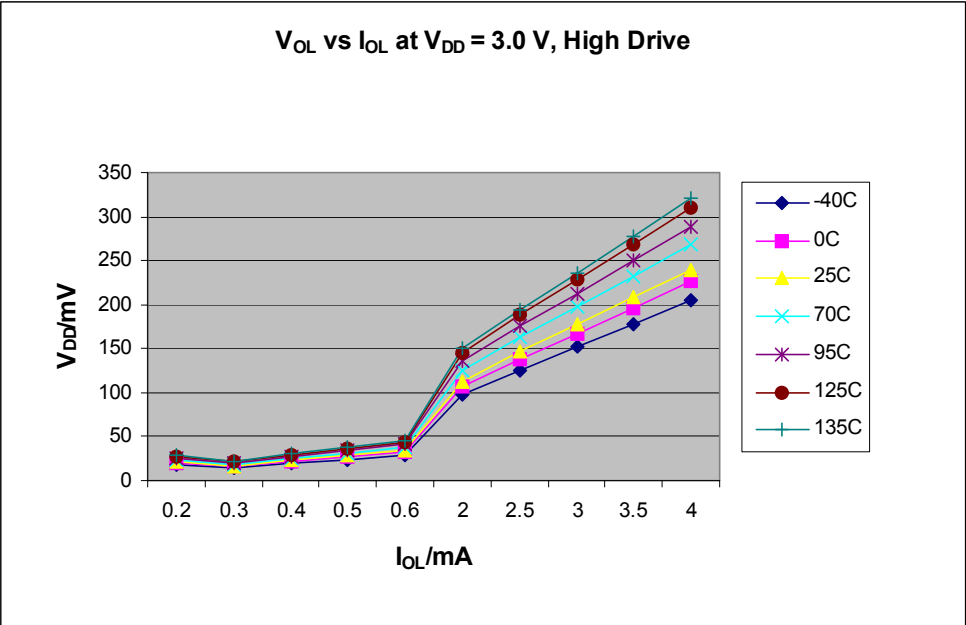


Figure 5. Typical V_{OL} vs. I_{OL} for High Drive Enabled Pad ($V_{DD} = 3$ V)

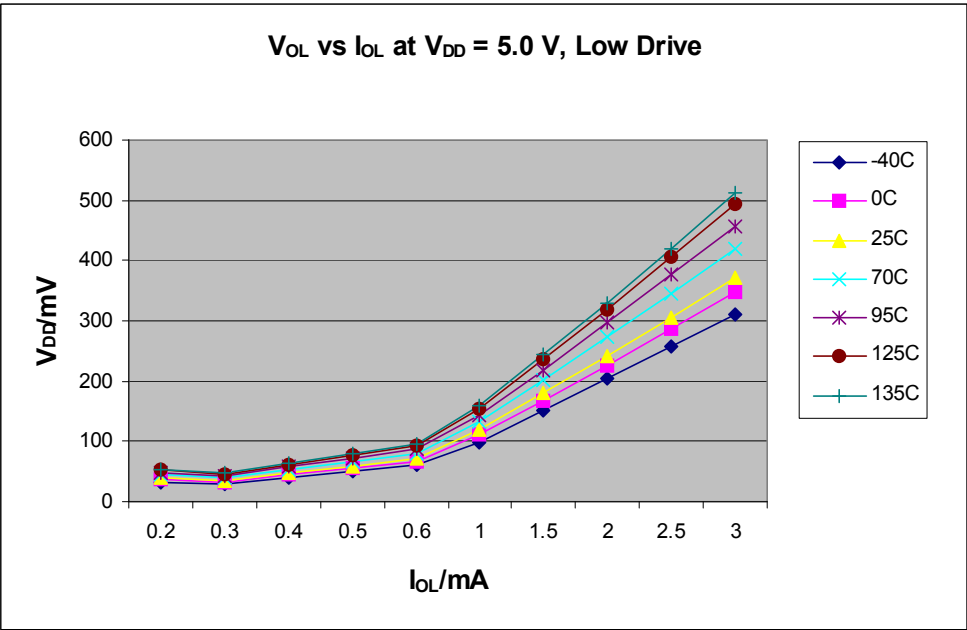


Figure 6. Typical V_{OL} vs. I_{OL} for Low Drive Enabled Pad ($V_{DD} = 5$ V)

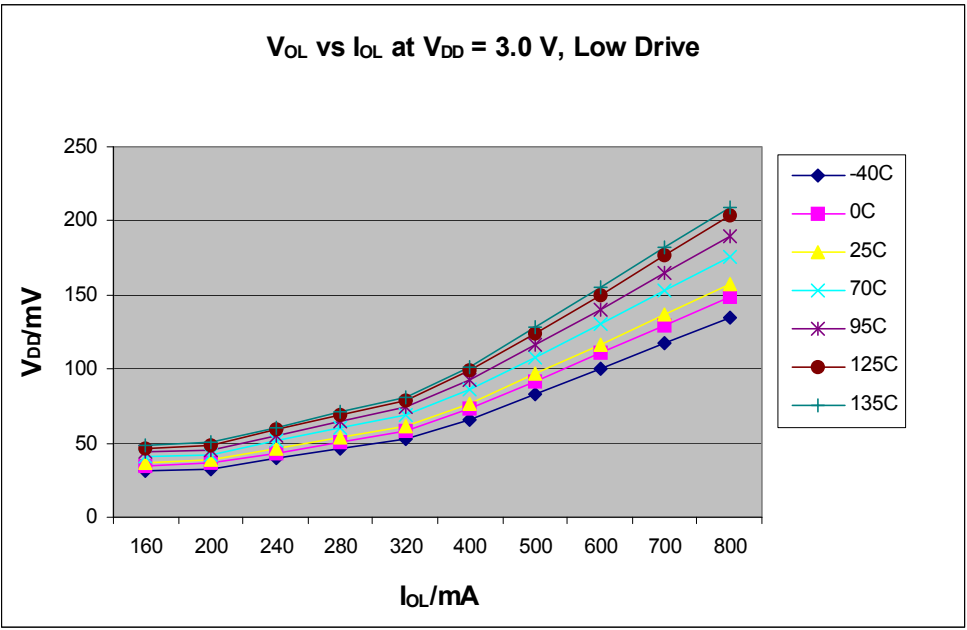


Figure 7. Typical V_{OL} vs. I_{OL} for Low Drive Enabled Pad ($V_{DD} = 3$ V)

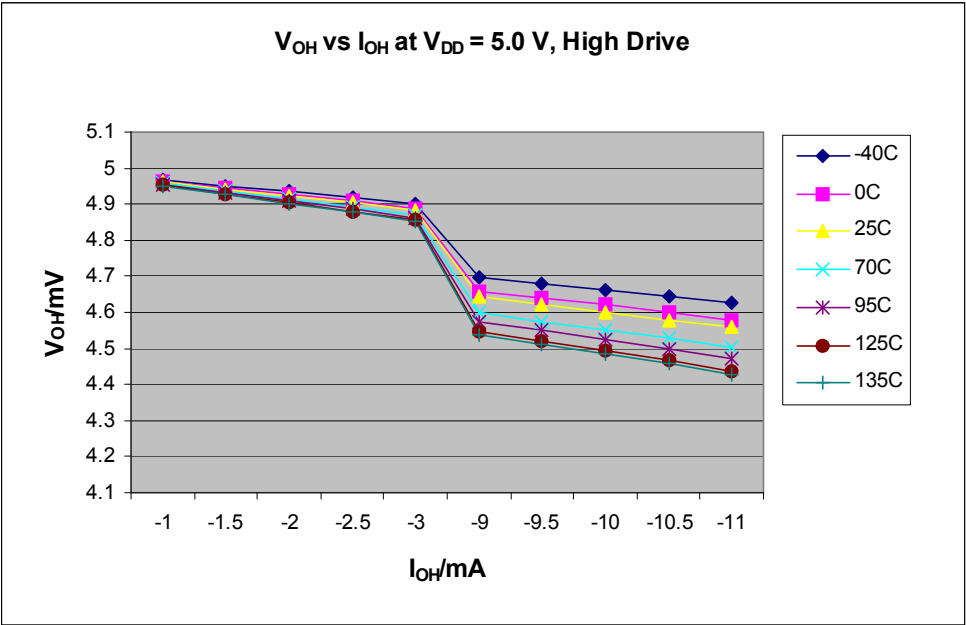


Figure 8. Typical V_{OH} vs. I_{OH} for High Drive Enabled Pad ($V_{DD} = 5$ V)

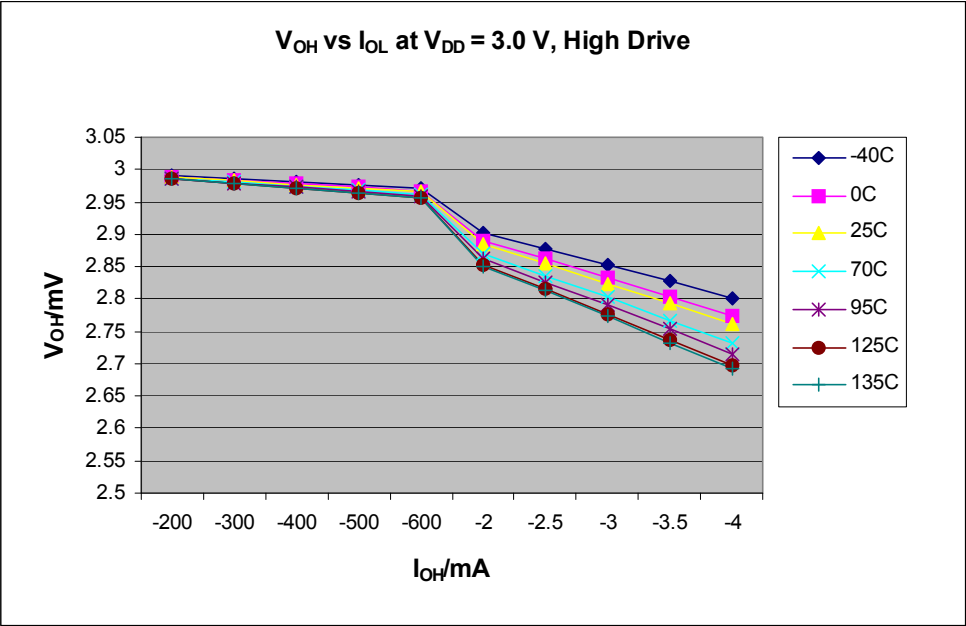


Figure 9. Typical V_{OH} vs. I_{OH} for High Drive Enabled Pad ($V_{DD} = 3$ V)

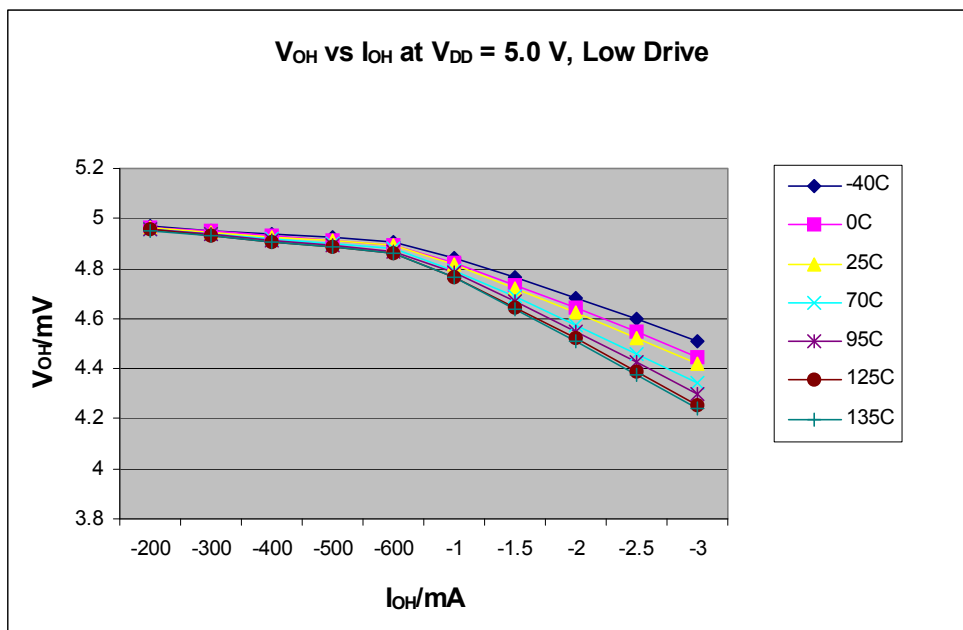


Figure 10. Typical V_{OH} vs. I_{OH} for Low Drive Enabled Pad ($V_{DD} = 5$ V)

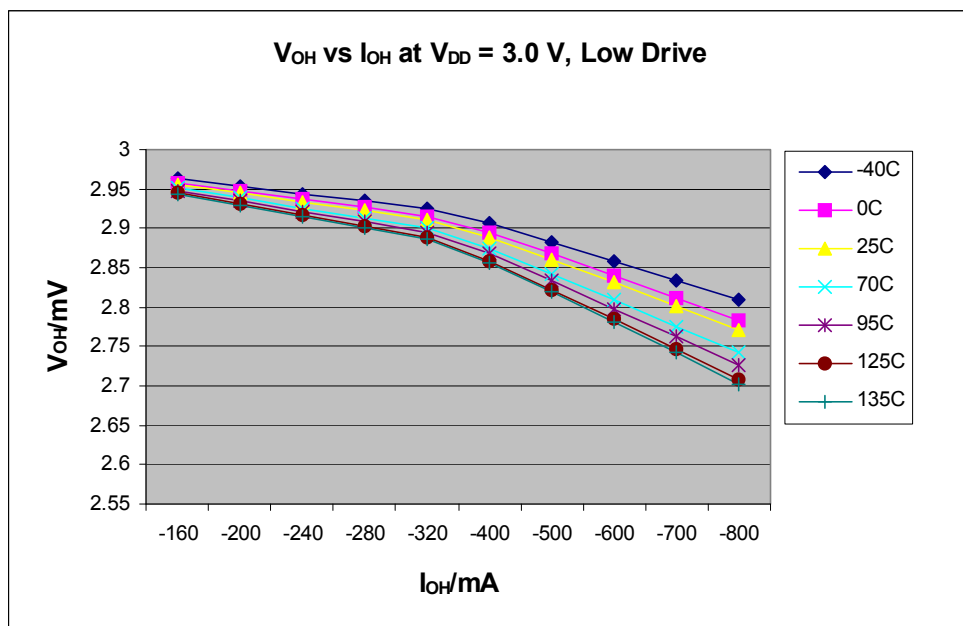


Figure 11. Typical V_{OH} vs. I_{OH} for Low Drive Enabled Pad ($V_{DD} = 3$ V)

3.6 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

| Num | C | Parameter | Symbol | V _{DD} (V) | Typical ¹ | Max | Unit | Temp (°C) |
|-----|---|--|-----------------------|------------------------|----------------------|------------------|------|---------------------------------------|
| 1 | C | Run supply current ² measured at (CPU clock = 4 MHz, f _{BUS} = 2 MHz) | R _I DD | 5 | 2.4 | 2.72 | mA | –40 to 125 |
| | | | | 3 | 2.18 | 2.26 | | |
| 2 | P | Run supply current ² measured at (CPU clock = 20 MHz, f _{BUS} = 10 MHz) | R _I DD | 5 | 6.35 | 7.29 | mA | –40 to 125 |
| | | | | 3 | 5.79 | 6.42 | | |
| 3 | P | Wait supply current ² measured at f _{BUS} = 2 MHz | W _I DD | 5 | 1.4 | 1.56 | mA | –40 to 125 |
| | | | | 3 | 1.36 | 1.53 | | |
| 4 | P | Stop2 mode supply current | S2I _{DD} | 5 | 1.4 | 19 28 45.8 | μA | –40 to 85 –40 to 105 –40 to 125 |
| | | | | 3 | 1.3 | 15 22 37.2 | μA | –40 to 85 –40 to 105 –40 to 125 |
| 5 | P | Stop3 mode supply current | S3I _{DD} | 5 | 1.61 | 23 43 76.1 | μA | –40 to 85 –40 to 105 –40 to 125 |
| | | | | 3 | 1.44 | 19 38 66.4 | μA | –40 to 85 –40 to 105 –40 to 125 |
| 6 | P | RTC adder to stop2 or stop3 ³ | S23I _{DDRTI} | 5 | 300 | 500 500 | nA | –40 to 85 –40 to 125 |
| | | | | 3 | 300 | 500 500 | nA | –40 to 85 –40 to 125 |
| 7 | C | LVD adder to stop3 (LVDE = LVDSE = 1) | S3I _{DDLVD} | 5 | 122 | 180 | μA | –40 to 125 |
| | | | | 3 | 110 | 160 | μA | –40 to 125 |
| 8 | C | Adder to stop3 for oscillator enabled ⁴ (OSCSTEN = 1) | S3I _{DDOSC} | 5,3 | 5 | 8 | μA | –40 to 125 |

¹ Typical values are based on characterization data at 25 °C unless otherwise stated. See [Figure 12](#) through [Figure 13](#) for typical curves across voltage/temperature.

² All modules except ADC active, ICS configured for FBE, and does not include any dc loads on port pins.

³ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 220 μA at 5 V with f_{BUS} = 1 MHz.

⁴ Values given under the following conditions: low range operation (RANGE = 0) with a 32.768 kHz crystal and low power mode (HGO = 0).

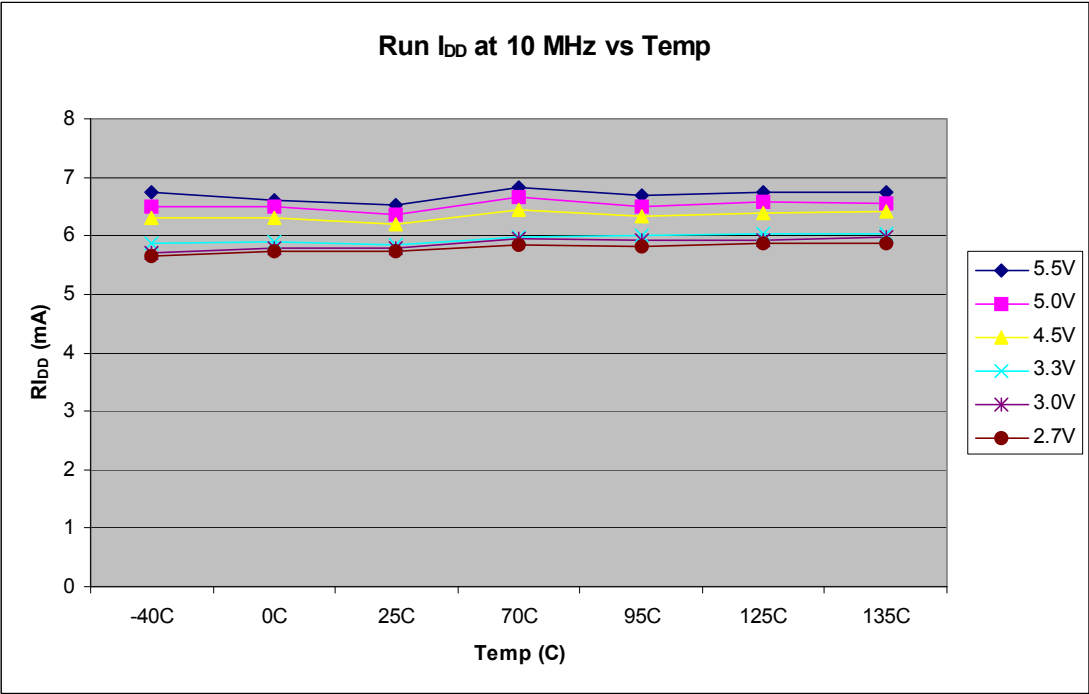


Figure 12. Typical Run I_{DD} Curves

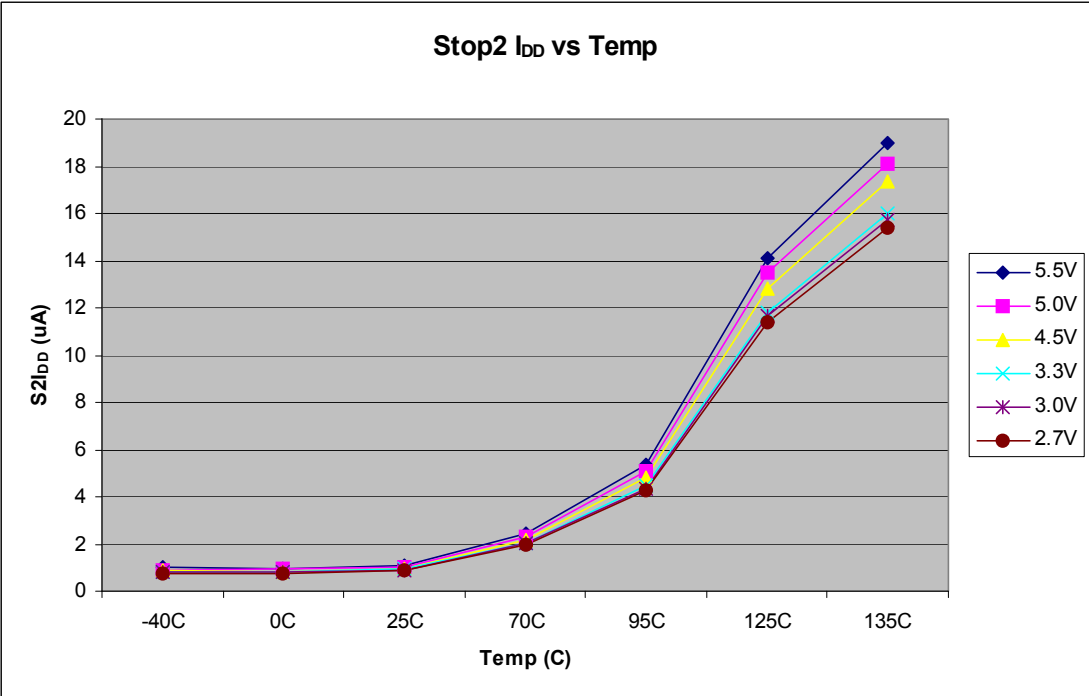


Figure 13. Typical Stop2 I_{DD} Curves

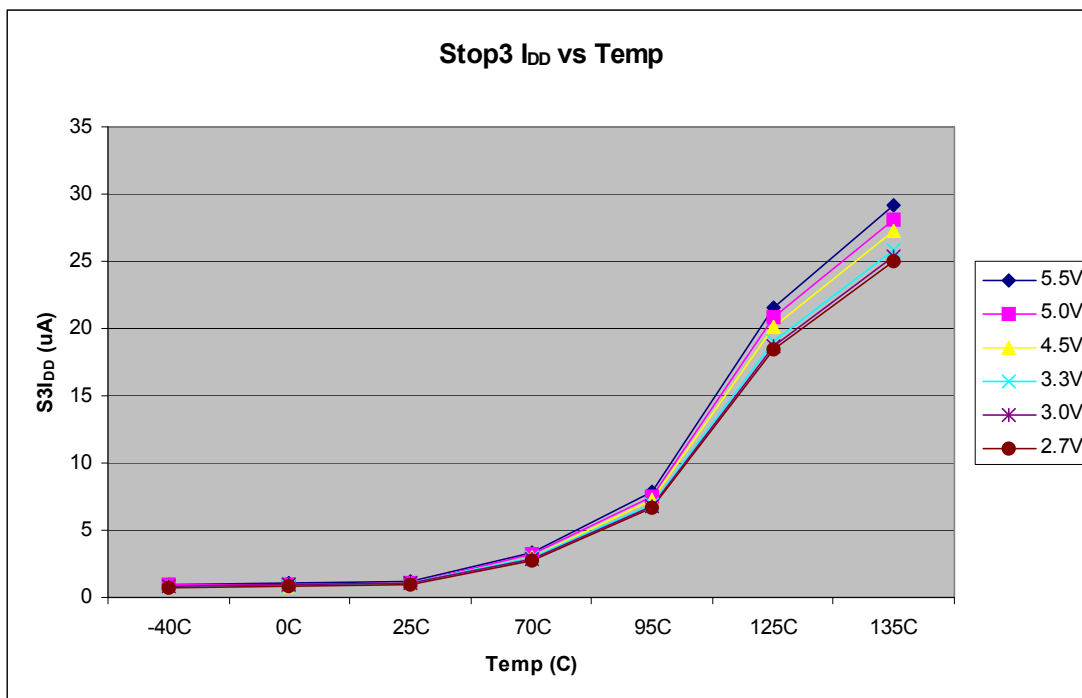


Figure 14. Typical Stop3 I_{DD} Curves

3.7 External Oscillator (XOSC) Characteristics

Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)

| Num | C | Characteristic | Symbol | Min. | Typical ¹ | Max. | Unit |
|-----|---|--|---------------------------------|--|----------------------|------|------|
| 1 | C | Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) | | | | | |
| | | Low range (RANGE = 0) | f _{lo} | 32 | — | 38.4 | kHz |
| | | High range (RANGE = 1), high gain (HGO = 1) ² | f _{hi-hgo} | 1 | — | 16 | MHz |
| | | High range (RANGE = 1), low power (HGO = 0) ² | f _{hi-lp} | 1 | — | 8 | MHz |
| 2 | — | Load capacitors | C ₁ , C ₂ | See crystal or resonator manufacturer's recommendation | | | |
| 3 | — | Feedback resistor | R _F | | | | |
| | | Low range (32 kHz to 100 kHz) | | — | 10 | — | MΩ |
| | | High range (1 MHz to 16 MHz) | | — | 1 | — | |
| 4 | — | Series resistor | R _S | | | | |
| | | Low range, low gain (RANGE = 0, HGO = 0) | | — | 0 | — | kΩ |
| | | Low range, high gain (RANGE = 0, HGO = 1) | | — | 100 | — | |
| | | High range, low gain (RANGE = 1, HGO = 0) | | — | 0 | — | |
| | | High range, high gain (RANGE = 1, HGO = 1) | | | | | |
| | | ≥ 8 MHz | | — | 0 | 0 | |
| | | 4 MHz | | — | 0 | 10 | |
| | | 1 MHz | | — | 0 | 20 | |

Table 9. Oscillator electrical specifications (Temperature Range = –40 to 125°C Ambient)

| Num | C | Characteristic | Symbol | Min. | Typical ¹ | Max. | Unit |
|-----|---|--|----------------|---------|----------------------|------|------|
| 5 | T | Crystal start-up time ³ | | | | | |
| | | Low range, low gain (RANGE = 0, HGO = 0) | $t_{CSTL-LP}$ | — | 200 | — | ms |
| | | Low range, high gain (RANGE = 0, HGO = 1) | $t_{CSTH-HGO}$ | — | 400 | — | |
| | | High range, low gain (RANGE = 1, HGO = 0) ⁴ | $t_{CSTH-LP}$ | — | 5 | — | |
| | | High range, high gain (RANGE = 1, HGO = 1) ⁴ | $t_{CSTH-HGO}$ | — | 15 | — | |
| 6 | T | Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) | | | | | |
| | | FEE or FBE mode ² | f_{extal} | 0.03125 | — | 20 | MHz |
| | | FBELP mode | | 0 | — | 20 | MHz |

- ¹ Typical column was characterized at 5.0 V, 25 °C or is recommended value.
- ² The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
- ³ This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications. This data will vary based upon the crystal manufacturer and board design. The crystal should be characterized by the crystal manufacturer.
- ⁴ 4 MHz crystal.

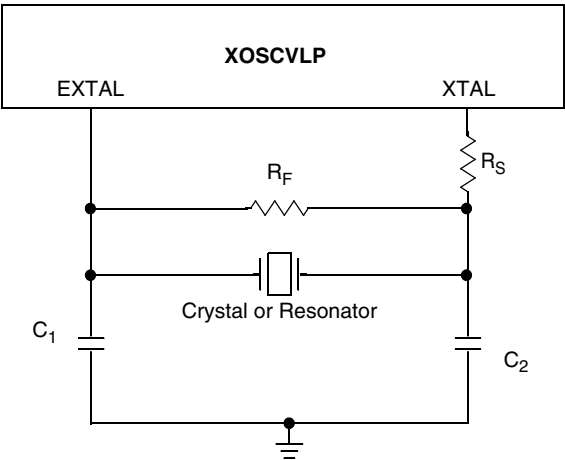


Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

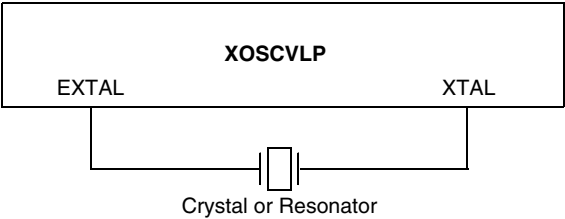


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.8 Internal Clock Source (ICS) Characteristics

Table 10. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

| Num | C | Characteristic | Symbol | Min. | Typical ¹ | Max. | Unit |
|-----|---|--|--------------------------|-------|----------------------|----------|-------------|
| 1 | P | Average internal reference frequency — factory trimmed at $V_{DD} = 5\text{ V}$ and temperature = 25 °C | f_{int_t} | — | 39.0625 | — | kHz |
| 2 | P | Internal reference frequency — user trimmed | f_{int_ut} | 31.25 | — | 39.06 | kHz |
| 3 | T | Internal reference start-up time | t_{IRST} | — | 60 | 100 | μs |
| 4 | D | DCO output frequency range — trimmed ² Low range (DRS = 00) | f_{dco_t} | 16 | — | 20 | MHz |
| 5 | D | DCO output frequency ² Reference = 32768 Hz and DMX32 = 1 | f_{dco_DMX32} | — | 59.77 | — | MHz |
| 6 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM) | $\Delta f_{dco_res_t}$ | — | ±0.1 | ±0.2 | % f_{dco} |
| 7 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM) | $\Delta f_{dco_res_t}$ | — | ±0.2 | ±0.4 | % f_{dco} |
| 8 | C | Total deviation of DCO output from trimmed frequency ³ Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C | Δf_{dco_t} | — | –1.0 to 0.5 ±0.5 | ±2 ±1 | % f_{dco} |
| 10 | C | FLL acquisition time ⁴ | $t_{Acquire}$ | — | — | 1 | ms |
| 11 | C | Long term jitter of DCO output clock (averaged over 2-ms interval) ⁵ | C_{Jitter} | — | 0.02 | 0.2 | % f_{dco} |

¹ Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

³ This parameter is characterized and not tested on each device.

⁴ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

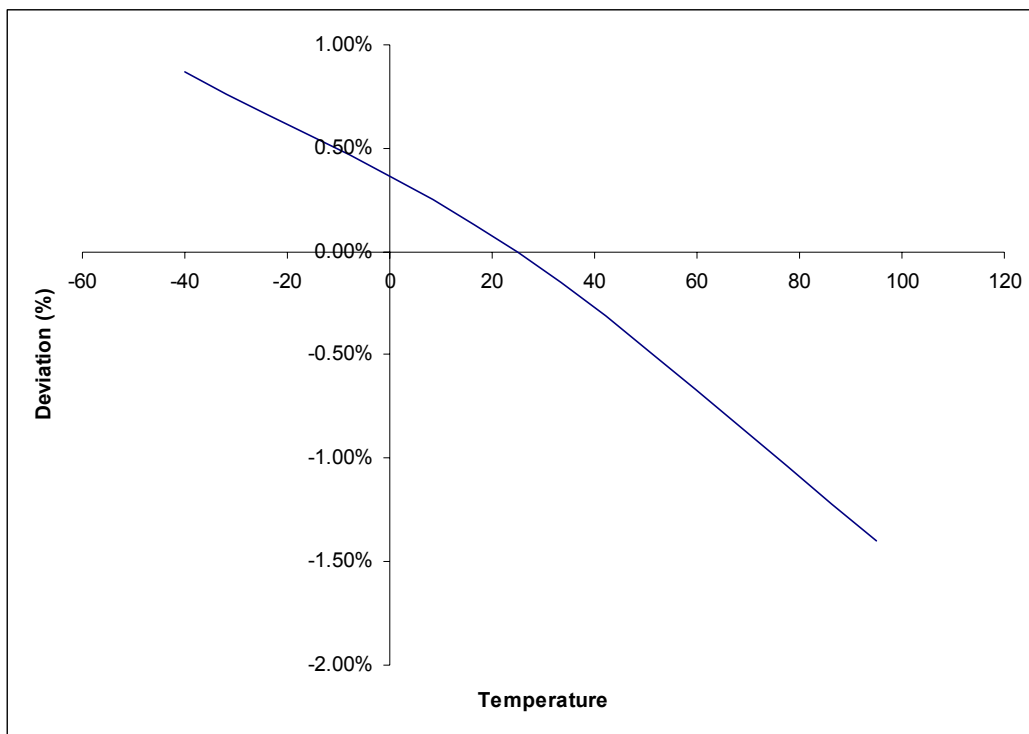


Figure 17. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.9 ADC Characteristics

Table 11. 10-Bit ADC Operating Conditions

| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|--------------------------------|---|------------------|------------|------------------|------------|------------|-----------------|
| Supply voltage | Absolute | V_{DDA} | 2.7 | — | 5.5 | V | |
| | Delta to V_{DD} ($V_{DD} - V_{DDA}$) ² | ΔV_{DDA} | -100 | 0 | 100 | mV | |
| Ground voltage | Delta to V_{SS} ($V_{SS} - V_{SSA}$) ² | ΔV_{SSA} | -100 | 0 | 100 | mV | |
| Input voltage | | V_{ADIN} | V_{REFL} | — | V_{REFH} | V | |
| Input capacitance | | C_{ADIN} | — | 4.5 | 5.5 | pF | |
| Input resistance | | R_{ADIN} | — | 3 | 5 | k Ω | |
| Analog source resistance | 10-bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$ | R_{AS} | — — | — — | 5 10 | k Ω | External to MCU |
| | 8-bit mode (all valid f_{ADCK}) | | — | — | 10 | | |
| ADC conversion clock frequency | High speed (ADLPC = 0) | f_{ADCK} | 0.4 | — | 8.0 | MHz | |
| | Low power (ADLPC = 1) | | 0.4 | — | 4.0 | | |

Electrical Characteristics

¹ Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

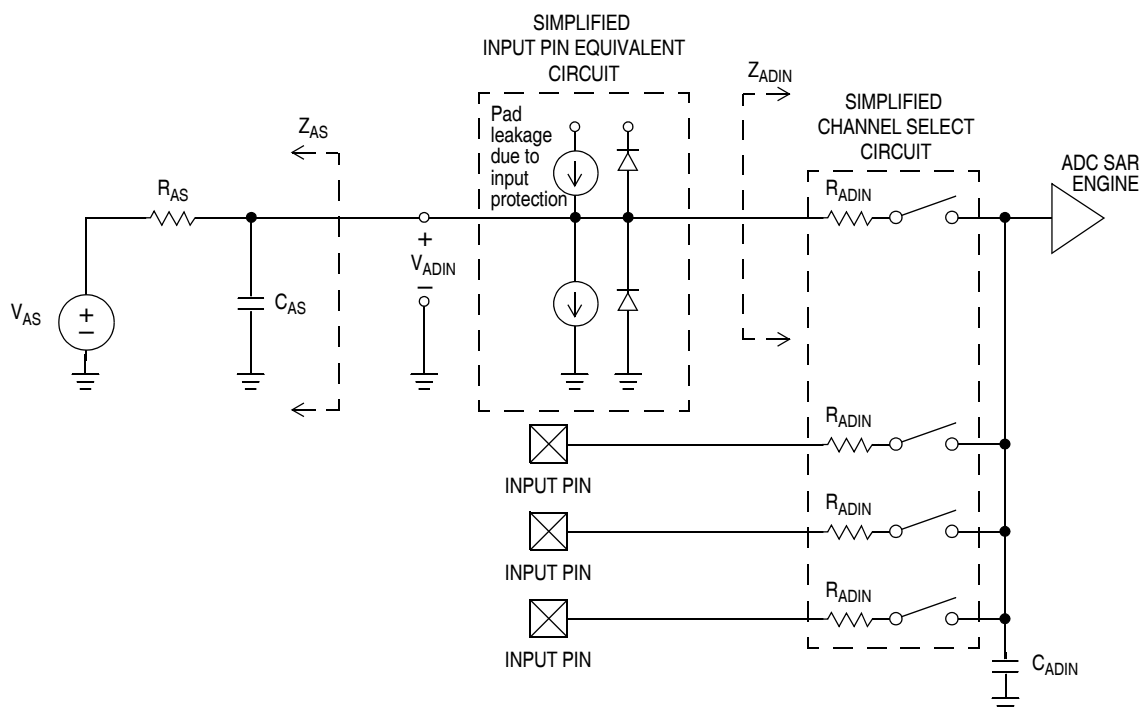


Figure 18. ADC Input Impedance Equivalency Diagram

Table 12. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit | Comment |
|---|-------------------------|---|-----------|-----|------------------|-----|---------|---------|
| Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1 | | T | I_{DDA} | — | 133 | — | μ A | |
| Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1 | | T | I_{DDA} | — | 218 | — | μ A | |
| Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1 | | T | I_{DDA} | — | 327 | — | μ A | |
| Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1 | | D | I_{DDA} | — | 0.582 | 1 | mA | |
| Supply Current | Stop, Reset, Module Off | D | I_{DDA} | — | 0.011 | 1 | μ A | |

Table 12. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit | Comment |
|--|---------------------------|---|---------------------|------|------------------|------|------------------|--|
| ADC Asynchronous Clock Source | High Speed (ADLPC = 0) | D | f _{ADACK} | 2 | 3.3 | 5 | MHz | t _{ADACK} = 1/f _{ADACK} |
| | Low Power (ADLPC = 1) | | | 1.25 | 2 | 3.3 | | |
| Conversion Time (Including sample time) | Short Sample (ADLSMP = 0) | D | t _{ADC} | — | 20 | — | ADCK cycles | See SE8 reference manual for conversion time variances |
| | Long Sample (ADLSMP = 1) | | | — | 40 | — | | |
| Sample Time | Short Sample (ADLSMP = 0) | D | t _{ADS} | — | 3.5 | — | ADCK cycles | |
| | Long Sample (ADLSMP = 1) | | | — | 23.5 | — | | |
| Temp Sensor Slope | –40°C– 25°C | D | m | — | 3.266 | — | mV/°C | |
| | 25°C– 125°C | | | — | 3.638 | — | | |
| Temp Sensor Voltage | 25°C | D | V _{TEMP25} | — | 1.396 | — | mV | |
| Characteristics for 28-pin packages only | | | | | | | | |
| Total Unadjusted Error | 10-bit mode | P | E _{TUE} | — | ±1 | ±2.5 | LSB ³ | Includes quantization |
| | 8-bit mode | P | | — | ±0.5 | ±1.0 | | |
| Differential Non-Linearity | 10-bit mode ² | P | DNL | — | ±0.5 | ±1.0 | LSB ³ | |
| | 8-bit mode ³ | P | | — | ±0.3 | ±0.5 | | |
| Integral Non-Linearity | 10-bit mode | T | INL | — | ±0.5 | ±1.0 | LSB ³ | |
| | 8-bit mode | T | | — | ±0.3 | ±0.5 | | |
| Zero-Scale Error | 10-bit mode | P | E _{ZS} | — | ±0.5 | ±1.5 | LSB ³ | V _{ADIN} = V _{SSA} |
| | 8-bit mode | P | | — | ±0.5 | ±0.5 | | |
| Full-Scale Error | 10-bit mode | T | E _{FS} | — | ±0.5 | ±1 | LSB ³ | V _{ADIN} = V _{DDA} |
| | 8-bit mode | T | | — | ±0.5 | ±0.5 | | |
| Quantization Error | 10-bit mode | D | E _Q | — | — | ±0.5 | LSB ³ | |
| | 8-bit mode | | | — | — | ±0.5 | | |
| Input Leakage Error | 10-bit mode | D | E _{IL} | — | ±0.2 | ±2.5 | LSB ³ | Pad leakage ^{4*} R _{AS} |
| | 8-bit mode | | | — | ±0.1 | ±1 | | |
| Characteristics for 16-pin package only | | | | | | | | |
| Total Unadjusted Error | 10-bit mode | P | E _{TUE} | — | ±1.5 | ±3.5 | LSB ³ | Includes quantization |
| | 8-bit mode | P | | — | ±0.7 | ±1.5 | | |

Electrical Characteristics

Table 12. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit | Comment |
|----------------------------|--------------------------|---|----------|-----|------------------|------|------------------|---------------------------------------|
| Differential Non-Linearity | 10-bit mode ³ | P | DNL | — | ±0.5 | ±1.0 | LSB ³ | |
| | 8-bit mode ³ | P | | — | ±0.3 | ±0.5 | | |
| Integral Non-Linearity | 10-bit mode | T | INL | — | ±0.5 | ±1.0 | LSB ³ | |
| | 8-bit mode | T | | — | ±0.3 | ±0.5 | | |
| Zero-Scale Error | 10-bit mode | P | E_{ZS} | — | ±1.5 | ±2.1 | LSB ³ | $V_{ADIN} = V_{SSA}$ |
| | 8-bit mode | P | | — | ±0.5 | ±0.7 | | |
| Full-Scale Error | 10-bit mode | T | E_{FS} | — | ±1 | ±1.5 | LSB ³ | $V_{ADIN} = V_{DDA}$ |
| | 8-bit mode | T | | — | ±0.5 | ±0.5 | | |
| Quantization Error | 10-bit mode | D | E_Q | — | — | ±0.5 | LSB ³ | |
| | 8-bit mode | | | — | — | ±0.5 | | |
| Input Leakage Error | 10-bit mode | D | E_{IL} | — | ±0.2 | ±2.5 | LSB ³ | Pad leakage ^{4*} R_{AS} |
| | 8-bit mode | | | — | ±0.1 | ±1 | | |

¹ Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes

³ $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$

⁴ Based on input pad leakage current. Refer to pad electricals.

3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

| Num | C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|----------------------|-----------------------------|----------------------|------|---------|
| 1 | D | Bus frequency ($t_{cyc} = 1/f_{Bus}$) | f_{Bus} | DC | — | 10 | MHz |
| 2 | D | Internal low power oscillator period | t_{LPO} | 700 | — | 1300 | μs |
| 3 | D | External reset pulse width ² | t_{extrst} | 100 | — | — | ns |
| 4 | D | Reset low drive ³ | t_{rstdrv} | $34 \times t_{cyc}$ | — | — | ns |
| 5 | D | BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes | t_{MSSU} | 500 | — | — | ns |
| 6 | D | BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ⁴ | t_{MSH} | 100 | — | — | μs |
| 7 | D | IRQ pulse width Asynchronous path ² Synchronous path ⁵ | t_{LIH}, t_{IHL} | 100 $1.5 \times t_{cyc}$ | — | — | ns |
| 8 | D | Pin interrupt pulse width Asynchronous path ² Synchronous path ⁵ | t_{LIH}, t_{IHL} | 100 $1.5 \times t_{cyc}$ | — | — | ns |
| 9 | C | Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) ⁶ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | t_{Rise}, t_{Fall} | — | 40 75 | — | ns |
| | | Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | t_{Rise}, t_{Fall} | — | 11 35 | — | ns |

¹ Typical values are based on characterization data at $V_{DD} = 5.0$ V, 25 °C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ When any reset is initiated, internal circuitry drives the reset pin (if enabled, RSTPE = 1) low for about 34 cycles of t_{cyc} .

⁴ To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

⁵ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁶ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 125 °C.

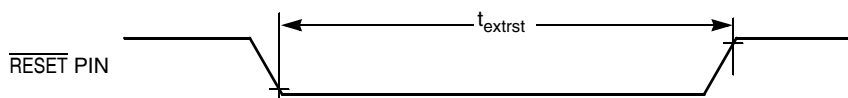


Figure 19. Reset Timing

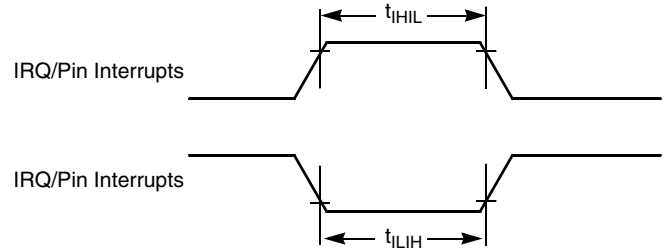


Figure 20. IRQ/Pin Interrupt Timing

3.10.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

| Num | C | Rating | Symbol | Min | Max | Unit |
|-----|---|---------------------------|--------------|-----|-------------|-----------|
| 1 | D | External clock frequency | f_{TPMext} | DC | $f_{Bus}/4$ | MHz |
| 2 | D | External clock period | t_{TPMext} | 4 | — | t_{cyc} |
| 3 | D | External clock high time | t_{clkh} | 1.5 | — | t_{cyc} |
| 4 | D | External clock low time | t_{clkl} | 1.5 | — | t_{cyc} |
| 5 | D | Input capture pulse width | t_{ICPW} | 1.5 | — | t_{cyc} |

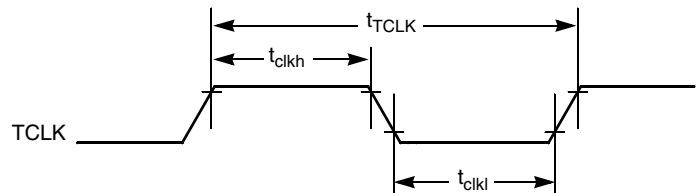


Figure 21. Timer External Clock

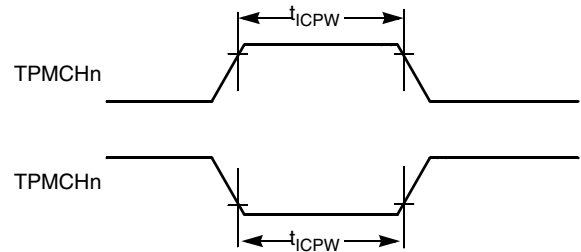


Figure 22. Timer Input Capture Pulse

3.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section in the reference manual.

Table 15. Flash Characteristics

| Num | C | Characteristic | Symbol | Min | Typical | Max | Unit |
|-----|---|---|-------------------------|--------|--------------|------|-------------------|
| 1 | D | Supply voltage for program/erase | $V_{\text{prog/erase}}$ | 2.7 | — | 5.5 | V |
| 2 | D | Supply voltage for read operation | V_{Read} | 2.7 | — | 5.5 | V |
| 3 | D | Internal FCLK frequency ¹ | f_{FCLK} | 150 | — | 200 | kHz |
| 4 | D | Internal FCLK period (1/FCLK) | t_{Fcyc} | 5 | — | 6.67 | μs |
| 5 | P | Byte program time (random location) ² | t_{prog} | 9 | | | t_{Fcyc} |
| 6 | P | Byte program time (burst mode) ² | t_{Burst} | 4 | | | t_{Fcyc} |
| 7 | P | Page erase time ² | t_{Page} | 4000 | | | t_{Fcyc} |
| 8 | P | Mass erase time ² | t_{Mass} | 20,000 | | | t_{Fcyc} |
| 9 | C | Program/erase endurance ³ T_L to T_H = $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ $T = 25\text{ }^{\circ}\text{C}$ | n_{FLPE} | 10,000 | — 100,000 | — | cycles |
| 10 | C | Data retention ⁴ | $t_{\text{D_ret}}$ | 15 | 100 | — | years |

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

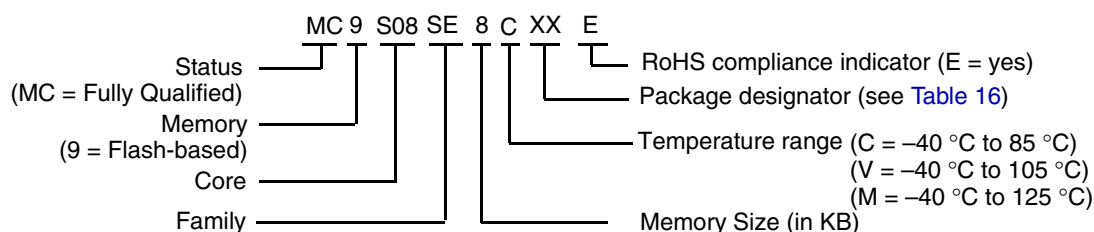
³ **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

⁴ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to $25\text{ }^{\circ}\text{C}$ using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.

4 Ordering Information

This chapter contains ordering information for the device numbering system.

Example of the device numbering system:



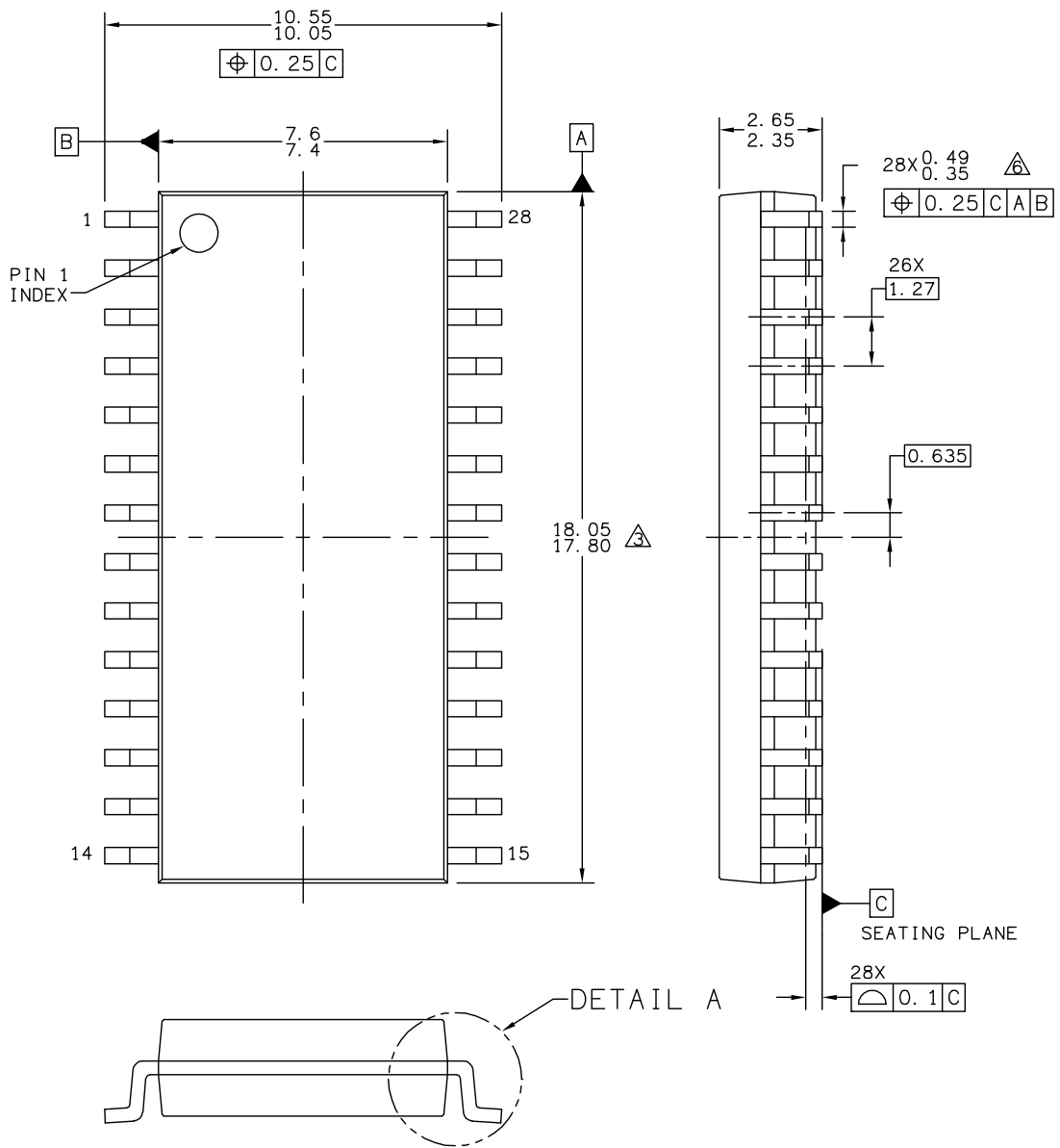
4.1 Package Information

Table 16. Package Descriptions

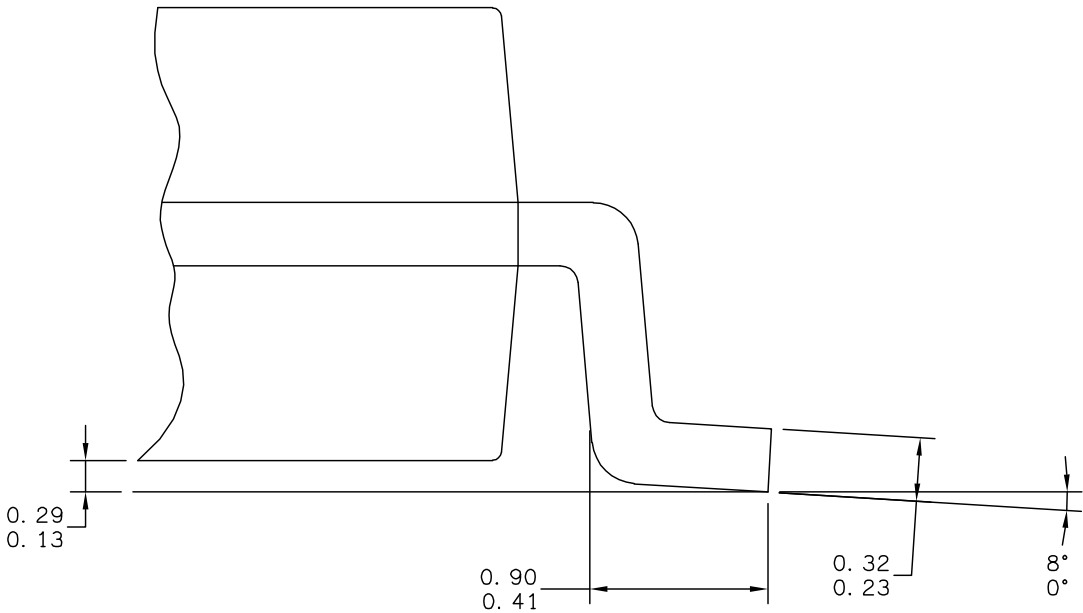
| Pin Count | Package Type | Abbreviation | Designator | Case No. | Document No. |
|-----------|-----------------------------------|--------------|------------|----------|--------------|
| 28 | Plastic Dual In-line Pin | PDIP | RL | 710 | 98ASB42390B |
| 28 | Small Outline Integrated Circuit | SOIC | WL | 751F | 98ASB42345B |
| 16 | Thin Shrink Small Outline Package | TSSOP | TG | 948F | 98ASH70247A |

4.2 Mechanical Drawings

The following pages are mechanical drawings for the packages described in [Table 16](#).



| | | | | |
|---|---|--|----------------------------|-------------|
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| | TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE | | DOCUMENT NO: 98ASB42345B | REV: G |
| | | | CASE NUMBER: 751F-05 | 10 MAR 2005 |
| | | | STANDARD: MS-013AE | |

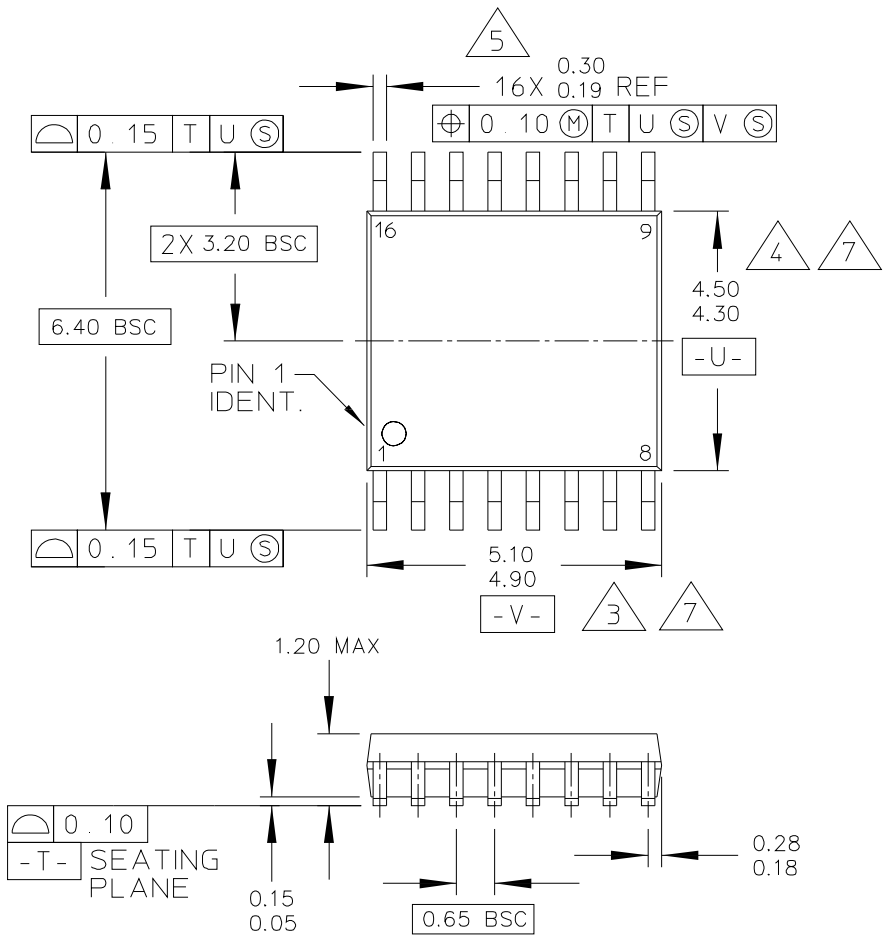


| | | | | | |
|---|--|--------------------------|--|----------------------------|--|
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| TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE | | DOCUMENT NO: 98ASB42345B | | REV: G | |
| | | CASE NUMBER: 751F-05 | | 10 MAR 2005 | |
| | | STANDARD: MS-013AE | | | |

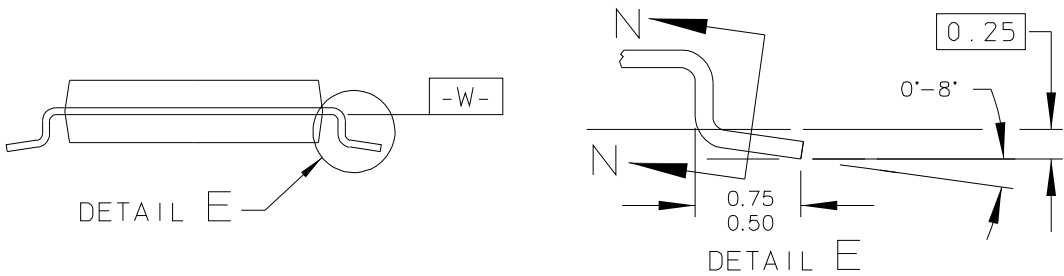
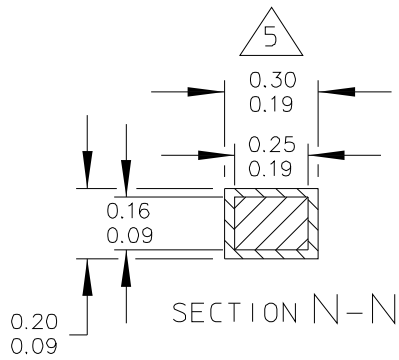
NOTES:

1. POSITIONAL TOLERANCE OF LEADS, SHALL BE WITHIN 0.25 MM (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STD 710-02.
5. CONTROLLING DIMENSION: INCH

| INCH | | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|---|-----------|-------|------------|--------------------|--------------------------|------|----------------------------|-------------|-----|
| DIM | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | 1.435 | 1.465 | 36.45 | 37.21 | | | | | |
| B | 0.540 | 0.560 | 13.72 | 14.22 | | | | | |
| C | 0.155 | 0.200 | 3.94 | 5.08 | | | | | |
| D | 0.014 | 0.022 | 0.36 | 0.56 | | | | | |
| F | 0.040 | 0.060 | 1.02 | 1.52 | | | | | |
| G | 0.100 BSC | | 2.54 BSC | | | | | | |
| H | 0.065 | 0.085 | 1.65 | 2.16 | | | | | |
| J | 0.008 | 0.015 | 0.20 | 0.38 | | | | | |
| K | 0.115 | 0.135 | 2.92 | 3.43 | | | | | |
| L | 0.600 BSC | | 15.24 BSC | | | | | | |
| M | 0° | 15° | 0° | 15° | | | | | |
| N | 0.020 | 0.040 | 0.51 | 1.02 | | | | | |
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| TITLE: 28 LD PDIP | | | | | DOCUMENT NO: 98ASB42390B | | | REV: D | |
| | | | | | CASE NUMBER: 710-02 | | | 24 MAY 2005 | |
| | | | | | STANDARD: NON-JEDEC | | | | |



| | | | |
|---|--|--------------------------|----------------------------|
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| TITLE: 16 LD TSSOP, PITCH 0.65MM | | DOCUMENT NO: 98ASH70247A | REV: B |
| | | CASE NUMBER: 948F-01 | 19 MAY 2005 |
| | | STANDARD: JEDEC | |



| | | | | | |
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| | | CASE NUMBER: 948F-01 | | 19 MAY 2005 | |
| | | STANDARD: JEDEC | | | |

Ordering Information

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

| | | | |
|---|--------------------------|--------------------|----------------------------|
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| TITLE: 16 LD TSSOP, PITCH 0.65MM | DOCUMENT NO: 98ASH70247A | | REV: B |
| | CASE NUMBER: 948F-01 | | 19 MAY 2005 |
| | STANDARD: JEDEC | | |

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