
HF Transmission

Introduction

This document deals with HF Transmission issues in high-speed and broadband applications using Atmel ADCs and DACs. It stresses the hardware choices to be made to reach an optimum tradeoff between high-speed, broadband performances and system cost.

From the package to the printed circuit board, critical HF transmission issues are explored and addressed with respect to performance (noise immunity and speed) and cost.



HF Transmission

Application Note

Rev. 5352A-BDC-10/03





HF Transmission Performance and Cost Tradeoff

Nowadays, high-speed systems have to deal with two critical and often contradictory parameters: the system performance and its cost.

This document first focuses on the several methods and recommended schemes to ensure the high-frequency (HF) performance of a system and in particular a system using Atmel ADCs or DACs, whereas the second part of the document addresses the cost issue.

In high frequency, we refer to speeds above 1 GHz.

In performance, we refer to the speed and the immunity to noise in nominal conditions but also in varying environments (sensitivity to temperature for example).

HF Performances at Device Level

Atmel broadband data converters are characterized as high-speed and broadband converters, where “high-speed” gives an idea of the conversion rate performed by the converter and “broadband” underlines the converters’ capability to deal with broad signals (over 100 MHz bandwidth). Both these important characteristics make Atmel converters’ design-ins very critical in terms of high frequency transmission since all noise, signal attenuation, and impedance matching issues have to be carefully addressed.

The HF issues have to be taken into account in the very early stages of the development of a converter and then all through its implementation stage into a system. A device with good HF performances loses all its benefits if assembled into a package with poor HF performances.

Technology

The technology used is the first parameter a designer has in hand to define the HF performances of its future device.

The Ft parameter is very critical and dimensions the future capabilities of a device.

All Atmel converters are designed using very high-speed processes with cutoff frequencies well above 25 GHz and even reaching 75 GHz. This ensures that Atmel converters can feature bandwidths well beyond 1 GHz.

Architecture

The converter’s architecture is also critical and the architecture’s limiting stage defines the maximum analog bandwidth attainable.

In Atmel converters, the converters’ first stages are the limiting ones. Thanks to the process and architecture used as well as the designers’ know-how, Atmel is the first company worldwide to have introduced converters with full power input bandwidth of more than 3.5 GHz, achieving a band flatness of ± 0.5 dB over more than 1.8 GHz.

Impedance Matching

In addition to the process’ intrinsic capabilities and the converters’ architecture, some special care is systematically taken with the impedance matching issue.

In particular, most Atmel converters have a 50 Ω matched impedance for the clock, analog inputs and outputs.

The die itself is wire-bonded to its package with 50 Ω impedance wires.

The converter’s Voltage Standing Wave Ratio (VSWR) is usually simulated, measured and optimized to 1.1 for all Atmel converters on a given band of interest.

For devices such as the TS8388BGL (8-bit 1 Gsps ADC in a CBGA 68 package) and the TS83102G0BGL (10-bit 2 Gsps ADC in a CBGA 152 package), the 50 Ω termination on

the clock and analog signals is either on-package or inside the package cavity, thus optimizing the overall system dimensions.

Package Parasitics

The package plays an important role in the HF transmission issues for high-speed broadband devices, in addition to thermal and mechanical aspects.

The package has to ensure that the HF performances of the die are not too affected by the parasitics engendered by the package itself.

The same die in two different packages can show different performances, optimizing the package's thermal, mechanical or HF characteristics.

The case of the 8-bit 1 Gbps ADC is a good illustration of this. This device is available in two different packages: either CBGA 68 or CQFP 68. The first one has proven to have better HF performances than the second, which has nevertheless better thermal performances. In the case of the CQFP 68 package, the device's full power input bandwidth is limited by the package itself whereas it is not the case for the CBGA 68 package.

As a whole, BGA (Ball Grid Array) packages show overall better HF performances than QFP (Quad Flat Pack) packages, or leaded packages in general, because of the low inductance of the balls compared to the inductance of the leads.

The HF issues then become a critical point in the design of QFP packages, when thermal performances are the main issue for BGA packages.

HF Performances at Board Level

After optimization of the die in its package, the way the device is implemented on a board has to be considered so as to keep all the benefits of the previous optimizations on the die and on the package.

The board material is one parameter which should not be neglected. The board layout is also an important factor in the HF transmission issues. Finally, the noise isolation on board eventually consolidates the board design and device integration.

Board Characteristics

The key parameters in the selection of a printed circuit board substrate for HF applications are the following:

- Dielectric constant (ϵ_r)
- Loss tangent ($\tan \delta$)
- Temperature variation of dielectric constant ($C_t\epsilon_r$)
- Coefficient of thermal expansion (CTE or TEC Thermal Expansion Coefficient)

To these parameters can be added the cost of the printed circuit board, which can be a limiting factor in certain applications.

Most well-known manufacturers of high-speed low loss laminates are given in the following table with some typical characteristics.

Table 1. Examples of Laminate Performance

Supplier	Material	ϵ_r	Tan δ at 1 GHz	Ct ϵ_r (ppm/°C)	CTE(X,Y) (ppm/°C)
Rogers	RO4003 (woven glass/ceramic PTFE)	3.38	0.0022	50	11 - 14
	RO3003 (ceramic filled PTFE)	3.00	0.0013	13	17
	ULTRALAM (woven glass PTFE)	2.40	0.0019	-100	15
Arlon	AR320 (woven glass PTFE)	3.20	0.0030	-100	9 - 12
Taconic Plastics	TLC-32	3.20	0.0030	-37.5	9 - 12
	TLE (woven glass PTFE)	2.95	0.0028	-37.5	9 - 12
	TLY-3 (woven glass PTFE)	2.20	0.0012	-100	20 - 35
	TLX (woven glass PTFE)	2.50	0.0019	-70	9 - 12
Park Nelco	N4000-6-FC BC (FR4 HTG)	4.1	0.015		16
Polyclad	PCL 370 (FR4-HTG)	4.3	0.0015	51	17
Isola	FR4 117 (FR4 HTG)	4.4	0.013		17
Other	FR4	4.6	0.030	17	

It is generally taken for granted that a very low insertion loss material should have the following characteristics (or should at least be as close as possible to these characteristics):

- Loss tangent ranging from 0.0012 to 0.0022
- Dielectric constant ranging from 2.1 to 2.5
- Coefficient of thermal expansion close to the one of the material used for signal traces (in general, the laminates are copper-cladded and should thus match the copper CTE of 17 ppm/°C)

For its converter evaluation boards, Atmel made the choice of RO4003 woven glass PTFE material for its low insertion loss performance and cost-effectiveness as well as FR4-HTG (BT/Epoxy) dielectric substrate for its enhanced mechanical characteristics for high temperature operations.

Please note that for high frequency applications, the standard FR4 material is not suitable (because of very poor performances). Instead, we recommend the use of enhanced/composite FR4 materials (for example FR4-HTG).

This choice was made because of these materials' characteristics:

- RO4003
 - 0.044dB/inch insertion loss at 2.5 GHz
 - 0.318dB/inch insertion loss at 18 GHz
 - Dielectric constant = 3.4 at 10 GHz
- FR4-HTG (BT/Epoxy)
 - Dielectric constant = 4.5 at 1 MHz
 - Operating temperature = 170°C (125°C for FR4 material)
 - Withstands thermal shocks very well (from -65°C up to 170°C)

The RO4003 material is used for the external layers, while the FR4-HTG is used for internal planes.

Board Layout

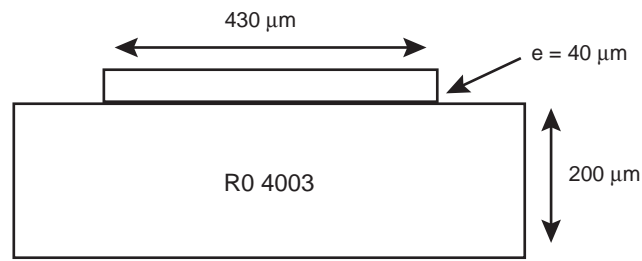
The material used for the printed circuit board is very important for signal transmission in the high frequency domain and in extended temperature ranges. Another key parameter is the layout itself.

There are common rules for the layout of HF systems, such as the following:

- Avoid traces with angles or too many patterns (to avoid crosstalks between traces)
- Keep all traces matched to $50\ \Omega$
- Have the same length for traces corresponding to signals of the same function (clock, analog in, analog out, data in, data out)
- Avoid through-hole vias for signal traces
- For differential signals, keep the True and False signal traces close to one another
- For single-ended signals, make sure all signals are far enough from their neighbor to avoid crosstalks

The following shows the recommended board layout, as used for Atmel converter evaluation boards.

Figure 1. $50\ \Omega$ Matched Line on R04003 Layout



The characteristics of the boards used for Atmel converter evaluation boards are:

- Top and bottom layer material is RO4003
- Internal layer is FR4-HTG
- $40\ \mu\text{m}$ traces on RO4003 dielectric ($\epsilon_r = 3.38$, $200\ \mu\text{m}$ width)
- Copper traces on top and bottom layers plus NiAu finish (total = $40\ \mu\text{m}$)
- Internal layer width is $35\ \mu\text{m}$
- Total width of the printed circuit board is $1.6\ \text{mm}$

Decoupling, Bypassing and Grounding Schemes

Noise coming from the analog parts of the system have to be properly isolated so that it does not contaminate the “clean” parts of the system. One recommended operation is to always make sure the noisy sources are switched on before the clean sources. By abiding by this rule, we can make sure that the noisy sources, after reaching their steady state, do not perturb the clean sources.

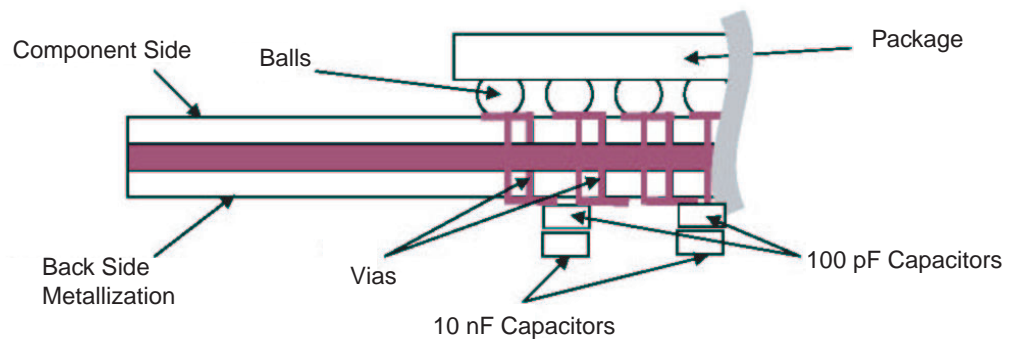
Proper decoupling, grounding and bypassing schemes also have to be applied to ensure good immunity to system noise.

Some simple rules can be used, such as:

- Decoupling
Decoupling capacitors should be placed as close as possible to the PCB connectors. Their value has to be chosen with respect to the frequency of operation of the system.

- Grounding**
 All Atmel ADCs have separated analog and digital grounds at the die level. These ground planes are brought together at the package level. Consequently, analog and digital grounds must be merged at the board level. This is not true for Atmel DACs (refer to the device specifications).
- Bypassing**
 The bypassing capacitors should be placed as close as possible to the device power accesses. Their value has to be chosen with respect to the frequency of operation of the system. Atmel usually recommends stacking the bypassing capacitors at the back side of the board for room saving and optimization of the bypassing. In this case, the capacitor of lowest value should be soldered first. An example is given in the following figure.

Figure 2. Bypassing Capacitors Mounting Scheme



Cost Issues

A tradeoff has to be defined between the performances of the PCB and its cost. Atmel's choice in terms of PCB for its data converter evaluation board was to adopt PCBs with RO4003 dielectric instead of FR4 dielectric material, for its enhanced performances over temperature and in the high frequency domain.

The following table presents several laminates sorted by cost/sq ft (this is a rough order of magnitude). The unity considered is the price of the FR4 material (it has the lowest cost/sq ft among the listed materials).

Example: the RO4003 material is approximately five times as expensive as FR4.

Table 2. Laminates Cost/Sq Ft Ranking (Highest Cost = Rank 1)

Cost (per FR4 Cost/Sq Ft Unit)	Material	ϵ_r	Tan δ at 1 GHz	Ct ϵ_r (ppm/°C)	CTE(X,Y) (ppm/°C)
9	RO3003	3.00	0.0013	13	17
7	TLY-3	2.20	0.0012	-100	20 - 35
6	ULTRALAM	2.40	0.0019	-100	15
6	TLX	2.50	0.0019	-70	9 - 12
5	RO4003	3.38	0.0022	50	11 - 14
3.5	TLE	2.95	0.0028	-37.5	9 - 12
3.5	AR320	3.20	0.0030	-100	9 - 12
2.5	TLC-32	3.20	0.0030	-37.5	9 - 12
1	FR4	4.6	0.030		17

As underlined in Table 2, the RO4003 material provides a good compromise between high-frequency and high-temperature characteristics and cost.

Conclusion

In this document, HF performances at both device and system levels are discussed. The stress is particularly put on the parameters to be taken into account to reach a tradeoff between performances and cost when choosing board materials. Several laminates are presented and compared so that you can have a global view of what is available on the market today.



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5352A-BDC-10/03