MICRON TECHNOLOGY, INC.

4, 8 MEG x 72 BUFFERED DRAM DIMMs

DRAM MODULE

MT6LDT472 (X)
MT12LDT872 (X)

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 32MB (4 Meg x 72) and 64MB (8 Meg x 72)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- All inputs are buffered except RAS#
- 4,096 cycles (12 row, 10 column addresses)
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles

OPTIONS — MARKING

- Package
  168-pin DIMM (gold) — G
- Timing
  50ns access — -5*
  60ns access — -6
- Access Cycles
  FAST PAGE MODE — None
  EDO PAGE MODE — X

* EDO version only

KEY TIMING PARAMETERS

EDO Operating Mode

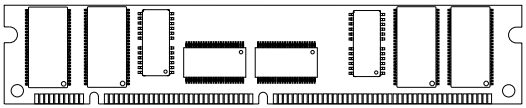
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-5	84ns	50ns	20ns	30ns	18ns	8ns
-6	104ns	60ns	25ns	35ns	20ns	10ns

FPM Operating Mode

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	35ns	20ns	40ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	OE2#	86	DQ36	128	RFU
3	DQ1	45	RAS2#	87	DQ37	129	RAS3#
4	DQ2	46	CAS4#	88	DQ38	130	CAS5#
5	DQ3	47	RFU	89	DQ39	131	RFU
6	V_{DD}	48	WE2#	90	V_{DD}	132	PDE#
7	DQ4	49	V_{DD}	91	DQ40	133	V_{DD}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V_{DD}	101	DQ49	143	V_{DD}
18	V_{DD}	60	DQ24	102	V_{DD}	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	V_{SS}	65	DQ25	107	V_{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	WE0#	69	DQ28	111	RFU	153	DQ64
28	CAS0#	70	DQ29	112	CAS1#	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	RAS0#	72	DQ31	114	RAS1#	156	DQ67
31	OE0#	73	V_{DD}	115	RFU	157	V_{DD}
32	V_{SS}	74	DQ32	116	V_{SS}	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC (A12)	81	PD5	123	NC (A13)	165	PD6
40	V_{DD}	82	PD7	124	V_{DD}	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	V_{DD}	126	B0	168	V_{DD}

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT6LDT472G-5 X	4 Meg x 72 ECC	50ns
MT6LDT472G-6 X	4 Meg x 72 ECC	60ns
MT12LDT872G-5 X	8 Meg x 72 ECC	50ns
MT12LDT872G-6 X	8 Meg x 72 ECC	60ns

FPM Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT6LDT472G-6	4 Meg x 72 ECC	60ns
MT12LDT872G-6	8 Meg x 72 ECC	60ns

GENERAL DESCRIPTION

The MT6LDT472 (X) and MT12LDT872 (X) are randomly accessed 32MB and 64MB memories organized in a x72 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the address bits. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for four-byte applications which interleave between two four-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71. RAS# is used to latch the first 12 bits and CAS# the latter 10 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

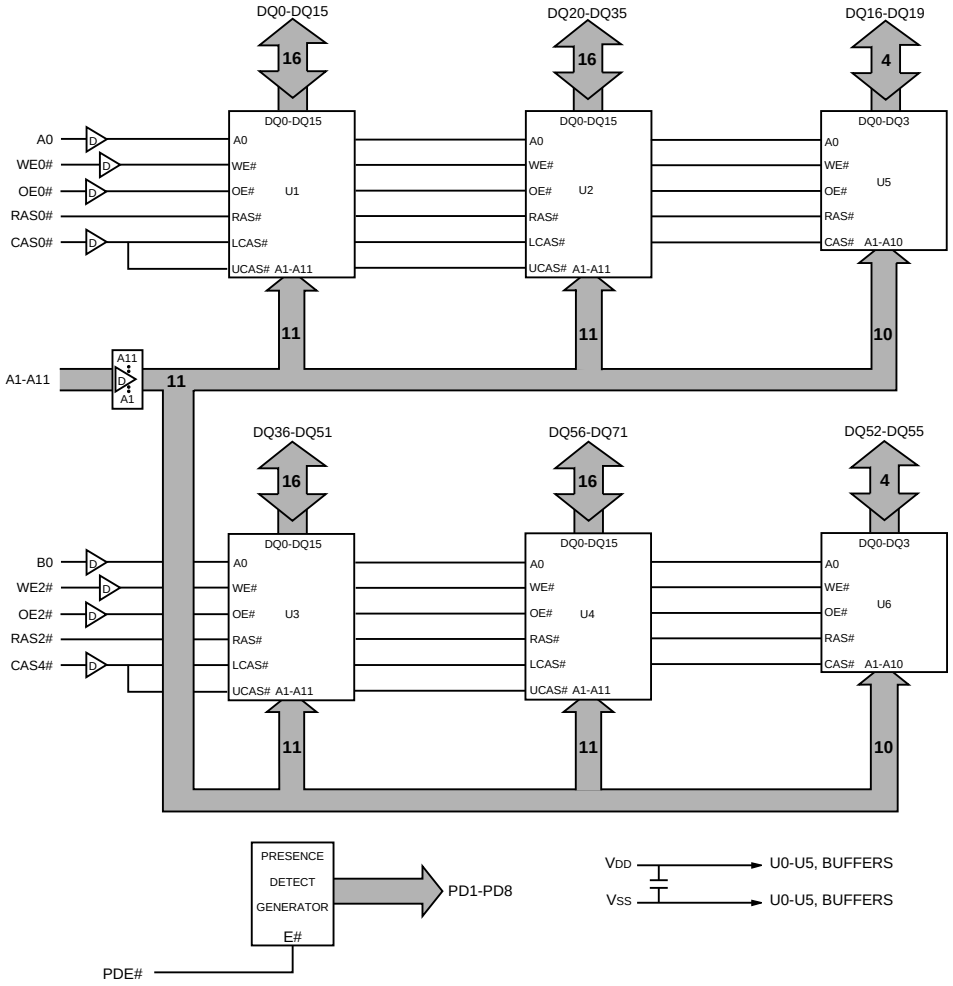
FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 4 Meg x 16 [MT4LC4M16R6] DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

FUNCTIONAL BLOCK DIAGRAM
MT6LDT472(X) (32MB)



U1-U4 = MT4LC4M16F5 FAST PAGE MODE

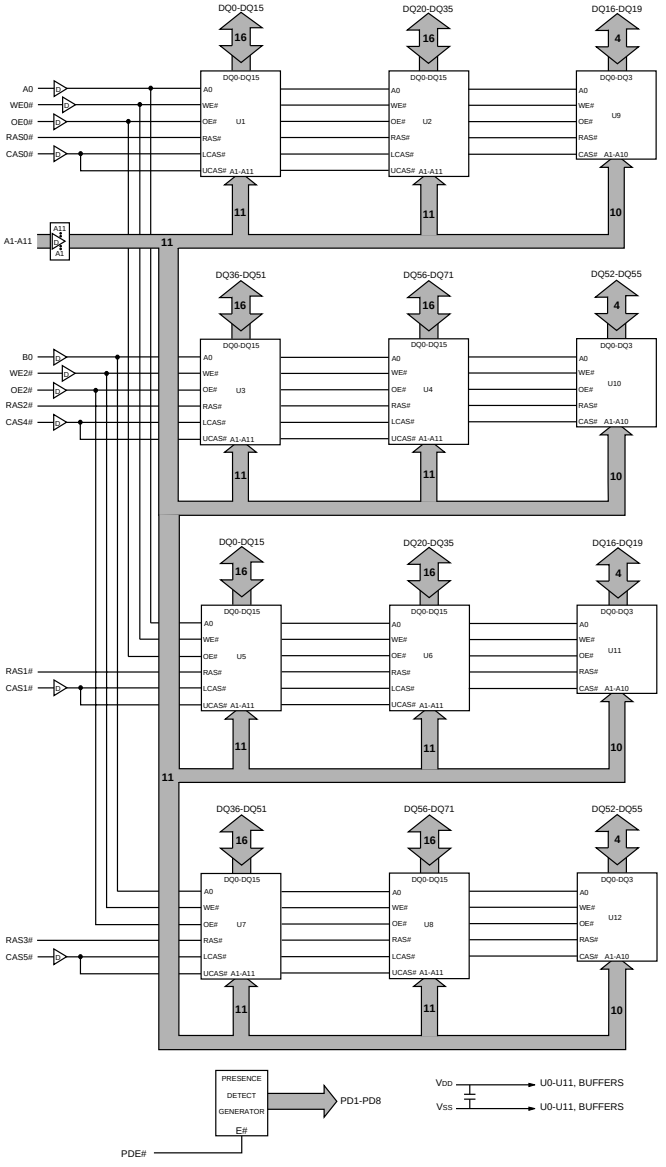
U5, U6 = MT4LC4M4A1 FAST PAGE MODE

U1-U4 = MT4LC4M16R6 EDO PAGE MODE

U5, U6 = MT4LC4M4E9 EDO PAGE MODE

NOTE: 1. All inputs, with the exception of RAS#, are redriven.
2. D = line buffers.

FUNCTIONAL BLOCK DIAGRAM
MT12LDT872(X) (64MB)



NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 114, 45, 129	RAS0#-RAS3#	Input	Row-Address Strobe: RAS# is used to clock-in the row-address bits. Two RAS# inputs allow for one x72 bank or two x36 banks.
28, 112, 46, 130	CAS0#, CAS1# CAS4#, CAS5#	Buffered Input	Column-Address Strobe: CAS# is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	WE0#, WE2#	Buffered Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. WE0# controls DQ0-DQ35. WE2# controls DQ36-DQ71. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Buffered Input	Output Enable: OE# is the input/output control for the DQ pins. OE0# controls DQ0-DQ35. OE2# controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-122, 126	A0-A11, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#. A0 is common to the DRAMs used for DQ0-DQ35 while B0 is common to the DRAMs used for DQ36-DQ71.
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either no connect (1), or they will be driven to V_{OL} (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	–	Reserved for Future Use: These pins should be left unconnected.
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	V_{SS}	Supply	Ground.
83, 167	ID0, ID1	Output	ID Bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (V_{SS}).
132	PDE#	Input	Presence-Detect Enable: PDE# is the READ control for the buffered presence-detect pins.

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	**Module Configuration**	**Row/Column Addresses**	**ID0**	**ID1**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0MB	No module installed	X			1	1	1	1				
8MB	1 Meg x 64/72	10/9			1	1	0	0				
8MB 16MB	1 Meg x 64/72 2 Meg x 64/72	10/10 10/10			0 1	0 0	1 1	0 0				
16MB 32MB	2 Meg x 64/72 4 Meg x 64/72	11/10 11/10			1 0	0 1	0 0	1 1				
• 32MB • 64MB	4 Meg x 64/72 8 Meg x 64/72	12*/11* 12*/11*			1 0	1 0	0 1	1 1				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
Data Width		x64, No Parity	Vss									
		x72, ECC	Vss									0

NOTE: V_{SS} = Ground; V_{OL} = 0; NC = 1.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Pin Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +125°C
Power Dissipation 12W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	36
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.5	0.8	V	36
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V (All other pins not under test = 0V)	CAS0#, CAS1#, CAS4#, CAS5#, A0-A11, B0, PDE#, WE0#, WE2#, OE0#, OE2#	I_{I1}	-2	2	µA	
	RAS0#-RAS3#	I_{I2}	-6	6	µA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V_{OUT} ≤ V_{DD} + 0.3V	DQ0-DQ71, PD1-PD8	I_{OZ}	-10	10	µA	37
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}	–	0.4	V	

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 5, 6) (V_{DD} = +3.3V ±0.3V)

			MAX			
PARAMETER/CONDITION	**SYMBOL**	**SIZE**	**-5***	**-6**	**UNITS**	**NOTES**
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{DD1}	32MB	63	63	mA	
		64MB	75	75	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = V_{DD} - 0.2V)	I_{DD2}	32MB	60	60	mA	
		64MB	69	69	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{DD3}	32MB	880	820	mA	3, 29
		64MB	886	826	mA	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{DD4}	32MB	–	520	mA	3, 29
		64MB	–	526	mA	
OPERATING CURRENT: EDO PAGE MODE ("X" version only) Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{DD5}	32MB	820	680	mA	3, 29
		64MB	826	686	mA	
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{DD6}	32MB	880	820	mA	3, 29
		64MB	886	826	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{DD7}	32MB	880	820	mA	3, 4
		64MB	886	826	mA	

* EDO version only

CAPACITANCE

		MAX			
PARAMETER	**SYMBOL**	**32MB**	**64MB**	**UNITS**	**NOTES**
Input Capacitance: A0-A11, B0, PDE#, OE0#, OE2#	C_{I1}	6	6	pF	2
Input Capacitance: WE0#, WE2#, CAS0#, CAS1#, CAS4#, CAS5#	C_{I2}	6	6	pF	2
Input Capacitance: RAS0#-RAS3#	C_{I3}	24	24	pF	2
Input/Output Capacitance: DQ0-DQ71	C_{IO}	10	17	pF	2
Output Capacitance: PD1-PD8	C_O	10	10	pF	2

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 35) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		35	ns	23
Column-address hold time (referenced to RAS#)	^tAR	43		ns	22
Column-address setup time	^tASC	2		ns	21
Row-address setup time	^tASR	5		ns	23
Column address to WE# delay time	^tAWD	57		ns	21, 28
Access time from CAS#	^tCAC		20	ns	14, 23
Column-address hold time	^tCAH	15		ns	23
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	8		ns	4, 22
CAS# to output in Low-Z	^tCLZ	5		ns	21, 30
CAS# precharge time	^tCP	10		ns	15
Access time from CAS# precharge	^tCPA		40	ns	23
CAS# to RAS# precharge time	^tCRP	10		ns	23
CAS# hold time	^tCSH	58		ns	22
CAS# setup time (CBR Refresh)	^tCSR	7		ns	4, 21
CAS# to WE# delay time	^tCWD	42		ns	21, 28
WRITE command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	15		ns	23, 27
Data-in setup time	^tDS	-2		ns	22, 27
Output disable	^tOD	3	15	ns	
Output enable	^tOE		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	13		ns	22, 26
Output buffer turn-off delay	^tOFF	5	20	ns	19, 25,33
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	
PDE# to valid presence-detect data	^tPD		10	ns	32
PDE# inactive to presence-detects inactive	^tPDOFF	2		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	87		ns	21
Access time from RAS#	^tRAC		60	ns	13
RAS# to column-address delay time	^tRAD	13		ns	17, 24
Row-address hold time	^tRAH	8		ns	22
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	110		ns	
RAS# to CAS# delay time	^tRCD	18		ns	16, 24
READ command hold time (referenced to CAS#)	^tRCH	2		ns	18, 21
READ command setup time	^tRCS	2		ns	21
Refresh period (4,096 cycles)	^tREF		64	ms	

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 35) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
RAS# precharge time	^{t}RP	40		ns	
RAS# to CAS# precharge time	^{t}RPC	0		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		ns	18
RAS# hold time	^{t}RSH	20		ns	23
READ-WRITE cycle time	^{t}RWC	160		ns	23
RAS# to WE# delay time	^{t}RWD	87		ns	21, 28
WRITE command to RAS# lead time	^{t}RWL	20		ns	23
Transition time (rise or fall)	^{t}T	2	50	ns	
WRITE command hold time	^{t}WCH	15		ns	23
WRITE command hold time (referenced to RAS#)	^{t}WCR	43		ns	22
WE# command setup time	^{t}WCS	2		ns	21, 28
WRITE command pulse width	^{t}WP	10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		ns	22
WE# setup time (CBR Refresh)	^{t}WRP	12		ns	21

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 33) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		30		35	ns	24
Column-address setup to CAS# going HIGH during WRITE	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	36		43		ns	22
Column-address setup time	^tASC	2		2		ns	21
Row-address setup time	^tASR	5		5		ns	24
Column address to WE# delay time	^tAWD	44		51		ns	22, 28
Access time from CAS#	^tCAC		18		20	ns	14, 24
Column-address hold time	^tCAH	13		15		ns	24
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	6		8		ns	4, 22
CAS# to output in Low-Z	^tCLZ	2		2		ns	22, 30
Data output hold after CAS# LOW	^tCOH	5		5		ns	
CAS# precharge time	^tCP	8		10		ns	15
Access time from CAS# precharge	^tCPA		33		40	ns	24
CAS# to RAS# precharge time	^tCRP	10		10		ns	24
CAS# hold time	^tCSH	36		43		ns	23
CAS# setup time (CBR Refresh)	^tCSR	7		7		ns	4, 22
CAS# to WE# delay time	^tCWD	30		37		ns	22, 28
WRITE command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	13		15		ns	24, 27
Data-in setup time	^tDS	-2		-2		ns	23, 27
Output disable	^tOD	0	12	0	15	ns	30
Output enable	^tOE		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	6		8		ns	23
OE# HIGH hold time from CAS# HIGH	^tOEHC	5		10		ns	
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	2	17	2	20	ns	19, 26
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	
PDE# to valid presence-detect data	^tPD		10		10	ns	31
PDE# inactive to presence-detects inactive	^tPDOFF	2		2		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	49		58		ns	22
Access time from RAS#	^tRAC		50		60	ns	13
RAS# to column-address delay time	^tRAD	7		10		ns	17, 25
Row-address hold time	^tRAH	7		8		ns	23
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	9		12		ns	16, 25

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 33) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ command hold time (referenced to CAS#)	^{t}RCH	2		2		ns	18, 22
READ command setup time	^{t}RCS	2		2		ns	22
Refresh period (4,096 cycles)	^{t}REF		64		64	ms	
RAS# precharge time	^{t}RP	30		40		ns	
RAS# to CAS# precharge time	^{t}RPC	5		5		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	18
RAS# hold time	^{t}RSH	18		20		ns	24
READ-WRITE cycle time	^{t}RWC	121		145		ns	24
RAS# to WE# delay time	^{t}RWD	69		81		ns	22, 29
WRITE command to RAS# lead time	^{t}RWL	18		20		ns	24
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
WRITE command hold time	^{t}WCH	13		15		ns	24
WRITE command hold time (referenced to RAS#)	^{t}WCR	36		43		ns	23
WE# command setup time	^{t}WCS	2		2		ns	22, 28
WE# to outputs in High-Z	^{t}WHZ	2	17	2	20	ns	24
WRITE command pulse width	^{t}WP	5		5		ns	
WE# pulse width to disable outputs	^{t}WPZ	10		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	6		8		ns	23
WE# setup time (CBR Refresh)	^{t}WRP	10		12		ns	22

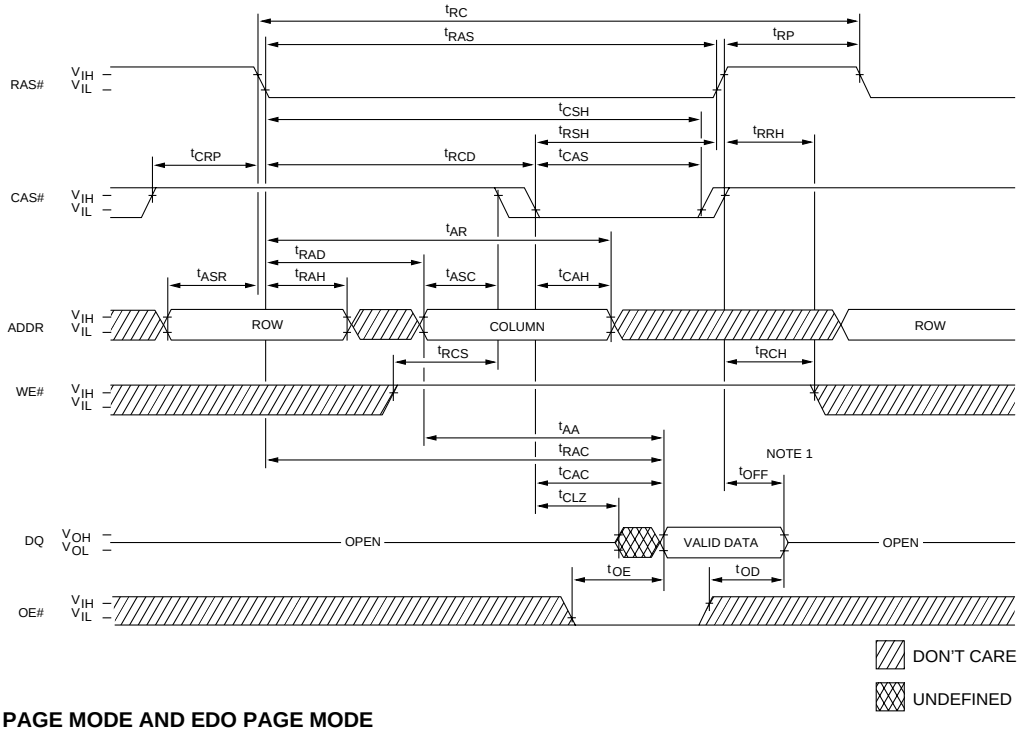
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
3. I_{DD} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns for FPM and 2.5ns for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. Requires that ^{t}AA and ^{t}CAC are not violated.
14. Requires that ^{t}AA and ^{t}RAC are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
16. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
17. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
18. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
19. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
22. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
23. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^{t}OEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
27. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
28. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}WCS < ^{t}WCS (MIN) and ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
29. Column address changed once each cycle.
30. The 3ns minimum parameter guaranteed by design.

NOTES (continued)

31. ^{t}PDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
32. Measured with specified current load and 100pF.
33. With the FPM option, ^{t}OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
34. Applies to both FPM and EDO operating modes.
35. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
36. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.
37. 32MB module values will be half of those shown.

READ CYCLE [34]



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

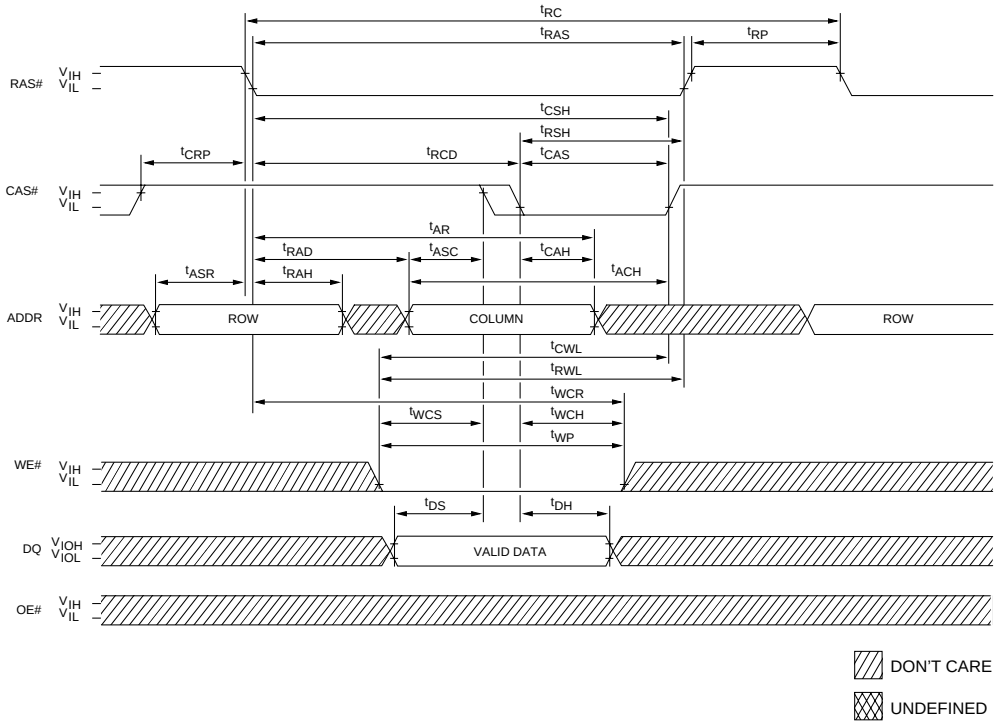
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tACH (EDO)	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCLZ (EDO)	2		2		ns
tCLZ (FPM)	–		5		ns
tCRP	10		10		ns
tCSH (EDO)	36		43		ns
tCSH (FPM)	–		58		ns
tOD (EDO)	0	12	0	15	ns
tOD (FPM)	–	–	3	15	ns
tOE		12		15	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOFF (EDO)	2	17	2	20	ns
tOFF (FPM)	–	–	5	20	ns
tRAC		50		60	ns
tRAD (EDO)	7		10		ns
tRAD (FPM)	–		13		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRC (EDO)	84		104		ns
tRC (FPM)	–		110		ns
tRCD (EDO)	9		12		ns
tRCD (FPM)	–		18		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	18		20		ns

*EDO version only

NOTE: 1. For EDO, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE [34]



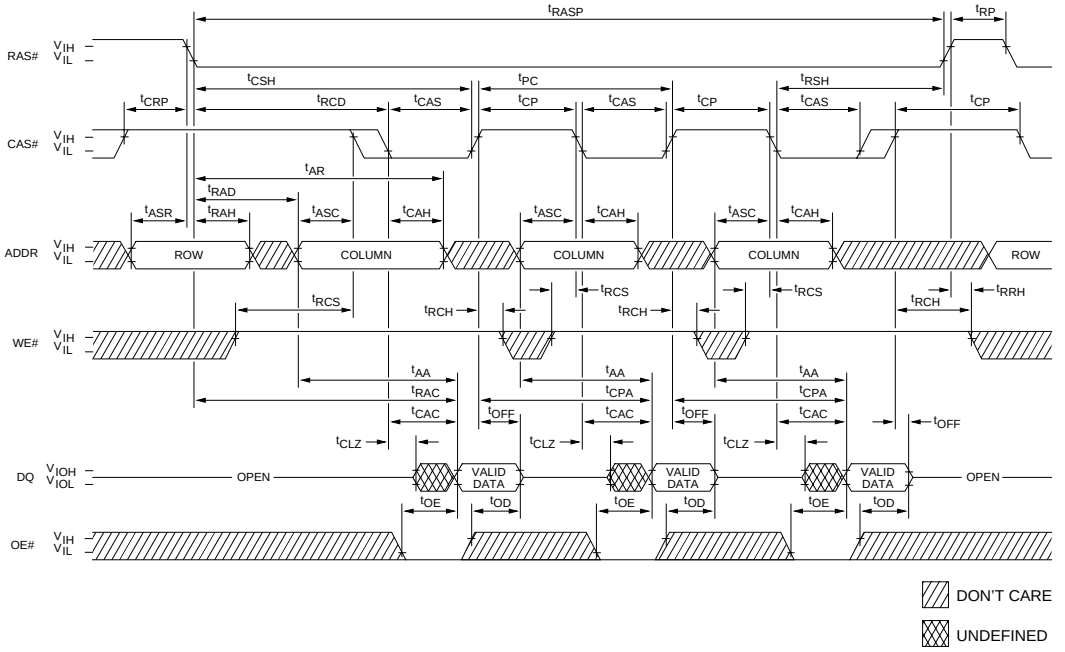
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tACH (EDO)	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAH	13		15		ns
tCAS (FPM)	–	–	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCRP	10		10		ns
tCSH (FPM)	–		58		ns
tCSH (EDO)	36		43		ns
tCWL (FPM)	–		15		ns
tCWL (EDO)	8		10		ns
tDH	13		15		ns
tDS	-2		-2		ns
tRAD (FPM)	–		13		ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tRAD (EDO)	7		10		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	–		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	–		18		ns
tRCD (EDO)	9		12		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWL	18		20		ns
tWCH	13		15		ns
tWCR	36		43		ns
tWCS	2		2		ns
tWP (FPM)	–		10		ns
tWP (EDO)	5		5		ns

*EDO version only

FAST-PAGE-MODE READ CYCLE

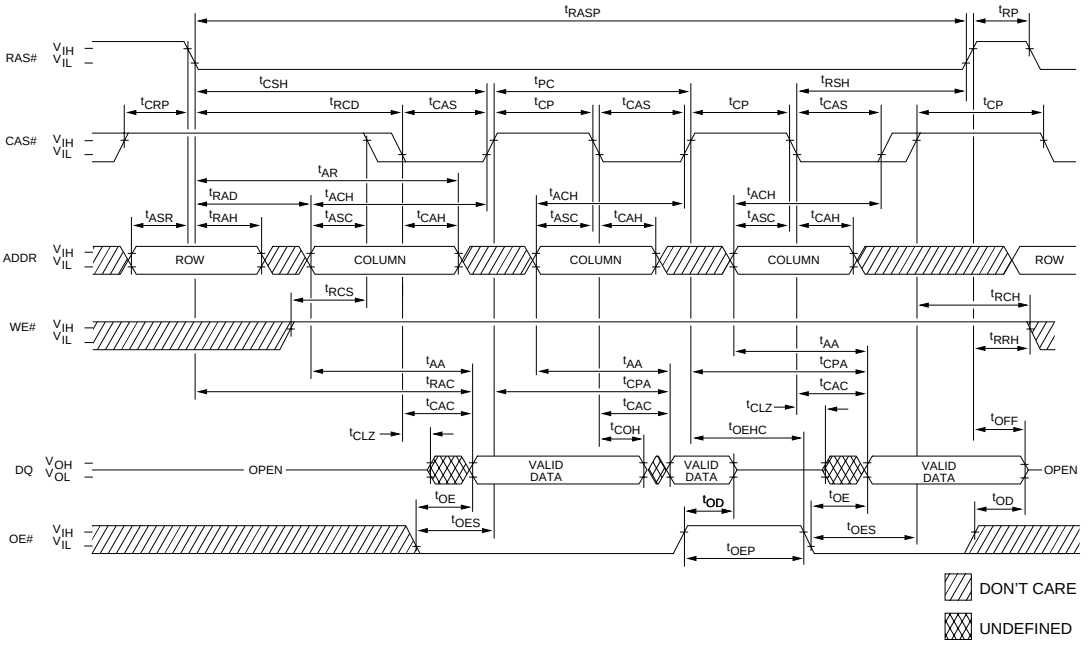


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		35	ns
tAR	43		ns
tASC	2		ns
tASR	5		ns
tCAC		20	ns
tCAH	15		ns
tCAS	15	10,000	ns
tCLZ	5		ns
tCP	10		ns
tCPA		40	ns
tCRP	10		ns
tCSH	58		ns
tOD	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOE		15	ns
tOFF	5	20	ns
tPC	35		ns
tRAC		60	ns
tRAD	13		ns
tRAH	8		ns
tRASP	60	125,000	ns
tRCD	18		ns
tRCH	2		ns
tRCS	2		ns
tRP	40		ns
tRRH	0		ns
tRSH	20		ns

EDO-PAGE-MODE READ CYCLE

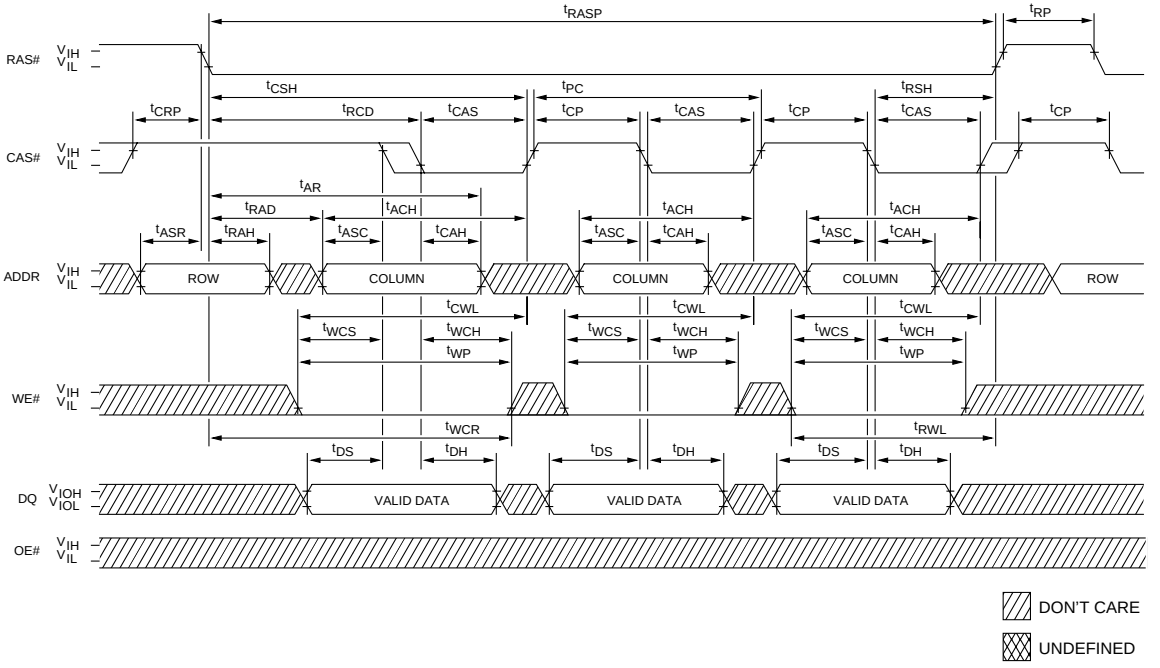


EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	2		2		ns
tCOH	5		5		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH	36		43		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	2	17	2	20	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	18		20		ns

FAST/EDO-PAGE-MODE EARLY WRITE CYCLE [34]



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

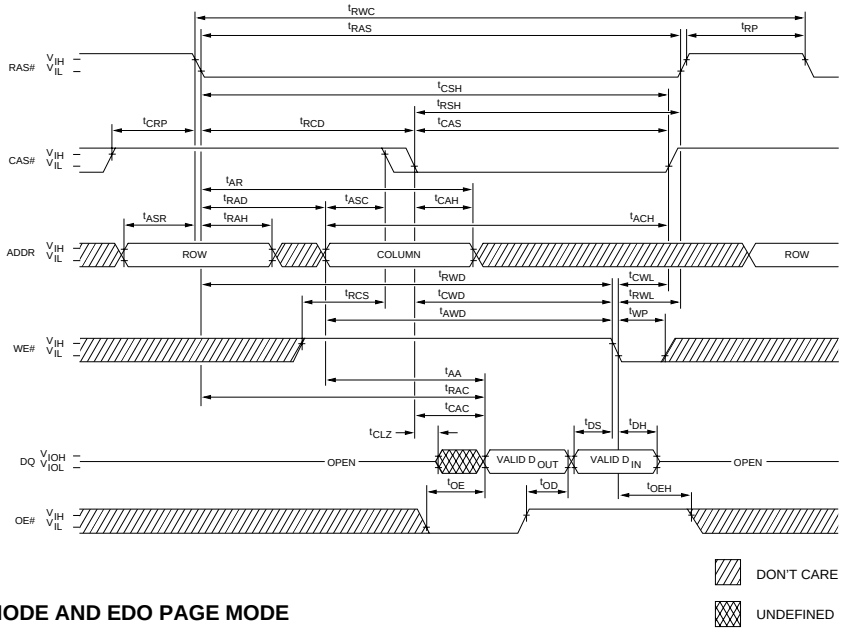
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tACH (EDO)	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAH	13		15		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCP	8		10		ns
tCRP	10		10		ns
tCSH (EDO)	36		43		ns
tCSH (FPM)	–		58		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	–		15		ns
tDH	13		15		ns
tDS	-2		-2		ns
tPC (EDO)	20		25		ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tPC (FPM)	–		35		ns
tRAD (EDO)	7		10		ns
tRAD (FPM)	–		13		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	9		12		ns
tRCD (FPM)	–		18		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWL	18		20		ns
tWCH	13		15		ns
tWCR	36		43		ns
tWCS	2		2		ns
tWP (EDO)	5		5		ns
tWP (FPM)	–		10		ns

*EDO version only

READ-WRITE CYCLE [34]

(LATE WRITE and READ-MODIFY-WRITE cycles)



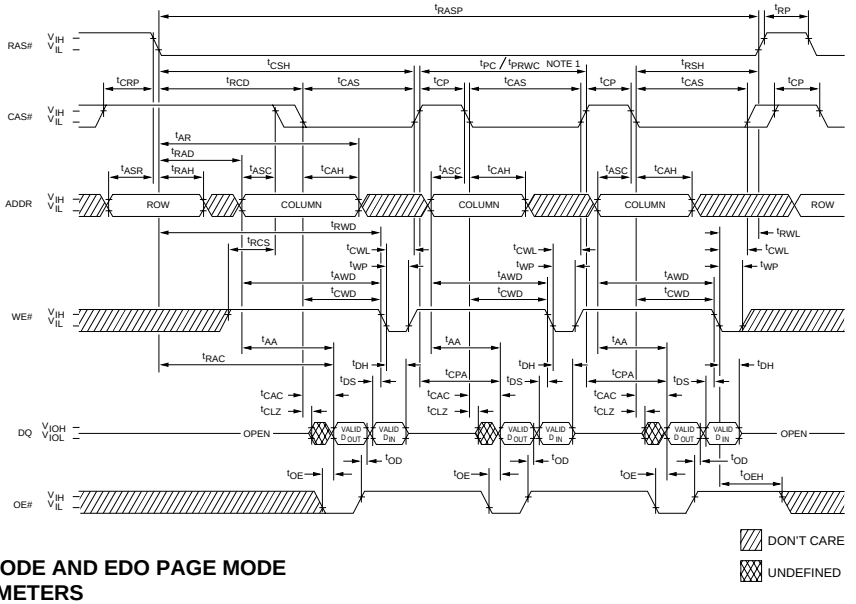
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tACH (EDO)	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tAWD (EDO)	44		51		ns
tAWD (FPM)	–		57		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCLZ (EDO)	2		2		ns
tCLZ (FPM)	–		5		ns
tCRP	10		10		ns
tCSH (EDO)	36		43		ns
tCSH (FPM)	–		58		ns
tCWD (EDO)	30		37		ns
tCWD (FPM)	–		42		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	–		15		ns
tDH	13		15		ns
tDS	-2		-2		ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOD (EDO)	0	12	0	15	ns
tOD (FPM)	–	–	3	15	ns
tOE		12		15	ns
tOEH (EDO)	6		8		ns
tOEH (FPM)	–		13		ns
tRAC		50		60	ns
tRAD (EDO)	7		10		ns
tRAD (FPM)	–		13		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRCD (EDO)	9		12		ns
tRCD (FPM)	–		18		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWC (EDO)	121		145		ns
tRWC (FPM)	–		160		ns
tRWD (EDO)	69		81		ns
tRWD (FPM)	–		87		ns
tRWL	18		20		ns
tWP (EDO)	5		5		ns
tWP (FPM)	–		10		ns

*EDO version only

FAST/EDO-PAGE-MODE READ-WRITE CYCLE [34]
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

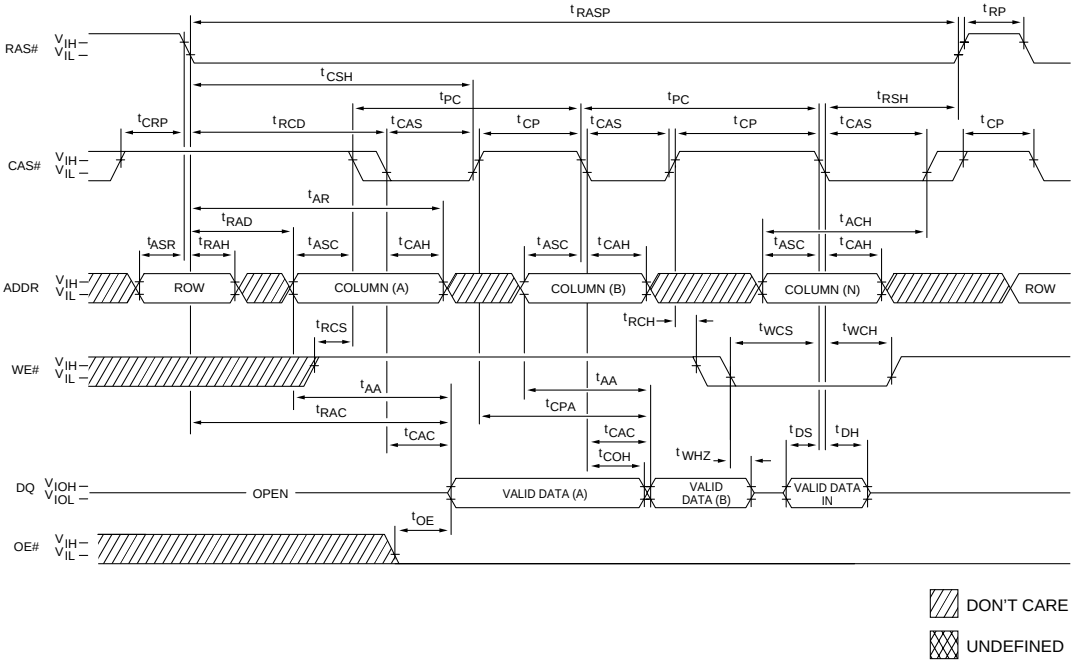
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tAWD (EDO)	44		51		ns
tAWD (FPM)	–		57		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCLZ (EDO)	2		2		ns
tCLZ (FPM)	–		5		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH (EDO)	36		43		ns
tCSH (FPM)	–		58		ns
tCWD (EDO)	30		37		ns
tCWD (FPM)	–		42		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	–		15		ns
tDH	13		15		ns
tDS	-2		-2		ns
tOD (EDO)	0	12	0	15	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOD (FPM)	–	–	3	15	ns
tOE		12		15	ns
tOEH (EDO)	6		8		ns
tOEH (FPM)	–		13		ns
tPC (EDO)	20		25		ns
tPC (FPM)	–		35		ns
tPRWC (EDO)	49		58		ns
tPRWC (FPM)	–		87		ns
tRAC		50		60	ns
tRAD (EDO)	7		10		ns
tRAD (FPM)	–		13		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	9		12		ns
tRCD (FPM)	–		18		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWD (EDO)	69		81		ns
tRWD (FPM)	–		87		ns
tRWL	18		20		ns
tWP (EDO)	5		5		ns
tWP (FPM)	–		10		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

*EDO version only

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

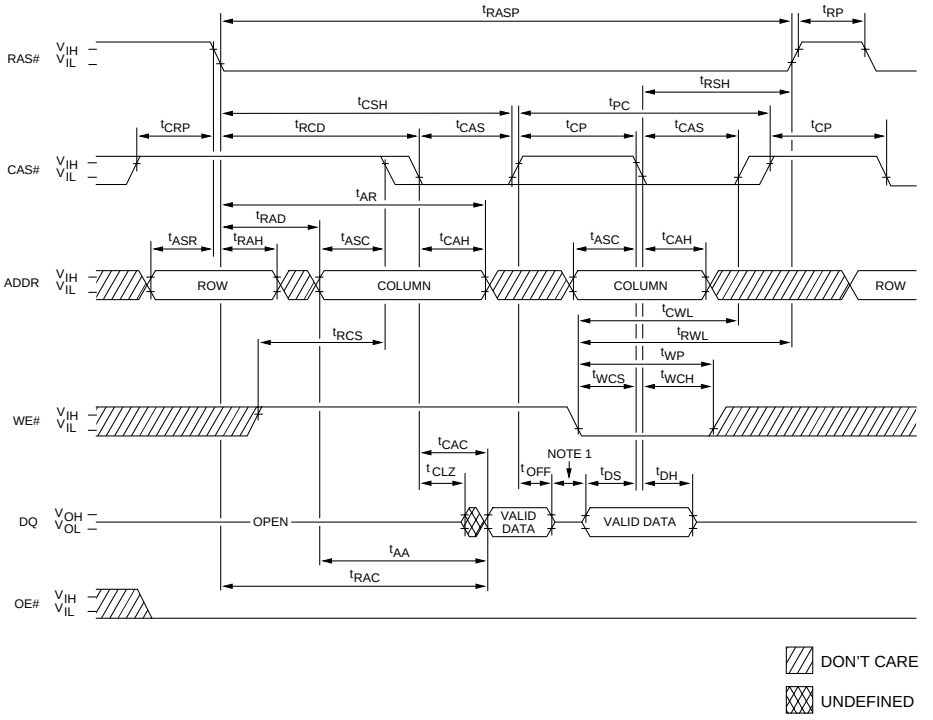


EDO PAGE MODE TIMING PARAMETERS

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCOH	5		5		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH	36		43		ns
tDH	13		15		ns
tDS	-2		-2		ns

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tWCH	13		15		ns
tWCS	2		2		ns
tWHZ	2	17	2	20	ns

FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



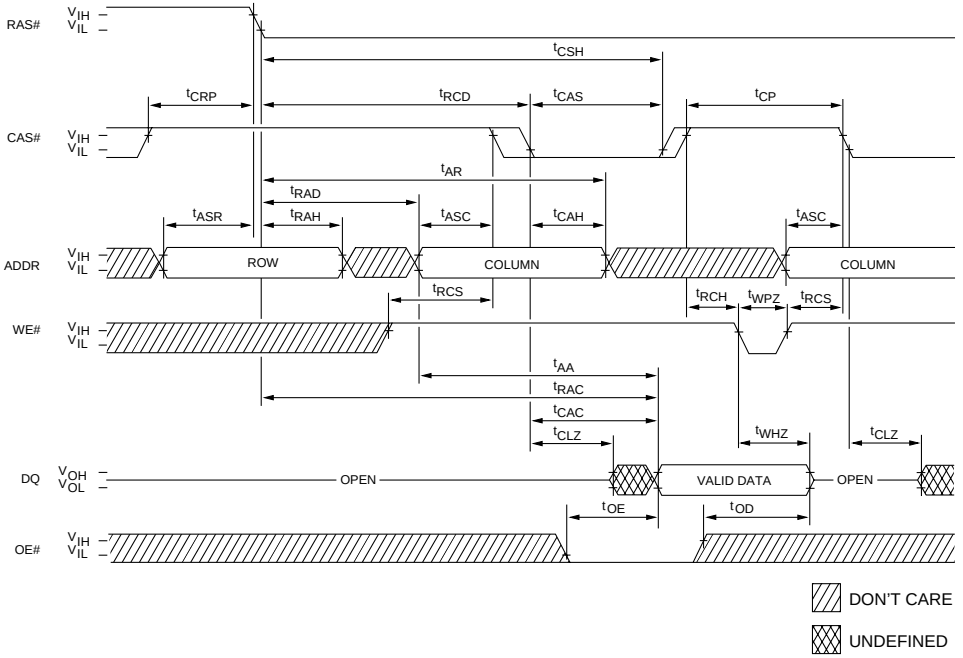
FAST PAGE MODE
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		35	ns
tAR	43		ns
tASC	2		ns
tASR	5		ns
tCAC		20	ns
tCAH	15		ns
tCAS	15	10,000	ns
tCLZ	5		ns
tCP	10		ns
tCRP	10		ns
tCSH	58		ns
tCWL	15		ns
tDH	15		ns
tDS	-2		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	5	20	ns
tPC	35		ns
tRAC		60	ns
tRAD	13		ns
tRAH	8		ns
tRASP	60	125,000	ns
tRCD	18		ns
tRCS	2		ns
tRP	40		ns
tRSH	20		ns
tRWL	20		ns
tWCH	15		ns
tWCS	2		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)

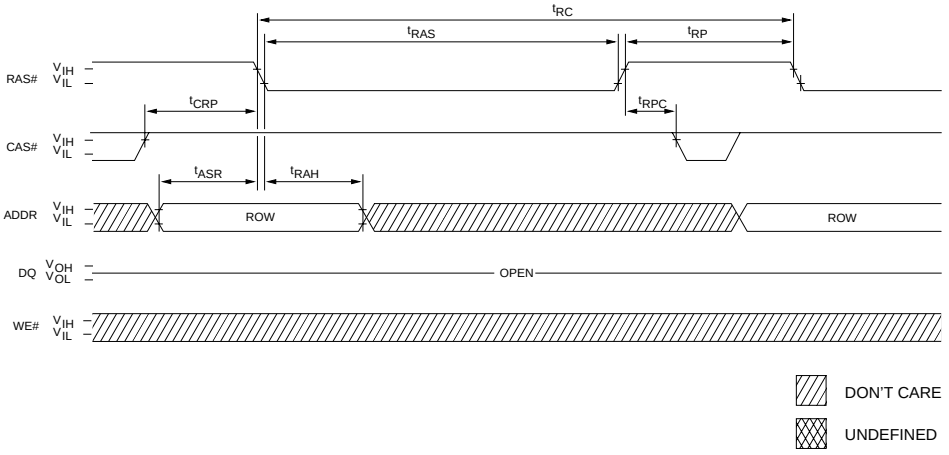


EDO PAGE MODE
TIMING PARAMETERS

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	2		2		ns
tCP	8		10		ns
tCRP	10		10		ns
tCSH	36		43		ns

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tWHZ	2	17	2	20	ns
tWPZ	10		10		ns

RAS#-ONLY REFRESH CYCLE [34]



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

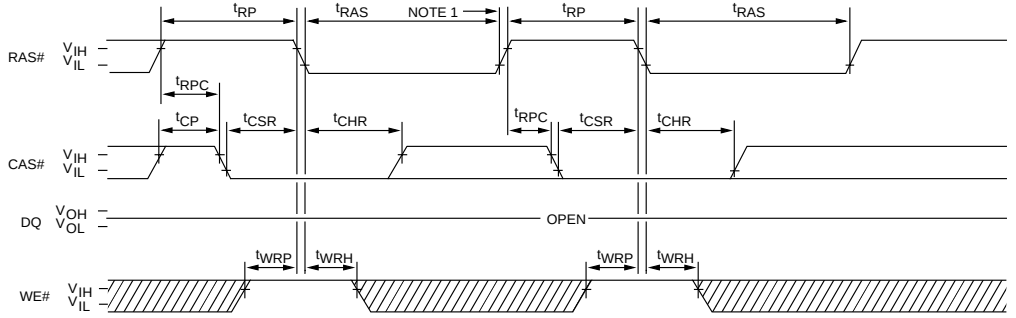
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tASR	5		5		ns
tCRP	10		10		ns
tCSR	7		7		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tRC (FPM)	–		110		ns
tRC (EDO)	84		104		ns
tRP	30		40		ns
tRPC (FPM)	–		0		ns
tRPC (EDO)	5		5		ns

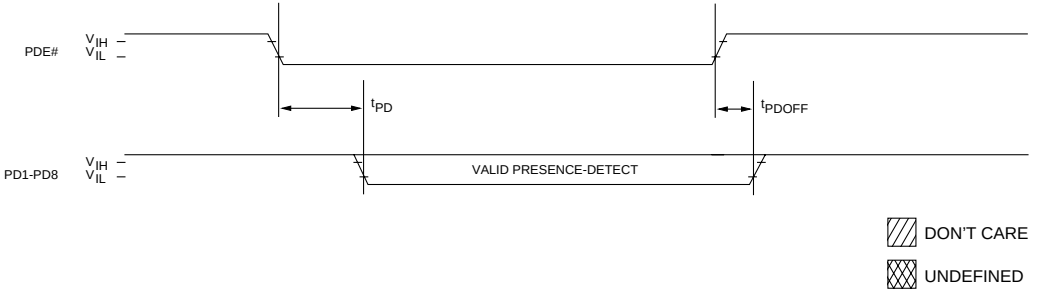
*EDO version only

CBR REFRESH CYCLE [34]

(Addresses, OE# = DON'T CARE)



PRESENCE-DETECT READ CYCLE [34]



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tCHR	6		8		ns
tCP	8		10		ns
tCSR	7		7		ns
tPD		10		10	ns
tPDOFF	2		2		ns
tRAS	50	10,000	60	10,000	ns

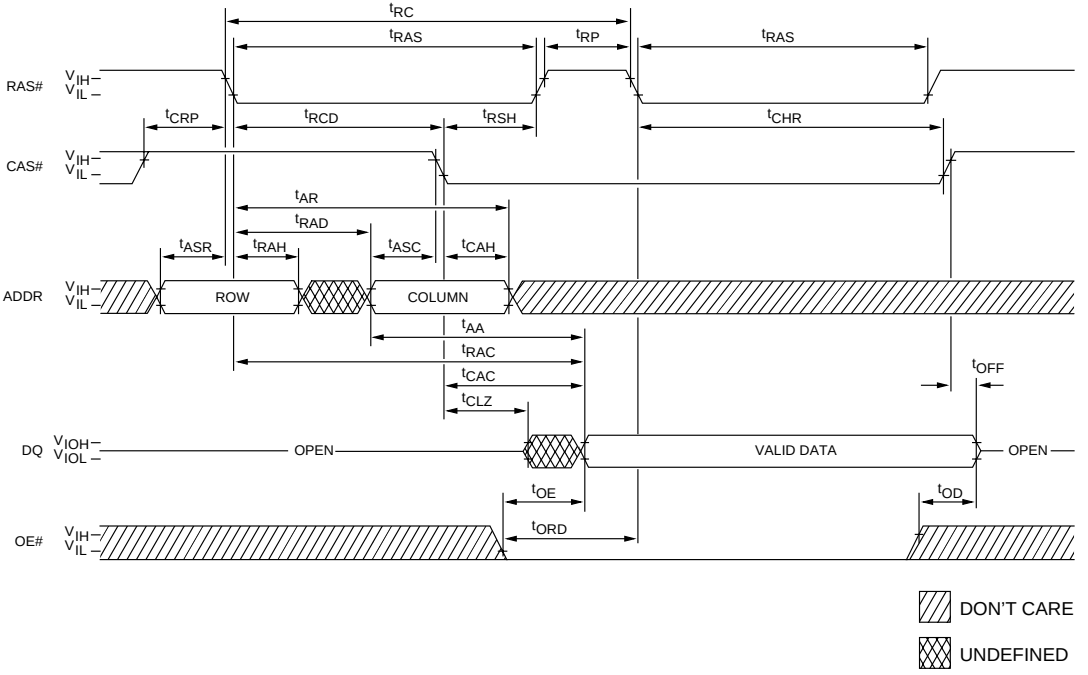
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tRP	30		40		ns
tRPC (FPM)	–		0		ns
tRPC (EDO)	5		5		ns
tWRH	6		8		ns
tWRP	10		12		ns

*EDO version only

NOTE: 1. PD pins must be pulled HIGH at next level of assembly.

HIDDEN REFRESH CYCLE [20, 34]

(WE# = HIGH; OE# = LOW)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCHR	6		8		ns
tCLZ (FPM)	–		5		ns
tCLZ (EDO)	2		2		ns
tCRP	10		10		ns
tOD (FPM)	–	–	3	15	ns
tOD (EDO)	0	12	0	15	ns
tOE		12		15	ns

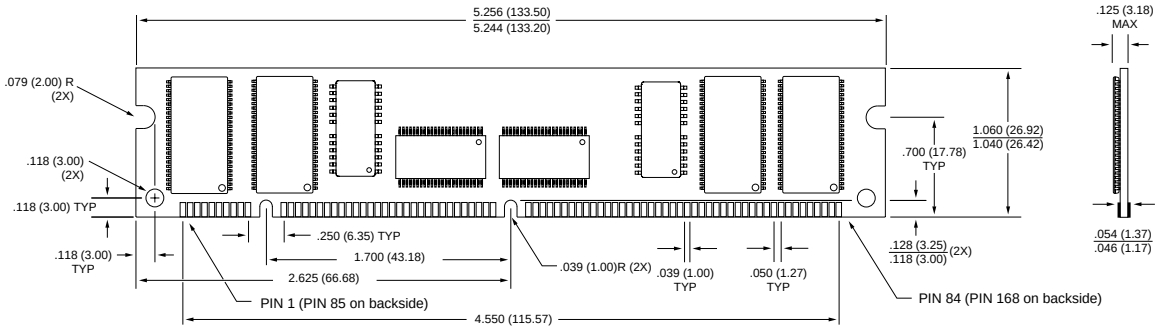
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOFF (FPM)	–	–	5	20	ns
tOFF (EDO)	2	17	2	20	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD (FPM)	–		13		ns
tRAD (EDO)	7		10		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRCD (FPM)	–		18		ns
tRCD (EDO)	9		12		ns
tRP	30		40		ns
tRSH	18		20		ns

*EDO version only

168-PIN DIMM

(32MB)

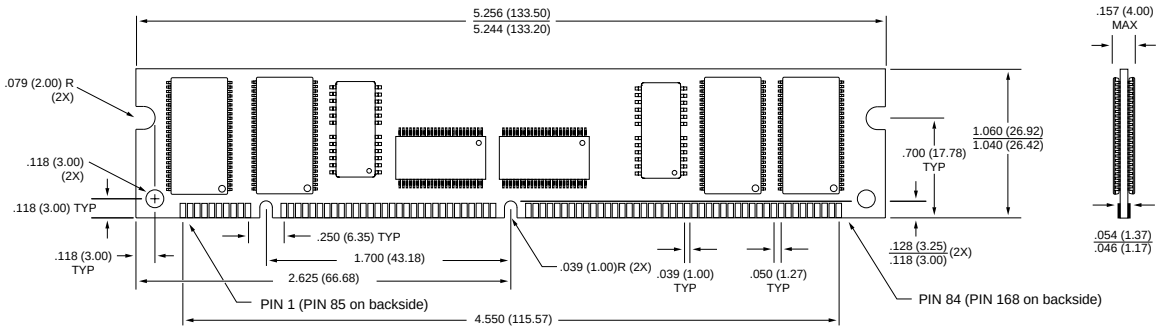
FRONT VIEW



168-PIN DIMM

(64MB)

FRONT VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992