Micro Linear

Application Note 78
ML2722 & ML2751 Evaluation Design

OVERVIEW

The ML2722/ML2751 evaluation design demonstrates the performance, simplicity and size of a transceiver for two application areas. First is a Direct Sequence Spread Spectrum (DSSS) at 1.536M chips per second and a 102.4Kb data rate. Second is a 1mW low power transceiver operating at up to a 1.6Mbps data rate. The design shows how a low cost, high performance radio can be built with the ML2722 Low IF Transceiver, ML2751 Power and Low Noise Amplifier and a small number of discrete components, without expensive, single sourced, filters.

The design is suitable for direct inclusion into products using the 902 - 928MHz ISM band such as:

- cordless phones
- transceiver links
- wireless networks
- game controllers

CIRCUIT DIAGRAM AND LAYOUT

The circuit diagram for the ML2722/ML2751 evaluation design is given in Figure 1. The layout is given in Figure 2. A Bill of Materials is attached as Appendix A.

NOTE: The operator must insure that all laws and regulations of the country of operation are obeyed. This includes suitable shielding, enclosures and Faraday cages.

FEATURES

- Transceiver area only 37 x 21mm
- Low component count - 2 ICs, 59 discretes plus the reference oscillator
- Low cost
- Double sided FR4 PCB populated on one side only
- Easy connection to test system - single 34 pin IDC connector with all baseband connections

CIRCUIT DESCRIPTION

The evaluation design consists of the ML2722 transceiver, the ML2751 LNA/PA IC and discrete circuitry for the RF filtering, PLL loop filter and T/R switch. At the baseband end, the ML2722 is connected to a 34 way IDC connector for ease of connection to a personal computer or micro processor for evaluation. At the RF end, a single SMA connector provides the antenna connection for transmit and receive.

DESIGN DESCRIPTION

ML2722

Regulator Decoupling

The components surrounding the ML2722 are mainly decoupling capacitors. The regulators are designed to work with 220nF capacitive load. Ceramic dielectric types are suitable for C6, C7, C8, C9, C10, C11, C12 and C13. The input supplies have extra 10nF dielectric capacitors (C1, C2) to improve the frequency range of the decoupling.

To improve the supply rejection at the VCO which would result in unwanted modulation, the VCO supply is double regulated. The VCO regulator takes its input from the output of the mixer regulator, RVCC7, pin 27. R2 and C3 provide an extra pole of filtering between this output and the VCO regulator input, VCC2. The regulators have a bandwidth greater than 3MHz with the 220nF decouplers used. The maximum value of R2 is set by the maximum voltage drop (= the difference between VRVCC7 (2.7V) and the dropout voltage of the VCO regulator plus margin (1.5V)) and the VCO current of approx 8mA max. A value much less than this (10Ω) has been found to be adequate. The value of C3 is not critical, but can be varied to change the roll off of this network. The 10Ω and 10nF values set the -3dB point at 1.5MHz.

Reference Frequency Input

The reference frequency for the PLL is capacitively coupled in to REF, pin 9. The maximum value of the coupling capacitor is set by the transceiver startup time from cold. Pin 9 is a CMOS input with 80KΩ bias resistors to VDD and GND. 470pF is a good compromise between loss of signal level across the capacitor and a fast start-up time.

Loop Filter

The dynamics of the PLL are set by the loop filter. This network is connected from VTUNE (pin 15) and GND. The values given on the circuit diagram are for a loop bandwidth of 54KHz and a damping factor of 0.8. In practice, the measured overshoot when switching between receive and transmit modes is only about 4KHz.

The VCO operates open loop during the transmit and receive slots to reduce power consumption. During such periods the loop filter must maintain the voltage with very little droop. The KV of the VCO at the 900MHz output frequency is approx 90MHz/V, so for a drift of <10KHz the filter voltage must change by less than 0.11mV. For a 47nF loop filter capacitor, the leakage current during a 10ms slot must be less than 500pA! The VTUNE input and QPO output are very high impedances during the transmit and receive slots. PCB soldering flux, dirt and moisture can all cause excessive frequency drift, resulting in out of spec emissions on transmit or loss of sensitivity on receive. In high field strength electrical fields, electrostatic pickup may be a problem, (e.g., from power cables) and screening will be necessary. For applications where moisture may condense on the board, conformal coating is recommended to alleviate any problems.

The PCB layout allows for two types of loop filter capacitors. For applications where mechanical and thermal shock are low, ceramic dielectric capacitors may be used. The smaller value (C44) should preferably be C0G or NP0 dielectric (minimum change with temperature) and the larger value (C45) X7R (-55^{0}C to +125^{0}C with +/-15% change) dielectric. Dielectrics with high temperature coefficients such as Y5V (-30^{0}C to +85^{0}C with -82% to +22% change) or Z5U (+10^{0}C to +85^{0}C with -56% to +22% change) should be avoided. In addition to the problem of the potential for loop instability at temperature extremes, these dielectrics are more piezoelectric and will cause a larger frequency excursion under mechanical shock.

For other applications where the ceramic capacitors are not considered acceptable, the PCB will accept WIMA polyester 2220 series for C20 and an 0805 size for C21, eg Panasonic polyphenylene sulphide ECHU series.

Transmit Output, TRFO

The signal output from the ML2722 in transmit mode is from TRFO, pin 23. The output impedance is nominally 50Ω (the output stage being an emitter follower with a series resistor to define the impedance). This configuration gives the lowest harmonic distortion (<-30dBc) without external filtering. The output is active both during VCO calibration and during transmit.

The VCO runs at twice the output frequency, and is therefore susceptible to changes in the level at the 2nd harmonic of the output frequency around the IC, hence the low distortion output stage. If this output is used to drive a non-linear load such as a class-C PA input (which is enabled after the PLL has gone open loop), care must be taken to minimize the amount of 2nd harmonic reaching the TRFO pin. The problems manifest themselves as a frequency shift on the VCO.

In practice, the combination of the ML2751 input and a simple filter, such as the 3 pole Butterworth, f-3dB = 1.2GHz, formed by C42, the microstrip track and C43, is acceptable.

Receive Input, RRFI

The impedance at the receive input, RRFI (pin 21), must be matched to 50Ω with an external network. The input impedance of the ML2722 RRFI pin is typically 180Ω/3pF at 915MHz. In this design, the matching is achieved from the final resonator of a two pole filter. The input is onto the base of a bipolar transistor and therefore requires ac coupling.

DESIGN DESCRIPTION

ML2751

The ML2751 contains the PA, LNA and PIN switch drivers in this design. Additionally, all control (turn on and turn off) of the PA is handled by circuitry internal to the ML2751.

Transmit Path

The ML2751 is in the transmit mode when both PAON (pin 1) and FEEN (pin 2) are both high. In this state the PIN switch drivers assume the state with PIN (pin 12) high and PINB (pin 13) low.

The PA input TRFI (pin 3) is driven from the lowpass filter by the output of the ML2722 (pin 23). The filter reduces 2nd harmonic generated in the base emitter junction of the input transistor inside the ML2751 and prevents pulling the VCO.

Internally the PA is a three stage amplifier with the first two stages obtaining power from VCC pin 15. The final stage is a grounded emitter transistor with an open collector, operated in class C. The connection to the supply is via the discrete inductor L1. The range and values of the decoupling capacitors on the supply end of L1 are essential due to the high currents which flow, and to reduce supply induced AM.

The optimum impedance presented to TPAO for maximum power output and efficiency is 21Ω/4.7pF. On the PCB, a 6th order lowpass Chebyshev filter removes the harmonics and transforms the 50Ω load to close to 21Ω at the ML2751. The supply inductor L1 is resonated at 915MHz with the capacitor C47 to correct the shunt susceptance to maximize output power. This also forms a pole providing additional harmonic attenuation. Additional deviations from a classical filter topology are provided by the inductance in the ground connections of the capacitors, which provide notches at the harmonic frequency, and the ac-coupling capacitor C15, which resonates out some of the stray inductance in the PCB trace and the PIN diode bond wires. The final shunt capacitance of the filter is distributed between C41 and C40 on the output.

The transmit/receive switching is achieved with a PIN diode switch. Use of a double diode keeps the BOM cost low. The forward diode achieves a resistance of approx 2Ω at the 5mA dc current used. The off diode has approx 2V reverse bias (hence the use of two resistors R6 and R8, otherwise only 0.7V reverse bias would be achieved if L7 and L8 joined to a common resistor), however significant amounts of harmonic regrowth were observed, which was cured by splitting the last capacitor of the transmit filter. The harmonics are reduced by:

a) the LC filtering from trace inductance and C40, and
b) the change of matching components for the receive path. This reduces C37, such that in transmit, the receive diode has a higher impedance to ground, and therefore generates less harmonic current.

Bias voltages are applied to the diodes through 220nH inductors L7 through L9 which present an impedance of several kΩ at 900MHz. The 22pF decouplers on the cold end of each inductor ensure that any RF leakage goes no further.

The load impedance presented at the SMA connector should be 50Ω.

The output power from the connector is set to +20dBm by R3.

Resistor R5 sets the gain of the ML2751 power control circuitry to the highest gain setting, and resistor R3 is used to set the output power.

Receive Path

The ML2751 is in the receive mode when PAON (pin 1) is low and FEEN (pin 2) is high. In this state the PIN switch drivers assume the state with PIN (pin 12) low and PINB (pin 13) high.

The components C40, C35, C37 and the track from C37 to IC2 pin 11 transform the 50Ω input impedance to present the optimum noise match to the ML2751 RRFI input. The gain between pin 11 and RRFO (pin 5) is approx 20dB and care must be taken to avoid feedback between these two pins.

The power supply for the LNA is input to VCC, pin 15, and via an external inductor from the supply to RRFO, pin 5. The inductor forms part of a 2 pole bandpass filter together with C19, C18, L3 and C17. The filter is nominally centered on 915MHz with a -3dB bandwidth of 200MHz. The low Q removes any need for trimming or adjustment of the filter characteristic.

The filter is designed to present an impedance of 200Ω to the LNA output. The output is matched to 50Ω by C16 and the stray capacitance of the ML2722 input. Loss in the filter is less than 1.5dB. The Gain and NF from the input to the output of the filter are typically 17dB and 3.3dB respectively.

The 12.5% chip error rate sensitivity of the receiver is typically -105dBm at 1.536Mchips.

Current Consumption - typical

Mode	Icc
Standby - no clock	75µA
Standby - with clock	90µA
Receive	55mA
Transmit (+20dBm O/P)	180mA

DESIGN DESCRIPTION

DESIGN COST REDUCTION IDEAS

The design presented in this document already provides a low cost solution, but further savings may be made by adopting some of the ideas below which were not tested on this design. Some of the potential cost savings may be achieved by:

a) Replacement of the inductors in the harmonic filter (L1, L2, L5 and L6) with microstrip patterns. This will have the side effect of making the PA slightly less efficient as power will be wasted in the lower Q microstrip inductors.
b) Replacement of the inductors in the receive filter (L3, L4) with microstrip patterns. This will occupy more PCB real estate, but will have negligible effect on sensitivity (1dB extra loss will reduce sensitivity by less than 0.2dB).
c) Removal of decoupling capacitors C26, C27 and C46 in the PIN switch driver circuitry. Other decouplers might be surplus but performance will be layout dependent and would require thorough checking.

TYPICAL ALTERNATIVE CONFIGURATIONS

ML2722 STAND ALONE, LOW POWER CONFIGURATION

The typical ML2722 simplified evaluation schematic (See Figure 3) allows a functional evaluation of the ML2722. In Figure 4 the addition of an antenna switch and an antenna matching network (network not shown as it depends upon the specific antenna and board layout) completes the ML2722 RF section as a stand alone transceiver. The antenna switch function may be implemented with Pin Diode switches as in Figure 1 or with a industry standard integrated switch module.

ML2722 WITH CUSTOMER SUPPLIED LNA (LOW NOISE AMPLIFIER) AND PA (POWER AMPLIFIER)

Figure 1 uses a ML2722 and ML2751 in combination, as previously noted, (Page 3, “Transmit output, TRFO”) a three pole Butterworth filter is inserted between the ML2722 pin 23 and the ML2751 Pin 3. The combination of the filter and the input characteristics of the ML2751 are sufficient to protect the ML2722 output from second harmonic effects.

In the alternative configurations such as when the customer chooses to implement a different Power Amplifier the objective of isolating the ML2722 pin 23 from second harmonics generated by the external PA must be realized. Figure 5 is an example of the use of discrete amplifiers as the LNA and PA in place of the ML2751 shown in Figure 1. Note that in the case of Figure 5 an “ISOLATION MEANS” is included between the ML2722 Pin 23 and the Power Amplifier. For optimum performance we recommend that the second harmonic level from the output Power Amplifier reflected back into the ML2722 output pin 23 be less than –30 dBm. This can be accomplished by the “ISOLATION MEANS” that is one or a combination of the following; resistive termination or a network which looks to the part resistive, (such as the input to a laboratory grade test instrument) a filter, a pad or matching network or a buffered high input impedance power amplifier.

DESIGN DESCRIPTION

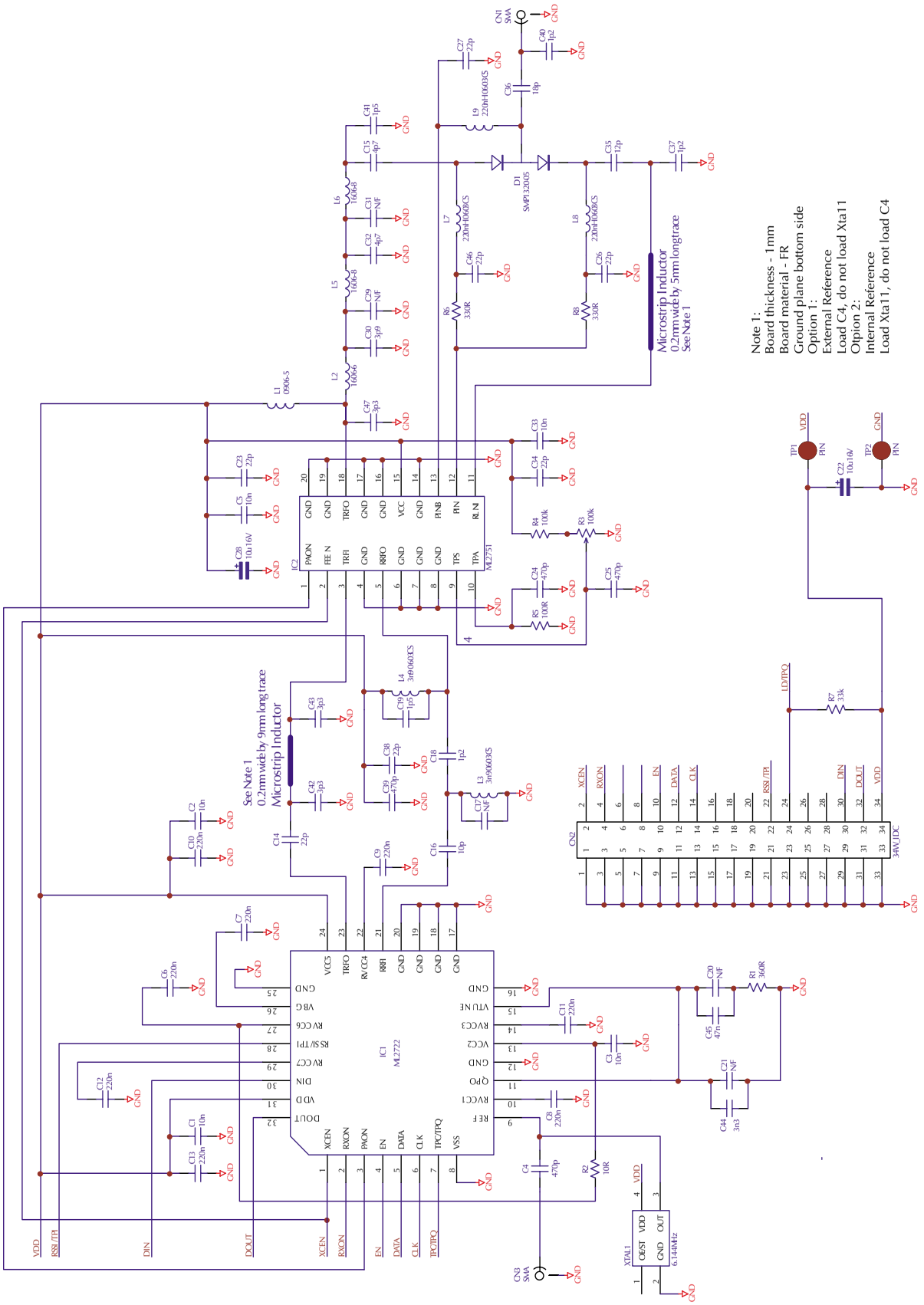

Figure 1. Design Evaluation Circuit Diagram

DESIGN DESCRIPTION

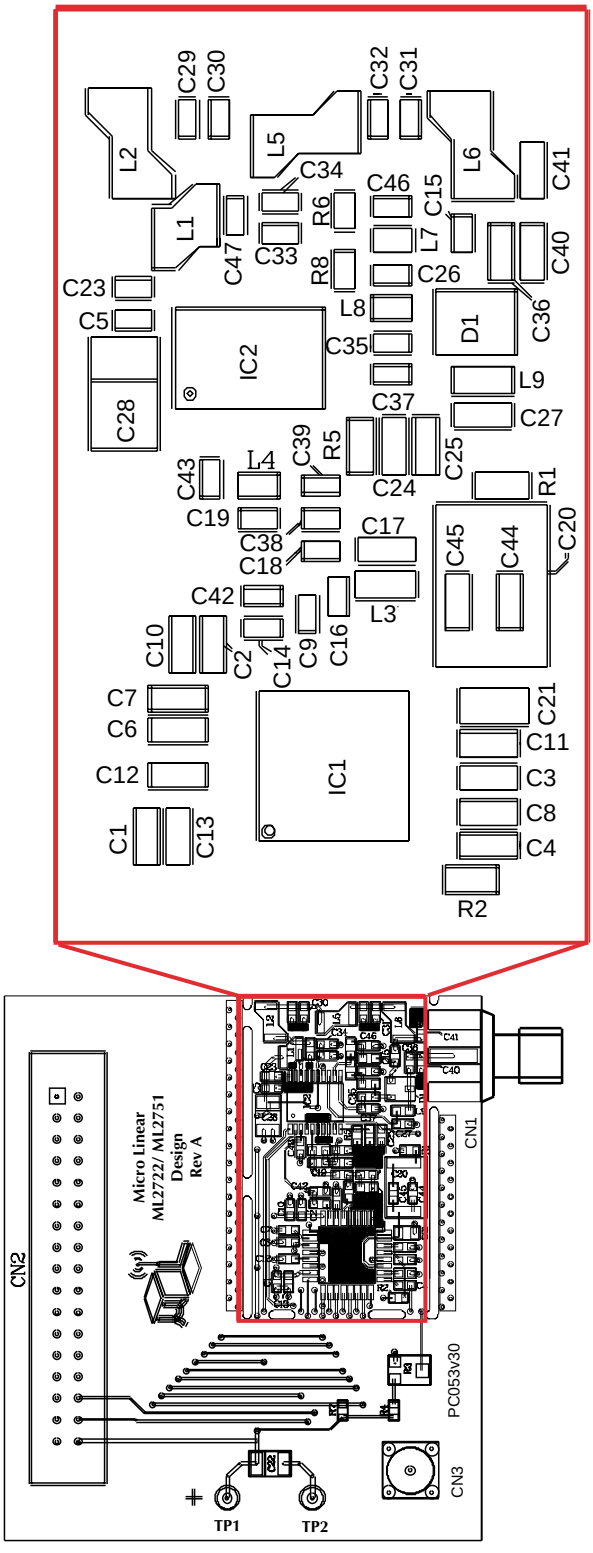

Figure 2. Evaluation PCB Layout

DESIGN DESCRIPTION

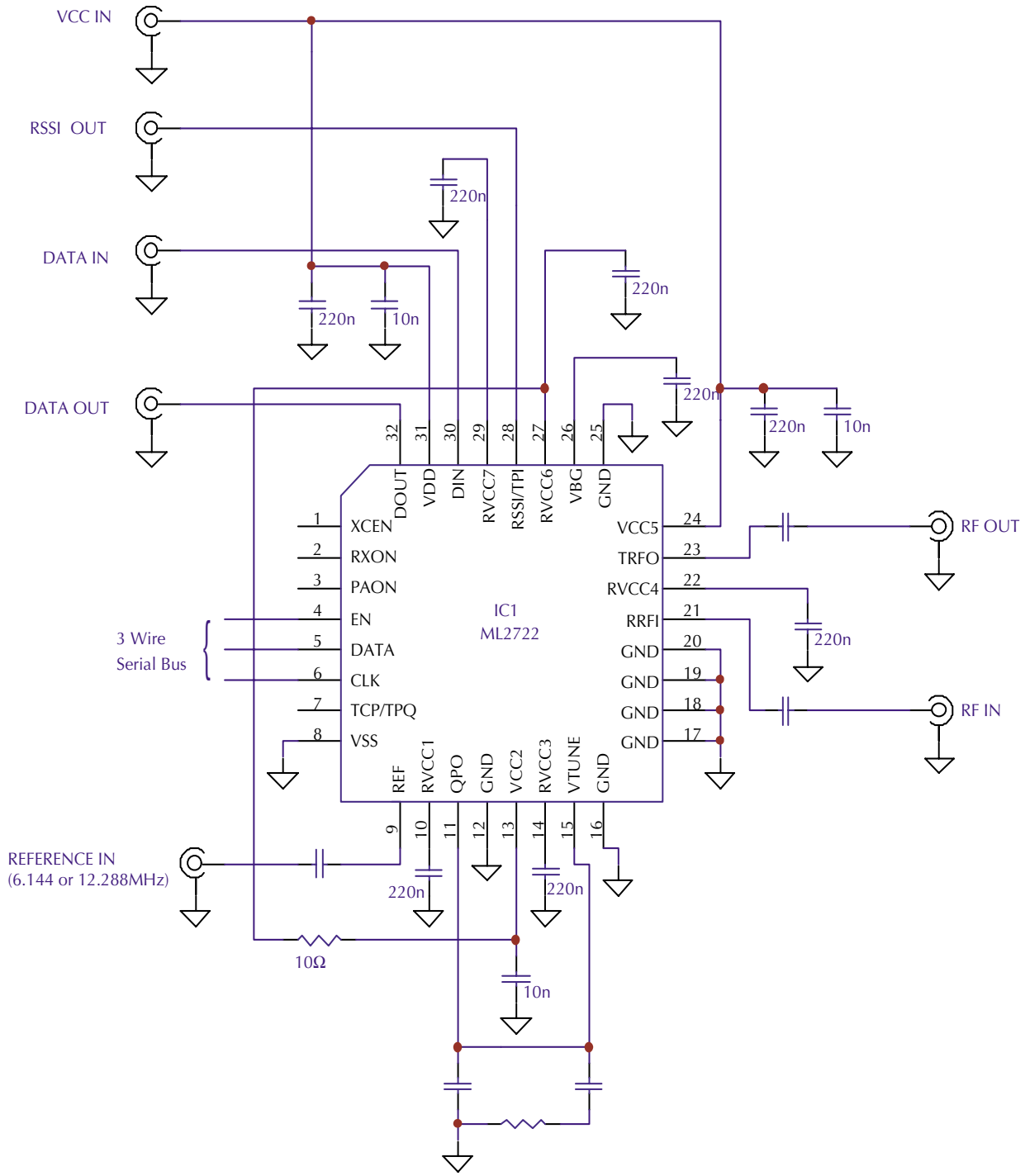

Figure 3. Typical Simplified ML2722 Evaluation Schematic

DESIGN DESCRIPTION

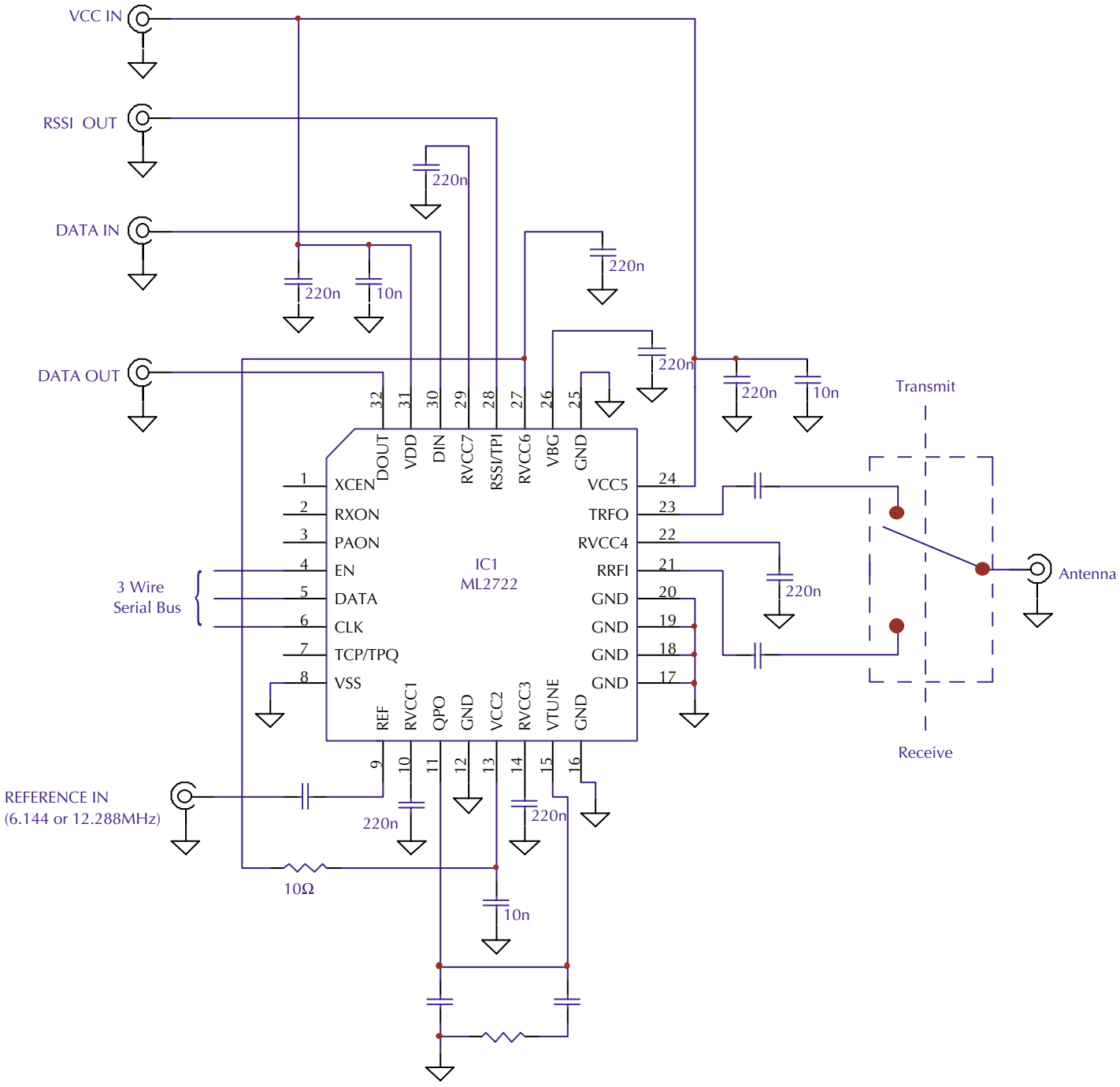

Figure 4. Typical ML2722 Evaluation Schematic For a Stand Alone Configuration

DESIGN DESCRIPTION

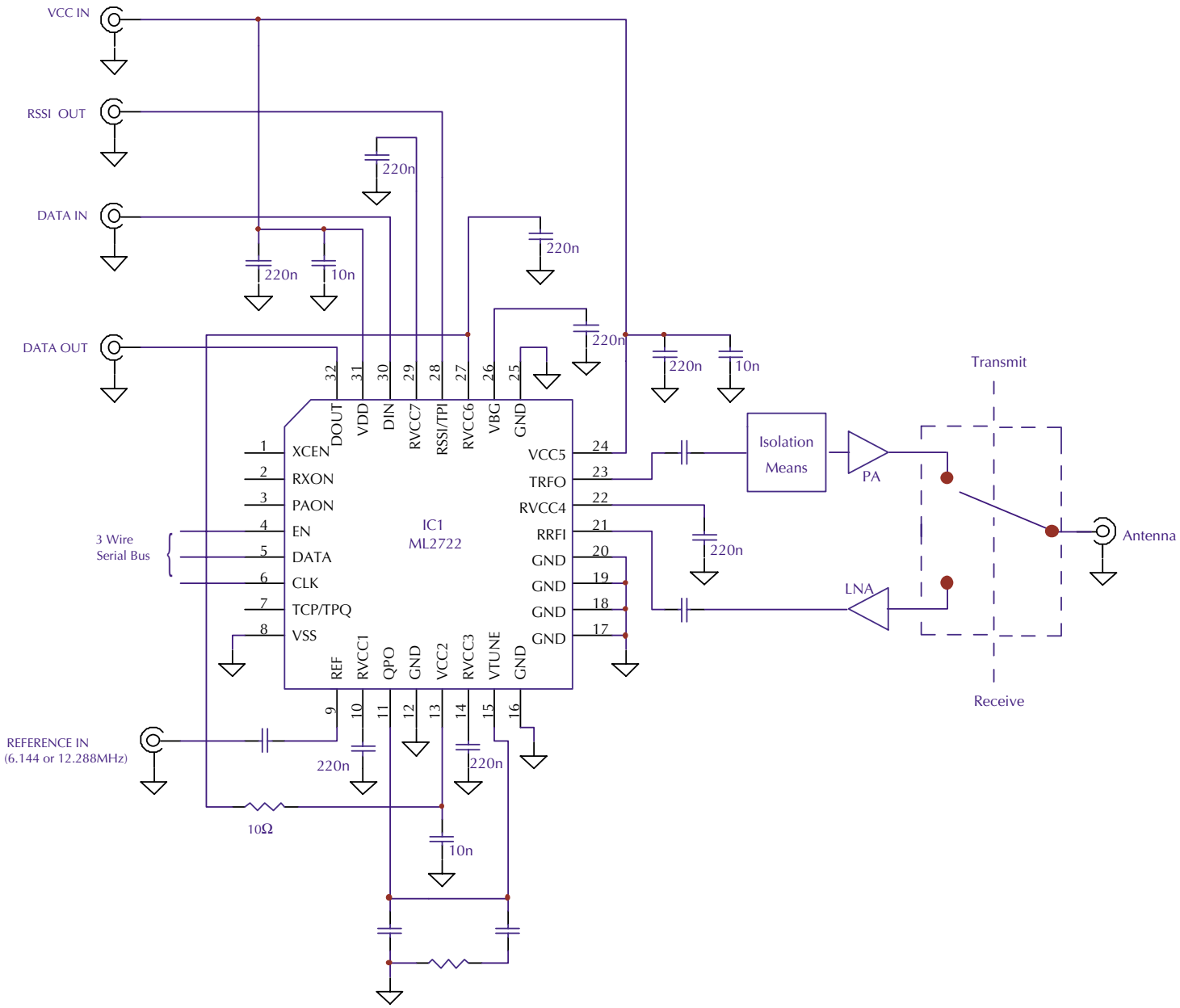

Figure 5. Typical ML2722 Evaluation Schematic Using External Amplifiers

APPENDIX A - BILL OF MATERIALS FOR FIGURE 1

Designator	Part Type	Footprint	Description	Manufacturer	Manufacturers Part Number
C1	10n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 X7R 103 K50
C2	10n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 X7R 103 K50
C3	10n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 X7R 103 K50
C4	470p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 471 J50
C5	10n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 X7R 103 K50
C6	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C7	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C8	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C9	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C10	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C11	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C12	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C13	220n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 Y5V 224 Z16
C14	22p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 220 J50
C15	4p7	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 4R7 C50
C16	10p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 100 C50
C17	N/F	CAP0603	Not Fitted		
C18	1p2	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 1R2 C50
C19	1p5	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 1R5 C50
C20	N/F	WIMA2220	Not Fitted		
C21	N/F	CAP0805	Not Fitted		
C22	10u 16V	TANTB	B Case Tantalum Capacitor	NEC	NRS106K16R8
C23	22p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 220 J50
C24	470p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 471 J50
C25	470p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 471 J50
C26	22p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 220 J50
C27	22p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 220 J50
C28	10u 16V	TANTB	B Case Tantalum Capacitor	NEC	NRS106K16R8
C29	N/F	CAP0603	Not Fitted		
C30	3p9	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 3R9 C50
C31	N/F	CAP0603	Not Fitted		
C32	4p7	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 4R7 C50
C33	10n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 X7R 103 K50
C34	22p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 220 J50
C35	12p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 120 C50
C36	18p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 180 J50
C37	1p2	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 1R2 C50
C38	22p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 220 J50
C39	470p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 471 J50
C40	1p2	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 1R2 C50

APPENDIX A - BILL OF MATERIALS

Designator	Part Type	Footprint	Description	Manufacturer	Manufacturers Part Number
C41	1p5	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 1R5 C50
C42	3p3	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 3R3 C50
C43	3p3	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 3R3 C50
C44	3n3	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 X7R 332 K50
C45	47n	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 X7R 473 K16
C46	22p	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 220 J50
C47	3p3	CAP0603	0603 Ceramic Capacitor	Murata	GRM39 C0G 3R3 C50
CN1	SMA	SMA_PCBEDGE	SMA PCB Edge Connector		
CN2	34W_IDC	34W_IDC	34 way IDC Receptacle		
CN3	SMA	SMA	SMA Vertical PCB Connector		
D1	SMP1320-011	SOT23	PIN Diode	Alpha Industries	SMP1320-05
IC1	ML2722-TQFP32	TQFP32	Transceiver IC	Micro Linear	ML2722
IC2	ML2751-TSSOP20	SSOP20	Front End IC	Micro Linear	ML2751
L1	0906-5	IND0906	Micro Spring Inductor	Coilcraft	0906-5
L2	1606-6	IND1606	Micro Spring Inductor	Coilcraft	1606-6
L3	3n9 0603CS	IND0603	Surface mount inductor	Coilcraft	0603CS-3N9XJBC
L4	3n9 0603CS	IND0603	Surface mount inductor	Coilcraft	0603CS-3N9XJBC
L5	1606-8	IND1606	Micro Spring Inductor	Coilcraft	1606-8
L6	1606-8	IND1606	Micro Spring Inductor	Coilcraft	1606-8
L7	220nH 0603CS	IND0603	Surface mount inductor	Coilcraft	0603CS-R22XJBC
L8	220nH 0603CS	IND0603	Surface mount inductor	Coilcraft	0603CS-R22XJBC
L9	220nH 0603CS	IND0603	Surface mount inductor	Coilcraft	0603CS-R22XJBC
R1	360R	RES0603	0603 Resistor	Neohm	CRG0603 1% 360R
R2	10R	RES0603	0603 Resistor	Rohm	MCR03 EZH J 100
R3	100k	3303W_TRIMMER	Variable Resistor	Bourns	3303W 100k
R4	100k	RES0603	0603 Resistor	Rohm	MCR03 EZP FX 1003
R5	100R	RES0603	0603 Resistor	Rohm	MCR03 EZP FX 1000
R6	330R	RES0603	0603 Resistor	Rohm	MCR03 EZP FX 3300
R7	33k	RES0603	0603 Resistor	Rohm	MCR03 EZP FX 3302
R8	330R	RES0603	0603 Resistor	Rohm	MCR03 EZP FX 3300
TP1	PIN	PIN	PCB PIN		
TP2	PIN	PIN	PCB Pin		
PCB	PC053V30				
OSC	Oscillator		6.144MHz Oscillator	Digi-Key	SG-636 PCE 6.144MC2

More capacitor information can be found at:
www.murata.com
www.panasonic.com
www.wima.de

PUBLICATION INFORMATION

PARTS	PUBLICATION	DATE	FILE
ML2722 ML2751	Application Note 78	January, 2001	AN78-01.pdf

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