PCB Layout Guidelines for Designing with Avago SFP+Transceivers

Application Note 5362

Introduction

Avago Technologies offers a broad portfolio of SFP+ solutions include SR, LR, and LRM variants operating up to 10.3125 Gb/s. As small form pluggable transceiver data rates move from 4Gb/s to 10 Gb/s, great care must be taken when designing the SFP+ / host board high speed interface to minimize impedance discontinuities which can negatively impact signal integrity. Areas to pay particular attention to are:

1. Dielectric properties of the PCB material
2. High speed trace geometry (stripline or microstrip)
3. Physical configuration of vias
4. Discontinuities caused by AC coupling components and connector

This application note describes a series of layout options the host PCB designer can implement to optimize the signal integrity of the SFP+ high speed data path.

Typical SFP+ High Speed Electrical Channel

The following diagram illustrates the basic components of a typical SFP+ high speed electrical channel:

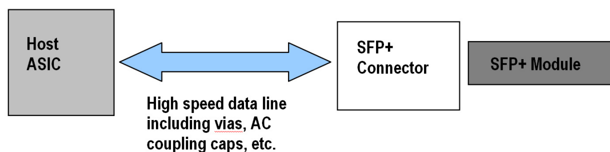
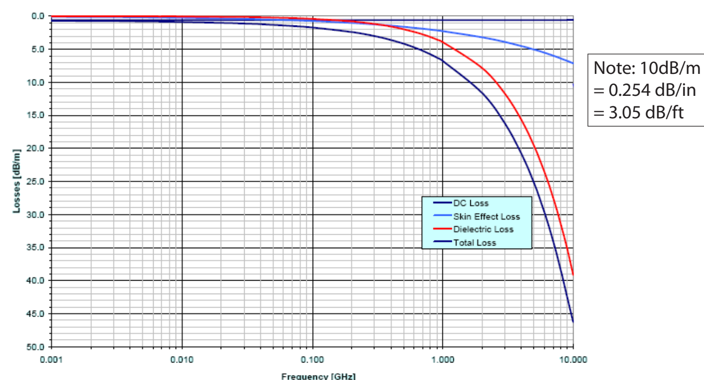


Figure 1. SFP+ High Speed Electrical Channel

Host PCB Dielectric Properties

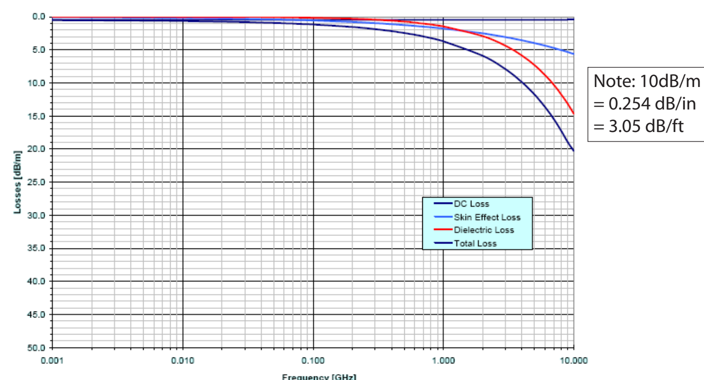
The differential input and output impedance of the SFP+ module is designed to have a nominal value of 100 ohms The high speed data lines interfacing the SFP+ connector to the host ASIC should also be designed to provide a low loss, 100 ohm differential path with a minimum of impedance discontinuities. PCB dielectric material choice and high speed trace geometry play an integral part in determining the overall signal integrity of the channel.

The most common choice of PCB dielectric material today is FR4. Typical FR4 material has a dielectric constant of 4.2 (@ 5GHz) and a loss tangent of approximately 0.02 (worst case). If the host ASIC proves to be especially sensitive to vertical eye closure and timing jitter, the designer may choose to employ a higher performance material if there is a need for longer (greater than 6 to 8 inches) track lengths. Nelco 4000-13 is one such material with a dielectric constant of approximately 3.7 (@ 2.5GHz) and loss tangent of 0.014. The following tables illustrate the loss properties of FR4 and Nelco 4000-13.



DC Loss = Skin Effect Loss @ 70.65 MHz, Skin Loss = Dielectic Loss @ 330.56 MHz
Differential FR-4 PCB: DC, Cu Skin Effect, Dielectic and Total Loss Vs. Freqency
(Trace Impedance = 100 ohms, Avg. trace width ~ 6.2mils [0.158mm], 0.5 oz Copper)

Figure 2. FR-4 Insertion Loss vs. Frequency



DC Loss = Skin Effect Loss @ 66.6 MHz, Skin Loss = Dielectic Loss @ 1474 MHz
Differential Nelco-4000-13SI PCB: DC, Cu Skin Effect, Dielectic and Total Loss Vs. Freqency
(Trace Impedance = 100 ohms, Avg. trace width ~ 8.1mils [0.205mm], 0.5 oz Copper)

Figure 3. Nelco-4000 Insertion Loss vs. Frequency

High Speed Trace Geometry

In terms of high speed trace geometry, the designer may choose to implement either a stripline or microstrip based design. Each design has its advantages and disadvantages. The buried stripline typically exhibits lower EMI surface emission and tends to show better EMI immunity versus the microstrip. On the other hand, the buried stripline requires the use of vias which can lead to reduced signal integrity (higher jitter, vertical eye closure) due to impedance discontinuities. The following table (from SFF-8431, table2) illustrates how far a typical high speed trace can extend for a specified material design and geometry.

Via Configuration

In the event that the design necessitates the use of striplines, the number of vias in the high speed path should be kept to an absolute minimum. If possible, newer via technologies should be employed (blind vias, micro vias, etc.) to minimize via inductance and stub effects. Should standard through-hole vias be needed, then the signal lines should be routed from layer to layer using the maximum via length to reduce via stub size.

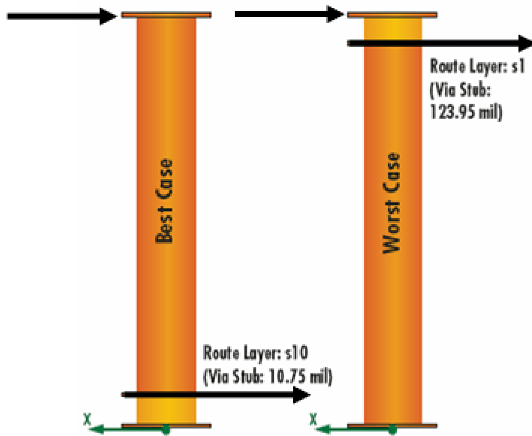


Figure 4. Routing Top Layer to Layer 10 vs. Top Layer to Layer 1

In addition to minimizing via stub length, ground vias should be placed next to each signal via of the differential pair to form a G-S-S-G configuration. The exact spacing of the ground and signal vias will be design dependent and should be confirmed through 3-D electromagnetic simulation. As a rule of thumb, the ground via to signal via separation (p) should be at least as great as the signal to signal via separation.

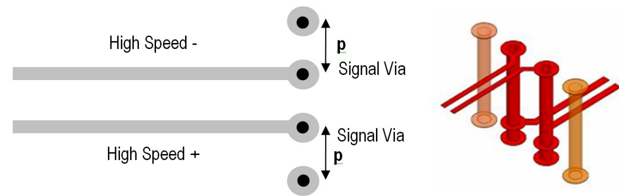


Figure 5. G-S-S-G Configuration

Since the signal vias will be traversing any number of power and ground planes, care must be taken to provide a gap between the via pad and the power / ground plane to reduce excess capacitance. This gap is sometimes referred to as an anti-pad. Again, the exact width of the gap should be determined through 3-D electromagnetic simulation.

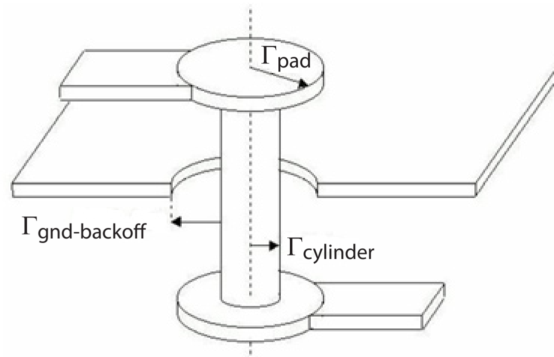


Figure 6. Signal Via to Gnd/Pwr Plane Gap

Table 1. Trace Length vs. Design

Type	Material	Trace Width (mm)	Loss Tangent	Copper Thickness (oz) [1]	Copper Thickness (mm)	Trace Length (mm)
Microstrip	FR4-6/8	0.3	0.022	1	35	200
	Nelco 4000-13	0.3	0.016	1	17.5	300
Stripline	FR4-6/8	0.125	0.022	0.5	17.5	150
	Nelco 4000-13	0.125	0.016	0.5	35	200

Notes:

1. Copper (oz) is defined as an ounce of copper rolled over one square foot of laminate.

Discontinuities Caused by AC Coupling Components and Connector

Anti-pads should be employed beneath any AC coupling components located in the high speed data path. As a rule of thumb, the size of the anti-pad should be at least as large as the outline of the component PCB footprint. In the diagram below, lap and wap are the length and width of the ground plane cut out beneath the components.

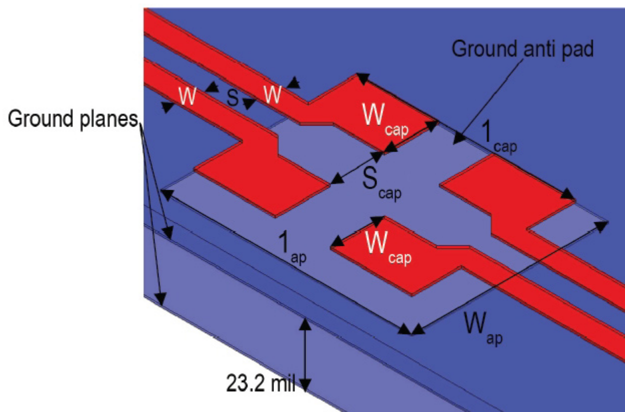


Figure 7. Component Anti-pad Geometry

As a pluggable device, the SFP+ module interfaces to a host board through an edge type 20 position PCB connector. When choosing a connector, the designer should opt for one which has been specifically optimized for operation at 10 Gb/s. Tyco part number 1888247-1 and Molex part number 74441-0010 are two possible options. In general, the surface mount variant of a connector should be selected over the pin-through-hole version as through-hole connections increase the risk of creating stub discontinuities.

Figure 9 gives an example of how to route the high speed TX and RX lines to the SFP+ edge connector footprint through microstrip transmission lines. This design is implemented in the Avago Technologies SFP+ evaluation kit (part number AFCT-5016Z) which can be ordered separately. The PCB board stack up for this particular high speed trace geometry is as follows.

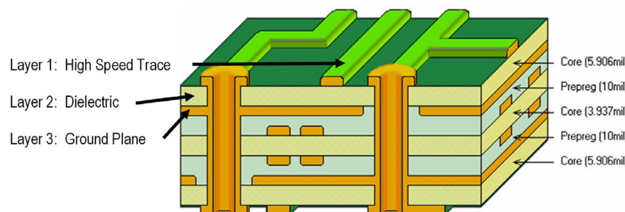


Figure 8. Example PCB Layer Stackup

In order to minimize the impedance discontinuity at the transmission line / connector interface, anti-pads should be employed under the SFP+ connector pads and should be placed (if possible) on all metal layers below the pads. In this case, one large anti-pad for each pair of data lines placed on the ground and power layers below the signal layer.

High Speed Trace Width=0.28mm

High Speed Trace Separation=0.525mm

Dielectric Thickness=150um

Approximate Anti-pad Dimensions=3.2mm x 1.9mm

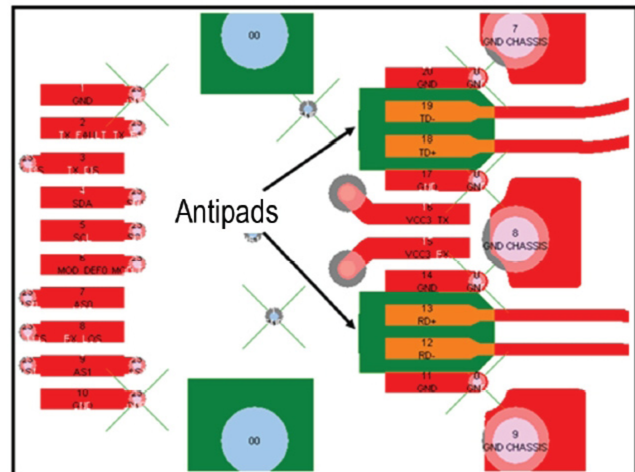


Figure 9. SFP+ Connector Footprint with Anti-pads

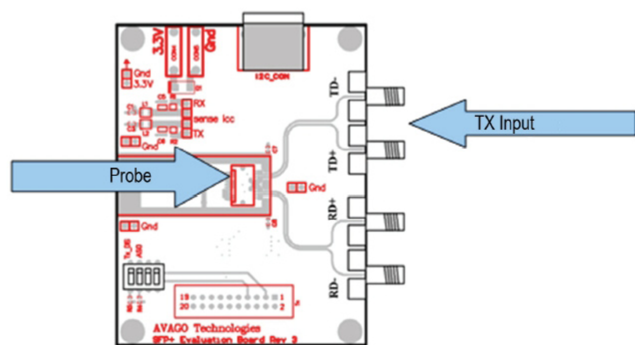
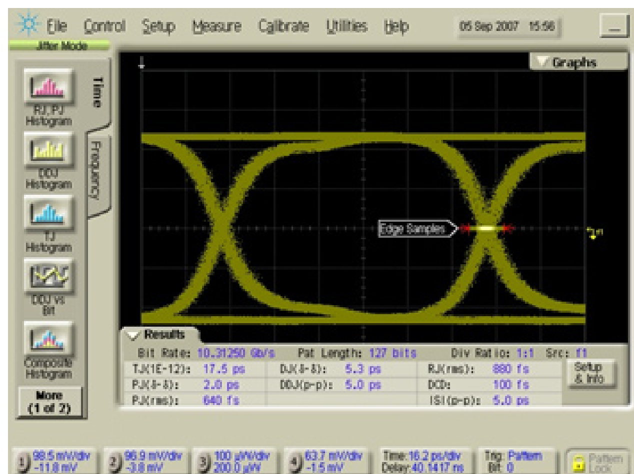
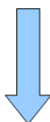


Figure 10. SFP+ Evaluation Board

The following eye diagrams were obtained by applying a 10.3125 Gb/s PRBS7 signal to the TX input channel of the Avago Technologies SFP+ evaluation board, and probing the channel after the SFP+ edge connector with a Spirent Communications SFF-8431 Host System Compliance test board (PN 40-001663). Much of the measured increase in timing jitter can be attributed to a bandwidth limitation associated with the SFP+ edge connector.

TX Input





Probe Signal

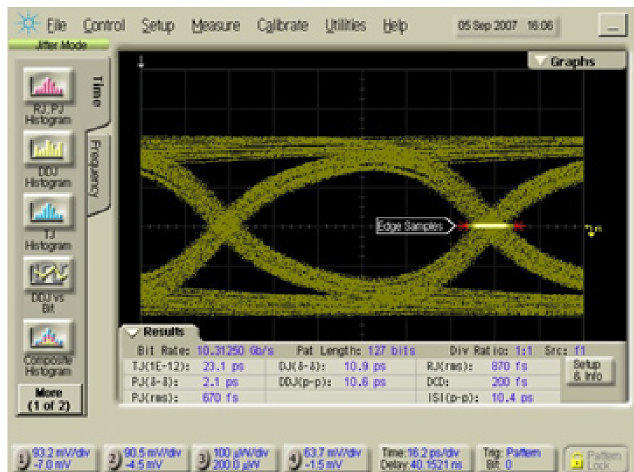


Figure 11. TX Input Signal and Resulting Probe Signal

Related Materials

For designers wishing to develop simulation models of the high speed SFP+ channel, HSPICE models of Avago Technologies receiver output and transmitter input are available upon request. For further information please visit www.avagotech.com. To order Avago Technologies SFP+ evaluation board or SFP+ samples, contact support @avagotech.com.

References

1. [Bowers 2003] Steve Bowers, Dr. Herbert Lage, “Considerations for High Speed PCB Track Design in 10Gb/s Serial Data Transmission”, www.agilent.com
2. [Aeluros] Aeluros, “Application Note: Puma AEL1001 Optical Module Board Design Considerations”, www.aeluros.com
3. [Sayer 2005] Dr. Edward P. Sayer, “Design of Multi-Gigabit ATCA Backplanes and Logic Card Interfaces”, ATCA Summit Presentation

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