Introduction

Avago Technologies offers a broad portfolio of SFP+ solutions including SR, LR, and LRM variants operating up to 10.3125 Gb/s. As small form pluggable transceiver data rates move from 4Gb/s to 10 Gb/s, great care must be taken when designing the SFP+ / host board high speed interface to minimize impedance discontinuities which can negatively impact signal integrity. Areas to pay particular attention to are:

1. Dielectric properties of the PCB material
2. High speed trace geometry (stripline or microstrip)
3. Physical configuration of vias
4. Discontinuities caused by AC coupling components and connector

This application note describes a series of layout options the host PCB designer can implement to optimize the signal integrity of the SFP+ high speed data path.

Typical SFP+ High Speed Electrical Channel

The following diagram illustrates the basic components of a typical SFP+ high speed electrical channel:

![SFP+ High Speed Electrical Channel Diagram](image)

Figure 1. SFP+ High Speed Electrical Channel

Host PCB Dielectric Properties

The most common choice of PCB dielectric material today is FR4. Typical FR4 material has a dielectric constant of 4.2 (@ 5GHz) and a loss tangent of approximately 0.02 (worst case). If the host ASIC proves to be especially sensitive to vertical eye closure and timing jitter, the designer may choose to employ a higher performance material if there is a need for longer (greater than 6 to 8 inches) track lengths. Nelco 4000-13 is one such material with a dielectric constant of approximately 3.7 (@ 2.5GHz) and loss tangent of 0.014. The following tables illustrate the loss properties of FR4 and Nelco 4000-13.

![FR-4 Insertion Loss vs. Frequency](image)

![Nelco-4000 Insertion Loss vs. Frequency](image)

DC Loss = Skin Effect Loss @ 70.65 MHz, Skin Loss = Dielectric Loss @ 330.56 MHz
Differential FR-4 PCB: DC, Cu Skin Effect, Dielectric and Total Loss Vs. Frequency
(Trace Impedance = 100 ohms, Avg. trace width ~ 6.2mils [0.158mm], 0.5 oz Copper)

Note: 10dB/m = 0.254 dB/in = 3.05 dB/ft

DC Loss = Skin Effect Loss @ 66.6 MHz, Skin Loss = Dielectric Loss @ 1474 MHz
Differential Nelco-4000-13 PCB: DC, Cu Skin Effect, Dielectric and Total Loss Vs. Frequency
(Trace Impedance = 100 ohms, Avg. trace width ~ 8.1mils [0.205mm], 0.5 oz Copper)

Note: 10dB/m = 0.254 dB/in = 3.05 dB/ft

Figure 2. FR-4 Insertion Loss vs. Frequency

Figure 3. Nelco-4000 Insertion Loss vs. Frequency
High Speed Trace Geometry

In terms of high speed trace geometry, the designer may choose to implement either a stripline or microstrip based design. Each design has its advantages and disadvantages. The buried stripline typically exhibits lower EMI surface emission and tends to show better EMI immunity versus the microstrip. On the other hand, the buried stripline requires the use of vias which can lead to reduced signal integrity (higher jitter, vertical eye closure) due to impedance discontinuities. The following table (from SFF-8431, table2) illustrates how far a typical high speed trace can extend for a specified material design and geometry.

Via Configuration

In the event that the design necessitates the use of striplines, the number of vias in the high speed path should be kept to an absolute minimum. If possible, newer via technologies should be employed (blind vias, micro vias, etc.) to minimize via inductance and stub effects. Should standard through-hole vias be needed, then the signal lines should be routed from layer to layer using the maximum via length to reduce via stub size.

Table 1. Trace Length vs. Design

<table>
<thead>
<tr>
<th>Type</th>
<th>Material</th>
<th>Trace Width (mm)</th>
<th>Loss Tangent</th>
<th>Copper Thickness (oz) [1]</th>
<th>Copper Thickness (mm)</th>
<th>Trace Length (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microstrip</td>
<td>FR4-6/8</td>
<td>0.3</td>
<td>0.022</td>
<td>1</td>
<td>35</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td>Nelco 4000-13</td>
<td>0.3</td>
<td>0.016</td>
<td>1</td>
<td>17.5</td>
<td>300</td>
</tr>
<tr>
<td>Stripline</td>
<td>FR4-6/8</td>
<td>0.125</td>
<td>0.022</td>
<td>0.5</td>
<td>17.5</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td>Nelco 4000-13</td>
<td>0.125</td>
<td>0.016</td>
<td>0.5</td>
<td>35</td>
<td>200</td>
</tr>
</tbody>
</table>

Notes:
1. Copper (oz) is defined as an ounce of copper rolled over one square foot of laminate.
Discontinuities Caused by AC Coupling Components and Connector

Anti-pads should be employed beneath any AC coupling components located in the high speed data path. As a rule of thumb, the size of the anti-pad should be at least as large as the outline of the component PCB footprint. In the diagram below, lap and wap are the length and width of the ground plane cut out beneath the components.

In order to minimize the impedance discontinuity at the transmission line / connector interface, anti-pads should be employed under the SFP+ connector pads and should be placed (if possible) on all metal layers below the pads. In this case, one large anti-pad for each pair of data lines placed on the ground and power layers below the signal layer.

- High Speed Trace Width=0.28mm
- High Speed Trace Separation=0.525mm
- Dielectric Thickness=150um
- Approximate Anti-pad Dimensions=3.2mm x 1.9mm

Figure 7. Component Anti-pad Geometry

As a pluggable device, the SFP+ module interfaces to a host board through an edge type 20 position PCB connector. When choosing a connector, the designer should opt for one which has been specifically optimized for operation at 10 Gb/s. Tyco part number 1888247-1 and Molex part number 74441-0010 are two possible options. In general, the surface mount variant of a connector should be selected over the pin-through-hole version as through-hole connections increase the risk of creating stub discontinuities.

Figure 9 gives an example of how to route the high speed TX and RX lines to the SFP+ edge connector footprint through microstrip transmission lines. This design is implemented in the Avago Technologies SFP+ evaluation kit (part number AFCT-5016Z) which can be ordered separately. The PCB board stack up for this particular high speed trace geometry is as follows.

Figure 8. Example PCB Layer Stackup

Figure 9. SFP+ Connector Footprint with Anti-pads

Figure 10. SFP+ Evaluation Board
The following eye diagrams were obtained by applying a 10.3125 Gb/s PRBS7 signal to the TX input channel of the Avago Technologies SFP+ evaluation board, and probing the channel after the SFP+ edge connector with a Spirent Communications SFF-8431 Host System Compliance test board (PN 40-001663). Much of the measured increase in timing jitter can be attributed to a bandwidth limitation associated with the SFP+ edge connector.

**Related Materials**

For designers wishing to develop simulation models of the high speed SFP+ channel, HSPICE models of Avago Technologies receiver output and transmitter input are available upon request. For further information please visit www.avagotech.com. To order Avago Technologies SFP+ evaluation board or SFP+ samples, contact support @avagotech.com.

**References**


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**Figure 11. TX Input Signal and Resulting Probe Signal**

For product information and a complete list of distributors, please go to our web site:  [www.avagotech.com](http://www.avagotech.com)

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