Temperature compensation by indirect method

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Keywords

- *Temperature compensation*
- *Frequency error*
- *Crystal oscillators*
- *Initial crystal tolerance*
- *Crystal temperature drift*
- *Crystal aging*
- *Crystal loading*
- *Narrowband systems*
- *EN 300 220*
- *ARIB STD T-67*

Introduction

A Phase Locked Loop (PLL) is used to generate the RF frequency in all Chipcon RF transceivers and transmitters. The PLL reference frequency is derived from a crystal. If the crystal frequency is incorrect, the RF frequency will also be incorrect. Due to the frequency multiplication in the PLL, the crystal frequency error will be multiplied and can degrade the performance of the RF link and/or cause a radio regulation violation.

According to the European regulations (EN 300 220) the frequency error, for a 25 kHz channel spacing, shall not exceed ±2.0 kHz in the 433 MHz frequency band or ±2.5 kHz in the 868 MHz frequency band for mobile and fixed (base) stations. For portable stations the frequency error, for a 25 kHz channel spacing, shall not exceed ±2.5 kHz in the 433 MHz frequency band or ±3.0 kHz in the 868 MHz frequency band [1].

According to the Japanese ARIB STD T-67 standard the frequency error shall be less than ±4 ppm (parts per million) [2].

For a transceiver to comply with the EN 300 220 narrowband and ARIB STD T-67 frequency accuracy requirements the system needs either

1) a very accurate (and expensive) crystal or
2) a cheaper crystal and compensation for the crystal frequency error both in production and in the field.

A unique feature in all Chipcon RF transceivers and transmitters is the very fine frequency resolution, which can be used for temperature compensation of the crystal if its temperature drift curve is known and a temperature sensor is included in the system. Even initial adjustment can be performed using the frequency programmability. This eliminates the need for an expensive TCXO and trimming in some applications. This application note describes how to perform crystal error compensation by re-programming the PLL. The main focus is on temperature compensation, but compensation of initial crystal tolerance and crystal loading is also discussed. The discussion and measurements in this application note is based on the ***CC1020*** transceiver.

Chipcon is a supplier of RFICs for all kinds of short range communication devices. Chipcon has a world-wide distribution network.

Sources of crystal frequency error

Initial crystal tolerance
Initial crystal tolerance is the frequency error at a given temperature, usually room temperature (25^{o}C) and can be minimized in production by trimming using a variable capacitor. This can be a time consuming as well as an expensive process. A different approach is to utilize the very fine frequency resolution of all Chipcon RF transceivers and transmitters. Re-programming the PLL to account for the initial crystal tolerance does not require manual labour or tuning elements and is thus a cheaper and less time consuming method.

Crystal loading
The crystal loading is realised by two capacitors, one from each crystal terminal to ground. Using the wrong crystal loading will result in a frequency error. The crystal loading error is compensated for similar to the initial tolerance error.

Aging
Aging is a frequency error mainly caused by stresses in the crystal package. The frequency error will typically decrease exponentially with time, so aging is typically only a problem during the first year - unless the crystal is pre-aged to remove most of the aging. A typical specification is ±3-5 ppm/year for the first year and half of this the next year and so on. It is impossible to compensate for aging, because it is hard to say which way the crystal will drift. Pre-aged crystals with a total ±2 ppm frequency error over time are available at relatively low cost.

Temperature drift
The crystal frequency will change with temperature and the amount of change depends on the crystal used. Temperature compensated crystal oscillators (TCXO) with excellent performance can be bought, but the price in small to medium quantities is normally comparable to that of the RF transceiver chip. The current consumption of a TCXO is also significantly larger than for the crystal oscillator integrated within the Chipcon RF transceivers and transmitters.

If the temperature drift of a standard crystal can be predicted, a (fairly) low cost and simple alternative can be implemented by re-programming the PLL to compensate for the predicted frequency error. The crystal error can be characterized by a 3rd-order polynomial equation, and there are manufacturers (e.g. Nihon Dempa Kogyo (NDK), HongKongCrystal) that provide the temperature coefficients as a bar code on top of the crystal housing. The temperature drift frequency error (in ppm) at temperature *T* is expressed by the following equation:

$$T_{error}(T) = A \cdot T^3 + B \cdot T^2 + C \cdot T \ + D \tag{1}$$

where *T* is the temperature in degree Celsius and *A*, *B*, *C* and *D* are the temperature coefficients provided by the crystal manufacturer. Figure 1 shows the temperature drift frequency error for 14 different crystals [5].

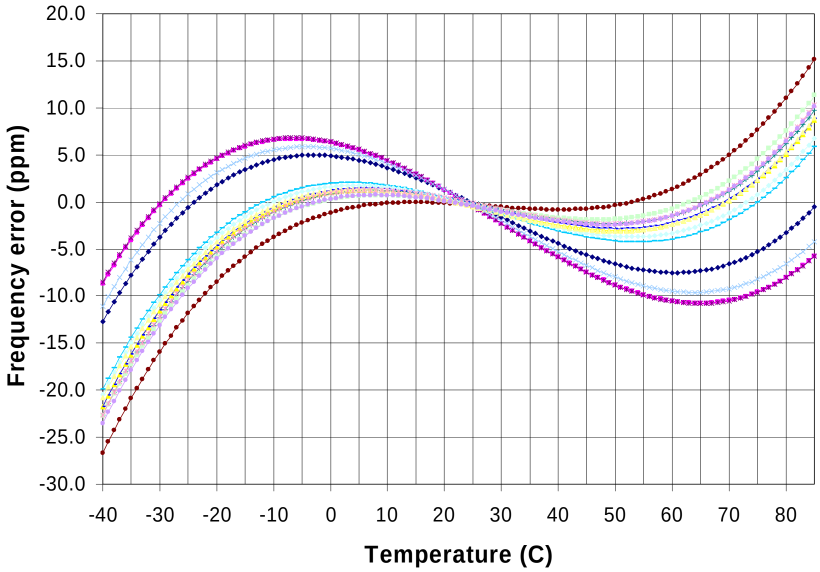

Figure 1. Typical temperature drift error [5]

Frequency error requirements

The European regulation EN 300 220 frequency accuracy requirement for mobile and fixed stations of ±2.0 kHz in the 433 MHz band corresponds to a relative accuracy of ±4.6 ppm, while ±2.5 kHz in the 868 MHz band corresponds to a relative accuracy of ±2.9 ppm. The frequency accuracy requirement for portable stations of ±2.5 kHz in the 433 MHz band corresponds to a relative accuracy of ±5.8 ppm, while ±3.0 kHz in the 868 MHz band corresponds to a relative accuracy of ±3.4 ppm. A device must meet the requirements over a temperature range from –10°C to +55°C. The device manufacturer may specify a wider temperature range than this [1].

In the Japanese ARIB T-67 standard the frequency error shall be less than ±4 ppm [2].

The total frequency error budget is therefore quite small and must account for frequency errors due to temperature drift, initial crystal tolerance, crystal loading and aging.

The CC1020 has very fine frequency resolution and the VCO output frequency can be set in steps of [3]:

$$Step\_size = \frac{f_{xosc}}{(REF\_DIV + 1)} \cdot \frac{1}{16384} \cdot \frac{1}{N} \qquad (2)$$

where

f_{xosc} is the nominal crystal oscillator frequency
REF_DIV is an integer between 1 and 7
N=1 in the 804 – 960 MHz frequency band
N=2 in the 402 – 480 MHz frequency band

For CC1020, f_{xosc} is typically 14.7456 MHz and REF_DIV is typically 1. The step size is therefore typically 225 Hz in the 402 – 480 MHz frequency band and 450 Hz in the 804 – 960 MHz frequency band. The step size can also expressed in ppm relative to the RF frequency. The step size is 0.53 ppm at 426 MHz and 0.52 ppm at 868 MHz. Thus, the initial crystal tolerance and crystal loading frequency errors can be compensated for to within ±0.27 ppm at 426 MHz and to within ±0.26 ppm at 868 MHz.

Table 1 summarizes the maximum frequency error as specified by the EN 300 220 and ARIB STD T-67 standards.

Standard	ARIB T-67	EN 300 220[1]	EN 300 220[2]	EN 300 220[1]	EN 300 220[2]
Frequency (MHz)	426	433	433	868	868
Temperature range (^{o}C)	-40 to +85	-10 to +55	-10 to +55	-10 to +55	-10 to +55
Requirement total frequency error (ppm)	±4	±4.6	±5.8	±2.9	±3.4
Requirement total frequency error (kHz)	±1.7	±2.0	±2.5	±2.5	±3.0

Note: [1] mobile and fixed stations, [2] portable stations

Table 1. Maximum frequency error

Correction factors and temperature drift correction factor look-up table

Appendix A provides the procedure and equations necessary to determine the correction factors to compensate for initial crystal tolerance, crystal loading and crystal oscillator temperature drift errors.

Compensation of the initial crystal tolerance and crystal loading errors is performed during production. The actual RF output frequency is measured and compared with the programmed RF frequency. The correction factor is calculated and re-programming of the PLL compensates for the frequency error.

The crystal frequency will drift with temperature and it is therefore necessary to generate a look-up table during production with correction factors for different temperatures. The look-up table is calculated from the crystal temperature coefficients supplied by the crystal manufacturer and must be stored in non-volatile memory. Each crystal needs a separate look-up table as the crystal temperature coefficients varies from crystal to crystal (see Figure 1). Compensation of the temperature error needs to be done during actual use.

Assume the crystal frequency is 14.7456 MHz and REF_DIV is maximum 2. If the maximum initial crystal tolerance and crystal loading error is ±40 ppm it can be shown that the maximum correction factor is ±127 decimal (i.e. 8 bits). Similarly, if the maximum temperature error is ±40 ppm it can be shown that the maximum temperature error correction factor is ±127 decimal (i.e. 8 bits). For best accuracy the look-up table shall have entries for temperatures in the range –40^{o}C to +85^{o}C in steps of 1^{o}C. That is, 126 entries of 1 byte each ranging from *FREQ_ERR1(-40)* to *FREQ_ERR1(85)*. Note that crystal errors larger than ±40 ppm do not exceed the PLL's ability to perform the correction. The limit is set to ±40 ppm merely to save memory space.

Temperature sensor

There are many different kinds of temperature sensor available. Some sensors have a digital output, which may be connected directly to a microcontroller, others have analogue outputs and should be connected to an ADC. The sensor should be mounted as close to the crystal as physically possible, preferably in thermal contact with the crystal case.

The accuracy of the temperature drift error compensation is determined by the accuracy of the predicted crystal temperature drift curve and the accuracy of the temperature sensor.

Measurement results

Figure 2 shows the measurement setup.

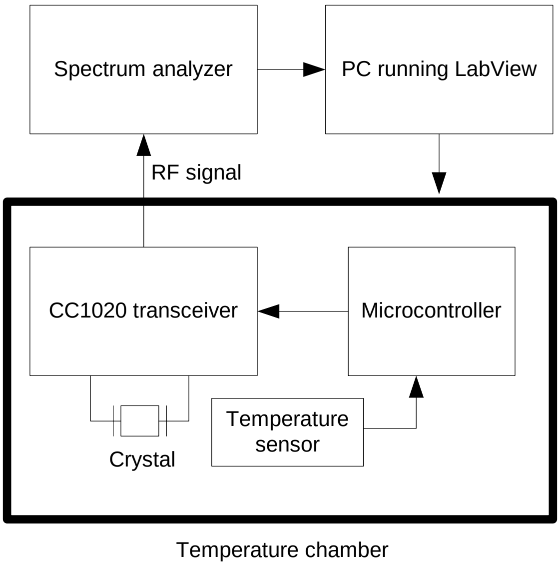

Figure 2. Measurement setup

- The temperature sensor used was Microchip TC1046 [4]
- A source code based on the procedure and equations in appendix A was written for an AVR ATMega8L microcontroller
- The temperature chamber and spectrum analyser were controlled by LabView through a GPIB bus
- The initial crystal tolerance and crystal loading error compensation was performed at 25^{o}C (i.e. $T_{error}(T_0) = T_{error}(25^oC)$ in equation 10a)
- The CC1020 VCO was calibrated at –40^{o}C, -10^{o}C, +25^{o}C, +50^{o}C and +80^{o}C

Figure 3 shows the predicted temperature error from –40°C to +85°C of two 5 x 3.2 mm SMD crystals from HongKongCrystal [5]. Figure 4 shows the total error after compensating for initial crystal tolerance, crystal loading and temperature drift errors.

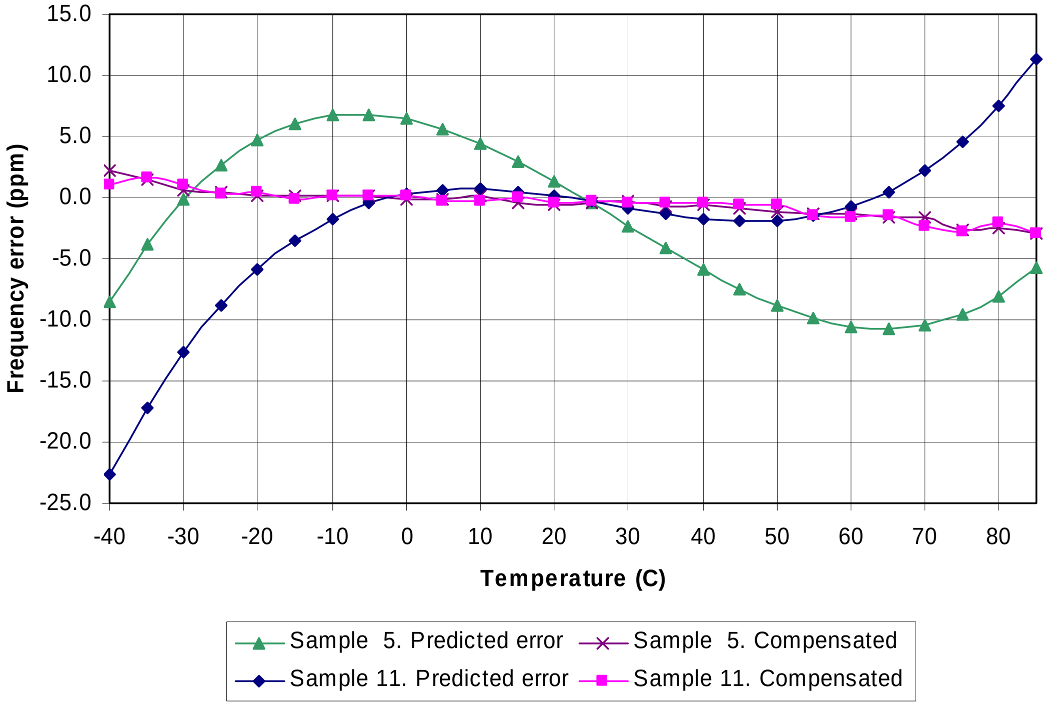

Figure 3. Predicted and compensated error. HongKongCrystal

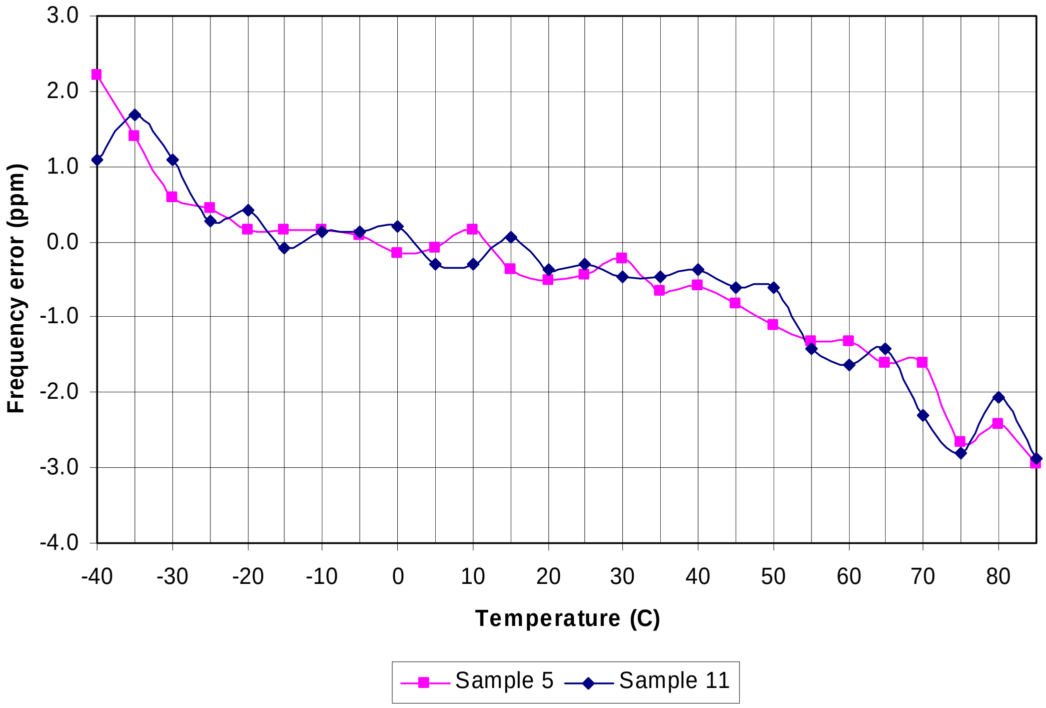

Figure 4. Frequency error after compensation. HongKongCrystal

Figure 5 shows the predicted temperature error from –40°C to +85°C of a NX5032SA (W-191-520) crystal from NDK [6]. Figure 6 shows the total error after compensating for initial crystal tolerance, crystal loading and temperature drift errors.

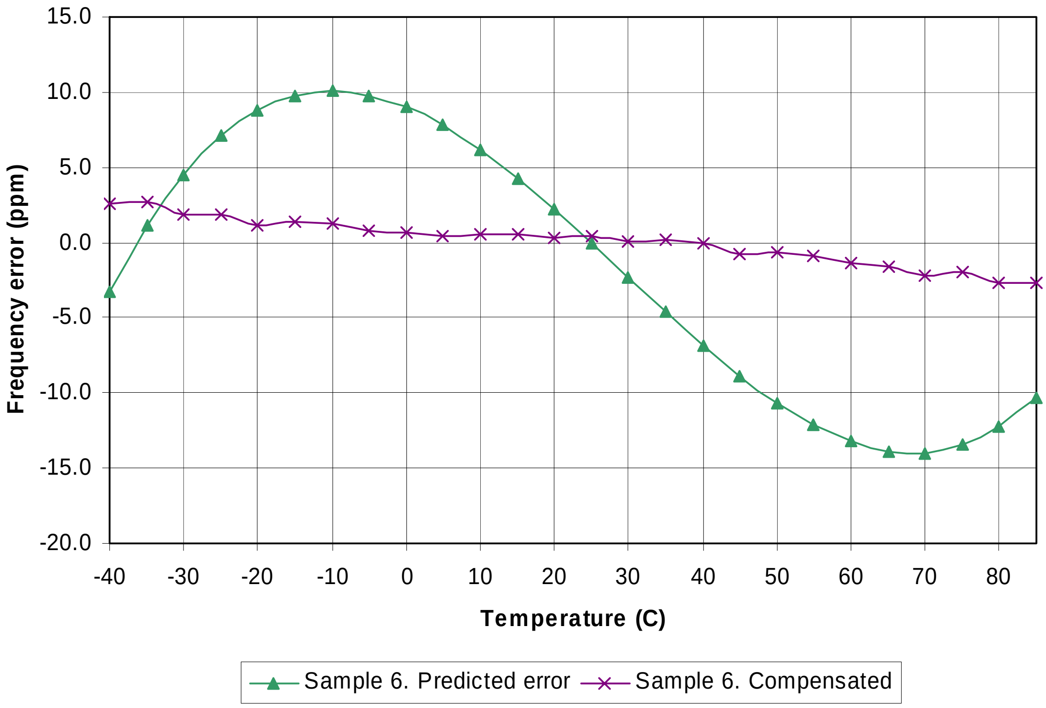

Figure 5. Predicted and compensated error. NDK

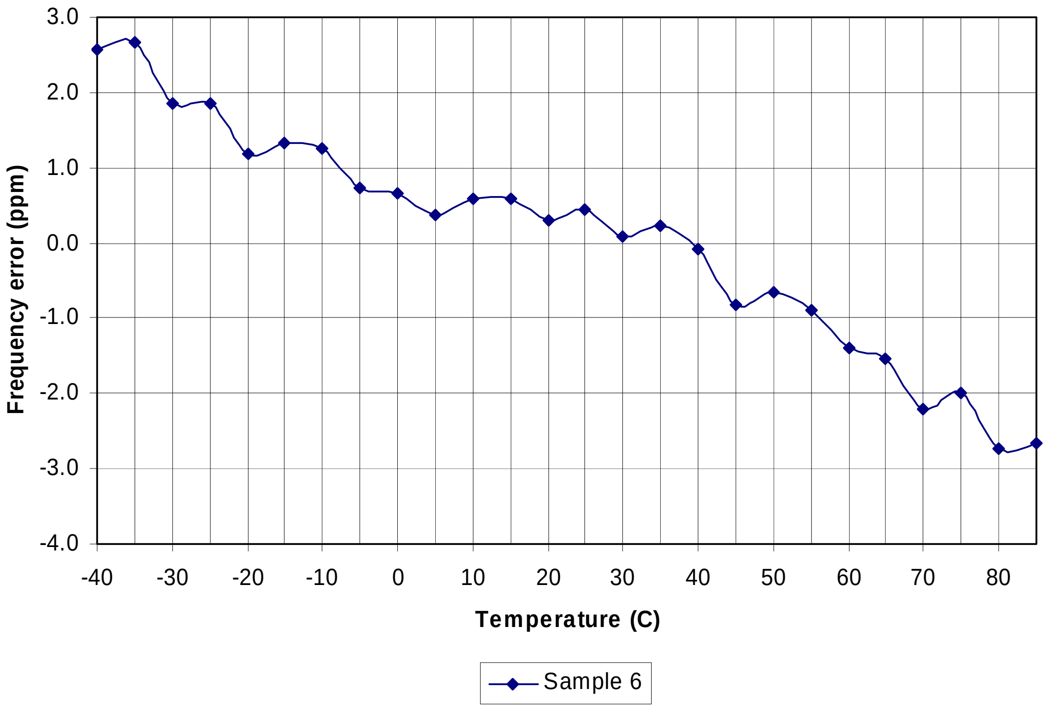

Figure 6. Frequency error after compensation. NDK

Conclusion

To meet the frequency error requirements for narrowband applications as given by the EN 300 220 and ARIB STD T-67 standards it is necessary to compensate every crystal for temperature drift. The traditional solution is to utilize a TCXO. The availability of low-cost crystals with known temperature behaviour, however, allow designers of cost-sensitive RF systems to consider indirect compensation of crystal temperature drift instead of using a TCXO. That is, by exploiting the very fine frequency tuning properties of the Chipcon transceivers and transmitters the temperature drift compensation can be performed using an external temperature sensor and a frequency compensation look-up table. Furthermore, the initial crystal tolerance and crystal loading frequency errors can easily be corrected for during production by utilizing the high resolution of the PLL and hence there is no need to use expensive crystals with very tight frequency tolerances. Re-programming the PLL to minimize the frequency errors of a standard crystal offers the benefit of cost reduction as well as a lower oscillator current consumption than using a TCXO.

Figure 4 and Figure 6 show that the frequency error requirement defined in the EN 300 220 standard for the temperature range from –10^{o}C to +55^{o}C is met using indirect compensation of the crystal frequency errors. For 868 MHz operation the maximum allowed crystal aging is ±1.5 ppm for mobile and fixed (base) stations and ±2.0 ppm for portable stations. For 433 MHz operation the maximum allowed crystal aging is ±3.0 ppm for mobile and fixed (base) stations and ±4.5 ppm for portable stations.

Figure 4 and Figure 6 show that the frequency error requirement defined in the ARIB STD T-67 standard for the temperature range from –40^{o}C to +85^{o}C is met using indirect compensation of the crystal frequency errors. The maximum allowed crystal aging is ±1 ppm.

The crystal manufacturer measures the temperature behaviour using a specified crystal load. Using a crystal load different from that specified by the crystal manufacturer will tilt the curve describing the temperature behaviour slightly. The reason for the declining slope in the compensated frequency error versus temperature plots in Figure 4 and Figure 6 is due to non-optimum crystal loading being used. Using the correct crystal loading will reduce the compensated frequency error and thus relax the maximum crystal aging requirement.

A narrowband system incorporating a bar-coded crystal, a temperature sensor and a transceiver or transmitter IC with sufficiently fine frequency resolution, provides the user with a cost-effective alternative to TCXO in many applications. The cost associated with the required production testing must, however, be taken into account.

Appendix A: Compensation of crystal frequency errors using CC1020

Introduction

Programming the frequency word in the configuration registers defines the operational frequency. There are two frequency words, termed *FREQ_A[22:0]* and *FREQ_B[22:0]*, which can be programmed to two different frequencies. One of the frequency words can be used for Rx and the other for Tx in order to be able to switch very fast between Rx mode and Tx mode. They can also be used for Rx (or Tx) at two different channels. In this application note we assume *FREQ_A[22:0]* is used for Rx mode and *FREQ_B[22:0]* is used for Tx mode.

In Rx mode the frequency word defines the local oscillator (LO) frequency. In Tx mode the frequency word defines the transmit carrier frequency. It can be shown that the same correction factors can be used both for the Rx and Tx frequency words. In the following we assume that the correction factors are calculated with the CC1020 set in Tx mode.

Tx frequency word

Define *FREQ_B[22:0]* as *[FREQ_TX1:DITHER]* , where *FREQ_TX1* is bits 22 down to 1 and *DITHER* is bit 0.

3) Calculate the *FREQ_TX1* decimal value, which corresponds to the desired carrier frequency, as:

In the 804 – 960 MHz frequency band:

$$FREQ\_TX1 = \left[\frac{f_{cd}(REF\_DIV + 1)}{f_{xosc}} - \frac{3}{2} \right] \cdot 16384 - 0.5 \cdot DITHER \tag{3a}$$

In the 402 – 480 MHz frequency band:

$$FREQ\_TX1 = \left[\frac{f_{cd}(REF\_DIV + 1)}{f_{xosc}} - \frac{3}{4} \right] \cdot 32768 - 0.5 \cdot DITHER \tag{3b}$$

where

f_{cd} is the desired RF carrier frequency
f_{xosc} is the nominal crystal oscillator frequency
REF_DIV is an integer between 1 and 7

4) Round *FREQ_TX1* to the nearest integer value

5) The *FREQ_B[22:0]* register contents (decimal) is then calculated as:

$$FREQ\_B = 2 \cdot FREQ\_TX1 + DITHER \tag{4}$$

Rx frequency word

Define *FREQ_A[22:0]* as *[FREQ_RX1:DITHER]*, where *FREQ_RX1* is bits 22 down to 1 and *DITHER* is bit 0.

6) Calculate the *FREQ_RX1* decimal value, which corresponds to the desired carrier frequency, as:

In the 804 – 960 MHz frequency band:

$$FREQ\_RX1 = \left[\frac{(f_{cd} - IF) \cdot (REF\_DIV + 1)}{f_{xosc}} - \frac{3}{2} \right] \cdot 16384 - 0.5 \cdot DITHER \quad \text{(5a)}$$

In the 402 – 480 MHz frequency band:

$$FREQ\_RX1 = \left[\frac{(f_{cd} - IF) \cdot (REF\_DIV + 1)}{f_{xosc}} - \frac{3}{4} \right] \cdot 32768 - 0.5 \cdot DITHER \quad \text{(5b)}$$

IF is the intermediate frequency and is calculated as:

$$IF = \frac{ADC\_CLK}{4} = \frac{f_{xosc}}{4 \cdot (ADC\_DIV \cdot 2 + 2)} \quad \text{(6)}$$

where

the IF frequency should be as close to 307.2 kHz as possible
f_{xosc} is the nominal crystal oscillator frequency
ADC_DIV is the ADC clock divisor

7) Round *FREQ_RX1* to the nearest integer value

8) The *FREQ_A[22:0]* register contents (decimal) is then calculated as:

$$FREQ\_A = 2 \cdot FREQ\_RX1 + DITHER \quad \text{(7)}$$

Initial crystal tolerance and crystal loading errors correction factor

The initial tolerance and crystal loading correction factor, *FREQ_ERR0* is calculated as follows:

9) Measure the carrier frequency at temperature T_0 (e.g. ambient temperature (25^{o}C)).

10) Calculate the correction factor for the initial crystal tolerance and the crystal loading compensation *FREQ_ERR0* as:

In the 804 – 960 MHz frequency band:

$$FREQ\_ERR0 = \left[\frac{16384 \cdot (REF\_DIV + 1)}{f_{xosc}} \right] \cdot [f_{cd} - f_{cm}] \quad \text{(8a)}$$

In the 402 – 480 MHz frequency band:

$$FREQ\_ERR0 = \left[\frac{32768 \cdot (REF\_DIV + 1)}{f_{xosc}} \right] \cdot [f_{cd} - f_{cm}] \quad \text{(8b)}$$

where

f_{cm} is the measured RF carrier frequency

11) Round *FREQ_ERR0* to the nearest integer value

12) Store the correction factor *FREQ_ERR0* in the microcontroller flash memory

Compensation of initial crystal tolerance and crystal loading errors

Compensate for initial crystal tolerance and crystal loading compensation by calculating a new *FREQ_B[22:0]* frequency word as:

$$FREQ\_B1 = FREQ\_B + 2 \cdot FREQ\_ERR0 \tag{9}$$

Note that the temperature error at temperature T_o is also compensated for in the above procedure.

Temperature drift correction factor

The temperature drift correction factor at temperature T, *FREQ_ERR1(T)* is calculated as follows:

13) Calculate the temperature drift correction factor at temperature T, *FREQ_ERR1(T)*, as:

In the 804 – 960 MHz frequency band:

$$FREQ\_ERR1(T) = \left[\frac{16384 \cdot (REF\_DIV + 1)}{f_{xosc}}\right] \cdot f_{cd} \cdot \left[T_{error}(T) - T_{error}(T_0)\right] \tag{10a}$$

In the 402 – 480 MHz frequency band:

$$FREQ\_ERR1(T) = \left[\frac{32768 \cdot (REF\_DIV + 1)}{f_{xosc}}\right] \cdot f_{cd} \cdot \left[T_{error}(T) - T_{error}(T_0)\right] \tag{10b}$$

where

$T_{error}(T)$ is given by equation 1

$T_{error}(T_0)$ is the temperature at which initial crystal tolerance and crystal loading compensation was performed

14) Round *FREQ_ERR1(T)* to the nearest integer value

15) Store the correction factor *FREQ_ERR1(T)* in the microcontroller flash memory

Compensation of crystal temperature errors

Compensate for frequency errors over temperature by calculating a new *FREQ_B[22:0]* frequency word for as:

$$FREQ\_B(T) = FREQ\_B1 - 2 \cdot FREQ\_ERR1(T) \tag{11}$$

References

[1] ETSI EN 300 220. http://www.etsi.org
[2] ARIB STD T-67 Standard
[3] Chipcon, *CC1020 data sheet*. Downloadable from http://www.chipcon.com
[4] Microchip, *TC1046 High-precision temperature-to-voltage converter data sheet*
[5] HKC, 5 x 3.2 mm SMD crystal. http://www.hongkongcrystal.com
[6] NDK, NX5032SA (W-191-520), 5 x 3.2 mm SMD crystal. http://www.ndk.com

Document History

Revision	Date	Description/Changes
1.0	January 2004	Initial release
1.1	June 2004	The declining slope in the compensated frequency error versus temperature plots in Figure 4 and Figure 6 is due to non-optimum crystal loading being used and not the temperature sensor accuracy.

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