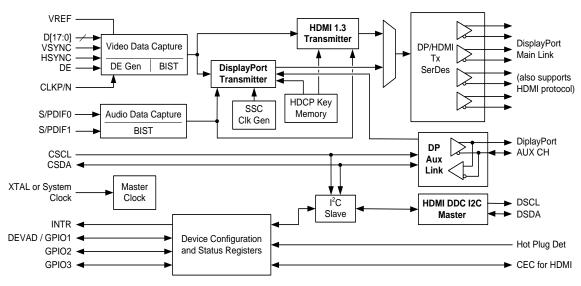


DisplayPortTM/HDMITM Transmitter

- Product Compliance
 - DisplayPortTM 1.1a with HDCP 1.3
 - $\mathrm{HDMI}^{\mathrm{TM}}$ 1.3 with HDCP 1.2
 - $\mathrm{HDMI}^{\mathrm{TM}}$ 1.2 and DVI 1.0 backward compatible
- Output Interface
 - Dual Mode: DisplayPort[™] or HDMI[™] output
 - 1/2/4 lane operation at up to HBR(2.7 Gbps/lane) and RBR(1.62 Gbps/lane)
 - DisplayPort[™] mode Spread Spectrum Clock (SSC) support
 - Support up to 2560X1600(WQXGA)@60Hz with 30bpp colour depth
 - YCbCr to RGB conversion
 - 4:4:4 and 4:2:2 data input formats
 - 18/24/30/36 bits per pixel video support
 - Embedded audio support
 - HDCP encryption
- Input Interface
 - -18 -bit DVO/LVTTL flexible video input
 - SDR and DDR data modes support
 - Deep colour up to 36bpp in DDR support

- Audio Input Interface
 - S/PDIF audio mode including two-channel uncompressed L-PCM and multi-channel compressed DTS support
 - 32,44.1,48,88.2,96,176.4 to 192KHz audio sampling rates support
- Embedded HDCP key shared for DisplayPort[™], HDMI[™], and DVI modes
- Programmable output swing and pre-emphasis
- Support of upstream content protection protocol with embedded upstream keys
- Hot Plug and Unplug detection mechanism
- Built-in video pattern generator and audio tone generator for system self-test
- Package: 80-pin TQFP
- 0.18um CMOS process
- Power Management
 - 1.8V and 3.3V Power supplies
 - Software controlled power management
- RoHS compliant and Halogen free package



ANX9805 Block Diagram



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Reference

Application Notes	Comments
DisplayPort TM Specification, Ver.1 Rev.1a	
HDMI specifications	
I2C SPECIFICATION	

Revision History

Revision	Date	Comments
Version 1.5	December 2007	
Issue 2	September 2011	Removed all references to BGA package, which is now end of life. Removed all part number variants other than ANX9805J, which are end of life.

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