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Texas Instruments

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TEXAS INSTRUMENTS

TEXAS INSTRUMENTS STORAGE PRODUCTS

Texas Instruments Storage Products is a leading designer and manufacturer of advanced semiconductors for mass storage applications. Addressing the performance, capacity and cost demands of the storage market, Texas Instruments Storage Products' integrated circuits (ICs) deliver total systems solutions to storage customers worldwide.

Texas Instruments Storage Products combines digital signal processor (DSP) and analog and mixed signal leadership, with high performance read channels, industry leading preamps and custom servo/spindle control, and ASIC backplane capabilities to benefit customers. Together with design and systems firmware expertise, application and engineering support and manufacturing prowess, Texas Instruments Storage Products provides customers with total systems solutions and product differentiation, resulting in faster time-to-market.

Our commitment to the storage industry continues with research and development of next generation products and technologies, including our latest advances in complete Systems-On-a-Chip (SOC) solutions. Our leading edge SuperChannel technology provides the best industry solutions, combining our performance leading DSP architecture with high speed signal processing read channels and industry leading embedded SRAM capabilities.

For additional information visit us at www.ti.com/storage.

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Texas Instruments Storage Products Group

SHORT FORM CATALOG

2000

THE WORLD LEADER IN DSP AND ANALOG

Texas Instruments

Hard Disk Drives Products

Read Channel Devices

Device Number	Circuit Function	Features
32F8101/02/03/04	Low Power Digitally Programmable Filter	(8101/02/03) - 8001/02/03 w/serial port & DACs, 95 mW, (8104) - Similar to 8103, *f*c range 3-9 MHz
32P4101A	Complete Read Channel	EPR4, ML Channel, 67 to 200 Mbit/s, byte wide NRZ, 16/17 (0,6,8) code, A,B,C,D area detect servo
32P4103A	Complete Read Channel	EPR4, ML Channel, 80 to 240 Mbit/s, byte wide NRL, 16/17 code, A.,B,C,D servo
32P4103B	Complete Read Channel	32P4103A with area detect servo
32P4103S	Complete Read Channel	32P4103A with high fly write detect
32P4104H	Complete Read Channel	EPR4, ML Channel, 100 to 300 Mbit/s, byte wide NRL, 16/17 code, A.,B,C,D servo
32P4104S	Complete Read Channel	EPR4, ML Channel, 125 to 350 Mbit/s, with high fly write detect
32P4129	Complete Read Channel	EPR4, ML Channel, 42 to 135 Mbit/s, byte-wide NRZ, 16/17 code A,B,C,D area detect servo
32P4802	Complete Read Channel	EEPR4, ML Channel, 30 to 120 Mbit/s, dual bit NRZ, 1/7 code, A,B,C,D servo
32P4937A	Complete Read Channel	PR4, ML Channel, 80 to 240 Mbit/s, byte-wide NRZ, A,B,C,D area detect servo
SP4107A	Complete Read Channel	EPR4, ML Channel, 125 to 350 Mbit/s, 10 bit A/D servo parrallel port
SP4140A	Complete Read Channel	EPR4, CMOS ML Channel, 450 Mbit/s, digital servo

Head Positioning and Spindle Motor Control

Device Number	Circuit Function	Features
32H6742	Servo/Spindle 12 V Predriver	PWM/Linear spindle control, serial port, SilentSpin™ TPICxxx power driver array support
32H6816	Servo/Spindle 5 V Driver	10-bit D/A, serial port, speed control, shock detector, 1.5 A SPM
32H6818	Servo/Spindle 5 V Driver	10-bit D/A, serial port, speed control, shock detector, ramp loading
32H6826	Servo/Spindle 12 V Predriver	SilentSpin™ acoustic noise reduction, PWM buffers, synchronous phase detection
32H6829	Servo/Spindle 12 V Predriver	PWM spindle control, PLL synchronous comutation, PWM buffers
32H6829A	32M6825 replacement	Servo/spindle 12 V predriver, PWM, synchronous commutation, 48-pin version of 32H6829
32H6840	Servo/Spindle 12 V Predriver	DSP with 15-MIPS DSP core, SilentSpin™ spindle/VCM controller, two 10-bit D/A, 10-bit A/D
32H6900	Servo/Spindle 12 V Driver	1.2 A spindle, 0.5 A VCM, synchronous PWM commutation, 0.8 RDS(on), 1.0 RDS(on)
32H6910	Servo/Spindle 12 V Driver	1,2 A spindle, 0.8 VCM, 2.0 Ω RDS (on) VCM and spindle, on-chip 14-bit VCM DAC and 8-bit spindle DAC
TLS2231	Servo/Spindle 12 V Predriver	PWM/linear spindle control, TPICxxx power driver array support
TLS2232	Servo/Spindle 12 V Predriver	PWM/linear spindle control, TPICxxx power driver array support
TLS2233	Servo/Spindle 12 V Predriver	PWM/linear spindle control, TPICxxx power driver array support
TLS2234	Servo/Spindle 12 V Predriver	PWM/linear spindle control, TPICxxx power driver array support
TLS2235	Servo/Spindle 12 V Predriver	PWM/linear spindle control, serial port, TPICxxxx power driver array support
TLS2245	Servo/Spindle 5 V Driver	10-bit D/A, serial port, speed control, shock detector, 1A spm
TLS2251	Servo/Spindle 5 V Driver	10-bit D/A, serial port, speed control, shock detector, 1A spm
TLS2270	12V Predriver	Class-AB VCM with discrete FETs, 10-bit VCM DAC, 10-bit ADC
TLS2271	12V Predriver	Class-AB VCM with discrete FETs, 10-bit VCM DAC, 10-bit ADC

Regional Sales Offices:

Asia (65) 744-7700

Eastern U.S. (603) 898-1444

Japan (81) 3-3769-8705

Northwest U.S. (408) 432-7100

Southwest U.S. and Europe (303) 651-5900

Tustin (714) 573-6567

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MR Read/Write Preamps

Differential

Market Number	Channels	Archi-tecture	Serial Port	Power Supply	Thermal Asperity	MR Head Resis-tance	Voltage Gain	Noise nV/Hz	Band-Width MHz	Write Current mA	Head Swing Min, Vp-p	Rise Time, ns
32R1574R	10	Ib, Vs	No	+5, -5	Fast	22-85	150	0.55	100	10-45	12	2.7
32R1577R	10	Ib, Vs	Yes	+5, -5	Det, Fast, Comp	30-85	150-300	0.55	150-225	20-60	16	1.7
32R1590AR	10	Ib, Vs	Yes	+5, -5	Det, Fast, Comp	40-70	150-300	0.55	150-225	20-60	16	1.3
SR1581A	4,8	Ib, Vs	Yes	+5, -5	Fast	25-80	100-150	0.8	220	15-65	12	1.4
SR1595A	12	Ib, Vs	Yes	+5, -5	Det, Fast	40-80	150-300	0.5	150-300	10-50	16 nom	0.9
SR1720A	12	Ib, Vs	Yes	+5, -5	Det, Fast	30-80	150-300	0.5	175-350	20-65	16 nom	0.55
SR1731B	4	Ib, Vs	Yes	+5, -5	Det, Fast	25-80	100-150	0.5	300	15-65	12	0.8
SR1750A	8	Ib, Vs	Yes	+5, -5	Det, Fast	30-80	150-300	0.7	150-300	32-63	16 nom	0.55
SR1770A	12	Ib, Vs	Yes	+5, -5	Det, Fast, Comp	30-80	100-250	0.5	175-350	20-65	16 nom	0.55
TLS26286	6	Ib, Vs	Yes	+5, -3 V	Det, Comp, Rec	29-80 Ω	120-150	0.5	200	27.5-65	12	1.7

Single-Ended

32R1606R/AR	4,8	Ib, Is	Yes	+5	Det, Fast, Comp	25-41	200/300	0.75	130	14-45	9	2
32R1607AR	4,8	Ib, Is	Yes	+5	Det, Fast, Comp	35-60	200/300	0.85	130	15-50	9	2
32R1608CR	4,8	Ib, Is	Yes	+5	Det, Fast, Comp	40-65	100-200	0.85	150	10-45	9	2
32R1610AR	8	Ib, Is	Yes	+5,+8	Det, Fast, Comp	35-80	150/220	0.75	180	15-55	7.5	1.3
32R1611D	4,6	Ib, Is	Yes	+5,+8	Det, Fast, Comp	25-75	225/300	1.1	250	15-60	8	1.1
32R1615DR	4,8	Ib, Is	Yes	+5,+8	Det, Fast, Comp	35-80	150/220	0.75	180	15-60	7.5	1.3
SR1621A	4	Ib, Is	Yes	+5	Det, Fast, Comp	46-86	200/250	1	160	15-50	9	1.6
SR1622A	4	Ib, Is	Yes	+5,+8	Det, Fast, Comp	25-75	112-150	1.1	280	15-60	8	0.9
SR1710A	4	Ib, Is	Yes	+5,+8	Det, Fast, Comp	25-80	100-220	0.72	330	15-50	7.5	0.6
TLS25004	4	Ib, Is	Yes	+5	Det, Fast, Comp	15-45	290/362	0.55	165	10-60	6	2
TLS25006	6	Ib, Is	Yes	+5	Det, Comp	15-45	290/362	0.55	165	10-60	6	2.2
TLS26354	4	Ib, Vs	Yes	+5, +8	Det, Rec	30-75	200/280	0.55	100-190	32-63	12	1.4
TLS26356	6	Ib, Vs	Yes	+5, +8	Det, Rec	30-75	200/280	0.55	100-190	32-63	12	1.4
TLS26454	4	Ib, Vs	Yes	+8	Det, Comp, Rec	25-85	120/150	0.5	175-300	31-59	12	1.3
TLS26458	8	Ib, Vs	Yes	+8	Det, Comp, Rec	25-85	120/150	0.5	175-300	31-59	12	1.3
TLS36531	1	Ib, Vs	No	+5	No	30-75	200	0.55	180	20-60	8.9	2.5
TLS26554	4	Ib, Vs	Yes	+5, +8	No	30-75	200	0.55	180	20-60	12	1.3

Thin Film Read/Write Preamps

5 Volt

Market Number	Channels	Flip Flop	Input Type	Noise nV/Hz	Write Current, mA	Input Cap, pF	Servo Enable	Voltage Gain	Damp Resistor	Rise Time ns	Band-width MHz, Min.	Min. Head Swing Vp-p
32R2410R-2	2	Yes	PECL	0.45	3-20	6	Yes	200, 250, 300, 350	350	2	80	7
32R2410R-4	4	Yes	PECL	0.45	3-20	6	Yes	200, 250, 300, 350	350	2	80	7
32R2412R-2	2	No	PECL	0.45	3-20	6	Yes	200, 250, 300, 350	350	2	80	7
32R2412R-4	4	No	PECL	0.45	3-20	6	Yes	200, 250, 300, 350	350	2	80	7
TLS21H62/L62/L72	2	Yes	TTL	0.5	3-35	8.5	No	300	350	7	65	6.8

Texas Instruments

Storage Products

Texas Instruments Storage Products is a leading designer and manufacturer of advanced semiconductors for mass storage applications. It has design, manufacturing and sales offices in more than 25 countries.

Addressing the performance, capacity and cost demands of the storage market, Texas Instruments Storage Products integrated circuits (ICs) deliver total systems solutions to customers worldwide. These customers develop and manufacture hard disk drives, removable drives and emerging mass storage technologies.

Texas Instruments Storage Products combines digital signal processor (DSP) and analog and mixed signal leadership, with industry-proven read channels, servo motor speed control, preamps, controllers, interface controllers and ASIC capabilities to benefit customers. Together with design and firmware expertise, application and engineering support, and manufacturing prowess, Texas Instruments Storage Products provides customers with total systems solutions and product differentiation resulting in faster time-to-market.

For additional Texas Instruments Storage Products information visit www.ti.com/storage

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SQHT004 (03/00)

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Product Line introduced in 2000:

SR1595AEA6 +5V, -5V, 6-Channel, MR Head Read/Write Device

SR1621AAA4 +5V, 4-Channel, MR Head Read/Write Device

SR1622ABA4 +5V, +8V, 4-Channel, MR Head Read/Write Device

SR1710AFA +5V, +8V, 4-Channel, MR Head Read/Write Device

SR1720DDA +5V, -5V, 10-Channel, MR Head Read/Write Device

SR1730 +5V, -5V, 4, 8-Channel MR Read/Write Device

SR1760 +5V, -5V, 4-Channel, MR Read/Write Device

SR1731BBA4 +5V, -5V, 4-Channel, MR Head Read/Write Device

TLS2271 12V Predriver

Continuing Product Line:

32F8101 Low-Power Programmable Filter

32F8102/03/04 Low-Power Programmable Filter

32H6826A Advanced Servo and Spindle Predriver

32H6829/6829A Servo and Spindle Predriver

32H6840 Advanced Servo and Spindle Predriver with DSP

32H6900 Servo/Spindle Driver

32H6910 12V VCM/Spindle Driver

32R1590AR +5V, 10-Channel, MR Head Read/Write Device

32R1608CR +5V, 4, 8-Channel, MR Head Read/Write Device

32R1610AR +5V, +8V, 4, 8-Channel, MR Head Read/Write Device

32R1611D +5V, +8V, 4, 6-Channel, MR Head Read/Write Device

32R1615DR +5V, +8V, 4, 8-Channel, MR Head Read/Write Device

32R2410/11/12R +5V, 2, 4-Channel, Thin Film Read/Write Device

32P4103A EPRML Read Channel with 16,17's ENDEC, 4-Burst Servo (A, B, C, D)

32P4103B EPRML Read Channel with 16,17's ENDEC, 4-Burst Area Detect Servo (A, B, C, D)

32P4104A EPRML Read Channel with 16,17's ENDEC, 4-Burst Area Detect Servo (A, B, C, D)

33P3705 E2PR4ML Read Channel with 1,7 ENDEC, Data Resync Capability

34H3306 Servo-Combination Driver

34H3307 Servo-Combination Driver

34P3211B Read Channel for Tape Storage

34P3214 Read Channel for High Density Floppy and Tape/Disk Drives

34P3216A Read Preamp/Channel for Tape Storage

34P3402A 8 to 53 Mbit/s Read Channel with Adaptive Threshold Qualifier

34R3430R +5V, 2-, 4-Channel, 3-Terminal Read/Write Device

34R3433R 3.3V/5V, 2-Channel, Read/Write Device

34R3435 5/12V, 1-Channel BiCMOS Thin Film and MR Tape Drive R/W Device

34R3436 +5/+12V, 1-Channel, TFH/MR Tape Drive Read/Write IC

34R3437B 5V, 2-Channel, Write Coil Driver with Read Buffer

34R3440B Preamp and Analog Front End / Write Driver for 4 Channel Magnetic Tape Drives

34R3443A +5V Coil Driver for Tape Drivers

SR1595AEA6 +5V, -5V, 6-Channel, MR Head Read/Write Device

SR1621AAA4 +5V, 4-Channel, MR Head Read/Write Device

SR1622ABA4 +5V, +8V, 4-Channel, MR Head Read/Write Device

SR1710AFA +5V, +8V, 4-Channel, MR Head Read/Write Device

SR1720DDA +5V, -5V, 10-Channel, MR Head Read/Write Device

SR1730 +5V, -5V, 4, 8-Channel MR Read/Write Device

SR1731BBA4 +5V, -5V, 4-Channel, MR Head Read/Write Device

SR1760 +5V, -5V, 4-Channel, MR Read/Write Device

T320C2700 Customizable Digital Signal Processor (c' DSP™) Core

TLS21H62-3PW 5V Thin Film 2-Channel Low Noise Read/Write Preamplifiers

TLS2231 Servo-Combination Predriver

TLS2232 Servo-Combination Predriver

TLS2233 Servo-Combination Predriver

TLS2234 Servo-Combination Predriver

TLS2242 Servo Combination Driver

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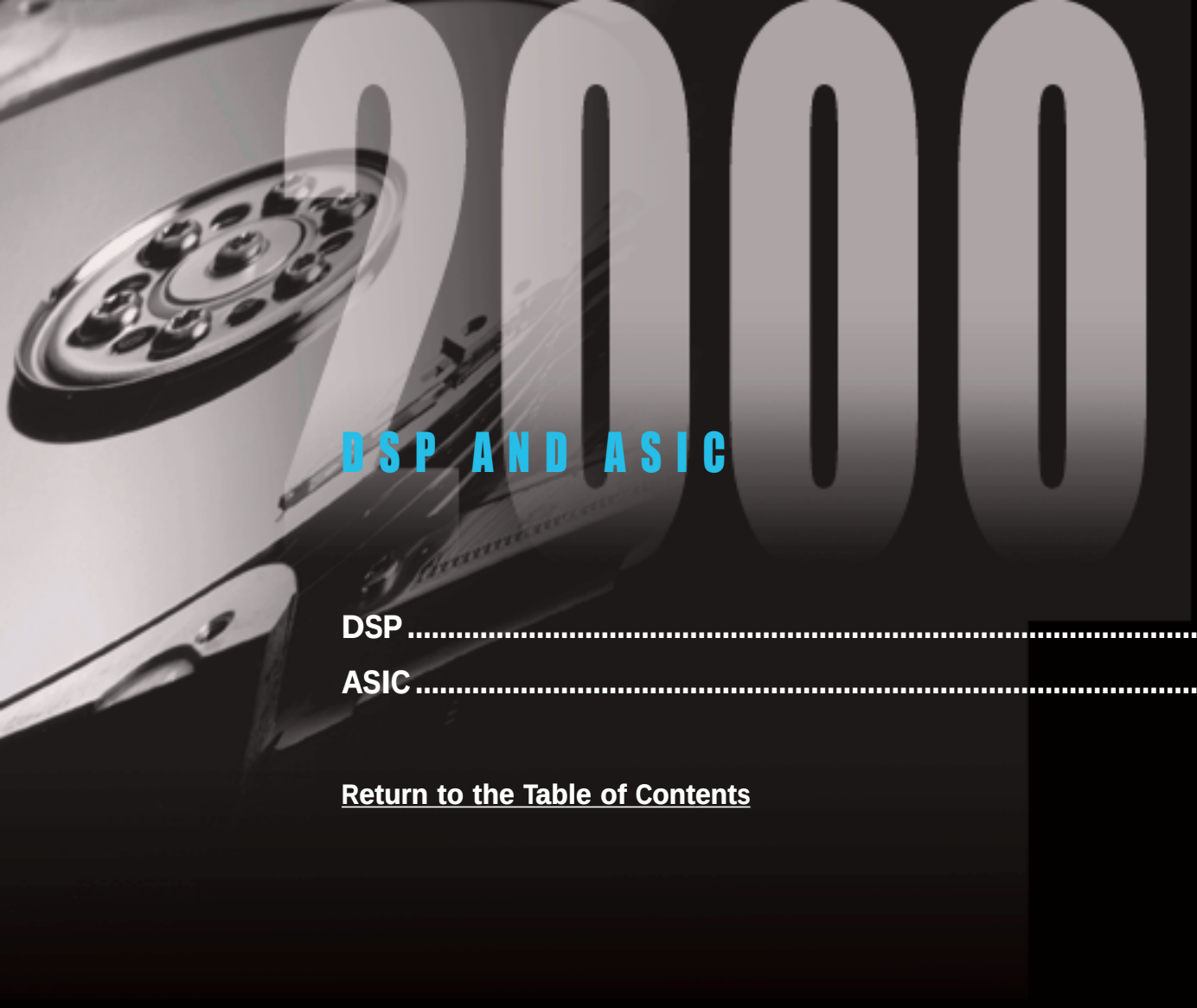

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DV25 Chipset

DSP Solutions for Mass Storage

Typically, digital signal processors are used to implement servo timing and control and power management functions in mass storage equipment. In many designs, DSPs simultaneously perform host-interface control processing, eliminating the need for a separate microcontroller or microprocessor. DSP software can replace such hardware functions as real-time error correction, predictive caching and adaptive disk-head equalization.

DSP technology from Texas Instruments offers a broad array of options for mass storage designers including 16-bit fixed point customizable DSP (cDSP) cores which are all well suited for control applications, as well as fully integrated advanced digital solutions.

Designers also have access to TI's extensive development tools, emulators and code developers. With 15 years of DSP leadership experience, and an ongoing commitment to new standard products and cores, TI's storage products are uniquely positioned to help mass storage designers maximize the potential benefits found in DSP solutions.

Texas Instruments cDSP technology offers high volume customers the opportunity to design a mass storage processor from the ground up. Using one of the most advanced ASIC processes in the industry, customers have the flexibility to integrate peripherals that they designed with the large base of intellectual property provided by TI. TI's extensive ASIC libraries include DSP cores, memory, A/D's, and host-port interface technology blocks for SCSI, ATA, 1394 and Fiberchannel designs. Moving to a custom solution allows for maximum design integration while also lowering the total system costs.

TMS320C27x 16-bit Fixed-Point Customizable DSP Core

For the first time in the history of embedded control a processor has been designed with features optimized for Mass Storage applications. The Texas Instruments TMS320C27x core combines the high speed multiply and accumulate (MAC) operations of Digital Signal Processors with the input/output (I/O) characteristics of microcontrollers. The result is a high performance processor with a world of capabilities solely meant for current and future real-time embedded applications. TI also has a roadmap to higher performance processors that will allow our customers to design innovative solutions well into the future. The benefits of the 'C27x available to our customers today are:

DSP Solutions for Mass Storage (continued)

General features

- 16-bit, fixed point architecture
- 150 MIPS performance in a 1.8V, 0.18-micron (Leff) version
- 7 ns instruction cycle time
- 32-bit on-chip data bus fetches two words in a single cycle
- Register-based architecture
- 16- or 32-bit instructions with total address space equal to 16 MB
- Dedicated stack pointer

DSP features

- Separate program and data busses (modified Harvard architecture)
- 16x16-bit multiplier
- Single-cycle multiply and accumulate (MAC)
- Saturation instructions and modes

MCU features

- Configurable in Von Neumann mode (combined bus)
- Single-cycle, atomic, read-modify-write operations (logical and arithmetic)
- Automatic context save and restore for fast interrupt response
- Fast interrupt response (53 ns latency, 80 ns for full context switch)
- MCU-like instruction set mnemonics

Emulation features

- Zero-overhead, hardware-based, real-time debug capability
- Real-Time Data logging capability
- Two hardware break points
- Single data watch point
- Benchmarking counter
- Programmable signature analysis
- Available real-time code trace

ASIC Solutions for Mass Storage

Texas Instruments and Silicon Systems are working together to create optimum ASIC solutions for mass storage. Together we offer access to advanced architecture, simplified design support, advanced process and packaging technology, and high-volume manufacturing.

Advanced Architecture

Our portfolio offers cost-effective ASIC technology for designs ranging from a relatively low level of integration to highly integrated, high-speed designs. With our new TImeCell Architecture, designers can cut costs by using ultra-dense standard cells for proven sections of design, and can cut cycle time by using gate arrays for new logic. This approach reduces layout and prototype fab time by more than 50 percent over standard-cell architecture and allows design changes up until the last minute. The TI GS30 0.15-_m CMOS ASIC uses the new TImeCell Architecture.

To simplify the design process we offer many cores, cells and macros for use in mass storage systems. A few of them are:

- Advanced core technology including: DSPs and customizable 32-bit RISC microcontrollers
- A full line of memory cells for use in your designs, including: ROM, synthesizable RAM, CAM and SRAM (dual-port, single-port, two-port and three-port macros)
- High-performance I/Os: SCSI Ultra3, ATA-66, 1394, Fibre Channel
- A full line of analog functions: APLL, 8- and 10-bit analog-to-digital and digital-to-analog converters, oscillator, clock squarer with low-power mode, analog comparator, analog threshold cell

Flexible Design Support

By working with Silicon Systems and TI, you have access to technology blocks for interface controllers. These blocks include error correction circuitry, clock control, disk formatter, buffer manager, and processor. We also offer a flexible business environment that ranges from tactical cell development to full custom designs using the TI ASIC backplane. Knowledgeable systems engineers are available to help you make the right technology tradeoffs when considering new system design.

We provide many choices for third-party tools support, including Cadence, Synopsys, Mentor Graphics and many others. And our TI technology centers around the world offer on-the-spot design assistance.

Advanced Packaging and Process Technology

We offer a variety of advanced packaging choices for mass storage designs, including PowerPad TQFP for high-power applications and microStar BGA.

Our leadership in process technology ensures that we have technology that can accommodate designs with low gate counts through highly integrated, high gate count designs. All this while being able to deliver high-performance with minimal power consumption.

Manufacturing Strength

With six wafer fabs producing ASIC products and two high-volume assembly plants, we have the manufacturing capacity to accommodate large orders, providing a stable supply of products for your business needs.

Let Texas Instruments and Silicon Systems be your ASIC provider for mass storage.

2000 QUALITY AND TECHNOLOGY

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Texas Instruments

Quality and Technology

March 1998

INTRODUCTION

"BE THE SUPPLIER OF CHOICE BY EXCEEDING CUSTOMER EXPECTATIONS THROUGH CONTINUOUS IMPROVEMENT IN OUR PRODUCTS, SYSTEM AND SERVICES"

SPG is committed to the goal of customer satisfaction through the on-time delivery of products that exceed the customer's expectations and requirements.

We realize and practice the concept that quality and reliability must be designed and built into our products. We consider it every employee's responsibility to identify and implement quality initiatives in our work environment.

In addition, SPG utilizes rigid inspections and data analysis to evaluate the acceptability and variation existing in incoming materials and performs stringent outgoing quality verification. The manufacturing process flow is encompassed by an effective system of test/inspection checks and in-line monitors which focus on the control and reduction of process variation. These gates and monitors ensure precise adherence to prescribed standards and procedures. We provide 100% electrical testing for our products.

SPG also incorporates the use of statistical process control techniques into company operations. The control and reduction of the process variation by the use of statistical problem solving techniques, analytical controls and other quantitative methods ensures that SPG's products maintain the highest levels of quality and reliability.

BUSINESS EXCELLENCE ROADMAP

Business excellence is SPG's strategic thrust for the year 2000. To ensure that all aspects of our business are encompassed by this mandate, Quality and Technology has been chartered with the responsibility for developing, educating and overseeing the worldwide business excellence process. The continuous improvement initiative will lead to developing a new organizational culture, changing attitudes and stronger ownership and accountability for total customer satisfaction.

Characteristics of SPG's Continuous Improvement Mission and Objectives

- Executive Steering Committee leadership and direction - defines the right things to do and provides guidance - the right way to do them.
- Customer focus and partnering have been set up through on-site customer quarterly reviews. Quality, service, delivery score cards are reviewed with customers to ensure that customers' expectations are understood and new goals addressed.
- Continuous improvement is measured everywhere and by everyone. Metrics that reflect pride in accomplishment are celebrated.
- ISO 9000 certification is an important strategy for achieving total customer satisfaction. Our Singapore assembly and test operations facility has been ISO 9002 certified and our domestic facilities' quality systems have ISO 9001 certified through Intertek. We believe strongly that ISO 9000 certification proves that SPG is doing the right things right.
- Time-to-volume mindset and Reduction Plans for Defective Products Per Million have been institutionalized and monitored for effectiveness to targets.
- Quality management and employee empowerment are encouraged at all levels.
- Supplier partnership is a critical element of our quality strategy.

Quality and Technology

Quality Objectives

It is the practice of SPG to have quality and reliability objectives encompass all of its activities. This starts with a strong commitment of support from the company level and continues with exceptional customer support long after the product has been shipped.

SPG emphasizes the belief that quality and reliability must be built into all of its products by ensuring that all employees are educated in the quality philosophy of the company. Some of the features built into SPG quality culture include;

a. Structured training programs directed at wafer fabrication, test, process control personnel and supporting organizations.

- Team-based problem solving methodologies.
- Company-wide training of quality philosophy and statistical methods.

b. Designs for quality approach which includes scrutiny of the designs using statistically based automated models for simulations as well as device reliability checks.

To achieve it, we begin far “upstream” in the product development process.

c. Advanced technology engineering with emphasis on creating cost effective and highly integrated system solutions. Process technologies combine small geometry digital circuit capability with high performance analog processes (NPNS) and CMOS features.

d. Stringent in-process inspections, gates, and monitors.

e. Rigorous qualifications, evaluation of designs, materials, and processing procedures.

f. Stringent electrical testing (100% and QC AQL Sample testing).

g. Ongoing reliability monitors and process verifications.

h. Real-time use of statistical process control methodology.

i. Company level audits of manufacturing, subcontractors, and suppliers.

j. Control of non-conforming material.

k. A robust corrective action system that is modeled after 8D principles with a strong focus on verification and follow-thru for permanent systematic solutions.

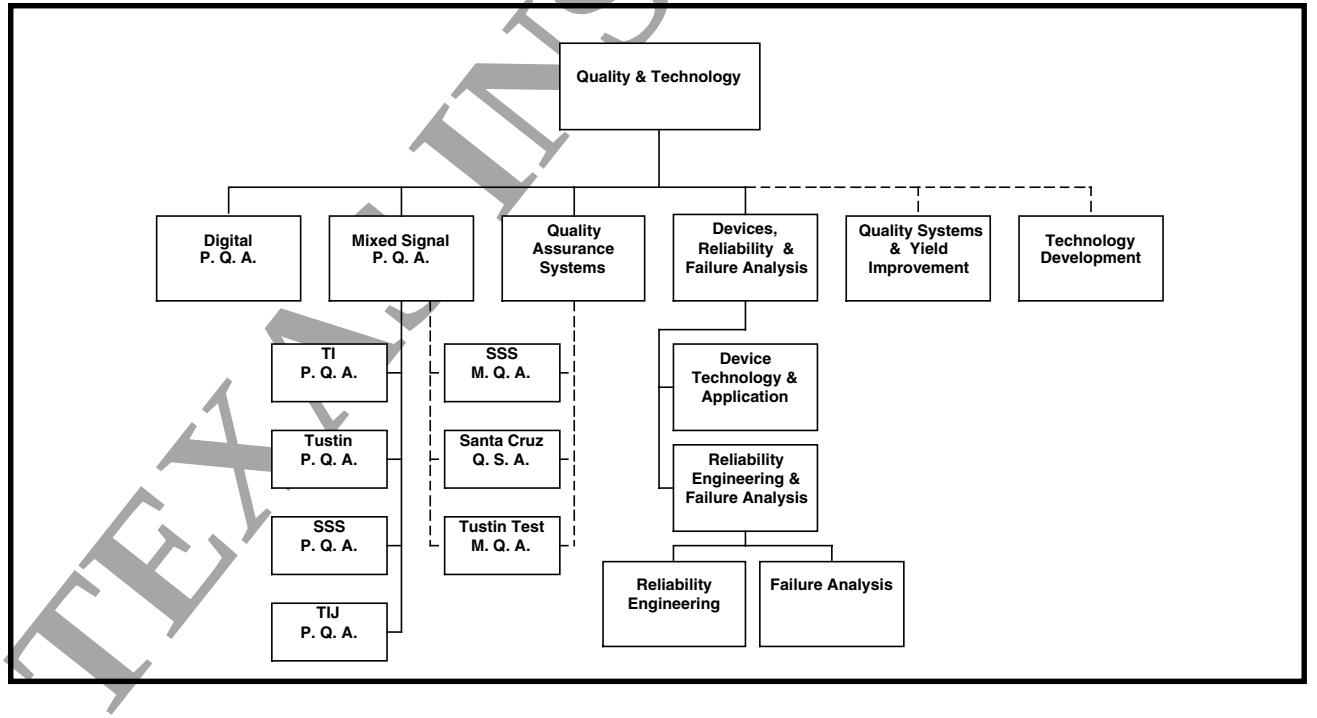

FIGURE 1: Quality and Technology

Overview of Quality Assurance Role and IC Program Management

IC Program management is the management process of defining, planning, developing, testing and manufacturing an IC product from initial conception through end- of- life. There are four phases with specific requirements and deliverables to support concurrent engineering. There is an under-lying basic assumption that the manufacturability and reliability issues must be comprehended at the design level in order to manufacture a reliable product that meets customer requirements. In this regard, the Quality and Technology organization is involved in all phases of the life cycle of the product. In SPG the Phases are as follows:

The definition phase covers the product launch, and product approval cycles needed to initiate the deign cycle. The customer's input is an essential part of this phase.

The development phase covers the detailed design, release of the IC design database (tape out), the fabrication of the prototypes and customer samples, the development of a test plan and functional test vectors, development of the verification plan, first article characterization and evaluation.

The verification phase covers all the testing (characterization, system level, beta site etc..) that is performed to ensure that the product conforms to the electrical specification.

The production ramp (sometimes known as manufacturability) phase covers all the product support, yield enhancement and other IC program management activities to ensure consistent and reliable product deliveries.

Throughout these phases, checklists are used to assure that potentials for errors are reviewed and risks eliminated.

The program team consist of members from marketing, design, product and process engineering ,testing, and quality organizations .Many activities are initiated in parallel in the spirit of concurrent engineering to bring a manufacturable and reliable product to market on time.

Quality and Technology is responsible for proactive quality systems to ensure that SPG's products will meet or exceed customer requirements and expectations. This includes facilitation of timely implementation of solutions and monitoring the effectiveness of corrective actions. These organizational strategies support the continuing enhancement of quality consciousness throughout SPG. Figure 1 shows the organization in presentation format.

A. Quality Assurance Departments:

- Product Quality Assurance (PQA)
- Quality Assurance Systems (QAS) and Documentation Control Systems
- Manufacturing QA organizations (MQA)

B. Reliabilty and Technology Departments supporting Process and Product Development

- Device Technology and Applications
- Reliability Engineering
- Failure Analysis

While all SPG employees have direct responsibility for quality in their functions, the Quality Assurance organizations have the ultimate responsibility for the reliable performance of our products.

Product Quality Assurance provides the liaison between SPG and the customer for all product quality related concerns. Quality Assurance supports, coordinates and actively participates in the formal qualification of suppliers, material, processes, and products, and the administration and audit of quality systems to assure that our products meet SPG quality standards. Manufacturing Quality Assurance administers the manufacturing quality systems and reports quality monitor data to the factory.

CUSTOMER FOCUSED QUALITY ASSURANCE SYSTEMS

Customer Interface

Product Quality Assurance (PQA) is involved with understanding the customers' requirements, even in the early stages of developing the business relationship. Shortly after the initial Sales contact, PQA becomes the contact point for customers regarding review of the customers' reliability and quality requirements such as FITS and MTBF targets, and even systems qualification requirements.

Quality and Technology

Customer Requirement Review

Customer specifications are channeled through the Customer Marketing, Sales and Quality Assurance organizations. These specifications are reviewed and compared to SPG standards. Any areas of incongruencies are noted and dialogue to resolve these differences are initiated with the customers contacts. Contracts are reviewed and modified to reflect any necessary changes.

DPPM Reduction Program

The primary purpose of a DPPM (Defective Parts Per Million)reduction program is to provide a formalized feedback system in which data from non-conforming products can be used to improve future product consistency and reliability.

Requests for evaluations by customers or first article evaluations or line-fallouts that may be application or test coverage issues are immediately processed through a system called Customer Return for Analysis.

The action portion of this program is accomplished in three stages:

1. Identification of defects by verification of failure and failure mode analysis.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

Customer Business Review

Partnership with customer is encouraged through a periodic business review program. The customer and SPG's operational groups, including the Quality Assurance group, meet periodically and review through a score card system, the state of the products and services.

Product Verification, Design Reviews and Process Change Notifications Notification

Product Quality Assurance is involved in the verification of the readiness of products to market at various stages of the design process as well as in the qualification of the process technologies. Process Changes Notification is also done through this group.

Product Alert, through a database created by the Marketing group, is used to alert the operational groups and field sales for any information relative to product application.

QUALITY ASSURANCE IN DESIGN / PROCESS DEVELOPMENT

SPG's strategy of continuously reducing the time to volume for new products is based on the use of concurrent engineering methodology (i.e. simultaneous product, technology and support systems development). For concurrent engineering to be successful, the tasks involved have to be clearly identified and partitioned, and close coordination among the organizations involved must take place.

For products utilizing a new technology, each phase requires 6 concurrent processes to take place:

#1 - Wafer Fabrication Process Development

#2 - Design Tools Development

#3 - Product Development

#4 - Process Technology Specification Development

#5 - Design Manual Development

#6 - Wafer Fabrication Process Qualification

Wafer Fabrication Process Development, Qualification, and Technology Specifications

The development of a wafer fabrication process consists of the integration of a series of manufacturing steps, some of which may need to be developed, and all of which exhibit some amount of normal variation. The integration of these manufacturing steps has as its aim the fabrication of a target set of devices and its associated set of layout rules. The Process, set of devices, and layout rules are interdependent and their definition must support the design and manufacture of products with competitive performance, reliability, and cost.

The specification targets and limits are set conservative enough to accommodate the uncertainties anticipated during the development and revised eventually to reflect the final wafer process developed and qualified.

These specification targets and limits are the basis for product design rules and design limits.

The process Technology Specification

- describes the wafer process,
- establishes the physical and electrical requirements,
- establishes some of the criteria for qualifying the wafer process,
- establishes the criteria for accepting production wafers,
- forms the basis for product design rules and design limits,
- becomes part of the Design Manual for a given process technology.

QUALITY ASSURANCE IN MANUFACTURING

A key to quality in IC manufacturing is Statistical Process Control. SPG has been immersed in this process for the last ten years; using the JEDEC 19 framework in the last two years. The IC industry has been very attached to the Military Standards 883 and 38510 for the last 20 years, and this has resulted in the establishment of "Product Inspection Gates" throughout the IC manufacturing process. It is timely that SPC is beginning to provide process control data in lieu of inspection steps/gates as a means of ensuring sustained product quality.

The other key is consistent documentation for requirements and procedures. This standardizes the operation steps, product traceability, data collection activity and nonconformity or abnormality control.

Incoming Inspections/Certfied Supplies

Incoming inspection plays a key role in SPG's quality efforts. Small variations in incoming material can traverse the entire production cycle before being detected much later in the process. By paying strict attention to the monitoring of materials at the earliest possible stage, variation can be reduced, resulting in a stable uniform process.

Through the supplier certification process, the manufacturing Quality Assurance groups, develop confidence in the stability of the process by evaluating key commodities' supplier processes. This reduces the need for incoming inspections without increasing the risks.

In-Process Inspections

SPG has established key inspection monitors in the following strategic areas: wafer fabrication, wafer probe, assembly, and final test.

Quality control monitors have been integrated throughout the manufacturing flow so that data may be collected and analyzed to verify the results of intermediary manufacturing steps. This data is used to document quality trends or long term improvements in the quality of specific operations.

Abnormality control is being used to enhance the effectiveness of this process. In process monitors such as oxide integrity, electromigration immunity and other parameters monitor long term reliability as well as circuit performance.

As stated in the introductory section, Statistical Process Control has replaced a number of Quality Assurance steps, giving the operations group the responsibility to collect data, analyze trends and stop an out-of control process and taking actions where required, or Out-of Control Action Plan (OCAP).

PPM Reduction Program

Within the manufacturing process the primary purpose of a PPM reduction program is to provide a formalized feedback system in which data from non-conforming products can be used to improve future product consistency and reliability. Similar to the Customer Request for Analysis, this early warning step takes the form of three stages:

1. Identification of defects by failure mode.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

The data summarized from the established PPM program is compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of defective parts per million (PPM).

Computer Aided Manufacturing Control

Computer Aided Manufacturing (CAM) is used throughout SPG for the identification, control, collection and dissemination of timely information for logistics control. SPG also uses this type of computerized system for statistical process control and manufacturing monitoring. PROMIS (PROcess Management and Information System) displays approved/controlled recipes, processes, and procedures; tracks work-in-process; reports accurate inventory information; allows continuous recording of facilities data; contains statistical analysis capabilities; and much more. PROMIS allows for a paperless facility, a major element in minimizing contamination of clean room areas.

RELIABILITY

Reliability Program

A primary objective at SPG is to improve the reliability of our products through characterization of our manufacturing operations. The identification of specific failure mechanisms occurring in the wafer fabrication and assembly processes is prerequisite to effective corrective action aimed at reducing defects and improving quality and reliability.

SPG has defined various programs that will characterize product reliability levels on a continuous basis. These programs can be categorically described by:

1. Qualifications
2. Product monitors
3. Evaluations
4. Failure analysis
5. Wafer level reliability
6. Data collection and presentation for improvement projects

Qualifications

Criteria used are periodically reviewed to be consistent with quality requirements extensive qualification testing and data collection ensures that all new product designs, processes, and packaging configurations meet the absolute maximum ratings of design and the worst case performance criteria for end users. A large database generated by means of accelerated stress testing results in a high degree of confidence in predicting final use performance. The qualification process focuses on increasing quality and reliability goals in support of our customers.

Product Monitors (Ongoing Reliability Monitors)

This program has been established to randomly select a statistically significant sample of production products for subjection to maximum stress test levels in order to evaluate the useful life of the product in a field use environment.

The accelerated stress test methods are defined in section 9.8 . This analysis of production monitor at SPG provides valuable information on possible design/ process changes which assure continued improved reliability. The monitors are periodically reviewed for effectiveness and improvements.

Evaluations

The evaluation program at SPG is an ongoing effort that defines standards which address the reliability assessment of the circuit design, process parameters, and package of a new product. This program continuously analyzes updated performance characteristics of product as they undergo improvement efforts at SPG.

Failure Analysis

The failure analysis function is an integral part of the Quality and Reliability department at SPG. SPG has assembled a highly technical and sophisticated failure analysis laboratory and staff. This laboratory provides visual analysis, electrical reject mode analysis, and both destructive and non-destructive data to aid the engineers in developing corrective action for improvement. These test analyses may include metallurgical, optical, chemical, electrical, SEM with X-ray dispersive analysis, and E-Beam non-contact analysis as needed.

These conclusive in-house testing and analysis techniques are complemented by outside support, such as scanning acoustic microscopy, focused ion beam, and complete surface and material analysis. This allows SPG to monitor all aspects of product manufacturing to ensure that the product of highest quality is shipped to our customers.

Wafer Level Reliability Program

The primary advantage of wafer level reliability testing is the speed at which results can be derived, thereby providing additional response time and an early warning of process changes. This tool provides SPG with a very rapid analysis tool which allows for the early identification of possible problems and a determination of their origin.

The continuous improvement approach taken at SPG uses wafer level reliability tests as tools to improve the process, identify potential problems, determine the sources of any process weakness and eliminate problems upstream in the process. This results in a focus on reliability improvement that goes well beyond merely determining the projected lifetime of a product to a detailed characterization, measurement and control of the specific parameters which actually determine product lifetime.

Data Collection and Presentation for Improvement Projects

Data collected from each element of the Reliability program is summarized for scope and impact and distributed among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review the performance of our product.

Reliability Methods

The Reliability program utilizes a number of stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per spec 37.18Y 189, Storage Products Reliability Requirements.

RELIABILITY PREDICTION METHODOLOGY

At SPG, the Arrhenius model is used to relate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states FR = A exp(-Ea/KT)

Where:

FR = Failure rate

A = Constant

Ea = Activation Energy (ev)

K = Boltzmann's constant 8.62 • 105eV/°K

T = Absolute temperature (°K)

Electronic Discharge (ESD)

SPG recognizes that the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity is vital. ESD safe procedures are incorporated throughout all operations which come in contact with these devices. Continuous improvement in the ESD protection levels is being accomplished through the incorporation of increasingly robust protection devices during the circuit design process as well as work area improvements.

SPG's quality activity incorporates several protection measures for the control of ESD. Some of the preventive measures include handling of parts at static safe-guarded workstations, the wearing of wrist straps during all handling operations, the use of conductive lab coats in all test areas and all areas which handle parts and the packaging of components in conductive or anti-static containers.

QUALITY SYSTEMS

ISO 9000 Based Quality Systems

Successful implementation of ISO 9001 and 9002 standards was accomplished with knowledgeable and motivated people who understand the requirements and ultimate objectives.

The SPG Business Process & Quality System Manual (BPQSM) started as a framework to guide the implementation process. Now the BPQSM is clearly the repository of the basic goals and commitment of SPG to quality as measured against an International Standard and as aligned with customer expectations.

More and more customers are looking at a certified Quality Systems Management. The company has chosen to exceed the expectations by continually driving improvements beyond the minimum requirements.

Management Review Process and the Business Excellence Roadmap

In the area of management review, the company conducts three types of sessions or processes.

The first type is the Executive Staff review of business excellence practices and achievements to customer measures: product timeliness in the market, quality in products and service, and dependable growth in technology and capability. This is done initially as an annual Strategic Review, then quarterly, as milestone operations reviews.

The second type, focuses on Operation or Site reviews, which focus on the Key Tactics for meeting business and customer goals.

The third type which is set as an annual review, looks at the Quality Systems as it is deployed throughout the organization and a comparative look at its relevance and effectiveness. In this third type, the review focuses on Quality Systems audit results, business metrics and departmental/organizational plans for improvement of quality systems.

Company-Wide Corrective Action System

The Corrective Action system (CA) is designed to establish a company-wide system to handle customer complaint, product, process and quality system non-compliances. The goal of the CA system to implement the corrective action needed to eliminate the cause of the nonconformities.

Each functional element of the organization uses a common system in identifying problem, analyzing root cause and implementing preventive actions towards the elimination of the external customer complaints, product nonconformities, process and quality system deficiencies. Containment action is necessary to prevent possible problems.

CA system is also a tool used by the internal auditors to document nonconformities found during an audit. It is the responsibility of all employees to oversee that corrective actions are implemented. The Management Representative and QAS Director is responsible in the monitoring that the implementation of corrective actions are implemented according to the documented guidelines.

Company-Wide Audits

Internal audit system is designed to measure the effectiveness of quality system. It is also a tool used by the management to continuously improve the organizational performance. The management use the aid of internal auditors to assess the effectiveness of the documented quality system.

At prescribed interval, auditors are deployed. With the directive from Audit Review Board (ARB), the auditors are assigned to functional areas to assess compliance to the SPG Business Process & Quality System Manual and SOPs. All auditors are trained according to the SPG's quality system and internal audit guideline. The Management Representative and ARB chairperson oversee the effectiveness of the internal audit. Internal audit is scheduled according to is significance or need. At the conclusion of the audit, reports are generated and reported to the management by the management representative during management review.

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HDD READ/WRITE AMPLIFIERS

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Texas Instruments

Die Sales
Flip Chip Policy

February1999

DIE PRODUCT INFORMATION

GENERAL

Texas Instruments Storage Products provides selected devices in bare die or bumped die form. 100% of the dice are electrically tested at wafer probe prior to separation into individual die. Each die is visually inspected at 100X magnification using Texas Instruments Storage Products' standard visual criteria. The dice are packaged into waffle-pack carriers with an anti-static shield and cushioning strip placed over the active surface to ensure protection during shipment. Orientation of each die is the same in each waffle pack to facilitate pick-and place operations. See Attachment 1 for Die Process Flow Chart.

TESTING

A number of packaged product specifications can not be tested at the wafer level or at the package level, and some probed parameters may shift when the die is subjected to the stresses of the assembly and encapsulation process. However, it is Texas Instruments Storage Products' intent to provide dice tested to levels that can be expected to yield the same high quality results as our packaged parts. Probe testing can be performed to either a standard or an enhanced level as follows:

a. Standard Probe Test

100% of the die are probed using the same tests used for dice that would be packaged by Texas Instruments Storage Products.

b. Enhanced Probe Test

100% of the die are probed using the same tests as the packaged parts final test, as much as is practicable.

QUALITY CONTROL

QUALITY LEVEL

Each dice lot is guaranteed to meet:

1) Conformance to Texas Instruments Storage Products visual inspection criteria to a 0.065% AQL.

2) Conformance to the probe test level requested. If subjected to the same loading and test conditions, correctly assembled die should provide packaged product performance over the rated junction temperature range indicated on the data sheet.

RELIABILITY ASSURANCE

Texas Instruments Storage Products' (Silicon Systems') standard processing procedure includes ongoing Wafer Level Reliability (WLR) testing performed on a monitoring basis. These tests are designed to correlate to the fabrication process reliability and they provide a rapid analysis tool for early detection of problems and their cause. Monitor frequency, sample size, and test methods are determined by Corporate Reliability Engineering. The continuous improvement approach taken at Silicon Systems makes use of such tools to improve the process. This results in a methodology that focuses on upstream improvements to the process and controlling of the parameters which affect product lifetime.

QUALITY CONTROL (continued)

OPTIONS AVAILABLE

Contact Texas Instruments Storage Products for availability and pricing of the following:

1. Lot Acceptance Testing based on sample testing is offered at extra cost which will depend on the sample size and tests required. See Attachment 2 of a possible Lot Acceptance Test Flow.

2. Enhanced level probe testing as described above.

3. Tape and reel packaging.

4. Back grinding of bare die to other than the standard thickness. Minimum wafer thickness is 13.5 mils.

PHYSICAL CHARACTERISTICS

DIE THICKNESS

The standard thickness of Texas Instruments Storage Products dice is 21 ± 1 mils. The backside is unplated. For wafer bumped, die the bumps project 100 ± 16 microns from the surface on bumped die, with a coplanarity of 20 microns within each die.

DIE DIMENSIONS

The tolerance on length and width is ± 0.5 mil.

BONDING PADS/BUMPS

Minimum bare die pad dimensions are 4.0 mils by 4.0 mils of Al /1% Cu with 3.5 mil minimum passivation windows. Minimum bumped die pad dimensions are TBD.

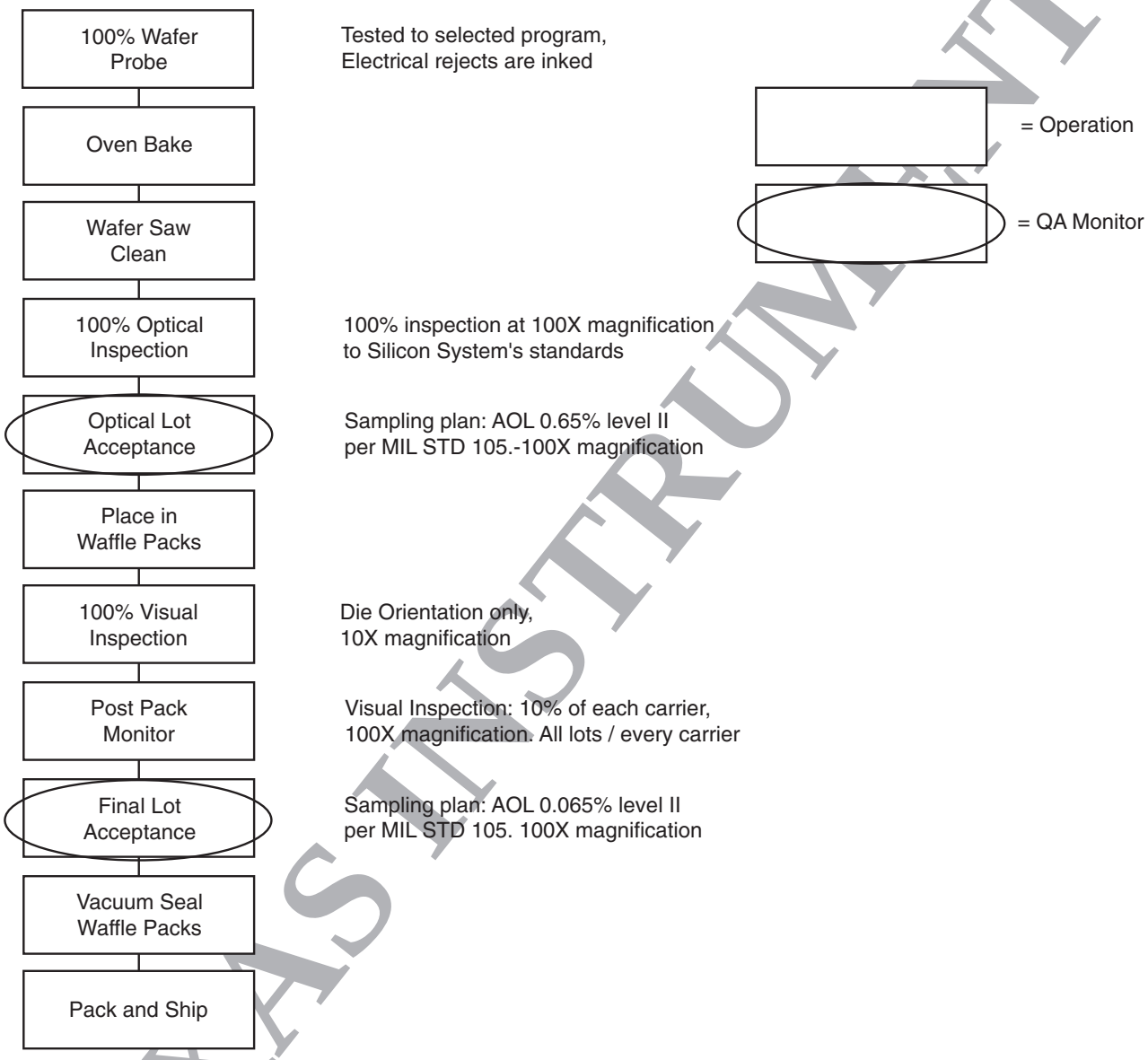
OTHER

Contact Silicon Systems for any additional information . Pad / bumped pad coordinates, test coverage and visual inspection criteria information will be provided upon request.

The reader is cautioned to verify that the information is current.

ATTACHMENT 1

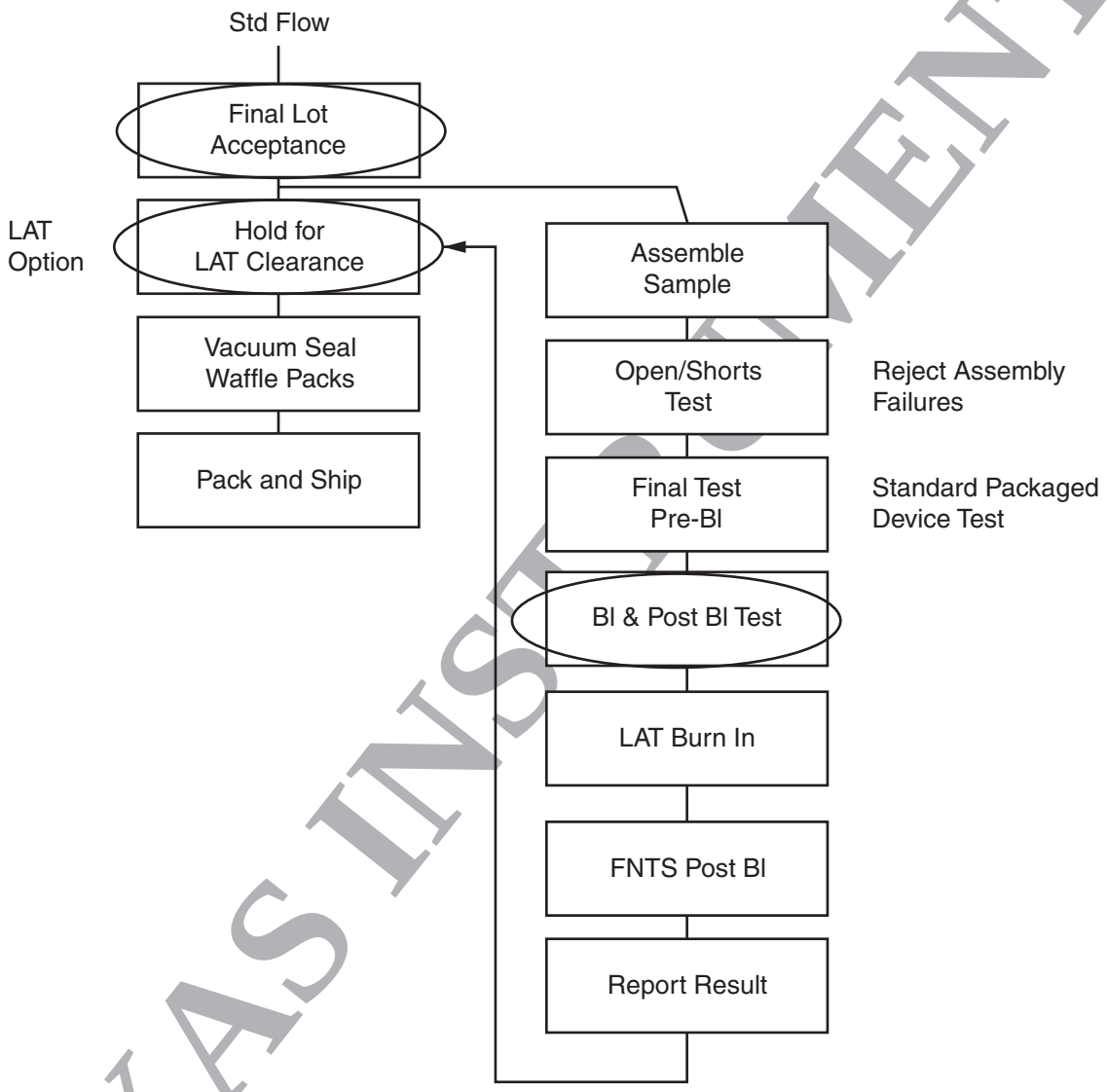
Bare & Bumped Die Sales Process Flow Chart



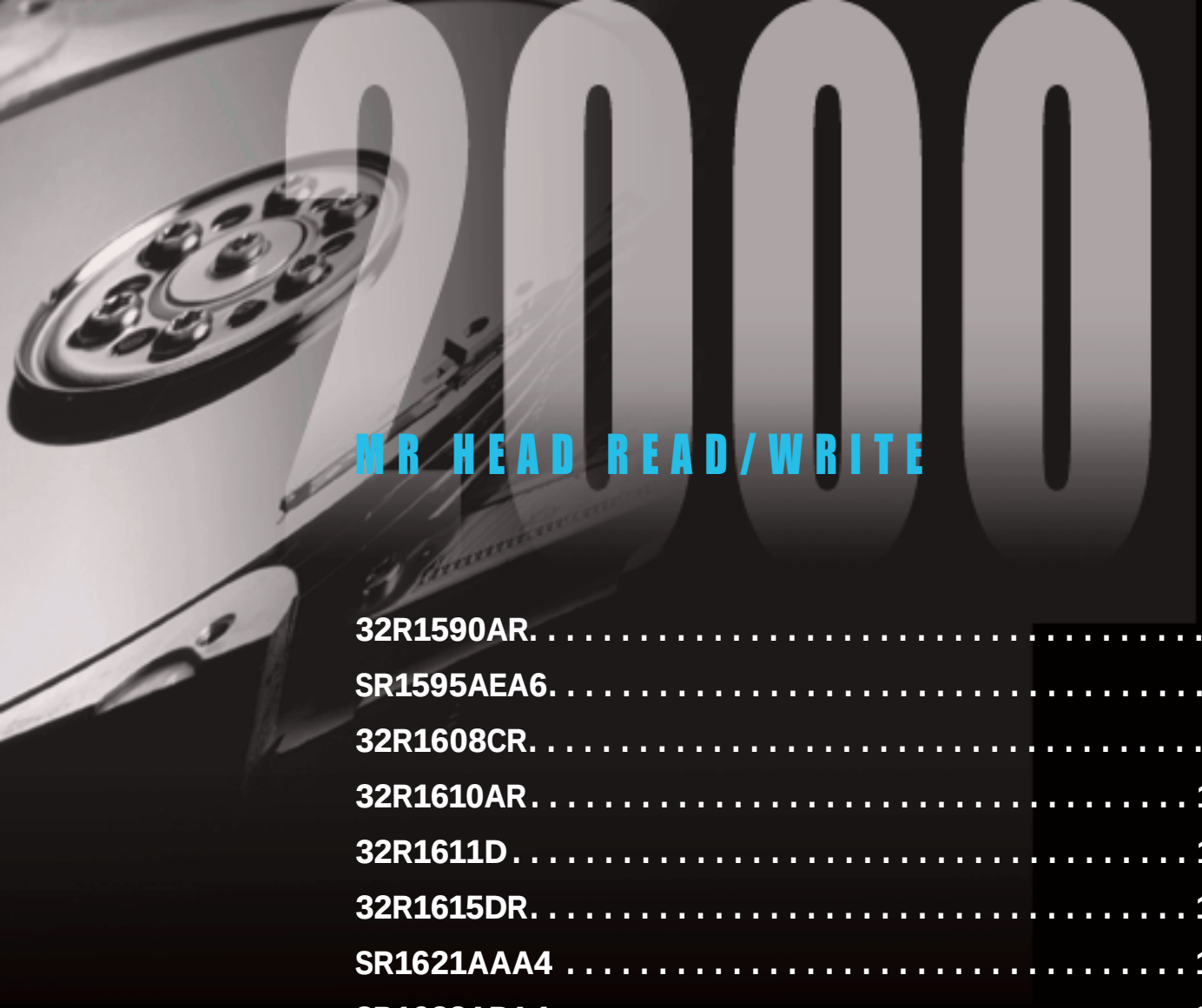
ATTACHMENT 2

Lot Acceptance Test Flow Example (Bare Die)

(available at additional cost)



Die Sample must be large enough to result in agreed number of samples for Final Test following opens / shorts test.



2000

MR HEAD READ/WRITE

*Data sheet available upon request

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32R1590AR
+5/-5V 10-CHANNEL MR PREAMPLIFIER IC

May, 2000

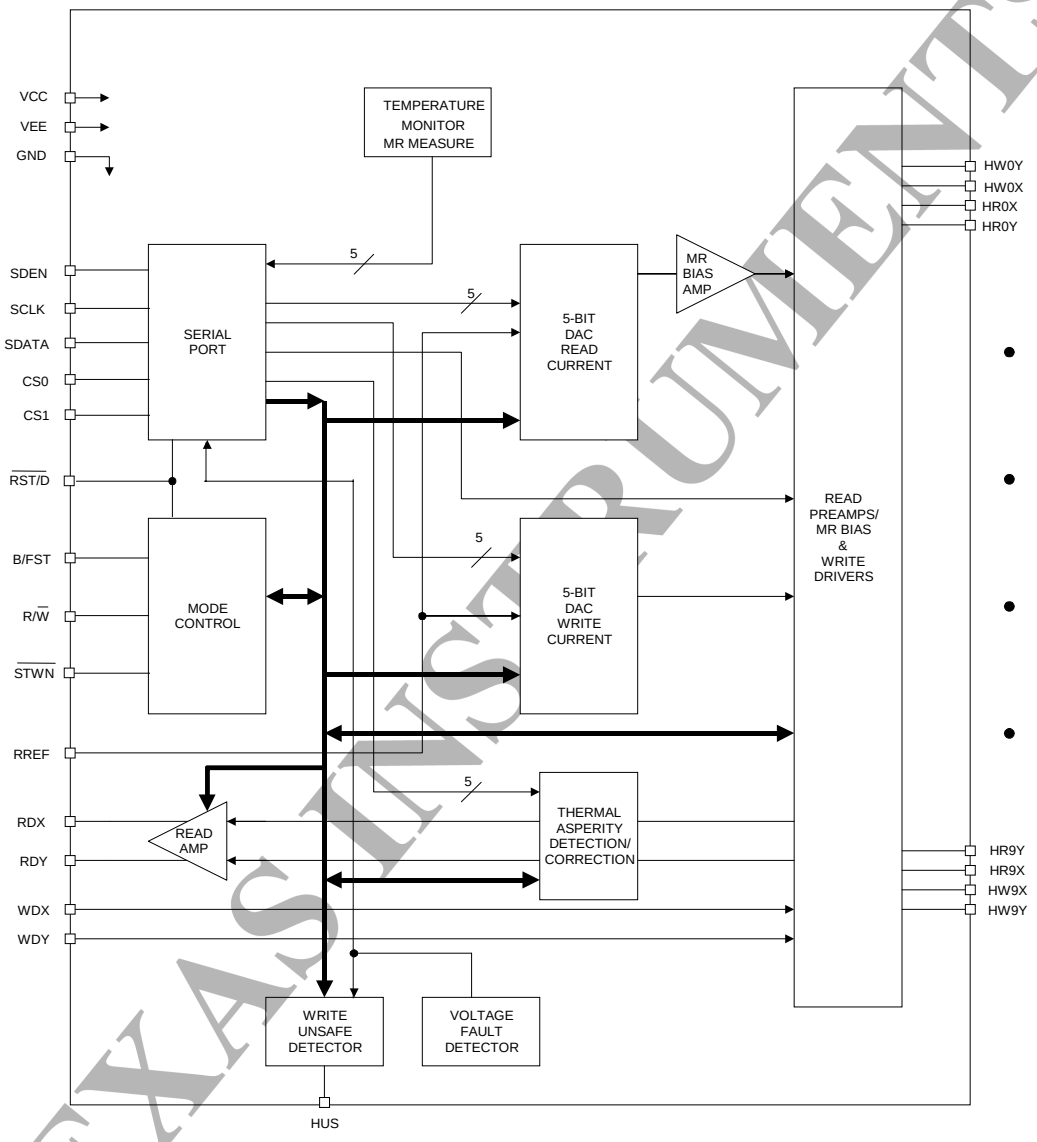
DESCRIPTION

The TI/SPG *32R1590AR* is a BiCMOS monolithic integrated circuit designed for use with 10 four-terminal Magneto-Resistive recording heads. It provides a write driver, low noise read amplifier and MR current bias with serial port controlled head selection, servo track write, write current, MR read bias current and fault detection circuitry. In servo write mode, 5 channels each can be separately selected. The device requires +5V and -5V and comes in a 100-pin TQFP package or as bumped die.

FEATURES

- **+5V ±10%, -5V ±5% supplies**
- **Designed for four-terminal MR heads**
- **Requires only one external resistor**
- **Truly differential current bias / voltage sense MR read Amplifier**
- **MR head bias current range = 4 -10 mA**
- **GMR head bias current range = 3.5 - 5 mA**
- **MR head resistance range of 45-85Ω**
- **Programmable MR read gain (150, 200, 250, or 300 V/V)**
- **Programmable voltage BW (Typ, 150 MHz - 225 MHz)**
- **MR read input noise = 0.5 nV/√Hz (Typ, Rmr=0Ω)**
- **MR read input current noise = 6pA/√Hz @ 6.4 mA (Typ)**
- **MR read input resistance = 1K Ohm (Typ)**
- **Programmable write data input - PECL or Current Mode**
- **Head voltage swing = 16 Vp-p (Typ)**
- **Head Current risetime of 0.9 ns (Typ, Iw=40mA, Ltot=100nH, RH=12Ω)**
- **Programmable write damping control**
- **Write current range = 13.5 - 53.5 mA**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Read/Write serial port controls head selection, write current, write damping, MR head bias current, thermal asperity threshold and mode, read gain, low power idle and sleep mode selection.**
- **Automatic MR head resistance measurement mode**
- **Low Bandwidth read gain test mode**
- **Thermal asperity detection and compensation**
- **MR head capacitive discharge protection**
- **On chip Temperature Monitor**
- **40 MHz Serial Interface**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 32R1590AR addresses up to 10 four-terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with the R/$\overline{W}$ pin and the serial port as shown in Table 1. All inputs, except the serial port, BFST and $\overline{RST}$/$\overline{D}$, have internal pull-ups so that when left open, they will default to the HIGH state. The three serial port i/o pins, BFST and $\overline{RST}$/$\overline{D}$ have internal pull-downs.

The serial data port is used to control chip selection, head selection, servo track write, write current, write damping control, MR head resistance measurement, MR bias current, read gain, thermal asperity threshold and mode.

CHIP SELECTION

The chip is selected during a serial port transfer by sending address bits, A0 and A1, that match the logic levels of the chip's chip select pins, CS0 and CS1. Address 1,1 is reserved for broadcast mode. The logic levels of CS0 and CS1 are ignored when the chip receives a serial port transaction with A0 and A1 set to 1, enabling all preamps on the serial bus to be written to with one serial data transfer.

SERIAL PORT

A complete data transfer is sixteen (16) bits long: one R/$\overline{W}$ bit, seven (7) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded before data. The first bit is the serial port R/$\overline{W}$ bit which is HIGH for a read operation or LOW for a write operation. The next two bits (A0-A1) are the device select bits and should match the state of the CS0 and CS1 pins. The following five bits (A2-A6) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map for more information)

Asserting the serial port data enable line, SDEN, initiates a transfer. SDATA is clocked into the internal shift register by the rising edge of SCLK. A counter on the device ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted, otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

SERIAL PORT WRITE TIMING

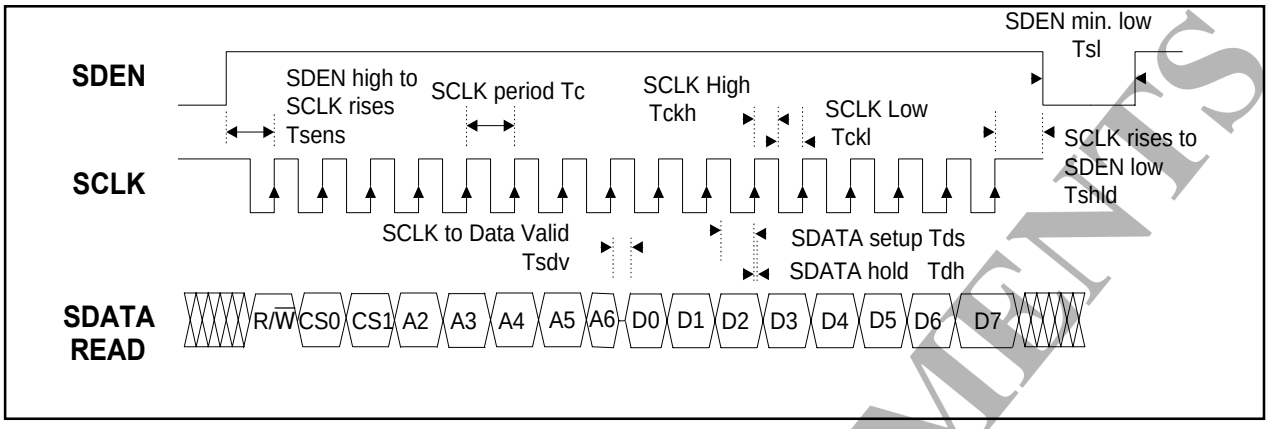


FIGURE 2: Serial Port Timing Diagram – Write

SERIAL PORT READ TIMING

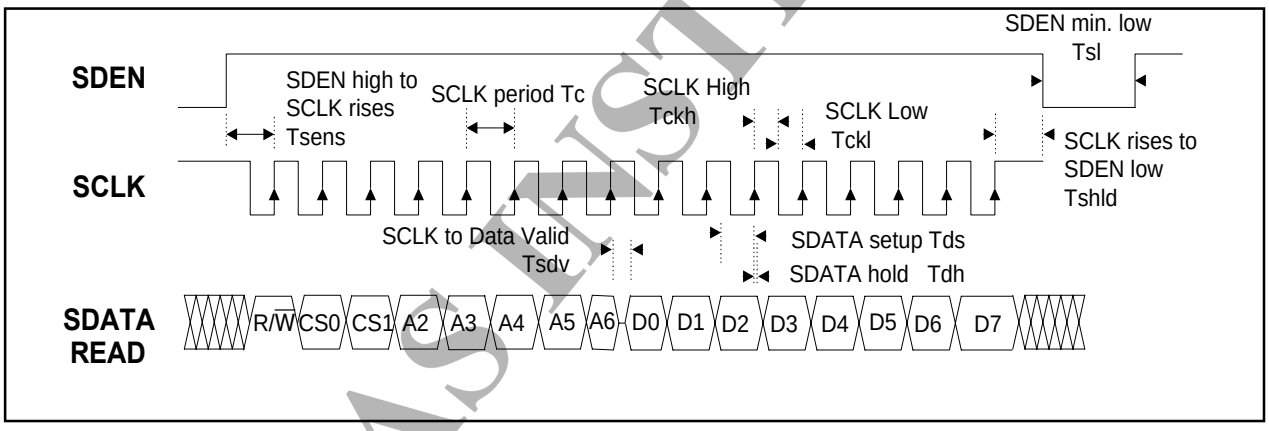


FIGURE 3: Serial Port Timing Diagram - Read

TABLE 1: Mode Selection

MODE	Pin R/W	Sport Reg 9 MODE1	Sport Reg 9 MODE0	Sport Reg 8 MRR	Sport Reg 8 TMF	Sport Reg 9 RST/DMY	Pin RST/D	Pin STWN	Sport Reg 2 DUMMY
Reset	x	x	x	x	x	0	0	x	x
Dummy	x	x	x	x	x	1	0	x	x
	x	x	x	x	x	x	1	x	0
SLEEP	x	0	0	0	0	0	1	x	x
IDLE	x	0	1	0	0	0	1	x	x
READ	1	1	0	0	0	0	1	x	x
WRITE	0	1	0	0	0	0	1	x	x
MR Measure	1	1	0	1	0	0	1	x	x
Temp Measure	x	1	0	0	1	0	1	x	x
SERVO WRITE	0	1	1	0	0	0	1	0	x

RESET

The device enters reset mode when the $\overline{RST}/\overline{D}$ pin is pulled LOW AND the $\overline{RST}$/DMY bit of reg 9 is 0. In reset mode, all registers are reset to their POR defaults, and the device enters SLEEP mode.

SLEEP MODE

This is the default power-on mode. The device enters sleep mode when the mode control bits of register 9 are set to 00 or a reset signal is received. In sleep mode, only the serial port of the device is active. The device may be brought out of sleep mode by setting the mode control bits in register 9 to idle , active read or write, or servo track write.

IDLE MODE

The device enters idle mode when register 9 mode control bits are programmed to 01. In idle mode, the device is inactive, but many blocks of the device are biased in preparation for switching to read or write mode. The device may be brought out of idle mode by writing register 9 mode control bits to sleep, active read or write, or servo track write.

READ MODE

The device enters Read Mode based on conditions described in Table 1 of Mode Selection Section. In Read Mode, gain is set to one of four values based on GAIN0-GAIN1 bits of register 2.

The HUS output is HIGH (open collector) in this mode unless a thermal asperity is detected, which causes the output to go LOW.

The outputs of the read amplifier RDX and RDY are emitter followers and are in phase with the voltage change at the selected input ports HRnX and HRnY where the respective MR head is attached. Current necessary for biasing the MR sensor is internally programmed by a 5 bit DAC via the serial port. The magnitude of the bias current is given by:

$$I_{MR} = 4mA + \frac{M}{31} 6mA$$

where M is the decimal value of IMR0-IMR4 (register 2 of serial port) and the GMR bit of Register 1 = 0. When the GMR bit is set to 1, the bias current is given by:

$$I_{MR} = 2mA + \frac{M}{31} 3mA .$$

NOTE: I_{MR} is only functional from 3.5mA to 5mA in the low current range.

In Read mode, the voltage at the midpoint of the selected MR head is forced to the ground potential. For the unselected MR heads, the head ports are pulled to ground by a low impedance and thus will prevent the heads from conducting current in the event of head to disk contact.

To improve the Write to Read recovery time, the MR bias current is maintained in Write mode.

The MR bias current is removed from the MR element when Dummy Mode is selected. Dummy mode is selected by either programming the DUMMY bit in Reg 2 to LOW, or setting the $\overline{\text{RST}}$/D pin LOW when the $\overline{\text{RST}}$/D pin is enabled by programming the $\overline{\text{RST}}$/DMY bit of Reg 9 (Dummy Pin enable) HIGH.

The MR bias can be forced to remain on and the read amplifier outputs active during WRITE mode by programming the ROUTON bit HIGH in Reg 1.

WRITE MODE

The device enters Write Mode based on conditions described in Table 1 of the Mode Selection Section.

The HUS output is LOW in this mode unless there is a write fault, which causes the output to go HIGH.

Selecting Write mode generates a write current from the internal 5 bit DAC, set by the serial port, and activates the Write Unsafe (WUS) detect circuitry. Head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each transition of the differential PECL signal WDX-WDY. When WDX>WDY I_W flows from X to Y.

The magnitude of the current (0-pk) is given by:

$$I_W = 13.5mA + 40mA \frac{N}{31}$$

where N is the decimal value of IW0-IW4 bits of the serial port register 4.

Note that the actual head current Ix,y is given by:

$$I_{x,y} = \frac{I_W}{1 + \frac{R_h}{R_d}}$$

where R_h is the head DC resistance and R_d is the damping resistance.

Programmable damping control is achieved by applying a damping current immediately after the write h-bridge switches. The value of the damping current is given by:

$$I_{DAMP} = 0.5mA + 7mA \frac{N}{7}$$

where N is the decimal value of WCP0-WCP2. This damping current can be translated into an equivalent ac damping impedance by the formula:

$$R_{DAMP} = \frac{10}{\sqrt{I_{\text{DAMP}}}} \Omega$$

SERVO TRACK WRITE MODE

The device enters Servo Track Write Mode based on the conditions described in Table 1 of Mode Selection. To enter Servo Track Write mode, Mode0 and Mode1 bits of Register 9 are set to 1, the $\overline{\text{STWN}}$ pin must be set LOW and the R/$\overline{\text{W}}$ pin must be set LOW. In Servo Track Write mode, the device writes the same signal to multiple write heads. Up to 5 heads may be enabled in Servo Track Write mode. Silicon Systems does not recommend that more than two heads be enabled at the same time due to power dissipation considerations.

The BANK bit of register 10 is used to select the odd or even bank of heads in Servo Track Write mode. Bank is set LOW for even heads and HIGH for odd heads. HD0/1-HD8/9 of Register 10 are used to select the heads active in each bank.

Write unsafe functions are not active in Servo Track Write mode.

READ/WRITE UNSAFE

In read or write mode, any of the following conditions will be indicated as a fault on the Head Unsafe (HUS) open collector output pin and reported in bits FCODE0-FCODE3 of register 7. FCODE0-FCODE3 are NOT latched. Fault codes have the following precedence.

- Low VCC
- Low VEE
- R_{EXT} open or shorted
- Illegal head address selection
- Write head shorted to ground (write mode only)
- Write head open (write mode only)
- WDX/WDY frequency too low (write mode only)
- Die Temperature too high
- MR head voltage too high (800 mV pk-pk differential)
- Write current present while not in write mode

In **read mode**, thermal asperity detection will only be indicated by a LOW level on the HUS output pin in order not to disturb the reader.

In read or write mode, if an illegal head address is received, all heads are unselected and the fault pin is asserted. The serial port registers remain unchanged.

In **write mode**, a power supply low fault will deselect the write current, set the HUS pin to HIGH, and not reset the serial port registers. Upon removal of the power supply fault, the write current bias is re-enabled and the HUS pin is set to LOW.

THERMAL ASPERITY DETECTION AND COMPENSATION

When the read head signal amplitude exceeds a serial port programmable threshold, a thermal asperity hit is detected and the HUS pin will go LOW until the thermal asperity level has dropped to 10-15% above the baseline. The equation describing this threshold is given by :

$$Threshold = 0.4mV + TRANGE * 3mV + 5.6mV\left(\frac{M}{31}\right)$$

(mV pk-pk input referred)

where M is the decimal value of TADT bits of the serial port register 5 (Thermal Asperity Detection Threshold ,TADT) and TRANGE has a value of 0 or 1.

Depending on the value of bits TAC, TAD, and TASD in conjunction with the value of input pin BFST(active HIGH), the device will handle thermal asperity according to the following table:

TABLE 2: Thermal Asperity Detection And Compensation Mode Selection

TASD	TAD	TAC	BFST[3]	Lower BW	HUS Flag	Mode
1	X	X	X	540KHz	No	**"TA Shutdown".**
0	0	0	0	1MHz	No	**"No Compensation"**
0	0	0	1	Serial Port	No	**"Fast"[1]**
0	1	0	0	1 MHz	Yes	**"Detection Only"**
0	1	0	1	Serial Port	Yes	**"Fast w/Detection"[1]**
0	1	1	1	1 MHz / Serial Port	Yes	**"Auto Compensation"[1,2]**

NOTE 1: The equation describing the lower bandwidth -3db frequency is given by :

$$Frequency = 2.5\,Mhz + 7.5\,Mhz\left(\frac{M}{3}\right)$$

where M is the decimal value of LBW0,LBW1 bits of the serial port register 3.

NOTE 2: In Auto Compensation Mode, when a thermal asperity is detected, the lower bandwidth -3db point is automatically shifted to the frequency set by the serial port.

NOTE 3: BFCTL bit in serial port register 1 must be set HIGH.

In **TA Shutdown** mode, the TA circuit is shut down (regardless the value of BFST pin)

In **No Compensation** mode, the TA circuit is powered up, but inactive. The lower bandwidth -3db point is set at 1MHz.

In **Fast** mode, the lower -3db reader bandwidth is shifted from 1MHz to a serial port programmable frequency whenever the asynchronous BFST pin is brought HIGH. When BFST pin is subsequently brought LOW, the pole frequency will immediately return to its original value.

In **Detection Only** mode, thermal asperities will be flagged by bringing the HUS pin LOW, but no compensation will be made.

In **Fast Mode w/Detection**, compensation is made in the same manner as Fast mode, but thermal asperity detection and flagging is also enabled.

In **Auto Compensation** mode, the circuit provides detection and correction without any assistance. After a thermal asperity is detected, the pole frequency is automatically shifted from 1MHz to a programmable frequency determined by the LBW0, LBW1 bits of reg 3. When HUS returns HIGH, the pole frequency is returned to 1 MHz after an additional delay of 1.5us.

MR HEAD RESISTANCE MEASUREMENT FUNCTION

When the device is in read mode and the MRR bit of register 8 is set HIGH, the device will automatically measure the DC resistance of the selected MR head and report the encoded result in bits M0-M4 and RANGE of register 8 after about 200uS.

NOTE: The result in register 8 is only valid if the measurement is made while the device is in READ mode.

The R_{MR} (Ω) can be calculated by the following equation:

$$R_{MR} = \frac{A + B*(M + 1/2)}{I_{MR} * G}$$

where

If M is equal to 0, the voltage across the MR head resistance may be out of range. MRR must be reset to zero before initiating another measurement.

To cover the full range (20 to 90 Ω) of head resistance values, it is recommended that the read head bias current should be at least 6.5mA. Bias current lower than 6.5mA could result in erroneous results for smaller resistance heads.

TEMPERATURE MONITOR FUNCTION

When the TMF bit of register 8 is set HIGH, the device will automatically measure its own die temperature and report the encoded result in bits M0 - M4 of register 8 after about 200uS. Temperature, T is given by:

$$T(^{o}C) = 78 + 2 * M$$

where M is the decimal value of bits M0-M4 of register 8. If M is 0, the device temperature is out of range, i.e., T < 78 °C or T > 140 °C.

NOTE: Operation beyond the absolute maximum rated temperature of 130°C is discouraged, and permanent damage to the device could result.

The temperature monitor function is only guaranteed to be accurate in IDLE mode, but may be used in other modes. TMF must be reset to zero before initiating another measurement.

A (Constant 1)	517.8
B (Constant 2)	32.36
M (Measure register value)	Decimal value of M0-M4 in the serial port
G (Gain of measure amp)	2 if RANGE bit is 0 4 if RANGE bit is 1
I_{MR} (Programmed MR bias current)	Programmed MR bias current (in mA)

TABLE 3: Serial Port Bit Map

Serial Port Data Format: R/$\overline{W}$ CS0 CS1 A2 A3 A4 A5 A6 D0 D1 D2 D3 D4 D5 D6 D7 (where A6 and D7 are MSBs)

						MSB							LSB
Reg	**A6**	**A5**	**A4**	**A3**	**A2**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	X	0	0	0	0	HS3 **0**	HS2 **0**	HS1 **0**	HS0 **0**	X **0**	X **0**	LCS1 **0**	LCS0 **0**
1	X	0	0	0	1	ROUTON **0**	X **0**	GMR **0**	X **0**	X **0**	X **0**	WVORI **0**	BFCTL **0**
2	X	0	0	1	0	DUMMY **0**	IMR4 **0**	IMR3 **0**	IMR2 **0**	IMR1 **0**	IMR0 **0**	GAIN1 **0**	GAIN0 **0**
3	X	0	0	1	1	X **0**	X **0**	X **0**	X **0**	HBW1 **0**	HBW0 **0**	LBW1 **0**	LBW0 **0**
4	X	0	1	0	0	IW4 **0**	IW3 **0**	IW2 **0**	IW1 **0**	IW0 **0**	WCP2 **0**	WCP1 **0**	WCP0 **0**
5	X	0	1	0	1	TRANGE **0**	TAD **0**	TAC **0**	TADT4 **0**	TADT3 **0**	TADT2 **0**	TADT1 **0**	TADT0 **0**
6	X	0	1	1	0	VEND7 **0**	VEND6 **0**	VEND5 **0**	VEND4 **0**	VEND3 **0**	VEND2 **0**	VEND1 **0**	VEND0 **1**
7	X	0	1	1	1	FLT3 **0**	FLT2 **0**	FLT1 **0**	FLT0 **0**	FCODE3 **0**	FCODE2 **0**	FCODE1 **0**	FCODE0 **0**
8	X	1	0	0	0	M4 **0**	M3 **0**	M2 **0**	M1 **0**	M0 **0**	RANGE **0**	TMF **0**	MRR **0**
9	X	1	0	0	1	X **0**	X **0**	X **0**	X **0**	X **0**	RST/DMY **0**	MODE1 **0**	MODE0 **0**
10	X	1	0	1	0	X **0**	X **0**	HD8/9 **0**	HD6/7 **0**	HD4/5 **0**	HD2/3 **0**	HD0/1 **0**	BANK **0**
15	X	1	1	1	1	TASD 0	Res 0	Res 0	Res 0	Res 0	Res 0	Res 0	Res 0

NOTE: Bits in table are not in the same order as bits written to the serial port for enhanced readability.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A5, A4, A3, A2. Serial port Read/Write and CS1, CS0 bits are not shown.

REGISTER 0
Address = 0000

BIT	NAME	DESCRIPTION
7:4	HS3:0	Head select bits.
3:2	X	Not used
1:0	LCS1:LCS0	Reports state of CS1/CS0 pins

REGISTER 1
Address = 0001

BIT	NAME	DESCRIPTION
7	ROUTON	1 = Reader ON during all modes 0 = Reader output OFF during write
6	X	Not Used
5	GMR	Rmr bias Range control 1 = Ibias range = 2 – 5 mA 0 = Ibias range = 4 – 10 mA
4:2	X	Not Used
1	WVORI	Write data input mode control 1 = Current mode write data input 0 = Voltage mode write data input
0	BFCTL	Bias/Fast (BFST) pin mode control 1 = BFST pin controls reader low corner frequency BFST = 1 = Raises low corner frequency BFST = 0 = Normal low corner frequency 0 = BFST pin controls reader bias BFST = 1 = MR bias current is OFF BFST = 0 = MR bias current is ON

REGISTER 2
Address = 0010

BIT	NAME	DESCRIPTION		
7	DUMMY	Dummy mode control 1 = Internal dummy load inactive 0 = Internal dummy load active		
6:2	IMR4:IMR0	Reader MR bias current DAC. Bias range set by GMR bit (Reg 1) When GMR = 1, range is 2 – 5 mA. Bias equation is: $I_{MR} = 2mA + \frac{M}{31}3mA$, where M is the decimal value of IMR. NOTE: MR biasing is non-functional below 3.5mA When GMR = 0, range is 4 – 10 mA. Bias equation is: $I_{MR} = 4mA + \frac{M}{31}6mA$, where M is the decimal value of IMR.		
1:0	GAIN1:0	GAIN1	GAIN0	Reader Gain
		1	1	300 V/V
		1	0	250 V/V
		0	1	200 V/V
		0	0	150 V/V

REGISTER 3
Address = 0011

BIT	NAME	DESCRIPTION		
7:4	X	Not Used		
3:2	HBW1:0	Reader high frequency bandwidth control		
		HBW1	HBW0	Frequency
		1	1	225 MHz
		1	0	200 MHz
		0	1	175 MHz
		0	0	150 MHz
1:0	LBW1:0	Reader low frequency bandwidth in Fast mode		
		LBW1	LBW0	Frequency
		1	1	10 MHz
		1	0	7.5 MHz
		0	1	5.0 MHz
		0	0	2.5 MHz

REGISTER 4
Address = 0100

BIT	NAME	DESCRIPTION
7:3	IW4:IW0	Write Current DAC, 13.5 mA to 53.5 mA. DAC equation: $I_W = 13.5mA + 40mA\frac{N}{31}$, where N is the decimal value of IW.
2:0	WCP2:WCP0	Write damping Control. Equation: $I_{DAMP} = 0.5mA + 7mA\frac{N}{7}$, where N is the decimal value of WCP2:0.

REGISTER 5
Address = 0101

BIT	NAME	DESCRIPTION
7	TRANGE	Thermal Asperity threshold range 1 = 3.4 = 9.0 mV pk-pk input referred 0 = 0.4 – 6.0 mV pk-pk input referred
6	TAD	Thermal Asperity Disable 1 = Disable Thermal Asperity
5	TAC	Thermal Asperity Compensation Disable 1 = No TA compensation
4:0	TADT4:0	Thermal Asperity Threshold DAC. Threshold equation: $Threshold = (0.4mV + TRANGE * 3mV) + 5.6mV\left(\frac{M}{31}\right)$, Where M is the decimal value of TADT4:TADT0

REGISTER 6 (READ ONLY)
Address = 0110

BIT	NAME	DESCRIPTION							
7:0	Vendor Code	Revision			Device ID		Texas Instruments		
		0	1	1	0	0	0	0	1

REGISTER 7
Address = 0111

BIT	NAME	DESCRIPTION	
7:4	FLT3:FLT0	Fault reporting mode	
		FLT3:FLT0	Faults reported
		0000	Report all faults
		1XXX	Disable open or shorted write head faults
		X1XX	Disable supply voltage out of range faults
		XX1X	Disable MR head overvoltage fault
		XXX1	Disable Temperature fault
		1111	Disable all faults
3:0	FCODE3:0	Fault report code. See Fault reporting Table 4	

Table 4. Fault reporting codes

Fault No	FCODE3:0	Precedence	Reason	Conditions
	0000			No fault
1	0001	10	Iw present while not in write mode	
2	0010	9	MR head voltage too high	Read mode only
6	0110	7	WDX/WDY frequency too low	Fwdx/y < 2 MHz write mode only
7	0111	6	Write head open	Write mode only
8	1000	5	Write current too low	Write mode only
9	1001	3	Rext open or shorted	
11	1011	1	Low Vcc	VCC < 3.9 V typ
12	1100	2	Low Vee	Vee > -3.9 V typ
13	1101	4	Illegal head selection	
15	1111	8	Temperature too high	Tj > 145°C

REGISTER 8
Address = 1000

BIT	NAME	DESCRIPTION
7:3	M4:M0	Measurement value for MR head resistance measurement or temperature monitor mode.
2	RANGE	MR head resistance measurement range.
1	TMF	Temperature monitor function 1 = Enable Temperature monitor
0	MRR	MR resistance measurement 1 = Enables MR resistance Measurement mode

REGISTER 9
Address = 1001

BIT	NAME	DESCRIPTION		
7:3	X	Not Used		
2	RST/DMY	Reset/Dummy (RST/D) pin mode control 1 = RST/D pin controls dummy mode RST/D = 1 = Normal bias mode RST/D = 0 = MR bias is removed from selected head 0 = RST/D pin controls reset function RST/D = 1 = Normal mode RST/D = 0 = Chip enters Reset mode		
1:0	MODE1:0	Mode Control		
		MODE1	MODE0	Device Mode
		1	1	Servo Track Write
		1	0	Active Read/Write mode
		0	1	Idle Mode
		0	0	Sleep Mode

REGISTER 10
Address = 1010

BIT	NAME	DESCRIPTION
7:6	X	Not Used
5:1	HD8/9:HD0/1	Selects write heads to be active in Servo Track Write Mode
0	BANK	ANDed with STWN pin = LOW to enable odd or even heads that are selected with the HDn/m bits for servo writing in Servo Track Write Mode 1 = Select odd heads 0 = Select even heads

REGISTER 15
Address = 1111

BIT	NAME	DESCRIPTION
7	TASD	Thermal Asperity Shut-down 1 = Enable bypass of TA circuitry
6:0	Res	Reserved for TI internal use. User setting = 0

PIN DESCRIPTION

POWER SUPPLY PINS

Pin Name	Description
GND	Ground
VCC	+5V ±10% Supply
VEE	-5V ±5% Supply

DIGITAL INPUT/OUTPUT PINS

(All inputs are TTL levels unless otherwise noted)

Pin Name	Input Bias	Description
CS0, CS1	pullup	Address select inputs,
R/W	pullup	Read/Write: a HIGH level enables the read mode,
SDEN	pulldown	Serial port enable input ,
SCLK	pulldown	Serial port clock input ,
SDAT	pulldown	Serial port data input/output,
WDX, WDY		Write Data Inputs PECL levels when WVORI = "0" Current mode when WVORI = "1"
RST/D	pulldown	If RST/DMY bit is "0", A LOW level will reset the device, If RST/DMY bit is "1", A LOW level will enable DUMMY mode
STWN	pullup	If MODE bits are 11, a LOW will enable Servo Track Write Mode
BFST	pulldown	If BFCTL bit is "0", a HIGH level turns MR head bias current off. If BFCTL bit is "1", a HIGH level activates the thermal asperity fast recovery mode.
HUS		Write/Read Unsafe; open collector output *2kΩ resistor to VCC recommended*

ANALOG OUTPUT PINS

PIN NAME	DESCRIPTION
RDX, RDY	Differential Read Data Output
HWnX, HwnY	Inductive write head X and Y connections

ANALOG INPUT PINS

HRnX, HrnY	MR read head X and Y connections
REXT	10 kΩ external resistor to ground for current reference *1% Metal Film recommended*

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	ABSOLUTE MAXIMUM RATINGS	UNITS
Positive 5V Supply Voltage (Vp)	-0.5 to + 7	V
Negative 5V Supply Voltage (Vn)	- 7 to + 0.5	V
Storage Temperature	-65 to + 150	° C
Solder Vapor Bath	215 ° C, 90 sec, 2 times	N/A
Junction Operating Temperature	+ 130	° C
Output Pins	±10	V
Analog & Digital Inputs	±10	mA
Voltage Applied to other Pins	- 0.3 to Vp + 0.3	V

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below.

Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Positive Supply Voltage		4.5	5.0	5.5	V
Negative Supply Voltage		-4.75	-5.0	-5.25	V
Junction Temperature		0		125	° C
Ambient Temperature		0		70	° C
MR Head Resistance		45	66	85	Ω

DEFAULT TEST CONDITIONS

Operation of the device is tested under the following default conditions unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Reader input voltage			1		mV
MR Head Resistance			66		Ω
MR Head Bias Current			6.4		mA
RDX/RDY Load Capacitance	Single ended to ground		20		pF
RDX/RDY Load Resistance	Differential		2		kΩ
Write Current			40		mA
Write Inductance $_{TOTAL}$			100		nH
Write Head Series Resistance			12		Ω
Write Head Capacitance	Differential		3		pF
WDX/WDY Frequency			10		MHz
Bias Resistor			10		kΩ
Read Characteristics measured at	For example noise and gain		10		MHz
HUS Resistor	Pullup for HUS pin		2		kΩ

POWER SUPPLY CURRENT AND POWER DISSIPATION

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Current	Read Mode	54	72	90	mA
	Write Mode	97	121	145	mA
	Idle Mode	13.2	22	31	mA
	Sleep Mode	2.1	3.5	5	mA
VEE Current	Read Mode	50	67	84	mA
	Write Mode	114	143	172	mA
	Idle Mode	15.6	26	36	mA
	Sleep Mode	3.6	6	8.5	mA
Power Dissipation	Read Mode	520	695	870	mW
	Write Mode	1055	1320	1585	mW
	Idle Mode	144	240	335	mW
	Sleep Mode	28	47.5	67.5	mW
VCC Fault Voltage	Iw<0.2mA, Ir<0.2mA	3.6	3.9	4.2	VDC
VEE Fault Voltage	IW<0.2mA, Ir,0.2mA	-3.6	-3.9	-4.2	VDC

NOTE: In READ or IDLE mode, I_{MR} is assumed to be 8 mA.

In WRITE mode, I_W is assumed to be 40 mA.

Type (T): * = no ATE, R= For Reference Only

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	TTL		0	0.8	V
Input High Voltage	TTL	2.0	5		V
Input Low Current	Vil = GND		30	100	µA
Input High Current	Vih = VCC		20	100	µA
Input Low – WDX,WDY	PECL	1.0	3	Vcc-1.1	V
Input Low – WDX,WDY	Current mode	-1.5		-1.25	mA
Input High – WDX,WDY	PECL	1.3	4	Vcc-0.5	V
Input High – WDX,WDY	Current Mode	-0.25		0	mA
Voltage compliance - WDX,WDY	Current Mode	Vcc-1.7			
Input Differential Voltage – PECL	V(WDX)-V(WDY)	0.3	1		V
Input Low Current –PECL	Vil2=Vcc-1.25V			50	µA
Input High Current – PECL	Vih2=Vcc-0.75V			50	µA

Type (T): * = no ATE, R= For Reference Only

DC OUTPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Output High Current (Ioh)	HUS			50	uA
	SDAT		30		mA
Output Low Current (Iol)	HUS			4	mA
	SDAT		30		mA
Output low voltage	HUS, Iol = 4mA			0.8	V
Ext. Reference Voltage	All Modes		-1.25		V

Type (T): * = no ATE, R= For Reference Only

SERIAL PORT TIMING

RAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Data Clock Period, T_C		25			ns
SCLK Low Time, T_{CKL}		10			ns
SCLK high time, T_{CKH}		10			ns
SDEN high to SCLK, T_{SENS}		10			ns
SCLK to SDEN low, T_{SHLD}		10			ns
Data setup time, T_{DS}		6			ns
Data hold time, T_{DH}		4			ns
SDEN min. low time, T_{SL}		25			ns
SCLK to Data Valid – Read mode		25			ns

Type (T) * = no ATE, R= For Reference Only

READ CHARACTERISTICS, MR HEAD AMPLIFIER

Recommended operating conditions apply unless otherwise specified.

Rmr = 66 Ohms; CL (RDX, RDY) <20 pF, RL(RDX,RDY) > 2K

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MR Current Range	GMR=LOW	4		10	mA
MR Current Accuracy		-6		+6	%
MR Head Voltage Common Mode	Selected Head	-100		100	mV
MR Head Voltage Differential	Selected Head	100		700	mV
Unselected MR Current			0.1		mA
Differential Volt Gain	Vin=1mVp-p @10 MHz, 66Ω R_{SOURCE}	125	150	175	V/V
		167	200	233	V/V
		208	250	292	V/V
		250	300	350	V/V
Programmable Voltage Bandwidth	Vin=1mVp-p, -3dB 66Ω Rmr, Lmr=30 nH	113	150	188	MHz
		131	175	219	MHz
		150	200	250	MHz
		175	225	281	MHz
Input Noise Voltage, V_n	5MHz-150MHz ave, Excludes R_{mr} thermal noise.		.5	.8	nV/√Hz
Input Noise Current, I_n	R_{mr} =66 ohms		6	14	pA/√Hz
Noise Figure, N.F.			2		dB

Type (T): * = no ATE, R= For Reference Only

$$N.F. = 10 * \log_{10}\left[1 + \frac{V_n^{\,2} + (I_n * R_{MR})^2}{4KT * R_{MR}}\right]$$

READ CHARACTERISTICS CONTINUED:

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Resistance	Vin=1mVp-p, @ 10MHz		1K		Ω
Diff Input Capacitance	Vin=1mVp-p, @ 10MHz	7	7	17	pF
Input Dynamic Range	gain falls to 90% of its small signal value	3	5		mV
CMRR	Vin=100mVp-p @10MHz	55			dB
PSRR	100mVp-p on VCC or VEE, @TBD MHz	40			dB
Channel Separation	Unselected Channels driven with 100mVp-p @10MHz	45			dB
Output Offset Voltage				100	mV
Output Resistance	Single Ended			30	Ω
Output Current		4			mA
RDX/RDY Common Mode Output Voltage			Vcc-3		V

Type (T): * = no ATE, R= For Reference Only

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified
lw=40mA, Ltot=100nH, Rh=12 Ohm

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Range		13.5		53.5	mApk
Write Current Accuracy		-10		+10	%
Differential Head Voltage Swing	Open Head	13	16		Vp-p
Unselected Head Current	DC		0.1		mA
Unselected Head Current	AC		1		mApk
Head Differential Damping AC Resistance	I_{DAMP}=1.5mA		260		Ω
Head Differential Damping DC Resistance			10K		Ω
Head Differential Output Capacitance		5		7.5	pF

Type (T) * = no ATE, R= For Reference Only

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified
Rmr=66 Ohm, 10% variation ; CL (RDX,RDY) < 20pF ; Iw=40mA
RL (RDX, RDY) > 1K; Ltotal = 100 nH, Rh = 12 ohm ; F (WDX/WDY)=10MHz

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read to Write Switching	To 90% of write current			50	nS
Write to Read Switching	Note 1			350	nS
Sleep to Read	Note 1			100	uS
Idle to Read	Note 1			5	uS
HSx to Read	Note 1, Note 2			5	uS
Safe to Unsafe	Write mode, from last WDX/WDY transition			1	uS
Unsafe to Safe	Fault cleared, from first positive (WDX-WDY) transition			500	nS
Write Propagation Delay	From 50% point			7	nS
Write Current Rise/Fall Time	10% to 90%, L_{TOTAL}=100nH C_h=3pF		1.1	1.5	nS
Write Current Asymmetry	Shorted Head			0.2	nS

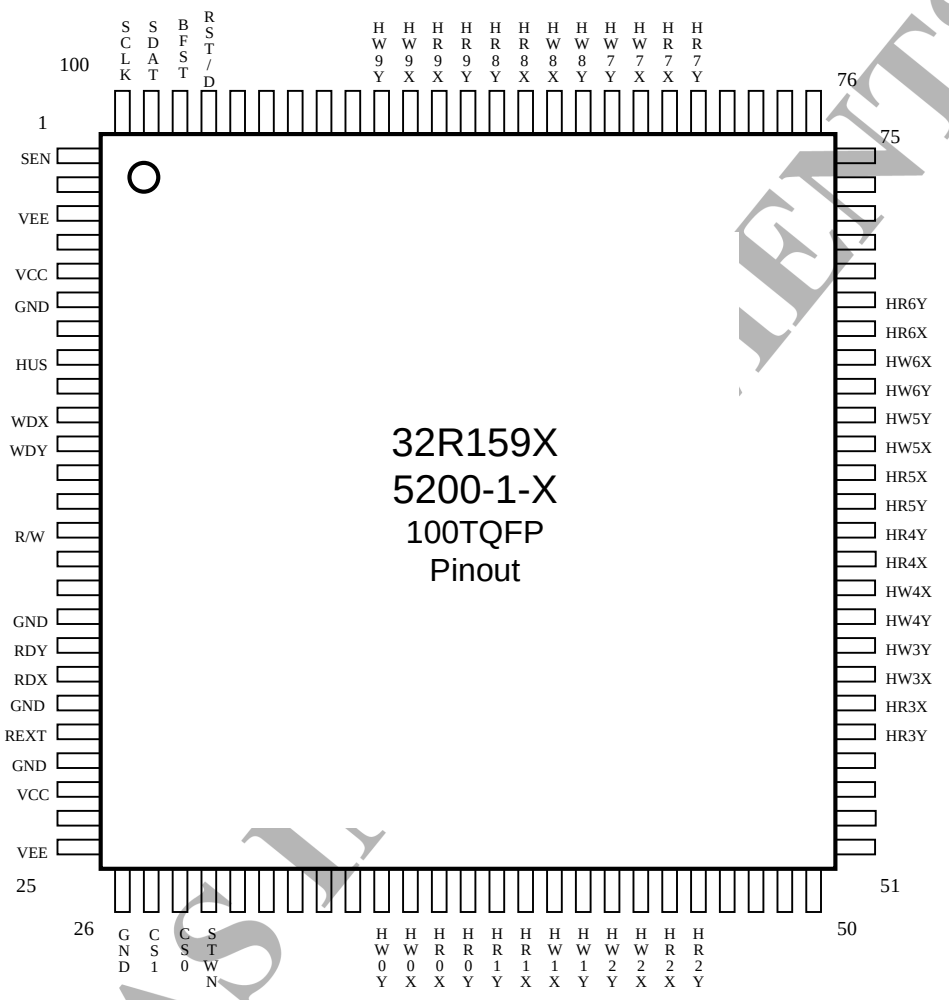
Type (T) * = no ATE, R= For Reference Only

NOTE1: Read signal recovery criteria is defined in terms of baseline and signal envelope. Recovery times are specified as the time it takes for the DC baseline at the reader output to settle within ±20mV of its final value and the signal envelope at RdOut to settle within 90% of its final value.

NOTE 2: Switching specs for modes accessed through serial port do not take into account any time needed to write to the serial port.

PACKAGE PIN DESIGNATIONS

(Top View)



Texas Instruments Storage Products, 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SR1595AE
+5/-5V 6-CHANNEL MR READ/WRITE DEVICE

June, 2000

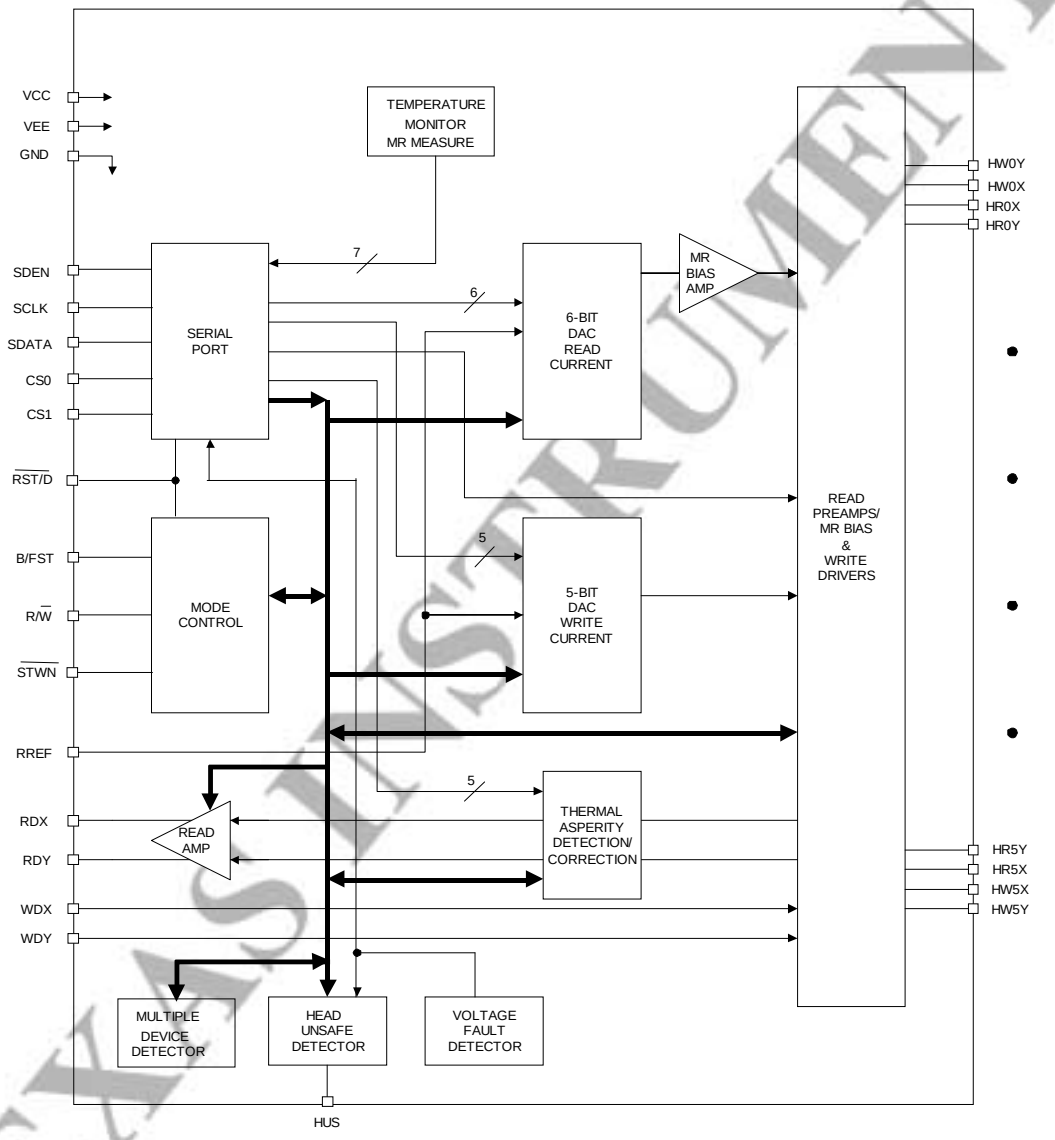
DESCRIPTION

The TI/SPG SR1595AE is a BiCMOS monolithic integrated circuit designed for use with 6 four-terminal Magneto-Resistive recording heads. It provides a write driver, low noise read amplifier and MR current bias with serial port controlled head selection, servo track write, write current, MR read bias current and fault detection circuitry. Several servo write modes are supported. The device requires +5V and -5V and comes in a 100-pin TQFP package or as bumped die.

FEATURES

- **+5V ±10%, -5V ±5% supplies**
- **Designed for four-terminal MR heads**
- **Requires only one external resistor**
- **Truly differential current or voltage bias / voltage sense MR read Amplifier**
- **Programmable MR head bias current (6 bits) = 3.0 – 10.0 mA**
- **or voltage bias (6 bits) = 131 - 378 mV**
- **MR head resistance range of 40-80Ω**
- **Programmable MR read gain (100, 150, 200, or 250 V/V)**
- **Programmable voltage BW (150 MHz - 300 MHz) min**
- **MR read input noise = 0.5 nV/√Hz (Typ, R_{mr}=0Ω)**
- **MR read input current noise = 6pA/√Hz @ 7.5 mA (Typ)**
- **MR read input resistance = 1K Ohm (Typ)**
- **Programmable write data input - Voltage or Current Mode**
- **Programmable read data output - Voltage or Current Mode**
- **Head voltage swing = 16 Vp-p (Typ)**
- **Head Current risetime-$t_{r\ 10\text{-}90}$- 0.7 ns (Typ, I_w=50mA, L_{tot}=60 nH, R_H=10Ω,C_H=3 pF)**
- **Programmable write current overshoot**
- **Programmable write damping control**
- **Write current range (5 bits) = 9.4 – 50.4 mA**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Read/Write serial port controls head selection, write current, write damping, MR head bias current, thermal asperity threshold and mode, read gain and bandwidth, low power idle and sleep mode selection and more.**
- **Automatic 7 bit MR head resistance and temperature measurement modes**
- **Low Bandwidth read gain test mode**
- **Thermal asperity detection and compensation**
- **MR head capacitive discharge protection**
- **40 MHz Serial Interface – 3.3V TTL / CMOS compatible**
- **Illegal Multiple Device Selected detection**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The TI/SPG SR1595AE addresses up to 6 four-terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with the R/$\overline{W}$ pin and the serial port as shown in Table 1. All inputs, except the serial port, BFST and $\overline{RST}$/$\overline{D}$, have internal pull-ups so that when left open, they will default to the HIGH state. The three serial port i/o pins, BFST and $\overline{RST}$/$\overline{D}$ have internal pull-downs.

The serial data port is used to control chip selection, head selection, servo track write, write current, write damping control, MR head resistance measurement, MR bias current, read gain and bandwidth, thermal asperity threshold and mode.

CHIP SELECTION

The chip is selected during a serial port transfer by sending address bits, CS0 and CS1, that match the logic levels of the chip's chip select pins, CS0 and CS1. Matching CS0, CS1 to the logic levels of the chip select pins during a serial port transfer has no effect on the mode the chip is in, the matching only determines which chip connected to the serial bus responds to the read or write request.

SERIAL PORT

A complete data transfer is sixteen (16) bits long: one R/$\overline{W}$ bit, seven (7) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded before data. The first bit is the serial port R/$\overline{W}$ bit which is HIGH for a read operation or LOW for a write operation. The next two bits (CS0-CS1) are the device select bits and should match the state of the CS0 and CS1 pins. The following five bits (A2-A6) are the register address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map for more information)

Asserting the serial port data enable line, SDEN, initiates a transfer. SDATA is clocked into the internal shift register by the rising edge of SCLK. A counter on the device ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted, otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN. Data transferred out of the serial port is timed to be sampled with the rising edge of SCLK. After the hold time specification is met, SDATA starts to change in order to meet the setup time specification for the next rising edge of SCLK at maximum SCLK frequency. In order to meet the turnaround delay between address and data during readback, SCLK must be held low for an extra clock period (25 ns) before the rising edge of SCLK for D0 (see fig. 3 timing diagram).

Multiple devices can be written to simultaneously by setting serial port address bits CS0 and CS1 to 1 and setting the $\overline{STWN}$ pin LOW. When CS0 and CS1 address bits are equal to 1 during a serial port transaction, the states of the CS pins CS0 and CS1 are ignored. When STWN is HIGH, transactions with CS0=CS1=1 are ignored.

SERIAL PORT WRITE TIMING

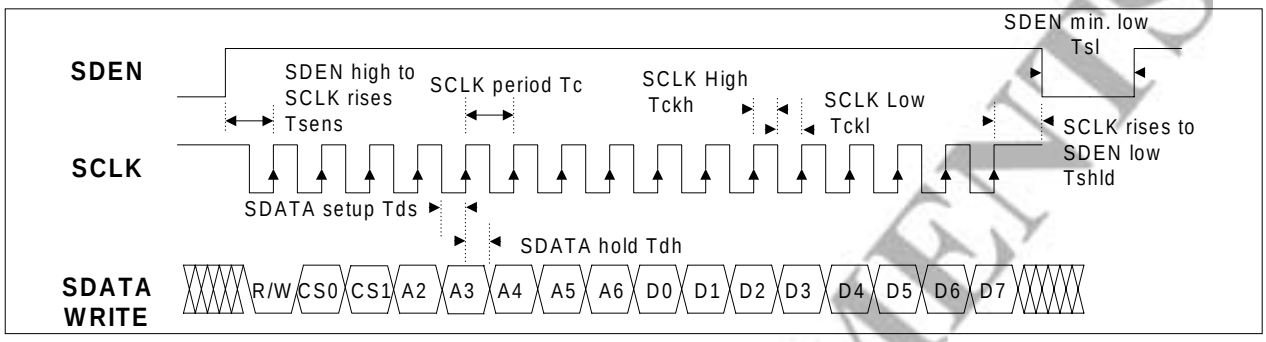


FIGURE 2: Serial Port Timing Diagram – Write

SERIAL PORT READ TIMING

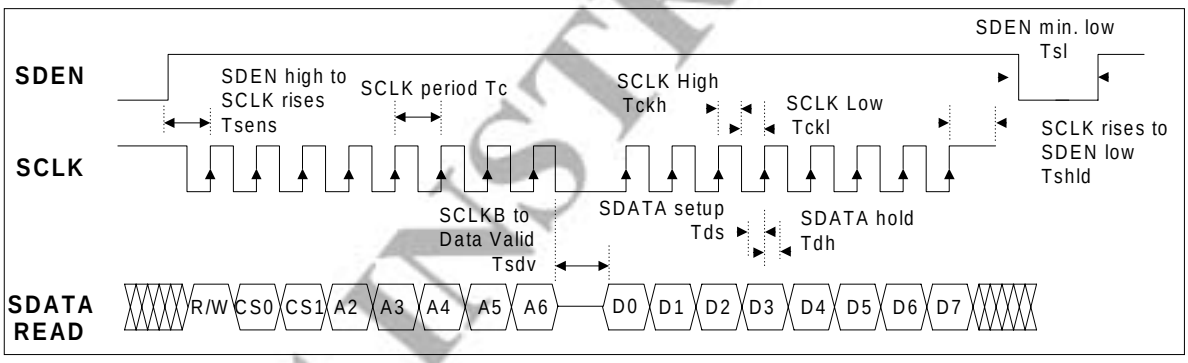


FIGURE 3: Serial Port Timing Diagram – Read

RESET

The device enters reset mode when the $\overline{RST}/\overline{D}$ pin is pulled LOW AND the $\overline{RST}$/DMY bit of reg 9 is 0. In reset mode, all registers are reset to their POR defaults, and the device enters SLEEP mode.

SLEEP MODE

This is the default power-on mode. Sleep mode is the lowest power consumption mode. The device enters sleep mode when the mode control bits of register 9 are set to 00 or a reset signal is received. In sleep mode, only the serial port of the device is active. The device may be brought out of sleep mode by setting the mode control bits in register 9 to idle, active read or write, or servo track write.

IDLE MODE

The device enters idle mode when register 9 mode control bits are programmed to 01. In idle mode, the device is inactive, but many blocks of the device are biased in preparation for switching to read or write mode. The device may be brought out of idle mode by writing register 9 mode control bits to sleep, active read or write, or servo track write.

TABLE 1: Mode Selection

MODE	Pin R/W	Sport Reg 9 MODE1	Sport Reg 9 MODE0	Sport Reg 9 MRR	Sport Reg 9 TMF	Sport Reg 9 RST/ DMY	Pin RST/D	Pin STWN	Sport Reg 1 DUMMY
Reset	x	x	x	x	x	0	0	x	x
Dummy	x x	x x	x x	x x	x x	1 x	0 1	1 1	x 0
SLEEP	x	0	0	0	0	0	1	x	x
IDLE	x	0	1	0	0	0	1	1	x
READ	1	1	0	0	0	0	1	1	x
WRITE	0	1	0	0	0	0	1	1	x
MR Measure	1	1	0	1	0	0	1	1	x
Temp Measure	x	1	0	0	1	0	1	1	x
SERVO WRITE*	0	1	x	0	0	0	1	0	x
ROUTON*	0	1	1	0	0	0	1	1	x

*The preamp must be addressed with CS0=CS1=1 and STWN low to enable SERVO WRITE and ROUTON modes.

READ MODE

The device enters Read Mode based on conditions described in Table 1 of Mode Selection Section. In Read Mode, gain is set to one of four values based on GAIN0-GAIN1 bits of register 2.

The HUS output is HIGH (open collector) in this mode unless a thermal asperity or read fault condition is detected, which causes the output to go LOW.

The outputs of the read amplifier RDX and RDY are programmable as either emitter followers or open collectors and are in phase with the voltage change at the selected input ports HRnX and HRnY where the respective MR head is attached.

RDX and RDY outputs can be set to current mode drive by setting the RVORI bit in register X HIGH. In this mode, each pin, RDX and RDY, will sink 1mA to GND and modulate that current in phase with the voltage change across the HRX/HRY pins. The channel must provide a low impedance input and bias voltage of not less than 2.4 volts on both RDX and RDY.

The gain of the amplifier in current mode drive will be approximately $V_{GAIN}/1000\Omega$, where V_{GAIN} is the equivalent voltage gain set in the serial port.

In Read mode, the voltage at the midpoint of the selected MR head is forced to ground by an internal feedback loop. For the unselected MR heads, the head ports are pulled to ground by a low impedance and thus will prevent the heads from conducting current in the event of head to disk contact.

To improve the Write to Read recovery time, the MR bias current is maintained in Write mode.

The MR bias current is removed from the MR element when Dummy Mode is selected. Dummy mode is selected by either programming the DUMMY bit in Reg 1 to LOW, or setting the $\overline{RST}/\overline{D}$ pin LOW when the $\overline{RST}/\overline{D}$ pin is enabled by programming the $\overline{RST}$/DMY bit of Reg 9 (Dummy Pin enable) HIGH.

The read path can be forced to remain on and the read amplifier outputs active during WRITE mode by programming ROUTON mode per Table 1.

The Reader Bandwidth is modified by programming register 3. There are 2 bits of control for the Lower Bandwidth pole and 2 bits of control for the Upper Bandwidth pole. The pole frequency control is programmed as shown in Table 2.

TABLE 2: Bandwidth Control

LBW1	LBW0	Frequency	LBW1	LBW0	Frequency
0	0	1.5 MHz	0	1	2.0 MHz
1	0	3.0 MHz	1	1	4.0 MHz

HBW1	HBW0	Frequency	HBW1	HBW0	Frequency
0	0	150 MHz	0	1	200 MHz
1	0	250 MHz	1	1	300 MHz

There are 3 bits of control for the Upper Bandwidth zero. The following formula describes the programming of the Upper Bandwidth zero:

HF Zero @ frequency = 1200 MHz / [(HFZ0 + 2*HFZ1 + 4*HFZ2) - 1]

Programming HFZ0= 0 or 1, and HFZ1=HFZ2 = 0 disables the Upper Bandwidth zero function.

MR HEAD BIASING

In Read mode, the MR Head can be biased in one of two modes: Constant Current biasing or Constant Voltage biasing. MR Head biasing is determined by the CVON bit (D6) in register 1. The power on state (CVON = 0) selects Constant Current mode.

In Constant Current mode (CVON=0), the necessary current for biasing the MR Head is internally programmed by a 6 bit DAC via the serial port. The magnitude of the bias current is given by:

$$I_{MR} = 3.0mA + \frac{M}{63}7.0mA$$

where M is the decimal value of IMR0-IMR5 (register 2 of the serial port).

In Constant Voltage mode (CVON=1), the necessary voltage for biasing the MR Head is internally programmed by a 6 bit DAC via the serial port. The magnitude of the bias voltage is given by:

$$V_{MR} = 131mV + \frac{M}{63}247mV$$

where M is the decimal value of IMR0-IMR5 (register 2 of the serial port).

WRITE MODE

The device enters Write Mode based on conditions described in Table 1 of the Mode Selection Section.

The HUS output is LOW in this mode unless there is a write fault, which causes the output to go HIGH.

Selecting Write mode generates a write current from the internal 5 bit DAC, set by the serial port, and activates the Write Unsafe (WUS) detect circuitry. Head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each transition of the differential voltage signal WDX-WDY. When WDX>WDY I_W flows from X to Y.

The magnitude of the current (0-pk) is given by:

$$I_W = 9.44mA + 40.97mA\frac{N}{31}$$

where N is the decimal value of IW0-IW4 bits of the serial port register 4.

Note that the actual head current Ix,y is given by:

$$I_{x,y} = \frac{I_W}{1 + \frac{R_h}{R_d}}$$

where R_h is the head DC resistance and R_d is the damping resistance.

Programmable damping control is achieved by applying a damping current immediately after the write h-bridge switches. The value of the damping current is given by:

$$I_{DAMP} = 0.5mA + 7mA\frac{N}{7}$$

where N is the decimal value of WCP0-WCP2. This damping current can be translated into an equivalent ac damping impedance by the formula:

$$R_{DAMP} = \frac{10}{\sqrt{I_{\mathrm{DAMP}}}}\Omega\,.$$

This impedance is not active when the writer is not switching. The damping resistance for a non-switching writer head is typically 10K ohms.

The MR bias can be forced to remain on and the read amplifier outputs active during WRITE mode by programming ROUTON mode per Table 1.

Write current overshoot is programmable through bits WCO0-WCO2 of register 14. The amount of overshoot is shown in Table 3. The % overshoot is dependent on the load and interconnect characteristics. The values in Table 3 are for the conditions specified in section 4.5.3. Programmable write current overshoot is enabled by setting the WCOEN bit HIGH in register 14.

TABLE 3: Write Current Overshoot

WCO2-WCO0	% OVERSHOOT
000	26
001	34
010	45
011	53
100	58
101	63
110	66
111	68
Disabled	94

Two bits, WCOB1 and WCOB0, are used to optimize the overshoot control for different writer head loads and interconnect. The target settings are:

TABLE 4: Write Current Overshoot Control

WCOB1-WCOB0	TOTAL LOAD
00	100 nH
01	67 nH
10	50 nH
11	40 nH

SERVO TRACK WRITE MODE

The device enters Servo Track Write Mode based on the conditions described in Table 1 of Mode Selection Section. To enter Servo Track Write mode, the $\overline{\text{STWN}}$ pin must be set LOW and the R/W pin must be set LOW and the serial port must be written to with CS0=CS1=1. In Servo Track Write mode, the device writes the same signal to one head, heads 0 thru 3, heads 4 & 5, or all heads as shown in Table 5. A serial port transaction that does not have CS0=CS1=1 will remove the preamp from Servo Track Write Mode. With the Mode bits of register 9 set to 10, and HS3 = 0, the value programmed in HS0 - HS2 of register 0 is selected. With the Mode bits set to 10, and HS3 = 1, HS0-HS2 values of 0-2 selects three heads; 0, 1, 2. With the Mode bits set to 10, and HS3 = 1, HS0-HS2 values of 3-5 selects three heads; 3 thru 5. With the Mode bits set to 11, and HS3 = 0, two heads are selected; the head value in HS0-HS2 and the head value in HS0-HS2 plus 1. With the Mode bits set to 11, and HS3 = 1, all six heads are selected, independent of the value in HS0-HS2.

Multiple devices can be written to simultaneously by setting serial port address bits CS0 and CS1 to 1 while $\overline{\text{STWN}}$ is low. When CS0 and CS1 address bits are set to 1, and the $\overline{\text{STWN}}$ pin is LOW during a serial port transaction, the states of the CS pins CS0 and CS1 are ignored. Up to 3 preamps can be selected simultaneously. The Multiple Device Selected fault is disabled in this mode. In addition, write unsafe functions are not active in Servo Track Write mode.

ROUTON MODE

The read path can be made active during write mode by: first - addressing the preamp with address bits CS0 = CS1 = 1 and the $\overline{\text{STWN}}$ pin set LOW, then second - programming the Mode bits of register 9 to 3 and setting the $\overline{\text{STWN}}$ pin HIGH as shown in the mode selection Table 1 in section 4.3.1. Only one read/write head is active in this mode, selected by the Head Select bits (HSn) in register 0. Routon is not supported in Servo track Write mode.

READ/WRITE UNSAFE

In Read or Write mode, any of the following conditions will be latched and indicated as a fault on the Head Unsafe (HUS) open collector output pin. The HUS pin flags a fault only while the fault is physically present. The latched faults will be encoded into 4 bits and stored in register 7 (FCODE0-FCODE3).

In read or write mode, if an illegal head address is received, all heads are unselected and the fault pin is asserted. Write and read currents are turned off. The serial port registers remain unchanged, except for the fault code in register 7.

In read or write mode, a power supply low fault will assert the fault pin and, in write mode, turn off the write current. The serial port registers are not reset and dummy is NOT selected. In write mode, upon removal of the power supply fault, the write current bias is re-enabled and the HUS pin is set to LOW.

The fault code is cleared on powerup, on system reset, and on writing to register 9. Fault codes have the following value and precedence as shown in Table 6.

TABLE 5: Servo Write Head Select

Mode	HS3	HS0-HS2	Active Write Head
10	0	0-5	K
10	1	0-3	Heads 0-3
10	1	4-5	Heads 4&5
11	0	0-4	K & K+1
11	1	X	All Heads

K = head selected by HS0-HS2 in register 0

The following equation is used to calculate approximate power dissipation in servo write mode:

Pd = [246 mA + (1.2 * Iw * # chnls)] * (Vcc + Vee)/2

TABLE 6: Fault Codes

	MSB LSB			
Fault #	**Code**	**Precedence**	**Fault**	**Conditions**
	0000			*No Fault*
1	0001	10	Iw present while not in write mode	
2	0010	8	MR head voltage too high	*Read Mode Only* *>800mVpp diff*
3	0011	13	Thermal Asperity detected	*Read Mode Only*
4	0100	11	Read head open	*Read Mode Only*
5	0101	9	Low write current	*Write Mode Only* *Iw < 5 mA*
6	0110	6	WDX/WDY frequency too low	Fwdx/y < 2 MHz *Write Mode Only*
7	0111	14	Write head open	
8	1000	4	Write head shorted to GND	*Write Mode Only*
9	1001	2	Rext open or shorted	
10	1010	5	Write to read head short	
11	1011	1	Low Vcc or Vee	Vcc < 3.9 V typ. Vee > -3.9V typ.
12	1100		Not assigned	
13	1101	3	Illegal head selection	
14	1110	12	Illegal MDS	
15	1111	7	Temperature too high	Tj > 145 C

Fault code mask bits disable the detection and flagging of faults as described in Table 7. One or more faults can be disabled by setting one or more of the fault bits in register 7 to one. Setting FLT0-FLT3 to all zeros enables are faults. Setting FLT0-FLT3 to all ones disables all faults.

FLT0-FLT3: 4 BITS; FAULT REPORTING MASK BITS

TABLE 7: Fault Code Mask Bits

MSB LSB	
FLT3 FLT0	**Faults reported**
0000	Report all faults
1XXX	Disable write head open or shorted, Rext open or shorted
X1XX	Disable WDX,Y frequency too low, MR head voltage too high
XX1X	Disable Temperature too high, MR head open
XXX1	Disable MDS, Thermal Asperity Detected, Write head open or shorted to GND
1111	Disable all faults

NOTE: Codes may be OR'ed together to disable multiple faults.

MULTIPLE DEVICE SELECTED DETECTION

In applications with more than one preamplifier, it is illegal to program more than one device simultaneously, unless Servo Track Write Mode is selected. Two bits in register 0, SELT and SELF, are used to determine if more than one preamp has been selected simultaneously. When SELT is set HIGH, the HUS pin pulls to 2/3 Vcc and does not respond to any faults. If the preamp is in Servo Write Mode, setting SELT has no effect. If more than one preamp has the SELT bit set high, than HUS will be pulled to 1/3 Vcc or lower. This causes a 1 to be set in the SELF bit of register 0 and fault code 14 to be latched in register 7. Reading back SELF = 0 indicates that only one preamp has been selected. For the communication between preamps using the HUS pin to function properly, a pull-up resistor with a value of **5 KΩ** is required.

The Multiple Device Selected Detection fault can only be cleared by sending an active low pulse to the RST/D (reset) pin.

THERMAL ASPERITY DETECTION AND COMPENSATION

When the read head signal amplitude exceeds a serial port programmable threshold, a thermal asperity hit is detected and the HUS pin will go LOW until the thermal asperity level has dropped to 10-15% above the baseline. The equation describing this threshold is given by :

$$Threshold = 0.4mV + TRANGE * 3mV + 5.6mV\left(\frac{M}{31}\right)$$

(mV pk-pk input referred)

where M is the decimal value of TADT bits of the serial port register 5 (Thermal Asperity Detection Threshold ,TADT) and TRANGE has a value of 0 or 1.

Depending on the value of bits TAC, TAD, and TASD in conjunction with the value of input pin BFST(active HIGH), the device will handle thermal asperity according to the following table:

TABLE 8: Thermal Asperity Detection And Compensation Mode Selection

TASD	TAD	TAC	BFST[3]	Lower BW	HUS Flag	Mode
1	X	X	X	540KHz	No	**"TA Shutdown"** [4]
0	0	0	0	Serial Port	No	**"No Compensation"** [1]
0	0	0	1	8 MHz	No	**"Fast"**
0	1	0	0	Serial Port	Yes	**"Detection Only"** [1]
0	1	0	1	8 MHz	Yes	**"Fast w/Detection"**
0	X	1	X	8 MHz / Serial Port	Yes	**"Auto Compensation"**[1,2]

NOTE 1: The table describing the lower bandwidth -3db frequency is :

TABLE 9: Low Bandwidth Frequency Selection

LBW1	LBW0	Frequency	LBW1	LBW0	Frequency
0	0	1.5 MHz	0	1	2.0 MHz
1	0	3.0 MHz	1	1	4.0 MHz

where LBW0,LBW1are bits in serial port register 3.

NOTE 2: In Auto Compensation Mode, when a thermal asperity is detected, the lower bandwidth -3db point is automatically shifted to 8 MHz.

NOTE 3: BFCTL bit in serial port register 1 must be set HIGH.

NOTE 4 : TA Shutdown is for test purposes only. Switching times are not guaranteed in this mode.

In **TA Shutdown** mode, the TA circuit is shut down (regardless the value of BFST pin)

In **No Compensation** mode, the TA circuit is powered up, but inactive. The lower bandwidth -3db point is set to the low bandwidth frequency determined by the LBW0, LBW1 bits of reg 3.

In **Fast** mode, the lower -3db reader bandwidth is shifted from the low bandwidth frequency determined by the LBW0, LBW1 bits of reg 3 to 8 MHz whenever the asynchronous BFST pin is brought HIGH. When BFST pin is subsequently brought LOW, the pole frequency will immediately return to its original value.

In **Detection Only** mode, thermal asperities will be flagged by bringing the HUS pin LOW, but no compensation will be made.

In **Fast Mode w/Detection**, compensation is made in the same manner as Fast mode, but thermal asperity detection and flagging is also enabled.

In **Auto Compensation** mode, the circuit provides detection and correction without any assistance. After a thermal asperity is detected, the pole frequency is automatically shifted from thelow bandwidth frequency determined by the LBW0, LBW1 bits of reg 3 to 8 Mhz. When HUS returns HIGH, the pole frequency is returned to the low bandwidth setting programmed after an additional delay of 1.5us.

MR HEAD RESISTANCE MEASUREMENT FUNCTION

When the device is in read mode and the MRR bit of register 9 is set HIGH, the device will automatically measure the DC resistance of the selected MR head and report the encoded result in bits M0-M6 of register 8 after about 800 uS.

NOTE: The result in register 8 is only valid if the measurement is made while the device is in READ mode.

The R_{MR} (Ω) can be calculated by the following equation:

$$R_{MR} = \frac{A + B*(M + 0.5)}{I_{MR}} \quad \text{where}$$

To cover the full range (40 to 80 Ω) of head resistance values, it is recommended that the read head bias current should be at most 5mA. Bias current other than 5mA could result in erroneous results.

TEMPERATURE MONITOR FUNCTION

When the TMF bit of register 9 is set HIGH, the device will automatically measure its own die temperature and report the encoded result in bits M0 - M6 of register 8 after about 800uS. The temperature of the die, T_{DIE} is given by:

$$T_{DIE}(^oC) = 0 + 1.14*M$$

where M is the decimal value of bits M0-M6 of register 8. If M is 0, the device temperature is out of range, i.e., $T <$ 0 °C or T > 145 °C.

NOTE: Operation beyond the absolute maximum rated temperature of 130°C is **discouraged, and permanent damage to the device could result.**

The temperature monitor function is only guaranteed to be accurate in IDLE mode, but may be used in other modes. The TMF bit must be reset to zero before initiating another measurement.

TABLE 10: MR Resistance Calculation Factors

A (Constant 1)	79.85
B (Constant 2)	2.5
M	Decimal value of M0-M6 in the serial port
I_{MR}	Programmed MR bias current (in mA)

If M is equal to 0, the voltage across the MR head resistance may be out of range. MRR must be reset to zero before initiating another measurement.

SERIAL PORT BIT MAP

Serial Port Data Format: R/$\overline{W}$ CS0 CS1 A2 A3 A4 A5 A6 D0 D1 D2 D3 D4 D5 D6 D7 (where A6 and D7 are MSBs)

TABLE 11: Serial Port Bit Mapdescription Of Mode Control Bits

						MSB							*LSB*
Reg	**A6**	**A5**	**A4**	**A3**	**A2**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	X	0	0	0	0	HS3 **0**	HS2 **0**	HS1 **0**	HS0 **0**	SELT **0**	SELF **R**	LCS1 **R**	LCS0 **R**
1	X	0	0	0	1	X **0**	CVON **0**	DUMMY **0**	X **0**	X **0**	RVORI **0**	WVORI **0**	BFCTL **0**
2	X	0	0	1	0	IMR5 **0**	IMR4 **0**	IMR3 **0**	IMR2 **0**	IMR1 **0**	IMR0 **0**	GAIN1 **0**	GAIN0 **0**
3	X	0	0	1	1	X **0**	HFZ2 **0**	HFZ1 **0**	HFZ0 **0**	HBW1 **0**	HBW0 **0**	LBW1 **0**	LBW0 **0**
4	X	0	1	0	0	IW4 **0**	IW3 **0**	IW2 **0**	IW1 **0**	IW0 **0**	WCO2 **0**	WCO1 **0**	WCO0 **0**
5	X	0	1	0	1	TRANGE **0**	TAD **0**	TAC **0**	TADT4 **0**	TADT3 **0**	TADT2 **0**	TADT1 **0**	TADT0 **0**
6	X	0	1	1	0	VEND7 **1**	VEND6 **0**	VEND5 **0**	VEND4 **0**	VEND3 **1**	VEND2 **0**	VEND1 **1**	VEND0 **1**
7	X	0	1	1	1	FLT3 **0**	FLT2 **0**	FLT1 **0**	FLT0 **0**	FCODE3 **R**	FCODE2 **R**	FCODE1 **R**	FCODE0 **R**
8	X	1	0	0	0	X **0**	M6 **R**	M5 **R**	M4 **R**	M3 **R**	M2 **R**	M1 **R**	M0 **R**
9	X	1	0	0	1	X **0**	X **0**	TMF **0**	MRR **0**	SIOLVL **0**	RST/DMY **0**	MODE1 **0**	MODE0 **0**
10	X	1	0	1	0	- **0**	RES **0**	RES **0**	RES **0**	RES **0**	RES **0**	RES **0**	RES **0**
14	X	1	1	1	1	WCP2 **0**	WCP1 **0**	WCP0 **0**	WCOB1 **1**	WCOB0 **1**	WCOEN **0**	WDDIS **0**	CCDIS **0**
15	X	1	1	1	1	TASD **0**	RES **0**	RES **0**	RES **0**	RES **0**	RES **0**	RES **0**	RES **0**

NOTE: Bits in table are not in the same order as bits written to the serial port for enhanced readability. R=readback only.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A5, A4, A3, A2. Serial port Read/Write and CS1, CS0 bits are not shown.

REGISTER 0
Address = 0000

BIT	NAME	DESCRIPTION
7:4	HS3:0	Head select bits.
3	SELT	1 = Enable MDS detection 0 = Disable MDS detection
2	SELF	MDS detection readback 1 = Illegal multiple device selection detected 0 = Only one device detected during MDS test
1:0	LCS1:LCS0	Reports state of CS1/CS0 pins

REGISTER 1
Address = 0001

BIT	NAME	DESCRIPTION
7	X	Not Used
6	CVON	Constant voltage bias 1 = Enable constant Voltage bias mode 0 = Enable constant current bias mode
5	DUMMY	Internal Dummy load control 1 = Dummy load Inactive 0 = Dummy Load Active
4:3	X	Not Used
2	RVORI	Reader output control 1 = Reader output in current mode 0 = Reader output in voltage mode
1	WVORI	Write data input mode control 1 = Current mode write data input 0 = Voltage mode write data input
0	BFCTL	Bias/Fast (BFST) pin mode control 1 = BFST pin controls reader low corner frequency BFST = 1 = Raises low corner frequency BFST = 0 = Normal low corner frequency 0 = BFST pin controls reader bias BFST = 1 = MR bias current is OFF BFST = 0 = MR bias current is ON

REGISTER 2
Address = 0010

BIT	NAME	DESCRIPTION		
7:2	IMR5:IMR0	Reader MR bias current or voltage DAC. Mode controlled by CVON bit. When CVON = 0, current range is 3 – 10 mA. Bias equation is: $I_{MR} = 3mA + \frac{M}{63}7mA$, where M is the decimal value of IMR. When CVON = 1, voltage range is 131 to 378 mV. Bias equation is: $V_{MR} = 131mV + \frac{M}{63}247mV$, where M is the decimal value of IMR.		
1:0	GAIN1:0	GAIN1	GAIN0	Reader Gain
		1	1	250 V/V
		1	0	200 V/V
		0	1	150 V/V
		0	0	100 V/V

REGISTER 3
Address = 0011

BIT	NAME	DESCRIPTION		
7	X	Not Used		
4:6	HFZn	High frequency zero control Hfzero@f = 1200 MHz/[(HFZ0 + 2*HFZ1 + 4*HFZ2)-1], HFZ0 = 0 or 1 and HFZ1 =HFZ2 = 0 disables HF Zero		
3:2	HBW1:0	Reader high frequency bandwidth control		
		HBW1	HBW0	Frequency
		1	1	300 MHz
		1	0	250 MHz
		0	1	200 MHz
		0	0	150 MHz
1:0	LBW1:0	Reader low frequency bandwidth		
		LBW1	LBW0	Frequency
		1	1	4 MHz
		1	0	3.0 MHz
		0	1	2.0 MHz
		0	0	1.5 MHz

REGISTER 4
Address = 0100

BIT	NAME	DESCRIPTION	
7:3	IW4:IW0	Write Current DAC, 9.4 mA to 50.4 mA. DAC equation: $I_W = 9.4mA + 40.97mA\frac{N}{31}$, where N is the decimal value of IW.	
2:0	WCP2:WCP0	Write Current Overshoot Control.	
		WCO2:WCO0	% Overshoot
		000	26
		001	34
		010	45
		011	53
		100	58
		101	63
		110	66
		111	68
		Disabled	94

REGISTER 5
Address = 0101

BIT	NAME	DESCRIPTION
7	TRANGE	Thermal Asperity threshold range 1 = 3.4 = 9.0 mV pk-pk input referred 0 = 0.4 – 6.0 mV pk-pk input referred
6	TAD	Thermal Asperity Detection 1 = Enable Thermal Asperity
5	TAC	Thermal Asperity Compensation 1 = Enable TA compensation
4:0	TADT4:0	Thermal Asperity Threshold DAC. Threshold equation: $Threshold = (0.4mV + TRANGE * 3mV) + 5.6mV\left(\frac{M}{31}\right)$, Where M is the decimal value of TADT4:TADT0

REGISTER 6 (READ ONLY)
Address = 0110

BIT	NAME	DESCRIPTION							
7:0	Vendor Code	Revision			Texas Instruments SR1595AEA6				
		1	0	0	0	1	0	1	1

REGISTER 7
Address = 0111

BIT	NAME	DESCRIPTION	
7:4	FLT3:FLT0	Fault reporting mode	
		FLT3:FLT0	Faults reported
		0000	Report all faults
		1XXX	Disable open or short write head, Rext open or short
		X1XX	Disable WDX,Y low frequency, MR head overvoltage
		XX1X	Disable Temperature too high, MR head open
		XXX1	Disable MDS, TA detected, Write open or short to GND
		1111	Disable all faults
3:0	FCODE3:0	Fault report code. See Fault reporting Table 12	

TABLE 12: Fault reporting codes

Fault No	FCODE3:0	Precedence	Reason	Conditions
	0000			No fault
1	0001	10	Iw present while not in write mode	
2	0010	8	MR head voltage too high	Read mode only >800 mV diff
3	0011	13	Thermal Asperity detected	Read mode only
4	0100	11	Read head open	Read mode only
5	0101	9	Low write current	Write mode only, Iw < 5mA
6	0110	6	WDX/WDY frequency too low	Fwdx/y < 2 MHz write mode only
7	0111	14	Write head open	
8	1000	4	Write head shorted to GND	Write mode only
9	1001	2	Rext open or shorted	
10	1010	5	Write to read head short	
11	1011	1	Low Vcc or Vee	VCC < 3.9 V typ Vee > -3.9 V typ
12	1100		Not assigned	
13	1101	3	Illegal head selection	
14	1110	12	Illegal MDS	
15	1111	7	Temperature too high	Tj > 145°C

REGISTER 8
Address = 1000

BIT	NAME	DESCRIPTION
7	X	Not Used
6:0	M6:M0	Read Only. Measurement value for MR head resistance measurement or temperature monitor mode. Rmr is calculated from the following equation: $R_{MR} = \frac{A + B*(M + 0.5)}{I_{MR}}$, where A = 79.85, B = 2.5, M is decimal value of M6:M0, and Imr is the programmed MR bias current in mA. Die temperature, T_{DIE} is given by: $T_{DIE}(^oC) = 0 + 1.14*M$, where M is decimal value of M6:M0

REGISTER 9
Address = 1001

BIT	NAME	DESCRIPTION		
7:6	X	Not Used		
5	TMF	Temperature Monitor Function 1 = Enables temperature monitor		
4	MRR	MR Resistance Measurement Mode 1 =enables MR resistance measurement mode		
3	SIOLVL	Serial Data Readback Level 1 = Sets SDATA readback level to 5V compatible 0 = Sets SDATA readback level to 3.3V compatible		
2	RST/DMY	Reset/Dummy (RST/D) pin mode control 1 = RST/D pin controls dummy mode RST/D = 1 = Normal bias mode RST/D = 0 = MR bias is removed from selected head 0 = RST/D pin controls reset function RST/D = 1 = Normal mode RST/D = 0 = Chip enters Reset mode		
1:0	MODE1:0	Mode Control		
		MODE1	MODE0	Device Mode
		1	1	Servo Track Write/Routon
		1	0	Active Read/Write mode/Servo Track Write
		0	1	Idle Mode
		0	0	Sleep Mode

REGISTER 10
Address = 1010

BIT	NAME	DESCRIPTION
7	X	Not Used
6:1	Res	Reserved for TI Internal Use. User setting = 0
0	BANK	Selects even or odd bank of heads in Servo Track Write Mode 1 = Select even heads 0 = Select odd heads

REGISTER 14
Address = 1110

BIT	NAME	DESCRIPTION	
7:5	WCP2:WCP0	Write Damping Control. Equation: $I_{DAMP} = 0.5mA + 7mA\frac{N}{7}$, where N is the decimal value of WCP2:0	
4:3	WCOB1:0	Write Overshoot Blanking Control	
		WCOB1:WCOB0	Total Load
		00	100 nH
		01	67 nH
		10	50 nH
		11	40 nH
2	WCOEN	Write Current Overshoot Enable 1 = Enable write current overshoot	
1	WDDIS	Write Damping Control Disable 1 = Write damping disabled	
0	CCDIS	Input Cap Cancellation Disable 1 = Input capacitance cancellation OFF	

REGISTER 15
Address = 1111

BIT	NAME	DESCRIPTION
7	TASD	Thermal Asperity Shut-down 1 = Enable bypass of TA circuitry
6:0	Res	Reserved for TI internal use. User setting = 0

INPUT-OUTPUT PIN DESCRIPTIONS

POWER SUPPLY PINS

PIN NAME	DESCRIPTION
GND*	Ground
VCC*	+5V ±10% Supply
VEE*	-5V ±5% Supply

DIGITAL INPUT/OUTPUT PINS

(All inputs are TTL levels unless otherwise noted)

PIN NAME	INPUT BIAS	DESCRIPTION
CS0*, CS1*	pull-up	Address select inputs,
R/W*	pull-up	Read/Write: a HIGH level enables the read mode,
SDEN*	pull-down	Serial port enable input ,
SCLK*	pull-down	Serial port clock input ,
SDAT*	pull-down	Serial port data input/output,
WDX*, WDY*		Write Data Inputs Voltage mode when WVORI = "0" Current mode when WVORI = "1"
RST/D*	pull-down	If RST/DMY bit is "0", A LOW level will reset the device, If RST/DMY bit is "1", A LOW level will enable DUMMY mode
STWN*	pull-up	Enables Servo Track Write Mode when LOW.
BFST*	pull-down	If BFCTL bit is "0", a HIGH level turns MR head bias current off. If BFCTL bit is "1", a HIGH level activates the thermal asperity fast recovery mode.
HUS*		Write/Read Unsafe; open collector output *5kΩ resistor to VCC required*

ANALOG OUTPUT PINS

PIN NAME	DESCRIPTION
RDX*, RDY*	Differential Read Data Output – Voltage out when RVORI = 0 Current out when RVORI = 1
HWnX, HWnY	Inductive write head X and Y connections

*In a multi preamp configuration, this signal can be wire OR'd together.

ANALOG INPUT PINS

PIN NAME	DESCRIPTION
HRnX, HRnY	MR read head X and Y connections
REXT	10 kΩ external resistor to ground for current reference *1% Metal Film recommended*

OPERATING LIMITS AND VALUES

Absolute maximum ratings

Operation above the maximum ratings may damage the device.

PARAMETER	ABSOLUTE MAXIMUM RATINGS	UNITS
Positive 5V Supply Voltage (Vp)	-0.5 to + 5.75	V
Negative 5V Supply Voltage (Vn)	- 5.5 to + 0.5	V
Storage Temperature	-65 to + 150	° C
Solder Vapor Bath	215 ° C, 90 sec, 2 times	N/A
Junction Operating Temperature	+ 130	° C
Analog Output Pins	-5.5 to 5.75	V
Analog & Digital Inputs	±10	mA
Logic Output Pins	-0.5 to 5.75	V

Recommended operating conditions

The recommended operating conditions for the device are indicated in the table below.

Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Positive Supply Voltage		4.5	5.0	5.5	V
Negative Supply Voltage		-4.75	-5.0	-5.25	V
Junction Temperature		0		125	° C
Ambient Temperature		0		70	° C
MR Head Resistance		40	50	80	Ω

DEFAULT TEST CONDITIONS

Operation of the device is tested under the following default conditions unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Reader input voltage			1		mV
MR Head Resistance			50		Ω
MR Head Bias Current			5.5		mA
RDX/RDY Load Capacitance	Single ended to ground		20		pF
RDX/RDY Load Resistance	Differential		1K		Ω
Write Current			50		mA
Write Inductance TOTAL			60		nH
Write Head Series Resistance			10		Ω
Write Head Capacitance	Differential		3		pF
WDX/WDY Frequency			10		MHz
Bias Resistor - R_{EXT}			10		kΩ
Read Characteristics measured at	For example noise and gain		20		MHz
HUS Resistor	Pull-up for HUS pin		5		kΩ

POWER SUPPLY CURRENT AND POWER DISSIPATION

Recommended operating conditions apply unless otherwise specified.

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.4.1		VCC Current	Read Mode-CC mode		67	89	mA
1.5.4.2			Read Mode-CV mode		68	90	mA
1.5.4.3			Write Mode		112	149	mA
1.5.4.4			Idle Mode		19.5	26	mA
1.5.4.5			Sleep Mode		2.1	8.5	mA
1.5.4.6		VEE Current	Read Mode-CC mode		68	91	mA
1.5.4.7			Read Mode-CV mode		69	92	mA
1.5.4.8			Write Mode		146	195	mA
1.5.4.9			Idle Mode		26.8	35.7	mA
1.5.4.10			Sleep Mode		3.6	10.6	mA
1.5.4.11		Power Dissipation	Read Mode-CC mode		675	967	mW
1.5.4.12			Read Mode-CV mode		683	910	mW
1.5.4.13			Write Mode		1290	1720	mW
1.5.4.14			Idle Mode		231	308	mW
1.5.4.15			Sleep Mode		28	95	mW
1.5.4.16		VCC Fault Voltage	Iw<0.2mA, Ir<0.2mA	3.6	3.9	4.2	VDC
1.5.4.17		VEE Fault Voltage	IW<0.2mA, Ir,0.2mA	-3.8	-4.1	-4.3	VDC

NOTE: In READ or IDLE mode, I_{MR} is assumed to be 7.5 mA.

In WRITE mode, I_w is assumed to be 50 mA.

Type (T): * = no ATE, R= For Reference Only

DIGITAL INPUTS

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.5.1		Input Low Voltage	TTL	0		0.8	V
1.5.5.2		Input High Voltage	TTL	2.0		Vcc	V
1.5.5.3		Input Low Current	Vil = GND		30	100	μA
1.5.5.4		Input High Current	Vih = VCC		20	100	μA
1.5.5.5		Input Low – WDX,WDY	Voltage mode	1.0	3	Vcc-1.1	V
1.5.5.6		Input Low – WDX,WDY	Current mode	-1.5		-1.25	mA
1.5.5.7		Input High – WDX,WDY	Voltage mode	1.3	4	Vcc-1.0	V
1.5.5.8		Input High – WDX,WDY	Current Mode	-0.25		0	mA
1.5.5.9		Voltage compliance - WDX,WDY	Current Mode	Vcc-1.7			
1.5.5.10		Input impedance -WDX,WDY	Single Ended Current Mode		60		Ω
1.5.5.11		Input impedance -WDX,WDY	Single Ended Voltage Mode		>10K		Ω
1.5.5.12		Input impedance - WDX, WDY	Differential Current Mode		120		Ω
1.5.5.13		Input impedance -WDX,WDY	Single Ended Voltage Mode		>10K		Ω
1.5.5.14		Input Differential Voltage – Voltage mode	V(WDX)-V(WDY)	0.3	1		V

Type (T): * = no ATE, R= For Reference Only

DC OUTPUTS

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.6.1		Output High Current (Ioh)	HUS			50	uA
1.5.6.2			SDAT @ 2V		30		mA
1.5.6.3		Output Low Current (Iol)	HUS			4	mA
1.5.6.4			SDAT @ 0.8V	10	17		mA
1.5.6.5		Output low voltage	HUS, Iol = 4mA			0.56	V
1.5.6.6		Output high voltage	3 volt mode			3.5	V
1.5.6.7		Ext. Reference Voltage	All Modes except Sleep and Write		-1.23		V
1.5.6.8		Ext. Reference Voltage	Write Mode		-1.27		V

Type (T): * = no ATE, R= For Reference Only

SERIAL PORT TIMING

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.7.1		SCLK Data Clock Period, T_C		25			ns
1.5.7.2		SCLK Low Time, T_{CKL}		10			ns
1.5.7.3		SCLK high time, T_{CKH}		10			ns
1.5.7.4		SDEN high to SCLK, T_{SENS}		10			ns
1.5.7.5		SCLK to SDEN low, T_{SHLD}		10			ns
1.5.7.6		Data setup time, T_{DS}		6			ns
1.5.7.7		Data hold time, T_{DH}		4			ns
1.5.7.8		SDEN min. low time, T_{SL}		25			ns
1.5.7.9		SCLK low to Data Valid – Read mode, T_{SDV}				25	ns

Type (T) * = no ATE, R= For Reference Only

READ CHARACTERISTICS, MR HEAD AMPLIFIER

Recommended operating conditions apply unless otherwise specified.

Rmr = 50 Ohms; CL (RDX, RDY) <20 pF, RL(RDX,RDY) = 1K

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.8.1		MR Current Range		3.0		10.0	mA
1.5.8.2		MR Current Accuracy	IMR DAC = 0 to 50	-7		+7	%
			IMR DAC = 51 to 63	-8		+8	%
1.5.8.3		MR Voltage Range	Voltage bias mode	131		378	mV
1.5.8.4		MR Voltage Accuracy	Voltage bias mode	-6		+6	%
1.5.8.5		MR Measurement Accuracy	Excludes Imr Accuracy	-4		+4	%
1.5.8.6		Temp Measurement Accuracy		-5		+5	Deg C
1.5.8.7		MR Head Voltage Common Mode	Center of Selected Head	-100		100	mV
1.5.8.8		MR Head Voltage, Diff	Selected Head	100		700	mV
1.5.8.9		Unselected MR Current			0.1		mA
1.5.8.10		Differential Volt Gain	Vin=1mVp-p @20 MHz,	83	100	117	V/V
1.5.8.11			50 Ω R_{SOURCE}	125	150	175	V/V
1.5.8.12			RVORI = 0	167	200	233	V/V
1.5.8.13				208	250	292	V/V
1.5.8.14		Differential Trans-conductance	1 mV pp input RVORI = 1	V_{GAIN}/1350	V_{GAIN}/1000	V_{GAIN}/650	mhO
1.5.8.15		Programmable Voltage Bandwidth	Vin=1mVp-p, -3dB 50 Ω Rmr, Lmr=30 nH	150	180		MHz
1.5.8.16				200	240		MHz
1.5.8.17				250	300		MHz
1.5.8.18				300	360		MHz
1.5.8.19		Input Noise Voltage, V_n	5MHz-150MHz avg, Excludes I_n and R_{mr} thermal noise.		.5	.6	nV/√Hz
1.5.8.20		Input Noise Current, I_n	R_{mr}=50 ohms		6	8.5	pA/√Hz

Type (T): * = no ATE, R= For Reference Only

READ CHARACTERISTICS (CONTINUED)

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.8.21		Noise Figure, N.F.			1.41		dB
1.5.8.22		Differential Input Resistance	Vin=1mVp-p @ 10MHz,		1K		Ω
1.5.8.23		Diff Input Capacitance	Vin=1mVp-p @ 10MHz	1	5	9	pF
1.5.8.24		Input Dynamic Range	gain falls to 90% of its small signal value	3	5		mV
1.5.8.25		CMRR – output referred	Vin=100mVp-p @10MHz	55			dB
1.5.8.26		PSRR – output referred	100mVp-p on VCC or VEE, @10 MHz	40			dB
1.5.8.27		Channel Separation	Unselected Channels driven with 100mVp-p @10MHz	45			dB
1.5.8.28		Output Offset Voltage	RVORI = 0			60	mV
1.5.8.29		Output Resistance Single Ended	RVORI = 0			40	Ω
1.5.8.30		Output Current	RVORI = 0	3	3.4	3.8	mA
1.5.8.31		RDX/RDY Common Mode Output Voltage	RVORI = 0	Vcc-3.36	Vcc-3	Vcc-2.92	V
1.5.8.32		RDX,RDY Bias Current	RVORI = 1 VRDX,RDY = 2.4V	0.7	1.0	1.2	mA

Type (T): * = no ATE, R= For Reference Only

$$N.F. = 10 * \log_{10}\left[1 + \frac{V_n^{\,2} + (I_n * R_{MR})^2}{4KT * R_{MR}}\right]$$

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified
Iw=50mA, Ltot=60 nH, Rh=10 Ohm

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.9.1		Write Current Range		9.44		50.4	mApk
1.5.9.2		Write Current Accuracy	VCC = 5.0 V VEE = -5.0V	-7		+7	%
1.5.9.3		Differential Head Voltage Swing	Open Head	12.7	16		Vp-p
1.5.9.4		Unselected Head Current	DC		0.1		mA
1.5.9.5		Unselected Head Current	AC		1		mApk
1.5.9.6		Head Differential Damping AC Resistance	I_{DAMP}=1.5mA		260		Ω
1.5.9.7		Head Differential Damping DC Resistance			10K		Ω
1.5.9.8		Head Differential Output Capacitance				8	pF

Type (T) * = no ATE, R= For Reference Only

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified
Rmr=50 Ohm, 10% variation ; CL (RDX,RDY) < 20pF ; Iw=50mA
RL (RDX, RDY) = 1K; Ltotal = 60 nH, Rh = 10 ohm ; F (WDX/WDY)=10MHz

SPEC #	T	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5.10.1		Read to Write Switching	To 90% of write current			50	nS
1.5.10.2		Write to Read Switching	Note 1			300	nS
1.5.10.3		Sleep to Read	Note 1			100	uS
1.5.10.4		Idle to Read	Note 1			20	uS
1.5.10.5		HSx to Read	CV Mode, Note 1, Note 2			8.6	uS
1.5.10.6		HSx to Read	CC Mode, Note 1, Note 2 Imr = 5 mA			1	uS
1.5.10.7		Safe to Unsafe	Write mode, from last WDX/WDY transition			1	uS
1.5.10.8		Unsafe to Safe	Fault cleared, from first positive (WDX-WDY) transition			500	nS
1.5.10.9		Write Propagation Delay	From 50% point			5	nS
1.5.10.10		Write Current Rise/Fall Time	10% to 90%, L_{TOTAL}=60nH, C_h=3pF		0.65	0.8	nS
1.5.10.11		Write Current Asymmetry	Shorted Head			0.1	nS

Type (T) * = no ATE, R= For Reference Only

NOTE1: Read signal recovery criteria is defined in terms of baseline and signal envelope. Recovery times are specified as the time it takes for the DC baseline at the reader output to settle within ±20mV of its final value and the signal envelope at RdOut to settle within 90% of its final value. The reader output is measured at the load shown in Fig. 4.

NOTE 2: Switching specs for modes accessed through serial port do not take into account any time needed to write to the serial port.

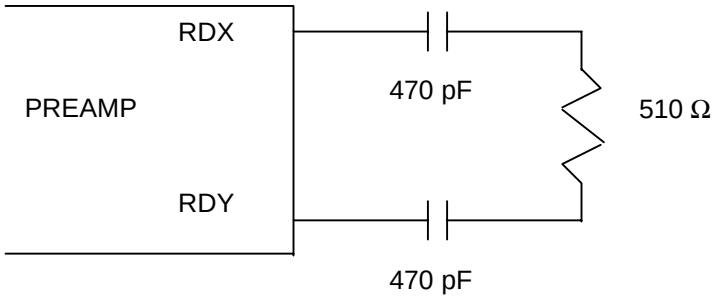
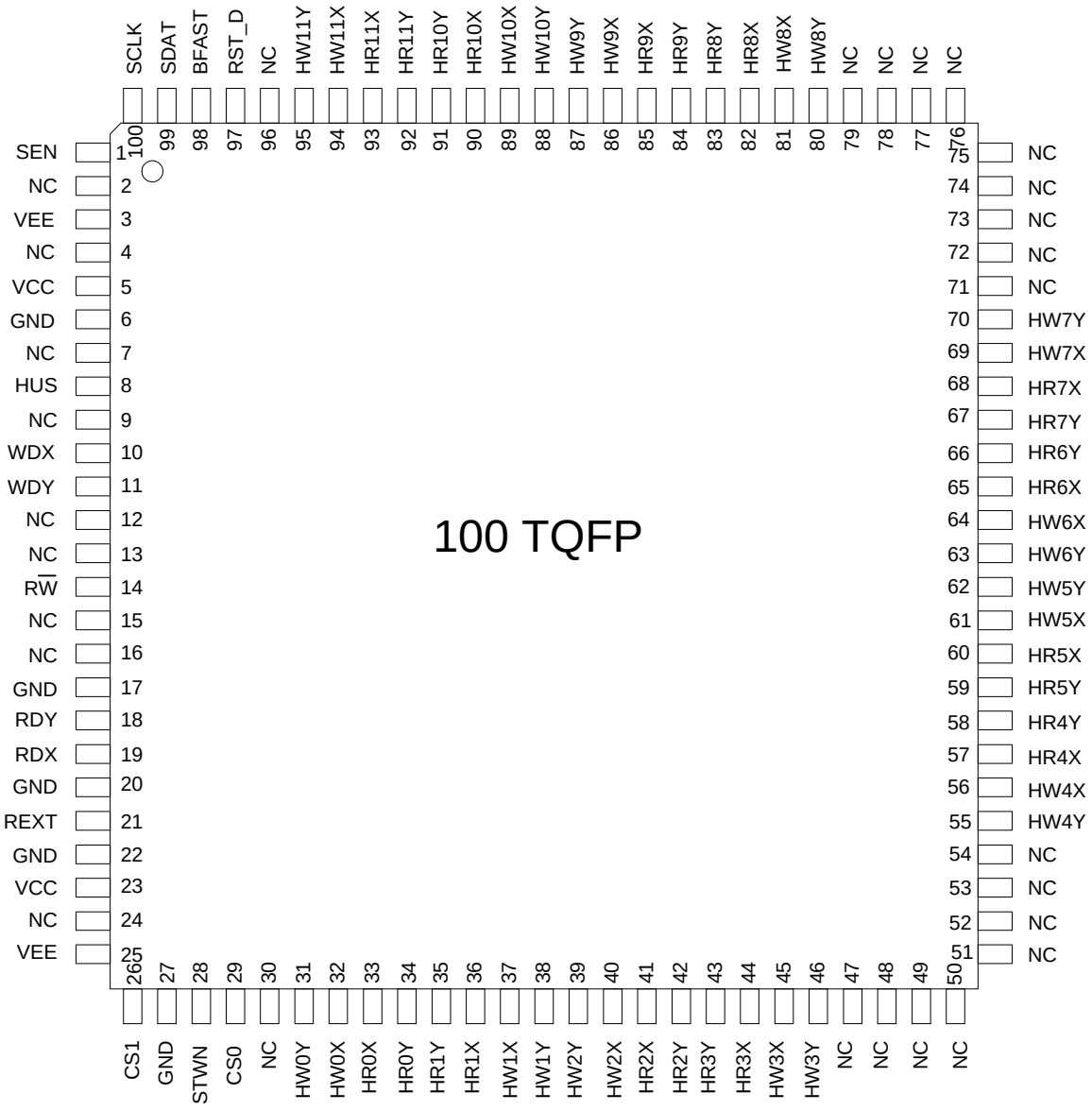


FIGURE 4: Reader Output Load

PACKAGE PIN DESIGNATIONS



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SSI 32R1608CR
+5 V, 4,8 - Channel MR Read/Write Device

Preproduction

March 1999

DESCRIPTION

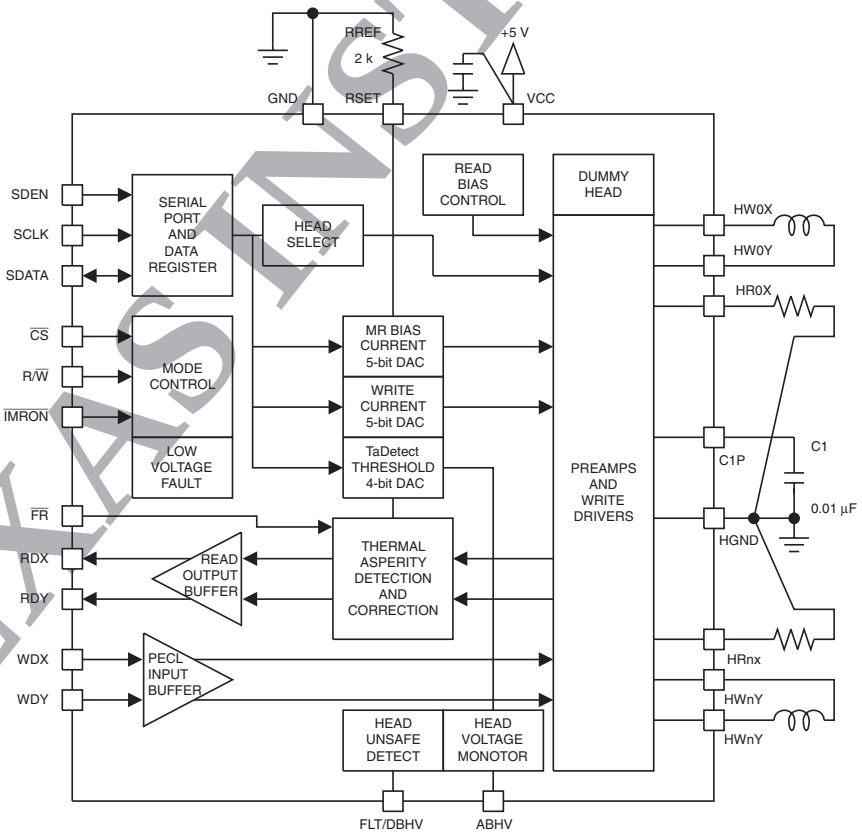
The SSI 32R1608CR is a BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive read and thin film write composite recording heads. It provides a low noise MR head amplifier, MR bias current control, thin film write driver, write current control, thermal asperity detection and correction, and TFH fault detection circuit for up to eight channels. The device features programmable read gain, write damping resistance and thermal asperity threshold level. The device allows multiple channel write functions for servo writing. Half or all of the heads can be simultaneously selected in the servo write mode. Control of features and thresholds is provided through a serial port interface. The SSI 32R1608CR requires a single 5 V supply.

FEATURES

- **One side grounded input, fully differential output**
- **Unselected read/write heads at GND potential**
- **Thermal asperity detection and compensation**
- **Fast recovery mode**
- **MR resistor measurement mode**
- **MR bias current range = 4.25 to 13.55 mA (5-bit)**
- **MR resistor range = 40 to 65 Ω**
- **Programmable read gain = 100/200 V/V @50 Ω 8.75 mA**
- **Input equivalent noise 0.85 nV/√Hz @50Ω (1 to 50 MHz)**
- **Write current rise/fall time 2.0 ns (Lh = 185 nH, Rh = 21 Ω, Iw = 30.32 mA)**

(continued)

BLOCK DIAGRAM



SSI 32R1608CR
+5 V, 4,8 - Channel
MR Read/Write Device

FEATURES (continued)

- Write current range = 10 to 45 mA (5-bit)
- Programmable write damping resistor (2-bit)
- PECL no flip-flop
- Rail to rail head swing
- Servo write (half bank, all bank write)
- Power fault protection

FUNCTIONAL DESCRIPTION

The SSI 32R1608CR addresses four terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with TTL pins $\overline{CS}$, R/$\overline{W}$, $\overline{IMRON}$ and the serial port as shown in the Table 1. The $\overline{CS}$, R/$\overline{W}$ and $\overline{IMRON}$ inputs have internal pull-up resistors so that when left opened, they will default to the TTL High state.

The serial port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold level and mode.

WRITE MODE

Taking R/$\overline{W}$ low in non-idle mode selects write mode. Write current is enabled to the selected channel and write data (WDX/WDY) controls the write current polarity. Head current is toggled between the X and Y side of the selected head on each transition of the differential PECL signal WDX-WDY. When WDX is higher than WDY, the current flows from X (HWnX) to Y (HWnY), (i.e., the X side of the head voltage is higher than the Y side).

Write current magnitude is controlled by a 5-bit on board DAC. The DAC is programmed via the serial port. The magnitude of the write current (0-pk) is given by:

$$Iw\ (mA) = 10 + \frac{35}{31} \bullet N$$

where RREF = 2.0 kΩ and N = 0,1 ... 31 is the decimal value of serial port register bits IW0:IW4.

Note that the actual head current Ix,y is given by:

$$Ix,y\ (mA) = \frac{Iw}{1 + \frac{Rh}{Rd}}$$

where Rh is the head DC resistance and Rd is the damping resistor.

TABLE 1: Mode Selection

$\overline{SLP}$ (MODE REG)	$\overline{IDL}$ (MODE REG)	R/$\overline{W}$	$\overline{IMRON}$	BNK0 • BNK1 (WRITE/MODE REG)	MODE
0	X	X	X	X	Sleep
1	0	X	1	X	Idle, IMR off
1	0	X	0	X	Idle, IMR on
1	1	1	1	X	Read, IMR off
1	1	1	0	X	Read, IMR on
1	1	0	1	0	Write, IMR off
1	1	0	0	0	Write, IMR on
1	1	0	1	1	Servo write, IMR off

NOTES: Optional $\overline{CS}$ input pin is logically OR'd with $\overline{IDL}$ bit to set idle mode:
Either $\overline{CS}$ = 1 or $\overline{IDL}$ = 0 sets chip to idle mode. $\overline{CS}$ = 0 and $\overline{IDL}$ = 1 for non idle modes.

SERVO BANK WRITE MODE

By setting both serial port register bits BNK0 and BNK1 high when in write mode, the chip goes into servo write mode. Heads activated in servo mode can be selected by HS0, HS1 bits, as shown in Tables 4 and 5. Bit HS0 controls the upper half channels, and HS1 controls the lower half channels. Setting both HS0 = HS1 = 1 selects all heads. It is recommended that the chip operate in a well controlled ambient temperature when servo write is active to prevent excessive junction temperatures. The thermal resistance of the package varies by mount conditions.

READ MODE

By taking the R/$\overline{W}$ pin high in non-idle mode selects read mode which activates the MR bias current generator and low noise differential amplifier. $\overline{IMRON}$ must be low to activate the MR bias current through the designated head. When $\overline{IMRON}$ is high, MR current is disabled, but C1P capacitor voltage is retained to improve recovery time. The outputs of the read amplifier RDX/RDY are emitter followers and are in phase with the resistivity change at the selected input port (HRn) where the respective MR head is attached. The read mode gain is set to one of four values based on the G1:G0 bits of Serial Port Mode Register.

The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port, while the reference current is set by an external resistor from pin RREF to ground (Vref = 2.0 VDC). The magnitude of the bias current is set according to the following equation:

$$Imr\ (mA) = 4.25 + \frac{9.3}{31} \bullet N$$

where RREF = 2.0 kΩ and N = 0,1,...31 is the decimal value of Serial Port Register bits IR0:IR4.

In read mode, the device requires one external capacitor. Capacitor C1, connected between C1P and HGND is the bias loop control capacitor. The value of C1 will effect the lower frequency corner of the read amplifier.

FAST WRITE TO READ RECOVERY MODE

The FWR bit of the Mode Register enables the fast write to read recovery mode. In this mode, the lower corner of the read amplifier is shifted up to 5 MHz (nominal) upon assertion of the R/$\overline{W}$ signal. The lower corner is held at 5 MHz for 900 ns, then returned to the normal frequency. The corner frequency shift in this mode eliminates the low frequency content of the transient read signal, thus improving the write to read recovery time.

IDLE MODE

$\overline{IDL}$ bit (D1) in Mode Register of the serial port controls idle mode. The internal reference voltage and DACs are activated when $\overline{IDL}$ bit is set to low in non-sleep mode. MR bias current can be activated by $\overline{IMRON}$ pin to allow quick recovery to read mode or disabled to get lower power consumption. When IMRON is set active (low), MR bias current is diverted to the internal dummy head. Idle mode can be controlled by either $\overline{IDL}$ bit or $\overline{CS}$ pin. Both $\overline{IDL}$ = 1 and $\overline{CS}$ = 0 are required to place the chip into active mode.

SLEEP MODE

The chip is set to sleep mode by setting $\overline{SLP}$ bit (D0 in Mode Register). Only the serial port and voltage fault monitor are active in this mode. The $\overline{SLP}$ bit overrides all other mode control setting bits and pins.

FUNCTIONAL DESCRIPTION (continued)

HUS OPERATION

The FLT/DBHV pin is an open collector output line, multiplexed between two functions. When MR measurement mode is inactive, the output is a fault status output and has the following polarity. The FLT output flags low when the chip is in a voltage fault condition, regardless of operating mode. It also flags low when an invalid head is selected on 4-channel device (bit 2 of the HS/IMR Register).

Read Mode

A low on the FLT pin indicates one of the following unsafe conditions:

- Device in TA fast recovery mode (triggered by TA event)
- TA event detected, if enabled (programmable threshold).
- Read head input short to GND
- Low Vcc
- Open head for longer than 400 ns

Write Mode

A high on the FLT pin indicates one of the following unsafe conditions:

- An open head, valid up 10 MHz
- Head shorted to ground
- Write data too slow
- An open reference resistor
- Low Vcc (reported) - the writer is disabled for the duration of the fault condition

Servo Bankwrite Mode

A high on the FLT pin indicates the following unsafe condition:

- Low Vcc (reported) - The writer is disabled for the duration of the fault condition

TABLE 2. Thermal Asperity Mode Control

			TA MODE	
$\overline{FR}$	FRON (MODE REG)	TAD (TA REG)	CORRECTION MODE	TA DETECTOR (FLT REPORTED)
0	X	0	Fast recovery	Off
0	X	1	Fast recovery	On
1	0	0	Off	Off
1	0	1	Off	On
1	1	0	Fast recovery	Off
1	1	1	On-the-fly compensation and fast recovery by TA trigger	On

NOTE: $\overline{FR}$ is pulled high internally on 4-channel version. No $\overline{FR}$ pin available on 30VT packaged part.

THERMAL ASPERITY DETECTION AND COMPENSATION

The thermal asperity circuitry can be controlled by the combination of the $\overline{FR}$ pin, serial port bits FRON and TADet, and the thermal asperity threshold setting (TA3:TA0). The thermal asperity can be set to on of 4 modes: TA off, TA detection only, TA fast recovery (retry mode), and TA correction triggered by TA detect (on-the-fly-correction). See Table 2 for thermal asperity mode settings.

In TA detection only mode, the FLT pin will indicate a TA event when the signal crosses the TA threshold voltage. The threshold is programmable through use of the TA3:TA0 serial port bits (see threshold equation below). The FLT output will indicate the TA fault for as long as the signal remains above the TA threshold plus some hysteresis.

In TA fast recovery mode, the lower corner frequency of read amplifier is shifted up to 5 MHz (nom) to eliminate low frequency component from the read signal. This mode can be entered by either activating the FRON bit with TA detection disabled, or by setting the $\overline{FR}$ pin low. Note that there is no $\overline{FR}$ pin available with the 4-channel version. Setting the $\overline{FR}$ pin low overrides other TA correction modes, placing the read amplifier into fast recovery mode for as long as the pin is held low. The TA fast recovery mode is used primarily for read retry.

In the TA on-the-fly correction mode, the chip detects the peak voltage of the thermal asperity and subtracts the peak from the read output (called TA compensation). In addition, the lower corner frequency is shifted to 5 MHz as in fast recovery mode. The amplifier returns to its normal operating state 5 µs after the uncompensated signal has returned below the TA threshold voltage plus some hysteresis. The FLT pin flags low during the correction period.

The threshold level for the thermal asperity detector is programmable through the serial port according to the following:

$$Vta\ (mV) = 50 + (750/15) \bullet N$$

where RREF = 2.0 kΩ and N = 0,1...15 is the decimal value of serial port register bits TA0:TA3. Threshold level is referred to output level.

MR RESISTANCE MEASUREMENT MODE

MR resistance measurement can be activated in read mode by setting MRM bit (D4) in the Mode Register. The ABHV and DBHV outputs are activated in this mode. The ABHV output is a buffered MR head voltage with gain of 5 V/V. The DBHV/FLT pin is a logic output. When the head voltage stays inside of set window, it flags high.

VOLTAGE FAULT MONITOR

During power up or power fault condition, the voltage monitor disables the chip from any active mode. The Serial Data Registers are reset to sleep mode with default power-on setting values. The threshold voltage for the serial port power-on reset is 1.8 V (typical). The threshold voltage for VCC fault, which also disables the write mode but does not reset the Serial Data Registers, is 4.1/3.8 V (typical).

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold and mode. The serial port bit map is shown in Table 3.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/$\overline{W}$ bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0 = 1, S1 = 0, and S2 = 0 for R/$\overline{W}$ amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits (see Serial Port Bit Map).

Asserting the serial port enable line SDEN (TTL) initiates a transfer, SDATA (TTL) is clocked into the Internal Shift Register by the rising edge of SCLK (TTL). A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

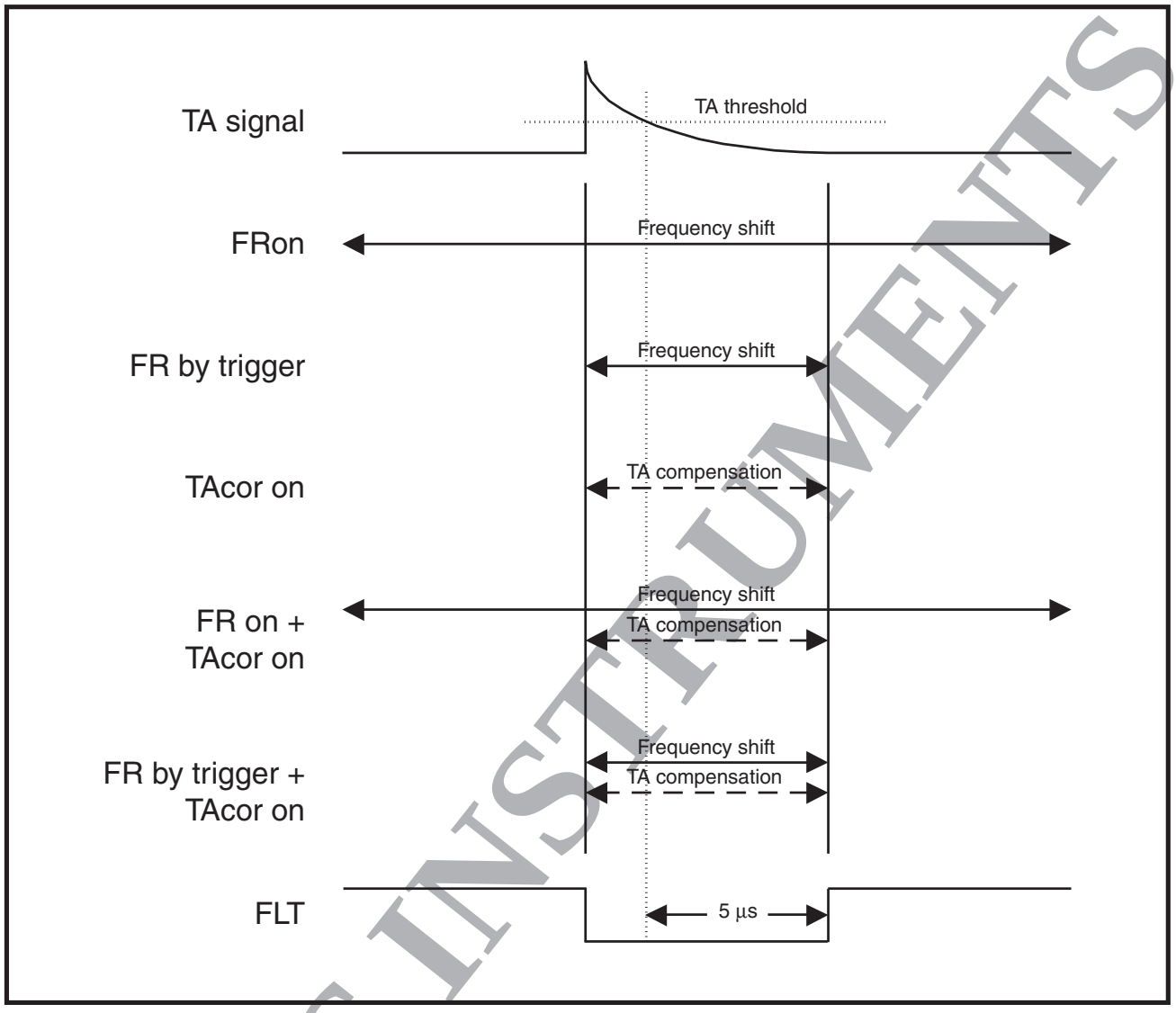


FIGURE 1: Thermal Asperity Modes

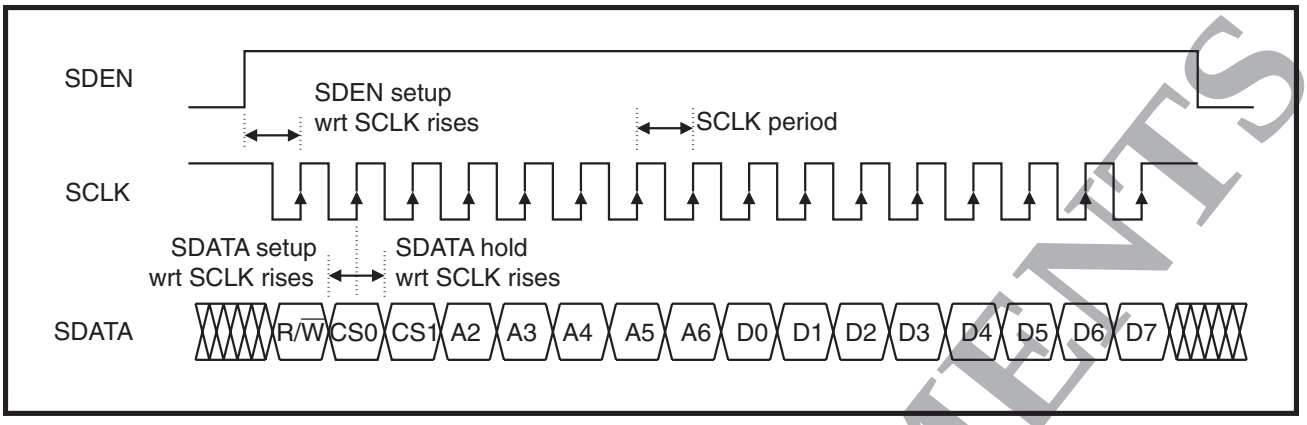


FIGURE 2: Serial Port Timing

TABLE 3. Serial Port Bit Map

REG	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	1	0	0	VS0	VS1	VS2	CH	1
HS/IMR	100	1000	HS0	HS1	HS2	IR0	IR1	IR2	IR3	IR4
WRITE	100	0100	IW0	IW1	IW2	IW3	IW4	0	WCB	BNK0
TA	100	1100	0	DR0	DR1	TADET	TA0	TA1	TA2	TA3
MODE	100	0010	$\overline{SLP}$	$\overline{IDL}$	G0	G1	MRM	FRON	BNK1	FWR

ID Register is read only.

All Data bits are set to 0 by at reset condition, i.e.; power-up or voltage fault condition, except ID Register.

REGISTER DESCRIPTION

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port read/write bit is not shown.

ID REGISTER (READ ONLY REGISTER) **ADDRESS = 0000 001**

BIT	NAME	DESCRIPTION
7		ID bit = 1, internally set by TI SPG
6	CH	Channel version 1 = 4-channel version 0 = 8-channel version
5:3	VS2:VS0	Device revision bits. Initial revision for 1608CR is 100 (D5:4:3)
2:0		ID bits = 001, internally set by TI SPG

HS/IMR REGISTER **ADDRESS = 0001 001**

7:3	IR4:0	MR bias current setting (see Read Mode Description for bias equation) 11111 = maximum MR bias current 00000 = minimum MR bias current
2	HS2	8-channel head select bit for heads 4 through 7 0 = Select heads 0 through 3. Correct setting for 4 channel version 1 = Select heads 4 through 7 for 8 channel version. Invalid head select for 4 channel version, FLT flags low and no head selected
1:0	HS1:HS0	Head select bits, see Tables 4 and 5 for head select bit maps

WRITE REGISTER **ADDRESS = 0010 001**

7	BNK0	Servo bank control bit, operate in conjunction with BNK1 in Mode Register 1 = Servo bank mode (both BNK0 and BNK1 must be 1 to enable servo) 0 = Servo bank mode off
6	WCB	Write current boost 1 = Enable write current boost 0 = Disable write current boost
5		Not used. User setting = 0
4:0	IW4:0	Write current magnitude (see Write Mode Description for equation) 11111 = maximum write current 00000 = minimum write current

TA REGISTER **ADDRESS = 0011 001**

BIT	NAME	DESCRIPTION
7:4	TA3:0	Thermal asperity threshold (see Thermal Asperity Description section for equation) 1111 = Maximum TA threshold setting 0000 = Minimum TA threshold setting
3	TADet	Thermal asperity detector control 1 = Enable TA detector 0 = Disable TA detector
2:1	DR1:0	Write damping resistor setting, 11 = 110 Ω 10 = 150 Ω 01 = 240 Ω 00 = 600 Ω
0	Res	Reserved for TI Storage Products internal use User setting = 0

MODE REGISTER **ADDRESS = 0100 001**

7	FWR	Fast write to read enable 1 = Fast write to read enabled 0 = Fast write to read disabled
6	BNK1	Servo bank control bit, operate in conjunction with BNK0 in Write Register 1 = Servo bank mode (both BNK0 and BNK1 must be 1 to enable servo) 0 = Servo bank mode off
5	FRON	Fast recovery mode enable 1 = Fast recovery mode enabled (low corner frequency shift) 0 = Fast recovery mode disabled
4	MRM	MR measurement mode 1 = Enables MR measurement mode. Activates digital and analog BHV 0 = Disables MR measurement mode
3:2	G1:G0	Read amplifier gain select 11 = 200 V/V 10 = 155 V/V 01 = 126 V/V 00 = 100 V/V
1	$\overline{IDL}$	Idle control bit 0 = Idle mode enabled
0	$\overline{SLP}$	Sleep control bit 0 = Sleep mode enabled - overrides all other control modes

TABLE 4: Head Selection, 4 Channel Version

HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	X
0	1	1	2,3
1	0	2	0,1
1	1	3	All heads

TABLE 5: Head Selection, 8 Channel Version

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	0	X
0	0	1	1	4,5,6,7
0	1	0	2	0,1,2,3
0	1	1	3	All heads
1	0	0	4	X
1	0	1	5	4,5,6,7
1	1	0	6	0,1,2,3
1	1	1	7	All heads

NOTE: Servo mode head selection controlled by HS0 and HS1 bits only

PIN DESCRIPTION

Pin types are defined as: A = Analog; D = Digital; G = Ground; I = Input; O = Output; P = Power

NAME	TYPE	DESCRIPTION
RREF	I/O	External resistor connection to set reference current for current DACs
HWnX, HWnY	O	Inductive write head connection
HRn	I/O	MR read head connection
HGND	I/O	MR read head current return
FLT/DBHV	O	FAULT / DIGITAL BUFFERED HEAD VOLTAGE: An open collector output Fault mode: Read mode: A low indicates abnormal read condition Write mode: A high indicates abnormal write condition MR measure mode: A high indicates the head is in proper range
ABHV	O	Analog buffered head voltage monitor output
R/$\overline{W}$	I	READ/WRITE: TTL, with internal pull-up
RDX,RDY	O	Differential read data output
$\overline{CS}$	I	CHIP SELECT: Active low with internal pull-up
GND	I	Ground
VCC	I	+5 V power supply
C1P	I	Bias loop control capacitor connected to HGND
$\overline{IMRON}$	I	MR CURRENT ON: Activates MR bias in write mode - TTL, with internal pull-up
SDEN	I	SERIAL PORT ENABLE: TTL, with internal pull-down
SDATA	I/O	SERIAL DATA: TTL, with internal pull-up
SCLK	I	SERIAL CLOCK: TTL, with internal pull-down
WDX,WDY	I	Differential PECL write data inputs
$\overline{FR}$	I	Fast recovery control (8-channel version only)

ELECTRICAL SPECIFICATION

Unless otherwise specified, Rmr = 50 Ω, Imr = 8.75 mA, Rref = 2.0 kΩ, CX1 = 0.01 µF, Lhw = 185 nH, Rhw = 21 Ω, Iw = 30.32 mA, Vcc = 5.0 V

ABSOLUTE MAXIMUM RATINGS

Operation beyond maximum ratings may result in permanent damage to the device

PARAMETER		RATINGS
DC Supply Voltage	VCC	-0.3 to 6 VDC
Logic Input Voltage	TTL	-0.3 to VCC + 0.3 VDC
	PECL	0 to VCC VDC
Write Current	Iw	70 mA
MR Bias Current	I_{MR}	30 mA
Write Head Voltage	V_{WH}	-0.3 V to Vcc + 0.3 V
Read Head Voltage	V_{MR}	0 to 0.6 V
Output Current	RDX,Y	-10 mA
	FLT/DBHV	+8 mA
Storage Temperature	Tstg	-65 to 150 °C
Operating Junction Temperature	Tj	+135 °C

RECOMMENDED OPERATION CONDITIONS

DC Supply Voltage	VCC	4.5 to 5.5 VDC
Write Head Load Range	L_H	60 to 250 nH
Write Head Resister Range	R_{WH}	5 to 25 Ω
MR Head Range	R_{MR}	40 to 65 Ω
Operating Ambient Temperature	Ta	0 to 70 °C

DC CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	VCC	Read IMR off		10	15	mA
		Read IMR on, Imr = 8.75 mA		36	50	mA
		Write IMR off, Iw = 30.32 mA		57	80	mA
		Write IMR on, Iw = 30.32 mA Imr = 8.75 mA		67	94	mA
		Servo (2-channel), Iw = 24 mA Vcc = 4.5 V		75	90	mA
		Servo (4-channel), Iw = 24 mA Vcc = 4.5 V		135	165	mA
		Servo (8-channel), Iw = 24 mA Vcc = 4.5 V		255	300	mA
		Idle IMR off		8	12	mA
		Idle IMR on, Imr = 8.75 mA		28	40	mA
		Sleep		0.6	2	mA
VCC Fault Voltage		Fault detected	3.6	3.8	4.0	V
		Fault removed	3.9	4.1	4.3	V
POR VCC Voltage		Reset removed		1.9	2.3	V

DIGITAL INPUT/OUTPUT

Input High Voltage	V_{IH1}	TTL	2.0			VDC
Input Low Voltage	V_{IL1}	TTL			0.8	VDC
Input High Current	I_{IH1}	V_{IH1} = 2.0 V			160	µA
Input Low Current	I_{IL1}	V_{IL1} = 0.8 V	-400			µA
Input High Voltage	V_{IH3}	PECL	2.0		Vcc - 0.6	VDC
Input Low Voltage	V_{IL3}	PECL	1.2		V_{IH3} - 0.3	VDC
Input Δ Voltage			0.3	0.8	2.0	VDC
Input High Current	I_{IH3}	V_{IH3} = 4.0 V		5	100	µA
Input Low Current	I_{IL3}	V_{IL3} = 3.2 V		5	100	µA
Output High Current	I_{OH}	FLT/DBHV VOH = VCC			20	µA
Output Low Voltage	V_{OL}	FLT/DBHV I_{OL} = 2 mA			0.5	V

ELECTRICAL SPECIFICATION (continued

SERIAL PORT TIMING, READ/WRITE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		50			ns
SCLK Low Time	T_{CKL}		30			ns
SCLK High Time	T_{CKH}		30			ns
Enable to SCLK	T_{SENS}		10			ns
SCLK to Disable	T_{SENH}		40			ns
Data Set-up Time	T_{DS}		5			ns
Data Hold Time	T_{DH}		5			ns
SDEN Min Low Time	T_{SL}		160			ns

SERIAL PORT TIMING, WRITE ONLY

SCLK Clock Period	T_C		50			ns
SCLK Low Time	T_{CKL}					ns
SCLK High Time	T_{CKH}					ns
Enable to SCLK	T_{SENS}					ns
SCLK to Disable	T_{SENH}					ns
Data Set-up Time	T_{DS}					ns
Data Hold Time	T_{DH}					ns
SDEN Min Low Time	T_{SL}					ns

CURRENT DAC REFERENCE

Voltage Reference	Vref		1.9	2.0	2.1	V
Reference R Range	Rref			2.0		kΩ
Reference Current	Iref			1		mA

READ CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		40	50	65	Ω
MR Bias Current		4.25		13.55	mA
MR Bias Current Resolution			5		bit
LSB	Rref = 2 kΩ		300		µA
MR Current Tolerance		-6		+6	%
MR Head DC Voltage Range				0.7	V
Unselected Head Current				10	µA
Input Resistance	Rmr = 50 Ω, Imr = 8.75 mA		5		Ω
Differential Voltage Gain	R_{MR} = 50 Ω, Imr = 8.75 mA 1 mVp-p @ 10 MHz G1G0 = 00	82	100	115	V/V
	G1G0 = 01	105	126	147	V/V
	G1G0 = 10	128.7	155	181.4	V/V
	G1G0 = 11	166	200	234	V/V
Read Gain Constant	Av • (RMR + RIN) G1G0 = 00		5500		Ω
	G1G0 = 01		6930		Ω
	G1G0 = 10		8745		Ω
	G1G0 = 11		11000		Ω
Bandwidth	Lower -3 dB, C1 = 0.01 µF		0.55	0.7	MHz
	Lower -3 dB, fast recovery		5	7	MHz
	Higher -1 dB		90		
	Higher -3 dB, Rmr = 50 Ω Imr = 8.75 mA	150	185	210	MHz
Input Noise	R_{MR} = 50 Ω, Imr = 8.75 mA F = 1 to 50 MHz		0.85		nV/√Hz
Dynamic Range	Gain falls to 90% @ 5 MHz	3.5			mV
Output Offset Voltage		-200		200	mV
Output Current		1.5	2.2		mA
Output Voltage	RDX,RDY		VCC - 2.3		V
Output Resistance		30	50	65	Ω
PSRR	@25 MHz		46		dB
Channel Separation	@25 MHz	45	60		dB

ELECTRICAL SPECIFICATION (continued

WRITE/SERVO CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range		10	30.32	45	mA
Write Current Resolution			5		bit
LSB			1.13		mA
Write Current Accuracy @ Servo		-9.5		+9.5	%
Differential Head Swing	Open head		9		Vp-p
	Transient		10		Vp-p
Unselected Head Current	DC			50	µA
	Transient			1	mA pk
Damping Resistor	<RD0,RD1> = <0,0>		600		Ω
	<RD0,RD1> = <1,0>		240		Ω
	<RD0,RD1> = <0,1>		150		Ω
	<RD0,RD1> = <1,1>		110		Ω
Differential Output Capacitance				15.5	pF

HEAD VOLTAGE MONITOR

DBHV Upper Threshold	HUS = high to low	571	614	657	mV
DBHV Lower Threshold	HUS = low to high	339	365	383	mV
ABHV Gain		4.75	5	5.25	V/V
ABHV Output Range		0.5		2.75	V
ABHV Output Current	Output drops to 90%	1			mA
ABHV Output Offset		-120	-20	80	mV

THERMAL ASPERITY DETECTION/CORRECTION/FAST RECOVERY

TA Detection Range	At output before correction	100			mV
TA Detection Resolution			4		bit
LSB	Rref = 2 kΩ		50		mV
Lower Corner Frequency	Fast recovery mode		5	7	MHz
TA Detection Delay			30	100	ns
TA Compensation Delay			0.4	1.0	µs
TA Compensation Timer			5		µs

SWITCHING CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Write to Read	R/$\overline{W}$	90% signal envelope, ±30 mV DC		0.4	0.8	µs
Read to Write	R/$\overline{W}$	90% of Iw		30	50	ns
Idle to Read	$\overline{CS}$	90% signal envelope, ±30 mV DC		3	15	µs
Write to Idle	$\overline{CS}$	10% of Iw			1	µs
Head Switching	HSn	90% signal envelope, ±30 mV DC		3	15	µs
Write Current Rise/Fall Time		Lh = 185 nH, Iw = 30 mA, Rh = 21 Ω, Rd = 600 Ω, 10% to 90%			2	ns
		Lh = 185 nH, Iw = 30 mA, Rh = 21 Ω, Rd = 240 Ω, 10% to 90%			2.2	ns
Head Current Delay		50% of WD to 50% of Iw			20	ns
Write Current Asymmetry		Propagation delay difference			0.5	ns

HEAD UNSAFE DETECTION

FLT Low to High		0.5	1	2	µs
FLT High to Low				200	ns
Write Data Frequency	Valid transient detector			100	MHz
	Valid open detector			10	MHz
MR Head Open Threshold		918	995	1072	MV
MR Head Short Threshold			55	75	MV

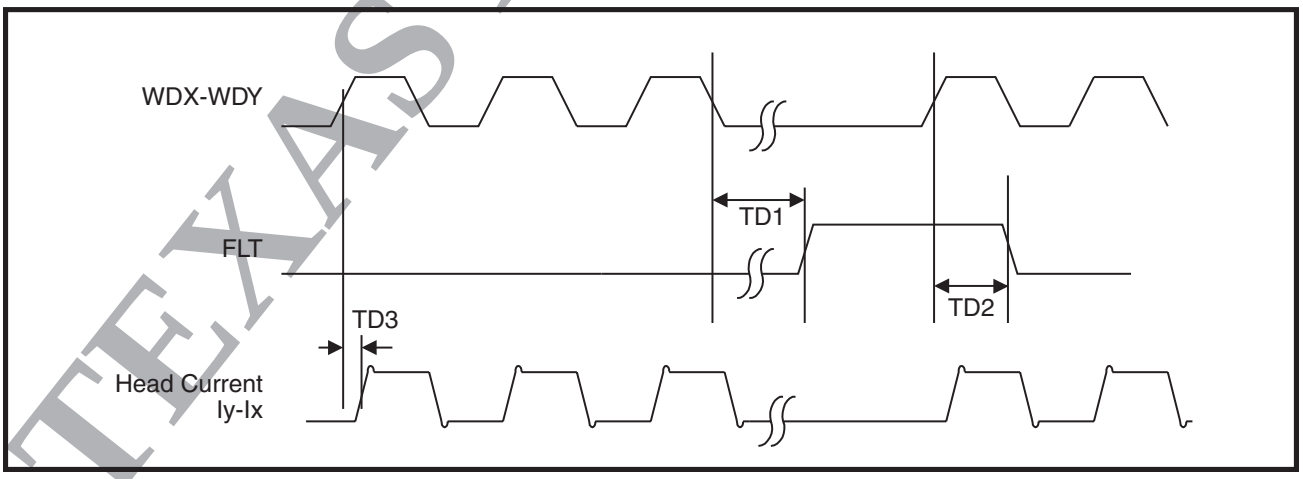
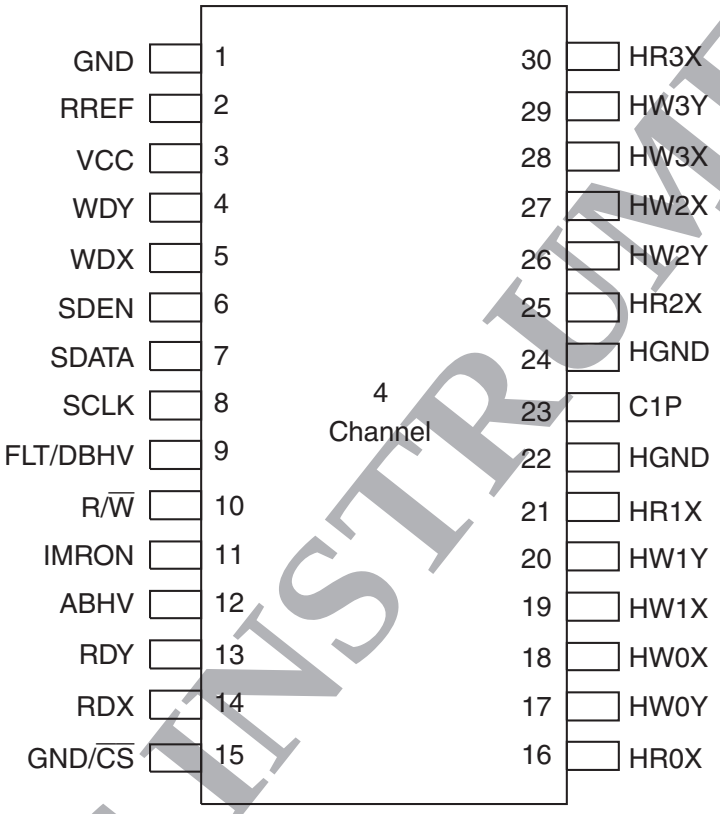


FIGURE 3: Write Current & Head Unsafe Timing

PACKAGE PIN DESIGNATIONS

(Top View)

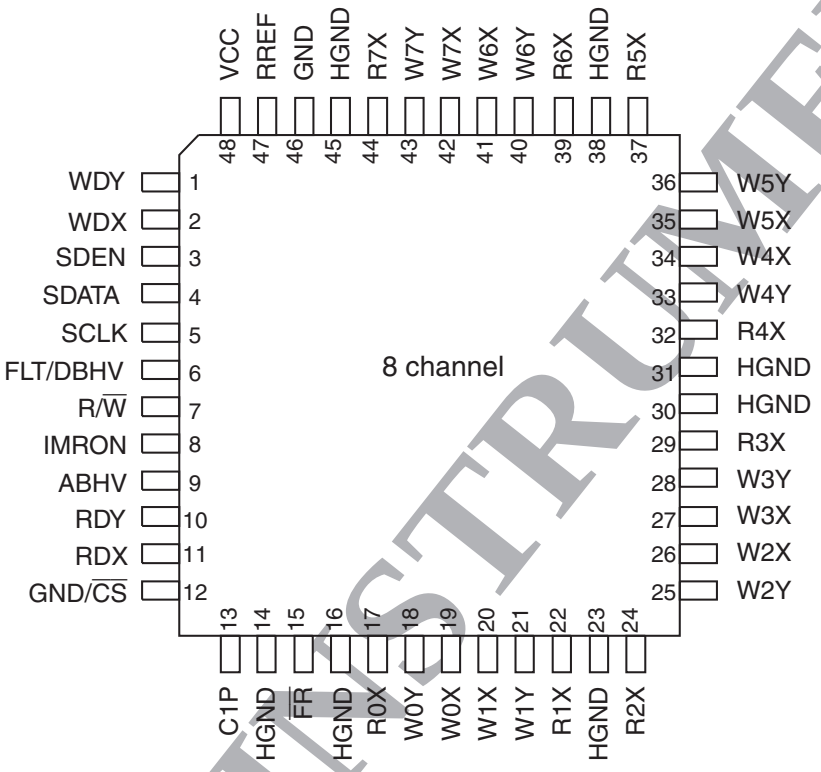


30-Lead TSSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

(Top View)



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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SSI 32R1610AR
+5 V, +8 V, 8-Channel MR/GMR Read/Write Device

Preproduction

April 1999

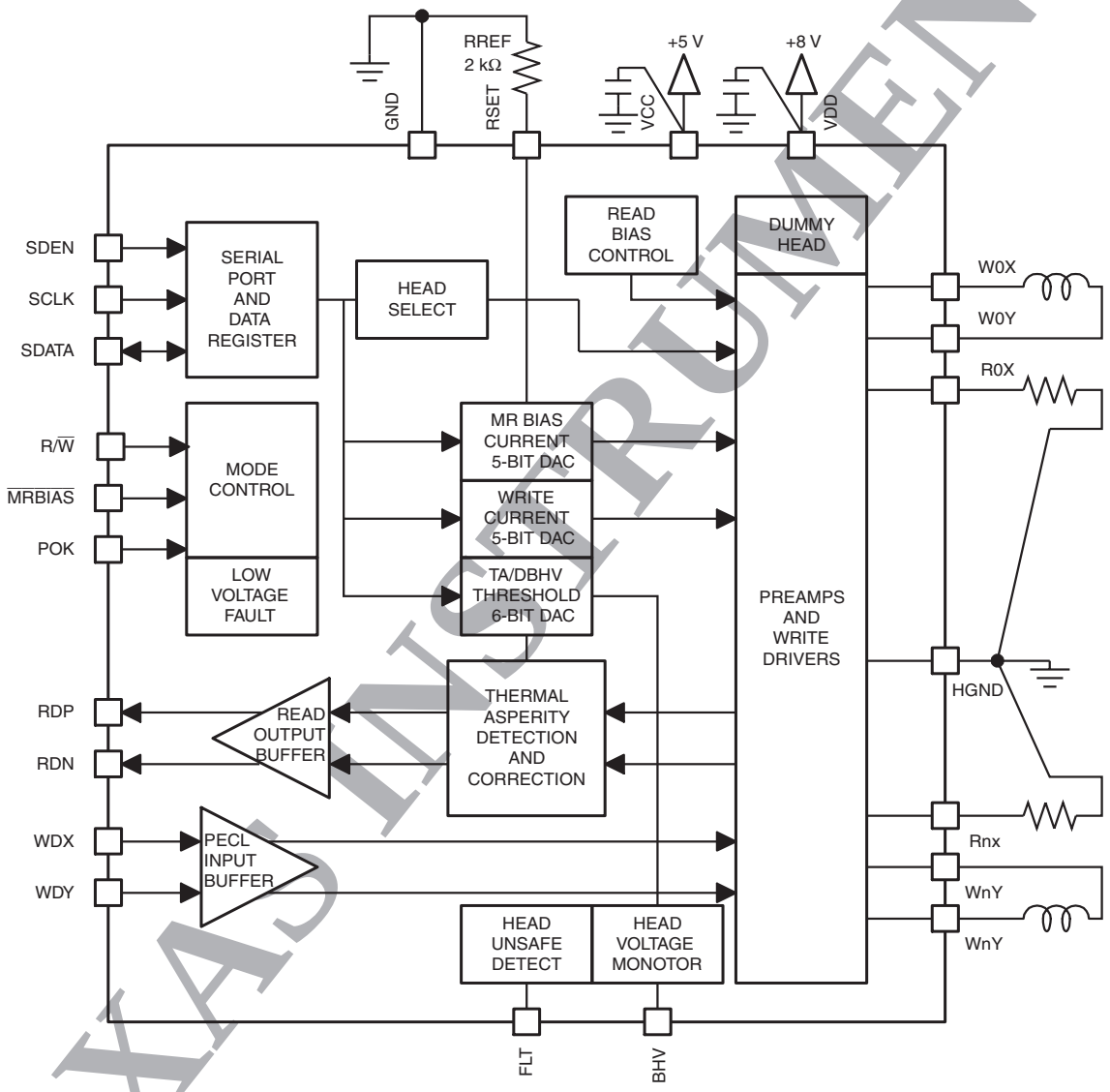
DESCRIPTION

The SSI 32R1610AR is a BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive read and thin film write composite recording heads. It provides a low noise 5 V MR head amplifier, MR bias current control, an 8 V thin film write driver, write current control, thermal asperity detection and correction, and TFH fault detection circuit for up to eight channels. The device features programmable read gain, write damping resistance and thermal asperity threshold level. The device allows multiple channel write functions for servo writing. Half or all of the heads can be simultaneously selected in the servo write mode. Control of features and thresholds is provided through a serial port interface. The SSI 32R1610AR requires a +5 V and an +8 V supply and is available in an eight channel version.

FEATURES

- **One side grounded input, fully differential output**
- **Unselected read/write heads at GND potential**
- **Thermal asperity detection and compensation**
- **MR resistor measurement mode**
- **MR bias current range = 2 to 8 mA (5-bit)**
- **MR resistor range = 35 to 80 Ω**
- **Programmable read gain constant = 9100 Ω or 13000 Ω**
- **Input equivalent noise 1.0 nV/√Hz @ 50 Ω**
- **Read frequency boost**
- **Write current range = 15 to 55 mA (5-bit)**
- **Programmable write damping resistor (2-bit)**
- **Programmable write current boost (3-bit)**
- **PECL no flip-flop**
- **Servo bank write**
- **MR bias during servo write capability**
- **Read blocking and noise capacitors integrated on chip**
- **Power fault protection**
- **3 V compatible analog and digital I/O**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 32R1610AR addresses up to 8 four-terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with TTL pins R/$\overline{W}$, $\overline{MRBIAS}$ and the serial port as shown in Table 1. The R/$\overline{W}$ and POK inputs have an internal pull-up resistor so that when left opened, it will default to the TTL High state, while the $\overline{MRBIAS}$ input has an internal pull-down resistor.

The serial port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold level and mode.

WRITE MODE

Taking R/$\overline{W}$ low with POK high in non-idle mode selects write mode. Write current is enabled to the selected channel and write data (WDX/WDY) controls the write current polarity. Head current is toggled between the X and Y side of the selected head on each transition of the differential PECL signal WDX-WDY. When WDX is higher than WDY, the current flows from X (WnX) to Y (WnY).

Write current magnitude is controlled by a 5-bit on board DAC. The DAC is programmed via the serial port. The magnitude of the write current (0-pk) is given by:

$$Iw\ (mA) = 15 + 1.29 \bullet N\ (mA\ 0\text{-}p)$$

where RREF = 2.0 kΩ and N = 0,1 ... 31 is the decimal value of Serial Port Register bits IW0:IW4.

Note that the actual head current Ix,y is given by:

$$Ix,y(mA) = \frac{Iw}{1 + \frac{Rh}{Rd}}$$

where Rh is the head DC resistance and Rd is the damping resistor (programmable).

The SSI 32R1610AR offers a write current boost feature which can enhance the write current rise time under certain load conditions. Write current boost adds additional current during the rise/fall transition of the write current output. The amount of current boost is controlled by the serial port bits WC0:WCB2. With WCB0:WCB2 set to 000, no current boosting occurs. The LSB of the WCB control is 7.5 mA (nominal). The combination of programmable write current boost and write damping resistance allows the user to adjust the write current waveform to achieve an optimized response with various load conditions.

The MR head can be bias with a programmable voltage in either write or servo mode through use of the HB3:HB0 bits in the TADC Serial Port Register. This feature provides a means to maintain the MR head voltage above ground potential during write operations. The MR bias voltage is given by:

$$V_{MR} = 30 \bullet N\ (mV)$$

where N = 0..15 is the decimal value of HB3:0.

TABLE 1: Mode Selection

$\overline{SLP}$	$\overline{IDL}$	R/$\overline{W}$	$\overline{MRBIAS}$	SBW	POK	MODE
0	X	X	X	X	X	Sleep
1	0	X	X	X	X	Idle
1	1	1	0	X	X	Read, IMR on (selected head)
1	1	1	1	X	X	Read, IMR off
1	1	0	X	0	0	Write disabled, IMR off
1	1	0	X	0	1	Write, IMR off
1	1	0	X	1	0	Servo write disabled, IMR off
1	1	0	X	1	1	Servo write, IMR off

NOTE: MR Bias voltage can be applied to selected head(s) in write or servo write modes

SERVO BANK WRITE MODE

By setting the Serial Port Register bit SBW high and placing the device in write mode with POK high, the chip goes into servo write mode. Heads activated in servo mode can be selected by HS0, HS1, and HS2 bits, as shown in Tables 4 and 5. The SSD bit must be set high in order for servo bank write mode to operate properly. It is recommended that the chip operate in a well controlled ambient temperature when servo write is active to prevent excessive junction temperatures. The thermal resistance of the package varies by mount conditions.

MR bias voltage can be applied to all active heads using bits HB3:0 as described in write section.

READ MODE

Taking the R/$\overline{W}$ pin high in non-idle mode selects read mode which activates the MR bias current generator and low noise differential amplifier. $\overline{MRBIAS}$ pin must be low to activate the MR bias current through the designated head. When $\overline{MRBIAS}$ is high in read mode, MR current is disabled. The MR bias current is kept off during write mode regardless of the state of the $\overline{MRBIAS}$ pin.

The outputs of the read amplifier RDX/RDY are emitter followers and are in phase with the resistivity change at the selected input port (RnX/HGND) where the respective MR head is attached. The read mode gain is set to one of two values based on the GAIN bit of Serial Port Mode Register.

The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port, while the reference current is set by an external resistor from pin RREF to ground (Vref = 2.0 VDC). The magnitude of the bias current is set according to the following equation:

$$Imr\ (mA) = 2 + 0.194 \bullet N$$

where RREF = 2.0 kΩ and N = 0,1,...31 is the decimal value of Serial Port Register bits IR0:IR4.

When switching from head to head, the chip selects an internal dummy head (15 Ω nominal) to discharge C1 capacitor so that the selected MR will see no current overshoot during the transition.

IDLE MODE

The $\overline{IDL}$ bit (D1) in Mode Register of the serial port controls idle mode. The internal reference voltage and DACs are activated when $\overline{IDL}$ bit is set to low in non-sleep mode. All connections to the internal C1 capacitor are opened to preserve charge on the capacitor.

SLEEP MODE

The chip is set to sleep mode by setting $\overline{SLP}$ bit (D0 in Mode Register) low. Only the serial port and voltage fault monitor are active in this mode. The $\overline{SLP}$ bit overrides all other mode control setting bits and pins.

FAULT DETECTOR

The FLT pin is an open collector output line, multiplexed between the DBHV output. When MR measurement mode is inactive (MRM = 0), the pin is a fault status output. The FLT output is asserted when the chip is in a voltage fault condition, regardless of operating mode. The FLT output is a flag only and does not interrupt the chip function.

Read Mode

A low on the FLT pin indicates one of the following unsafe conditions:

- Device in TA correction mode
- TA event detected
- Open or shorted MR element
- Vcc supply voltage fault

Write Mode

The polarity of the FLT output in write mode is programmable. If FPS = 0, the FLT pin goes low when a write fault is detected. If FPS = 1, the FLT output goes high when a write fault is detected.

A fault is asserted on the FLT pin under one of the following unsafe conditions:

- An open head. Does not respond to frequency above 10 MHz to avoid false alarm
- Write data too slow
- An open reference resistor
- Vcc or Vdd supply voltage fault

Servo Mode

A low on the FLT pin indicates the following unsafe condition:

- Chip temperature too high
- Vcc supply voltage fault

Idle/Sleep Mode

A low on the FLT pin indicates the following unsafe condition:

- Vcc supply voltage fault

THERMAL ASPERITY DETECTION AND COMPENSATION

The thermal asperity circuitry can be controlled by the combination of TAC and TAD bits in TADC Data Register. The two bits control four combinations of thermal asperity handling, i.e., TA off, TA detection only, on-the-fly TA correction mode and retry TA correction mode, as shown in Table 2 and Figure 1. When the TA detector is active (TAD = 1), the FLT pin flags low when the chip detects the output exceeds the TA threshold setting.

TABLE 2: Thermal Asperity Modes

TAD	TAC	THERMAL ASPERITY MODE
0	0	Off
1	0	TA detection only
0	1	Retry mode (low corner frequency shift)
1	1	On the fly mode (low corner frequency shift when TA detected)

In on-the-fly TA correction mode, the signal pass band lower corner frequency is shifted up to 5 MHz when the TA threshold is exceeded. The TA correction stays on for 2 µs after the TA event ends (signal drops below TA threshold) and returns to normal operating mode by itself.

The TA detection threshold is set by bits TB0:TB5 of the TA/BHV Data Register. This DAC is shared by the DBHV comparator; the active mode is determined by the state of the TAD and MRM Register bits. The threshold level for the thermal asperity detector is programmable through the serial port according to the following:

$$Vta\ (mV) = 200 + 30 \bullet N \quad \text{(nominal)}$$

where RREF = 2.0 kΩ and N = 0,1...63 is the decimal value of Serial Port Register bits TB0:TB5. Threshold level is referred to the peak of the RDX output prior to the TA disturbance.

During retry TA correction mode, the pass band lower corner frequency is shifted up to 5 MHz and remains there until the retry TA correction mode is disabled.

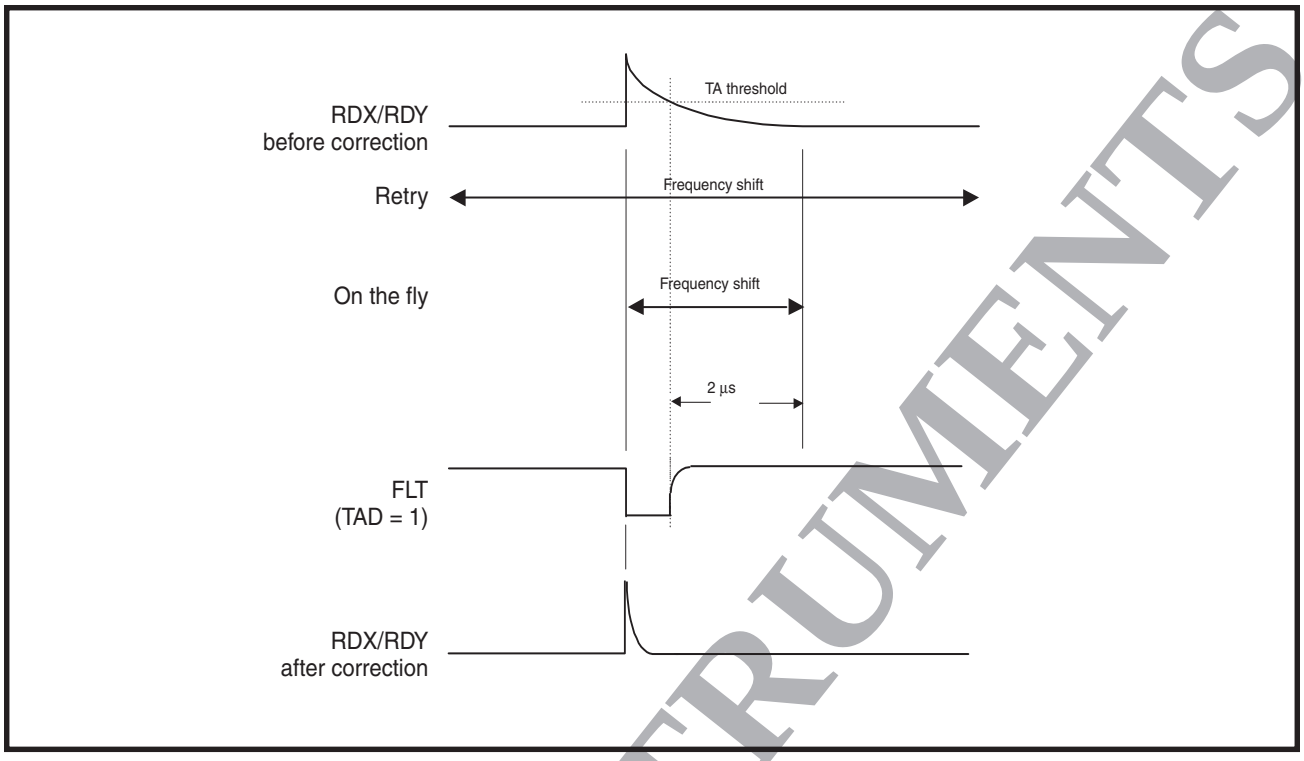


FIGURE 1: Thermal Asperity Modes

MR RESISTANCE MEASUREMENT MODE

MR resistance measurement can be activated in read mode by setting MRM bit (D3) in the Mode Register. With MRM = 1, the BHV pin outputs the analog head voltage with gain of 5 V/V and the FLT/DBHV pin becomes the digital head voltage monitor output. The ABHV output utilizes an internal clamp circuit which maintains the output below 2.8 V at any head DC voltage. The DBHV threshold is programmed by TA/BHV Data Register. When the MR head voltage is lower than the set internal threshold voltage, the FLT pin flags a high. When the MR head voltage is higher than the set DBHV threshold, FLT flags low.

The threshold voltage for the DBHV is programmable through the TA/BHV Serial Port Register according to the following:

$$Vdbhv\ (mV) = 160 + 24 \bullet N\ (nominal)$$

Where N = 0,1... 63 is the decimal value of Serial Port Registers TB0:TB5.

Note that the full DBHV threshold range overlaps the MR open head threshold. Since the MR open/short detectors are not disabled during MR measurement mode, the user should restrict the DBHV threshold setting to voltages below the MR open threshold (500 mV max recommended setting, N = 14).

VOLTAGE FAULT MONITOR

During power up or power fault condition, the voltage monitor disables the chip from any active mode. VCC fault monitor is active at any mode. The VDD fault monitor is active only in write mode to prevent false flag during servo bank write. The serial port has it's own power on reset circuit and serial data is cleared at VCC =1.6 V nominal.

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold and mode. The serial port bit map is shown in Table 3.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/$\overline{W}$ bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0 = 1, S1 = 0, and S2 = 0 for R/$\overline{W}$ amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits (see Serial Port Bit Map).

Asserting the serial port enable line SDEN (TTL) initiates a transfer, SDATA (TTL) is clocked into the Internal Shift Register by the rising edge of SCLK (TTL). A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being deasserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

TABLE 3: Serial Port Bit Map

REG	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	1	0	REV	REV	REV	CID	CID	0
HS/IMR	100	1000	HS0	HS1	HS2	IR0	IR1	IR2	IR3	IR4
Write	100	0100	IW0	IW1	IW2	IW3	IW4	WCB0	WCB1	WCB2
TADC	100	1100	TAC	DR0	DR1	TAD	HB0	HB1	HB2	HB3
TA/BHV	100	0010	TB0	TB1	TB2	TB3	TB4	TB5	FPS	Res
Mode	100	1010	$\overline{SLP}$	$\overline{IDL}$	GAIN	MRM	RB	SBW	SSD	Res

ID Register is read only
All data bits are set to 0 at power-up, except ID Register
X = Not used
Res = Reserved for TI internal use. User setting = 0

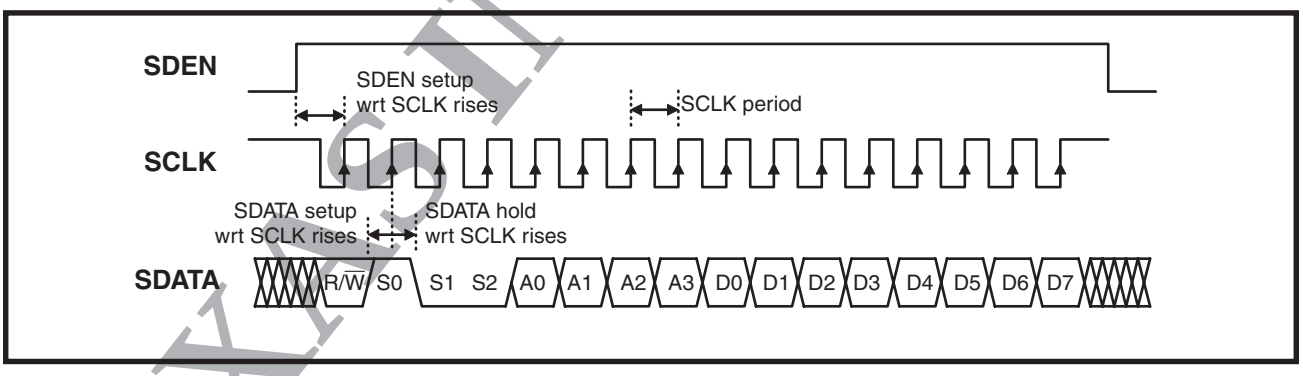


FIGURE 2: Serial Port Timing

REGISTER DESCRIPTION

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port read/write bit is not shown.

ID REGISTER (READ ONLY REGISTER) **ADDRESS = 0000 001**

BIT	NAME	DESCRIPTION
7		Not used
6:5	CID	CHANNEL ID: 01 is given for 8 channel version
4:2	REV	CHIP REVISION: 001 for the SSI 32R1610AR
1:0	VID	VENDER ID: 01 is given for the SSI 32R1610AR-8

HS/IMR REGISTER **ADDRESS = 0001 001**

7:3	IR4:IR0	MR bias current setting, see Read Mode section for bias equation 11111 = Maximum MR bias current (8 mA) 00000 = Minimum MR bias current (2 mA)
2:0	HS2:HS0	Head select bits, see Table 4 for head select bit maps

WRITE REGISTER **ADDRESS = 0010 001**

7:5	WCB2:WCB0	Write current boost 111 = Maximum write current boost 001 = Minimum write current boost 000 = No write current boost
4:0	IW4:IW0	Write current magnitude, see Write Mode section for equation 11111 = Maximum write current (55 mA) 00000 = Minimum write current (15 mA)

TA REGISTER **ADDRESS = 0011 001**

BIT	NAME	DESCRIPTION
7:4	IBR	MR head bias voltage in write/servo mode. LSB = 30 mV 1111 = Maximum head bias voltage (450 mV) 0000 = Minimum head bias voltage (off)
3	TAD	Thermal asperity detector control 1 = Enable TA detector 0 = Disable TA detector
2:1	DR1:DR0	Write damping resistor setting 00 = 1 kΩ 01 = 450 Ω 10 = 250 Ω 11 = 150 Ω
0	TAC	Thermal asperity correction enable when high Correction on the fly 1 = TAC 1 = TAD Correction retry mode 1 = TAC 0 = TAD

TADET/DBHV REGISTER **ADDRESS = 0100 001**

7	Res	Reserved for TI internal use. User setting = 0
6	FPS	Write fault polarity 1 = Write fault indicated by FLT = high (No write faults: FLT = low) 0 = Write fault indicated by FLT = low (No write faults: FLT = high)
5:0	TB5:TB0	TA detection threshold (TAD = 1, MRM = 0) or digital buffered head voltage comparator threshold (TAD = 0, MRM = 1) 111111 = Maximum threshold (TA = 2090 mV, DBHV = 1672 mV) 000000 = Minimum threshold (TA = 200 mV, DBHV = 160 mV)

REGISTER DESCRIPTION(continued)

MODE REGISTER **ADDRESS = 0101 001**

BIT	NAME	DESCRIPTION
7	Res	Reserved for TI internal use. User setting = 0
6	SSD	Servo mode open head shut down disable. When set high, open head self shut down circuit in servo write mode is disabled. This circuit is inoperative in the SSI 32R1610AR-8, user must set SSD = 1 to activate servo bank write mode.
5	SBW	Servo bank write mode enabled when high in write mode
4	RB	Read frequency boost enabled when high
3	MRM	MR measurement mode for analog BHV and digital BHV 1 = Enables MR measurement mode (TAD = 0) 0 = Disables MR measurement mode
2	GAIN	Read amplifier gain select 1 = High gain mode 0 = Low gain mode
1	$\overline{IDL}$	Idle control bit 0 = Idle mode enabled
0	$\overline{SLP}$	Sleep control bit 0 = Sleep mode enabled. Overrides all other control modes

TABLE 4: Head Selection, 8 Channel Version

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	0	none
0	0	1	1	1,3,5,7
0	1	0	2	0,2,4,6
0	1	1	3	all
1	0	0	4	none
1	0	1	5	none
1	1	0	6	none
1	1	1	7	none

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RREF	I/O	External resistor connection to set reference current for current DACs
$\overline{\text{MRBIAS}}$	I	MR BIAS CURRENT ON: TTL, internal pull-down. Bias current active at low
WnX, WnY	O	Inductive write head connection
RnX	I/O	MR read head connection, positive end
HGND	I	MR head connection, negative end
FLT/DBHV	O	FAULT: An open collector output Fault mode: Read mode: A low indicates abnormal read condition Write mode: A high (FPS = 1) or low (FPS = 0) indicates abnormal write condition MR measure mode: DBHV comparator output A low indicates the head voltage is higher than the set threshold A high indicates the head voltage is lower than the set threshold Servo write mode: A low indicates abnormal die temperature
POK	I	POWER OK: A low disables write function. TTL with internal pull-up
BHV	O	Analog buffered head voltage monitor output with gain of 5
R/$\overline{\text{W}}$	I	READ/WRITE: TTL, with internal pull-up
RDX,RDY	O	Differential read data output
GND	I	Ground
VCC	-	+5 V power supply
VDD	-	+8 V power supply for write driver
SDEN	I	SERIAL PORT ENABLE: TTL, internal pull-down
SDATA	I/O	SERIAL DATA: TTL, internal pull-up
SCLK	I	SERIAL CLOCK: TTL, internal pull-down
WDX/WDY	I	Write data input, PECL

ELECTRICAL SPECIFICATION

Unless otherwise specified, Rmr = 50 Ω, Imr = 5.10 mA (setting value), RREF = 2.00 kΩ, Lwh = 130 nH, Rwh = 10 Ω, Iw = 40.8 mA (setting value)

ABSOLUTE MAXIMUM RATINGS

Operation beyond maximum ratings may result in permanent damage to the device

PARAMETER		RATING
DC Supply Voltage	VCC	-0.3 to 6 VDC
DC Supply Voltage	VDD	-0.3 to 9 VDC
Logic Input Voltage	TTL	-0.3 to VCC + 0.3 VDC
	PECL	0 to VCC
Write Current	Iw	120 mA
MR Bias Current	I_{MR}	20 mA
Write Head Voltage	V_{WH}	-0.3 V to VDD + 0.3 V
Read Head Voltage	V_{MR}	0 to 1.2 V
Output Current	RDX,Y	-10 mA
	FLT/DBHV	+8 mA
Storage Temperature	Tstg	-65 to 150 °C
Operating Junction Temperature	Tj	+135 °C

RECOMMENDED OPERATION CONDITIONS

DC Supply Voltage	VCC	4.5 to 5.5 VDC
DC Supply Voltage	VDD_Write	7.2 to 8.8 VDC
	VDD_Servo	5.0 to 8.8 VDC
Write Head Load Range	L_H	60 to 250 nH
Write Head Resistor Range	R_{WH}	5 to 25 Ω
MR Head Range	R_{MR}	35 to 80 Ω
Operating Ambient Temperature	Ta	0 to 70 °C

POWER SUPPLY

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VDD Supply Current	I_{DD-R}	Read		0	0.2	mA
	I_{DD-W}	Write, Iw = 40 mA		56	72	mA
	I_{DD-S2}	Servo 2 channel, Iw = 30 mA		75	98	mA
	I_{DD-S4}	Servo 4 channel, Iw = 30 mA		150	196	mA
	I_{DD-S8}	Servo 8 channel, Iw = 30 mA		300	392	mA
	I_{DD-IL}	Idle		0	0.2	mA
	I_{DD-SP}	Sleep		0	0.2	mA
VCC Supply Current	I_{cc-R0}	Read IMR off		12	18	mA
	I_{cc-R1}	Read IMR on, Imr = 8 mA		41	60	mA
	I_{cc-W0}	Write, Iw = 40 mA		25	33	mA
	I_{cc-S2}	Servo 2 channel, Iw = 30 mA		31	40	mA
	I_{cc-S4}	Servo 4 channel, Iw = 30 mA		47	62	mA
	I_{cc-S8}	Servo 8 channel, Iw = 30 mA		78	100	mA
	I_{cc-IL}	Idle		9	15	mA
	I_{cc-SP}	Sleep		4	7	mA
VCC Fault Voltage		Write mode Iw < 0.2 mA		3.75	4.2	V
VDD Fault Voltage		Write mode Iw < 0.2 mA		VCC - 0.7	VCC	V
VCC Fault Voltage		Clears serial data		1.6		V

NOTE: Supply current equation, in mA, N = number of active channels at servo write mode
IDD_W = 16 + Iw
IDD_servo = (7.5 + Iw) • N
ICC_W0 = 15.2 + 0.15 • Iw + 0.21 • Imr
ICC_R1 = 25 + 1.21 • Imr + 0.15 • Iw
ICC_servo = 12 + 6 • N + (2 + N)/20 • Iw + 0.21 • Imr

ELECTRICAL SPECIFICATION(continued)

DIGITAL INPUT/OUTPUT

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R/$\overline{W}$, $\overline{MRBIAS}$, POK, SDATA SDEN, SCLK						
Input High Voltage	V_{IH1}	TTL	2.2		Vcc + 0.3	VDC
Input Low Voltage	V_{IL1}	TTL	-0.3		0.8	VDC
Input High Current	I_{IH1}	V_{IH1} = 2.2 V			160	µA
Input Low Current	I_{IL1}	V_{IL1} = 0.8 V	-400			µA
WDX, WDY						
Input High Voltage	V_{IH3}	PECL	1.9		Vcc - 0.9	VDC
Input Low Voltage	V_{IL3}	PECL	1.0		V_{IH3} - 0.3	VDC
Input Δ Voltage			0.3	0.8	2.0	VDC
Input High Current	I_{IH3}	V_{IH3} = 4.0 V		4	5.5	µA
Input Low Current	I_{IL3}	V_{IL3} = 3.2 V	-5.5	-4		µA
WD Termination	R_{WDin}		150	200	250	Ω
FLT (open collector)						
Output High Current	I_{OH}	V_{OH} = VCC			20	µA
Output Low Voltage	V_{OL}	I_{OL} = 2 mA			0.5	V
SDATA (readback)						
Output High Voltage	V_{OH2}	3 V CMOS	2.4		3.0	V
Output Low Voltage	V_{OL2}				0.8	V

SERIAL PORT TIMING

Read/Write						
SCLK Clock Period	T_C	Write operation	25			ns
		Read operation	40			ns
SCLK Low Time	T_{CKL}		5			ns
SCLK High Time	T_{CKH}		5			ns
Enable to SCLK	T_{SENS}		10			ns
SCLK to Disable	T_{SENH}		10			ns
Data Set-up Time	T_{DS}		5			ns
Data Hold Time	T_{DH}		5			ns
SDEN Min Low Time	T_{SL}		25			ns
SCLK Fall to Data Valid	T_{SDV}	Read operation			17	ns
SDATA Hold Time	T_{SDH}	Read operation	20			ns
SDEN Fall to SDATA Tristate	T_{SDTRI}	Read operation			20	ns

CURRENT DAC REFERENCE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Voltage Reference	Vref		1.9	2.0	2.1	V
Reference R Range	Rref			2.0		kΩ
Reference Current	Iref	Rref = 2 kΩ		1		mA

WRITE/SERVO CHARACTERISTICS

Write Current Nominal Range	Single head write	15		55	mA
Maximum Write Current, Servo Mode	4-heads, Vdd = 5 VDC	42			mA
	8-heads, 5 V < Vdd < 6 V	26	34		mA
	8-heads, 6 V < Vdd < 7 V	34			mA
	8-heads, 7 V < Vdd < 8.8 V	40			mA
Write Current Resolution			5		bit
LSB			1.29		mA
Write Current Accuracy		-8		+8	%
Head Voltage Swing	Open head, Vdd = 8 VDC		6.5		Vp-p
	Transient, Vdd = 8 VDC		7.5		Vp-p
	Open head, Vdd = 5 VDC		3.5		Vp-p
	Transient, Vdd = 5 VDC		4.0	1	Vp-p
Damping Resistor	<DR0,DR1> = <0,0>		1		kΩ
	<DR0,DR1> = <1,0>		450		Ω
	<DR0,DR1> = <0,1>		250		Ω
	<DR0,DR1> = <1,1>		150		Ω
Unselected Head Current	DC			100	µA
	Transient			1	mApk
Write Current Matching	Servo mode, channel to channel variation from mean			10	%

MR BIAS VOLTAGE IN WRITE/SERVO

MR Head Voltage Bias Range		0		0.45	V
Resolution			4		bit
LSB	Rmr = 50 Ω		30		mV
Absolute Tolerance	Rmr = 50 Ω	-25		25	%

ELECTRICAL SPECIFICATION (continued)

READ CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		35	50	80	Ω
MR Bias Current Nominal Range		2		8	mA
MR Bias Current Resolution			5		bit
LSB			194		µA
MR Current Tolerance		-8		+8	%
MR Head DC Voltage Range		0.1		0.75	V
Unselected Head Current				10	µA
Input Resistance (RIN)			5		Ω
Differential Voltage Gain	R_{MR} = 50 Ω, low gain		165		V/V
	R_{MR} = 50 Ω, high gain		240		V/V
Read Gain Constant	Av • (RMR + RIN), low gain		9100		Ω
	Av • (RMR + RIN), high gain		13000		Ω
Bandwidth	Lower -3 dB		0.65	1	MHz
	Higher -1 dB	125	174		MHz
	Higher -3 dB, RB = 0	180	230		MHz
	Higher -3 dB, RB = 1	185	236	287	MHz
Input Noise (Excludes RMR,	R_{MR} = 35 Ω		0.75		nV/√Hz
Includes Current Noise)	R_{MR} = 50 Ω		1.00		nV/√Hz
Dynamic Range	Gain falls to 90%	2			mV
Output Offset Voltage		-100		100	mV
Output Current		2.5			mA
Output Voltage		1.0		3.0	V
Output Resistance	Single-ended		50		Ω
PSRR	@ 5 MHz	45	60		dB
	@ 20 MHz		45		dB
Channel Separation	@ 5 MHz	45	60		dB
	@ 20 MHz		45		dB

HEAD VOLTAGE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DBHV Threshold Resolution			6		bit
DBHV Minimum Threshold		140	160	173	mV
LSB		22.08	24	25.92	mV
DBHV Threshold Accuracy	DAC setting = 0 to 14, after offset compensation	-8		+8	%
BHV Gain		4.7	5	5.3	V/V
BHV Output Range		0.4		3.0	V
BHV Output Current	Output drops to 90%	0.5			mA
BHV Output Offset		-100		100	mV
BHV Output Clamp Voltage	Vin = 0.48 - 0.75 V		2.4	2.8	V
MR Head Short Detect Threshold			40	60	mV
MR Head Open Detect Threshold		600	660		mV

THERMAL ASPERITY DETECTION/CORRECTION/FAST RECOVERY

TA Detection Resolution			6		bit
TA Detection Minimum Threshold	Relative to RDX output peak prior to correction	150	200	250	mV
TA Detection Threshold, Nominal Range	Relative to RDX output peak prior to correction	200		2190	mV
LSB	Ref = 2 kΩ	22.5	30	37.5	mV
Lower Corner Frequency	TAC = 1		5		MHz
TA Detection Delay	TAD = 1		30	100	ns
TA Correction Delay	TAC:TAD = 11		0.4	1.0	µs
TA Correction Timer	TAC:TAD = 11		2		µs

SWITCHING CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write to Read Switching	90% signal envelope, ±30 mVDC		0.4	TBD	µs
Read to Write Switching	90% of Iw, single write		25	50	ns
	90% of Iw, servo write			70	ns
Read, MR Bias Off to On	90% signal envelope, ±30 mVDC		0.6	TBD	µs
Idle to Read Switching	90% signal envelope, ±30 mVDC		1	TBD	µs
Read to Idle Switching	10% of read envelope			0.6	µs
Head Switching	90% signal envelope, ±30 mVDC		1	10	µs
Iw Rise/Fall Time 10% to 90%	Lh = 130 nH, Iw = 40 mA, Vdd = 8 V		1.3	TBD	ns
	Lh = 130 nH, Iw = 30 mA, Vdd = 5 V		2.0		ns
Head Current Delay TD3	50% of WD to 50% of Iw			30	ns
Write Current Asymmetry	Propagation delay difference 50% duty cycle write data			0.5	ns

WRITE UNSAFE DETECTION

FLT Safe to Unsafe TD1		0.5	1	2	µs
FLT Unsafe to Safe TD2				200	ns
Write Data Frequency	Valid transient detector			160	MHz
	Valid open detector			10	MHz

OVER TEMPERATURE DETECTION

Over Temperature Detection Threshold	Servo mode, FLT = low		135		°C

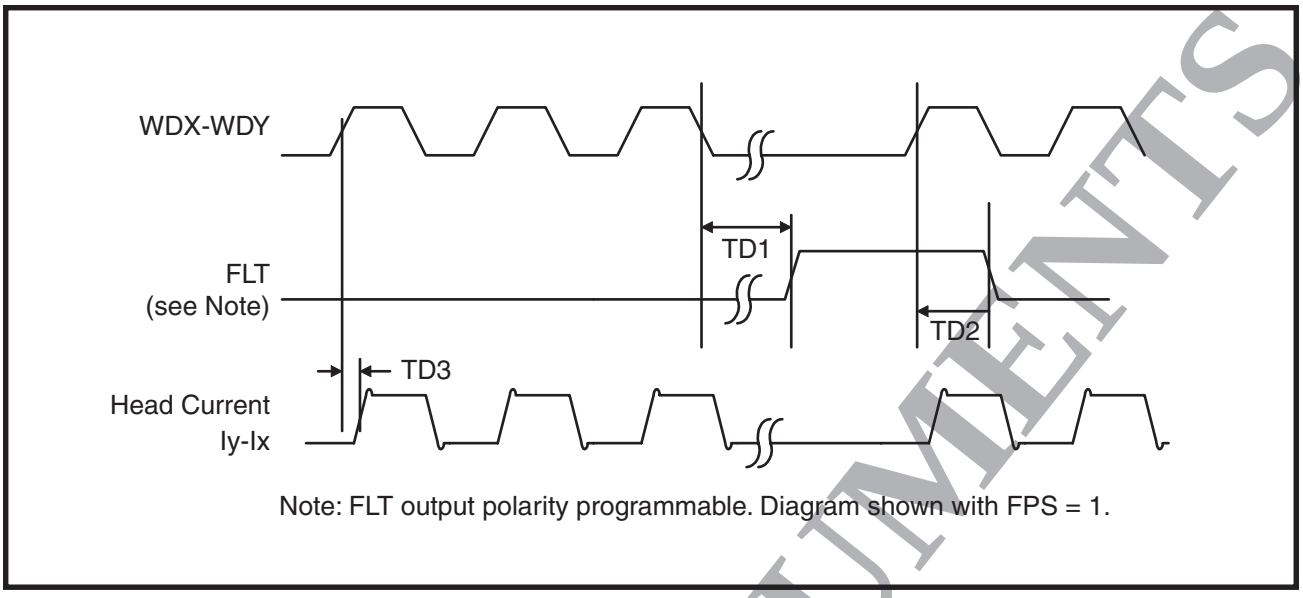
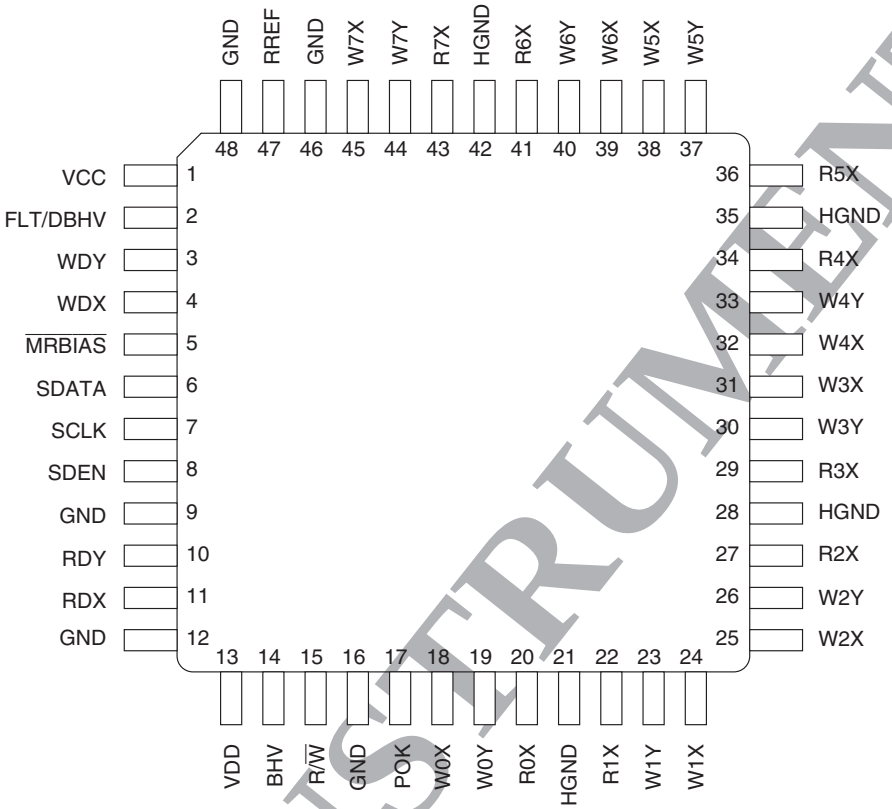


FIGURE 3: Write Current and Head Unsafe Timing

SSI 32R1610AR
+5 V, +8 V, 8-Channel MR/GMR Read/Write Device

PACKAGE PIN DESIGNATIONS

(Top View)



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32R1610AR 48-Lead TQFP	32R1610AR-8GT	32R1610AR8

Preproduction: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

32R1611D
+5, +8V, 4,6-CHANNEL MR READ/WRITE DEVICE

June, 2000

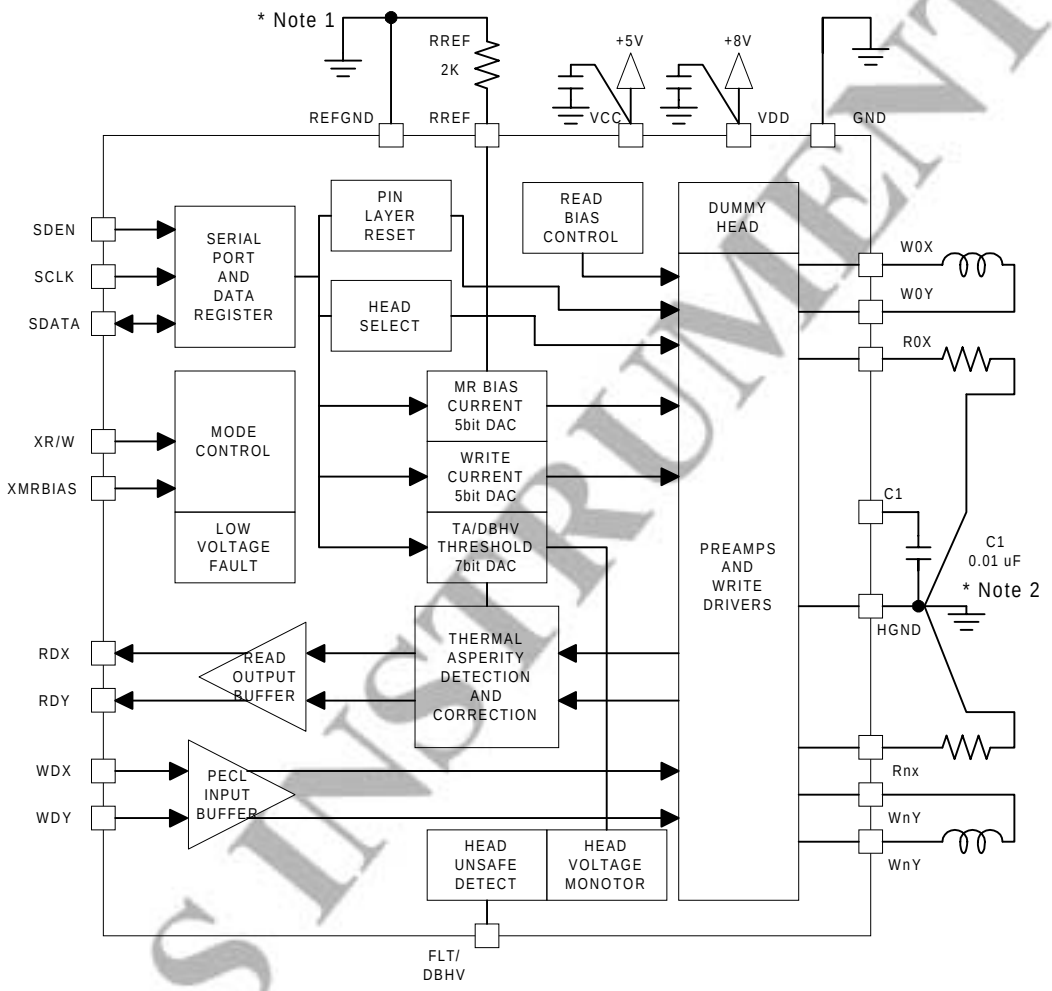
DESCRIPTION

The TI 32R1611D is a BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive read and thin film write composite recording heads. It provides a low noise 5 volt MR head amplifier, MR bias current control, thermal asperity detection and correction, GMR pin layer reset function, an 8 volt thin film write driver, write current control, and TFH fault detection circuit for up to six channels. The device features programmable read gain, write damping resistance and thermal asperity threshold level. The device allows multiple channel write functions for servo writing in the bankwrite mode. Control of features and thresholds is provided through a serial port interface. The 32R1611D requires a +5V and a +8V supply, and comes in a 30 TSSOP (4-channel), or a 38 TSSOP (6-channel) package. Part marking is P32R1611Dx, where x is the channel count.

FEATURES

- **One side grounded input, fully differential output**
- **Unselected Read/Write heads at GND potential**
- **Thermal asperity detection and compensation**
- **MR resistor measurement mode**
- **MR bias current range = 2 to 9.75mA (5bit)**
- **MR resistor range =25 to 75 Ω**
- **Programmable read gain =225 V/V or 300 V/V @45Ω, IMR=6 mA**
- **Input equivalent noise 1.1 nV/√Hz @45Ω**
- **Read Frequency boost**
- **Write current range = 15 to 60 mA (5bit)**
- **Active write damping**
- **Programmable write current boost control (2 bit)**
- **Programmable write current undershoot control (1 bit)**
- **Impedance matched differential write data input, no flip-flop**
- **Bank write mode**
- **Power fault protection**
- **3.3 V CMOS compatible logic interface**
- **Fast write current rise/fall times = 0.9 ns (Ltf = 90 nH, Rtf = 18 Ω, Iw = 40 mA)**
- **GMR pinned layer reset voltage pulse capability**
- **Internal reference resistor (4-ch version only)**

BLOCK DIAGRAM



Notes:

1. External Reference resistor required for 6-channel device only. Resistor integrated on 4- channel version.
2. Recommended values for C1 cap include 0.01 uF and 0.022 uF. C1 value affects the reader low frequency response and switching times.

FUNCTIONAL DESCRIPTION

The 32R1611D addresses up to 6 four terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with 3.3V logic pins XR/W, XMRBIAS and the serial port as shown in Table 1. The XR/W input has an internal pull-down resistor so that when left opened, it will default to the logic low state, while the XMRBIAS input has an internal pull-up resistor.

The serial port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold level and mode.

Device power-on resets the serial port bits to their default values, which places the device into sleep mode. To place preamp into an active mode (read or write mode) from sleep mode, the device should be placed in idle mode and then read mode to activate an internal quick recovery circuit.

SLEEP MODE

The chip is set to sleep mode by setting XSLP bit of the Mode register low. Only the serial port and voltage fault monitor is active in this mode. The XSLP bit overrides all other mode control setting bits and pins. Upon power-up, the device will reset the serial port to its default values, which places the device into sleep mode. The only fault detected in idle mode is low VCC. If the VCC voltage drops below 3.75 V, the FLT output will go low. When the power supply voltage returns to above 3.9 V, the fault will clear.

IDLE MODE

The XIDL bit in Mode register of the serial port controls idle mode. Internal reference voltage and DACs are activated when XIDL bit is set to low in non-sleep mode. During idle mode, the internal write current generator, and read output buffer are deactivated. The reference circuit is on, but MR bias current does not flow through either the selected head or the internal dummy head. All the connections to the external C1 capacitor are opened to preserve charge on the capacitor. If entering Idle mode from Sleep mode, the C1 cap will have no charge when exiting Idle mode. If entering Idle mode from an active mode (read or write mode) with XMRBIAS = 0, the C1 cap will attempt to preserve the charge during Idle mode, subject to capacitor leakage.

The only fault detected in idle mode is low VCC. If the VCC voltage drops below 3.75 V, the FLT output will go low. When the power supply voltage returns to above 3.9 V, the fault will clear.

TABLE 1: Mode Selection.

XSLP	XIDL	XR/W	XMRBIAS	SBW0/SBW1	Mode
0	X	X	X	X	Sleep
1	0	X	X	X	Idle
1	1	0	0	X	Read, IMR on (selected head)
1	1	0	1	X	Read, IMR off
1	1	1	0	0/0	Write, IMR on (selected head)
1	1	1	1	0/0	Write, IMR off
1	1	1	1	1/1	Servo Write, IMR off
1	1	1	0	1/1	Servo Write, IMR on

Notes.
- XSLP, XIDL, SBW0/SBW1 are serial port bits (Mode register)
- See Servo mode section for Bankwrite activation procedure

READ MODE

Taking the XR/W pin low in non-idle mode selects read mode, which activates the MR bias current generator and low noise differential amplifier. XMRBIAS pin must be low to activate the MR bias current through the designated head. When XMRBIAS is high, MR current to the selected head is disabled and the C1 node will be set to high impedance, similar to Idle mode. MR bias current is diverted to the internal dummy load when the head selection bits are set to a value outside the allowed range and, on the 4-channel version only, a fault is reported by placing the FLT output low.

The outputs of the read amplifier RDX/RDY are emitter followers and are in phase with the resistivity change at the selected input port (RnX/HGND) where the respective MR head is attached. The read mode gain is set to one of two values based on the GAIN bit of the Mode serial port register.

The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port. The magnitude of the bias current is set according to the following equation:

$$Imr\ (mA) = 2.0 + 0.250 \bullet N$$

where RREF = 2.0KΩ (when applicable) and N = 0,1,...31 is the decimal value of serial port register bits IR0:IR4.

In write mode, when XMRBIAS pin is low, MR bias current remains on the selected MR head. When XMRBIAS pin is high in write mode, MR bias current to the selected head is turned off and the external C1 capacitor preserves its charge by making all its connections high impedance.

During switching from head to head, the chip selects an internal dummy head (20 ohm nominal) to discharge C1 capacitor so that the selected MR will see no current overshoot during the transition. It is recommended that all head switches occur only in Read mode to prevent bias current overshoot conditions. In addition, if the MR bias current needs to be changed in conjunction with a head switch, it is recommended that change be performed in two steps to prevent bias overshoot conditions on the new head. When the head switch includes a decrease in bias current, first reduce the bias current on the present head, wait a minimum of 15 usec, and then switch heads. When the head change includes an increase in bias current, the head should be switched before increasing the bias current setting. Alternatively, when increasing the bias current, the head switch and bias current change can be performed at the same time with a simultaneous serial port command.

Note that the C1 capacitor can be placed in a high impedance state with one of two methods: placing XMRBIAS pin high, or placing the preamp into idle mode. The high-impedance state of C1 allows very fast recovery to active read mode provided the C1 cap has maintained the charge developed at the time the device last exited read mode. During the high impedance mode, C1 will gradually lose its charge due to leakage. If C1 discharges enough, a momentary MR fault will be reported when switching back into read mode due to the low initial head voltage. This momentary fault also occurs the first time read mode is entered after sleep mode or initial power-up, conditions where the C1 capacitor is discharged. The user should clear the fault reporting register after entering read mode from a sleep condition, or if the device has had C1 in high impedance mode for a long period (>10 msec). The Idle-to-Read switching time assumes total discharge of the C1 capacitor and a C1 value of 0.010 uF.

THERMAL ASPERITY DETECTION AND COMPENSATION

The Thermal Asperity circuitry can be controlled by the combination of serial port bits TAC, TAD and the thermal asperity threshold setting, bits TA6:TA0. These bits control four combination of thermal asperity handling, i.e. Off, TA detection only, TA correction On the Fly mode, and TA correction Retry mode (see Table 2). Note that to enable TA detection, the TAD = 1, MRM = 0, and the threshold bits TA6:0 must be set for the appropriate threshold.

In TA Retry mode, the low corner frequency of the read amplifier is shifted up to 5 MHz to remove low frequency content of the TA event. TA Retry mode activates and maintains the low corner frequency shift as long as the mode is enabled.

In On the Fly mode, both TA compensation and the low frequency corner shift are activated when a thermal asperity is detected. With TA compensation, the chip detects the peak voltage of the thermal asperity and subtracts the peak from the read output. The amplifier returns to its normal operating state 2 μsec after the signal has returned below the TA threshold voltage. The TA detection threshold is

set by bits TA0:TA6 of the TA data register. The threshold value is same as the DBHV threshold voltage.

In On the Fly mode, FLT/BHV pin flags low when the chip detects a thermal asperity, and returns high once the uncompensated read signal returns below the threshold. In Retry mode, the FLT/BHV pin flags low until retry mode is deactivated.

The threshold level for the thermal asperity detector is programmable through the serial port according to the following:

$$Vta\ (mV) = 6 \bullet N \quad \text{(nominal)}$$

where RREF = 2.0 KΩ (when applicable) and N = 1,2...127 is the decimal value of serial port register bits TA0:TA6. The threshold level is referred to the peak of the RDX output prior to the TA disturbance.

TABLE 2: Thermal Asperity Modes

TAC	TAD (MRM=0)	Thermal Asperity Mode
0	0	Off (no detection or compensation)
0	1	TA Detection only Threshold set by TA6:0
1	0	Retry mode (low corner frequency shift)
1	1	On the Fly mode (TA comp plus corner frequency shift) Threshold set by TA6:0

Note: To enable TA detector, TAD = 1 and MRM = 0. TAD takes priority over MRM if both TAD = 1 and MRM = 1.

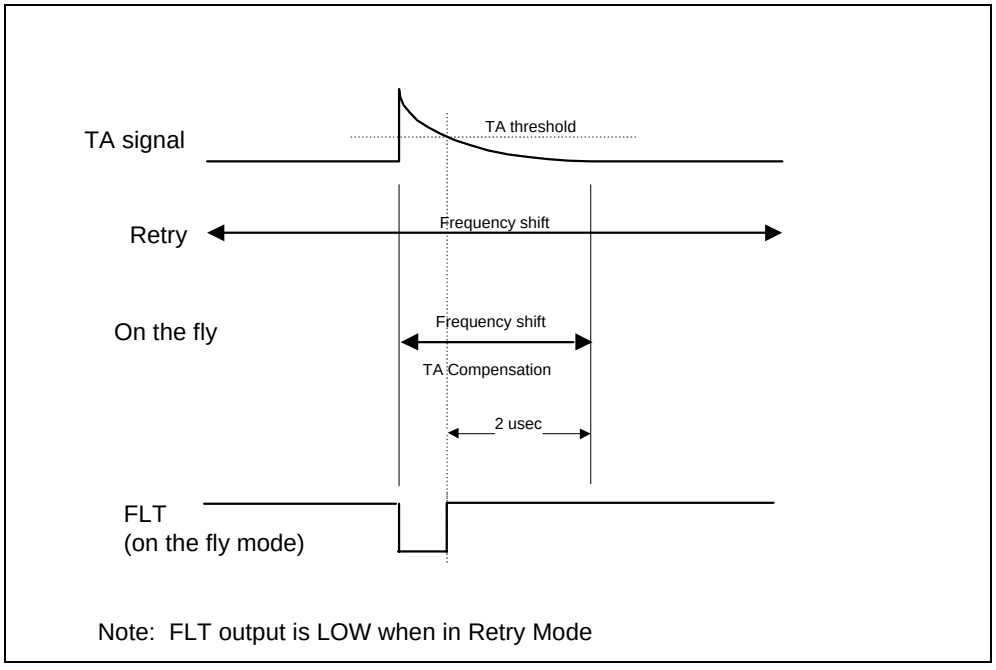


FIGURE 1: Thermal Asperity Modes

WRITE MODE

Taking XR/W high in non-idle mode selects write mode. Write current is enabled to the selected channel and write data (WDX/WDY) controls the write current polarity. Head current is toggled between the X and Y side of the selected head on each transition of the differential signal WDX-WDY, when WDX is higher than WDY, the current flows from X (WnX) to Y (WnY). The write data input buffer is active in all modes except sleep mode.

Write current magnitude is controlled by a five-bit on board DAC. The DAC is programmed via the serial port. The magnitude of the write current (0-pk) is generally given by:

6-Channel device (all write modes) and 4-Channel device (bank write mode):

Iw (mA) = 15 + 1.45 • N (0-pk), N = 0,1 ... 31

4-Channel device (single head mode):

Iw (mA) = 16.32 + 1.458 •N (0-pk), N = 0,1 …15

Iw (mA) = 19.29 + 1.330 •N (0-pk), N = 16,17 …31

where RREF = 2.0 KΩ (when applicable) and N = 0,1 ... 31 is the decimal value of serial port register bits IW0:IW4.

A tabulation of the write current is shown in Table 3.

Unselected write heads are pulled to ground potential (+/- 0.3 V).

The MR bias current on the selected head can be controlled in write mode by the state of the XMRBIAS pin. When XMRBIAS = 0, bias current will flow through the selected head. The magnitude of the MR bias current is set by the serial register bits IR0:IR4 (register HS/IMR). When XMRBIAS = 1, the MR bias current will be deactivated.

TABLE 3: Write Current , 6-Channel (32R1611D-6) And 4-Channel Device (32R1611D-4)

Iw DAC (decimal)	Iw (mA) 4-Ch, single-hd	Iw (mA) 6-Ch, all modes. 4-ch servo	Iw DAC (decimal)	Iw (mA) 4-Ch, single-hd	Iw (mA) 6-Ch, all modes. 4-ch servo
0	16.32	15.00	16	40.57	38.20
1	17.78	16.45	17	41.90	39.65
2	19.24	17.90	18	43.23	41.10
3	20.69	19.35	19	44.56	42.55
4	22.15	20.80	20	45.89	44.00
5	23.61	22.25	21	47.22	45.45
6	25.07	23.70	22	48.55	46.90
7	26.53	25.15	23	49.88	48.35
8	27.98	26.60	24	51.21	49.80
9	29.44	28.05	25	52.54	51.25
10	30.90	29.50	26	53.87	52.70
11	32.35	30.95	27	55.20	54.15
12	33.82	32.40	28	56.53	55.60
13	35.27	33.85	29	57.86	57.05
14	36.73	35.30	30	59.19	58.50
15	38.19	36.75	31	60.52	59.95

The 32R1611D writer features overshoot and undershoot control. There are 2 serial port bits that affect overshoot performance, OC1:OC0, and 1 bit that controls undershoot, UC. Table 4 describes the amount of overshoot change vs. write current and OC bit setting. UC = 0 is only valid when OCO = 1.

TABLE 4: WRITE CURRENT OVERSHOOT CONTROL. (IW SETTING BASED ON 6-CH DEVICE)

% overshoot vs. write current and overshoot control settings.

Write Current Iw (mA)	% Overshoot			
	OC = 00	OC = 01	OC = 10	OC = 11
15	65	355	285	375
20.8	60	240	205	255
26.6	55	177	160	180
33.85	53	117	110	122
39.65	50	91	82	91
46.9	42	62	58	63
54.15	31	40	35	42

Single head write. Lh = 90nH, Rh = 15 •.

BANK WRITE MODE

Servo bank write mode allows simultaneous writing to multiple heads to reduce servo write efforts. Heads activated in bank write mode can be selected by HS0, HS1, and HS2 bits, as shown in Table 9.

The steps to activate servo bank write mode are as follows:

1. Place device in read mode (XR/W pin low).
2. Set VDMSKH bit to 1 when operating with VDD < 8.0 Vdc.
3. Set SBW0 bit to 1.
4. Set SBW1 bit to 1.
5. Set SBW0 bit to 0.
6. Load head select bits for desired bank write configuration.
7. Load MR bias current DAC (IMR Register). See description below of bias setting.
8. Place device in write mode (XR/W pin high).

Once steps 1 through 6 above have been initiated, bank write current can be enabled/disabled by the state of the XR/W pin. The device exits bank write mode when SBW1 = 0.

The MR bias current will be disabled in bank write mode when XMRBIAS = 1. The MR bias current can be enabled in bank write mode by placing XMRBIAS = 0. When enabled, the MR bias current is divided among all selected read elements. The actual current delivered to each individual head depends on its resistance; the total current to all selected heads will equal the MR bias current set by the IMR DAC. Assuming the MR resistance of all heads are equivalent and all heads are connected, the MR bias current delivered to each selected head will be 1/6th, 1/4th, 1/3rd,or 1/2 of the programmed value of the IMR DAC, depending on the device channel count and whether all-head or half-head bank write mode is selected. Since the normal MR bias range is 2 – 9.75 mA, the MR bias range in servo bank write mode is one of the following:

32R1611D-6 (6-channel): 0.33 – 1.625 mA (6–head write) or 0.67 – 3.250 mA (3–head write).

32R1611D-4 (4-channel): 0.50 – 2.437 mA (4–head write) or 1.00 – 4.875 mA (2–head write).

The VDMSKH bit of serial register Write/SB1 allows the user to disable the Low VDD fault detection. This step is necessary when operating the device in bank write mode with VDD = +5 VDC to reduce power dissipation.

During an all head bank write condition, the write current should be limited to less than 35 mA 0-pk. In addition, it is recommended that the chip operate in a well-controlled ambient temperature when servo write is active to prevent excessive junction temperatures. The thermal resistance of the package varies by mount conditions. Setting the OTMSKL bit of the Mode register to 1 will enable the over - temperature monitor. With OTMSKL=1, when an over temperature condition is detected the IC will assert the FLT/BHV pin high, set the HOT bit of the Fault Status register to 1, and shut off the writer current.

FAULT OPERATION

The function of the FLT/BHV pin is multiplexed between the ABHV, DBHV and FLT output. In FLT and DBHV modes, the FLT pin is configured as an open collector output. When ABHV = 0 and MRM = 0, the pin is a fault status output. Certain faults are also flagged in the Fault Status register of the serial port. Writing 00h to the Fault Status register will clear all bits in this register. The Fault Status register may not power-up with all fault bits cleared. The user should clear the Fault Status register by writing 00h after power-up. Serial port bit FMSKH can be used to disable all fault reporting. Table 5 summarizes the fault operation in various modes.

TABLE 5: Fault Reporting Summary

Fault	Condition	See Note	FLT pin logic level				Fault Status
			Read	Write	Bank	Idle/ Sleep	Register Bit Set = 1
None	Safe		H	L	L	H	None
Low VCC	VCC < 3.75 V clears when VCC > 3.9 V	1	L	H	H	L	None
Low VDD	VDMSKH = 0 VDD < 6.1 V clears when VDD > 6.7 V	2	L	H	H	X	D1
Illegal Head Select	Out of range head selected (4 channel only)		L	H	X	X	None
Open MR Head	Vmr > 900 mV	3	L	X	X	X	D2
Shorted MR Head	Vmr < 50 mV	4	L	X	X	X	D3
Thermal Asperity Detect	TAD = 1, RDX > Vta (TA threshold)		L	X	X	X	None
Thermal Asperity Retry	TAD = 0 , TAC = 1		L	X	X	X	None
Low Write Frequency	> 1 usec between WDX/WDY transitions, Fwd < 400 MHz	5	X	H	X	X	D6
Write Head Open	Fwd < 13.5 MHz	6	X	H	X	X	D4
Write Head Short to ground	Fwd < 13.5 MHz	7	X	H	X	X	D4
High Die Temperature	OTMSKL = 1 Die Temp > 135°C	8	X	X	H	X	D0

FAULT REPORTING NOTES

GENERAL FAULTS:

1. Low VCC

If the VCC power supply drops below the Low VCC threshold (3.75 V, typ), a fault will be detected and reported at the FLT pin. The write current and MR bias (if active) will be disabled upon detecting a Low VCC fault. When the power supply returns to a normal level (3.9 V), the fault will be cleared: the FLT pin will return to its safe mode and the write current and MR bias reactivated if XMRBIAS = low.

2. Low VDD

If the VDMSKH bit is set to 0 and if the VDD power supply drops below the Low VDD threshold (6.1 V typ) a fault will be detected and reported at the FLT pin and the corresponding serial port fault status bit will be set. The IC will shut off the write current and MR bias (if active) upon detecting a Low VDD fault. When the VDD voltage returns to a normal level, or the VDMSKH bit is set to 1, the fault will be cleared: the FLT pin will return to safe mode and the MR bias reactivated if XMRBIAS = low.

READ MODE FAULT DETAILS:

3. **Open MR element**

When the voltage across the selected MR head exceeds the open head threshold (900mV typ) in read mode, a MR open fault is detected and reported by setting the FLT output low and the corresponding serial port fault status bit is set. To prevent damage to the head, the MR bias current is shutoff and the fault latched. The fault may be cleared by selecting a normal head or by switching to idle mode and back to read mode following removal of the open head. The FLT output returns high after the fault has been cleared. Note that MR Measurement mode does not disable the MR open fault detection.

4. MR Element Short To Ground

When the voltage across the selected MR head drops below the shorted head threshold (50 mV typ) in read mode, a MR short to ground fault is detected and reported by setting the FLT output low and the corresponding serial port fault status bit is set. The MR bias is not disabled upon detection of this fault, and the fault is not latched. The FLT pin returns high when the fault condition no longer exists. Note that MR Measurement mode does not disable the MR short to ground fault detection. When entering read mode on a normal head with the C1 capacitor fully discharged a MR short fault will be reported until the head voltage has exceeded the MR short threshold. This fault is short in duration, but typically long enough to set the MR short bit (D3) of the Fault Status register. The user should clear the fault register after entering read mode from a mode where the C1 capacitor is discharged. The C1 capacitor is considered discharged upon power up and during sleep mode.

WRITE MODE FAULT DETAILS:

Only the Low supply voltage fault disables the write current (non-latching fault). The Low supply fault can be either a Low VDD or Low VCC fault. Low VDD fault detection can be disabled through use of the serial register bit Low VDD Disable.

5. Write Frequency Too Low

The 32R1611D will report a fault condition if the write data frequency is too low. If no data transition is detected for 1.0 μs (nom), a fault will be reported by placing the FLT pin high and the bit D6 of the Fault Status register will be set. The fault will clear within 300 ns (nom) of the next detected write data transition.

6. Write Head Open

If the write head output develops an open circuit during write mode, a fault will be detected and reported by placing the FLT pin high and the corresponding serial port fault status bit will be set. The operation of the writer does not change when an open head is detected. The fault will be cleared when the open circuit condition is removed or if a non-faulted head is selected. The open head detector operates over a restricted range of write data frequency, and will detect an open head when the write data frequency is less than 13.5 MHz (nom). The detector is disabled above this frequency to eliminate any false detection.

7. Write Head Short to Ground

If the write head shorts to ground, a fault will be detected and reported by setting the FLT pin high. The write current and MR bias current are not disabled when a write head short is detected. The FLT pin will return low once the short condition is removed. The 32R1611D does not distinguish between open and shorted write heads, therefore the write head short to ground is reported to the serial port fault status register as an TF OPEN fault.

BANK WRITE MODE FAULT DETAILS

Over Temperature

When register bit OTMSKL=1, an over-temperature condition will be indicated by setting register bit HOT to 1, and the write current will be disabled. The over-temperature detection can be disabled by setting OTMSKL = 0.

MR RESISTANCE MEASUREMENT MODE

MR resistance measurement can be activated in read mode by setting MRM bit in the Mode register with ABHV = 0. In this mode, the FLT/BHV pin is configured to output a Digital Buffered Head Voltage (DBHV) indication.

With MRM = 1, TAD = 0 and ABHV = 0, the FLT/BHV pin becomes the digital head voltage monitor. The DBHV threshold is programmed by TA/BHV data register. When the MR head voltage is lower than the set internal threshold voltage, the FLT/BHV pin flags high. When the MR head voltage is higher than the set DBHV threshold, FLT/BHV flags low.

A recommended application of the MRM mode is to fix the MR bias current, adjust the DBHV threshold until the FLT/BHV pin changes state. The MR resistance is equal to the DBHV threshold setting (in mV) divided by the MR bias setting (in mA). It is recommended that the MR bias setting be fixed while the TA threshold is adjusted, rather than fixing the threshold and adjusting the MR bias, to prevent damage to the head from excessive bias current.

The MR open and short fault detectors are not disabled in MR Measurement mode. While it is not possible to set the DBHV threshold to a voltage that is equivalent to an open head, the threshold can be set such that it overlaps the MR short range. When the head voltage is below the MR short threshold or above the MR open head threshold, the FLT output will be low regardless of the DBHV threshold, resulting in an invalid MR measurement. In addition, the DBHV comparator can make large errors at low threshold settings. Proper DBHV comparator operation is guaranteed for thresholds above 204 mV. Therefore, MR Measurement mode should be performed with the DBHV threshold above this minimum guaranteed threshold ($\geq$ 204 mV). This is equivalent to setting the TA/BHV DAC $\geq$ 34 (decimal) for MRM mode. Note that the fault mask bit (FMSKH) disables all fault detection, including DBHV.

In Fault or DBHV mode, the FLT/BHV pin is configured as an open collector digital output.

ANALOG BHV MODE

Setting bit ABHV = 1, with MRM = 1, configures the FLT/BHV pin to output an analog voltage which is the buffered version of the MR head voltage. The gain of the ABHV amplifier is 5 V/V. ABHV mode is not operational in the 6-channel version of the 32R1611D. Any pull-up resistors should be disconnected from the FLT output during ABHV mode.

GMR RESET MODE

The 32R1611D includes a voltage pulse generation feature to provide a pinned layer reset function for GMR heads. When activated, the device will generate a positive voltage pulse (relative to HGND) of programmable magnitude, from 0.41 V to 1.48 V. The duration of the pulse can be selected between two settings, 48 ns or 95 ns. The pulse will decay to ground potential with a turn-off decay slew rate that can be set to one of four settings. The circuit uses a constant decay current so the resulting decay time is proportional to the voltage difference between the applied reset magnitude and ground potential. The decay slew rate is selectable as shown in Table 6. The Reset pulse is applied from zero bias voltage. See Figure 2 for reset pulse timing.

TABLE 6: GMR Reset Pulse Decay Slew Rate

PLRDT1	PLRDT0	Decay Slew Rate (C1=10 nF)	Decay Slew Rate (C1=22 nF)
0	0	11.9 V/µsec	6.8 V/µsec
0	1	9.3 V/µsec	5.3 V/µsec
1	0	6.6 V/µsec	3.6 V/µsec
1	1	3.5 V/µsec	1.9 V/µsec

The reset pulse circuit must be armed prior to triggering the reset pulse. The following procedure will properly arm the reset circuit:

1. Turn MR bias current off by setting XMRBIAS = 1.
2. Place device into Idle mode. Program the PLR magnitude using the write current register (IW4:IW0) and the desired MR bias current (IR4:IR0).
3. Place device in Read mode. Select valid read head. Set serial port bit FMSKH = 1 to mask faults, and select desired settings of serial port bits PLRPW0, PLRDT1 and PLRDT0.
4. Make PLREN =1. Device enters PLR ARM mode at the end of serial port transfer.

The reset pulse fires when the XMRBIAS pin is brought low after arming. The pulse trigger must be applied at least 50 µs after arming the reset circuit. Placing XMRBIAS = 1 will disarm the reset circuit. Consecutive reset pulsing requires arming the circuit before it can be re-triggered. In other words, the user must bring PLREN bit to 0, and then to 1, before the PLR pulse can be triggered again. After completion of PLR action, recovery to normal read mode is accomplished by setting PLREN = 0 and bringing the XMRBIAS pin low. Recovery to Read mode is equivalent to normal Idle to Read switching time.

The magnitude of the reset voltage pulse is controlled by the write current DAC (IW4:IW0). The minimum setting is 0.41V; the maximum setting is 1.48V. See Table 7 for reset magnitude.

Other serial port bits used by the GMR reset circuit includes:

- PLREN: enables the pin layer reset mode.
- PLRPW0: selects the reset pulse width, T2 (48 ns or 95 ns).
- PLRDT1, PLRDT0: select pulse decay rate, T1 (refer to Table 6).

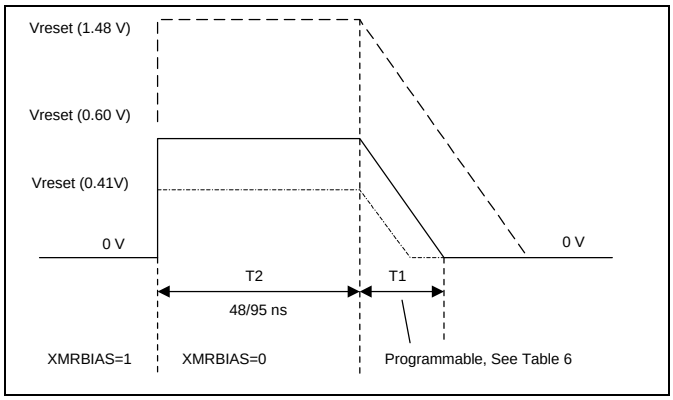


FIGURE 2: Typical GMR Reset Pulse Shape

TABLE 7: GMR Reset Pulse Amplitude (Set by IW DAC)

IW4	IW3	IW2	IW1	IW0	PLR Amp(V)
0	0	0	0	0	0.41
0	0	0	0	1	0.45
0	0	0	1	0	0.49
0	0	0	1	1	0.53
0	0	1	0	0	0.57
0	0	1	0	1	0.60
0	0	1	1	0	0.64
0	0	1	1	1	0.68
0	1	0	0	0	0.72
0	1	0	0	1	0.76
0	1	0	1	0	0.80
0	1	0	1	1	0.83
0	1	1	0	0	0.87
0	1	1	0	1	0.91
0	1	1	1	0	0.95
0	1	1	1	1	0.99

IW4	IW3	IW2	IW1	IW0	PLR Amp(V)
1	0	0	0	0	1.05
1	0	0	0	1	1.09
1	0	0	1	0	1.12
1	0	0	1	1	1.16
1	0	1	0	0	1.20
1	0	1	0	1	1.24
1	0	1	1	0	1.27
1	0	1	1	1	1.31
1	1	0	0	0	1.34
1	1	0	0	1	1.37
1	1	0	1	0	1.40
1	1	0	1	1	1.42
1	1	1	0	0	1.44
1	1	1	0	1	1.45
1	1	1	1	0	1.47
1	1	1	1	1	1.48

Note: DAC step size is not linear for upper DAC settings.

VOLTAGE FAULT MONITOR

During power up or power fault condition (approximately VCC < 1.1 VDC), the voltage monitor disables the chip from any active mode. The serial data is reset to sleep mode with the default setting value.

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold and mode. The serial port bit map is shown in Table 8A (6-ch version) and Table 8B (4/8-ch versions).

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/W bit, which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0, and S2=0 for

R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map).

Asserting the serial port enable line SDEN initiates a transfer, SDATA is clocked into the internal shift register by the rising edge of SCLK. A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. When writing to a register, loading of the register takes place on the

falling edge of SDEN. The SDATA bits are clocked on the rising edge of SCLK when writing to the preamp registers (see Figure 3).

On register readback, the address bits are clocked on the rising edge of SCLK, as in write mode. The data bits are clocked out of the register on the rising edge of SCLK in order for the readback device to clock in the data bits on the subsequent falling edge of SCLK (see Figure 4).

The three serial port lines are 3.3 volt logic compatible. See Digital Input/Output specifications for 3.3 V logic details.

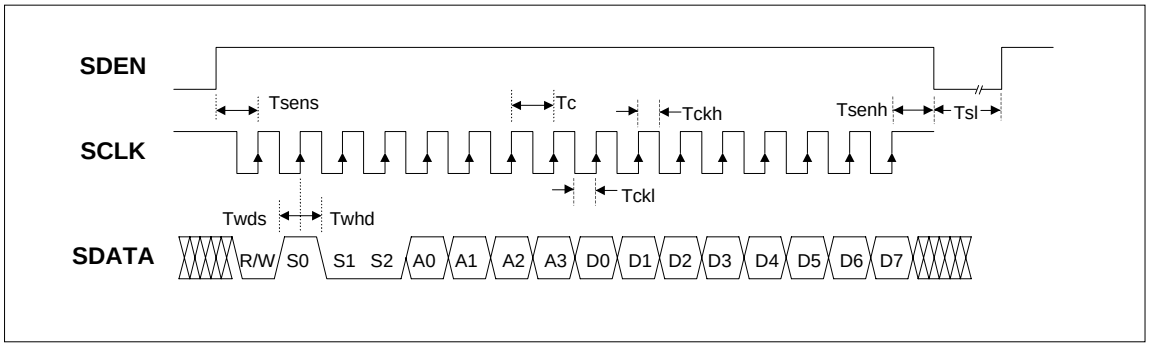


FIGURE 3: Serial Port Timing, Write Mode

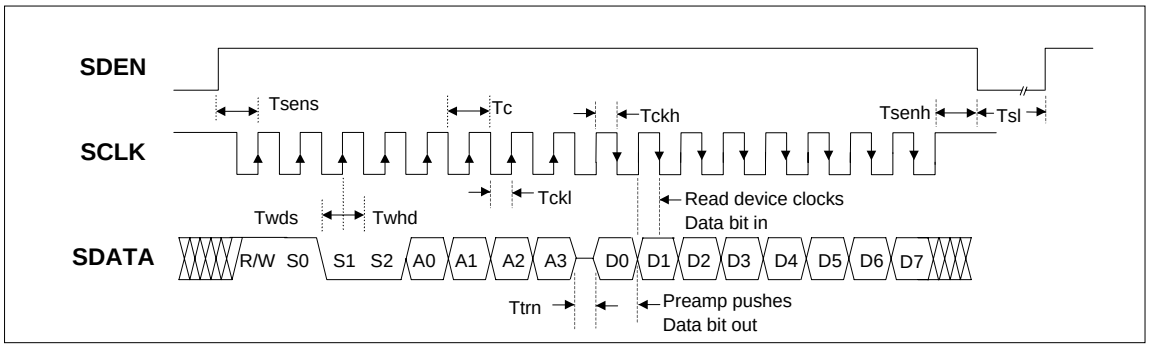


FIGURE 4: Serial Port Timing, Read Back Mode

TABLE 8A: Serial Port Bit Map, 6-Channel Device (32R1611D-6)

Reg	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	VEN0 =1	VEN1 =0	VEN2 =0	REV0 =0	REV1 =1	REV2 =1	REV3 =0	CH =0
HS/IMR	100	1000	HS0	HS1	HS2	IR0	IR1	IR2	IR3	IR4
Write	100	0100	IW0	IW1	IW2	IW3	IW4	TBLKL	VDMSKH	SBW1
TA/BHV	100	1100	TA0	TA1	TA2	TA3	TA4	TA5	TA6	TAC
Mode	100	0010	XSLP	XIDL	GAIN	MRM	RB	SBW0	Res	OTMSKL
Misc	100	1010	FMENL	GMENL	OC0	OC1	UC	BWR1	BWR2	FMSKH
Fault	100	0110	HOT	Low VDD	MR_O	MR_S	TF_O	TF_S	TF_F_L	X
PLR	100	1110	PLRDT1	PLRDT0	PLRPW1	PLRPW0	PLREN	WFMSKH	TAD	SGMENL

TABLE 8B: SERIAL PORT BIT MAP, 4-CHANNEL DEVICE (32R1611D-4)

Reg	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	VEN0 =1	VEN1 =0	VEN2 =0	REV0 =0	REV1 =0	REV2 =0	REV3 =0	CH =1/0
HS/IMR	100	1000	HS0	HS1	HS2	IR0	IR1	IR2	IR3	IR4
Write	100	0100	IW0	IW1	IW2	IW3	IW4	TBLKL	VDMSKH	SBW1
TA/BHV	100	1100	TA0	TA1	TA2	TA3	TA4	TA5	TA6	TAC
Mode	100	0010	XSLP	XIDL	GAIN	MRM	RB	SBW0	ABHV	OTMSKL
Misc	100	1010	SGMENL	GMENL	OC0	OC1	UC	BWR1	BWR2	FMSKH
Fault	100	0110	HOT	Low VDD	MR_O	MR_S	TF_O	TF_S	TF_F_L	X
PLR	100	1110	PLRDT1	PLRDT0	PLRPW1	PLRPW0	PLREN	WFMSKH	TAD	Res

ID register is read only.
Data bits default to 0 at reset condition, i.e. power-up or voltage fault condition, except ID register.
X = not used
Res = Reserved for TI internal use or future control features, User setting = 0.
FMENL hardwired = 0 in 4-channel device.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port Read/Write bit is not shown.

ID REGISTER (Read Only Register)
Address = 0000 001

BIT	NAME	DESCRIPTION
7	CH	Channel ID. 1 = 4 channel device 0 = 6 or 8 channel device
6:3	REV3:0	Device Revision. 110 assigned to 32R1611D6 (6-channel) 000 assigned to 32R1611D4 (4-channel)
2:0	VEN2:0	Vender ID. 001 is assigned for the 32R1611D

HS/IMR REGISTER
Address = 0001 001

BIT	NAME	DESCRIPTION
7:3	IR4:IR0	MR bias current setting, see Read Mode description for bias equation. LSB = 0.25 mA. 11111 = maximum MR bias current (9.75 mA) 00000 = minimum MR bias current (2.0 mA)
2:0	HS2:HS0	Head Select bits, see Table 9 for head select bit maps

WRITE REGISTER
Address = 0010 001

BIT	NAME	DESCRIPTION
7	SBW1	Servo Bank Write Control bit. Must be used in conjunction with SBW0 bit to activate servo bank write mode (see Bank Write Mode description) 1 = Activate servo bank write mode 0 = Disable servo bank write mode
6	VDMSKH	Low VDD Disable. 1 = Disable Low VDD voltage detection and reporting 0 = Enable Low VDD voltage detection and reporting.
5	TBLKL	Blanking time duration control. Sets the duration of the blanking time for write-to-read and MR bias off-to-on switching. 1 = Blanking on duration = 200 nsec 0 = Blanking on duration = 400 nsec
4:0	IW4:IW0	Write current magnitude, see Write Mode description for equation. DAC also used to set PLR pulse magnitude. Write mode: See Table 3. LSB = 1.45 mA (nom) 11111 = maximum write current (60 mA) 00000 = minimum write current (15 mA) PLR mode: See Table 7.

TAD REGISTER
Address = 0011 001

BIT	NAME	DESCRIPTION
7	TAC	Thermal Asperity Correction, enable when high. Correction on the fly. (TA compensation plus frequency shift at TA) TAC = 1 TAD = 1 MRM = 0 Correction retry mode. (continuous low corner frequency shift) TAC = 1 TAD = 0 MRM = 0
6:0	TA6:0	TA detection threshold (MRM=0, TAD = 1) or Digital Buffered Head Voltage comparator threshold (MRM=1, TAD = 0). LSB = 6 mV 1111111 = maximum threshold (762 mV) 0000001 = minimum threshold (6 mV) 0000000 = Invalid threshold setting

MODE REGISTER
Address = 0100 001

BIT	NAME	DESCRIPTION
7	OTMSKL	Over temperature detection, bank write mode only. 1 = Over temperature detection enabled Over temp condition sets HOT flag in Fault Status register. (No effect on read mode). 0 = Over temperature detection disabled
6	ABHV	ABHV Control. 6-channel version does not include ABHV feature. 1 = Enable ABHV mode when MRM = 1. FLT/BHV output configured as amplifier output. 0 = Disable ABHV mode.
5	SBW0	Servo Bank Write Mode enabled when toggled with other conditions. (See Bank Write Mode description)
4	RB	Read frequency boost 1 = Read Boost enabled. 2.5 dB boost at 220 MHz 0 = Disable Read frequency boost
3	MRM	MR Measurement Mode for digital BHV. (see MR Measurement Mode) 1 = Enables MR measurement mode (TAD = 0) 0 = Disables MR measurement mode
2	GAIN	Read Amplifier Gain select 1 = high gain mode (300 V/V) 0 = low gain mode (225 V/V)
1	XIDL	Idle Control Bit 0 = Idle mode enabled
0	XSLP	Sleep control bit 0 = Sleep mode enabled. Overrides all other control modes

MISC REGISTER
Address = 1010 001

BIT	NAME	DESCRIPTION
7	FMSKH	Fault report disable 1 = Disable reporting of all faults. MR bias will not be disabled upon an open MR head fault. 0 = Enable normal fault reporting
6:5	BWR2:BWR1	Programmable read bandwidth (-1 dB, nominal values listed) 11 = 123 MHz 10 = 110 MHz 01 = 288 MHz 00 = 241 MHz
4	UC	Write Current Undershoot Control 1 = maximum write current undershoot 0 = minimum write current undershoot. UC = 0 only valid when OC0 = 1.
3:2	OC1:OC0	Write Current Overshoot Control. (Alternate names: OC0 = DRV, OC1 = XC) 11 = Current boost and capacitive boost activated 10 = Capacitive boost only activated (XC) 01 = Current boost only activated (DRV) 00 = minimum write current overshoot
1	GMENL	High-Gm enable. Controls whether the High-Gm mode is activated during mode switching. The write-to-read, idle-to-read, MR bias off-to-on, head-to-head, and super-high-Gm on-to-off switching times are affected by this bit. 1 = High-Gm mode disabled 0 = High-Gm mode enabled. (Recommended setting = 0).
0 (6-ch)	FMENL	Fast mode during mode switching. Fast mode shifts the low corner frequency to 5 MHz for about 300 ns from the middle of the High-Gm period. Although other switching times are affected, this bit is primarily to improve write-to-read switching time. 1 = Disable Fast mode during High Gm period. 0 = Enable Fast mode during High Gm period. (Recommended setting = 0). Note: no FMENL bit in 4-ch device. FMENL = 0 by internal hardwire in 4-ch version.
0 (4-ch)	SGMENL	Super Gm mode control. Bit can be used to optimize idle-to-read and write-to-read switching times. 1 = Disables super high Gm stage irrespective of the operating mode. 0 = Enables super high Gm mode during certain mode conditions (Recommended setting = 0).

FAULT STATUS REGISTER
Address = 0110 001
Fault Status register provides status bits for determining which fault triggered an indication on the FLT/BHV pin. Logic 1 indicates the respective fault was detected. Writing 00h to this register will clear all status bits. Faults are written to this register on the active edge of the fault event. Therefore, if a fault condition continues to exist after clearing the status register, it will not be latched into this register again. Fault register may not clear upon power-up, user should write 00h to register to clear status register as part of power-up routine.

BIT	NAME	DESCRIPTION
7	--	Not Used
6	TF_F_L	Write Data Frequency Low detected
5	TF_S	Reserved for Write Head Short to Ground detected (Not operational on 32R1611D. Write head short will be reported as an write open head TF_O)
4	TF_O	Write Head Open or Short to Ground detected
3	MR_S	MR Head Short detected
2	MR_O	MR Head Open detected
1	Low VDD	Low VDD voltage detected.
0	HOT	Over temperature condition detected in bank write mode only. OTMSKL bit must be enabled to activate this flag.

PLR REGISTER
Address = 1110 001

BIT	NAME	DESCRIPTION
7 (6-ch)	SGMENL	Super Gm mode control. Bit can be used to optimize idle-to-read and write-to-read switching times. 1 = Disables super high Gm stage irrespective of the operating mode. 0 = Enables super high Gm mode during certain mode conditions (Recommended setting = 0).
7 (4-ch)	Res	Reserved. 0 = User setting.
6	TAD	Thermal Asperity Detector Enable 1 = Enables thermal asperity detector when MRM = 0. TA threshold set by TA6:0 bits (Register TAD) 0 = Disable TA detector
5	WFMSKH	Disable write faults 1 = Disables write fault reporting only. The functioning of the writer remains unchanged. All other fault modes operate normally. 0 = Enable normal write fault reporting
4	PLREN	Pin Layer Reset Enable 1 = Enable Pin Layer Reset mode 0 = Disable Pin Layer Reset mode
3	PLRPW0	PLR reset pulse width control, T2 1 = 95 nsec 0 = 48 nsec
2	Res	Reserved for PLRPW1. User setting = 0
1:0	PLRDT0:PLRDT1	PLR pulse decay slew rate control. See Table 6. Times assume C1 = 22 nF. 11 = 1.9 V/µsec 01 = 3.6 V/µsec 10 = 5.3 V/µsec 00 = 6.8 V/µsec

TABLE 9: Head Selection

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	BANKWRITE MODE HEAD SELECTED
0	0	0	0	None
0	0	1	1	Odd heads (1,3,5,7)
0	1	0	2	None
0	1	1	3	None
1	0	0	4 (4 ch = Dummy)	None
1	0	1	5 (4 ch = Dummy)	All Heads
1	1	0	Dummy	None
1	1	1	Dummy	Even heads (0,2,4,6)

NOTE: Selection of out-of-range head selects internal dummy head. Out-of-range heads include heads 4,5,6,7 on 4-channel device, and heads 6,7 on 6-channel device. Out-of-range head selection reported as FLT on 4-channel device only.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RREF	I/O	Applies to 6-channel device only. External resistor connection to set reference current for internal current DACs. 2KΩ reference resistor connects between RREF and REFGND.
REFGND	I/O	Applies to 6-channel device only. Return connection for reference resistor (RREF).
XMRBIAS	I	MR bias current on: 3.3V logic with internal pull-up. Bias current active at low.
WnX, WnY	O	Inductive write head connection.
RnX	I/O	MR read head connection, positive end.
HGND	I	MR head connection, negative end.
FLT/BHV	O	Multiplexed pin: Fault output, BHV or ABHV. Fault mode: (MRM = 0) (ABHV = 0). An open collector output. Read mode: A low indicates abnormal read condition. Write mode: A high indicates abnormal write condition. MR measure mode: DBHV comparator output. (MRM = 1) (ABHV = 0). An open collector output. A high indicates the head voltage is lower than the set threshold. A low indicates the head voltage is higher than the set threshold. ABHV mode: (ABHV = 1, MRM = 1). The output is an analog voltage which is a measure of head voltage (ABHV gain = 5V/V). Remove any pull-up resistors on FLT/BHV output in ABHV mode. 6-channel device does not include ABHV function.
XR/W	I	Read/Write: 3.3 V logic with internal pull-down. Write active high
RDX,RDY	O	Differential Read Data output.
GND	I	Ground
VCC	-	+5V power supply.
VDD	-	+8V power supply.
SDEN	I	Serial Port Enable. 3.3 V logic.
SDATA	I/O	Serial Data. 3.3 V logic.
SCLK	I	Serial Clock. 3.3 V logic.
C1	I	Bias loop control capacitor, C1, connected to ground (0.01 or 0.022 μF)
WDX/WDY	I	Write Data input, PECL

ELECTRICAL SPECIFICATION

Unless otherwise specified, RREF = 2.0KΩ, Rmr=45Ω Imr=6mA (setting value), C1 = 0.022 uF, Ltf=90nH, Rtf=18Ω, Iw=39.65 mA (setting value,6-ch), Iw=40.57 mA (setting value,4-ch). RDX/RDY load = 2 KΩ diff.

ABSOLUTE MAXIMUM RATINGS

Operation beyond maximum ratings may result in permanent damage to the device.

PARAMETER		RATINGS
DC Supply Voltage	VCC	-0.3 to 6 VDC
DC Supply Voltage	VDD	-0.3 to 9 VDC
Logic Input Voltage	3.3 V Logic	-0.3 to VCC + 0.3 V
	WDX/WDY	-0.3 to 6.0 VDC
Differential WD Input Voltage	WDX/WDY	2.0 V
Write Current	Iw	75 mA 0-pk
MR Bias Current	I	20 mA
Write Head Voltage	V	-0.3V to VDD+0.3 V
Read Head Voltage	V	-0.3 to 1.5 V
Output Current	RDX,Y	-10 mA
Storage Temperature	Tstg	-55 to 150 °C
Operating Junction Temperature	Tj	+150 °C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		RANGE
DC Supply Voltage	VCC	4.5 to 5.5 VDC
DC Supply Voltage	VDD_Write	7.2 to 8.8 VDC
	VDD_Bankwrite	4.5 to 5.5 VDC
Write head load range	L	60 to 180 nH
Write head resister range	R	5 to 25 Ω
MR head range	R	25 to 75 Ω
Operating Ambient temperature	Ta	0 to 70 °C

POWER SUPPLY

FMENL = GMENL = SGMENBL = BWR2 = 0, TBLKL = BWR1 = 1

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current VCC	Sleep		1.6	4	mA
	Idle		8	11	mA
	Read IMR off		12	15	mA
	Read IMR on		35	50	mA
	Write IMR off,		28	35	mA
	Write IMR on,		36	49	mA
	Bankwrite 4 channel, all hds Iw=30mA, Vdd = +5.5 Vdc, Vcc = +5.5 Vdc, Imr on		70	95	mA
	Bankwrite 6 channel, all hds Iw=30mA, Vdd = +5.5 Vdc, Vcc = +5.5 Vdc Imr on		84	115	mA
	Imr off		76	100	MA
VDD Supply Current VDD	Sleep		0.12	0.5	mA
	Idle		4.4	5.5	mA
	Read, Imr on		16	22	mA
	Read Imr off		4.5	5.6	mA
	Write, Imr on		71	89	mA
	Write, Imr off		59	74	mA
	Bankwrite 4 channel, all hds Iw=30mA, Vdd = +5.5 Vdc, Vcc = +5.5V, Imr on		168	205	mA
	Bankwrite 6 channel, all hds Iw=30mA, Vdd = +5.5 Vdc, Vcc = +5.5 Vdc Imr on		238	286	mA
	Imr off		226	270	

Servo Bank Write Equations (mA): I(Vdd) = 95+23.8*N (Imr ON). I(Vdd) = 83+23.8*N (Imr OFF).
(6-Channel) I(Vcc) = 97-2.22*N (Imr ON). I(Vcc) = 89-2.22*N (Imr OFF).
Where N = # of Channels activated

DIGITAL INPUT/OUTPUT

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input High Voltage (XR/W,SDEN,SCLK, SDATA,XMRBIAS)	V_{IH1}	3.3 V Logic C_L = 30 pF	1.75			VDC
Input Low Voltage (XR/W,SDEN,SCLK, SDATA,XMRBIAS)	V_{IL1}	3.3 V Logic C_L = 30 pF			0.7	VDC
Input Hysteresis	V_{HYS}		120	185	260	mV
Input Leakage Current (SDEN,SCLK,SDATA)	Ileak	Inactive state			1	µA
Pull-up resistor (XMRBIAS)	Rpu		15	20	25	KΩ
Pull-down resistor (XR/W)	Rpd		37.5	50	62.5	KΩ
Common mode voltage	V_{CMW}	WDX-WDY PECL Inputs	1.4	2	2.6	VDC
Input Δ Voltage	ΔV_{I3W}	Write Mode	0.4			V diff
Input Δ Voltage	ΔV_{I3R}	Read or Idle Mode	0			V diff
Input Δ Voltage	ΔV_{I3S}	Sleep mode	0			V diff
Differential input R	Z_{ID}	WDX/WDY input	100	125	150	Ω
Input Capacitance	Cinw	WDX,WDY Cap to ground			5	pF
Input Current	I_{IH3}	Write Mode ΔV_{I3W} = 0.4V		3.2		mA
Output High Voltage	V_{OH}	R_L = 1.7K Ω (FLT)	Open Collector			
		R_L = 1K Ω (SDATA)				
Output Low Voltage	V_{OL}	R = 1.7K Ω to 3..6 V (FLT)			0.3	V
		R_L = 1K Ω to 3.6 V (SDATA)			0.3	V
Output Low Sink Current	I_{OL}	R = 1.7K Ω to 3..6 V (FLT)	3.0			mA
		R_L = 1K Ω to 3.6 V (SDATA)	5.0			mA

SERIAL PORT TIMING
(See Figures 3 & 4)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		40			nS
SCLK Low Time	T_{CKL}		14			nS
SCLK High Time	T_{CKH}		14			nS
Enable to SCLK	T_{SENS}		14			nS
SCLK to Disable	T_{SENH}		10			nS
Data Set-up Time	T_{WDS}		6			nS
Data Hold Time	T_{WHD}		6			nS
SDEN min. Low Time	T_{SL}		80			nS
Address to Data Turnaround time	T_{trn}		20			nS

CURRENT DAC REFERENCE (6-CHANNEL DEVICE ONLY)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Voltage Reference	Vref		1.9	2.0	2.1	V
Reference R Range	Rref			2.0		KΩ
Reference Current	Iref	Rref=2k		1		mA

READ CHARACTERISTICS

SGMENL = GMENL = BWR2 = FMENL = 0, TBLKL = BWR1 = 1, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		25	45	75	Ω
MR Bias Current	Programmable Range	2.0		9.75	mA
MR Bias Current Resolution			5		bit
LSB			250		μA
MR Current Tolerance	IR DAC = 0	-15		+15	%
	IR DAC >0	-8		+8	%
MR Head DC Voltage Range		100		900	mV
Unselected Head Current				± 10	μA
Input Resistance (RIN)			3.2		Ω
Differential Voltage Gain	R_{MR} = 45Ω, Low Gain load = 2KΩ diff, f = 80 MHz	180	225	270	V/V
	R_{MR} = 45Ω, High Gain load = 2KΩ diff, f = 80 MHz	240	300	360	V/V
Read Gain Constant	Av*(RMR+RIN), Low Gain		10850		Ω
	Av*(RMR+RIN), High Gain		14460		Ω
Head to head gain variation				2	%
Bandwidth, Low Gain	Lower -3dB, C1 = 0.01 uF	150	540	800	KHz
Rmr = 45 Ω, , Lh = 0 nH,	Lower -3dB, C1 = 0.022 uF	100	350	685	KHz
BWR2,BWR1 = 00	Higher -1dB	170	241		MHz
load = 2KΩ diff,	Higher -3dB, RB=0	280			MHz
(see Note 1)					
Bandwidth Control	Higher –1 dB, BWR2:1 = 01		288		MHz
Low Gain, load = 2KΩ diff	Higher –1 dB, BWR2:1 = 10		110		MHz
Rmr = 60 Ω, Lh = 0 nH	Higher –1 dB, BWR2:1 = 11		123		MHz
Group delay flatness	f = 15 - 170 MHz, low gain, no boost		0.35		ns
Boost Voltage Gain	Low gain, RB = 1 BWR2,BWR1 = 00	1.8 @ 160	2.5 @ 220	3.1 @ 310	dB @ MHz
Input Noise (Excludes RMR, includes current noise)	R_{MR} = 45Ω, low gain mode, f = 1 - 85 MHz, Load = 2KΩ		1.1		nV/√Hz
THD	Vin = 0.5 mV p-p, F=40 MHz Imr = 6 mA, Load=220Ω diff		-58	-53	dB
Dynamic range	THD < -40 dB@ 40 MHz Imr = 6 mA, Load=220Ω diff	3	3.5		mV

NOTE 1: Bandwidth Is Specified For Rmr = 45 Ω And Lh = 0. Device Verification Performed At Rmr = 60 Ω To Offset Test Set-Up Inductance.

READ CHARACTERISTICS (CONTINUED)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Offset Voltage	Low Gain	-200		200	mV
	High Gain	-300		300	mV
Head to head offset voltage				50	mV
Output Current	220 ohm load differential	2.3	4	6	mA
Output Current Leakage	Non-read mode	-40		+40	µA
Output Common Mode Voltage		Vcc-3.85	Vcc-3.25	Vcc-2.85	V
Output Resistance	Single-ended		40		Ω
Output Resistance	Differential		100		Ω
PSRR (VCC)	Vin = 100 mV p-p @ 40 MHz Load = 2KΩ diff, no bypass caps	41			dB
PSRR (VDD)	Vin = 100 mV p-p @ 40 MHz Load = 2KΩ diff, no bypass caps	42			dB
Channel Separation	15 - 40 MHz	49.5			dB
	40 - 170 MHz	35.5			dB

MR BIAS OVERSHOOT/UNDERSHOOT

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
MR bias overshoot	Iosbir	Idle to read		0		%
MR bias overshoot	Iosbri	Read to idle		0		%
MR bias overshoot	Iosvfr	Vcc Fault to read		0		%
MR bias overshoot	Iosvdfr	VDD fault to read		0		%
MR bias overshoot	Iosrwe	Read to write with bias on		0		%
MR bias overshoot	Ioswrd	Write to read with bias off		0		%
MR bias overshoot	Ioswre	Write to read with bias on		0		%
MR bias overshoot	Ioshs	Head switch, no bias change		0		%
MR bias overshoot	Iosc	Bias cycling		0		%

WRITE CHARACTERISTICS

OC1 = OC0 = 1, UC = 0, GMENL = BWR2 = SGMENL = FMENL =0, TBLKL = BWR1 = 1,
Iw = 39.65 mA (setting value,6-ch), Iw = 40.57 mA (setting value,4-ch) .

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Nominal Range (see Table 3)	Single head write 6-Channel device	15		60	mA
	Single head write 4-Channel device	16.3		60.5	mA
Write Current Resolution			5		bit
LSB	6-Channel device		1.45		mA
	4-Channel device, 0 ≤ N≤ 15		1.458		mA
	4-Channel device, 16 ≤ N≤ 31		1.330		mA
Write Current Accuracy	6-Channel device, N ≥ 3	-8		+8	%
	6-Channel device, N ≤ 2	-15		+15	%
	4-Channel device, 3 ≤ N ≤ 28	-8		+8	%
	4-Channel device, N≤2,N≥29	-15		+15	%
Head Voltage Swing	Open Head, Vdd = 8 VDC		7.5		Vpp
	Transient, Vdd = 8 VDC		7.5		Vpp
Unselected Head Current	DC	-50		50	μA
Write data frequency range		5		400	MHz

BANK WRITE CHARACTERISTICS

OC1 = OC0 = 1, UC = 0, GMENL = BWR2 = SGMENL = FMENL =0, TBLKL = BWR1 = 1, VDD = 5.0 VDC.
Iw = 29.5 mA

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Nominal Range	All head bank write	15		35	mA
Write Current Resolution			5		bit
LSB			1.45		mA
Write Current Accuracy		-8		+8	%
Head Voltage Swing	Open Head, Vdd = 5 VDC		3.5		Vpp
	Transient, Vdd = 5 VDC		4.0		Vpp

MR BIAS DURING SERVO BANK WRITE

OC1 = 1, OC0 = 1, UC = 0, GMENL = BWR2 = SGMENL = FMENL =0, TBLKL = BWR1 = 1, VDD = 5.0 VDC.
Iw = 29.5 mA

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR bias nominal current range, 32R1611D-6	6 head bank, all Rmr equal	0.33		1.625	mA
	3 head bank, all Rmr equal	0.67		3.25	mA
MR bias nominal current range, 32R1611D-4	4 head bank, all Rmr equal	0.50		2.437	mA
	2 head bank, all Rmr equal	1.00		4.875	mA

NOTE: Average MR bias /head = IMR setting / # of activated heads

HEAD VOLTAGE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DBHV threshold resolution			7		bit
DBHV minimum threshold setting	Guaranteed comparator operation over voltage/temp		204		mV
LSB			6		mV
DBHV threshold accuracy	Guaranteed DBHV threshold from 204 to 762 mV	-15		+15	%
MR head short detect threshold			50	75	mV
MR head open detect threshold		900	970	1040	mV
ABHV Gain	Room Temperature	4.6	4.9	5.2	V/V
ABHV Output Drive	FLT/BHV output, Imr = 6 mA	14	27		µA

THERMAL ASPERITY DETECTION/CORRECTION/FAST RECOVERY
SGMENL = GMENL = BWR2 = FMENL = 0, TBLKL = BWR1 = 1

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TA Detection Resolution			7		bit
TA Detection Minimum threshold	At output before correction	4.5	6	7.5	mV
TA Detection Maximum threshold	At output before correction	571	762	953	mV
LSB	Ref=2kΩ	4.5	6	7.5	mV
TA Detect Accuracy	TA threshold > 384 mV TA rise time = 30 ns, at output	-10		35	%
Lower Corner Frequency	- 3dB, correction mode	4.3	5	6	MHz
TA Detection Delay			65	100	ns
TA Correction Delay			0.4	1.0	µs
TA Event over Delay		0.1	0.3	1.0	µs

PLR CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLR Amplitude Resolution			5		bit
PLR Amplitude Range	T2 pulse amplitude	0.41	0.6	1.48	V
LSB	0d < Iw < 23d	30	40	50	mV
PLR Pulse width, T2	PLRPW = 0		48		ns
	PLRPW = 1		95		ns
PLR decay slew rate, T1 C1 = 10 nF (see Note 1)	PLRDT0/PLRDT1 = 11		3.5		V/µs
	PLRDT0/PLRDT1 = 01		6.6		V/µs
	PLRDT0/PLRDT1 = 10		9.3		V/µs
	PLRDT0/PLRDT1 = 00		11.9		V/µs
PLR decay slew rate, T1 C1 = 22 nF (see Note 1)	PLRDT0/PLRDT1 = 11		1.9		V/µs
	PLRDT0/PLRDT1 = 01		3.6		V/µs
	PLRDT0/PLRDT1 = 10		5.3		V/µs
	PLRDT0/PLRDT1 = 00		6.8		V/µs
PLR Trigger Delay (see Note 2)	C1 charge time after PLR armed. C1 = 10 nF		6.9	10.4	µs
	C1 = 22 nF		20	50	µs
PLR Recovery Delay (see Note 2)	C1 recovery to normal read after PLR disarm C1 = 10 nF		1.3	1.7	µs
	C1 = 22 nF		8	10	µs

NOTE 1: Decay slew rate measured from 70% to 30% of PLR amplitude.
NOTE 2: PLR delays are measured at 95% of C1 final value.

SWITCHING CHARACTERISTICS

SGMENL = GMENL = BWR2 = FMENL = 0, TBLKL = BWR1 = 1,and C1 = 0.022 µF, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write to Read Switching	90% signal envelope, ±30mV DC, after high pass filter TBLKL = 1,			500	ns
Read to Write Switching	90% of Iw		20	50	ns
Idle to Read Switching	90% signal envelope, ±30mV DC C1 fully discharged (C1=22 nF)		8	10	µs
Read to Idle Switching	10% of read envelope, ±30mV DC		100	700	ns
Head Switching, read mode	90% signal envelope, ±30mV DC		14	20	µs
Head Switching, write mode (see Note 1)	90% of write current		N/A		ns
Write to Idle or Iw turnoff	Delay for Iw to meet Ileak spec		30	50	ns
Sleep to Idle				600	µs
Idle to Sleep				10	µs
Iw rise/fall time 10% to 90%	Lh=90nH, Iw=39.65 mA (6-ch), Iw = 40.57 mA (4-ch) Vdd=8V, OC0/OC1 = 1/1		0.9		ns
	Lh=90nH, Iw=29.5 mA, Vdd=4.5V,		1.75		ns
Head Current Delay (TD3)	50% of WD to 50% of Iw		4.5	10	ns
Write Current Asymmetry	Propagation delay difference 50% duty cycle write data @ 15 MHz			0.1	ns

NOTE 1. Head switches in write mode are not recommended.

FAULT DETECTION

SGMENL = GMENL = BWR2 = FMENL = 0, TBLKL = BWR1 = 1, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
WD low freq fault detect FLT low to high (TD1)		0.5	1	2	µs
WD low freq fault clear FLT high to low (TD2)			0.3	1.1	µs
Write data frequency	Valid transient detector			400	MHz
	Valid Open detector	10	13.5	18	MHz
VCC Fault Voltage	Write mode Iw<0.2mA	3.55	3.75	3.95	V
VCC Fault hysteresis	Fault removed	100	130	200	mV
VDD Fault Voltage	Write mode Iw<0.2mA	5.6	6.1	6.6	V
VDD Fault hysteresis	fault removed	450	550	650	mV
Over temperature detection threshold	Servo Mode, HOT = 1		135		°C

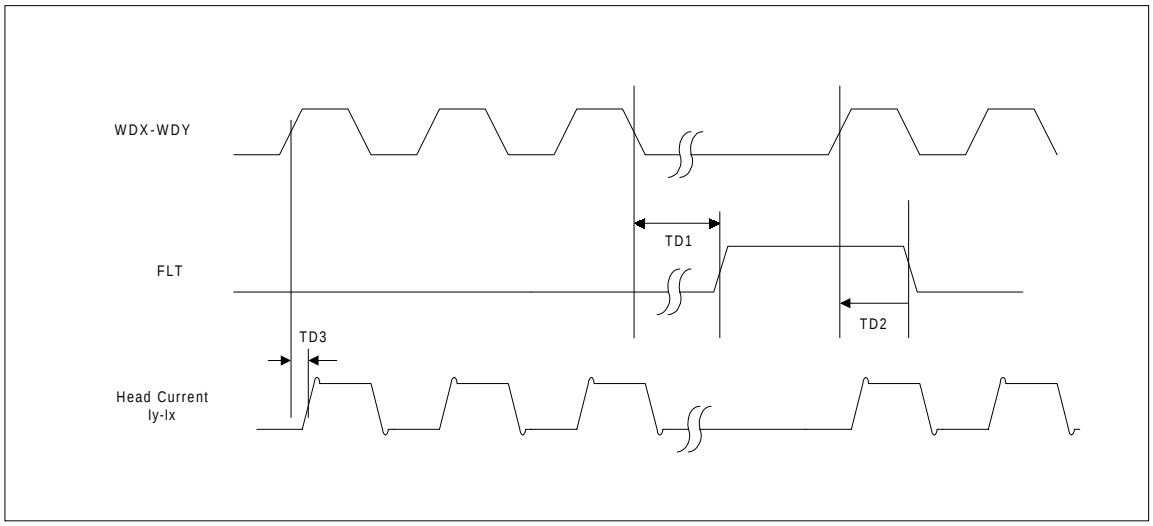


FIGURE 5: Write Current & Head Unsafe Timing

APPENDIX 1. APPLICATION NOTES

RECOMMENDED MODE SEQUENCES

Flowcharts of suggested sequences for various mode controls are included here. Although these charts represent recommended operational sequences, the do not represent the only sequence which will work for a particular operation. The charts each include some operational notes.

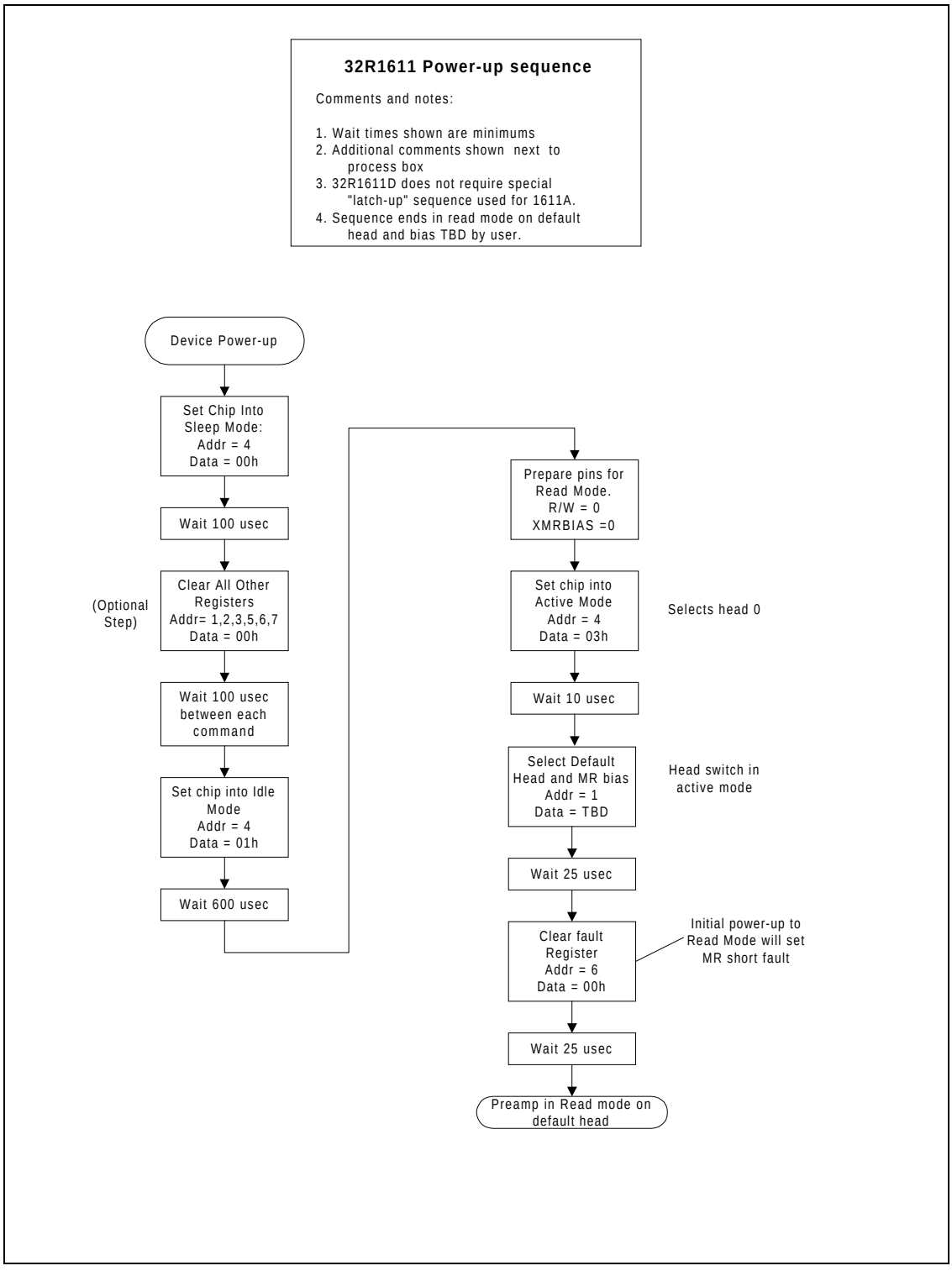


FIGURE A1: Power-up Sequence

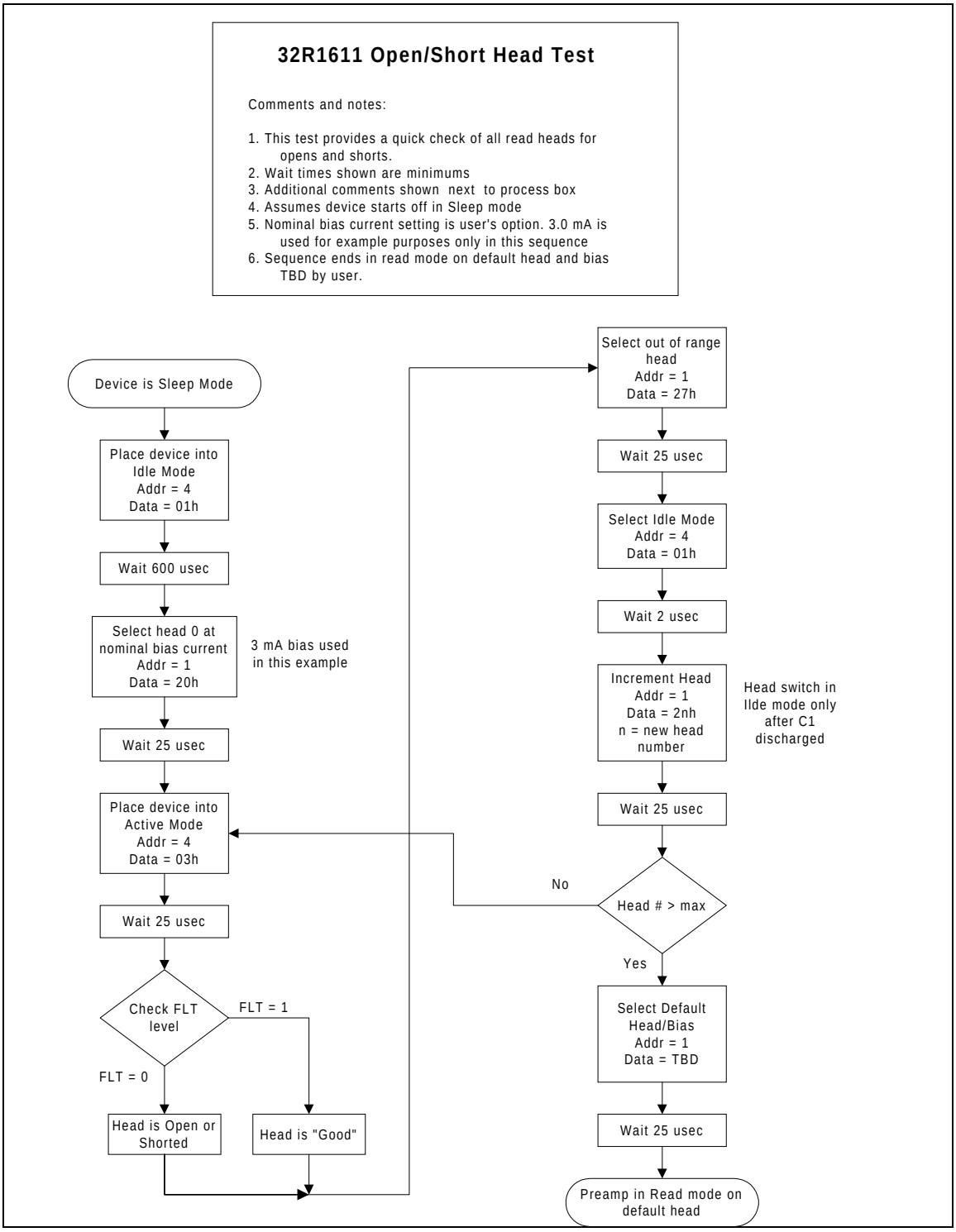


FIGURE A2: MR Open/Short Test Sequence

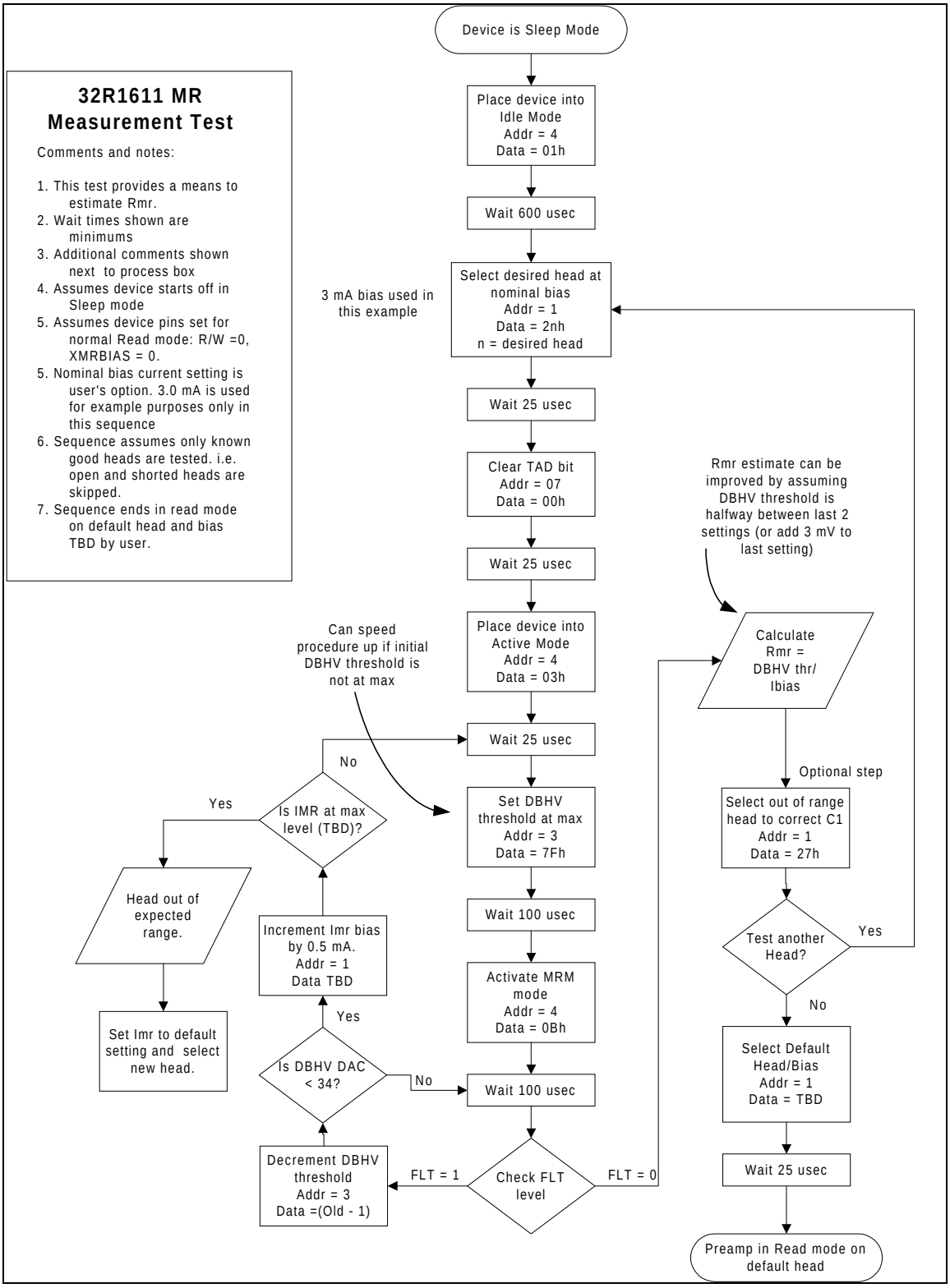


FIGURE A3: MR Measurement Sequence

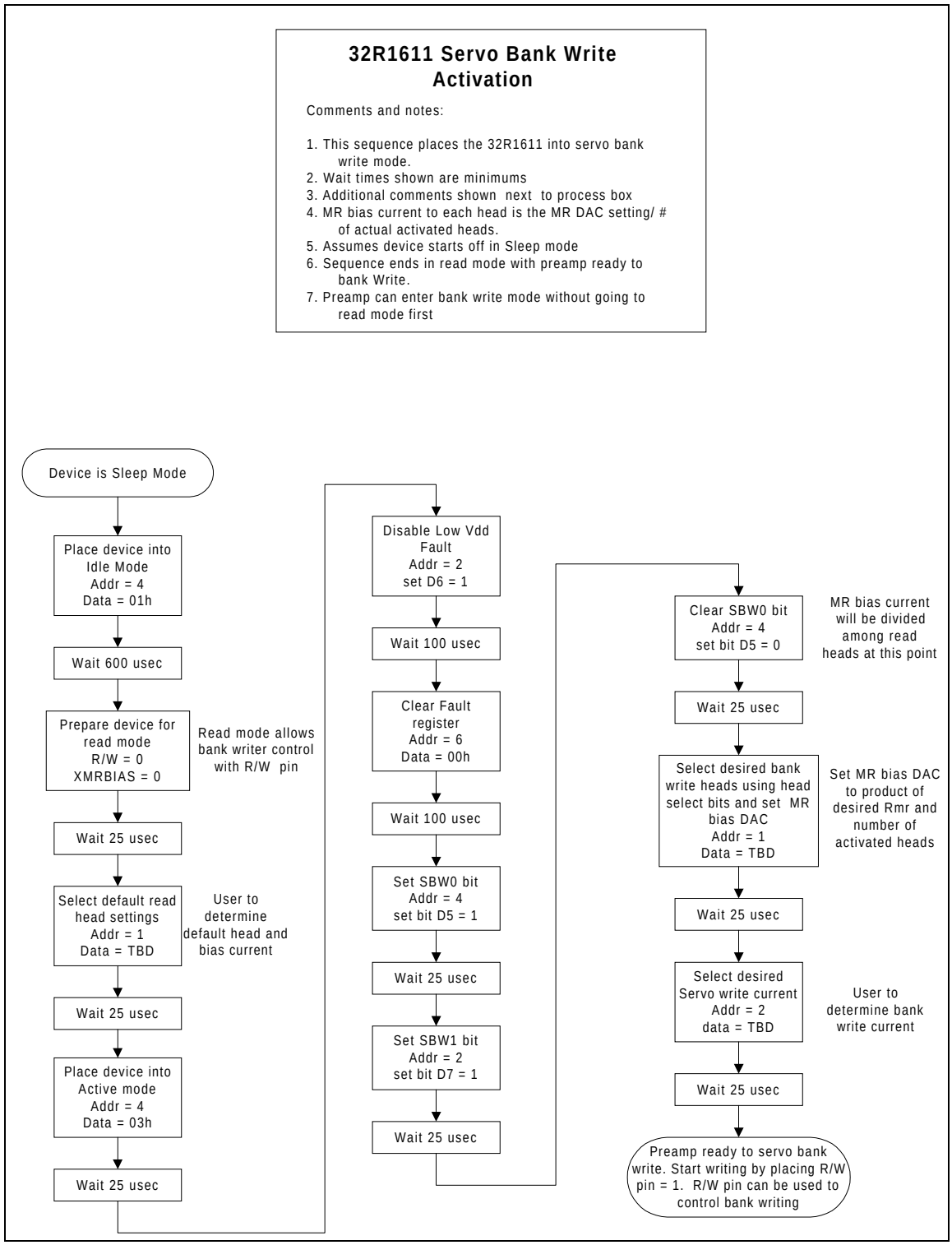


FIGURE A4: Servo Bank Write Activation

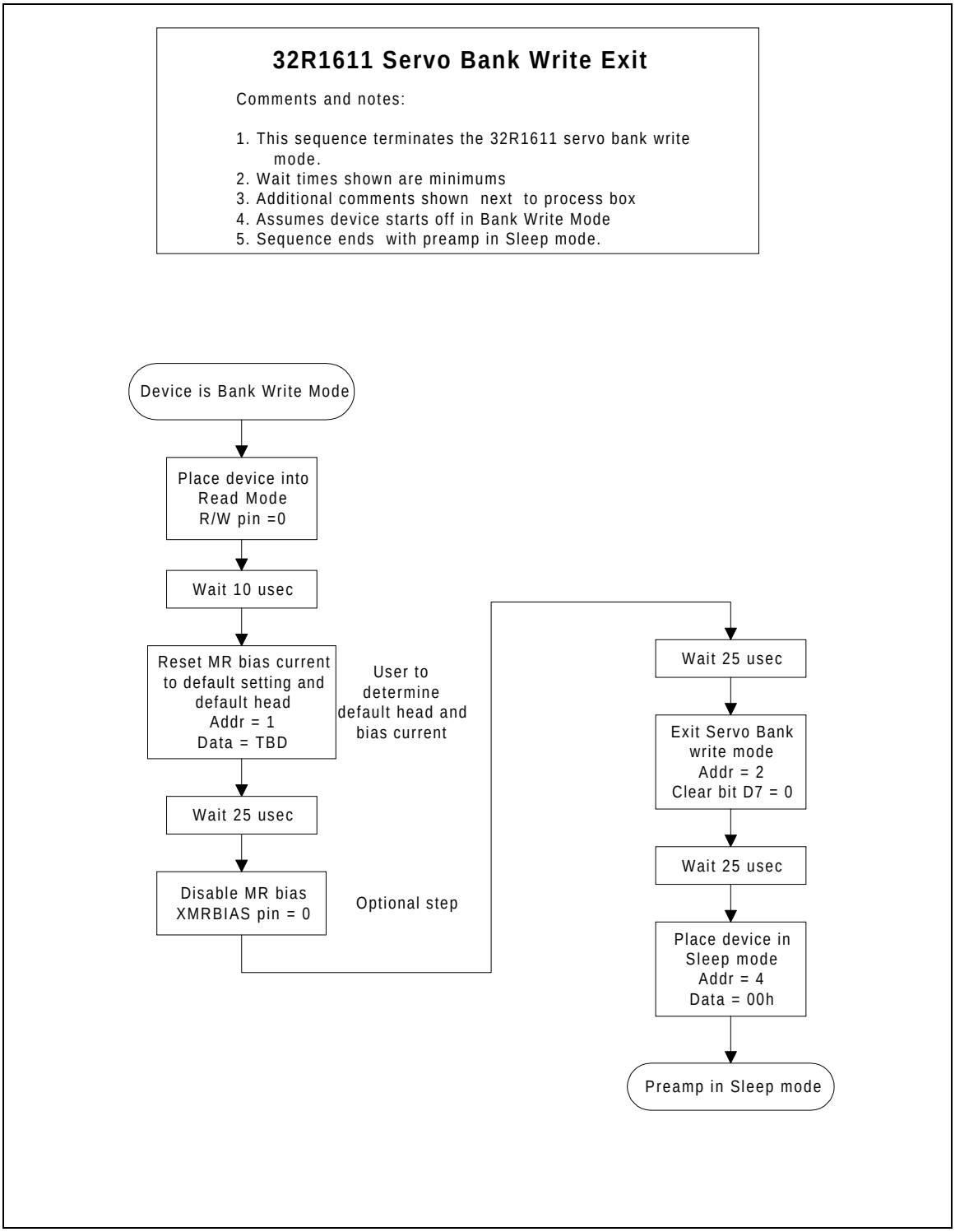


FIGURE A5: Servo Bank Write Exit Sequence

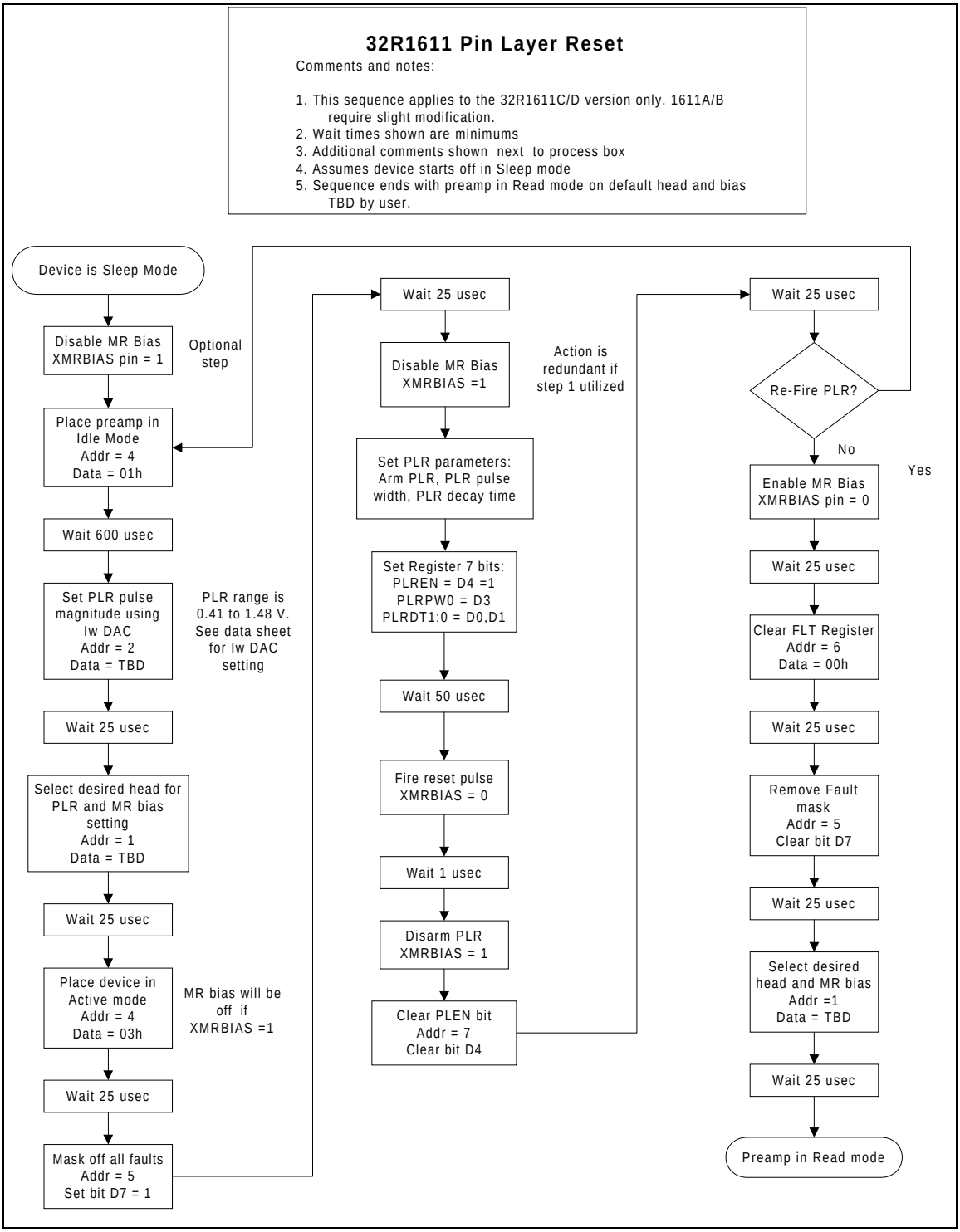
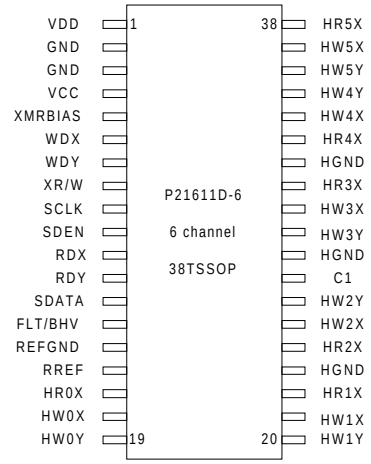
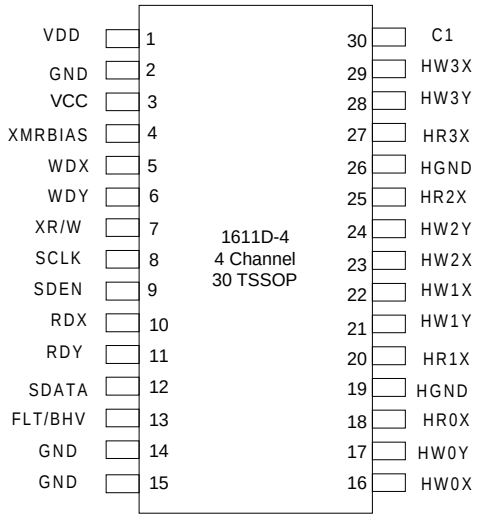


FIGURE A6: PLR Sequence

PACKAGE PIN DESIGNATIONS





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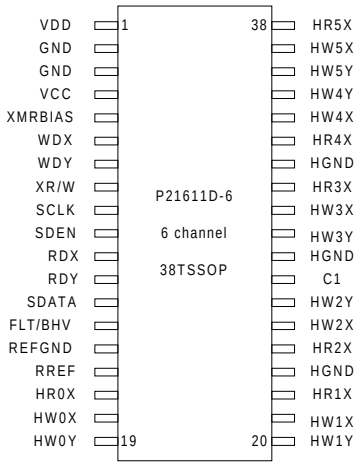
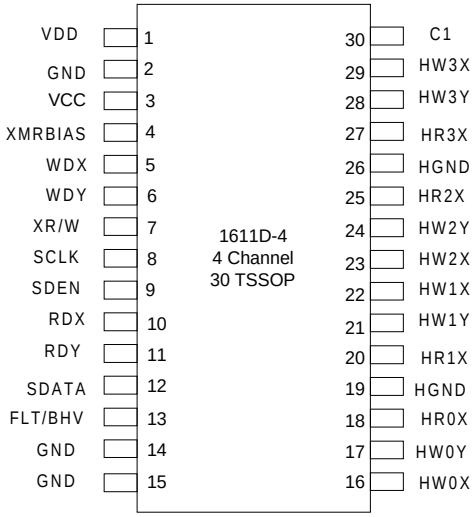
PACKAGE PIN DESIGNATIONS





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32R1615DR
+5, +8V 4/8-CHANNEL GMR READ/WRITE DEVICE

May 2000

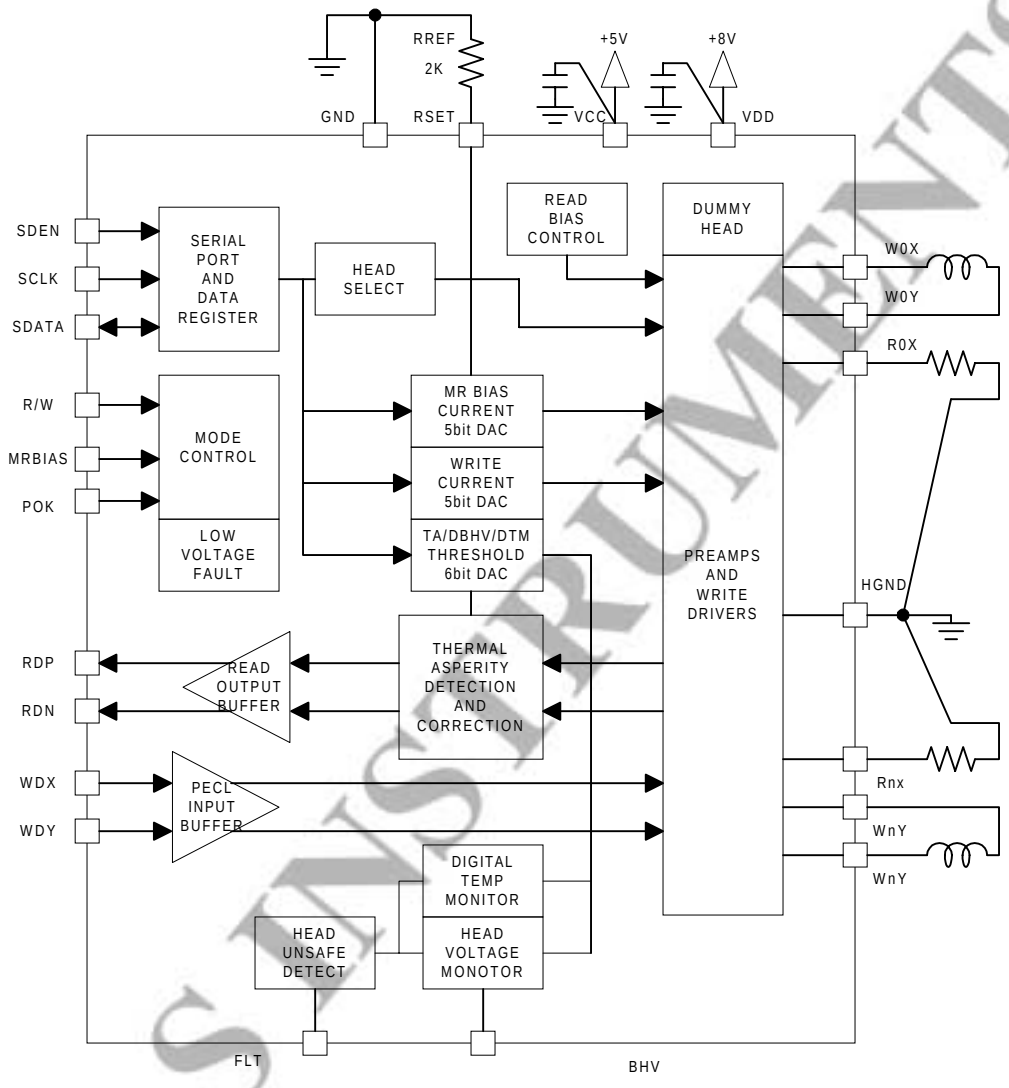
DESCRIPTION

The TI 32R1615DR is a BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive read and thin film write composite recording heads. It provides a low noise 5 volt GMR head amplifier, GMR bias current control, an 8 volt thin film write driver, write current control, thermal asperity detection and correction, and TFH fault detection circuit for up to eight channels. The device features programmable read gain, write damping resistance and thermal asperity threshold level. The device allows multiple channel write functions for servo writing. Half or all of the heads can be simultaneously selected in the servo write mode. Control of features and thresholds is provided through a serial port interface. The TI 32R1615DR requires a +5V and a +8V supply and is available in an eight or four channel version.

FEATURES

- **One side grounded input, fully differential output**
- **Unselected Read/Write heads at GND potential**
- **Thermal asperity detection and compensation**
- **MR resistor measurement mode**
- **MR bias current range = 2.2 to 8.2 mA (5 bit)**
- **MR resistor range =35 to 80Ω**
- **Programmable read gain constant = 8000 Ω or 12000 Ω**
- **Input equivalent noise 1.0 nV/√Hz @ 50 Ω**
- **Read Frequency boost**
- **Read blocking and noise capacitors integrated on chip**
- **Write current range = 15.75 to 60.7 mA (5 bit)**
- **Programmable write damping resistor (2 bit)**
- **Active write damping (1 bit)**
- **Programmable write current boost (2 bit)**
- **PECL no flip-flop**
- **Servo bank write**
- **MR bias during servo write capability**
- **Analog and Digital temperature monitor function**
- **3V compatible analog and digital I/O**
- **Power fault protection**
- **8-Channel (32R1615DR-8) or 4-Channel (32R1615DR-4) versions**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

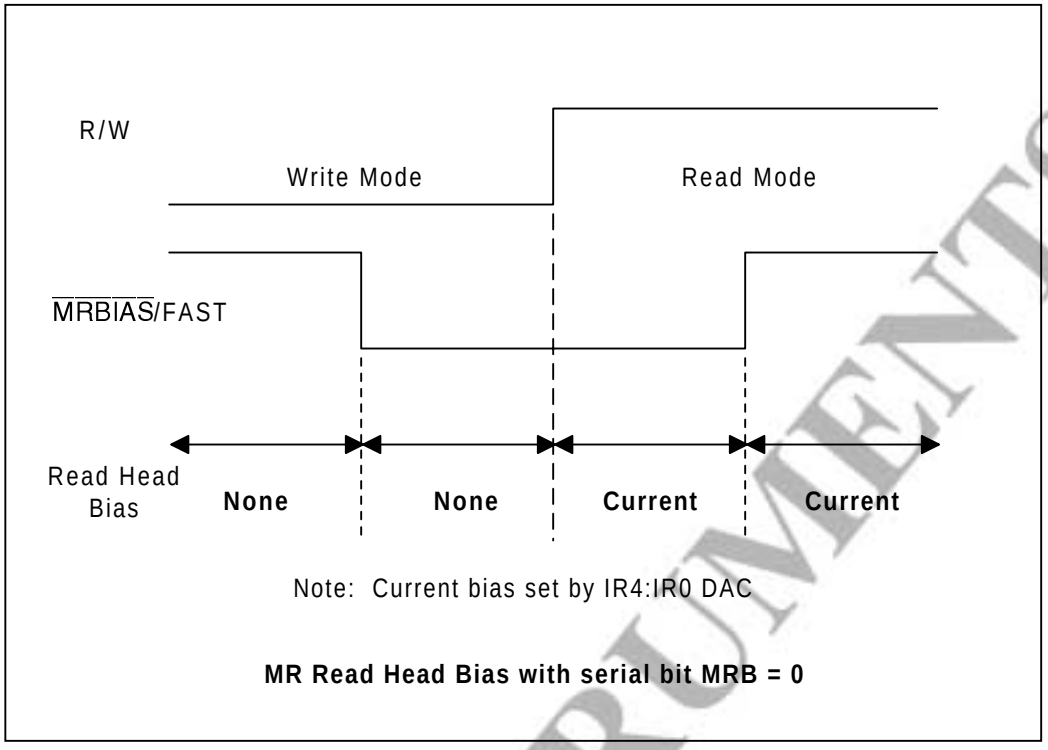
The TI 32R1615DR addresses up to 8 four-terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with TTL pins R/$\overline{W}$, $\overline{MRBIAS}$/FAST, POK and the serial port as shown in Table 1. The R/$\overline{W}$ and POK inputs have internal pull-up resistors so that when left opened, it will default to the TTL high state, while the $\overline{MRBIAS}$/FAST input has an internal pull-down resistor.

The serial port is used to control head selection, bank write mode, write current magnitude, MR bias current, read gain, MR head resistance measurement, and thermal asperity threshold level and mode.

TABLE 1: Mode Selection.

R/W	MRB	MRBIAS/FAST		SBW	IDL	SLP	POKB *POK Note 1	Mode	MR head bias on selected head	
									IMR DAC	HB DAC (IMRB)
1	1	1	-	x	1	1	x	Read Inactive Note 4	OFF	ON
1	1	0	-	x	1	1	x	Read Active	ON	OFF
1	0	-	1 Note 2	x	1	1	x	Read Active Fast recovery mode	ON	OFF
1	0	-	0 Note 2	x	1	1	x	Read Active	ON	OFF
1	0	x	x Note 3	x	1	1	x	Read Active	ON	OFF
0	1	1	-	0	1	1	1	Write	OFF	OFF
0	1	0	-	0	1	1	1	Write	OFF	ON
0	0	x	-	0	1	1	1	Write	OFF	OFF
0	x	x	-	1	1	1	1	Servo Bank Write	OFF	ON Note 5
0	x	x	-	x	1	1	0	Write /Servo Disabled	OFF	OFF
x	x	x	-	x	0	1	x	Idle	OFF	OFF
x	x	x	-	x	x	0	x	Sleep	OFF	OFF

NOTE 1. This represents the logical AND of POKB bit and POK pin
NOTE 2. When in TA retry recovery mode, TAD=0, TAC=1.
NOTE 3. When not in TA retry recovery mode.
NOTE 4. Read path is off in this mode.
NOTE 5. All MR heads are bias up to 120mV regardless head selection.



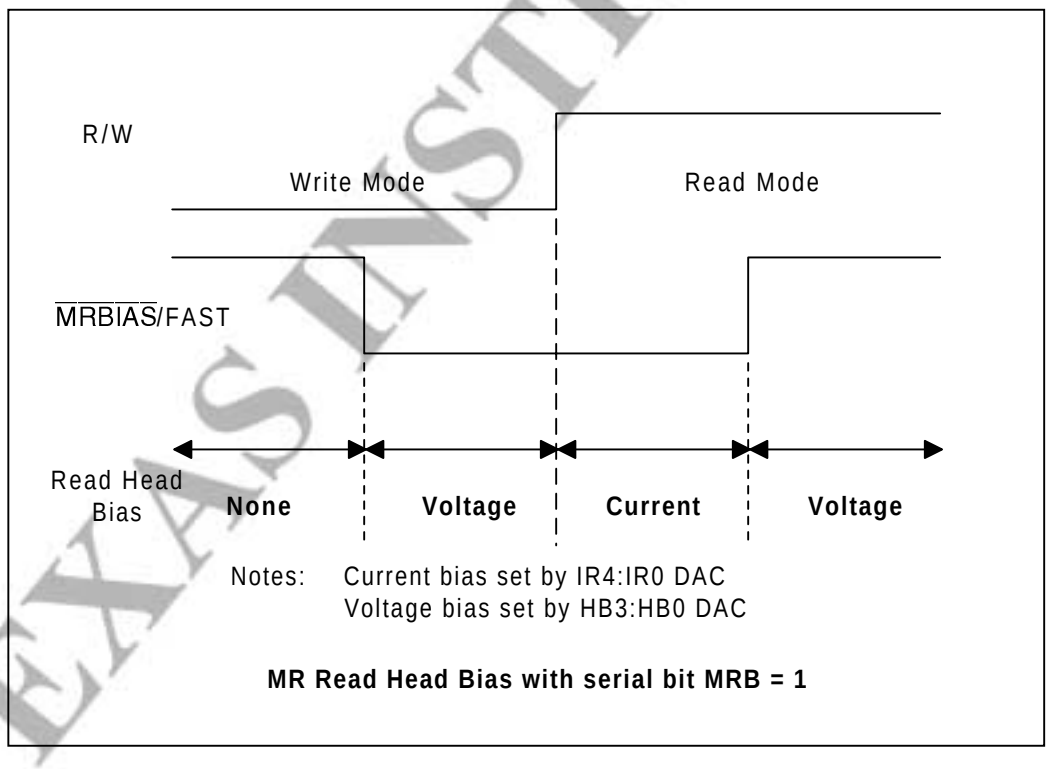


FIGURE 1: MR Bias Control

WRITE MODE

Taking R/$\overline{W}$ low in non-idle mode selects write mode. Write current is enabled to the selected channel and write data (WDX/WDY) controls the write current polarity. Head current is toggled between the X and Y side of the selected head on each transition of the differential PECL signal WDX-WDY. When WDX is higher than WDY, the current flows from X (WnX) to Y (WnY). The write function is disabled when POK pin is low.

The 32R1615DR write and servo bank write modes are fully enabled only when both the POK pin and POKB serial port bit are logic high (with R/$\overline{W}$ = 0). Placing the POK pin low will disable write mode. The POKB bit is bi-directional: the chip will reset POKB = 0 when the POK pin transitions from high to low. The user must set POKB = 1 and place the POK pin high in order to restore write mode control to the R/$\overline{W}$ pin.

Write current magnitude is controlled by a five-bit on board DAC. The DAC is programmed via the serial port. The magnitude of the write current (0-pk) is given by:

$$Iw\ (mA) = 15.75 + 1.45*N\ (mA\ 0\text{-}p)$$

where RREF = 2.0 KΩ and N = 0,1 ... 31 is the decimal value of serial port register bits IW0:IW4.

Note that the actual head current Ix,y is given by:

$$Ix,y\ (mA) = \frac{Iw}{1+\frac{Rh}{Rd}}$$

where Rh is the head DC resistance and Rd is the damping resistor (programmable).

The 32R1615DR writer includes 5 bits of write current waveshape control. There are 2 bits of write current boost (WCB2:WCB1), which boosts the write current during write data transitions. There are also 2 bits of damping resistance control to passively control overshoot and ringing (DR1:DR0). Lastly, the AWD bit provides active damping control. Note that active damping is enabled when AWD = 0, the default position for this bit.

The MR head can be biased with a programmable voltage in write mode depending on the state of the MRB serial port bit and the $\overline{MRB|AS}$/FAST pin. If MRB = 0, the MR bias is off. If MRB = 1, MR bias to the selected head is controlled by the state of the $\overline{MRB|AS}$/FAST pin. If $\overline{MRB|AS}$/FAST = 1, then the MR bias is disabled; if $\overline{MRB|AS}$/FAST = 0, then a voltage is applied to the selected head through the use of the HB3:HB0 serial port bits. See Figure 1. This feature provides a means to maintain the MR head voltage above ground potential during write operations. The MR bias voltage is given by:

$$V_{MR} = 30 \bullet N \quad \text{(mV), where N = 0..15 is the decimal value of HB3:HB0.}$$

SERVO BANK WRITE MODE

By setting the serial port register bit SBW high and placing the device in write mode, the chip goes into servo bank write mode. Heads activated in servo mode are selected by HS0, HS1, and HS2 bits, as shown in Tables 4 and 5. If there is no head connected to activated channels, the open head channels will be shut off in this mode. By setting SSD bit high, the open head shut off can be disabled. Exiting from servo write mode clears the shut off state. The 32R1615DR design allows write operation with VDD = 5.0V with slightly slower rise/fall time performance. This option is primarily intended to reduce device power dissipation in servo bank write mode. It is recommended that the chip operate in a well-controlled ambient temperature when servo write is active to prevent excessive junction temperatures. The thermal resistance of the package varies by mount conditions. The servo bank write function is disabled when the POK pin is low. See write mode section for a detailed description of the POK operation.

MR bias voltage of 120 mV is applied to all heads during servo bank write mode. The 4-channel and 8-channel devices respond differently when SBW bit is enabled. With SBW high, the 4-channel device will operate under normal single-head read mode conditions when pin R/$\overline{W}$ = 1, and will enter bank write mode when pin R/$\overline{W}$ = 0. The 4-channel device can amplify a read signal when R/$\overline{W}$ = 1 and then applies 120 mV MR bias to all heads when R/$\overline{W}$ transitions low.

On the 8-channel device, the preamp will enter bank write mode as soon as SBW = 1. With SBW = 1 and pin R/$\overline{W}$ = 1, the device will apply 120 mV to all activated read heads based on the servo head selection, but cannot amplify a read signal. With

SBW = 1 and R/$\overline{W}$ = 0, the 8-channel device will perform bank write, writing simultaneously to all

READ MODE

Taking the R/$\overline{W}$ pin high in non-idle mode selects read mode. MR bias for the selected head in read mode is controlled by the state of the MRB serial port bit in conjunction with the $\overline{MRB}$/$\overline{AS}$/FAST pin (see Figure 1). When MRB = 0, MR bias current is supplied to the selected head based on the value of serial port bits IR4:IR0, and the read path is activated (Read Active mode). When MRB = 1, MR bias is controlled by the state of the $\overline{MRB}$/$\overline{AS}$/FAST pin: $\overline{MRB}$/$\overline{AS}$/FAST = 0 enables MR bias current controlled by the IR4:IR0 bits and activates the read path (Read Active mode); $\overline{MRB}$/$\overline{AS}$/FAST = 1 enables MR bias voltage controlled by the state of the HB3:HB0 bits and the read path is disabled (Read Inactive mode).

To extend MR head life, the 32R1615DR is designed to switch between Read Inactive mode and Read Active through use of the MRB bit and $\overline{MRB}$/$\overline{AS}$/FAST pin. The MR bias will switch from voltage bias mode (Read Inactive) to current bias mode (Read Active). The 8-channel device includes timing modifications that delay and slow down the mode transitions to reduce effects of bias transients on the MR element.

In read active mode, the outputs of the read amplifier, RDX/RDY, are emitter followers and are in phase with the resistivity change at the selected input port (RnX/HGND) where the respective MR head is attached. The read mode gain is set to one of two values based on the GAIN bit of serial port Mode register.

In read active mode, the DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port, while the reference current is set by an external resistor from pin RREF to ground (Vref = 2.0 VDC). The magnitude of the

bias current is set according to the following equation:

$$Imr\ (mA) = 2.2 + 0.194*N$$

THERMAL ASPERITY DETECTION AND COMPENSATION

The Thermal Asperity circuitry can be controlled by the combination of TAC and TAD bits in TADC data register. The two bits control four combinations of thermal asperity handling, i.e. TA off, TA detection only, On-the-fly TA correction mode and Retry TA correction mode, as shown in Table 2. When the TA detector only mode is active (TAD = 1, TAC = 0), the FLT pin flags low when the chip detects the output exceeds the TA threshold setting.

heads activated based on the servo head selection, plus 120 mV will be supplied to all read heads.

where RREF = 2.0 KΩ and N = 0,1,...31 is the decimal value of serial port register bits IR0:IR4.

When switching from head to head, the chip selects an internal dummy head (15 ohm nominal) to discharge C1 capacitor so that the selected MR will see no current overshoot during the transition.

In read inactive mode, the bias voltage is given by:

$V_{MR} = 30 \bullet N$ (mV), where N = 0..15 is the decimal value of HB3:0.

MR RESISTANCE MEASUREMENT MODE

MR resistance measurement can be activated in read mode by setting MRM bit (D3) in the Mode register. With MRM = 1 (TAD = 0, DTM = 0), the BHV pin outputs the analog head voltage with gain of 5 V/V and the FLT/DBHV pin becomes the digital head voltage monitor output. The analog BHV output has an internal clamp circuit designed to keep the output voltage below 2.8 V at any MR head voltage. The DBHV threshold is programmed by TA/BHV data register. When the selected MR head voltage is lower than the set internal threshold voltage, the FLT pin flags a low. When the MR head voltage is higher than the set DBHV threshold, FLT flags high. The threshold voltage for the DBHV is programmable through the TA/BHV serial port register according to the following:

$$Vdbhv\ (mV) = 30 * N\ (nominal),$$

Where N = 0,1… 63 is the decimal value of serial port registers TB0:TB5

Note that the full DBHV threshold range overlaps the MR short and open head thresholds. Since the MR open/short detectors are not disabled during MR measurement mode, the user should restrict the DBHV threshold setting to voltages between the MR short and open thresholds (recommended range is 120 mV to 480 mV, 4< N< 16).

In On-the-fly TA correction mode (TAD = 1, TAC = 1), the signal pass band lower corner frequency is shifted up to 5 MHz when the TA threshold is exceeded. The TA correction stays on for 2 μsec after the TA event ends (Signal drops below TA threshold) and returns to normal operating mode by itself. The FLT output does not flag a TA event in On-the-fly mode.

The TA detection threshold is set by bits TB0:TB5 of the TA/BHV data register. The threshold value is same as the DBHV threshold voltage. The threshold level for the thermal asperity detector is programmable through the serial port according to the following:

Vta (mV) = 30 * N (nominal)

where RREF = 2.0 KΩ and N = 0,1...63 is the decimal value of serial port register bits TB0:TB5. Threshold level is referred to an averaged peak of the RDX output prior to the TA disturbance.

During Retry TA correction mode (TAD = 0, TAC = 1), the $\overline{\text{MRBIAS}}$/FAST pin controls the low corner frequency shift (FAST mode). When $\overline{\text{MRBIAS}}$/FAST = 1, the pass band lower corner frequency is shifted up to 5 MHz and remains there until the FAST mode is disabled by placing the $\overline{\text{MRBIAS}}$/FAST pin low. The FLT output does not flag a TA event in Retry mode.

TABLE 2: THERMAL ASPERITY MODES

TAD	TAC	Thermal Asperity Mode
0	0	Off
1	0	TA Detection only
0	1	Retry mode (low corner frequency shift) when MRBIAS/FAST = 1
1	1	On the Fly mode (low corner frequency shift when TA detected)

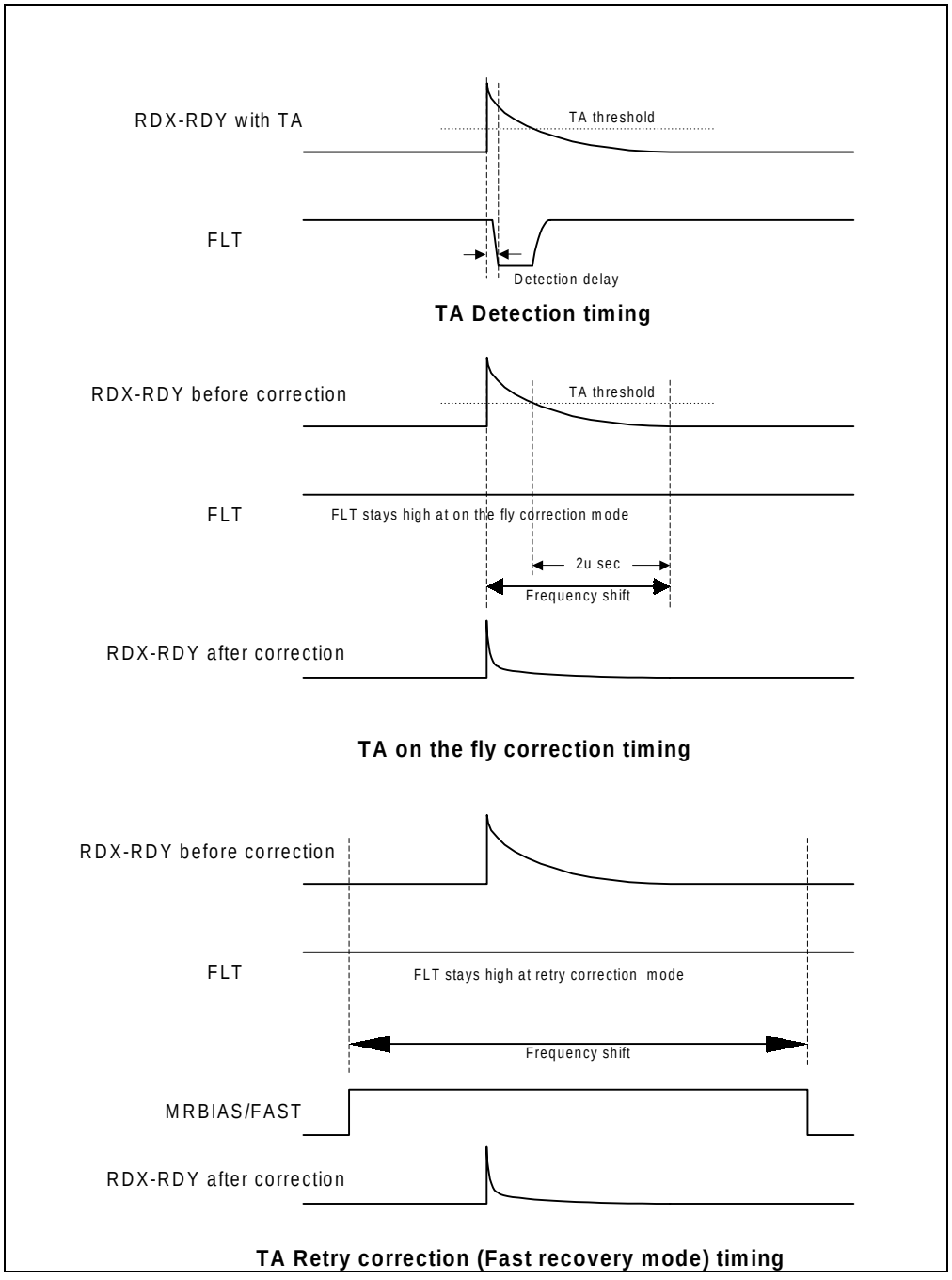


FIGURE 2: Thermal Asperity Modes

IDLE MODE

The $\overline{IDL}$ bit (D1) in Mode register of the serial port controls idle mode. The internal reference voltage and DACs are activated when $\overline{IDL}$ bit is set to low in non-sleep mode. All connections to the internal C1 capacitor are opened to preserve charge on the capacitor.

SLEEP MODE

The chip is set to sleep mode by setting $\overline{SLP}$ bit (D0 in Mode register) low. Only the serial port and voltage fault monitor is active in this mode. The $\overline{SLP}$ bit overrides all other mode control setting bits and pins. The FLT output remains low in sleep mode.

FAULT DETECTOR

The FLT pin is a 3-volt logic compatible output line, multiplexed between the DBHV and DTM output. When MR measurement and DTM modes are inactive (MRM = 0, DTM = 0), the pin is a fault status output. The FLT output is asserted when the chip is in a voltage fault condition, regardless of operating mode. The FLT output is a flag only and does not interrupt the chip function.

Read Mode

A low on the FLT pin indicates one of the following unsafe conditions:

- TA event detected in TA detection mode only (TAD =1,TAC=0).
- Open or shorted MR element.
- VCC supply voltage fault
- Invalid head select (i.e. HS2 = 1 on 4-channel device only)

Write Mode

The polarity of the FLT output in write mode is programmable. If FPS = 0, the FLT pin goes high when a write fault is detected. If FPS = 1, the FLT output goes low when a write fault is detected. FPS = 0 is default state.

A fault is asserted on the FLT pin under one of the following unsafe conditions:

- An open head. Does not respond to frequency above 10MHz to avoid false alarm
- Write data too slow.
- An open reference resistor.
- VCC or VDD supply voltage fault.
- Invalid head select (i.e. HS2 = 1 on 4-channel device only)

Servo Mode

A low on the FLT pin indicates the following unsafe condition:

- Chip temperature too high.
- VCC supply voltage fault.

Idle Mode

A low on the FLT pin indicates the following unsafe condition:

- VCC supply voltage fault.

Sleep Mode

- FLT stays low in sleep mode

VOLTAGE FAULT MONITOR

During power up or power fault condition, the voltage monitor disables the chip from any active mode. VCC fault monitor is active at any mode. The VDD fault monitor is active only in write mode to prevent false flag during servo bank write. The serial port has it's own power on reset circuit and serial data is cleared at VCC =1.6V nominal.

DIGITAL TEMPERATURE MONITOR

The digital temperature monitor is activated by setting MRM:TAD:DTM serial port bits to 0:0:1 in idle or read mode. An internal PTAT (proportional to absolute temperature) current is compared with a reference current set by the TA/BHV data register. The comparator output is monitored at the FLT output pin. To determine the chip temperature, the user increments the TA/BHV data register until the FLT output changes state. When the reference current is higher than the PTAT current, i.e. the set threshold temperature is higher than the chip temperature, the FLT pin flags low. The user can estimate the chip temperature based on the setting of the TA/BHV register when the FLT output changes state. One data bit corresponds to 2 °C.

An internal temperature monitor diode voltage can be monitored on the BHV pin when the digital

temperature monitor mode is activated. The chip provides an internally generated constant current to the temperature monitor diode.

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bank write, write current, MR head resistance measurement, MR bias current, read gain, PLR activation and timing, and thermal asperity threshold and mode. The serial port bit map is shown in Table 3.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/W bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0, and S2=0 for R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map).

Asserting the serial port enable line SDEN (TTL) initiates a transfer, SDATA (TTL) is clocked into the internal shift register by the rising edge of SCLK (TTL). A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

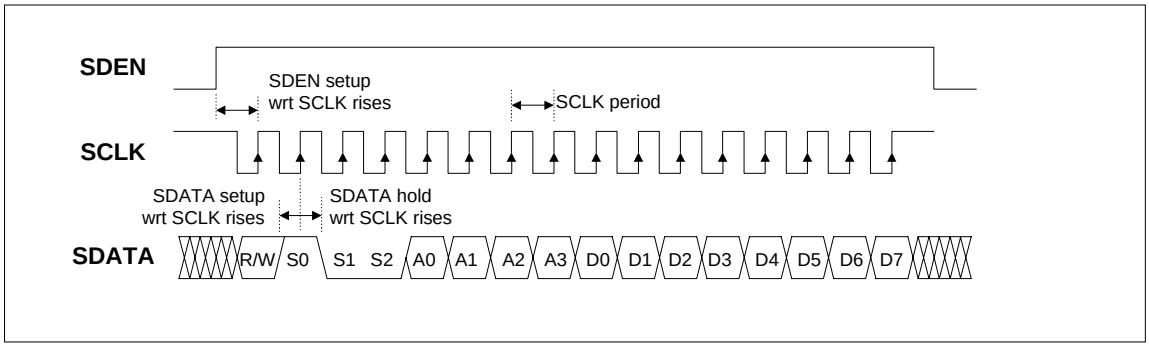


FIGURE 3: Serial Port Timing

TABLE 3: Serial Port Bit Map

Reg	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	VID = 1	VID = 0	PN0	PN1	PN2	REV0	REV1	REV2
HS/IMR	100	1000	HS0	HS1	HS2	IR0	IR1	IR2	IR3	IR4
Write	100	0100	IW0	IW1	IW2	IW3	IW4	AWD	WCB1	WCB2
TADC	100	1100	TAC	DR0	DR1	TAD	HB0	HB1	HB2	HB3
TA/BHV	100	0010	TB0	TB1	TB2	TB3	TB4	TB5	FPS	RES
Mode	100	1010	$\overline{SLP}$	$\overline{IDL}$	GAIN	MRM	RB	SBW	SSD	POKB
Fault	100	0110	FLT0	FLT1	FLT2	DTM	MRB	X	RES	RES
HFW	100	1110	X	X	X	X	X	X	X	X

ID register is read only.
All Data bits are set to 0 at power-up, except ID register.
X = Not Used
Res = Reserved for TI internal use. User setting = 0
Register 7 not included in 32R1615DR.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port Read/Write bit is not shown.

ID REGISTER (READ ONLY REGISTER)

Address = 0000 001

BIT	NAME	DESCRIPTION
7:5	REV2:REV0	Chip revision. 101 = 32R1615DR-8 100 = 32R1615DR-4
4:2	PN2:PN0	Product Number. 010 = 32R1615DR-8 (8-Channel device) 000 = 32R1615DR-4 (4-Channel device)
1:0	VID	Vender ID. 01 is given for TI SPG devices.

HS/IMR Register

Address = 0001 001

BIT	NAME	DESCRIPTION
7:3	IR4:IR0	MR bias current setting, see Read Mode description for bias equation. LSB = 0.2 mA 11111 = maximum MR bias current (8.2 mA) 00000 = minimum MR bias current (2.2 mA)
2:0	HS2:HS0	Head Select bits, see Table 4 and 5 for head select bit maps. Selection of HS2 valid only for 8-channel device. HS2 = 1 will cause Fault on 4-Channel device.

WRITE REGISTER

Address = 0010 001

BIT	NAME	DESCRIPTION
7:6	WCB2:WCB1	Write current boost. 11 = Maximum write current boost 00 = Minimum write current boost
5	AWD	Active write damping 1 = Active write damping disabled 0 = Active write damping enabled
4:0	IW4:IW0	Write current magnitude, see Write Mode description for equation. LSB = 1.45 mA 11111 = maximum write current (60 mA) 00000 = minimum write current (15 mA)

TA REGISTER

Address = 0011 001

BIT	NAME	DESCRIPTION
7:4	HB3:HB0	MR head protection bias voltage in read/write mode. LSB = 30 mV 1111 = Maximum head bias voltage (450 mV) 0000 = Minimum head bias voltage (off)
3	TAD	Thermal Asperity detector control 1 = Enable TA detector (when MRM = DTM = 0) 0 = Disable TA detector
2:1	DR1:DR0	Write damping resistor setting, 11 = Maximum damping 00 = Minimum damping
0	TAC	Thermal Asperity Correction enable when high. Correction on the fly. 1 = TAC 1 = TAD Correction retry mode. 1 = TAC 0 = TAD

TADET/DBHV REGISTER

Address = 0100 001

BIT	NAME	DESCRIPTION
7	X	Not Used
6	FPS	Write fault polarity 1 = Write fault indicated by FLT = low (No write faults: FLT = high) 0 = Write fault indicated by FLT = high (No write faults: FLT = low)
5:0	TB5:TB0	TA Detection threshold (TAD=1, MRM=0, DTM = 0) or Digital Buffered Head Voltage threshold (TAD=0, MRM=1, DTM = 0) or Digital Temperature Monitor reference (TAD = 0, MRM = 0, DTM = 1) Note: only one function can be selected for this DAC at a time. Simultaneous mode enables will disable DAC. LSB = 30 mV (TA or DBHV), = 2° C (DTM) 111111 = maximum threshold (TA or DBHV = 1890 mV) 000000 = minimum threshold (TA or DBHV = 0 mV)

MODE REGISTER

Address = 0101 001

BIT	NAME	DESCRIPTION
7	POKB	Power OK control bit (bi-directional). POKB low disables write mode. Both POKB and POK pin must be high for write mode activation. POKB will be set low by chip when POK pin transitions from high to low.
6	SSD	Servo mode open head shut down disable. When set high, open head self shut down circuit in servo write mode is disabled.
5	SBW	Servo Bank Write Mode enabled when high in write mode.
4	RB	Read frequency boost enabled when high.
3	MRM	MR Measurement Mode for analog BHV and digital BHV 1 = Enables MR measurement mode (TAD = 0, DTM = 0) 0 = Disables MR measurement mode
2	GAIN	Read Amplifier Gain select 1 = high gain mode 0 = low gain mode
1	$\overline{IDL}$	Idle Control Bit 0 = Idle mode enabled
0	$\overline{SLP}$	Sleep control bit 0 = Sleep mode enabled. Overrides all other control modes

FAULT REGISTER

Address = 0110 001

BIT	NAME	DESCRIPTION
7:6	RES	Reserved for TI internal use. User setting = 0
5	X	Not Used
4	MRB	MR Bias control pin. Used in conjunction with $\overline{MRBIAS}$/FAST pin to control MR head bias modes. See Table 1.
3	DTM	Digital temperature monitor enable 1 = Enable temperature monitor (MRM =TAD =0) 0 = Disable temperature monitor
2:0	FLT2:FLT0	Fault status registers. Not activated in 32R1615DR.

HFW REGISTER

Address = 0111 001

BIT	NAME	DESCRIPTION
7:0	RES	Reserved for future High Fly Write feature. Register is not active on 32R1615DR

TABLE 4: Head Selection, 8 Channel Version

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	0	none
0	0	1	1	1,3,5,7
0	1	0	2	0,2,4,6
0	1	1	3	all
1	0	0	4	none
1	0	1	5	none
1	1	0	6	none
1	1	1	7	none

TABLE 5: Head Selection, 4 Channel Version

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	0	none
0	0	1	1	1,3
0	1	0	2	0,2
0	1	1	3	All
1	X	X	Invalid (fault)	none

PIN DESCRIPTION

Name	Type	Description
RSET	I/O	External resistor connection to set reference current for current DACs.
MRBIAS/FAST	I	MRBIAS mode: MR bias current on: TTL, internal pull-down. Bias current active at low. FAST mode: TTL, internal pull down. FAST mode active at high.
WnX, WnY	O	Inductive write head connection.
RnX	I/O	MR read head connection, positive end.
HGND	I	MR head connection, negative end. Connect to system ground.
FLT/DBHV	O	Fault: A 3-volt logic compatible output. Fault mode: Read mode: A low indicates abnormal read condition. Write mode: A low (FPS = 1) or high (FPS = 0) indicates abnormal write condition. MR measure mode: DBHV comparator output. A high indicates the head voltage is higher than the set threshold. A low indicates the head voltage is lower than the set threshold. Servo write mode: A low indicates abnormal die temperature. Digital temperature monitor node: A low indicates the chip temperature is lower than the reference temperature.
POK	I	Power OK. A low disables write function. TTL with internal pull-up
BHV	O	MR measurement mode: Analog buffered head voltage monitor output with gain of 5. Temp monitor mode: Buffered temperature monitor diode output (2Vf)
R/W	I	Read/Write: TTL, with internal pull-up.
RDX,RDY	O	Differential Read Data output.
GND	I	Ground
VCC	-	+5V power supply.
VDD	-	+8V power supply for write driver.
SDEN	I	Serial Port Enable. TTL, with internal pull-down
SDATA	I/O	Serial Data. TTL., with internal pull-up
SCLK	I	Serial Clock. TTL, with internal pull-down.
WDX/WDY	I	Write Data input, PECL

ELECTRICAL SPECIFICATION

Unless otherwise specified, Rmr=50Ω Imr=5.10mA (setting value), RREF=2.00KΩ, Lwh=130nH, Rwh=10Ω, Iw=39.7mA (setting value).

ABSOLUTE MAXIMUM RATINGS

Operation beyond maximum ratings may result in permanent damage to the device.

PARAMETER		RATINGS
DC Supply Voltage	VCC	-0.3 to 6 VDC
DC Supply Voltage	VDD	-0.3 to 9 VDC
Logic Input Voltage	TTL	-0.3 to VCC + 0.3 VDC
	PECL	0 to VCC
Write Current	Iw	120 mA
MR Bias Current	I	20 mA
Write Head Voltage	V	-0.3V to VDD+0.3 V
Read Head Voltage	V	0 to 1.2 V
Output Current	RDX,Y	-10 mA
	FLT/DBHV	+8 mA
Storage Temperature	Tstg	-65 to 150 °C
Operating Junction Temperature	Tj	+135 °C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		RANGE
DC Supply Voltage	VCC	4.5 to 5.5 VDC
DC Supply Voltage	VDD_Write	7.2 to 8.8 VDC
	VDD_Servo	5.0 to 8.8 VDC
Write head load range	L	60 to 250 nH
Write head resister range	R	5 to 25 Ω
MR head range	R	35 to 80 Ω
Operating Ambient temperature	Ta	0 to 70 °C

POWER SUPPLY

Unless otherwise specified, Imr = 5.1 mA, Iw = 40 mA, Rmr = 50 Ω on all heads

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VDD Supply Current	I_{DD-R}	Read		0.25	1	mA
	I_{DD-W}	Write, Iw=40mA, IMRB off		56	72	mA
	I_{DD-S44}	32R1615DR-4 Servo 4channel, Iw=30mA		158	196	mA
	I_{DD-S4}	32R1615DR-8 Servo 4channel, Iw=30mA		158	196	mA
	I_{DD-S8}	32R1615DR-8 Servo 8channel, Iw=30mA		316	392	mA
	I_{DD-IL}	Idle		0	0.2	mA
	I_{DD-SP}	Sleep		0	0.2	mA
VCC Supply Current	I_{cc-R04}	Read IMR off, 1615D-4		25	34	mA
	I_{cc-R08}	Read IMR off, 1615D-8		17	24	mA
	I_{cc-R14}	Read IMR on, 1615D-4		48	67	mA
	I_{cc-R18}	Read IMR on, 1615D-8		40	55	mA
	I_{cc-W0}	Write, Iw=40mA, IMRB off		37	50	mA
	I_{cc-S44}	32R1615DR-4 Servo 4channel, Iw=30mA		68	88	mA
	I_{cc-S4}	32R1615DR-8 Servo 4channel, Iw=30mA		68	88	mA
	I_{cc-S8}	32R1615DR-8 Servo 8channel, Iw=30mA		92	120	mA
	I_{cc-IL4}	Idle, 32R1615DR-4		20	25	mA
	I_{cc-IL}	Idle, 32R1615DR-8		8	19	mA
	I_{cc-SP4}	Sleep, 32R1615DR-4		12	18	mA
	I_{cc-SP}	Sleep, 32R1615DR-8		2	8	mA
VCC Fault Voltage		Write mode Iw<0.2mA		3.75	4.2	V
VDD Fault Voltage		Write mode Iw<0.2mA		VCC-0.7	VCC	V
VCC Fault Voltage		Clears serial data		1.6		V

NOTE: Supply current equations, in mA, N = number of active channels in servo write mode.
Equations are for reference only; they are not verified as part of device testing.

IDD_W = 16 + Iw (nom), = 22 + (1.25 * Iw) (max)
IDD_Servo = (9.5 + Iw) * N (nom), = (11.5 + (1.25 * Iw)) * N (max)
ICC_W0 = 30 + (0.15 * Iw) + (0.21 * Imr) (nom), = 40 + (0.2 * Iw) + (0.3 * Imr) (max)
ICC_R14 = 36 + (1.21 * Imr) + (0.15 * Iw) (nom), = 50 + (1.8 * Imr) + (0.2 * Iw) (max)
ICC_R18 = 26 + (1.21 * Imr) + (0.15 * Iw) (nom), = 38 + (1.8 * Imr) + (0.2 * Iw) (max)
ICC_Servo = 40 + (4.5 * N) + (((2 + N)/20) * Iw) + (0.21 * Imr) (nom),
= 52 + (6 * N) + (((2 + N)/15) * IW) + (0.3 * IMR) (max)

CURRENT DAC REFERENCE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Voltage Reference	Vref		1.9	2.0	2.1	V
Reference R Range	Rref			2.0		KΩ
Reference Current	Iref	Rref=2k		1		mA

DIGITAL INPUT/OUTPUT

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R/W, MRBIAS, POK, SDATA SDEN, SCLK						
Input High Voltage	V_{IH1}	TTL	2.2		Vcc+.3	VDC
Input Low Voltage	V_{IL1}	TTL	-0.3		0.8	VDC
Input High Current	I_{IH1}	V =2.2V, R/W,POK SDATA, MRBIAS			160	µA
	I_{IH2}	V_{IH1} =2.2V, SDEN,SCLK		150		µA
Input Low Current	I_{IL1}	V_{IL1} =0.8V	-400			µA
WDX, WDY						
Input High Voltage	V_{IH3}	PECL	1.9		Vcc-0.9	VDC
Input Low Voltage	V_{IL3}	PECL	1.0		V_{IH3}-0.3	VDC
Input Δ Voltage			0.3	0.8	2.0	VDC
Input High Current	I_{IH3}	V_{IH3} =4.0V		4	5.5	µA
Input Low Current	I_{IL3}	V_{IL3} =3.2V	-5.5	-4		µA
WD termination	R_{WDin}		150	200	250	Ω
FLT						
Output High Voltage	V_{OH}	I_{OH} = 0 mA	2.4	2.7	3	V
Output Low Voltage	V_{OL}	I_{OL} =2mA			0.5	V
Pull-up resistor				2		KΩ
SDATA (readback)						
Output High Voltage	V_{OH2}	3V CMOS	2.4		3.0	V
Output Low Voltage	V_{OL2}				0.8	V

SERIAL PORT TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read/Write						
SCLK Clock Period	T_C	Write operation	25			ns
		Read operation	40			ns
SCLK Low Time	T_{CKL}		5			ns
SCLK High Time	T_{CKH}		5			ns
Enable to SCLK	T_{SENS}		10			ns
SCLK to Disable	T_{SENH}		10			ns
Data Set-up Time	T_{DS}		5			ns
Data Hold Time	T_{DH}		5			ns
SDEN min. Low Time	T_{SL}		25			ns
SCLK fall to data valid	T_{SDV}	Read operation			17	ns
SDATA hold tim	T_{SDH}	Read operation	20			ns
SDEN fall to SDATA tristate	T_{SDTRI}	Read operation			20	ns

READ CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		35	50	80	Ω
MR Bias Current Nominal Range		2.2		8.2	mA
MR Bias Current Resolution			5		bit
LSB			194		μA
MR Current Tolerance	N ≤ 2	-10		+10	%
	N ≥ 3	-8		+8	%
MR Head DC Voltage Range		0.1		0.64	V
Unselected Head Current				10	μA
Input Resistance (RIN)			5		Ω
Differential Voltage Gain	R_{MR} = 50Ω, Low Gain	127	150	180	V/V
	R_{MR} = 50Ω, High Gain	170	220	255	V/V
Read Gain Constant	Av*(RMR+RIN), Low Gain		8000		Ω
	Av*(RMR+RIN), High Gain		12000		Ω
Bandwidth	Lower -3dB		0.65	1	MHz
(Nom: Rmr = 50 Ω, Lh=40nH	Higher -1dB, RB = 0	100	150		MHz
Worst: Rmr = 35 Ω, Lh=40nH)	Higher -3dB, RB = 0	150	200		MHz
	Higher -1dB, RB = 1	145	200		MHz
	Higher -3dB, RB = 1	175	250		MHz
Input Noise (Excludes RMR,	R_{MR} = 35Ω		0.75		nV/√Hz
includes current noise)	R_{MR} = 50Ω		1.00		nV/√Hz
Dynamic Range	Gain falls to 90%	2			mV
Output Offset Voltage		-100		100	mV
Output Current		2.5			mA
Output Voltage		1.0		3.0	V
Output Resistance	Single-ended		50		Ω
PSRR	@ 5MHz	45	60		dB
	@ 20 MHz		45		dB
Channel Separation	@5 MHz	45	60		dB
	@ 20 MHz		45		dB

SECONDARY MR BIAS VOLTAGE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR head voltage bias range		0		0.45	V
Resolution			4		bit
LSB	Rmr = 50 Ω		30		mV
Absolute tolerance	Rmr = 50 Ω	-25		25	%

WRITE/SERVO CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Nominal Range		15.75		60.7	mA
Write Current Resolution			5		bit
LSB			1.45		mA
Write Current Accuracy	N ≤ 4	-10		+10	%
	N ≥ 5	-8		+8	%
Maximum Write Current, Servo Mode	4-heads, Vdd = 5 VDC	42			mA
	8-heads, 5 V < Vdd < 6 V	26			mA
	8-heads, 6 V < Vdd < 7 V	34			mA
	8-heads, 7 V < Vdd < 8.8 V	40			mA
Head Voltage Swing	Open Head, Vdd = 8 VDC		6.5		Vpp
	Transient, Vdd = 8 VDC		7.5		Vpp
	Open Head, Vdd = 5 VDC		3.5		Vpp
	Transient, Vdd = 5 VDC		4.0		Vpp
Damping Resistor	<DR0,DR1>=<0,0>	0.808	1	1.19	kΩ
	<DR0,DR1>=<1,0>	363	450	536	Ω
	<DR0,DR1>=<0,1>	202	250	298	Ω
	<DR0,DR1>=<1,1>	121	150	178	Ω
Unselected Head Current	DC			100	μA
	Transient			1	mApk
Write Current Matching	Servo mode, channel to channel variation from mean			10	%

HEAD VOLTAGE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DBHV threshold resolution			6		bit
DBHV minimum threshold			0		mV
LSB			30		mV
DBHV threshold accuracy	DAC setting = 4 to 16, after offset compensation	-8		+8	%
BHV gain		4.7	5	5.3	V/V
BHV output range		0.4		2.4	V
BHV output current	Output drops to 90%	0.5			mA
BHV output offset		-100		100	mV
BHV output clamp voltage	Vin = 0.48 - 0.75 V		2.4	2.8	V
MR head short detect threshold			50	75	mV
MR head open detect threshold		750	825		mV

THERMAL ASPERITY DETECTION/CORRECTION/FAST RECOVERY

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TA Detection Resolution			6		bit
TA Detection Minimum threshold	Relative to RDX output peak prior to correction.		0		mV
TA Detection Threshold, Nominal Range	Relative to RDX output peak prior to correction.	0		1890	mV
TA Threshold LSB	Ref=2kΩ	22.5	30	37.5	mV
Lower Corner Frequency	TAC = 1		5		MHz
TA Detection Delay	TAD = 1		30	100	ns
TA correction delay	TAC:TAD = 11		0.4	1.0	µs
TA correction timer	TAC:TAD = 11		2		µs

SWITCHING CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write to Read Switching	90% signal envelope, ±30mV DC		0.4	0.81	µs
Read to Write Switching	90% of Iw		25	50	ns
	90% of Iw, Servo write			70	ns
Read, MR bias off to on	90% signal envelope, ±30mV DC		0.6		µs
Idle to Read Switching	90% signal envelope, ±30mV DC		1	1.26	µs
Read to Idle Switching	10% of read envelope			0.6	µs
Head Switching	90% signal envelope, ±30mV DC		1	10	µs
Iw rise/fall time 10% to 90%	Lh=130nH, Iw=40mA, Vdd=8V		1.3	1.75	ns
	Lh=130nH, Iw=30mA, Vdd=5V		2.0		ns
Head Current Delay TD3	50% of WD to 50% of Iw			30	ns
Write Current Asymmetry	Propagation delay difference 50% duty cycle write data			0.5	ns
Minimum write data pulse width	Pulse width error within +/- 20% of write data input. 1T/10T pattern with shorted head		2.0	2.85	ns

WRITE UNSAFE DETECTION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FLT safe to unsafe TD1	Low Frequency Write Data	0.5	1	2	µs
FLT unsafe to safe TD2				200	ns
Write data frequency	Valid transient detector			160	MHz
	Valid Open detector			10	MHz

OVER TEMPERATURE DETECTION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Over temperature detection threshold	Servo Mode, FLT = low		135		°C

TEMPERATURE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Digital temperature monitor					
Resolution			6		bit
LSB			2		°C
Temperature range		0		126	°C
Temp diode voltage	Ta = 25 C		TBD		V

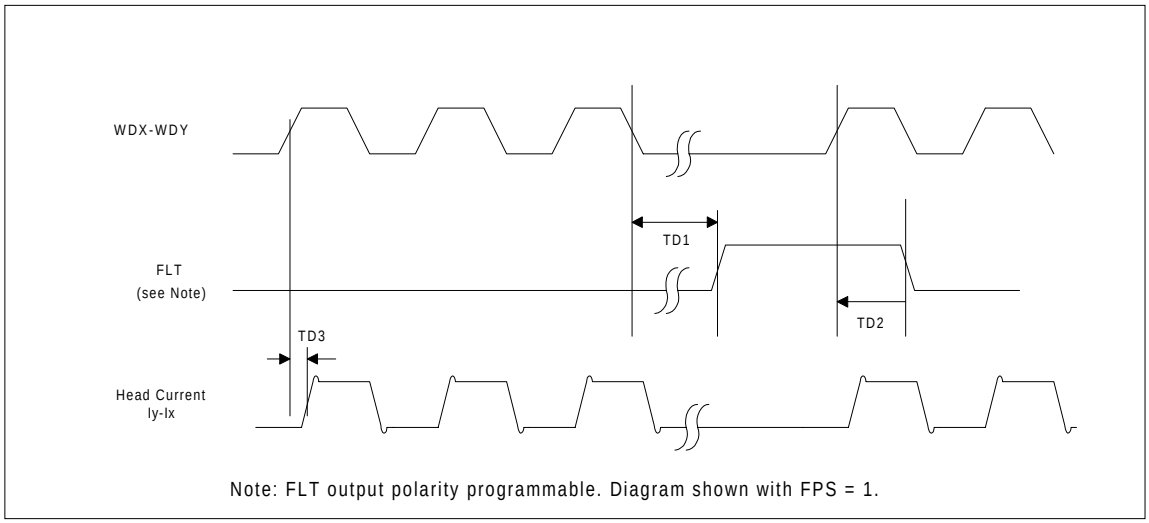
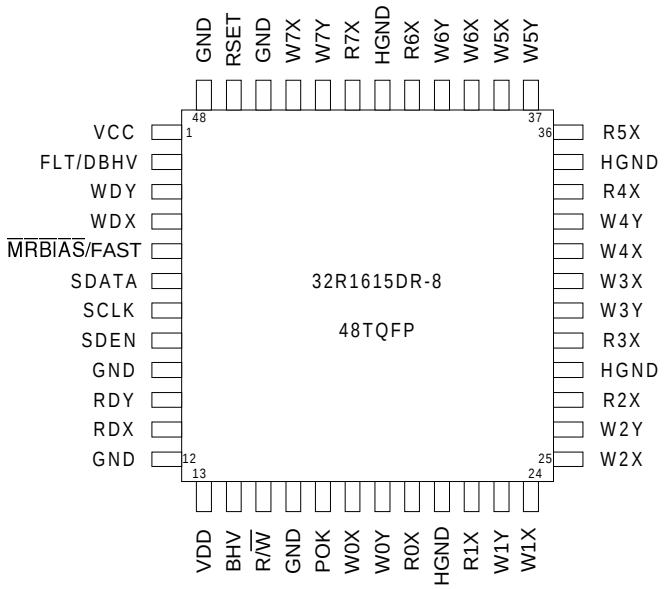
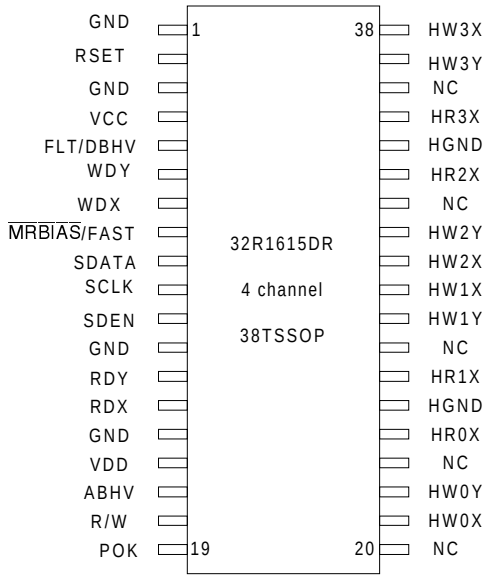


FIGURE 4: Write Current & Head Unsafe Timing

PACKAGE PIN DESIGNATIONS





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SR1621AAA
+5, 4-CHANNEL MR READ/WRITE DEVICE

Prototype

June, 2000

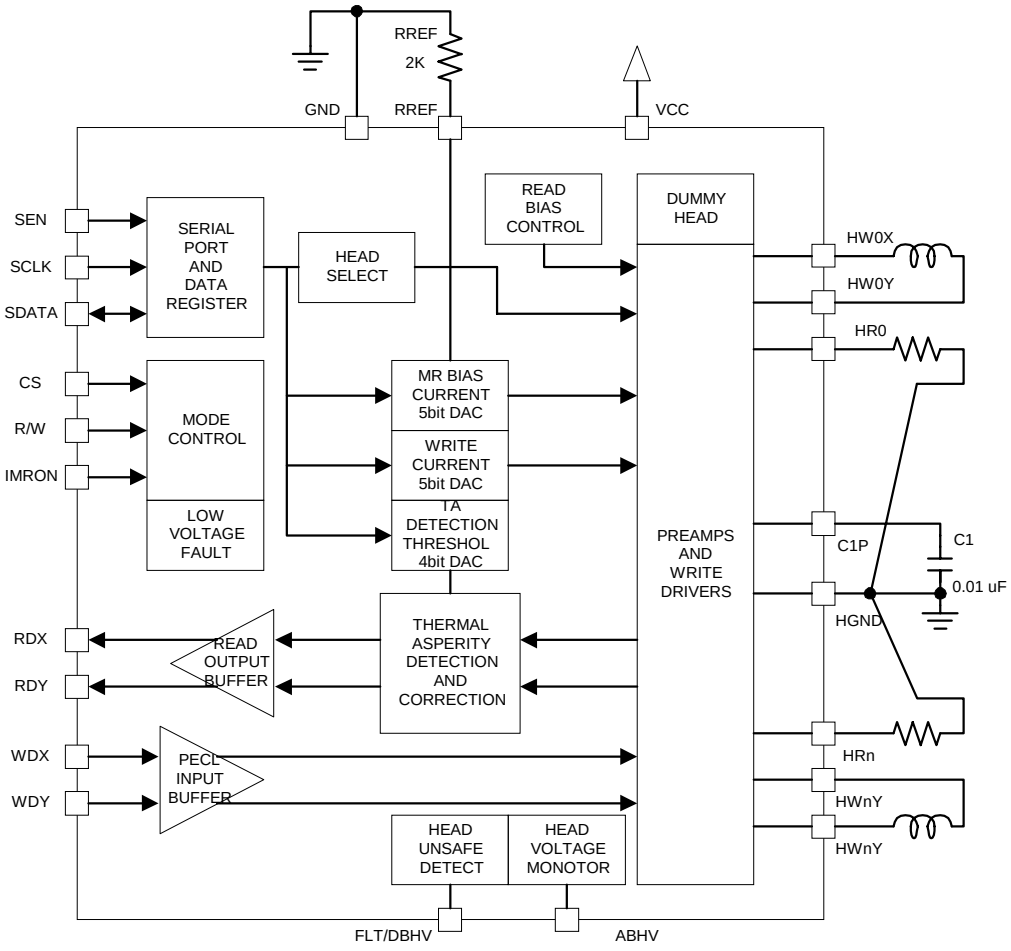
DESCRIPTION

The SR1621AAA is a BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive read and thin film write composite recording heads. It provides a low noise MR head amplifier, MR bias current control, thin film write driver, write current control, thermal asperity detection and correction, and TFH fault detection circuit for up to four channels. The device features programmable read gain, write damping resistance and thermal asperity threshold level. The device allows multiple channel write functions for servo writing. Half or all of the heads can be simultaneously selected in the servo write mode. Control of features and thresholds is provided through a serial port interface. The SR1621AAA requires a single 5V supply.

FEATURES

- **One side grounded input, fully differential output**
- **Unselected Read/Write heads at GND potential**
- **Thermal asperity detection and compensation**
- **Fast recovery mode**
- **MR resistor measurement mode**
- **MR bias current range = 2.0 to 11mA (5 bit)**
- **MR resistor range =46 to 86Ω**
- **Programmable read gain =200V/V and 250V/V @66Ω 7.23 mA**
- **Input equivalent noise 1.0 nV/√Hz @66Ω (1 to 50 MHz)**
- **DBHV lower threshold = 280mV, upper threshold = 480mV**
- **Write current rise/fall time 1.6nS (Lh=130nH, Rh=16Ω, Iw=30.8mA)**
- **Write current range = 15 to 50 mA (5 bit)**
- **Programmable write damping resistor (2 bit)**
- **WD PECL no flip-flop, 3V compatible**
- **Rail to rail head swing**
- **Servo write (Half bank, all bank write)**
- **Power fault protection**
- **Temperature monitor output**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SR1621AAA addresses four terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with TTL pins $\overline{CS}$, R/$\overline{W}$, $\overline{IMRON}$ and the serial port as shown in the Table 1. The $\overline{CS}$, R/$\overline{W}$ and $\overline{IMRON}$ inputs have internal pull-up resistors so that when left opened, they will default to the TTL High state.

The serial port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold level and mode.

WRITE MODE

Taking R/$\overline{W}$ low in non-idle mode selects write mode. Write current is enabled to the selected channel and write data (WDX/WDY) controls the write current polarity. Head current is toggled between the X and Y side of the selected head on each transition of the differential PECL signal WDX-WDY. When WDX is higher than WDY, the current flows from X (HWnX) to Y (HWnY), (i.e., the X side of the head voltage is higher than the Y side).

Write current magnitude is controlled by a five-bit on board DAC. The DAC is programmed via the serial port. The magnitude of the write current (0-pk) is given by:

$$Iw\ (mA) = 15 + \frac{35}{31} \bullet N$$

where RREF = 2.0 KΩ and N = 0,1 ... 31 is the decimal value of serial port register bits IW0:IW4.

Note that the actual head current Ix,y is given by:

$$Ix,y\ (mA) = \frac{Iw}{1 + \frac{Rh}{Rd}}$$

where Rh is the head DC resistance and Rd is the damping resistor.

SERVO BANK WRITE MODE

By setting both serial port register bits BNK0 and BNK1 high when in write mode, the chip goes into servo write mode. Heads activated in servo mode can be selected by HS0, HS1 bits, as shown in Table 3. Bit HS0 controls the upper half channels, and HS1 controls the lower half channels. Setting both HS0 = HS1 = 1 selects all heads. It is recommended that the chip operate in a well controlled ambient temperature when servo write is active to prevent excessive junction temperatures. The thermal resistance of the package varies by mount conditions.

TABLE 1: Mode Selection.

$\overline{SLP}$ (Mode Reg)	$\overline{IDL}$ (Mode Reg)	R/$\overline{W}$	$\overline{IMRON}$	BNK0*BNK1 (Write/Mode Reg)	MODE
0	X	X	X	X	Sleep
1	0	X	1	X	Idle, IMR off
1	0	X	0	X	Idle, IMR on
1	1	1	1	X	Read, IMR off
1	1	1	0	X	Read, IMR on
1	1	0	1	0	Write, IMR off
1	1	0	0	0	Write, IMR on
1	1	0	1	1	Servo Write, IMR off

NOTES: Optional CS input pin is logically OR'd with IDL bit to set Idle mode:
Either CS = 1 OR IDL = 0 sets chip to Idle mode. CS = 0 AND IDL =1 for non idle modes.

READ MODE

Taking the R/$\overline{W}$ pin high in non-idle mode selects read mode, which activates the MR bias current generator and low noise differential amplifier. $\overline{IMRON}$ must be low to activate the MR bias current through the designated head. When $\overline{IMRON}$ is high, MR current is disabled, but C1P capacitor voltage is retained to improve recovery time. The outputs of the read amplifier RDX/RDY are emitter followers and are in phase with the resistivity change at the selected input port (HRn) where the respective MR head is attached. The read mode gain is set to one of two values based on the GAIN bit of serial port Mode register.

The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port, while the reference current is set by an external resistor from pin RREF to ground (Vref = 2.0 VDC). The magnitude of the bias current is set according to the following equation:

$$\text{Imr (mA)} = 2.0 + \frac{9.3}{31} \bullet N$$

where RREF = 2.0 KΩ and N = 0,1,...31 is the decimal value of serial port register bits IR0:IR4.

In read mode, the device requires one external capacitor. Capacitor C1, connected between C1P and HGND is the bias loop control capacitor. The value of C1 will effect the lower frequency corner of the read amplifier.

Application Note: Read Open Head Detection

The SR1621AAA includes circuitry to report the read faults listed in the fault detector section but does not report a true open head as a fault as originally intended. The open head detector operates by monitoring the MR head voltage on the selected head , and will report a fault when the head voltage exceeds the open head threshold (970 mV). However, if the head voltage exceeds approximately 1.35 V, the fault reporting is disabled. Under a true open-circuit condition, the MR bias loop will drive the head voltage above 1.35 V and the open head fault is disabled. A recommended workaround to check for open head conditions is to utilize the MR Measurement mode, as an open head will never produce a head voltage that falls within the DBHV threshold window.

FAST WRITE TO READ RECOVERY MODE

The FWR bit of the Mode Register enables the fast write to read recovery mode. In this mode, the lower corner of the read amplifier is shifted from 0.6Mhz (typical) to 3.5 MHz (nominal), with C1=0.01uF, upon assertion of the R/$\overline{W}$ signal. The lower corner is held at 3.5 MHz for 900 nsec. The corner frequency shift in this mode eliminates the low frequency content of the transient read signal, thus improving the write to read recovery time.

IDLE MODE

$\overline{IDL}$ bit (D1) in Mode register of the serial port controls idle mode. The internal reference voltage and DACs are activated when $\overline{IDL}$ bit is set to low in non-sleep mode. MR bias current can be activated by $\overline{IMRON}$ pin to allow quick recovery to read mode or disabled to get lower power consumption. When IMRON is set active (low), MR bias current is diverted to the internal dummy head. Idle mode can be controlled by either $\overline{IDL}$ bit or $\overline{CS}$ pin. Both $\overline{IDL}$ = 1 and $\overline{CS}$ = 0 are required to place the chip into active mode.

SLEEP MODE

The chip is set to sleep mode by setting $\overline{SLP}$ bit (D0 in Mode register). Only the serial port and voltage fault monitor are active in this mode. The $\overline{SLP}$ bit overrides all other mode control setting bits and pins.

FAULT OPERATION

The FLT/DBHV pin is an open collector output line, multiplexed between two functions. When MR measurement mode is inactive, the output is a fault status output and has the following polarity. The FLT output flags low when the chip is in a voltage fault condition, regardless of operating mode.

Read Mode

A low on the FLT pin indicates one of the following unsafe conditions:

- Device in TA fast recovery mode (triggered by TA event).
- TA event detected, if enabled. (programmable threshold).
- Read head input short to GND
- Low Vcc
- Head voltage between MR open threshold and 1.35 V (see open head note under read mode)

Write Mode

A high on the FLT pin indicates one of the following unsafe conditions:

- An open head, valid up 10 MHz.
- Head shorted to ground
- Write data too slow.
- An open reference resistor.
- Low Vcc (reported). The writer is disabled for the duration of the fault condition.

SERVO BANKWRITE MODE

A high on the FLT pin indicates the following unsafe condition:

- Low Vcc (reported). The writer is disabled for the duration of the fault condition.

THERMAL ASPERITY DETECTION AND COMPENSATION

The thermal asperity circuitry can be controlled by serial port bits FRON and TADet, and the thermal asperity threshold setting (TA3:TA0). The thermal asperity can be set to one of 4 modes: TA off, TA detection only, TA Fast Recovery (retry mode), and TA correction triggered by TA detect (on-the-fly-correction). See Table 2 for Thermal Asperity mode settings.

In TA detection only mode, the FLT pin will indicate a TA event when the signal crosses the TA threshold voltage. The threshold is programmable through use of the TA3:TA0 serial port bits (see threshold equation below). The FLT output will indicate the TA fault for as long as the signal remains above the TA threshold plus some hysteresis.

In TA Fast Recovery mode, the lower corner frequency of read amplifier is shift up to 3.5 MHz (nom) to eliminate low frequency component from the read signal. This mode can be entered by activating the FRON bit with TA detection disabled. The TA fast recovery mode is used primarily for read retry.

In the TA on-the-fly correction mode, the chip detects the peak voltage of the thermal asperity and subtracts the peak from the read output (called TA compensation). In addition, the lower corner frequency is shifted to 3.5 MHz as in Fast Recovery mode. The amplifier returns to its normal operating state 5 μsec after the uncompensated signal has returned below the TA threshold voltage plus some hysteresis. The FLT pin flags low during the correction period.

The threshold level for the thermal asperity detector is programmable through the serial port according to the following:

$$Vta\ (mV) = 50 + 50 * N$$

where RREF = 2.0 KΩ and N = 0,1...15 is the decimal value of serial port register bits TA0:TA3. Threshold level is referred to output level.

TABLE 2: Thermal Asperity Mode Control

			TA mode	
/FR	**FRon**	**TAdet**	**Fast Recovery**	**TA detection**
0	X	0	On	Off
0	X	1	On	On
1	0	0	Off	Off
1	0	1	Off	On
1	1	0	On	Off
1	1	1	On by TA trigger	On

/FR in pulled high internally for 4 channel version. No /FR pin on 30VT packaged part.

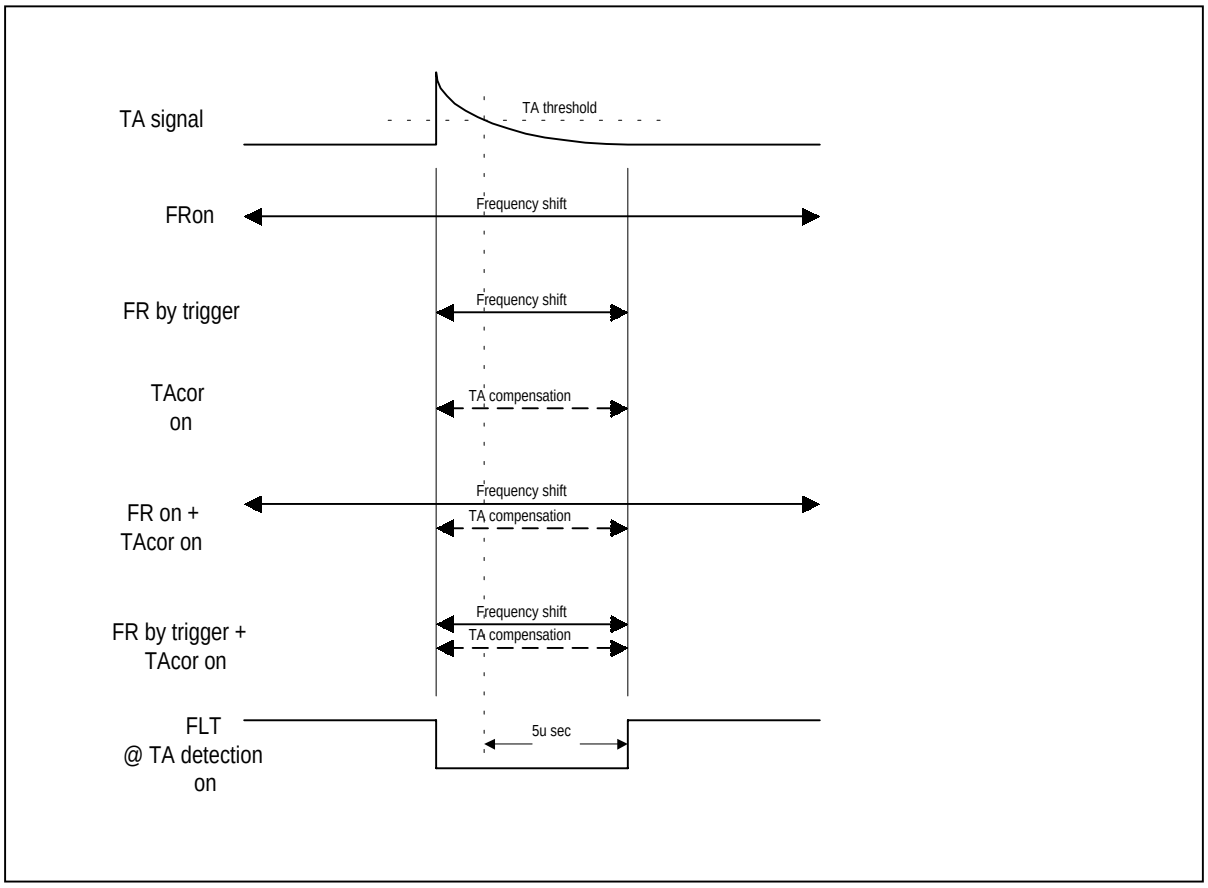


FIGURE 1: Thermal Asperity Modes

MR RESISTANCE MEASUREMENT/ TEMPERATURE MONITOR MODE

MR resistance measurement can be activated in read mode by setting MRM bit (D3) in the Mode register. The ABHV and DBHV outputs are activated in this mode. The ABHV output is a buffered MR head voltage with gain of 5V/V. The DBHV/FLT pin is a logic output: when the head voltage stays inside of set window, it flags high.

When MRM bit is low, ABHV acts as a die temperature monitor (except in sleep mode) according to the following equation:

ABHV(volts) = (temp/100 + 1)*(VCC/5)

Temp = degrees C

VOLTAGE FAULT MONITOR

During power up or power fault condition, the power-on voltage fault monitor disables the chip from any active mode. The serial data registers are reset to power-on setting values and the preamp enters sleep mode. The threshold voltage for the serial port power-on reset is 1.8V (typical). The threshold voltage for Vcc fault, which also disables the write mode but does not reset the serial data registers, is 3.9V/3.75V (typical, with hysteresis).

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold and mode. The serial port bit map is shown in Table 3.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/W bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0, and S2=0 for R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map).

Asserting the serial port enable line SDEN (TTL) initiates a transfer, SDATA (TTL) is clocked into the internal shift register by the rising edge of SCLK (TTL). A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

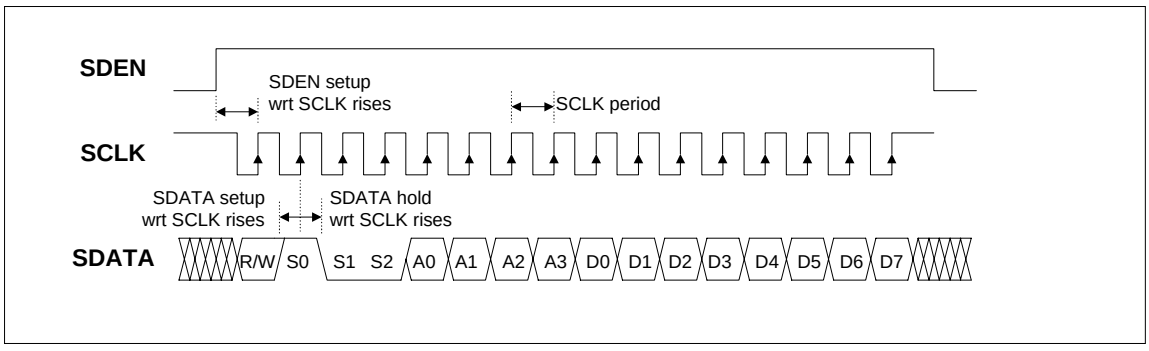


FIGURE 2: Serial Port Timing

TABLE 3: Serial Port Bit Map

Reg	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	1	0	0	VS0	VS1	VS2	CH	0
HS/IMR	100	1000	HS0	HS1	0	IMR0	IMR1	IMR2	IMR3	IMR4
WRITE	100	0100	IW0	IW1	IW2	IW3	IW4	WCB1	WCB0	BNK0
TA	100	1100	0	DR0	DR1	TADET	TA0	TA1	TA2	TA3
MODE	100	0010	$\overline{SLP}$	$\overline{IDL}$	GAIN	MRM	0	FRON	BNK1	FWR

ID register is read only.
All Data bits are set to 0 by at reset condition, i.e. power-up or voltage fault condition, except ID register.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port Read/Write bit is not shown.

ID Register (Read Only Register)
Address = 0000 001

BIT	NAME	DESCRIPTION
7		ID bit = 1, internally set by TI SPG
6	CH	Channel version 1 = 4 channel version
5:3	VS2:VS0	Device revision bits. (000 for 5050-6-1)
2:0		ID bits = 001, internally set by TI SPG

HS/IMR Register
Address = 0001 001

BIT	NAME	DESCRIPTION
7:3	IMR4:0	MR bias current setting, see Read Mode description for bias equation 11111 = maximum MR bias current 00000 = minimum MR bias current
2	Not Used	User setting = 0
1:0	HS1:HS0	Head Select bits, see Table 3 for head select bit maps

Write Register
Address = 0010 001

BIT	NAME	DESCRIPTION
7	BNK0	Servo Bank control bit, operate in conjunction with BNK1 in Mode Register 1 = Servo Bank mode (both BNK0 and BNK1 must be 1 to enable Servo) 0 = Servo Bank mode off
6:5	WCB1:0	Write Current Boost 00 = minimum write current boost 11 = maximum write current boost
4:0	IW4:0	Write current magnitude, see Write Mode description for equation 11111 = maximum write current 00000 = minimum write current

TA Register
Address = 0011 001

BIT	NAME	DESCRIPTION
7:4	TA3:0	Thermal Asperity Threshold. See Thermal Asperity Description for equation 1111 = maximum TA threshold setting 0000 = minimum TA threshold setting
3	TADET	Thermal Asperity detector control 1 = Enable TA detector 0 = Disable TA detector
2:1	DR1:0	Write damping resistor setting, 11 = 110 Ω 10 = 150 Ω 01 = 240 Ω 00 = 600 Ω
0	Res	Reserved for SSI internal use User setting = 0

Mode Register
Address = 0100 001

BIT	NAME	DESCRIPTION
7	FWR	Fast write to read enable 1 = Fast write to read enabled 0 = Fast write to read disabled
6	BNK1	Servo Bank control bit, operate in conjunction with BNK0 in Write Register 1 = Servo Bank mode (both BNK0 and BNK1 must be 1 to enable Servo) 0 = Servo Bank mode off
5	FRON	Fast Recovery Mode Enable 1 = Fast recovery mode enabled (low corner frequency shift) 0 = Fast recovery mode disabled
4	Res	User setting = 0
3	MRM	MR Measurement Mode 1 = Enables MR measurement mode. Activates digital and analog BHV 0 = Disables MR measurement mode
2	GAIN	Read Amplifier Gain select 1 = 250 V/V 0 = 200 V/V
1	$\overline{IDL}$	Idle Control Bit 0 = Idle mode enabled
0	$\overline{SLP}$	Sleep control bit 0 = Sleep mode enabled. Overrides all other control modes

TABLE 3: Head Selection, 4 Channel Version

HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	X
0	1	1	2,3
1	0	2	0,1
1	1	3	All heads

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RREF	I/O	External resistor connection to set reference current for current DACs.
HWnX, HWnY	O	Inductive write head connection.
HRn	I/O	MR read head connection.
HGND	I/O	MR read head current return.
FLT/DBHV	O	Fault / Digital Buffered Head Voltage. An open collector output. Fault mode: Read mode: A low indicates abnormal read condition. Write mode: A high indicates abnormal write condition. MR measure mode: A high indicates the head is in proper range.
ABHV	O	Analog buffered head voltage/temperature monitor output.
R/$\overline{W}$	I	Read/Write: TTL, with internal pull-up.
RDX,RDY	O	Differential Read Data output.
$\overline{CS}$	I	Chip Select. Active low with internal pull-up.
GND	I	Ground
VCC	I	+5V power Supply.
C1P	I	Bias loop control capacitor connected to HGND.
$\overline{IMRON}$	I	MR Current on: Activates MR bias in write mode. TTL, with internal pull-up.
SDEN	I	Serial Port Enable. TTL, with internal pull-down.
SDATA	I/O	Serial Data. TTL, with internal pull-down.
SCLK	I	Serial Clock. TTL, with internal pull-down.
WDX,WDY	I	Differential PECL write data inputs

ELECTRICAL SPECIFICATION

Unless otherwise specified, Rmr=66Ω Imr=7.23 mA, Rref=2.0KΩ, C1=0.01μF, Lhw=130nH, Rhw=16Ω, Iw=30.8 mA, Vcc = 5.0 V.

Absolute Maximum Ratings
Operation beyond maximum ratings may result in permanent damage to the device.

PARAMETER		RATINGS
DC Supply Voltage	VCC	-0.3 to 6 VDC
Logic Input Voltage	TTL	-0.3 to VCC + 0.3 VDC
	PECL	0 to VCC
Write Current	Iw	70 mA
MR Bias Current	I	30 mA
Write Head Voltage	V	-0.3V to Vcc+0.3 V
Read Head Voltage	V	0 to 0.6 V
Output Current	RDX,Y	-10 mA
	FLT/DBHV	+8 mA
Storage Temperature	Tstg	-65 to 150 °C
Operating Junction Temperature	Tj	+135 °C

Recommended Operation Conditions

PARAMETER		RANGE
DC Supply Voltage	VCC	4.5 to 5.5 VDC
Write head load range	L	60 to 250 nH
Write head resister range	R	5 to 25 Ω
MR head range	R	46to 86 Ω
Operating Ambient temperature	Ta	0 to 70 °C

DC Characteristics

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	VCC	Read IMR off		10	15	mA
		Read IMR on, Imr = 7.23 mA		35	50	mA
		Write IMR off, Iw = 30.8 mA		57	80	mA
		Write IMR on, Iw = 30.8 mA Imr = 7.23 mA		66	94	mA
		Servo (2 channel), Iw=24.03mA, Vcc = 4.5 V		75	90	mA
		Servo (4 channel), Iw=24.03mA, Vcc = 4.5 V		135	165	mA
		Servo (8 channel), Iw=24.03mA, Vcc = 4.5 V		255	300	mA
		Idle IMR off		8	12	mA
		Idle IMR on, Imr = 7.23 mA		27	40	mA
		Sleep		0.6	2	mA
VCC Fault Voltage		Fault detected	3.55	3.75	3.95	V
		Fault removed	3.7	3.9	4.1	V
POR VCC Voltage		Reset removed		1.8	2.0	V

Digital Input/Output

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input High Voltage	V_{IH1}	TTL	2.0			VDC
Input Low Voltage	V_{IL1}	TTL			0.8	VDC
Input High Current	I_{IH1}	V_{IH1} =2.0V			160	µA
Input Low Current	I_{IL1}	V_{IL1} =0.8V	-400			µA
Input High Voltage	V_{IH3}	PECL	2.0		Vcc-0.6	VDC
Input Low Voltage	V_{IL3}	PECL	1.2		V_{IH3}-0.2	VDC
Input Δ Voltage			0.2	0.6	1.8	VDC
Input High Current	I_{IH3}	V_{IH3} =4.0V		5	100	µA
Input Low Current	I_{IL3}	V_{IL3} =3.2V		5	100	µA
Output High Current	I_{OH}	FLT/DBHV V_{OH} =VCC			20	µA
Output Low Voltage	V_{OL}	FLT/DBHV I_{OL} =2mA			0.5	V

Serial Port Timing, Read/Write

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		50			nS
SCLK Low Time	T_{CKL}		30			nS
SCLK High Time	T_{CKH}		30			nS
Enable to SCLK	T_{SENS}		10			nS
SCLK to Disable	T_{SENH}		40			nS
Data Set-up Time	T_{DS}		5			nS
Data Hold Time	T_{DH}		5			nS
SDEN min. Low Time	T_{SL}		160			nS

Serial Port Timing, Write Only

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		50			nS
SCLK Low Time	T_{CKL}					nS
SCLK High Time	T_{CKH}					nS
Enable to SCLK	T_{SENS}					nS
SCLK to Disable	T_{SENH}					nS
Data Set-up Time	T_{DS}					nS
Data Hold Time	T_{DH}					nS
SDEN min. Low Time	T_{SL}					nS

Current DAC Reference

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Voltage Reference	Vref		1.9	2.0	2.1	V
Reference R Range	Rref			2.0		KΩ
Reference Current	Iref			1		mA

Read Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		46	66	86	Ω
MR Bias Current		2.0		11	mA
MR Bias Current Resolution			5		bit
LSB	Rref = 2 KΩ		290		μA
MR Current Tolerance		-6		+6	%
MR Head DC Voltage Range				0.7	V
Unselected Head Current				10	μA
Input Resistance	Rmr = 66 Ω, Imr = 7.23 mA		5		Ω
Differential Voltage Gain	R_{MR} = 66Ω, Imr = 7.23 mA 1 mV p-p @ 10 MHz GAIN = 0 GAIN = 1	 170 212	 200 250	 230 288	 V/V V/V
Read Gain Constant	Av*(RMR+RIN) GAIN = 0 GAIN = 1		 14200 17750		 Ω Ω
Bandwidth	Lower -3dB, C1 = 0.01 μF Lower -3dB, Fast recovery Higher -1dB Higher -3dB, Rmr = 66 Ω Imr = 8 mA	 160	0.60 3.5 140	0.90 5 240	MHz MHz MHz
Input Noise	R_{MR} = 66 Ω, Imr = 7.23 mA BW = 1 to 50 MHz		1		nV/√Hz
Dynamic Range	Gain falls to 90% @ 5 MHz	3.5			mV
Output Offset Voltage		-200		200	mV
Output Current			2.0		mA
Output Voltage	RDX,RDY		VCC – 2.3		V
Output Resistance		35	50	75	Ω
PSRR	@25MHz		46		dB
Channel Separation	@25MHz	45	60		dB

Write/Servo Characteristics

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range		15	30.8	50	mA
Write Current Resolution			5		bit
LSB			1.13		mA
Write Current Accuracy		-8		+8	%
Differential Head Swing	Open Head, Transient,		9 10		Vpp
Unselected Head Current	DC Transient			50 1	μA mA pk
Damping Resistor	<DR0,DR1>=<0,0> <DR0,DR1>=<1,0> <DR0,DR1>=<0,1> <DR0,DR1>=<1,1>		600 240 150 110		Ω

Head Voltage Monitor

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DBHV upper threshold	HUS = high to low		480		mV
DBHV lower threshold	HUS = low to high		280		mV
ABHV gain		4.75	5	5.25	V/V
ABHV output range		0.9		2.75	V
ABHV output current	Output drops to 90%	1			mA
ABHV output offset		-100		100	mV

Thermal Asperity Detection/Correction/Fast Recovery

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TA Detection Range	At output before correction	50		800	mV
TA Detection Resolution			4		bit
LSB	Rref = 2KΩ		50		mV
Lower Corner Frequency	Fast Recovery mode		3.5	5	MHz
TA Detection Delay			30	100	nS
TA compensation delay			0.4	1.0	µS
TA compensation timer			5		µS

Switching Characteristics

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Write to read	R/W	90% signal envelope, ±30mV DC		0.35	0.7	µS
Read to write	R/W	90% of Iw		30	50	nS
Idle to read	CS	90% signal envelope, ±30mV DC		3	15	µS
Write to idle	CS	10% of Iw			1	µS
Head Switching	HSn	90% signal envelope, ±30mV DC		3	15	µS
Write Current rise/fall time		Lh=185nH, Iw=30.8mA, Rh = 16Ω, Rd = 600 Ω, 10% to 90%		2	2.5	nS
Head Current Delay		50% of WD to 50% of Iw			20	nS
Write Current Asymmetry		Propagation delay difference			0.5	nS

Head Unsafe Detection

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FLT low to high		0.5	1	2	µS
FLT high to low				200	NS
Write data frequency	Valid transient detector			100	MHz
	Valid Open detector			10	MHz
MR head open threshold		895	970	1045	MV
MR head short threshold			50	60	MV

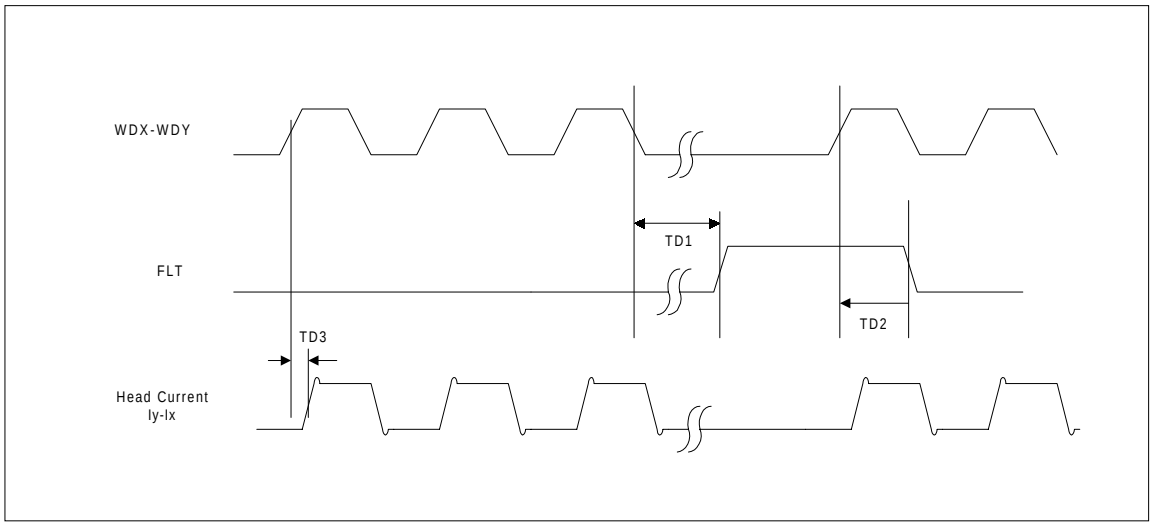
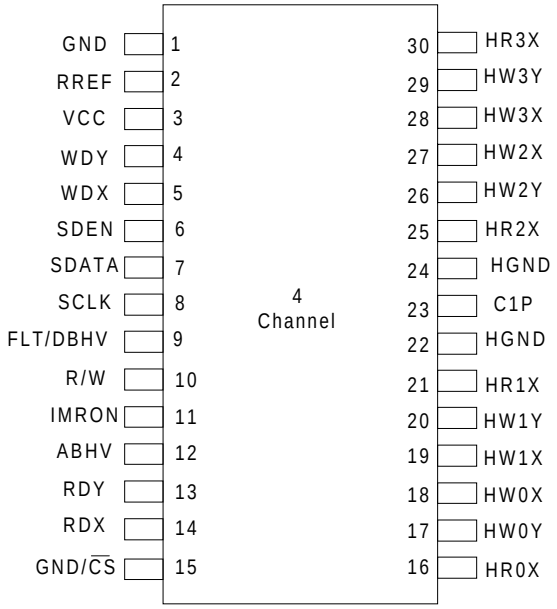


FIGURE 3: Write Current & Head Unsafe Timing

PACKAGE PIN DESIGNATIONS



30-Lead TSSOP

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SR1622AB
+5, +8V, 4-CHANNEL GMR READ/WRITE DEVICE

June, 2000

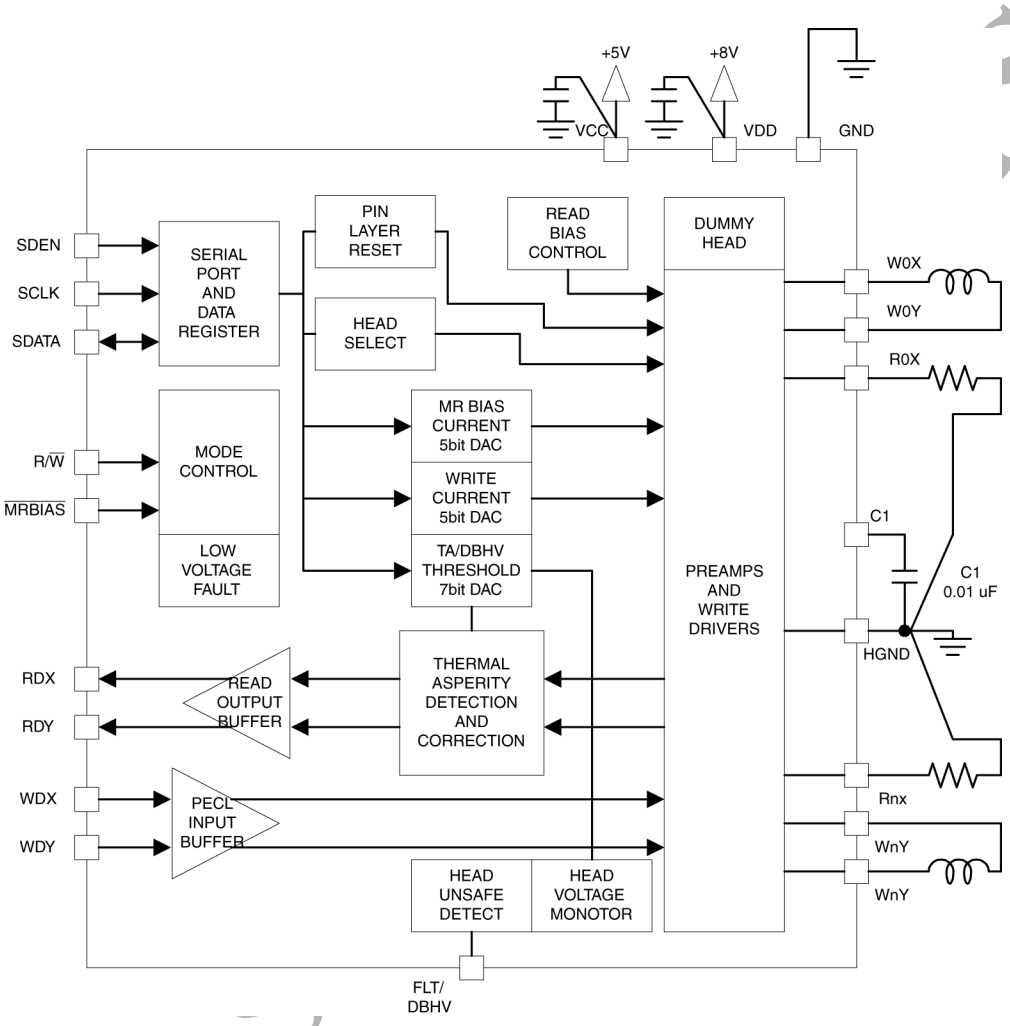
DESCRIPTION

The TI SR1622AB is a BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive read and thin film write composite recording heads. It provides a low noise 5 volt GMR head amplifier, GMR bias current control, thermal asperity detection and correction, GMR pin layer reset function, an 8 volt thin film write driver, write current control, and TFH fault detection circuit for up to four channels. The device features programmable read gain, write damping resistance and thermal asperity threshold level. The device allows multiple channel write functions for servo writing in the bank write mode. Control of features and thresholds is provided through a serial port interface. The SR1622AB requires a +5V and a +8V supply, and comes in a 38 TSSOP package. Part marking is SR1622AB. Note "/" in the part marking is a placeholder for a letter designating the manufacturing site.

FEATURES

- **One side grounded input, fully differential output**
- **Unselected Read/Write heads at GND potential**
- **Thermal asperity detection and compensation**
- **MR resistor measurement mode**
- **MR bias current range = 2 to 9.75mA (5bit) (all range guaranteed)**
- **MR resistor range =25 to 75 Ω**
- **Programmable read gain =150 V/V or 190 V/V @45Ω, IMR=6 mA**
- **Input equivalent noise 1.1 nV/√Hz @45Ω (TBD)**
- **Read Frequency boost**
- **Write current range = 16.17 to 61.20 mA (5bit)**
- **Active write damping**
- **Programmable write current boost control (2 bit)**
- **Programmable write current undershoot control (1 bit)**
- **Impedance matched differential write data input, no flip-flop**
- **Bank write mode**
- **Power fault protection**
- **3.3 V CMOS compatible logic interface**
- **Fast write current rise/fall times = 0.9 ns (Ltf = 90 nH, Rtf = 18 Ω, Iw = 39.65 mA)**
- **GMR pin layer reset voltage pulse capability**
- **Internal reference resistor**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SR1622AB addresses up to 4 four terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with 3.3V logic pins R/$\overline{W}$, $\overline{MRBIAS}$ and the serial port as shown in Table 1. R/$\overline{W}$ and $\overline{MRBIAS}$ inputs have internal pull-up resistors so that when left opened, they will default to the logic high state.

The serial port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold level and mode.

Device power-on resets the serial port bits to their default values, which places the device into sleep mode. To place preamp into an active mode (read or write mode) from sleep mode, the device should be placed in idle mode and then read mode to activate an internal quick recovery circuit.

SLEEP MODE

The chip is set to sleep mode by setting $\overline{SLP}$ bit of the Mode register low. Only the serial port and voltage fault monitor are active in this mode. The $\overline{SLP}$ bit overrides all other mode control setting bits and pins. Upon power-up, the device will reset the serial port to its default values, which places the device into sleep mode.

IDLE MODE

The $\overline{IDL}$ bit in Mode register of the serial port controls idle mode. Internal reference voltage and DACs are activated when $\overline{IDL}$ bit is set to low in non-sleep mode. During idle mode, the internal write current generator, and read output buffer are deactivated. The reference circuit is on, but MR bias current does not flow through either the selected head or the internal dummy head. All the connections to the external C1 capacitor are opened to preserve charge on the capacitor.

The only fault detected in idle mode is low VCC. If the VCC voltage drops below 3.5 V, the FLT output will go low. When the power supply voltage returns to above 4 V, the fault will clear.

TABLE 1: Mode Selection.

$\overline{SLP}$	$\overline{IDL}$	R/$\overline{W}$	$\overline{MRBIAS}$	SBW0/SBW1	Mode
0	X	X	X	X	Sleep
1	0	X	X	X	Idle
1	1	1	0	X	Read, IMR on (selected head)
1	1	1	1	X	Read, IMR off
1	1	0	0	0/0	Write, IMR on (selected head)
1	1	0	1	0/0	Write, IMR off
1	1	0	1	1/1	Servo Write, IMR off
1	1	0	0	1/1	Servo Write, IMR on

NOTES: $\overline{SLP}$, $\overline{IDL}$, SBW0/SBW1 are serial port bits (Mode register)
See Servo mode section for Bank write activation procedure

READ MODE

Taking the R/$\overline{W}$ pin high in non-idle mode selects read mode which activates the MR bias current generator and low noise differential amplifier. $\overline{MRBIAS}$ pin must be low to activate the MR bias current through the designated head. When $\overline{MRBIAS}$ is high, MR current to the selected head is disabled and the C1 node will be set to high impedance. MR bias current is diverted to the internal dummy load when the head selection bits are set to a value outside the allowed range.

The outputs of the read amplifier RDX/RDY are emitter followers and are in phase with the resistivity change at the selected input port (RnX/HGND) where the respective MR head is attached. The read mode gain is set to one of two values based on the GAIN bit of serial port Mode register. Make sure to set register bit WDH to zero for correct gain.

The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port. The magnitude of the bias current is set according to the following equation:

$$Imr\ (mA) = 2.0 + 0.250 \bullet N$$

where N = 0,1,...31 is the decimal value of serial port register bits IR0:IR4.

In write mode, when $\overline{MRBIAS}$ pin is low, MR bias current remains on the selected MR head. When $\overline{MRBIAS}$ pin is high in write mode, MR bias current to the selected head is turned off and the external C1 capacitor preserves its charge by making all its connections high impedance. During switching from head to head, the chip selects an internal dummy head (20 ohm nominal) to discharge C1 capacitor so that the selected MR will see no current overshoot during the transition.

N	Imr (mA)	N	Imr (mA)	N	Imr (mA)	N	Imr (mA)
0	2.00	8	4.00	16	6.00	24	8.00
1	2.25	9	4.25	17	6.25	25	8.25
2	2.50	10	4.50	18	6.50	26	8.50
3	2.75	11	4.75	19	6.75	27	8.75
4	3.00	12	5.00	20	7.00	28	9.00
5	3.25	13	5.25	21	7.25	29	9.25
6	3.50	14	5.50	22	7.50	30	9.50
7	3.75	15	5.75	23	7.75	31	9.75

THERMAL ASPERITY DETECTION AND COMPENSATION

The Thermal Asperity circuitry can be controlled by the combination of serial port bits TAC, TAD and the thermal asperity threshold setting bits TA6:TA0. These bits control four combination of thermal asperity handling, i.e. Off, TA detection only, TA correction On the Fly mode, and TA correction Retry mode (see Table 2). Note that to enable TA detection, the TAD = 1, MRM = 0, and the threshold bits TA6:0 must be set for the appropriate threshold.

In TA Retry mode, the low corner frequency of the read amplifier is shifted up to 5 MHz to remove low frequency content of the TA event. TA Retry mode activates and maintains the low corner frequency shift as long as the mode is enabled.

In On the Fly mode, both TA compensation and the low frequency corner shift are activated when a thermal asperity is detected. With TA compensation, the chip detects the peak voltage of the thermal asperity and subtracts the peak from the read output. The amplifier returns to its normal operating state 2 µsec after the signal has returned below the TA threshold voltage. The TA detection threshold is set by bits TA0:TA6 of the TA data register. The threshold value is same as the DBHV threshold voltage.

In On the Fly mode, FLT/DBHV pin flags low when the chip detects a thermal asperity, and returns high once the uncompensated read signal returns below the threshold. In Retry mode, the FLT/DBHV pin flags low until retry mode is deactivated.

The threshold level for the thermal asperity detector is programmable through the serial port according to the following:

$$Vta\ (mV) = 6 \bullet N \quad mV\ (nominal)$$

where N = 1,2...127 is the decimal value of serial port register bits TA0:TA6. The threshold level is referred to the peak of the RDX output prior to the TA disturbance.

TABLE 2: Thermal Asperity Modes

TAC	TAD (MRM=0)	Thermal Asperity Mode
0	0	Off (no detection or compensation)
0	1	TA Detection only Threshold set by TA6:0
1	0	Retry mode (low corner frequency shift)
1	1	On the Fly mode (TA comp plus corner frequency shift) Threshold set by TA6:0

NOTE: To enable TA detector, TAD = 1 and MRM = 0. TAD takes priority over MRM if both TAD = 1 and MRM = 1

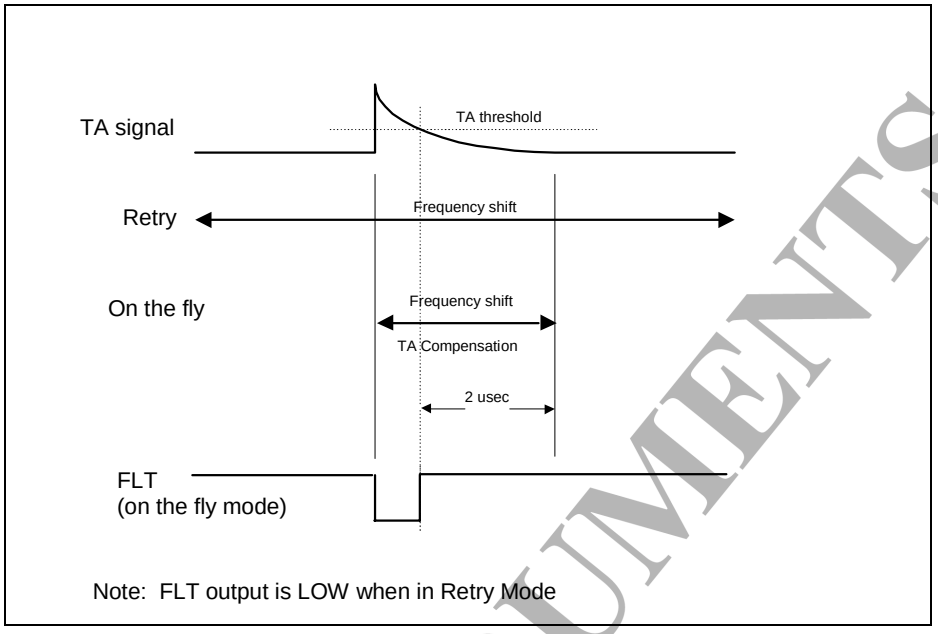


FIGURE 1: Thermal Asperity Modes

WRITE MODE

Taking R/$\overline{W}$ low in non-idle mode selects write mode. Write current is enabled to the selected channel and write data (WDX/WDY) controls the write current polarity. Head current is toggled between the X and Y side of the selected head on each transition of the differential signal WDX-WDY, when WDX is higher than WDY, the current flows from X (WnX) to Y (WnY). The write data input buffer is active in all modes except sleep mode.

Write current magnitude is controlled by a five-bit on board DAC. The DAC is programmed via the serial port. The magnitude of the write current (0-pk) is given by:

$$Iw\ (mA) = 16.17 + 1.474 \bullet N\ (mA\ 0\text{-}p)$$

N	Iw (mA)	N	Iw (mA)	N	Iw (mA)	N	Iw (mA)
0	16.17	8	27.96	16	39.75	24	51.55
1	17.64	9	29.44	17	41.23	25	53.02
2	19.12	10	30.91	18	42.70	26	54.49
3	20.59	11	32.38	19	44.18	27	55.97
4	22.07	12	33.86	20	45.65	28	57.44
5	23.54	13	35.33	21	47.12	29	58.92
6	25.01	14	36.81	22	48.60	30	60.39
7	26.49	15	38.28	23	50.07	31	61.86

where N = 0,1 ... 31 is the decimal value of serial port register bits IW0:IW4.

Unselected write heads are pulled to ground potential (+/- 0.3 V).

The MR bias current on the selected head can be controlled in write mode by the state of the $\overline{MRBIAS}$ pin. When $\overline{MRBIAS}$ = 0, bias current will flow through the selected head. The magnitude of the MR bias current is set by the serial register bits IR0:IR4 (register HS/IMR). When $\overline{MRBIAS}$ = 1, the MR bias current will be deactivated.

BANK WRITE MODE

Servo bank write mode allows simultaneous writing to multiple heads to reduce servo write efforts. Heads activated in bank write mode can be selected by HS0, HS1, and HS2 bits, as shown in Table 6. If there is no head connected to the selected channels, the open head channels will be shut off in this mode. Exiting from bank write mode clears the shut off state. To set the correct bank write current use the formula and the table given at the end of this section. Both, the formula and the table, are different from the formula and the table given in the WRITE MODE section.

The steps to activate servo bank write mode are as follows:

1. Place device in read mode (R/$\overline{W}$ pin high).
2. If VDD = +5.0 VDC set VDMSKH bit to 1.
3. Set SBW0 bit to 1.
4. Set SBW1 bit to 1.
5. Set SBW0 bit to 0.
6. Load head select bits for desired bank write configuration.
7. Load read MR bias current DAC (IMR Register).
8. Place device in write mode (R/$\overline{W}$ pin low).

The MR bias current will be disabled in bank write mode when $\overline{MRBIAS}$ = 1. MR bias current can be enabled in all-head or half-head bank write mode by placing $\overline{MRBIAS}$ pin low as described in Table 6. When enabled, the read MR bias current is divided equally to all four read elements. In other words, the MR bias current delivered to each head will be 1/4th or 1/2 the programmed value of the IMR DAC. Since normal MR bias range is 2 – 9.75 mA, the MR bias range in servo bank write mode is 0.50 – 2.4375 mA or 1.00 – 4.875 mA.

Once steps 1 through 5 above have been initiated, bank write current can be enabled/disabled by the state of the R/$\overline{W}$ pin. The device exits bank write mode when SBW1 = 0.

The VDMSKH bit of serial register Write allows the user to disable the Low VDD fault detection. This step is necessary when operating the device in bank write mode with VDD less than 7.2 VDC.

During an all head bank write condition, the write current should be limited to less than 40 mA 0-pk at VDD less than 6VDC. In addition, it is recommended that the chip operate in a well-controlled ambient temperature when servo write is active to prevent excessive junction temperatures. The thermal resistance of the package varies by mount conditions. Setting the OTMSKL bit of the Mode register to 1 will enable the over - temperature monitor. With OTMSKL=1, when an over temperature condition is detected the IC will assert the FLT/DBHV pin, set the HOT bit of the Fault Status register to 1, and shut off the writer current.

$$Iwbank\ (mA) = 16.17 + 1.474 \bullet N\ (mA\ 0\text{-}p)$$

N	Iw (mA)	N	Iw (mA)	N	Iw (mA)	N	Iw (mA)
0	16.17	8	27.96	16	39.75	24	51.55
1	17.64	9	29.44	17	41.23	25	53.02
2	19.12	10	30.91	18	42.70	26	54.49
3	20.59	11	32.38	19	44.18	27	55.97
4	22.07	12	33.86	20	45.65	28	57.44
5	23.54	13	35.33	21	47.12	29	58.92
6	25.01	14	36.81	22	48.60	30	60.39
7	26.49	15	38.28	23	50.07	31	61.86

FAULT OPERATION

The FLT/DBHV pin is an open collector output line, multiplexed between the DBHV and FLT output. When MR measurement mode is inactive, the pin is a fault status output. The FLT/DBHV output flags low when the chip is in a voltage fault condition, regardless of operating mode. Certain faults are also flagged in the Fault Status register of the serial port. Writing 00h to the Fault Status register will clear all bits in this register. The Fault Status register may not power-up with all fault bits cleared. The user should clear the Fault Status register by writing 00h after power-up.

READ MODE

A low on the FLT/DBHV pin indicates one of the following unsafe conditions:

- Device in TA correction mode (See TA detection description),
- TA event detected (See TA detection description),
- Open or shorted MR element,
- Low Vcc,
- Low Vdd (if active),
- Out of range head select

READ MODE FAULT DETAILS:

Open MR Element

When the voltage across the selected MR head exceeds the open head threshold (970mV typ), a MR open fault is detected and reported by setting the FLT output low and the corresponding serial port fault status bit is set. To prevent damage to the head, the MR bias current is shutoff and the fault latched. The fault may be cleared by selecting a normal head or by switching to idle mode and back to read mode following removal of the open head. The FLT output returns high after the fault has been cleared.

MR Element Short To Ground

When the voltage across the selected MR head drops below the shorted head threshold (50 mV typ), a MR short to ground fault is detected and reported by setting the FLT output low and the corresponding serial port fault status bit is set. The MR bias is not disabled upon detection of this fault, and the fault is not latched. The FLT pin returns high when the fault condition no longer exists.

Low VCC

If the VCC power supply drops below the Low VCC threshold (3.5 V, typ), a fault will be detected and reported by setting the FLT output low. The MR bias will be disabled (if active), upon detecting a Low VCC fault. When the power supply returns to a normal level (4V), the fault will be cleared: the FLT pin will go high and the MR bias reactivated if $\overline{\text{MRBIAS}}$ = low.

Low VDD

If the VDMSKH bit is set to 0, and if the VDD power supply drops below the Low VDD threshold (6.1 V typ) a fault will be detected and reported by setting the FLT output low and the corresponding serial port fault status bit will be set. The IC will shut off the MR bias current (if active) upon detecting a Low VDD fault. When the VDD voltage returns to a normal level, or the VDMSKH bit is set to 1, the fault will be cleared: the FLT pin will go high and the MR bias reactivated if $\overline{\text{MRBIAS}}$ = low.

Out Of Range Head Select

If an out of range head is selected a fault will be detected and reported by setting the FLT output low. The MR bias current is shunted to an internal dummy head.

Write Mode

A high on the FLT/DBHV pin indicates one of the following unsafe conditions:

- An open head, valid up 10 MHz (freq. TBD),
- Write head short to ground,
- Write data frequency too low (freq = 500 - 1000 KHz),
- An open reference resistor,
- Device in Servo Mode,
- Low supply voltage.

WRITE MODE FAULT DETAILS:

Write Head Open
If the write head output develops an open circuit during write mode, a fault will be detected and reported by placing the FLT pin high and the corresponding serial port fault status bit will be set. The operation of the writer does not change when an open head is detected. The fault will be cleared when the open circuit condition is removed or if a non-faulted head is selected. The open head detector operates over a restricted range of write data frequency, and will detect an open head when the write data pulse width is greater than TBD. The detector is disabled above this frequency to eliminate any false detection.

Write Head Short To Ground
If the write head shorts to ground, a fault will be detected and reported by setting the FLT pin high. The write current and MR bias current are not disabled when a write head short is detected. The FLT pin will return low once the short condition is removed. In this revision of the SR1622AB, the head short to ground is reported to the serial port fault status register as a TF OPEN fault.

Only the Low supply voltage fault disables the write current (non-latching fault). The Low supply fault can be either a Low VDD or Low VCC fault. Low VDD fault detection can be disabled through use of the serial register bit Low VDD Disable.

Low VCC
If the VCC power supply drops below the Low VCC threshold (3.5 V, typ), a fault will be detected and reported by setting the FLT output high. The write current and MR bias (if active) will be disabled upon detecting a Low VCC fault. When the power supply returns to a normal level (4V), the fault will be cleared: the FLT pin will go high and the write current and MR bias reactivated if $\overline{\text{MRBIAS}}$ = low.

Low VDD
If the VDMSKH bit is set to 0, and if the VDD power supply drops below the Low VDD threshold (6.1 V typ) a fault will be detected and reported by setting the FLT output low and the corresponding serial port fault status bit will be set. The IC will shut off the write current upon detecting a Low VDD fault. When the VDD voltage returns to a normal level, or the VDMSKH bit is set to 1, the fault will be cleared: the FLT pin will go high and the MR bias reactivated if $\overline{\text{MRBIAS}}$ = low.

Bank Write Mode
When register bit OTMSKL=1, an over-temperature condition will be indicated by setting register bit HOT to 1, and the write current will be disabled. The over-temperature detection can be disabled by setting OTMSKL = 0.

Idle/Sleep Mode
A low on the FLT/DBHV pin indicates the following unsafe condition:

Low supply voltage (VCC < 3.5 V typ).

MR RESISTANCE MEASUREMENT MODE

MR resistance measurement can be activated in read mode by setting MRM bit in the Mode register. In this mode, the FLT/DBHV pin can be configured to output a Digital Buffered Head Voltage (DBHV) indication.

With MRM = 1 and TAD = 0, FLT/DBHV pin becomes the digital head voltage monitor. The DBHV threshold is programmed by TA/BHV data register. When the MR head voltage is lower than the set internal threshold voltage, the FLT/DBHV pin flags high. When the MR head voltage is higher than the set DBHV threshold, FLT/DBHV flags low. In DBHV mode, fault protection can be disabled by setting FMSKH bit to high

A recommended application of the MRM mode is to fix the MR bias current, adjust the DBHV threshold until the FLT/DBHV pins asserts (goes low). The MR resistance is equal to the DBHV threshold setting (in mV) divided by the MR bias setting (in mA). It is recommended that the MR bias setting be fixed while the TA threshold is adjusted, rather than fixing the threshold and adjusting the MR bias, to prevent damage to the head from excessive bias current. Note that DBHV will not operate for thresholds below MR Short threshold of 50mV.

In Fault or DBHV mode, the FLT/DBHV pin is configured as an open collector digital output.

GMR RESET MODE

The SR1622AB includes a voltage pulse generation feature to provide a pinned layer reset function for GMR heads. When activated, the device will generate a positive voltage pulse (relative to HGND) of programmable magnitude, from 0.41 V to 1.48 V. The duration of the pulse can be selected between two settings, 48 ns or 95 ns. The pulse will decay to the ground potential with a turn-off decay slew rate, which can be set to one of four settings. The circuit uses a constant decay current so the resulting decay time is proportional to the voltage difference between the applied reset magnitude and the ground potential. The decay slew rateis selectable as shown in Table 3. The Reset pulse is applied from zero bias voltage. See Figure 2 for reset pulse timing.

TABLE 3: GMR Reset Pulse Decay Slew Rate

PLRDT1	PLRDT0	Decay Slew Rate [V/μs]
0	0	6.8
0	1	5.3
1	0	3.6
1	1	1.9

The reset pulse circuit must be armed prior to triggering the reset pulse. The following procedure will properly arm the reset circuit:

1. Turn MR bias current off by setting $\overline{\text{MRBIAS}}$ = 1.
2. Place device into Idle mode. Program the PLR magnitude using the write current register (IW4:IW0) and the desired MR bias current (IR4:IR0).
3. Place device in Read mode. Select valid read head. Set serial port bit FMSKH = 1 to mask faults, and select desired settings of serial port bits PLRPW, PLRDT1 and PLRDT0.
4. Make PLREN =1. Device enters PLR ARM mode at the end of serial port transfer.

The reset pulse fires when the $\overline{\text{MRBIAS}}$ pin is brought low after arming. The pulse trigger must be applied at least 50 μs after arming the reset circuit. Placing $\overline{\text{MRBIAS}}$ = 1 will disarm the reset circuit. Consecutive reset pulses require arming the circuit before it can be re-triggered. In other words, the user must bring PLREN bit to 0, and then to 1, before the PLR pulse can be triggered again.

The magnitude of the reset voltage pulse is controlled by the write current DAC (IW4:IW0). The minimum setting is 0.41V, the maximum setting is 1.48V. See Table 4 for reset magnitude.

Other serial port bits used by the GMR reset circuit include:

- PLREN: enables the pin layer reset mode.
- PLRPW: selects the reset pulse width, T2 (48 ns or 95 ns).
- PLRDT1, PLRDT0: select pulse decay time, T1 (refer to Table 3).

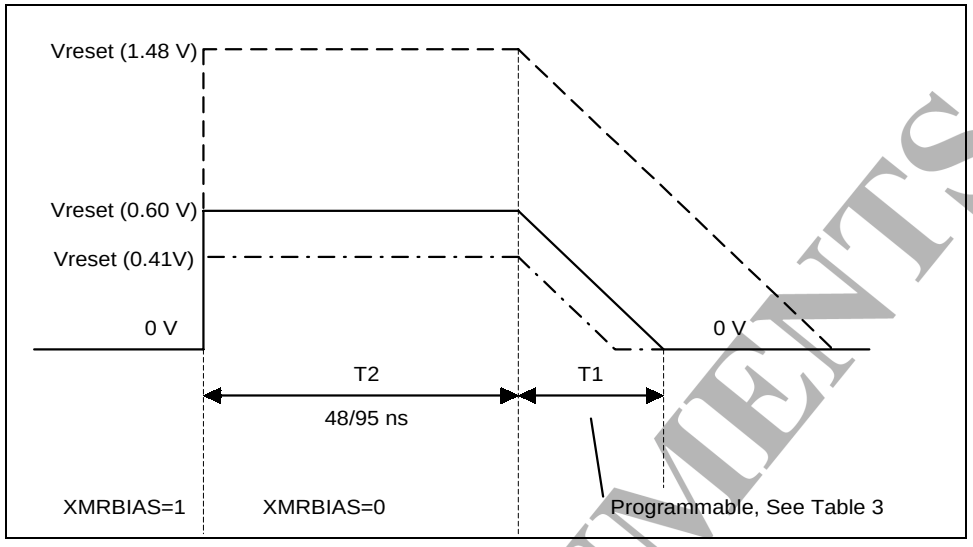


FIGURE 2: Typical GMR Reset Pulse Shape

Use the following table to set the GMR Reset Pulse Amplitude:

TABLE 4. GMR Reset Pulse Amplitude **(Set By IW DAC)**

IW4	IW3	IW2	IW1	IW0	PLR Amplitude
0	0	0	0	0	0.41 V
0	0	0	0	1	0.45 V
0	0	0	1	0	0.49 V
0	0	0	1	1	0.53 V
0	0	1	0	0	0.56 V
0	0	1	0	1	0.60 V
0	0	1	1	0	0.64 V
0	0	1	1	1	0.68 V
0	1	0	0	0	0.72 V
0	1	0	0	1	0.76 V
0	1	0	1	0	0.80 V
0	1	0	1	1	0.83 V
0	1	1	0	0	0.87 V
0	1	1	0	1	0.91 V
0	1	1	1	0	0.95 V
0	1	1	1	1	0.98 V

IW4	IW3	IW2	IW1	IW0	PLR Amplitude
1	0	0	0	0	1.05 V
1	0	0	0	1	1.09 V
1	0	0	1	0	1.12 V
1	0	0	1	1	1.16 V
1	0	1	0	0	1.20 V
1	0	1	0	1	1.23 V
1	0	1	1	0	1.27 V
1	0	1	1	1	1.30 V
1	1	0	0	0	1.34 V
1	1	0	0	1	1.37 V
1	1	0	1	0	1.40 V
1	1	0	1	1	1.42 V
1	1	1	0	0	1.44 V
1	1	1	0	1	1.45 V
1	1	1	1	0	1.47 V
1	1	1	1	1	1.48 V

NOTE: DAC step size is not linear for upper DAC settings.

VOLTAGE FAULT MONITOR

During power up or power fault condition (approximately VCC < 1.1 VDC), the voltage monitor disables the chip from any active mode. The serial data is reset to sleep mode with the default setting value.

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold and mode. The serial port bit map is shown in Table 5.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/$\overline{W}$ bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0, and S2=0 for preamplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map).

Asserting the serial port enable line SDEN initiates a transfer, SDATA is clocked into the internal shift register by the rising edge of SCLK. A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. When writing to a register, loading of the register takes place on the falling edge of SDEN. The SDATA bits are clocked on the rising edge of SCLK when writing to the preamp registers (see Figure 3).

On register readback, the address bits are clocked on the rising edge of SCLK, as in write mode. The data bits are clocked out of the register on the falling edge of SCLK in order for the readback device to clock in the data bits on the subsequent rising edge of SCLK (see Figure 3).

The three serial port lines are 3.3 volt logic compatible. See Digital Input/Output specifications for 3.3 V logic details.

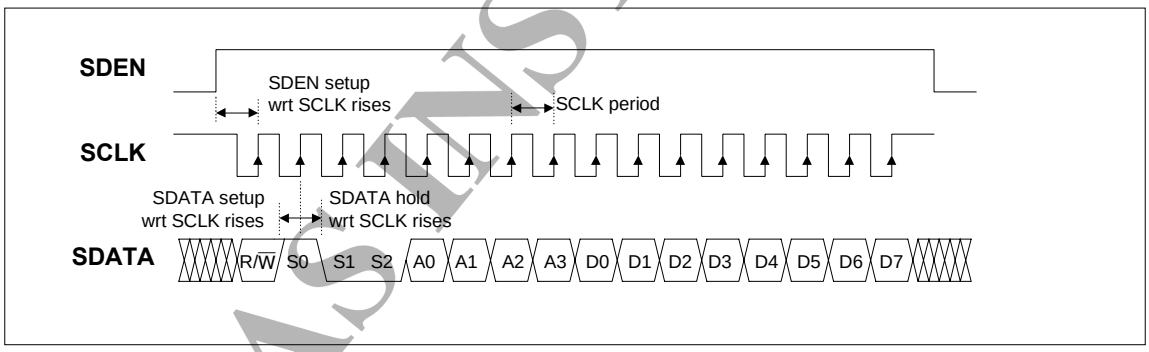


FIGURE 3: Serial Port Timing

TABLE 5: Serial Port Bit Map

Reg	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	VEN0	VEN1	VEN2	REV0	REV1	REV2	REV3	REV4
HS/IMR	100	1000	HS0	HS1	HS2	IR0	IR1	IR2	IR3	IR4
Write	100	0100	IW0	IW1	IW2	IW3	IW4	TBLKL	VDMSKH	SBW1
TA/BHV	100	1100	TA0	TA1	TA2	TA3	TA4	TA5	TA6	TAC
Mode	100	0010	$\overline{\text{SLP}}$	$\overline{\text{IDL}}$	GAIN	MRM	RB	SBW0	SGMENL	OTMSKL
Misc	100	1010	WDH	GMENL	OC0	OC1	UC	BWR1	BWR2	FMSKH
Fault	100	0110	HOT	Low VDD	MR_O	MR_S	TF_O	TF_S	TF_F_L	X
Res	100	1110	PLRDT1	PLRDT0	PLRPW1	PLRPW0	PLREN	WFMSKH	TAD	Res

ID register is read only.
All Data bits are set to 0 at reset condition, i.e. power-up or voltage fault condition, except ID register.
X = not used
Res = Reserved for TI internal use or future control features, User setting = 0.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A3, A2, A1, A0, S2, S1, S0. Serial port Read/Write bit is not shown.

ID REGISTER (READ ONLY REGISTER)

Address = 0000 001

BIT	NAME	DESCRIPTION
7:3	REV4:0	Device Revision (00001 is assigned for this revision).
2:0	VEN2:0	Vender ID (001 is assigned for the SR1622AB).

HS/IMR REGISTER

Address = 0001 001

BIT	NAME	DESCRIPTION
7:3	IR4:IR0	MR bias current setting, see Read Mode description for bias equation. LSB = 0.25 mA. 11111 = maximum MR bias current (9.75 mA) 00000 = minimum MR bias current (2.0 mA) (See the READ MODE section for the complete table.)
2:0	HS2:HS0	Head Select bits, see Table 6 for head select bit maps

WRITE REGISTER

Address = 0010 001

BIT	NAME	DESCRIPTION
7	SBW1	Servo Bank Write Control bit. Must be used in conjunction with SBW0 bit to activate servo bank write mode (see Bank Write Mode description) 1 = Activate servo bank write mode 0 = Disable servo bank write mode
6	VDMSKH	Low VDD Disable. 1 = Disable Low VDD voltage detection and reporting 0 = Enable Low VDD voltage detection.
5	TBLKL	Blanking time duration control. Sets the duration of the blanking time for write-to-read and MR bias off-to-on switching. 1 = Blanking on duration = 200 nsec 0 = Blanking on duration = 400 nsec
4:0	IW4:IW0	Write current magnitude. See the WRITE MODE section for the equation and the table. This DAC is also used to set the BANK WRITE MODE current and the PLR pulse magnitude. Write mode: LSB = 1.45 mA 11111 = maximum write current (61.20 mA) 00000 = minimum write current (16.25 mA) (See the BANK WRITE MODE section for the formula and the table.) (See the PLR MODE section, Table 4, to set the GMR Reset Pulse amplitude.)

TAD REGISTER
Address = 0011 001

BIT	NAME	DESCRIPTION
7	TAC	Thermal Asperity Correction enable when high. Correction on the fly. (TA compensation plus frequency shift at TA) TAC = 1 TAD = 1 MRM = 0 Correction retry mode. (continuous low corner frequency shift) TAC = 1 TAD = 0 MRM = 0
6:0	TA6:0	TA detection threshold (MRM=0, TAD = 1) or Digital Buffered Head Voltage comparator threshold (MRM=1, TAD = 0). LSB = 6 mV 1111111 = maximum threshold (762 mV) 0000001 = minimum threshold (6 mV) 0000000 = Invalid threshold setting (This DAC is also used for MR RESISTANCE MEASUREMENT MODE.)

MODE REGISTER
Address = 0100 001

7	OTMSKL	Over temperature detection, bank write mode only. 1 = Over temperature detection enabled (Over temp condition sets HOT flag in Fault Status register.) (No effect on read mode). 0 = Over temperature detection disabled
6	SGMENL	Super Gm mode control. Bit can be used to optimize idle-to-read and write-to-read switching times. 1 = Disables super high Gm stage irrespective of the operating mode. 0 = Enables super high Gm mode during certain mode conditions.
5	SBW0	Servo Bank Write Mode enabled when toggled with other conditions. (See Bank Write Mode description)
4	RB	Read frequency boost 1 = Read Boost enabled. 3.0 dB boost at 140 MHz 0 = Disable Read frequency boost
3	MRM	MR Measurement Mode for digital BHV. (see MR Measurement Mode) 1 = Enables MR measurement mode (TAD = 0) 0 = Disables MR measurement mode
2	GAIN	Read Amplifier Gain select when WDH = 0 1 = high gain mode (190V/V) 0 = low gain mode (150V/V) When WDH = 1 1 = high gain mode (225 V/V) 0 = low gain mode (150 V/V)
1	IDL	Idle Control Bit 0 = Idle mode enabled
0	SLP	Sleep control bit 0 = Sleep mode enabled. Overrides all other control modes

MISC REGISTER
Address = 1010 001

BIT	NAME	DESCRIPTION
7	FMSKH	Fault report disable 1 = Disable reporting of all faults. MR bias will not be disabled upon an open MR head fault. 0 = Enable normal fault reporting
6:5	BWR2:BWR1	Programmable read bandwidth (-1 dB, nominal values listed) 11 = 160 MHz 10 = 130 MHz 01 = 260 MHz 00 = 210 MHz
4	UC	Write Current Undershoot Control 1 = maximum write current undershoot 0 = minimum write current undershoot (only valid when OC0 = 1)
3:2	OC1:OC0	Write Current Overshoot Control. (Alternate names: OC0 = DRV, OC1 = XC) 11 = maximum write current overshoot 00 = minimum write current overshoot
1	GMENL	High-Gm enable. Controls whether the High-Gm mode is activated during mode switching. The write-to-read, idle-to-read, MR bias off-to-on, head-to-head, and super-high-Gm on-to-off switching times are affected by this bit. 1 = High-Gm mode disabled 0 = High-Gm mode enabled.
0	WDH	Reserved for gain testing.1 = +6dB 0 = default user setting.

FAULT STATUS REGISTER
Address = 0110 001

Fault Status register provides status bits for determining which fault triggered an indication on the FLT/DBHV pin. Logic 1 indicates the respective fault was detected. Writing 00h to this register will clear all status bits. Faults are written to this register on the active edge of the fault event. Therefore, if a fault condition continues to exist after clearing the status register, it will not be latched into this register again. Fault register may not clear upon power-up, user should write 00h to register to clear status register as part of power-up routine

BIT	NAME	DESCRIPTION
7	--	Not Used
6	TF_F_L	Write Data Frequency Low detected
5	TF_S	Write Head Short to Ground detected (Write head short will be reported as an write open head TF_O)
4	TF_O	Write Head Open or Short to Ground detected
3	MR_S	MR Head Short detected
2	MR_O	MR Head Open detected
1	Low VDD	Low VDD voltage detected.
0	HOT	Over temperature condition detected in bank write mode only. OTMSKL bit must be enabled to activate this flag.

RESERVED REGISTER
Address = 1110 001

BIT	NAME	DESCRIPTION
7	Res	Reserved for ABHV function in future revisions.
6	TAD	Thermal Asperity Detector Enable 1 = Enables thermal asperity detector when MRM = 0. TA threshold set by TA6:0 bits (Register TAD) 0 = Disable TA detector
5	WFMSKH	Disable write faults 1 = Disables write fault reporting only. The functioning of the writer remains unchanged. All other fault modes operate normally. 0 = Enable normal write fault reporting
4	PLREN	Pinned Layer Reset Enable 1 = Enable Pinned Layer Reset mode 0 = Disable Pinned Layer Reset mode
3	PLRPW0	PLR reset pulse width control, T2 1 = 95 nsec 0 = 48 nsec
2	Res	Reserved for PLRPW1. User setting = 0
1:0	PLRDT0:PLRDT1	PLR pulse decay slew rate control. See Table 3 11 = 1.9 V/µs 01 = 3.6 V/µs 10 = 5.3 V/µs 00 = 6.8 V/µs (For PLR Pulse Amplitude see Table 4 in the GMR RESET MODE section.)

TABLE 6: Head Selection

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	BANKWRITE MODE HEAD SELECTED
0	0	0	0	None
0	0	1	1	1,3
0	1	0	2	None
0	1	1	3	None
1	0	0	Dummy	None
1	0	1	Dummy	All Heads
1	1	0	Dummy	None
1	1	1	Dummy	0,2

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RREF	I/O	Not connected.
MRBIAS	I	MR bias current on: 3.3V logic with internal pull-up. Bias current active at low.
WnX, WnY	O	Inductive write head connection.
RnX	I/O	MR read head connection, positive end.
HGND	I	MR head connection, negative end.
FLT/DBHV	O	Multiplexed pin: Fault output or DBHV. An open collector output. Fault mode: (MRM = 0) Read mode: A low indicates abnormal read condition. Write mode: A high indicates abnormal write condition. MR measure mode: DBHV comparator output. (MRM = 1) A high indicates the head voltage is lower than the set threshold. A low indicates the head voltage is higher than the set threshold.
R/$\overline{W}$	I	Read/Write: 3.3 V logic with internal pull-down. Write active low.
RDX,RDY	O	Differential Read Data output.
GND	I	Ground
REFGND	I	Reference return. May or may not be externally tied to GND.
VCC	-	+5V power supply.
VDD	-	+8V power supply for write driver.
SDEN	I	Serial Port Enable. 3.3 V logic.
SDATA	I/O	Serial Data. 3.3 V logic.
SCLK	I	Serial Clock. 3.3 V logic.
C1	I	Bias loop control capacitor, C1, connected to ground (0.01 μF)
WDX/WDY	I	Write Data input, PECL

ELECTRICAL SPECIFICATION

Unless otherwise specified, Rmr=45Ω Imr=6mA (setting value), Ltf=90nH, Rtf=18Ω, Iw=40.90mA (setting value), RDX/RDY load = 2.00 kΩ diff.

ABSOLUTE MAXIMUM RATINGS

Operation beyond maximum ratings may result in permanent damage to the device.

PARAMETER		RATINGS
DC Supply Voltage	VCC	-0.3 to 6 VDC
DC Supply Voltage	VDD	-0.3 to 9 VDC
Logic Input Voltage	3.3 V Logic	-0.3 to 6 VDC
	WDX/WDY	-0.3 to 6.0 VDC
Differential WD Input Voltage	WDX/WDY	2.0 V
Write Current	Iw	75 mA 0-pk
MR Bias Current	I_{MR}	20 mA
Write Head Voltage	V_{WH}	-0.3V to VDD+0.3 V
Read Head Voltage	V_{MR}	0 to 1.2 V
Output Current	RDX,Y	-10 mA
Storage Temperature	Tstg	-55 to 150 °C
Operating Junction Temperature	Tj	+150 °C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		RANGE
DC Supply Voltage	VCC	4.5 to 5.5 VDC
DC Supply Voltage	VDD_Write	7.2 to 8.8 VDC
	VDD_Bankwrite	4.5 to 5.5 VDC
Write head load range	L_H	60 to 180 nH
Write head resister range	R_{WH}	5 to 25 Ω
MR head range	R_{MR}	25 to 75 Ω
Operating Ambient temperature	Ta	0 to 70 °C

POWER SUPPLY

GMENBL = TBLKL = 1 BWR1 = BWR2 =0, WDH = 0

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VDD Supply Current	VDD	Read	14	15	18	mA
		Write, Iw=40.90mA	69	72	79	mA
		Bankwrite 4 channels, Iw=39.65mA, Vdd= +5.0 Vdc	180	200	210	mA
		Idle	4	5	6	mA
		Sleep		0	1	mA
VCC Supply Current	VCC	Read IMR off	13	14	16	mA
		Read IMR on, Imr=7mA	29	39	44	mA
		Write IMR off, Iw=40mA	29	31	34	mA
		Write IMR on, Iw=40mA, Imr=8mA	39	49	55	mA
		Bankwrite 4 channels, Iw=39.65mA, Vdd=+5.0Vdc	65	75	85	mA
		Idle	8	9.3	11	mA
		Sleep	1	1.6	3	mA

DIGITAL INPUT/OUTPUT

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input High Voltage (R/$\overline{W}$,SDEN,SCLK, SDATA,$\overline{MRBIAS}$)	V_{IH1}	3.3 V Logic I_{IH1} = -4.5 mA, C_L = 30 pF	1.5			VDC
Input Low Voltage (R/$\overline{W}$,SDEN,SCLK, SDATA,$\overline{MRBIAS}$)	V_{IL1}	3.3 V Logic I_{IL1} = 9.0 mA, C_L = 30 pF			0.7	VDC
Input Hysteresis	V_{HYS}		TBD			mV
Input Leakage Current (SDEN,SCLK,SDATA)	Ileak	Inactive state			1	µA
Pull-up resistor ($\overline{MRBIAS}$)	Rpu			20		KΩ
Pull-up resistor (R/$\overline{W}$)	Rpu			50		KΩ
Common mode voltage	V_{CMW}	WDX-WDY PECL Inputs	1.4	2	V_{CC}-0.85	VDC
Input Δ Voltage	ΔV_{I3W}	Write Mode	0.4			V diff
Input Δ Voltage	ΔV_{I3R}	Read or Idle Mode	0.2			V diff
Input Δ Voltage	ΔV_{I3S}	Sleep mode	0.0			V diff
Differential input R	Z_{ID}	WDX/WDY input	100	125	150	Ω
Input Capacitance	Cinw	WDX,WDY Cap to ground			5	pF
Input Current	I_{IH3}	Write Mode ΔV_{I3W} = 0.4V		3.2		mA

DIGITAL INPUT/OUTPUT (continued)

Output High Voltage	V_{OH}	R_L = 1.7K Ω (FLT)	Open Collector			
		R_L = 1K Ω (SDATA)				
Output Low Voltage	V_{OL}	R_L = 1.7K Ω to 3.6 V* (FLT)			0.3	V
		R_L = 1K Ω to 3.6 V* (SDATA)			0.3	V
Output Low Sink Current	I_{OL}	(FLT)	3.0			mA
		(SDATA)	5.0			mA

* Note 3.6V was used as the worst case condition for the nominal 3.3V power supply.

SERIAL PORT TIMING, READ

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		40			nS
SCLK Low Time	T_{CKL}		16			nS
SCLK High Time	T_{CKH}		16			nS
Enable to SCLK	T_{SENS}		14			nS
SCLK to Disable	T_{SENH}		10		40	nS
Data Set-up Time	T_{DS}		6			nS
Data Hold Time	T_{DH}		6			nS
SDEN min. Low Time	T_{SL}		80			nS

READ CHARACTERISTICS

GMENL = TBLKL = 1, BWR2 = BWR1 = WDH = 0, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		25	45	75	Ω
MR Bias Current	Programmable Range	2.0		9.75	mA
MR Bias Current	Guaranteed performance range	4		9	mA
MR Bias Current Resolution			5		bit
LSB			250		µA
MR Current Tolerance		-8		+8	%
MR Head DC Voltage Range		100		900	mV
Unselected Head Current				± 10	µA
Input Resistance (RIN)			3.2		Ω
Differential Voltage Gain	R_{MR} = 45Ω, Low Gain load = 2KΩ diff, f = 80 MHz	135	150	165	V/V
	R_{MR} = 45Ω, High Gain load = 2KΩ diff, f = 80 MHz	171	190	209	V/V
Read Gain Constant	Av*(RMR+RIN), Low Gain		7230		Ω
	Av*(RMR+RIN), High Gain		9162		Ω
Head to head gain variation				2	%
Bandwidth Low Gain, Lh = 0 nH, Rmr = 60 Ω	Lower -3dB	150	540	800	KHz
	Higher -1dB	140	220	290	MHz
	Higher -3dB, RB=0	260	345	425	MHz
	Higher -3dB, RB=1	300	410	510	MHz
Group delay flatness	f = 15 - 170 MHz, low gain, no boost, Rmr = 60 Ω	0.2	0.7	1.0	ns
Boost Voltage Gain	f = 140 MHz, Rmr = 60 Ω	2.6	3.0	3.3	dB
Input Noise (Excludes RMR, includes current noise)	R_{MR} = 45Ω, low gain mode, f = 1 - 85 MHz	0.8	1.3	1.6	nV/√Hz
THD	Vin = 0.5 mV p-p, F =40MHz	44	46	47	dB
Dynamic range	THD < -40 dB@ 40 MHz	1.5	2	2.5	mV
Output Offset Voltage	Low Gain	-200		200	mV
	High Gain	-300		300	mV
Head to head offset voltage				TBD	mV
Output Current	220 ohm load differential	4.0			mA
Output current leakage	Non-read mode	-40		+40	µA
Output Voltage			Vcc-3.0		V
Output Resistance	Single-ended		40		Ω
Output Resistance	Differential		80		Ω
Input Ref. PSRR (VCC)	Vin = 100 mV p-p @ 40 MHz	35	39	45	dB
Input Ref. PSRR (VDD)	Vin = 100 mV p-p @ 40 MHz	35	44	50	dB
Channel Separation Rmr = 60 Ω	15 - 40 MHz	60	63	65	dB
	40 - 170 MHz	40	43	45	dB

MR BIAS OVERSHOOT

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
MR bias overshoot	Iosbir	Idle to read	-5	0	5	%
MR bias overshoot	Iosbri	Read to idle	-5	0	5	%
MR bias overshoot	Iosvfr	Vcc Fault to read	-5	0	5	%
MR bias overshoot	Iosvdfr	VDD fault to read	-5	0	5	%
MR bias overshoot	Iosrwe	Read to write with bias on	-5	0	5	%
MR bias overshoot	Ioswrd	Write to read with bias off	-5	0	5	%
MR bias overshoot	Ioswre	Write to read with bias on	-5	0	5	%
MR bias overshoot	Ioshs	Head switch*	-5	0	5	%
MR bias overshoot	Iosc	Bias cycling	-5	0	5	%

* Head switch includes all variations of switching from min. to max. Imrbias, from max. to min. Imrbias, from 30Ω to 50Ω Rmr, and from 50Ω to 30Ω Rmr.

WRITE/SERVO CHARACTERISTICS

OC1 = 1, OC0 = 1,UC = TBD, GMENL = BWR1 = BWR2 = TBLKL = WDH =0

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range		16.17		61.20	mA
Bank Write Current Range		16.17		61.2	mA
Write/Bank Write Current Resolution			5		bit
LSB			1.474		mA
Write/Bank Write Current Accuracy	N = 5 to 28	-8		+8	%
	N = 0 – 4, 29 – 31	-15		+15	%
Head Voltage Swing	Open Head, Vdd = 8 VDC				Vpp
	Transient, Vdd = 8 VDC				Vpp
	Open Head, Vdd = 5 VDC				Vpp
	Transient, Vdd = 5 VDC				Vpp
Unselected Head Current	DC	-100		100	µA
Write data frequency range		5		160	MHz

HEAD VOLTAGE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DBHV threshold resolution			7		bit
DBHV minimum threshold*			160		mV
LSB		4.5	6	7.5	mV
MR head short detect threshold			50	75	mV
MR head open detect threshold		900	970	1040	mV

* DBHV will not operate accurately for threshold levels below 160mv due to the current design's limitations.

THERMAL ASPERITY DETECTION/CORRECTION/FAST RECOVERY
GMENL = TBLKL =1, BWR2 = BWR1 = 0, WDH = 0.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TA Detection Resolution			7		bit
TA Detection Minimum threshold	At output before correction	4.5	6	7.5	mV
TA Detection Maximum threshold	At output before correction	571	762	953	mV
LSB		4.5	6	7.5	mV
TA detect accuracy				40	%
Lower Corner Frequency	At correction mode		8.5	10	MHz
TA Detection Delay			50	100	nS
TA Correction Delay			0.4	1.0	µS
TA Event over Delay		1.0	2.0		µS

SWITCHING CHARACTERISTICS
GMENL = TBLKL = 1, BWR2 = BWR1 = 0, WDH = 0, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write to Read Switching	90% signal envelope, ±30mV			500	nS
Read to Write Switching	90% of Iw		20	50	nS
Idle to Read Switching	90% signal envelope, ±30mV DC		8		µS
Read to Idle Switching	10% of read envelope			TBD	nS
Head Switching, read mode	90% signal envelope, ±30mV DC *		14	20	µS
Head Switching, write mode	90% of write current			TBD	nS
Write to Idle or Iw turnoff	Delay for Iw to meet leak spec			TBD	nS
Sleep to Idle				600	µS
Idle to Sleep				10	µS
Iw rise/fall time 10% to 90%, write mode	Lh=90nH, Iw=39.65mA, Vdd=8V		0.9	1.5	nS
Iw rise/fall time 10% to 90%, Servo Bank Write mode	Lh=90nH, Iw=29.5mA, Vdd=5.0V		1.25	1.6	nS
Head Current Delay (TD3)	50% of WD to 50% of Iw			TBD	nS
Write Current Asymmetry	Propagation delay difference 50% duty cycle write data @ 10 MHz		0.2	0.3	nS

* Head switch includes all variations of switching from min. to max. Imrbias, from max. to min. Imrbias, from 30Ω to 50Ω Rmr, and from 50Ω to 30Ω Rmr.

FAULT DETECTION

GMENL = TBLKL = 1, BWR2 = BWR1 = 0, WDH = 0, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
WD low freq fault detect FLT low to high (TD1)		0.5	1	2	µS
WD low freq fault clear FLT high to low (TD2)		50	85	115	nS
Write data frequency	Valid transient detector			160	MHz
	Valid Open detector		10	TBD	MHz
VCC Fault Voltage	Write mode Iw = 16.25mA		3.5		V
VCC Fault hysteresis	Fault removed		500		mV
VDD Fault Voltage	Write mode Iw = 16.25mA		6.1		V
VDD Fault hysteresis	fault removed		600		mV

OVER TEMPERATURE DETECTION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Over temperature detection threshold	Servo Mode, OTMSKL = 1		135		°C

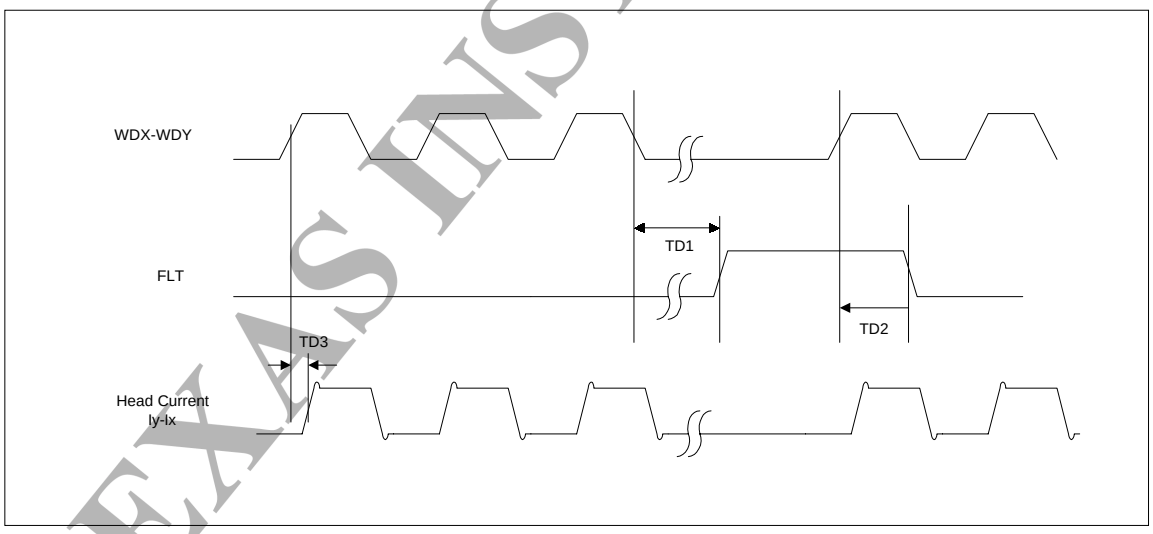
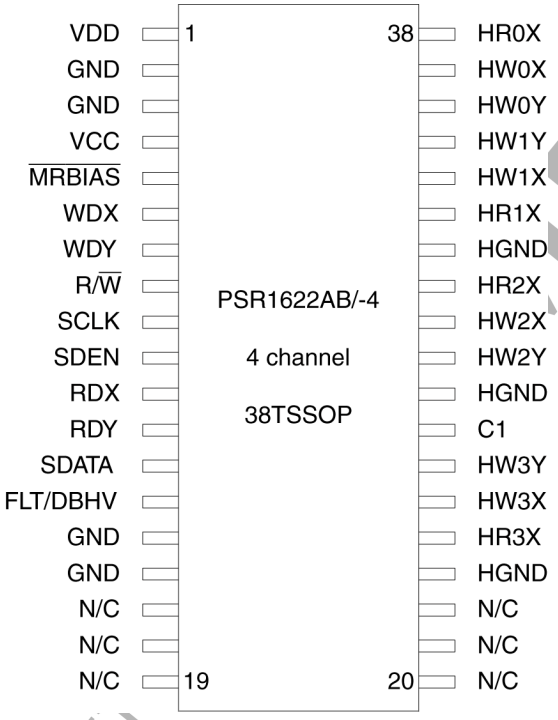


FIGURE 5: Write Current & Head Unsafe Timing

PACKAGE PIN DESIGNATIONS



Texas Instruments Storage Products, 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SR1710AFA
+5, +8V, 4/2/1-CHANNEL GMR READ/WRITE DEVICE

Prototype

May, 2000

DESCRIPTION

The TI SR1710AFA family of preamps are BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive read and thin-film write composite recording heads. It provides a low noise GMR head amplifier, GMR bias current control, an 8-volt thin film write driver with programmable overshoot, write current control, thermal asperity detection and correction, and fault detection circuit for up to four channels. The device features programmable read gain, write resistive and active damping and thermal asperity threshold level. The device allows multiple channel write functions for servo writing. In the 4- and 2-channel part, half or all of the heads can be simultaneously selected in the servo write mode. Control of features and thresholds is provided through a serial port interface. The TI SR1710AFA requires a +5V and a +8V supply and is available in a 38 pin TSSOP package for the 4 channel part and in a 24 pin TSSOP package for the 2 and 1 channel part.

FEATURES

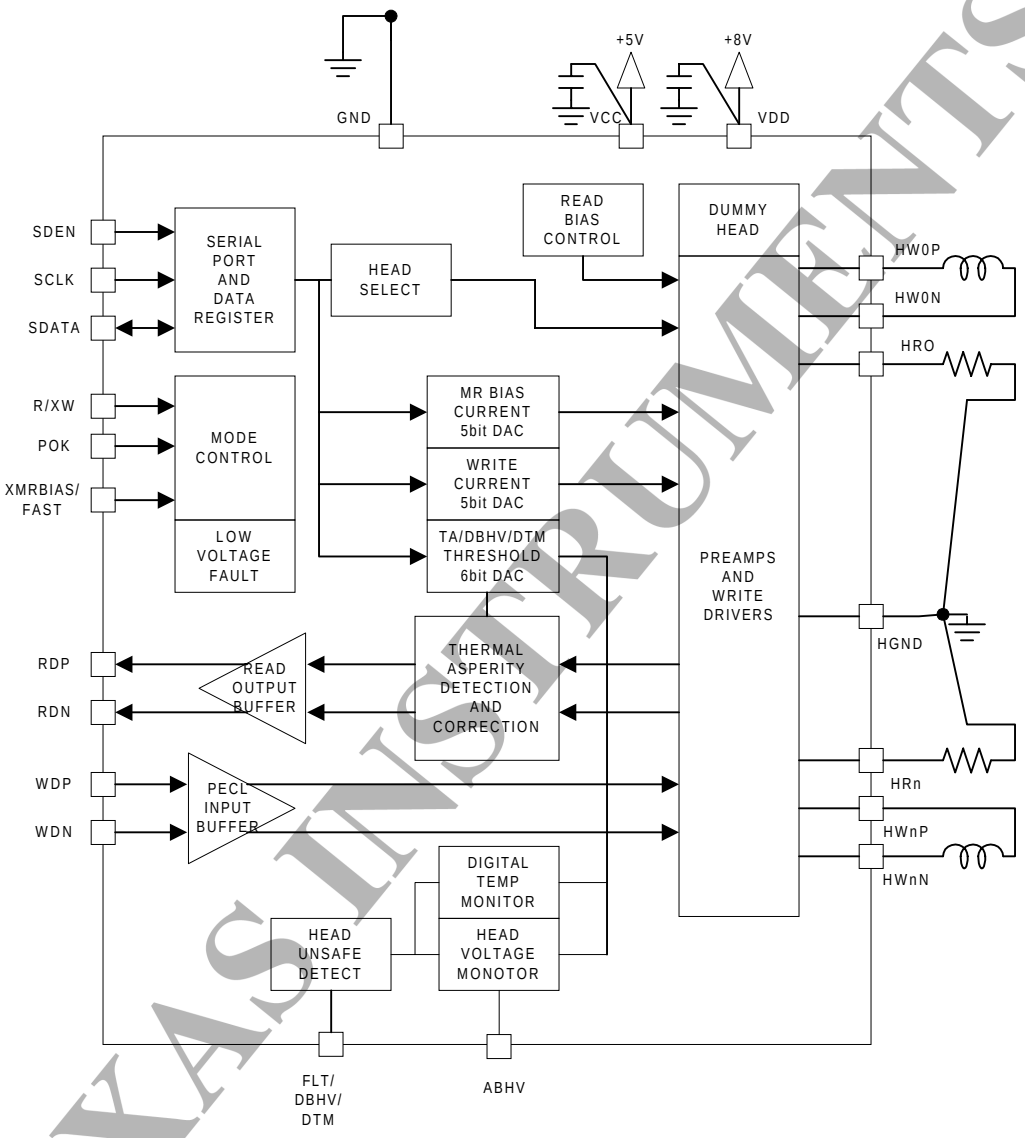
READ CHARACTERISTICS

- **One side grounded input, fully differential output**
- **I-bias/I-sense reader architecture**
- **Unselected Read/Write heads at GND potential**
- **Programmable read gain = 100 V/V, 150 V/V or 220 V/V @ 50Ω Rmr, Imr = 5.2ma**
- **MR bias current range = 2 to 8.2 mA (5 bit)**
- **Total input equivalent voltage and current noise 0.72 nV/√HZ @ 50 Ω, IBIAS 5.2 mA**
- **Automatic read input bandwidth compensation**
- **MR resistor range =25 to 80Ω**
- **Thermal asperity detection and compensation**
- **MR resistor measurement mode**
- **Read blocking and noise capacitors integrated on chip**
- **Current bias setting resistor on chip**

WRITE CHARACTERISTICS

- **Write current range = 15 to 60 mA (5bit)**
- **Fast write current rise/fall time = 0.75 ns (Lh = 90 nH, Rh = 18 Ω, Iw = 40 mA)**
- **Programmable write current boost (2bit)**
- **Programmable active or resistive write damping**
- **Impedance matched differential write data input, no flip-flop**
- **Servo bank write**
- **MR bias during servo write capability**

BLOCK DIAGRAM



FEATURES (continued)

GENERAL

- **Digital temperature monitor function**
- **3V compatible analog and digital I/O**
- **Power fault protection**
- **Drop-in replacement for 32R1615AR-4DBT GMR preamp (4-channel version only)**
- **Fast write to read switching time = 400 ns**

FUNCTIONAL DESCRIPTION

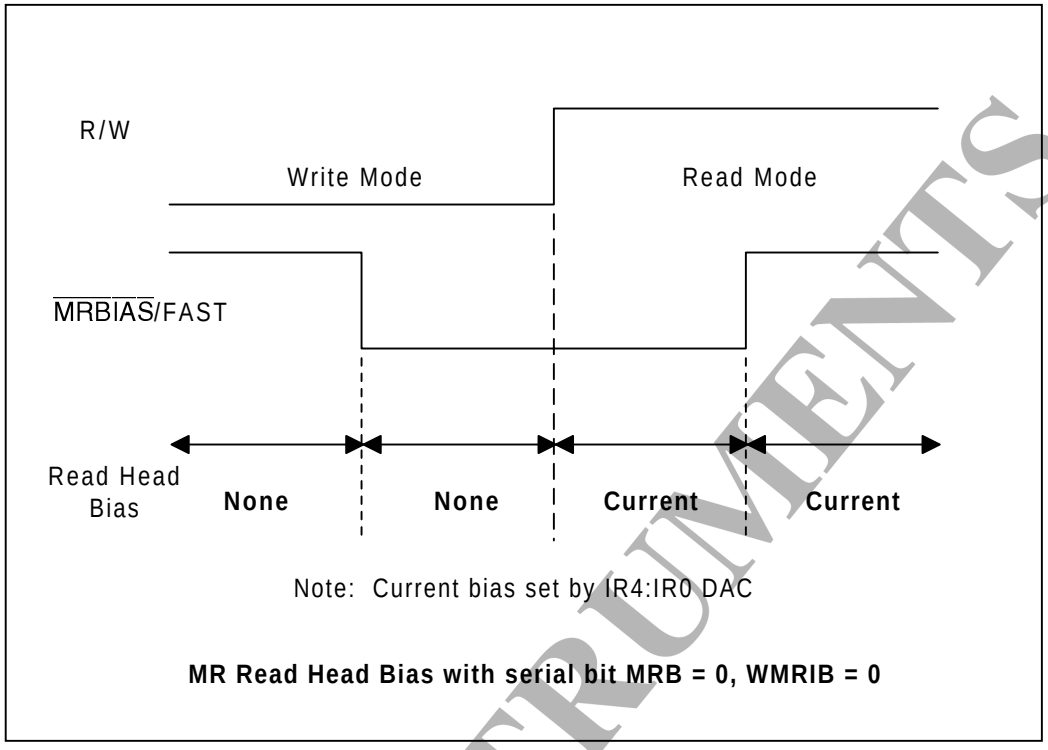
The TI SR1710AFA addresses 4, 2 or 1 four-terminal MR heads providing write drive or read bias and amplification. The mode control is accomplished with 3.3V compatible pins R/XW, XMRBIAS/FAST, POK and the serial port as shown in Table 1. The R/XW input has an internal pull-up resistor so that when left opened, it will default to the logic high state, while the XMRBIAS/FAST input has an internal pull-down resistor. The POK line has an internal pull-up resistor.

The serial port is used to control head selection, bank write mode, write current magnitude, MR bias current magnitude, read gain, MR head resistance measurement, and thermal asperity threshold level and mode.

TABLE 1: Mode Selection

R/XW (pin)	WM RIB (bit)	POKB *POK (Note 1)	MRB (bit)	XMRBIAS/ FAST (pin)		SBW (bit)	XIDL (bit)	XSLP (bit)	Mode	MR head bias on selected head	
										IMR DAC	HB DAC (IMRB)
1	X	X	1	0	-	0	1	1	Read Active	ON	OFF
1	X	X	1	1	-	0	1	1	Read Inactive (Note 4)	OFF	ON
1	X	X	0	-	1 (Note 2)	0	1	1	Read Active Fast recovery	ON	OFF
1	X	X	0	-	0 (Note 2)	0	1	1	Read Active	ON	OFF
1	X	X	0	X	X (Note 3)	0	1	1	Read Active	ON	OFF
0	X	1	1	1	-	0	1	1	Write	OFF	OFF
0	X	1	1	0	-	0	1	1	Write	OFF	ON
0	0	1	0	X	-	0	1	1	Write	OFF	OFF
0	1	1	0	X	-	0	1	1	Write	ON	OFF
0	X	1	1	0	-	1	1	1	Servo Bank Write	OFF	ON (Note 5)
1	X	1	1	0	-	1	1	1	Servo Bank Read	ON (Note 6)	OFF
0	X	0	1	0	-	X	1	1	Write/ Servo Disabled	OFF	OFF
X	X	X	X	X	-	X	0	1	Idle	OFF	OFF
X	X	X	X	X	-	X	X	0	Sleep	OFF	OFF

NOTE 1: This represents the logical AND of POKB bit and POK pin.
NOTE 2: When in TA retry recovery mode: TAD=0 and TAC=1.
NOTE 3: When not in TA retry recovery mode.
NOTE 4: Read path is off in this mode.
NOTE 5: The bias voltage is applied to all activated heads and is set by the HB serial port bits.
NOTE 6: Single-head read. Selected head based on single-head mode of HS bits.



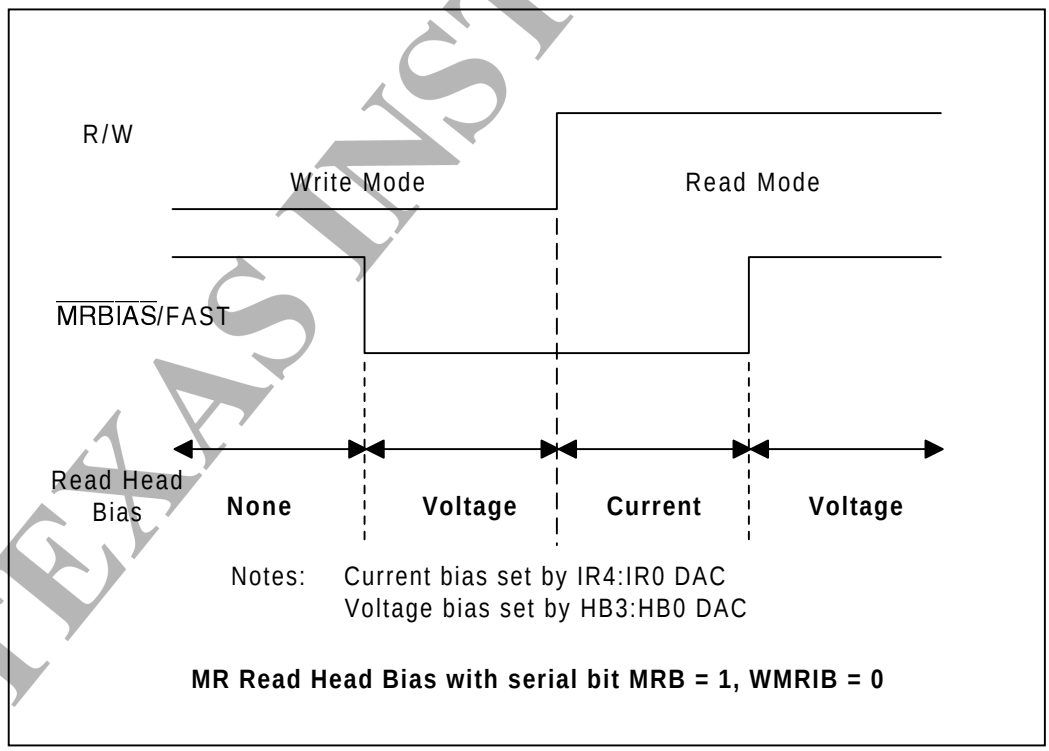
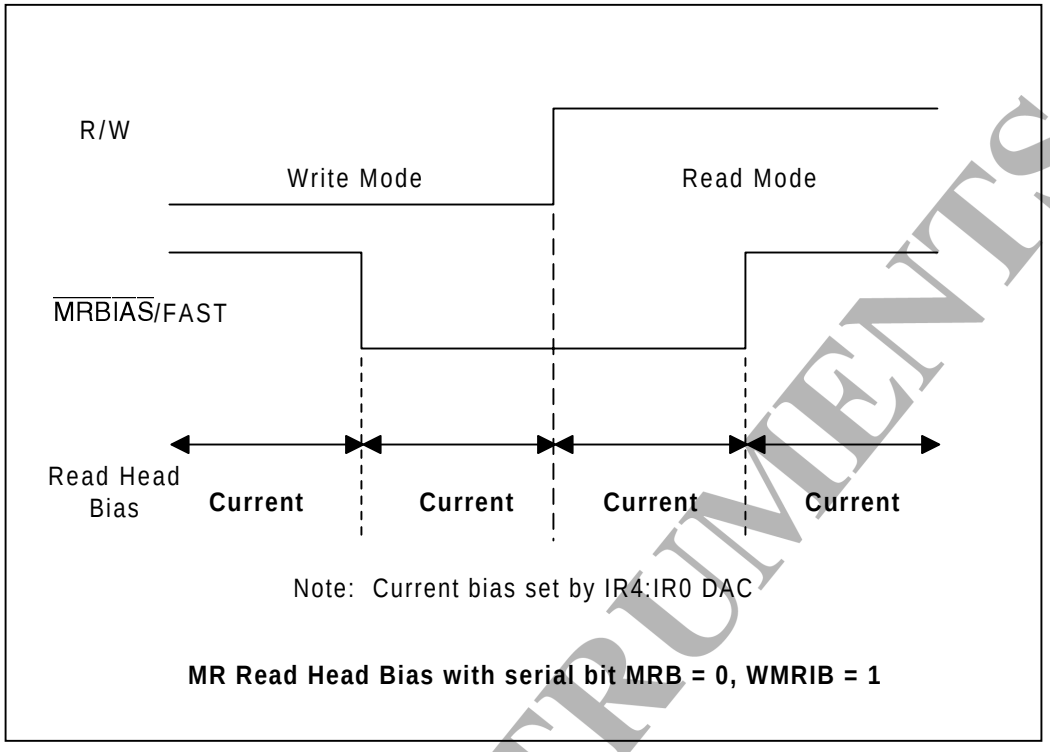


FIGURE 1A: MR Bias Control, 32R1615 Equivalent



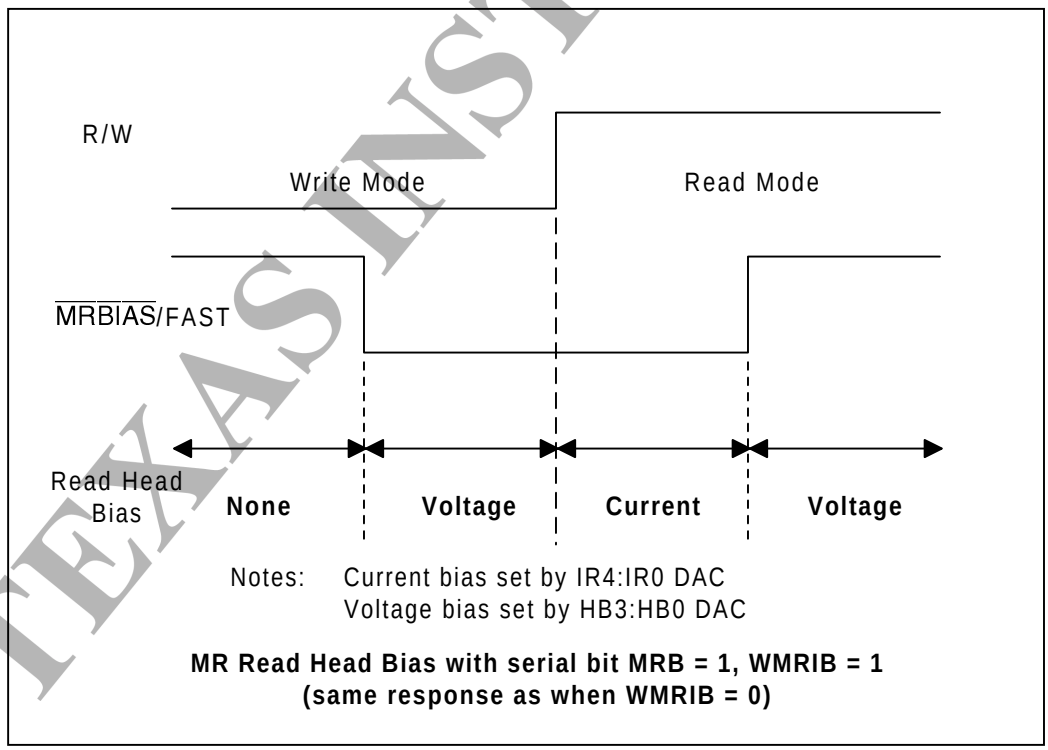


FIGURE 1B: MR Bias Control, Using WMRIB Bit

WRITE MODE

Taking R/XW low in non-idle mode selects write mode. Write current is enabled to the selected channel and write data (WDP/WDN) controls the write current polarity. Head current is toggled between the P and N side of the selected head on each transition of the differential PECL signal WDP-WDN. When WDP is higher than WDN, the current flows from P (WnP) to N (WnN). The write function is disabled when POK pin is low.

The SR1710AFA write and servo bank write modes are fully enabled only when both the POK pin and the POKB serial port bit are logic high, with R/XW low. Placing the POK pin low will disable write modes. The POKB serial port bit is bi-directional: the chip will reset POKB = 0 when the POK pin transitions from high to low. The user must set POKB = 1 and place the POK pin high in order to restore write mode control to the R/XW pin.

Write current magnitude is controlled by a five-bit on board DAC. The DAC is programmed via the serial port. The magnitude of the write current (0-pk) is given by:

$$Iw\ (mA) = 15 + 1.45*N\ (mA\ 0\text{-}p)$$

where N = 0,1 ... 31 is the decimal value of serial port register bits IW0:IW4.

Note that the actual head current Ix,y is given by:

$$Ix,y\ (mA) = \frac{Iw}{1 + \frac{Rh}{Rd}}$$

where Rh is the head DC resistance and Rd is the damping resistor. . When bit DRO = 0 or DR1 = 0, the writer is in active damping mode and Rd can be considered to be infinite in above equation. With DRO = 1and DR1 = 1, Rd = 150 ohms.

The SR1710AFA offers write current boost. The amount of current boost is controlled by the serial port bits WAC0:WAC1. With WAC0:WAC1 set to 00, maximum current boosting occurs. The combination of programmable write current boost and write damping control allows the user to adjust the write current waveform to achieve an optimized response with various load conditions.

The MR head can be biased with a programmable voltage or current in write mode depending on the state of the MRB and WMRIB serial port bits and the XMRBIAS/FAST pin (see Figure 1A and 1B). If MRB = 0, the MR bias current can be activated with by setting WMRIB bit = 1. When MRB = 0 and WMRIB = 1, MR bias current will be supplied to the read element. The amount of MR bias current is set by the IMR DAC as in read mode. When MRB = 0 and WMRIB = 0, no bias will be applied to the read element in write mode.

If MRB = 1, MR bias to the selected head is controlled by the state of the XMRBIAS/FAST pin. If XMRBIAS/FAST = 1, then the MR bias is disabled in write mode; if XMRBIAS/FAST = 0, then a voltage is applied to the selected head through the use of the HB3:HB0 serial port bits (IMRB DAC). This feature provides a means to maintain the MR head voltage above ground potential during write operations. The MR bias voltage is given by:

$V_{MR} = 30 \bullet N$ (mV), where N = 0..15 is the decimal value of HB3:HB0.

When switching between write and read mode, bias mode change overlaps by approximately 5 nsec to eliminate bias transient coupling. To prevent MR overbias during the overlap period, it is recommended that the Vmr setting be less than the head voltage resulting from normal read bias current.

SERVO BANK WRITE MODE

Servo bank write allows simultaneous writing to multiple heads to reduce servo write time and efforts. The design allows write operation with VDD = 5.0V with slightly slower rise/fall time performance. This option is primarily intended to reduce device power dissipation in servo bank write mode. It is recommended that the chip operate in a well-controlled ambient temperature when servo write is activated to prevent excessive junction temperatures. The thermal resistance of the package varies by mount conditions. Heads activated in the bank write mode are selected by HS0 and HS1 bits as shown in Table 4. Note that if HS2 = 1, a head select out of range fault will be reported. The recommended steps to activate servo bank write are as follows:

Option 1 (VDD < 6.6)

1. Power-up device with following conditions:
   - VDD = 6.6 volts or smaller
   - POK pin should be high
2. Set FLTDIS bit to 1 to disable faults.
3. Place device in read mode, RXW pin high.
4. Set SBW0 bit to 1.
5. Load head select bits for desired bank write activation (even, odd or all heads).
6. Load HBDAC bias voltage (TA4:7 Reg 3)
7. Place device in write mode, RXW pin low. The R/W pin is used to control write action.
8. Enable faults by setting FLTDIS bit to 0. This allows high temp fault to be monitored, however may cause low VDD fault when R/W pin = 1 (read mode).

NOTE: FLTDIS bit must be set to 1 before changing back to read mode with low VDD.

Option 2 (VDD = 6.6)

1. Power-up device with following conditions:
   - VDD = 6.6 volts
   - POK pin should be high
2. Place device in read mode, RXW pin high.
3. Set SBW0 bit to 1.
4. Load head select bits for desired bank write activation (even, odd or all heads).
5. Load HBDAC bias voltage (TA4:7 Reg 3).
6. Place device in write mode, RXW pin low. The R/W pin is used to control write action

Caution must be taken with VDD > 5v in Servo mode. Power dissipation must be considered.

Special attention and consideration should be drawn to the SBW bit when not in servo bank write mode. Ensuring its level prevents the device from writing data to the wrong head or reading data from the wrong head. The servo bank write function is disabled when the POK pin is low. See write mode section for a detailed description of the POK operation. MR bias voltage is applied to the read heads equal to the HB DAC setting (HB3:0) as in single-head write mode.

When R/W =1 in servo mode, the device can perform normal single-head reading on the head selected based on the HS0/HS1 bits single-head setting. When switching between write and read mode upon R/W transitions, bias mode change overlaps by approximately 5 nsec to eliminate bias transient coupling. To prevent MR overbias during the overlap period, it is recommended that the Vmr setting be less than the head voltage resulting from normal read bias current.

READ MODE

Taking the R/XW pin high in non-idle mode selects read mode. MR bias for the selected head in read mode is controlled by the state of the MRB serial port bit in conjunction with the XMRBIAS/FAST pin (see Figure 1A and 1B). When MRB = 0, MR bias current is supplied to the selected head based on the value of serial port bits IR4:IR0, and the read path is activated (Read Active mode). When MRB = 1, MR bias is controlled by the state of the XMRBIAS/FAST pin: XMRBIAS/FAST = 0 enables MR bias current controlled by the IR4:IR0 bits (IMR DAC) and activates the read path (Read Active mode); XMRBIAS/FAST = 1 enables MR bias voltage controlled by the state of the HB3:HB0 bits (IMRB DAC) and the read path is disabled (Read Inactive mode).

In read active mode, the outputs of the read amplifier, RDP/RDN, are emitter followers and are in phase with the resistivity change at the selected input port (HRn/HGND) where the respective MR head is attached. The read mode gain is set to one of two values based on the GAIN bit of serial port Mode register.

In read active mode, the DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port. The magnitude of the bias current is set according to the following equation:

$$Imr\ (mA) = 2 + 0.2 * N$$

N = 0,1,...31 is the decimal value of serial port register bits IR0:IR4.

When switching from head to head, or from idle to read mode, the chip selects an internal dummy head (15 ohm nominal) to discharge C1 capacitor (internal) so that the selected MR will see no current overshoot during the transition.

In read inactive mode, the bias voltage is given by:

$V_{MR} = 30 \bullet N$ (mV), where N = 0..15 is the decimal value of HB3:0.

In read inactive mode the C1 capacitor is in a high Z state. The drive should not stay in read inactive

mode for long periods of time to prevent drift on the capacitor. Drift could result in long settling times or, in rare cases, damage to the MR element.

When switching between read active and read inactive modes by using the XMRBIAS/FAST pin with MRB = 1, the bias mode change overlaps by approximately 5 nsec to eliminate bias transient coupling. To prevent MR overbias during the overlap period, it is recommended that the Vmr setting be less than the head voltage resulting from normal read bias current.

Over bias warning:

The SR1710AF will report an open head condition when the MR head voltage, generated as the product of the programmed MR bias current and the MR resistance, exceeds the open head threshold. The open head fault is a flag only, the preamp does not disable the MR bias current. The user should not use the open head fault as a warning of an over bias condition, since excessive MR current could have already caused permanent damage to the MR element before the open head fault is reported. The purpose of the fault is to detect an open head not protect against an over bias condition.

MR RESISTANCE MEASUREMENT MODE

The SR1710AFA offers both an analog and digital head voltage monitor which aids in MR resistance measurements. The ABHV pin outputs the analog head voltage with a gain of 5 V/V. The ABHV output is always on in read mode. The analog ABHV output has an internal clamp circuit designed to keep the output voltage below 2.8 V at any MR head voltage. The digital MR resistance measurement can be activated in read mode by setting MRM bit (D3) in the Mode register. With MRM = 1 (TAD = 0, DTM = 0), the FLT/DBHV pin becomes the digital head voltage monitor output. The DBHV threshold is programmed by TA/BHV data register. When the selected MR head voltage is lower than the set internal threshold voltage, the FLT pin flags a low. When the MR head voltage is higher than the set DBHV threshold, FLT flags high. The threshold voltage for the DBHV is programmable through the TA/BHV serial port register according to the following:

$$Vdbhv\ (mV) = 30 * N\ (nominal),$$

Where N = 0,1… 63 is the decimal value of serial port registers TB0:TB5

Note that the full DBHV threshold range overlaps the MR short and open head thresholds. Since the MR open detector is not disabled during MR measurement mode, the user should restrict the DBHV threshold setting to voltages lower than the MR-open threshold (recommended range is 120 mV to 390 mV, 4< N< 13).

THERMAL ASPERITY DETECTION AND COMPENSATION

The Thermal Asperity circuitry can be controlled by the combination of TAC and TAD bits in TADC data register. The two bits control four combinations of thermal asperity handling, i.e. TA off, TA detection only, On-the-fly TA correction mode and Retry TA correction mode, as shown in Table 2. When the TA detector only mode is active (TAD = 1, TAC = 0), the FLT pin flags low when the chip detects the output exceeds the TA threshold setting.

In On-the-fly TA correction mode (TAD = 1, TAC = 1), the signal pass band lower corner frequency is shifted up to 5 MHz when the TA threshold is exceeded. The TA correction stays on for 2 μsec after the TA event ends (Signal drops below TA threshold) and returns to normal operating mode by itself. The FLT output does not flag a TA event in On-the-fly mode.

The TA detection threshold is set by bits TB0:TB5 of the TA/DTM data register. The threshold level for the thermal asperity detector is programmable through the serial port according to the following:

$$Vta\ (mV) = 30 * N\ \ (nominal)$$

N = 0,1...63 is the decimal value of serial port register bits TB0:TB5. Threshold level is referred to the average of the peak of the RDP output prior to the TA disturbance.

During Retry TA correction mode (TAD = 0, TAC = 1), the XMRBIAS/FAST pin controls the low corner frequency shift (FAST mode). When XMRBIAS/FAST = 1, the pass band lower corner frequency is shifted up to 5 MHz and remains there until the FAST mode is disabled by placing the XMRBIAS/FAST pin low. The FLT output does not flag a TA event in Retry mode.

IDLE MODE

The XIDL bit (D1) in Mode register of the serial port controls idle mode. The internal reference voltage

and DACs are activated when XIDL bit is set to low in non-sleep mode. All connections to the internal C1 capacitor are opened to preserve charge on the capacitor. On an Idle-to-Read transition, the current is diverted to the dummy head for 1uS to ensure that the DC blocking capacitor is settled to a safe low voltage before switching.

SLEEP MODE

The chip is set to sleep mode by setting XSLP bit (D0 in Mode register) low. Only the serial port and internal serial port voltage fault monitor are active in this mode. The XSLP bit overrides all other mode control setting bits and pins. The FLT pull-up is disabled in sleep mode.

FAULT DETECTOR

The FLT pin is a 3-volt logic compatible output line, multiplexed between the DBHV and DTM output. When MR measurement and DTM modes are inactive (MRM = 0, DTM = 0), the pin is a fault status output. The FLT output is asserted when the chip is in a voltage fault condition, regardless of operating mode. In addition to asserting the FLT output, the detected fault updates the FLT register. The FLT register is updated whenever a FLT flag transition is detected. The FLT register is cleared by loading all zeros to it.

Read Active Mode

A low on the FLT pin indicates one of the following unsafe conditions:

- TA event detected in TA detection mode only (TAD =1,TAC=0).
- Open or shorted MR element. The MR bias is not disabled, see warning in Read Mode Description
- VCC & VDD supply voltage fault
- Invalid head select (i.e. HS2 = 1)

Write Mode

The polarity of the FLT output in write mode is programmable. If FPS = 0, the FLT pin goes high when a write fault is detected. If FPS = 1, the FLT output goes low when a write fault is detected. FPS = 0 is default state.

A fault is asserted on the FLT pin under one of the following unsafe conditions:

- An open head. Does not respond to frequency above 10MHz to avoid false alarm
- Shorted head to ground
- Write data frequency too slow.
- VCC or VDD supply voltage fault. – WR current will be turned off
- Invalid head select (i.e. HS2 = 1)

Servo Mode

A low on the FLT pin indicates the following unsafe condition:

- Chip temperature too high.
- VCC supply voltage fault.
- Fault reporting can be disabled through the serial port bit FLTDIS.

Idle Mode

A low on the FLT pin indicates the following unsafe condition:

- VCC supply voltage fault.

Sleep Mode

FLT Pull-up is disabled in sleep mode

VOLTAGE FAULT MONITOR

During power up or power fault condition, the voltage monitor disables the chip from any active mode. VCC fault monitor is active at any mode. The VDD fault monitor is active only in write mode to prevent false flag during servo bank write. The serial port has it's own power on reset circuit and serial data is cleared at VCC =1.6V nominal.

DIGITAL TEMPERATURE MONITOR

The digital temperature monitor is activated by setting MRM:TAD:DTM serial port bits to 0:0:1 in idle or read mode. An internal PTAT (proportional to absolute temperature) current is compared with a reference current set by the TA/DTM data register. The comparator output is monitored at the FLT output pin. To determine the chip temperature, the user increments the TA/DTM data register until the FLT output changes state. When the reference current is higher than the PTAT current, i.e. the set threshold temperature is higher than the chip temperature, the FLT pin flags low. The user can estimate the chip temperature based on the setting of the TA/DTM register when the FLT output changes state. One data bit corresponds to 2 °C.

TABLE 2: Thermal Asperity Modes

TAD	TAC	Thermal Asperity Mode
0	0	Off
1	0	TA Detection only
0	1	Retry mode (low corner frequency shift) when XMRBIAS/FAST = 1
1	1	On the Fly mode (low corner frequency shift when TA detected)

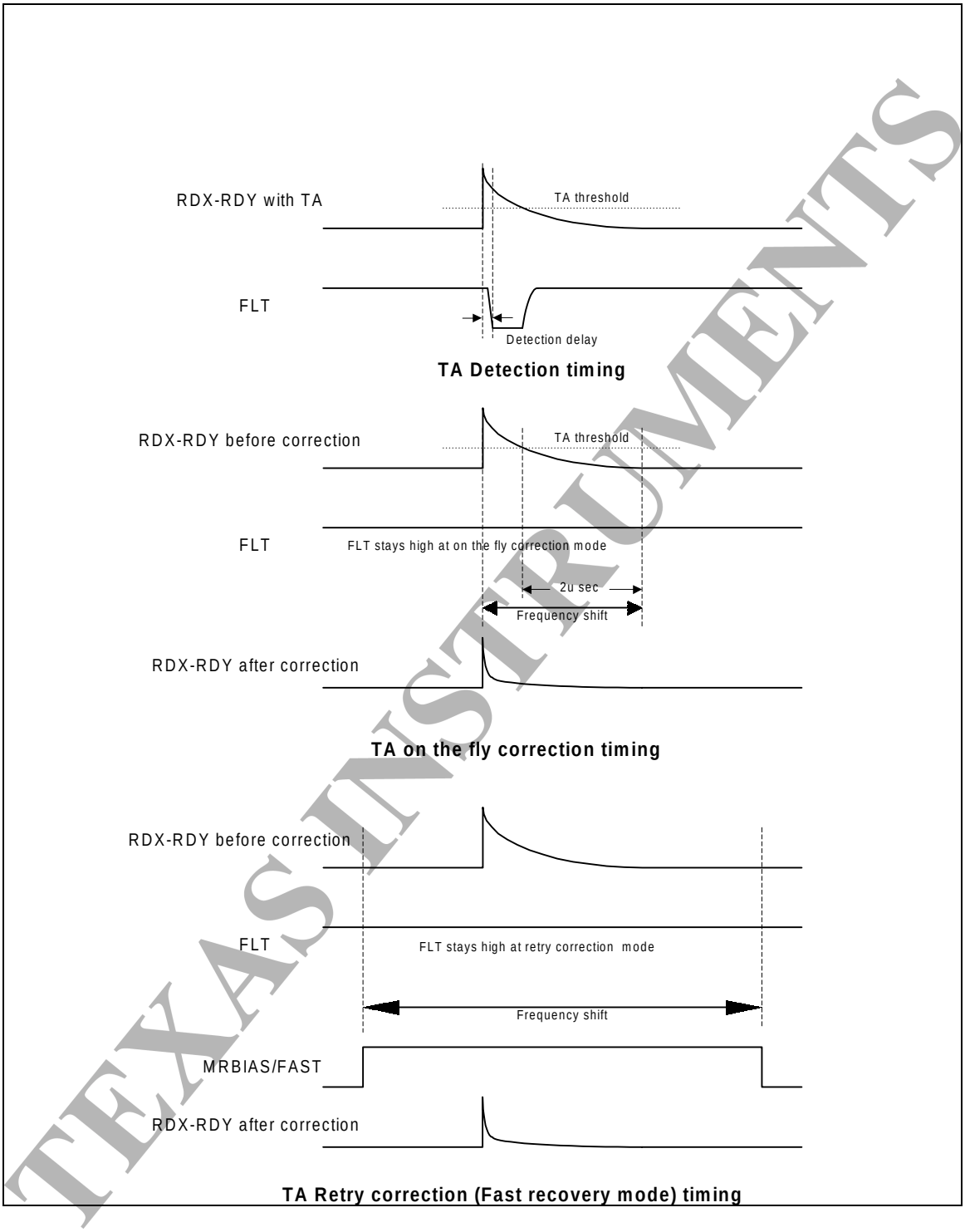


FIGURE 2: Thermal Asperity Modes

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bank write, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold and mode. The serial port bit map is shown in Table 3.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/W bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0, and S2=0 for R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map).

Asserting the serial port enable line SDEN initiates a transfer, SDATA is clocked into the internal shift register by the rising edge of SCLK. A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

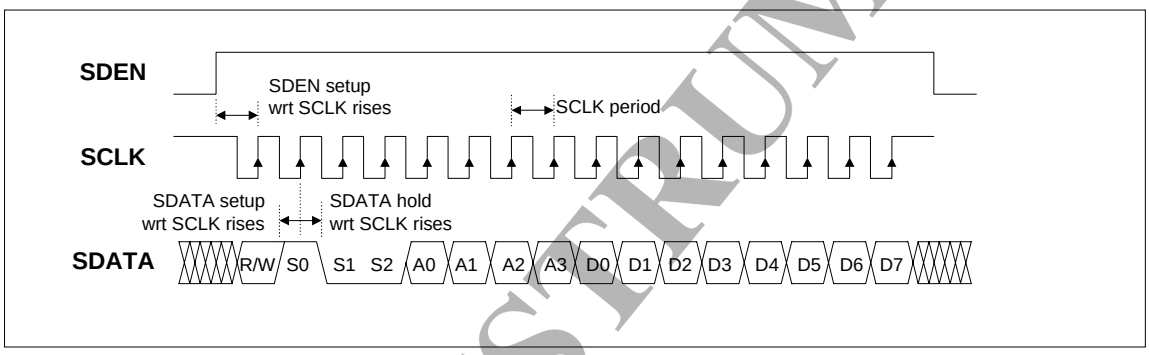


FIGURE 3: Serial Port Timing

TABLE 3: SR1710AFA Serial Port Bit Map (default values shown under each bit name)

Reg	S0:S2	A0:A3	D0	D1	D2	D3	D4	D5	D6	D7
ID	100	0000	VID = 1	VID = 0	PN0 **=N**	PN1 =0	PN2 =1	REV0 **=0**	REV1 **=1**	REV2 **=1**
HS/IMR	100	1000	HS0 =0	HS1 =0	(HS2) =0	IR0 =0	IR1 =0	IR2 =0	IR3 =0	IR4 =0
Write	100	0100	IW0 =0	IW1 =0	IW2 =0	IW3 =0	IW4 =0	WAC0 =0	WAC1 =0	**X** =0
TA	100	1100	TAC =0	DR0 =0	DR1 =0	TAD =0	HB0 =0	HB1 =0	HB2 =0	HB3 =0
TAD/DTM	100	0010	TB0 **=**0	TB1 **=**0	TB2 **=**0	TB3 **=**0	TB4 =0	TB5 =0	FPS =0	X =0
Mode	100	1010	XSLP =0	XIDL =0	GAIN =0	MRM =0	RB0 =0	SBW0 =0	**X** =0	POKB =0
FLT	100	0110	**FLT0** =0	**FLT1** =0	**FLT2** =0	DTM =0	MRB =0	X =0	BWR0 =0	**BWR1** =0
MISC	100	0001	FLTDIS =0	**OTMSK** =0	**WMRIB** =0	**TBLKH** =0	**GMENL** =0	**OCD** =0	**LGAIN** =0	**RES** =0
MISC2	100	1001	**BSTDIS** =0	**BST1** =0	**BST2** =0	**PLREN** =0	**RES** =0	**BSTK1** =0	**BSTK2** =0	**RES** =0

ID register is read only.
All Data bits are set to 0 at power-up, except ID register.
X = Not Used. Res = Reserved for TI internal use. User setting = 0
Bold indicates changes/additions from 32R1615AR
Register 7 not included in SR1710AFA.
ID(D2): N = 0 for 4-ch and = 1 for 2-ch and 1-ch

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port Read/Write bit is not shown.

ID REGISTER (READ ONLY REGISTER)
Address = 0000 001

BIT	NAME	DESCRIPTION
7:5	REV2:REV0	Chip revision. 110 = SR1710AFA4/2/1
4:2	PN2:PN0	Product Number. 100 = SR1710AFA-4 (4-Channel device) 101 = SR1710AFA2 and SR1710AFA1 (2-Channel and 1-Channel device)
1:0	VID	Vender ID. 01 is given for TI SPG devices.

HS/IMR REGISTER
Address = 0001 001

BIT	NAME	DESCRIPTION
7:3	IR4:IR0	MR bias current setting, see Read Mode description for bias equation. LSB = 0.2 mA 11111 = maximum MR bias current (8.2 mA) 00000 = minimum MR bias current (2 mA)
2	HS2	Reserved for HS2 for 8-channel device. HS2 = 1 causes Fault in 4/2/1- Ch.
1:0	HS1:HS0	Head Select bits, see Table 4 for head select bit maps.

WRITE REGISTER
Address = 0010 001

BIT	NAME	DESCRIPTION
7	X	Not Used. (Used to be WAC2)
6:5	WAC1:WAC0	Write Current Boost 11 = minimum write current boost 00 = maximum write current boost
4:0	IW4:IW0	Write current magnitude, see Write Mode description for equation. LSB = 1.45 mA 11111 = maximum write current (60 mA) 00000 = minimum write current (15 mA)

TA REGISTER
Address = 0011 001

BIT	NAME	DESCRIPTION
7:4	HB3:HB0	MR head protection bias voltage in read/write mode. LSB = 30 mV 1111 = Maximum head bias voltage (450 mV) 0000 = Minimum head bias voltage (off)
3	TAD	Thermal Asperity detector control 1 = Enable TA detector (when MRM = DTM = 0) 0 = Disable TA detector
2:1	DR1:DR0	Write damping resistor setting, 00, 01, 10 = Active damping only 11 = 150 Ω
0	TAC	Thermal Asperity Correction enable when high. Correction on the fly. 1 = TAC 1 = TAD Correction retry mode. 1 = TAC 0 = TAD

TAD/DTM REGISTER
Address = 0100 001

BIT	NAME	DESCRIPTION
7	X	Not Used
6	FPS	Write fault polarity 1 = Write fault indicated by FLT = low (No write faults: FLT = high) 0 = Write fault indicated by FLT = high (No write faults: FLT = low)
5:0	TB5:TB0	TA Detection threshold (TAD=1, MRM=0, DTM = 0) or Digital Temperature Monitor reference (TAD = 0, MRM = 0, DTM = 1) or DBHV threshold (TAD = 0, MRM = 1, DTM = 0) Note: only one function can be selected for this DAC at a time. Simultaneous mode enables will disable DAC. LSB = 30 mV (TA), = 2° C (DTM) 111111 = maximum threshold (TA = 1890 mV) 000000 = minimum threshold (TA = 0 mV)

MODE REGISTER
Address = 0101 001

BIT	NAME	DESCRIPTION
7	POKB	Power OK control bit (bi-directional). POKB low disables write mode. Both POKB and POK pin must be high for write mode activation. POKB will be set low by chip when POK pin transitions from high to low.
6	X	Not Used (SSD function of 32R1615_R removed from SR1710AFA)
5	SBW	Servo Bank Write Mode enabled when high in write mode.
4	RB0	Read frequency boost enabled when high.
3	MRM	MR Measurement Mode for digital BHV. Note: ABHV always active in read mode 1 = Enables digital MR measurement mode (TAD = 0, DTM = 0) 0 = Disables digital MR measurement mode
2	GAIN	Read Amplifier Gain select 1 = high gain mode 0 = low gain mode
1	XIDL	Idle Control Bit 0 = Idle mode enabled
0	XSLP	Sleep control bit 0 = Sleep mode enabled. Overrides all other control modes

FAULT REGISTER
Address = 0110 001

BIT	NAME	DESCRIPTION
7:6	BWR1:BWR0	Read Bandwidth reduction control TBD
5	X	Not Used
4	MRB	MR Bias control pin. Used in conjunction with XMRBIAS/FAST pin to control MR head bias modes. See Table 1.
3	DTM	Digital temperature monitor enable 1 = Enable temperature monitor (MRM =TAD =0) 0 = Disable temperature monitor
2:0	FLT2:FLT0	Fault status register. To clear Write all zeros. 000 = Writer open/short/no write current 001 = Write freq. too low 010 = Low VCC/VDD 011 = Invalid 100 = TA detect 101 = Open reader 110 = Short reader 111 = Over temp

HFW REGISTER (Does not physically exist in design)
Address = 0111 001

BIT	NAME	DESCRIPTION
7:0	RES	Reserved for future High Fly Write feature. Register not active on SR1710AFA

MISC REGISTER
Address = 1000 001

BIT	NAME	DESCRIPTION
7	TRIM	Reserved for TI Internal use.
6	LGAIN	Read Low Gain Control (GAIN = 0). Allows additional reduction of read gain. 1 = Read Gain = 100 V/V 0 = Read Gain = 150 V/V (default)
5	OCD	Reserved for TI internal use. (Offset correction disable).
4	GMENBL	High GM disable 1 = Disable High Gm mode 0 = Enable High Gm mode
3	TBLKH	W2R blanking time adjust 1 = Blanking time = 400 ns 0 = Blanking time = 200 ns
2	WMRIB	Write mode MR bias enable. Active only when MRB = 0 1 = Activates MR bias current in write mode. MR bias controlled by IR4:IR0 0 =No MR bias in write mode
1	OTMSK	Over temperature fault mask 1 = Disable over temperature fault 0 = Enable over temperature fault
0	FLTDIS	Fault Disable 1 = Disable all fault detection and reporting 0 = Enable all fault detection and reporting

MISC2 REGISTER
Address = 1001 001

BIT	NAME	DESCRIPTION
7	FUSE	Reserved for TI Internal use.
5,6	X	Not Used
4	ZE	Fuse Zap Enable Reserved for TI Internal use
3	PLREN	Reserved for TI Internal use.
1,2	BST1,BST2	Pole compensation adjust, effects reader bandwidth. BST1 BST2 0 0 = Default peaking 0 1 = 42.8% reduction in peaking 1 0 = 28.5% increase in peaking 1 1 = 14.3% increase in peaking
0	BSTDIS	Pole compensation disable

TABLE 4: Head Selection

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED		
				4-Ch	2-CH	1-Ch
0	0	0	0	None	None	None
0	0	1	1	1,3	1	n/a
0	1	0	2	0,2	0	0
0	1	1	3	All	All	All
1	X	X	Invalid	None		

NOTES:
1. HS2 = 1 will be reported as a fault.
2. On the 2 channel device, selecting heads 2 or 3 will result in an open head fault.
3. On the 1 channel device, selecting heads 1, 2 or 3 will result in an open head fault.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
XMRBIAS/ FAST	I	MRBIAS mode: MR bias current on: TTL, internal pull-down. Bias current active at low. FAST mode: TTL, internal pull down. FAST mode active at high.
HWnP, HWnN	O	Inductive write head connection.
HRn	I/O	MR read head connection, positive end.
HGND	I	MR head connection, negative end. Connect to system ground.
FLT/DBHV	O	Fault: A 3-volt logic compatible output. Fault mode: Read mode: A low indicates abnormal read condition. Write mode: A low (FPS = 1) or high (FPS = 0) indicates abnormal write condition. MR measure mode: DBHV comparator output. A high indicates the head voltage is higher than the set threshold. A low indicates the head voltage is lower than the set threshold. Servo write mode: A low indicates abnormal die temperature. Digital temperature monitor node: A low indicates the chip temperature is lower than the reference temperature.
R/XW	I	Read/Write: TTL, with internal pull-up.
RDP,RDN	O	Differential Read Data output.
GND	I	Ground
VCC	-	+5V power supply.
VDD	-	+8V power supply for write driver.
SDEN	I	Serial Port Enable. TTL/3.3V CMOS compatible, with internal pull-down.
SDATA	I/O	Serial Data. TTL/3.3V CMOS compatible, with internal pull-up.
POK	I	Power OK. A low disables write function. TTL/3.3VCMOS compatible with internal pull-up.
SCLK	I	Serial Clock. TTL/3.3V CMOS compatible, with internal pull-down.
WDP/WDN	I	Write Data input, PECL
ABHV	0	Analog Buffered Head Voltage Output.

ELECTRICAL SPECIFICATION

Unless otherwise specified, Rmr=50Ω Imr=5.20mA (setting value), Lwh=90nH, Rwh=18Ω, Iw=39.7mA (setting value).

ABSOLUTE MAXIMUM RATINGS

Operation beyond maximum ratings may result in permanent damage to the device.

PARAMETER		RATINGS
DC Supply Voltage	VCC	-0.3 to 6 VDC
DC Supply Voltage	VDD	-0.3 to 9 VDC
Logic Input Voltage	TTL	-0.3 to VCC + 0.3 VDC
	PECL	0 to VCC-.8
Write Current	Iw	120 mA
MR Bias Current	I	20 mA
Write Head Voltage	V	-0.3V to VDD+0.3 V
Read Head Voltage	V	0 to 1.2 V
Output Current	RDP,N	-10 mA
	FLT/DBHV	+8 mA
Storage Temperature	Tstg	-65 to 150 °C
Operating Junction Temperature	Tj	+135 °C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		RANGE
DC Supply Voltage	VCC	4.5 to 5.5 VDC
DC Supply Voltage	VDD_Write	7.2 to 8.8 VDC
	VDD_Servo	5.0 to 8.8 VDC
Write head load range	L	60 to 250 nH
Write head resister range	R	5 to 25 Ω
MR head range	R	25 to 80 Ω
Operating Ambient temperature	Ta	0 to 70 °C

POWER SUPPLY

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VDD Supply Current	I_{DD-R0}	Read, IMR off		TBD		mA
	I_{DD-R1}	Read, IMR on, Imr = 5.2 mA		15.6		mA
	I_{DD-W}	Write, Iw=40mA		66.3		mA
	I_{DD-S44}	Servo 4channel, Iw =30 mA		151		mA
	I_{DD-S2}	Servo 2channel, Iw =30 mA		TBD		mA
	I_{DD-IL}	Idle		10.1		mA
	I_{DD-SP}	Sleep		0.79		mA
VCC Supply Current	I_{cc-R0}	Read IMR off		TBD		mA
	I_{cc-R1}	Read IMR on, Imr = 5.2 mA		50		mA
	I_{cc-W0}	Write, Iw=40mA		42		mA
	I_{cc-S44}	Servo 4channel, Iw = 30 mA		83		mA
	I_{cc-S2}	Servo 2channel, Iw = 30 mA		TBD		mA
	I_{cc-IL4}	Idle		22		mA
	I_{cc-SP4}	Sleep		12.7		mA
VCC Fault Voltage		Write mode Iw<0.2mA		3.75		V
VDD Fault Voltage		Write mode Iw<0.2mA		6.4		V
VCC Fault Voltage		Clears serial data		1.6		V

DIGITAL INPUT/OUTPUT
(VCC refers to SR1710AF +5V power supply voltage)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R/XW, XMRBIAS, SDATA SDEN, SCLK						
Input High Voltage	V_{IH1}	3.3V Logic Cl=30pF	1.5		VCC+.3	VDC
Input Low Voltage	V_{IL1}	3.3V Logic Cl=30pF	-0.3		0.7	VDC
Input Hysteresis	V_{HYS}		100			mV
Pull-up Resistor (R/W,SDATA,POK)	R_{PU}			60		KΩ
Pull-down Resistor (SDEN,SCLK, XMRBIAS)	R_{PD}			60		KΩ
WDP, WDN						
Input High Voltage	V_{IH3}	PECL	1.3		VCC-0.9	VDC
Input Low Voltage	V_{IL3}	PECL	1.0		V_{IH3}-0.3	VDC
Input Δ Voltage			0.3	0.8	2.0	VDC
Input Current	I_{IH3}	Write mode ΔV_{IH3} =0.4V		2		mA
WD termination	R_{WDin}			110		Ω
FLT						
Output High Voltage	V_{OH}	I_{OH} = 0 mA	2.4	2.9	3.2	V
Output Low Voltage	V_{OL}	I_{OL} =2mA			0.5	V
Pull-up resistor				60		KΩ
SDATA (readback)						
Output High Voltage	V_{OH2}	3V CMOS	2.4		3.0	V
Output Low Voltage	V_{OL2}				0.8	V

SERIAL PORT TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read/Write						
SCLK Clock Period	T_C	Write operation	25			nS
		Read operation	40			nS
SCLK Low Time	T_{CKL}		5			nS
SCLK High Time	T_{CKH}		5			nS
Enable to SCLK	T_{SENS}		10			nS
SCLK to Disable	T_{SENH}		10			nS
Data Set-up Time	T_{DS}		5			nS
Data Hold Time	T_{DH}		5			nS
SDEN min. Low Time	T_{SL}		25			nS
SCLK fall to data valid	T_{SDV}	Read operation			17	nS
SDATA hold tim	T_{SDH}	Read operation	20			nS
SDEN fall to SDATA tristate	T_{SDTRI}	Read operation			20	nS

READ CHARACTERISTICS

Unless otherwise specified, Rmr=50Ω Imr=5.20mA (settling value), RDn/RDP load = 2KΩ diff.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		25	50	80	Ω
MR Bias Current Nominal Range		2		8.2	mA
MR Bias Current Resolution			5		bit
LSB			200		µA
MR Current Tolerance		-8		+8	%
MR Head DC Voltage Range		0.1		0.64	V
Unselected Head Current				10	µA
Input Resistance (RIN)	I-sense		5		Ω
Differential Voltage Gain	R_{MR} = 50Ω, Low Gain		150		V/V
f = 20 MHz, LGAIN = 0	R_{MR} = 50Ω, High Gain		220		V/V
Head to Head Gain Variation, f = 20 MHz	All heads Rmr = 50 Ω			2	%
Bandwidth	Lower -3dB		0.65	1	MHz
Rmr = 50 Ω, L = 45 nH	Higher -1dB		280		MHz
BWR1,BWR0 = 00	Higher -3dB, RB=0		330		MHz
	Higher -3dB, RB=1		TBD		MHz
Input Noise (Excludes RMR, includes current noise	R_{MR} = 50Ω, I-sense mode		0.72		nV/√Hz
Dynamic Range	THD @ Vin = 2 mV	40			dB
	THD @ Vin = 6 mV	20			dB
Output Offset Voltage		-100		100	mV
Output Current		2.5			mA
Output Voltage		1.3		2.7	V
Output Resistance	Single-ended		50		Ω
PSRR	Vin = 100 mV @ 15-40MHz	55	80		dB
VCC	Vin = 100 mV @ 40-300MHz	40	65		dB
PSRR	Vin = 100 mV @ 15-40MHz	55	80		dB
VDD	Vin = 100 mV @ 40-300MHz	40	65		dB
Channel Separation	Vin = 100 mV @ 15-40MHz	55	70		dB
	Vin = 100 mV @ 40-300MHz		55		dB

SECONDARY MR BIAS VOLTAGE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR head voltage bias range		0		0.45	V
Resolution			4		bit
LSB	Rmr = 50 Ω		30		mV
Absolute tolerance	Rmr = 50 Ω	-25		25	%

MR BIAS OVERSHOOT/UNDERSHOOT

All MR bias switching done with Imr = 5.2 mA

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
MR bias overshoot	Iosbir	Idle to read		0		%
MR bias undershoot	Iusbir	Idle to read		0		%
MR bias overshoot	Iosbri	Read to idle		0		%
MR bias undershoot	Iusbri	Read to idle		0		%
MR bias overshoot	Iosvfr	VCC fault to read		0		%
MR bias undershoot	Iusvfr	VCC fault to read		0		%
MR bias overshoot	Iosvdfr	VDD fault to read		0		%
MR bias undershoot	Iusvdfr	VDD fault to read		0		%
MR bias overshoot	Iosrwe	Read to write with bias on		0		%
MR bias undershoot	Iusrwe	Read to write with bias on		0		%
MR bias overshoot	Ioswrd	Write to read with bias off		0		%
MR bias undershoot	Iuswrd	Write to read with bias off		0		%
MR bias overshoot	Ioswre	Write to read with bias on		0		%
MR bias undershoot	Iuswre	Write to read with bias on		0		%
MR bias overshoot	Ioshs	Head switch, no bias change		0		%
MR bias undershoot	Iushs	Head switch, no bias change		0		%
MR bias overshoot	Iosc	Bias cycling		0		%

WRITE/SERVO CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Nominal Range	DR1:0 = 00. See note	15		60	mA
Write Current Resolution			5		bit
LSB			1.45		mA
Write Current Accuracy Single Channel	DR1:0 = 00.	-8		+8	%
Nominal Write Current Range, Servo Mode	4-heads, Vdd = 5 VDC	15		47	mA
Write Current Accuracy Servo Channel	DR1:0 = 00.	-8		+8	%
Head Voltage Swing	Open Head, Vdd = 8 VDC		7.5		Vpp
	Transient, Vdd = 8 VDC		10.4		Vpp
	Open Head, Vdd = 5 VDC		4.5		Vpp
	Transient, Vdd = 5 VDC		6.0		Vpp
Unselected Head Current	DC			100	µA
	Transient			1	mApk
Write Current Matching	Servo mode, channel to channel variation from mean			10	%

NOTE: Write current will reduce to Iw/(1+Rh/Rd) when DR1:0 = 11, where Rh is the write head resistance and Rd is the programmed damping resistance = 150 Ω.

HEAD VOLTAGE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DBHV threshold resolution			6		bit
DBHV minimum threshold			0		mV
LSB			30		mV
DBHV Threshold accuracy	DAC setting = 4 to 16, after offset compensation	-8		+8	%
ABHV gain		4.7	5	5.3	V/V
ABHV output range		0.4		2.4	V
ABHV output current	Output drops to 90%	0.5			mA
ABHV output offset	Vin=0.40 V	-100		+100	mV
ABHV clamp voltage	Vin>0.506V		2.4	2.8	V
MR head short detect threshold			50	75	mV
MR head open detect threshold			470		mV

THERMAL ASPERITY DETECTION/CORRECTION/FAST RECOVERY

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TA Detection Resolution			6		bit
TA Detection Minimum threshold	Relative to average of RDP output peak prior to correction		10		mV
TA Detection Threshold, Nominal Range	Relative to average of RDP output peak prior to correction	10		1700	mV
TA Threshold LSB	Ref=2kΩ	22.5	30	37.5	mV
Lower Corner Frequency	TAC = 1		4.3		MHz
TA Detection Delay	TAD = 1		37	100	ns
TA correction delay	TAC:TAD = 11		0.4	1.0	µs
TA correction timer	TAC:TAD = 11		1.8		µs

SWITCHING CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write to Read Switching	90% signal envelope, ±30mV DC		200	400	ns
Read to Write Switching	90% of Iw		25	50	ns
	90% of Iw, Servo write, room temp			50	ns
Read, MR bias off to on (see Note)	90% signal envelope, ±30mV DC, HB = 0, Imr = 5.2 mA		0.24	0.5	µs
Idle to Read Switching	90% signal envelope, ±30mV DC		1	TBD	µs
Read to Idle Switching	10% of read envelope			0.6	µs
Head Switching	90% signal envelope, ±30mV DC		1	10	µs
Iw rise/fall time 10% to 90% Single Channel	Lh=72nH, Iw=40mA, Vdd=8V Lh=90nH, Iw=40mA, Vdd=8V Lh=108nH, Iw=40mA, Vdd=8V		0.5 0.75 0.95	TBD	ns
Servo	Lh=72nH, Iw=30mA, Vdd=5V Lh=90nH, Iw=30mA, Vdd=5V Lh=108nH, Iw=30mA, Vdd=5V		0.8 1.0 1.15	TBD	ns
Iw transient undershoot	Lh = 90 nH, Iw = 40 mA		5		%
Head Current Delay TD3	50% of WD to 50% of Iw			10	ns
Write Current Asymmetry	Propagation delay difference 50% duty cycle write data T=2.5ns, minumum overshoot DR0 = 1, DR1 = 1, WAC0 =1, WAC1 = 1.			100	ps

NOTE: MR bias switch time measures from Vbias to Ibias mode assuming Ibias C1 cap fully charged before switching to Vbias mode. (i.e. sequence is Ibias-to-Vbias-to-Ibias)

WRITE UNSAFE DETECTION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FLT safe to unsafe TD1	Low Frequency Write Data	0.5	1	2	µS
FLT unsafe to safe TD2				200	nS
Write data frequency	Valid transient detector			400	MHz
	Valid Open detector (50% duty cycle)			10	MHz

OVER TEMPERATURE DETECTION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Over temperature detection threshold	Servo Mode, FLT = low		135		°C

TEMPERATURE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Digital temperature monitor					
Resolution			6		bit
LSB			2		°C
Temperature range		0		126	°C
Temp diode voltage	Ta = 25 C		TBD		V

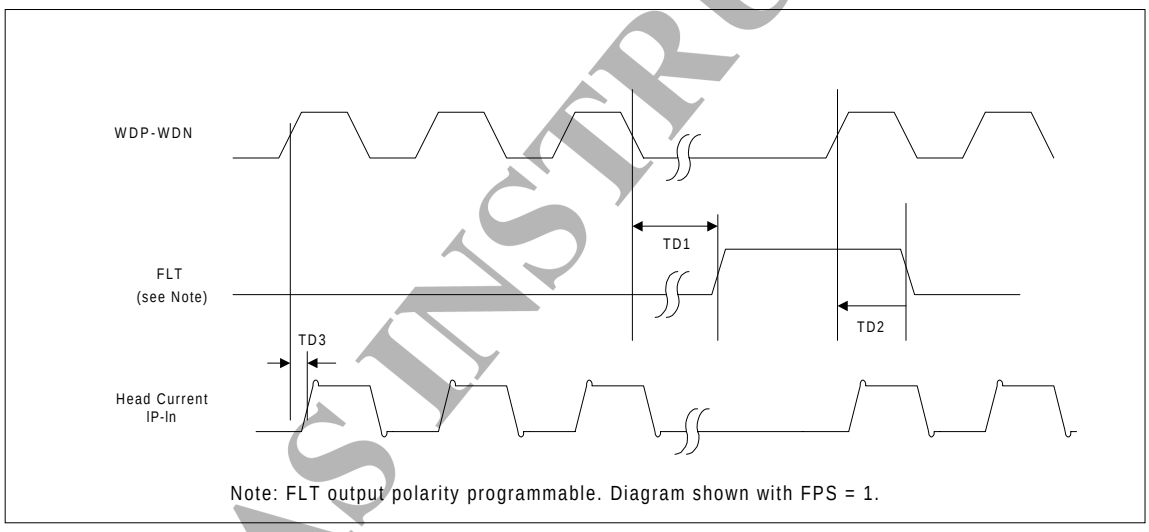
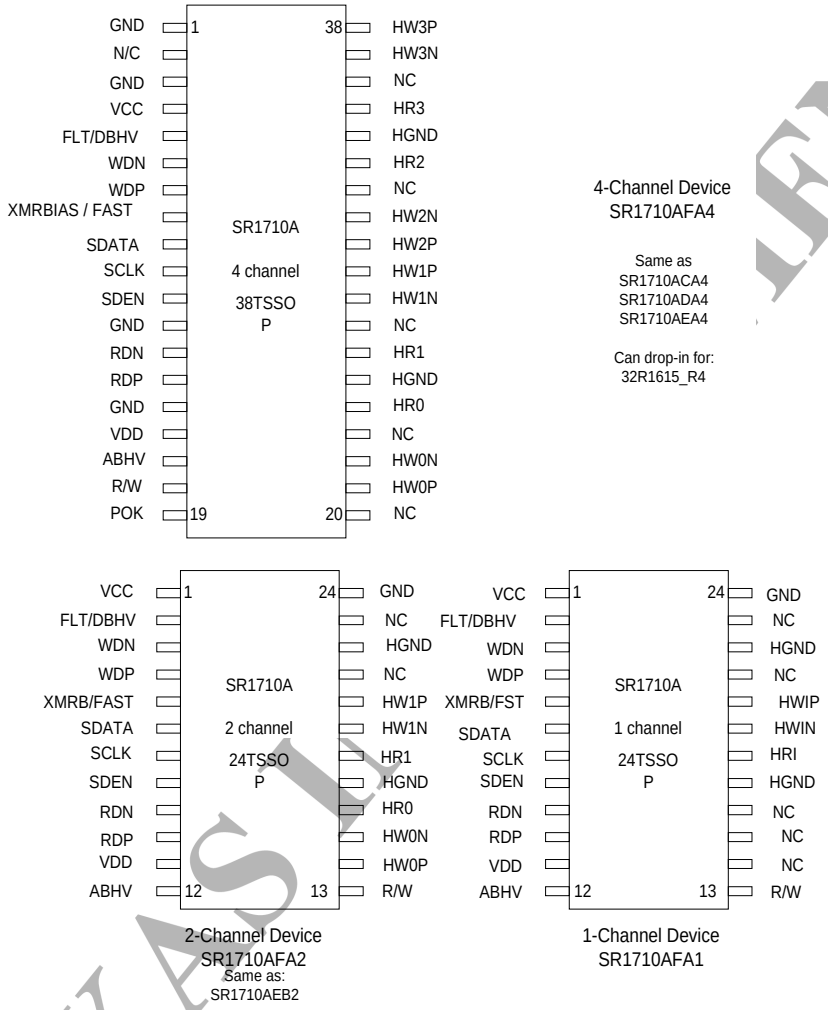


FIGURE 4: Write Current & Head Unsafe Timing

PACKAGE PIN DESIGNATIONS



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Abridged Version

SR1720DDA

MR READ/WRITE DEVICE

Target Specification

May, 2000

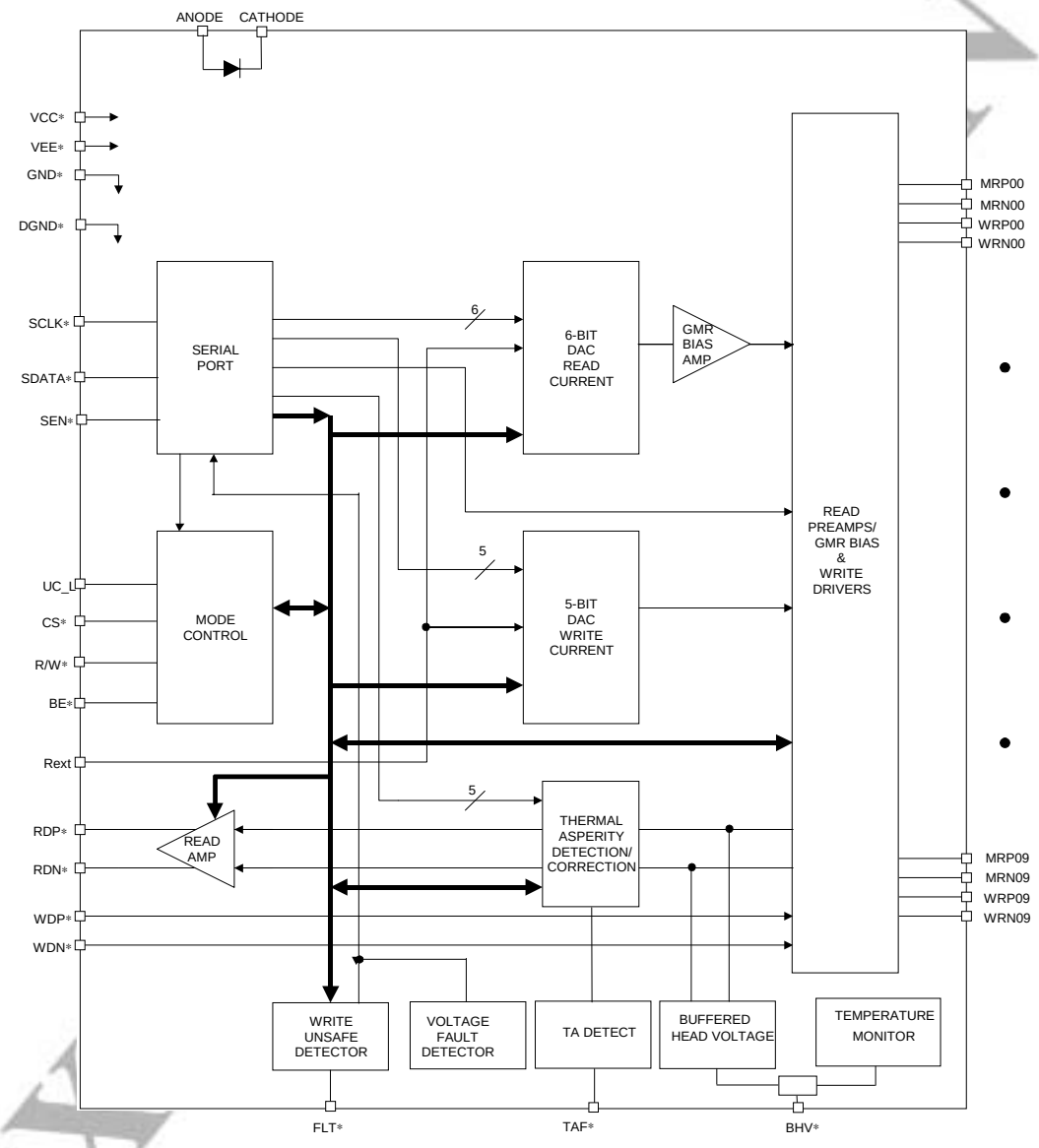
DESCRIPTION

The TI SR1720DDA is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. It provides a write driver, low noise read amplifier and MR current bias with serial port controlled head selection, servo track write, write current, MR read bias current, thermal asperity threshold and fault detection circuitry for up to ten channels. In servo write mode, 3 channels each can be separately selected. Required external components are minimized by integrating the reader coupling capacitors onto the die. The device requires +5V and -5V and comes in die form or 100-pin TQFP package.

FEATURES

- **+5V ±10%, -5V ±10% supplies**
- **Designed for four-terminal MR heads**
- **Requires only one external resistor**
- **Truly differential current bias / voltage sense MR read Amplifier**
- **GMR head bias current range = 2 – 8.23 mA**
- **MR head resistance range of 30-80 Ω**
- **Programmable MR read gain (150, 200, 250, or 300 V/V)**
- **Programmable voltage BW (Min, 175 MHz - 350 MHz)**
- **MR read input noise = 0.5 nV/√Hz (Typ, R_{mr}=0Ω)**
- **MR read input current noise = 6pA/√Hz @ 6.4 mA (Typ)**
- **MR read input resistance = 1K Ohm (Typ)**
- **PECL write data input**
- **Head voltage swing = 16 Vp-p (Typ)**
- **Head Current risetime of 0.55 ns (Typ, I_w=50mA, L_{tot}=70nH, R_H=12Ω)**
- **Programmable peak overshoot control**
- **Write current range = 26.7 - 71.7 mA**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Read/Write serial port controls head selection, write current, write overshoot, MR head bias current, thermal asperity threshold and mode, read gain, low power mode selection.**
- **Buffered head voltage**
- **Thermal asperity detection and compensation**
- **MR head capacitive discharge protection**
- **On chip Temperature Monitor**

BLOCK DIAGRAM



* MAY BE OR TIED TOGETHER IN A DUAL PREAMP APPLICATION

FUNCTIONAL DESCRIPTION

The TI SR1720DDA addresses up to 10 four-terminal GMR heads providing write drive or read bias and amplification. Mode control is accomplished with different combinations of the real-time control pins and the control and bits of serial port register 1 as summarized in Table 1. All inputs, except the serial port and BE, have internal pull-ups to Vcc so that when left open, they will default to the HIGH state. The three serial port I/O pins and BE have internal pull-downs.

The serial data port is used to control head selection, servo track write, write current, write damping control, MR head resistance measurement, MR bias current, read gain, thermal asperity threshold and mode.

Setting the CS pin LOW places the preamp into its normal power up state. A HIGH level forces the preamp into IDLE mode. The CS pin is logically OR'd with the IDLEOVR bit in register 1. The CS pin is internally pulled up to Vcc. The polarity of the CS pin can be inverted by programming CSPOL (bit D5 in register 0) HIGH. The power on reset value of CSPOL is LOW.

In a dual preamp application, the UC_L pin is used to determine which preamp responses to the lower or upper block of head select addresses. When UC_L is HIGH or left open, preamp channels 0-9 map to head select values 0-9. When UC_L is LOW, preamp channels 0-9 map to head select values 16-25. UC_L may be overridden with the WSER bit in register 1 to allow for dual chip servo write operation.

CHIP SELECTION

TABLE 1: Mode Select
Single preamp application. UC_L is HIGH.

MODE	CS (pin)	R/W *(pin)*	BE (pin)	WSER (SP bit Reg 1)	BIAS OVR (SP bit Reg 1)	IDLE OVR (SP bit Reg 1)	Iwc	MR bias in selected head
IDLE	X	X	X	X	X	1	OFF	OFF
IDLE	1	X	X	X	X	X	OFF	OFF
READ-INACTIVE	0	1	0	X	0	0	OFF	OFF
READ	0	1	1	X	X	0	OFF	ON
READ	0	1	X	X	1	0	OFF	ON
WRITE	0	0	1	0	X	0	ON	ON
WRITE	0	0	X	0	1	0	ON	ON
WRITE	0	0	0	0	0	0	ON	OFF
SERVO WRITE	0	0	X	1	X	0	ON	OFF

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, servo track write, write current, MR read bias current, read gain, thermal asperity threshold, fault detection, and operational mode. The serial port bit map is shown in Table 2.

TABLE 2: Serial Port Register Map

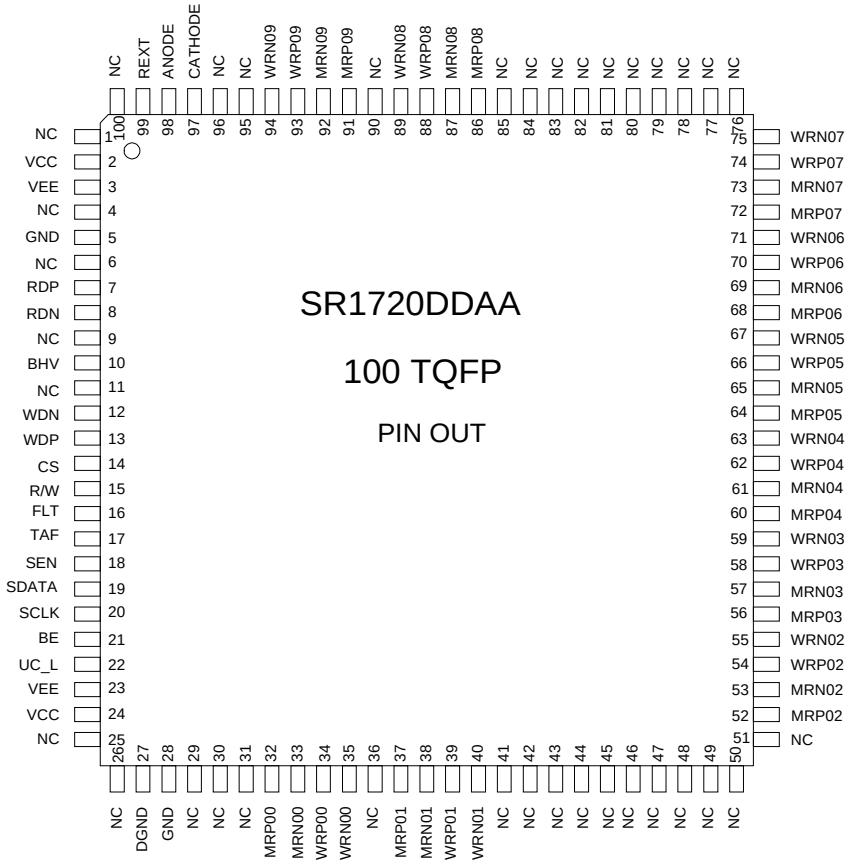
Register	D7	D6	D5	D4	D3	D2	D1	D0
0	X	X	CSPOL	HS4	HS3	HS2	HS1	HS0
1	TEST1	TEST0	BHVOE	PWREN	WSER	BIASOVR	IDLEOVR	CLR
2	WCO2	WCO1	WCO0	WC4	WC3	WC2	WC1	WC0
3	X	X	RB5	RB4	RB3	RB2	RB1	RB0
4	TALFO	LFC1	LFC0	X	BW1	BW0	GAIN1	GAIN0
5	TADOUT	TACEN	TADEN	TAL4	TAL3	TAL2	TAL1	TAL0
6	X	MRBHI	TAD	WHDO	WHSG	WDFL	LVRD	LVWR
7	FSR3	FSR2	FSR1	FSR0	FSW3	FSW2	FSW1	FSW0
8	X	DWE	UCE	LCE	UC1	UC0	LC1	LC0
9	X	X	CHNL	VRV2	VRV1	VRV0	VID1	VID0
10	HTFW11	HMR11	HTFW10	HMR10	HTFW9	HMR9	HTFW8	HMR8
11	HTFW7	HMR7	HTFW6	HMR6	HTFW5	HMR5	HTFW4	HMR4
12	HTFW3	HMR3	HTFW2	HMR2	HTFW1	HMR1	HTFW0	HMR0
13	X	X	X	X	X	X	BOOST1	BOOST0
15	Res	Res	Res	Res	Res	Res	Res	Res

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
R/W	input*	Read/Write: a high level enables the read mode.
CS	input	Chip Select. Low places preamp into normal power up state. Logically OR'd with IDLEOVR bit in Reg 1.
UC_L	input	Used in dual preamp configuration. Low maps head select values 0-9 to 16-25. WSER bit in Reg 1 overrides for servo write.
BE	input*	Bias Enable. High enables bias current to selected head. Logically OR'd with BIASOVR bit in Reg 1.
SEN	input*	Serial Enable line. Active High.
SCLK	input*	Serial Clock line. 40 MHz max.
SDAT	input*	Serial Data line. Bi-directional interface
FLT	output*	Fault. Signals High when a fault is detected. Open collector.
WDP, WDN	input*	Differential PECL . Internally terminated with 300 Ω
TAF	output*	Thermal asperity detected flag. Open collector
MRP00-MRP09	input	MR head connections, positive end
MRN00-MRN09	input	MR head connections, negative end
WRP00-WRP09	output	Write head connections, positive end
WRN00-WRN09	output	Write head connections, negative end
RDP,RDN	output*	Read Data, Differential read signal outputs
Rext	output	10KΩ external resistor to ground for current reference
BHV	output*	Buffered DC voltage across selected read head. Valid when BHVOE = 1.
VEE	input*	-5V supply
GND	input*	Ground
VCC	input*	+5V supply

* When more than one device is used, these signals can be wire OR'd together

PACKAGE PIN DESIGNATIONS



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SR1730ABA
+5/-5V 4/8-CHANNEL MR READ/WRITE DEVICE

Preproduction

May, 2000

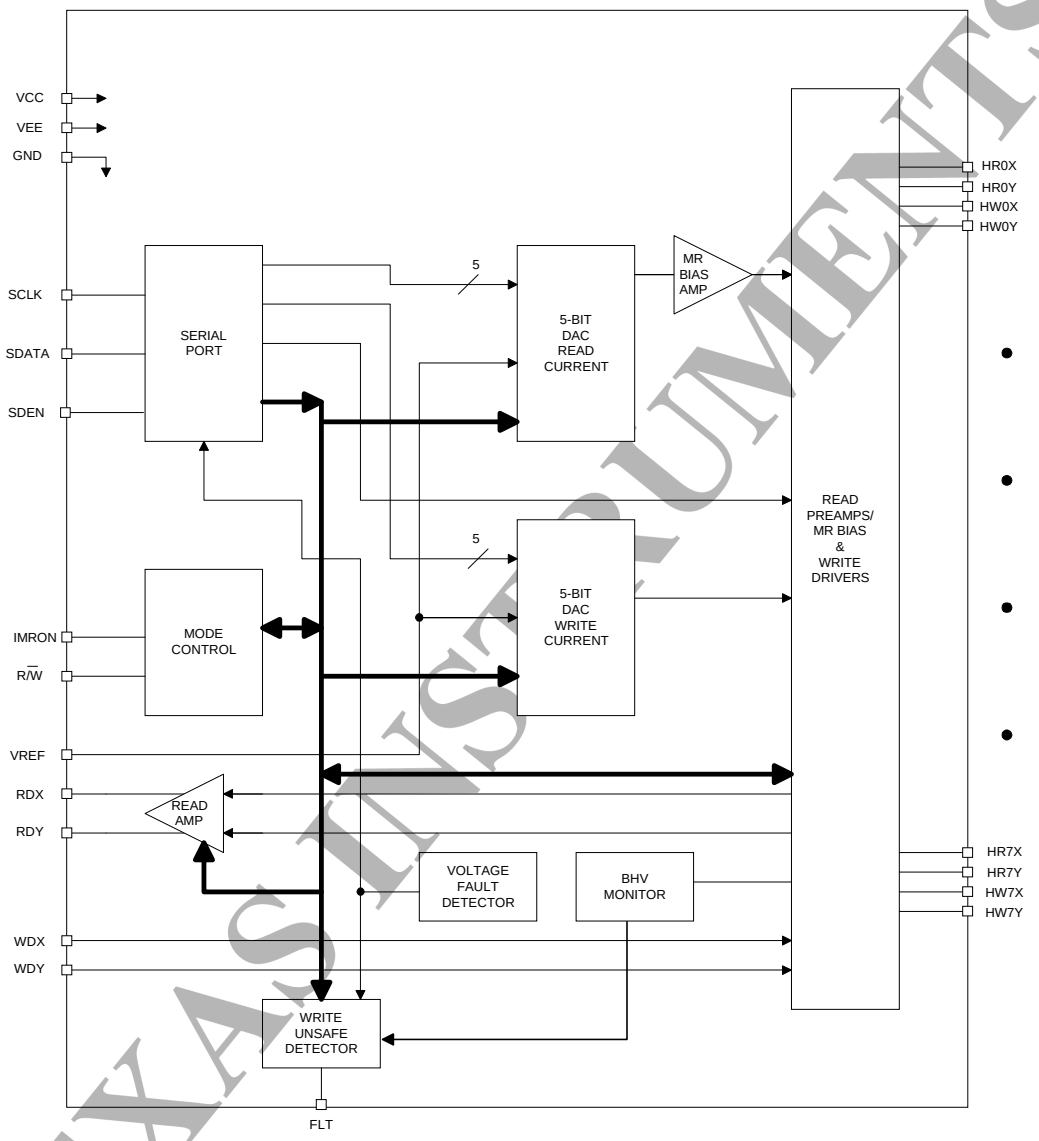
DESCRIPTION

The TI SR1730ABA is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. The reader architecture is MR current bias/voltage sense and will support a user data rate of up to 500 Mbits/sec. A read/write capable serial port is provided to enable the implementation of on-chip MR bias and Write current DACs. The device provides a write driver, low-noise read amplifier, serial port controlled head selection, write current, MR read bias current and read and write fault detection circuitry for up to eight channels. The device requires +5V and -5V and comes in die form or in a 48-pin TQFP package.

FEATURES

- **+5V ±10%, -5V ±10% supplies**
- **Designed for four-terminal MR heads with minimum external components**
- **DC blocking capacitors integrated on chip**
- **Truly differential current bias/voltage sense MR read Amp**
- **MR head bias current range = 2.1 – 9.6 mA (5-bit)**
- **MR read gain = 93 V/V and 137 V/V @ 45 Ω**
- **MR read input noise = .70 nV/√Hz @ 45 Ω**
- **Read bandwidth = 300 MHz**
- **Differential PECL write data input, 3V logic compatible**
- **Head voltage swing = 12 Vp-p**
- **Write current range = 15.8 - 63 mA (5-bit)**
- **Write current rise/fall time = 0.8 ns (Lh = 80 nH, Rh = 11 Ω, 50% boost)**
- **Servo bank write capability**
- **Read and write unsafe detection**
- **Thermal asperity detection and fast recovery**
- **Power supply fault protection**
- **Serial port controls head selection, write current, MR read bias current**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The TI SR1730ABA addresses up to 8 four-terminal MR heads providing write drive or read bias and amplification. TTL pins R/W and XIMRON, and serial port register bits control the operational mode as shown in Table 1. The R/W and XIMRON inputs have internal pull-up resistors so that when left opened, it will default to the TTL High state.

The three-line serial data interface, with both read/write capability, is used to control head selection, write current, MR bias current, and mode control. The serial data port includes 4 read/write capable data registers and 1 read only ID register. See Serial Interface Operation for description of the serial port operation. The three serial interface pins, SDEN, SDATA and SCLK, have internal pull-down resistors.

TABLE 1: Mode Select

XSLP	XIDL	R/W	XIMRON	BNK0	BNK1	Write Current	MR Current	Mode
1	1	1	0	X	X	OFF	ON	Read Mode
1	1	1	1	X	X	OFF	OFF	Read-Inactive
1	1	0	0	0	0	ON	ON	Write Mode (RBAW)
1	1	0	1	0	0	ON	OFF	Write Mode
1	1	0	X	1	1	ON	OFF	Servo Mode
1	0	X	X	X	X	OFF	OFF	Idle Mode
0	X	X	X	X	X	OFF	OFF	Sleep Mode

NOTE: XSLP, XIDL, BNK0, BNK1 are serial port register bits

WRITE MODE

In write mode, the write current is enabled to the selected channel, write data controls the write current polarity, and the FLT output is driven. Enabling the reader bias current is independent of this mode and is referred to as Read Bias Active in Write mode (RBAW). MR bias current is enabled by placing XIMRON input to a low logic state. Device power consumption is reduced when the MR bias is disabled. The read outputs, RDX/RDY, are set to a high impedance state during write mode.

The FLT output is LOW in this mode unless there is a write fault, which causes the output to go HIGH.

Referring to Table 1, selecting write mode configures the internal 5-bit write current DAC, programmable via serial port. Head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each transition of the differential PECL signal WDX-WDY; WDX>WDY will cause Iw to flow from X to Y. The WDX/WDY write data input includes a 130 Ω differential termination resistor.

The magnitude of the current (0-pk) is set by 5-bit DAC as below:

$$Iw\ (mA) = 15.8 + n * LSB$$

where the LSB = 1.522 mA and n = 0, 1 .. 31 is decimal value of 5-bit write current register bits IW0:IW4.

The SR1730ABA includes overshoot and undershoot control. 3 bits of write boost control (WCB2:WCB0), 3 bits of undershoot control (USC2:USC0), and 3 bits of write boost delay(WBD2:WBD0) provide means to optimize the write current waveshape.

SERVO BANK WRITE MODE

The SR1730ABA includes servo bank write capability, which allows multiple heads to be written simultaneously. Servo bank write mode is enabled by setting the BNK0 and BNK1 serial port bits to 1, followed by placing the R/W pin low. Note that the servo control bits are located in two different serial port registers to prevent accidental servo bank write activation. If only one of the two servo enable bits are set in write mode (BNK0 and BNK1), a write fault is produced.

Upon entering servo bank write mode, the device will concurrently enable the write current to the

selected heads. The activated heads in servo mode are determined by register bits HS2:HS0 as shown in Table 4.

Write current in servo bankwrite mode is controlled with the WC4:WC0 bits as in regular write mode, although the maximum expected write current in bankwrite mode is 35 mA 0-pk (TBD). The user is responsible for controlling the write duty cycle and environment in bankwrite mode to limit power dissipation and junction temperature.

The MR bias current is disabled in bankwrite mode regardless of the state of the XIMRON pin. Although only voltage faults are detected in bankwrite mode, write current is not disabled by a voltage fault condition.

READ MODE

In normal read mode, bias current is enabled to the selected head, the chip drives the RDX/RDY read signal outputs, and the FLT output is active.

The FLT output is HIGH in this mode unless there is a read fault, which causes the output to go LOW.

Referring to Table 1, selecting read mode activates the MR bias current generator and low-noise differential amplifier. The outputs of the read amplifier, RDX and RDY, are emitter followers and are in phase with the resistivity change at the selected input ports, HRnX and HRnY, where the respective MR head is attached. The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port. The DAC reference current is set by an external resistor 2.0 K Ω at pin VREF = 2.0V. The magnitude of the bias current is set according to the following equation:

$$I_{MR}\ (mA) = 2.1 + n * LSB, \text{ with } Rmr = 45\ \Omega,$$

where LSB = 242 μA and n = 0, 1 . . . 31, is the decimal value of the 5 bit serial port register bits IMR4:IMR0.

The resistance of the MR element has an effect on the actual MR bias current. The following equation can be used to determine the magnitude of the MR bias current with Rmr values other than 45 Ω:

$$I_{MR}\ (mA) = 136 * \frac{(n + 8.7)}{(520 + Rmr)},$$

where n = 0, 1 . . . 31, is the decimal value of the 5 bit serial port register bits IMR4:IMR0. The SR1730ABA is designed such that a Rmr of 45 Ω results in the specified MR bias range of 2.1 –9.6 mA.

The read amplifier's DC blocking capacitors and noise capacitor are integrated on the device, no external capacitors are required for the read circuit.

In Read mode, the voltage at the midpoint of the selected MR head is forced to the ground potential. For the unselected MR heads, the head ports become high impedance and thus will prevent the heads from conducting current in the event of head to disk contact.

To improve the write to read recovery time, the MR bias current can be activated during Write mode. With the MR bias current turned on, the voltage change across the internal DC blocking capacitors between write and read modes will be minimized which will result in faster write to read recovery time. Placing the XIMRON pin low enables the MR bias.

READ-INACTIVE MODE

Similar to read mode, but the MR bias current is diverted to an internal dummy resistor. The chip is in its normal power consumption mode. The FLT output is a constant LOW during this mode.

Read-inactive mode is entered when the MR bias current is disabled. Recovery time from this mode to Read mode will be no longer than the worst-case head-switch time.

The AC read signal output in this mode is undefined. The DC read signal outputs should be the same as in normal read mode in order to facilitate fast recovery to read mode.

IDLE MODE

Taking serial port bit XIDL low selects idle mode. In this mode, all outputs are disabled, with the reader and writer sections put into a reduced power consumption standby mode. The chip does not drive any of the outputs in this mode.

MR bias current is diverted to an internal dummy head to keep the DC blocking and noise filter caps biased properly, and all critical nodes on the chip will remain biased to facilitate quick recovery from this mode. Recovery form Idle mode to Read mode is expected to be no longer than the worst-case head

switch time. Recovery from this mode to write mode is not specified.

SLEEP MODE

Taking serial port bit XSLP low selects sleep mode. Sleep mode is equivalent to idle mode on the SR1730ABA.

POWER SUPPLY FAULT PROTECTION

During a power up condition, the power-on voltage monitor disables the chip from any active mode. The serial data registers are reset to sleep mode with default power-on setting values. The threshold voltage for the serial port power-on reset is 1.8 V (typical). The threshold voltage for a VCC or VEE fault which also disables the normal write mode but does not reset the serial port registers is 3.85V (typical, with hysteresis).

FAULT OPERATION

The FLT pin flags a fault condition in the read or write modes:

Read Fault Detection

A logic low on the FLT pin indicates a read fault condition. A read fault may be any one of the following conditions:

- Open MR element
- Shorted MR element
- Thermal asperity detected
- Low Vcc or Vee
- Illegal head selection (if applicable)
- MR bias current disabled by XIMRON = 1

Write Fault Detection

A logic high on the FLT pin indicates a write fault condition. A write fault may be any one of the following conditions:

- Low write data
- Head shorted to ground
- Illegal head selection (if applicable)
- Open write head,
- Low Vcc or Vee. Disables write current except in servo bank write mode.

Write Open Head Bench Testing

To test for a write open head, first place the preamp into read mode. While monitoring the Fault status pin, switch the preamp into write mode. If a head does not exist or is open, the Fault line will transition from Low to High. The preamp must be placed back into read mode in order to reset the Fault line.

The write open head detection circuitry will not work properly if head switching is performed while in write mode. To check a different write head for an open, first switch the preamp from write into read mode, then switch to the head of interest, finally place the preamp into write mode again. This procedure should be followed for subsequent heads.

MR MEASUREMENT MODE

The SR1730ABA includes a special test mode for making MR resistance measurements. This mode utilizes the Digital Buffered Head Voltage (DBHV) function. The test mode is activated when serial port bit MRM is set. When MRM is enabled, the FLT pin becomes the output of a window comparator that monitors the MR head voltage (Imr * Rmr). A LOW at the FLT output indicates the MR head voltage is outside the specified window. By adjusting the MR bias current, and knowing the fixed thresholds of the DBHV window, the resistance of the MR element can be calculated.

THERMAL ASPERITY DETECTION AND FAST RECOVERY

Thermal asperity detection is enabled by setting the TAD bit = 1. When activated, thermal asperity detection will flag a thermal asperity event whenever the RDX-RDY output signal exceeds the programmed threshold. A thermal asperity event will cause the FLT output to go LOW and it will remain low until the RDX/RDY output signal falls below the programmed threshold level plus some hysteresis. The TA threshold level can be programmed as follows:

TAth (mV) = $50 + 900 \bullet \frac{n}{15}$, where n = 0,1…15 is the decimal value of the 4 serial port register bits TAD3:TAD0.

A thermal asperity data retry feature called Fast recovery mode is available. The FRON serial port bit controls fast recovery mode. In Fast recovery mode the low frequency highpass cutoff point switches from 1.0 MHz (typical) to 3.5 MHz (typical), reducing the low frequency content of the readback signal.

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and thermal asperity threshold and mode. The serial port bit map is shown in Table 2.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/W bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0, and S2=0 for R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map).

Asserting the serial port enable line SDEN (TTL) initiates a transfer, SDATA (TTL) is clocked into the internal shift register by the rising edge of SCLK (TTL). A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

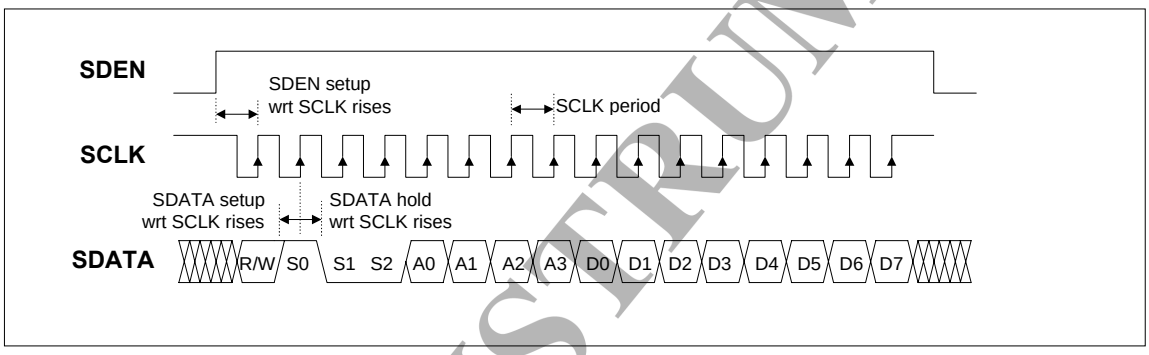


FIGURE 2: Serial Port Timing

TABLE 2. Serial Port Bit Map

Reg	A3:A0	S2:S0	D7	D6	D5	D4	D3	D2	D1	D0
ID	0000	001	0	CH	VS2	VS1	VS0	0	0	1
HS/IMR	0001	001	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
WRITE	0010	001	BNK0	X	X	IW4	IW3	IW2	IW1	IW0
TA	0011	001	TA3	TA2	TA1	TA0	TADET	WCB2	WCB1	WCB0
MODE	0100	001	WTDD	BNK1	FRON	X	MRM	GAIN	XIDL	XSLP
USC	0101	001	X	X	X	X	X	USC2	USC1	USC0
WBD	0110	001	X	X	X	X	X	WBD2	WBD1	WBD0

Register map not displayed in order of bit transfer.
ID register is read only.
X = Not Used
All Data bits are set to 0 by at reset condition, i.e. power-up or POR voltage fault condition, except ID register.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port Read/Write bit is not shown..

ID Register (Read Only Register)
Address = 0000 001

BIT	NAME	DESCRIPTION
7		ID bit = 0, internally set by TI SPG
6	CH	Channel version 1 = 4 channel version 0 = 8 channel version
5:3	VS2:VS0	Device revision bits. Revision for SR1730ABA is 001
2:0		ID bits = 001, internally set by TI SPG

HS/IMR Register
Address = 0001 001

BIT	NAME	DESCRIPTION
7:3	IR4:0	MR bias current setting, see Read Mode description for bias equation. LSB = 0.242 mA 11111 = maximum MR bias current (9.6 mA) 00000 = minimum MR bias current (2.1 mA)
2:0	HS2:HS0	Head Select bits, see Tables 3 and 4 for head select bit maps

Write Register
Address = 0010 001

BIT	NAME	DESCRIPTION
7	BNK0	Servo Bank control bit, operate in conjunction with BNK1 in Mode Register 1 = Servo Bank mode (both BNK0 and BNK1 must be 1 to enable Servo) 0 = Servo Bank mode off
6:5	X	Not Used
4:0	IW4:0	Write current magnitude, see Write Mode description for equation LSB = 1.522 mA 11111 = maximum write current (63 mA) 00000 = minimum write current (15.8 mA)

TA Register
Address = 0011 001

BIT	NAME	DESCRIPTION
7:4	TA3:0	Thermal Asperity Threshold.
3	TAD	Thermal Asperity detector control
2:0	WCB2:0	Write Current Boost control

Mode Register
Address = 0100 001

BIT	NAME	DESCRIPTION
7	WTDD	Write transition detector disable. Used for TI internal testing. 1 = Disable write data frequency detector 0 = Enable write data frequency detector (normal mode)
6	BNK1	Servo Bank control bit, operate in conjunction with BNK0 in Write Register 1 = Servo Bank mode (both BNK0 and BNK1 must be 1 to enable Servo) 0 = Servo Bank mode off
5	FRON	Fast Recovery Mode Enable 1 = Fast recovery mode enabled (low corner frequency shift) 0 = Fast recovery mode disabled
4	X	Not Used. User setting = 0.
3	MRM	MR Measurement Mode 1 = Enables MR measurement mode. Activates DBHV 0 = Disables MR measurement mode
2	Gain	Read Amplifier Gain select 1 = 137 V/V 0 = 93 V/V
1	XIDL	Idle Control Bit 0 = Idle mode enabled
0	XSLP	Sleep control bit 0 = Sleep mode enabled.

USC Register
Address = 0101 001

BIT	NAME	DESCRIPTION
7:3	X	Not Used
2:0	USC2:0	Write Current Undershoot Control

WBD Register
Address = 0110 001

BIT	NAME	DESCRIPTION
7:3	X	Not Used
2:0	WBD2:0	Write Current Boost Delay Control

TABLE 3: Head Selection, 4 Channel Version

HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	X
0	1	1	0,1
1	0	2	2,3
1	1	3	All heads

TABLE 4: Head Selection, 8 Channel Version

HS2	HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	0	X
0	0	1	1	0,1,2,3
0	1	0	2	X
0	1	1	3	X
1	0	0	4	X
1	0	1	5	X
1	1	0	6	4,5,6,7
1	1	1	7	All heads

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VREF	O	External resistor connection to set DAC reference current, Rref = 2.0K
VCC	I	+5V Supply
VEE	I	-5V Supply
GND		Ground
RDX, RDY	O	Differential MR head Read Data Output
WDX, WDY	I	Differential PECL Write Data Input, a transition of (WDX-WDY) toggles the direction of the head current
R/W	I	Read / Write control input with internal pull-up. A low selects write mode.
XIMRON	I	MR current on. TTL, with internal pull-up. A low activates MR bias.
FLT	O	Open-collector output. Read mode: a low indicates a read fault Write mode: a high indicates a write fault MRM mode: A high indicates the head voltage is in the proper range.
SDATA	I/O	Serial port data Input, TTL with internal pull-down
SCLK	I	Serial port clock input, TTL with internal pull-down
SDEN	I	Serial port enable input, TTL with internal pull-down
HRnX	I/O	MR read head input X connection
HRnY	I/O	MR read head input Y connection
HWnX	O	Inductive write head X connection
HWnY	O	Inductive write head Y connection

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may result in permanent damage to the device

PARAMETER		RATING
DC Supply Voltage	VCC VEE	-0.3 to +7 VDC -6 to 0.3 VDC
Logic Input Voltage	(All except WDX,WDY) TTL (WDX,WDY) PECL	-0.3 to VCC +0.3 VDC 0 to VCC VDC
Write Current	Iw	80 mA
Write Head Voltage	Vwh	Vee-0.3 V to Vcc+0.3V
MR bias Current	Imr	20 mA
Read head voltage (diff)	Vmr	0 to 0.8V
Output Current	FLT/DBHV RDX/RDY	+8 mA -10 mA
Operating Junction Temperature	Tj	+135°C
Storage Temperature	Tstg	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage	VCC VEE	4.5 to 5.5 VDC -4.5 to -5.5 VDC
Ambient Temperature	Ta	0 to 70°C
Reference Resistor,	Rref	2.0 KΩ
Write head load range	Lh	0 to 200 nH
Write head resistance range	Rh	5 to 20 Ω
Read head range	Rmr	25 to 80 Ω
Package thermal resistance, 48 TQFP	ΘjA	60°C/W

NOMINAL OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage	VCC VEE	4.5 to 5.5 VDC -4.5 to -5.5 VDC
Ambient Temperature	Ta	0 to 70°C
Reference Resistor,	Rref	2.0 KΩ
Write Current, single head write	Iw	40.1 mA
Write head load range	Lh	80 nH
Write head resistance range	Rh	11 Ω
Read head range	Rmr	45 Ω
MR bias current	Imr	5.0 mA

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. Rmr = 45 Ω, Imr=5.0 mA, Iw=40.1 mA, Lh = 80 nH, Rh = 11 Ω,Ch = 2 pF, WCB = 000, USC = 101

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current ICC	Read Imr off		32.4	40	mA
	Read Imr on		74	92	mA
	Write Imr off		86.4	108	mA
	Write Imr on		95	118	mA
	Servo (half bank 4-channel), Iw=25mA,VCC/VEE = 4.5 V		114		mA
	Servo (all head 4-channel), Iw=25mA, VCC/VEE = 4.5 V		186		mA
	Servo (half bank 8-channel), Iw=25mA,VCC/VEE = 4.5 V		198		mA
	Servo (all head 8-channel), Iw=25mA,VCC/VEE = 4.5 V		344		mA
	Idle		17	23.6	mA
	Sleep		17	23.6	mA
VEE Supply Current IEE	Read Imr off		48	60	mA
	Read Imr on		87	109	mA
	Write Imr off		112	140	mA
	Write Imr on		123	154	mA
	Servo (half bank 4-channel), Iw=25mA,VCC/VEE = 4.5 V		150		mA
	Servo (all head 4-channel), Iw=25mA, VCC/VEE = 4.5 V		240		mA
	Servo (half bank 8-channel), Iw=25mA,VCC/VEE = 4.5 V		275		mA
	Servo (all head 8-channel), Iw=25mA,VCC/VEE = 4.5 V		450		mA
	Idle		20	29	mA
	Sleep		20	29	mA
VCC/-VEE Fault	Fault detected	3.65	3.85	4.1	V
	Fault removed	3.75	4.0	4.3	V
POR VCC Voltage	Reset removed		1.8	2.1	V

ESD RATINGS

ESD STRESS MODEL	LOWEST PIN VOLTAGE RATING
Human Body Model	> 1000V
Charge Device Model	> 500 V

DIGITAL INPUTS AND OUTPUTS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input High Voltage	V_{IH1}	TTL	2.0			VDC
Input Low Voltage	V_{IL1}	TTL			0.8	VDC
Input High Current	I_{IH1}	V_{IH1} =2.0V			160	µA
Input Low Current	I_{IL1}	V_{IL1} =0.8V	-400			µA
Input High Voltage	V_{IH3}	PECL	2.0		Vcc-0.6	VDC
Input Low Voltage	V_{IL3}	PECL	1.2		V_{IH3}-0.2	VDC
Input Δ Voltage			0.2	0.6	1.8	VDC
Input High Current	I_{IH3}	V_{IH3} =4.0V		5	100	µA
Input Low Current	I_{IL3}	V_{IL3} =3.2V		5	100	µA
Differential Input Resistance		WDX/WDY		130		Ω
Output High Current	I_{OH}	FLT/DBHV V_{OH} =VCC			50	µA
Output Low Voltage	V_{OL}	FLT/DBHV I_{OL} =2mA			0.4	V

SERIAL PORT TIMING

Serial Port Timing, Readback

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		32			ns
SCLK Low Time	T_{CKL}		14			ns
SCLK High Time	T_{CKH}		14			ns
Enable to SCLK	T_{SENS}		9			ns
SCLK to Disable	T_{SENH}		9			ns
Data Set-up Time	T_{DS}		3			ns
Data Hold Time	T_{DH}		3			ns
SDEN min. Low Time	T_{SL}		32			ns

SERIAL PORT TIMING, WRITE ONLY

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		25			ns
SCLK Low Time	T_{CKL}		10			ns
SCLK High Time	T_{CKH}		10			ns
Enable to SCLK	T_{SENS}		9			ns
SCLK to Disable	T_{SENH}		9			ns
Data Set-up Time	T_{DS}		3			ns
Data Hold Time	T_{DH}		3			ns
SDEN min. Low Time	T_{SL}		25			ns

CURRENT DAC REFERENCE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Voltage Reference	Vref		1.848	1.945	2.042	V
Reference R Range	Rref			2.0		KΩ
Reference Current	Iref			1		mA

READ CHARACTERISTICS

Rmr = 45 Ω, Imr = 5.0 mA

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance	Recommended	25	45	80	Ω
MR Bias Current	Typical range	2.1		9.6	mA
MR Bias Current Resolution			5		bit
LSB	Rref = 2 KΩ		242		µA
MR Current Tolerance		-8		+8	%
MR Head DC Voltage Range				0.8	V
Unselected Head Current				15	µA
Input Resistance	Differential, Imr = 5.0 mA		500		Ω
Differential Voltage Gain	R_{MR} = 45Ω, Imr = 5.0 mA 1 mV p-p @ 15MHz GAIN = 0 GAIN = 1	 79.05 116.45	 93 137	 106.95 157.55	 V/V V/v
Bandwidth	Lower -3dB Lower -3dB, Fast recovery Higher -1dB Higher -3dB, Rmr = 45	 300	1.0 3.5 TBD TBD	1.5	MHz MHz MHz MHz
Input Voltage Noise	R_{MR} = 45, Imr = 5.0, Gain = 0 BW =10 to 100 MHz		0.70		nV/√Hz
Input Current Noise	R_{MR} = 45, Imr = 5.0, Gain = 0 BW =10 to 100 MHz		13		pA/√Hz
Dynamic Range	Gain falls to 90% @ 5 MHz	8			mV
Output Offset Voltage		-300		300	mV
Output Current			3.0		mA
Output Voltage	RDX,RDY		VCC – 1.6		V
Output Resistance	Single-ended	60	88	110	Ω
PSRR	@ 25 MHz, no bypass caps	40			dB
Channel Separation	@ 25 MHz, no bypass caps	TBD	30		dB
CMRR	@ 25 MHz, no bypass caps	40			dB
I/O Rejection	WDX, WDY, SDEN, SCLK, SDATA, R/W,XIMRON, FLT @ 25 MHz, no bypass caps	40			dB

WRITE/SERVO CHARACTERISTICS

Iw=40.1 mA, Lh = 80 nH, Rh = 11 Ω,Ch = 1/2/1 pF, WCB = 100, USC =101, WBD =TBD

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range	Typical	15.8	40.15	63	mA
Write Current Resolution			5		bit
LSB			1.522		mA
Write Current Accuracy	DC conditions	-10		+10	%
Boost Current Range	DC conditions	0		35	mA
Boost Current Resolution			3		bits
Boost Current LSB			5.0		mA
Boost Current Accuracy	DC conditions	-8		+8	%
Boost Delay Resolution			3		bits
Undershoot Current Resolution			3		bits
Differential Head Swing	Open Head,	7.5			Vpp
Unselected Head Current	DC Transient			100 1	μA mA pk
Common Mode head Voltage	Selected head, read mode		0		V
Common Mode head Voltage	Unselected head, all modes except selected head, Idle		0.5		V
Damping resistor	See note		1.35		KΩ
WDX/WDY Input Resistance	Internal Termination		130		Ω

NOTE: This is the DC resistance across head, it is not the primary writer damping control. Device uses active overshoot/undershoot control for writer

HEAD VOLTAGE MONITOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DBHV upper threshold	FLT = high to low	271.4	295	318.6	mV
DBHV lower threshold	FLT = low to high	128.34	139.5	150.66	mV

SWITCHING CHARACTERISTICS

Rmr = 45 Ω, Imr = 5.0 mA,Iw=40.1 mA, Lh = 80 nH, Rh = 11 Ω,Ch = 1/2/1 pF, WCB = 100, USC =101, WBD =000

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Write to read	R/W	90% signal envelope, ±30mV DC. XIMRON = 0		250	450	ns
Write to Read	R/W	10% of Iw, single head write			20	ns
		10% of Iw, servo bank write			20	ns
Read to write	R/W	90% of Iw, single head read			20	ns
	R/W	90% of Iw, servo bank write			30	ns
Idle to read	CS	90% signal envelope, ±30mV DC			5	µs
Write to idle	CS	10% of Iw			20	ns
Head Switching	HSn	90% signal envelope, ±30mV DC			5	µs
Write Current rise/fall time		Lh=80nH, Iw=40 mA, Rh = 11Ω WCB = 100, 10% to 90%		0.85	0.9	ns
Write Current undershoot		% of Iw steady state, WCB = 000 USC = 000 USC = 111		 30 0		 % %
Write Current undershoot		% of Iw steady state, USC = 101, WBD = 101 WCB = 000 WCB= 111		 80 165		 % %
Write Current settling time		95% to 105% of Iw steady state WCB = 000, USC = 101			8	ns
Head Current delay	TD3	50% of WD to 50% of Iw			5	ns
Write Current asymmetry		Propagation delay difference		500		ps

HEAD UNSAFE DETECTION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FLT low to high, TD1	No write data transition		500		ns
FLT high to low, TD2			20		ns
Write data frequency	Valid transient detector		160	TBD	MHz
	Valid Open detector			N/A	MHz
MR head open threshold		800	1000	1250	mV
MR head short threshold			35	60	mV

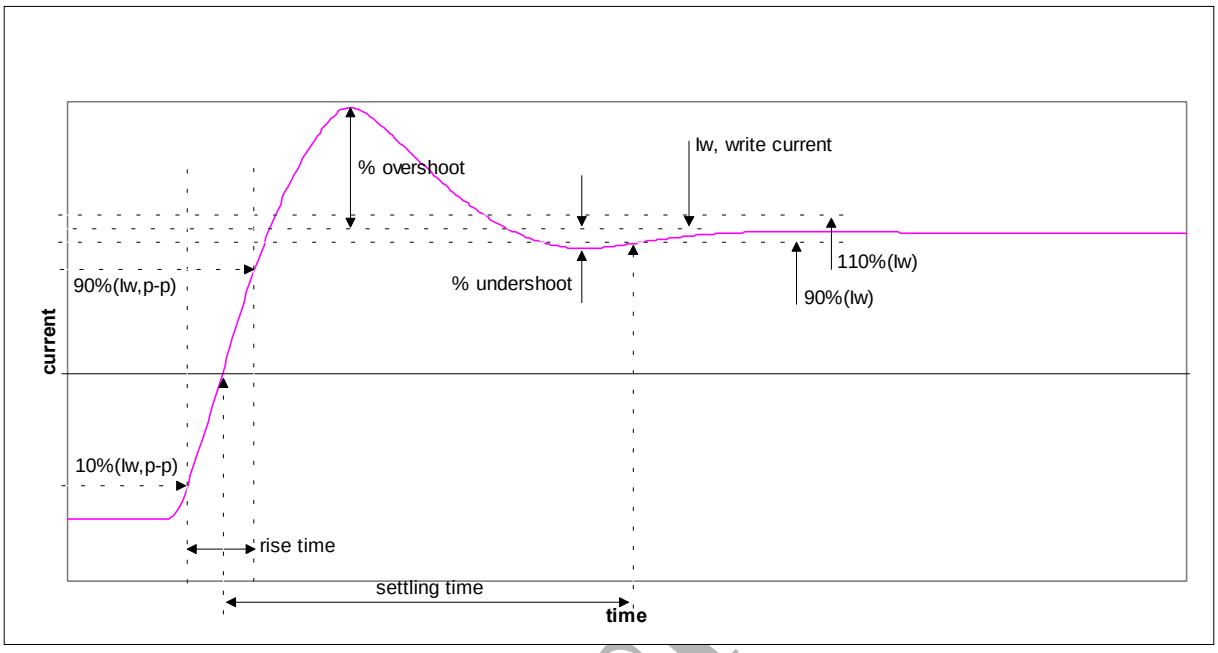


FIGURE 3: Write Current Waveform Characteristics

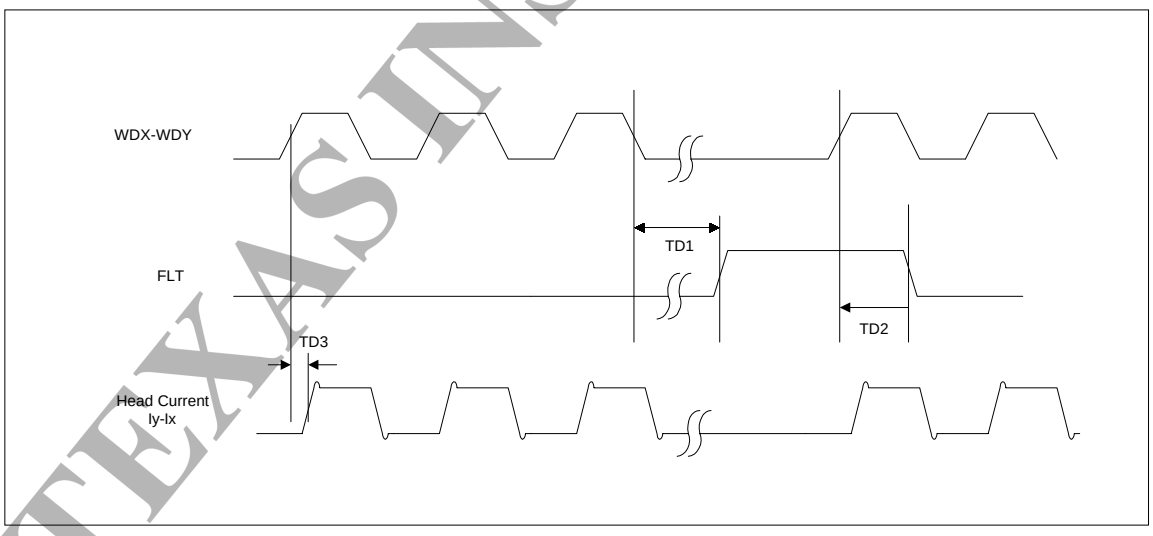
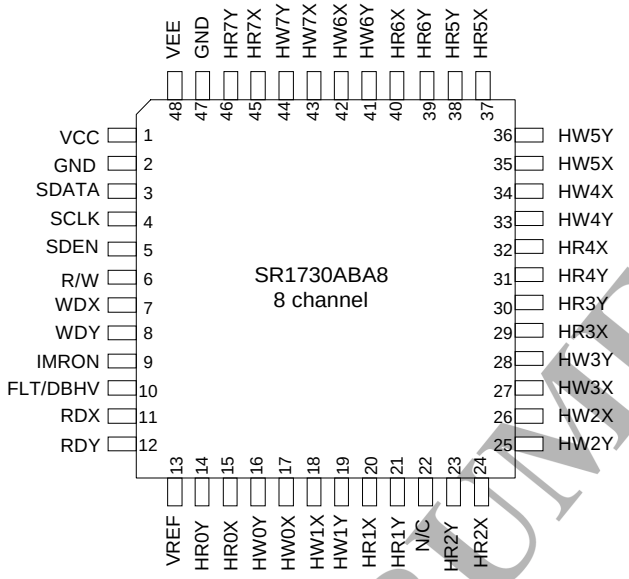
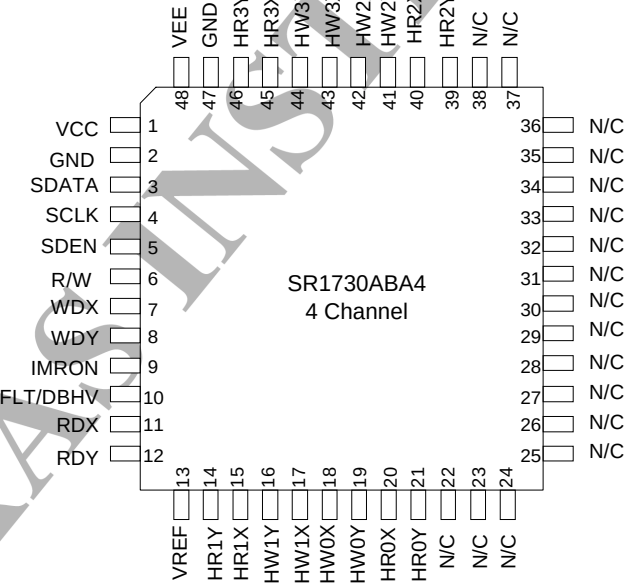


FIGURE 4: FLT Timing

PACKAGE PIN DESIGNATIONS





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SR1731BBA4DBT
+5/-5V IB/VS 4-CHANNEL GMR READ/WRITE DEVICE

Prototype

May, 2000

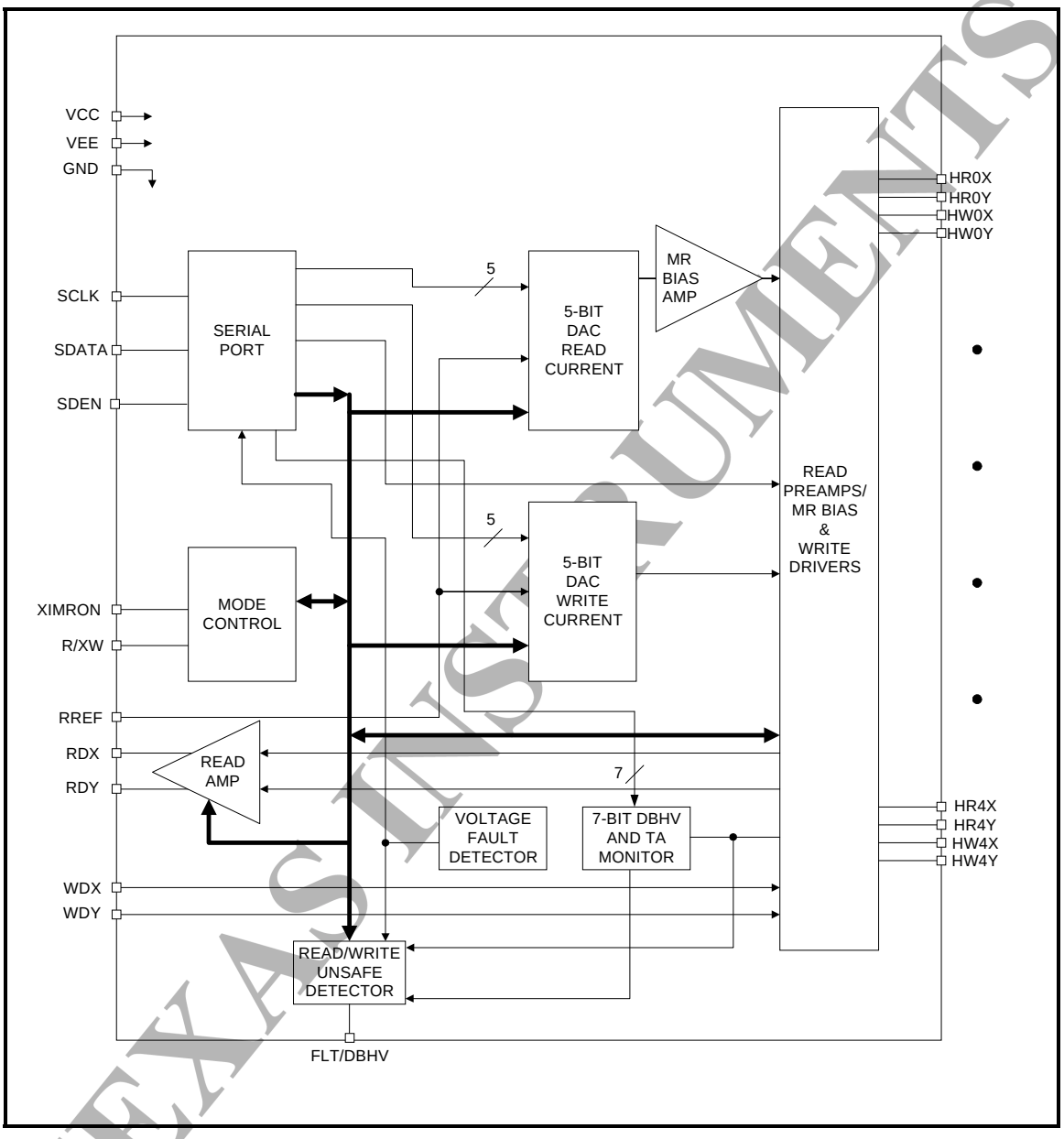
DESCRIPTION

The TI SR1731BBA4 is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. The reader architecture is MR current bias/voltage sense and will support a user data rate of up to 500 Mbits/sec. A read/write capable serial port is provided to enable the implementation of on-chip MR bias and Write current DACs. The device provides a write driver, low-noise read amplifier, serial port controlled head selection, write current, MR read bias current and read and write fault detection circuitry for up to four channels. The device requires +5V and -5V and comes in a 38-pin TSSOP/DBT package.

FEATURES

- **+5V ±10%, -5V ±10% supplies**
- **Designed for four-terminal MR heads with minimum external components**
- **DC blocking capacitors integrated on chip**
- **Truly differential current bias/voltage sense MR read Amp**
- **MR head bias current range = 2.12 – 9.56 mA (5-bit)**
- **MR read gain = 79.4 V/V and 112 V/V @ 45 Ω**
- **MR read input noise = .70 nV/√Hz @ 45 Ω**
- **Read bandwidth = 300 MHz**
- **Differential PECL write data input, 3V compatible**
- **Head voltage swing = 12 Vp-p**
- **Write current range = 15.75 – 62.25 mA (5-bit)**
- **Write current rise/fall time = 0.8 ns (Lh = 90 nH, Rh = 11 Ω, 50% boost)**
- **Servo bank write capability**
- **Read and write unsafe detection**
- **Thermal asperity detection and fast recovery**
- **Power supply fault protection**
- **Serial port controls head selection, write current, MR read bias current**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The TI SR1731BBA4 addresses up to 4 four-terminal MR heads providing write drive or read bias and amplification. TTL pins R/XW and XIMRON, and serial port register bits control the operational mode as shown in Table 1. The R/XW and XIMRON inputs have internal pull-up resistors so that when left opened, it will default to the TTL High state.

The three-line serial data interface, with both read and write capabilities, is used to control head selection, write current, MR bias current, and mode control. The serial data port includes 5 read/write capable data registers, one read/reset fault register, and one read only ID register. See Serial Interface Operation for description of the serial port operation. The three serial interface pins, SDEN, SDATA and SCLK have internal pull-down resistors.

WRITE MODE

In write mode, the write current is enabled to the selected channel, write data controls the write current polarity, and the FLT output is driven. Enabling the reader bias current is independent of this mode and is referred to as Read Bias Active in Write mode (RBAW). MR bias current is enabled by placing XIMRON input to a low logic state. Device power consumption is reduced when the MR bias is disabled. The read outputs, RDX/RDY, are set to a high impedance state during write mode.

The FLT output is LOW in this mode unless there is a write fault, which causes the output to go HIGH.

Referring to Table 1, selecting write mode configures the internal 5-bit write current DAC, programmable via serial port. Head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each transition of the differential PECL signal WDX-WDY, i.e. WDX>WDY will cause Iw to flow from X to Y. The WDX/WDY write data input includes a 130 Ω differential termination resistor.

The magnitude of the current (0-pk) is set by 5-bit DAC as below:

$$Iw\ (mA) = 15.75 + n * LSB$$

where the LSB = 1.5 mA and n = 0, 1 .. 31 is decimal value of 5-bit write current register bits IW0:IW4.

The SR1731BBA4 includes overshoot and undershoot control. 3 bits of write boost control (WCB2:WCB0), 3 bits of undershoot control (USC2:USC0), and 2 bits of write boost delay (WBD1:WBD0) provide means to optimize the write current wave shape.

TABLE 1: Mode Select

XSLP	XIDL	R/XW	XIMRON	BNK0	BNK1	Write Current	MR Current	Mode
1	1	1	0	0	X	OFF	ON	Read Mode
1	1	1	0	X	0	OFF	ON	Read Mode
1	1	1	1	X	X	OFF	OFF	Read-Inactive
1	1	1	0	1	1	OFF	OFF	Read-Inactive (ready for Servo)
1	1	0	0	0	0	ON	ON	Write Mode (RBAW)
1	1	0	1	0	0	ON	OFF	Write Mode
1	1	0	X	1	1	ON	OFF	Servo Mode
1	0	X	X	X	X	OFF	OFF	Idle Mode
0	X	X	X	X	X	OFF	OFF	Sleep Mode

NOTE: XSLP, XIDL, BNK0, BNK1 are serial port register bits

SERVO BANK WRITE MODE

The SR1731BBA4 includes servo bank write capability, which allows multiple heads to be written simultaneously. Servo bank write mode is enabled by setting the BNK0 and BNK1 serial port bits to 1, followed by placing the R/XW pin low. Note that the servo control bits are located in two different serial port registers to prevent accidental servo bank write activation. If only one of the two servo enable bits are set in write mode (BNK0 or BNK1), a write fault is produced.

Upon entering servo bank write mode, the device will concurrently enable the write current to the selected heads. The activated heads in servo mode are determined by register bits HS1:HS0 as shown in Table 4. HS1 activates the lower-half channels and HS0 controls the upper-half channels.

Write current in servo bankwrite mode is controlled with the WC4:WC0 bits as in regular write mode, although the maximum expected write current in bankwrite mode is 35 mA 0-pk . The user is responsible for controlling the write duty cycle and environment in bankwrite mode to limit power dissipation and junction temperature.

The MR bias current is disabled in bankwrite mode regardless of the state of the XIMRON pin. Although only voltage faults are detected in bankwrite mode, write current is not disabled by a voltage fault condition. If the servo enable bits are set in the read mode (BNK0 and BNK1), the preamp goes into the Read-Inactive mode and all four writers are pre-charged in order to accommodate a very fast Read-to-Servo-Bankwrite transition.

READ MODE

In normal read mode, bias current is enabled to the selected head, the chip drives the RDX/RDY read signal outputs, and the FLT output is active.

The FLT output is HIGH in this mode unless there is a read fault, which causes the output to go LOW.

Referring to Table 1, selecting read mode activates the MR bias current generator and low-noise differential amplifier. The outputs of the read amplifier, RDX and RDY, are emitter followers and are in phase with the resistivity change at the selected input ports, HRnX and HRnY, where the respective MR head is attached. The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port. The DAC reference current is set by an external resistor 2.0 K Ω at pin VREF = 2.0V. The magnitude of the bias current is set according to the following equation:

I_{MR} (mA) = 2.12 + 0.24*n, with Rmr = 45 Ω,

where n = 0, 1 . . . 31, is the decimal value of the 5 bit serial port register bits IMR4:IMR0.

The resistance of the MR element has an effect on the actual MR bias current. The following equation can be used to determine the magnitude of the MR bias current with Rmr values other than 45 Ω:

$$I_{MR}\,(\text{mA}) = 136 * \frac{(n + 8.8)}{(520 + Rmr)},$$

where n = 0, 1 . . . 31, is the decimal value of the 5 bit serial port register bits IMR4:IMR0. The SR1731BBA4 is designed such that a Rmr of 45 Ω results in the specified MR bias range of 2.12 –9.56 mA.

The read amplifier's DC blocking capacitors and noise capacitor are integrated on the device. Aside from normal power supply bypass capacitors, no external capacitors are required for the read circuit.

In Read mode, the voltage at the midpoint of the selected MR head is forced to the ground potential. For the unselected MR heads, the head ports become high impedance and thus will prevent the heads from conducting current in the event of head to disk contact.

To improve the write to read recovery time, the MR bias current can be activated during Write mode. With the MR bias current turned on, the voltage change across the internal DC blocking capacitors between write and read modes will be minimized which will result in faster write to read recovery time. Placing the XIMRON pin low enables the MR bias.

If the servo enable bits are set in the read mode (BNK0 and BNK1), the preamp goes into the Read-Inactive mode and all four writers are pre-charged in order to accommodate a very fast Read-to-Servo-Bankwrite transition.

READ-INACTIVE MODE

Similar to read mode, but the MR bias current is diverted to an internal dummy resistor. At the same time several control/bias circuits particular to each reader are disabled resulting in a lower VEE current. The FLT output is a constant LOW during this mode.

Read-inactive mode is entered when the MR bias current is disabled or the servo enable bits are set (BNK0 and BNK1). Recovery time from this mode to Read mode will be no longer than the worst-case head-switch time.

The AC read signal output in this mode is undefined. The DC read signal outputs should be the same as in normal read mode in order to facilitate fast recovery to read mode.

IDLE MODE

Taking serial port bit XIDL low selects idle mode. In this mode, all outputs are disabled, with the reader and writer sections put into a reduced power consumption standby mode. The chip does not drive any of the outputs in this mode.

MR bias current is diverted to an internal dummy head to keep the DC blocking and noise filter caps biased properly, and all critical nodes on the chip will remain biased to facilitate quick recovery from this mode. Recovery form Idle mode to Read mode is expected to be no longer than the worst-case head switch time. Recovery from this mode to write mode is not specified.

SLEEP MODE

Taking serial port bit XSLP low selects sleep mode.

POWER SUPPLY FAULT PROTECTION

During a power up condition, the power-on voltage monitor disables the chip from any active mode. The threshold voltage for the serial port power-on reset is 1.8 V (typical). The threshold voltage for a VCC or VEE fault, which also disables the normal write mode but does not reset the serial port registers, is 3.9V/3.7V (typical, with hysteresis).

Internally, the serial port logic operates between GND and VEE. If the VEE supply is removed from the device, such as under a VEE regulator shut-down mode, all serial port settings will be lost regardless of the state of the VCC supply. The serial port data bits will reset to the power-on default state (all 0's) when the power is restored. The desired serial port registers settings must be restored by the user after a VCC or VEE shut-down similar to a normal power-up condition. The device will survive the VEE shut-down condition (i.e. no latch-up) provided the VEE input is not allowed to rise more than a diode drop above GND.

FAULT OPERATION

The FLT pin flags a fault condition in the read or write modes:

Read Fault Detection

Logic low on the FLT pin indicates a read fault condition. A read fault may be any one of the following conditions:

- Open MR element (reported to FAULT register)
- Shorted MR element (reported to FAULT register)
- Thermal asperity detected
- Low Vcc or Vee (reported to FAULT register)
- Illegal head selection
- MR bias current disabled by XIMRON = 1

Write Fault Detection

Logic high on the FLT pin indicates a write fault condition. A write fault may be any one of the following conditions:

- Low write data frequency (reported to FAULT register)
- Write head terminal shorted to ground (reported to FAULT register)
  This fault is always latched and the preamp will be forced into IDLE mode until the fault latching circuit is cleared by setting the R/XW pin high (i.e. going back to READ mode).
- Illegal head selection
- Open write head (detected and latched in the READ mode for the selected head, but reported to the FLT pin and the FAULT register in the subsequent Write mode for the same head)
- Low Vcc or Vee (reported to FAULT register). Forces preamp into IDLE mode except in servo bank write mode.

Selected faults are reported to the FLT register (both in Read and Write mode), as depicted in the Serial

Interface Operation section. The FLT register is cleared at power up. The first fault that occurs is latched into the FLT register ignoring any consequent faults. No new faults will be latched in until the FLT register is cleared. In order to clear the FLT register the user has to write all zeros to it (note non zero values will not clear the FLT register). However, if the fault(s) is still present, the fault register will re-latch it in.

MR RESISTANCE MEASUREMENT MODE

MR resistance measurement can be activated in read mode by setting MRM bit in the Mode register. In this mode, the FLT pin can is configured to output a Digital Buffered Head Voltage (DBHV) indication.

With MRM = 1 the Thermal Asperity Detector is disabled and the FLT pin becomes the digital head voltage monitor. The DBHV threshold is programmed by the TA data register, bits TA0:TA6. When the MR head voltage is lower than the set internal threshold voltage, the FLT pin flags high. When the MR head voltage is higher than the set DBHV threshold, FLT flags low.

The recommended application of the MRM mode is to fix the MR bias current, adjust the DBHV threshold until the FLT pins asserts. The MR resistance is equal to the DBHV threshold setting (in mV) divided by the MR bias setting (in mA). It is recommended that the MR bias setting be fixed while the TA threshold is adjusted, rather than fixing the threshold and adjusting the MR bias, to prevent damage to the head from excessive bias current. In order to maximize the accuracy of the measured RMR resistance, it is best to keep the voltage drop across the RMR element between 150 mV and 250 mV.

THERMAL ASPERITY DETECTION AND FAST RECOVERY

Thermal asperity detection is enabled by setting the Thermal Asperity Threshold DAC (TA0:TA6) to a non-zero value. When activated, thermal asperity detection will flag a thermal asperity event whenever the RDX-RDY output signal exceeds the programmed threshold. A thermal asperity event will cause the FLT output to go LOW and it will remain low until the RDX/RDY output signal falls below the programmed threshold level plus some hysteresis. The TA threshold level can be programmed as follows:

$$TAth\ (mV) = 6*n\ mV\ ,\ where\ n = 1\ldots127$$

A thermal asperity data retry feature called Fast Recovery mode is available. The TAC serial port bit controls fast recovery mode. In Fast recovery mode the low frequency high-pass cutoff point switches from 1.0 MHz (typical) to 3.5 MHz (typical), reducing the low frequency content of the readback signal.

TABLE 1: Thermal Asperity Modes

TA6:0	TAC	Thermal Asperity Mode
0	0	Off (no detection or compensation)
X	1	Fast Recovery (low corner frequency shift)
Non-0	X	TA Detection mode (TA6:0 sets the threshold and must be nonzero)

NOTE: To enable TA detector: MRM = 0 and TA6:0 = nonzero. MRM has priority.

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, thermal asperity threshold and mode. Moreover, the serial data port contains a Fault register capable of latching in certain faults. The serial port bit map is shown in Table 3.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/W bit which is high for a read operation. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0, and S2=0 for R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits (See Serial Port Bit Map).

Asserting the serial port enable line SDEN (TTL) initiates a transfer, SDATA (TTL) is clocked into the internal shift register by the rising edge of SCLK (TTL). A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

Please see Power Supply Fault Protection section regarding serial port response to power supply shut-down.

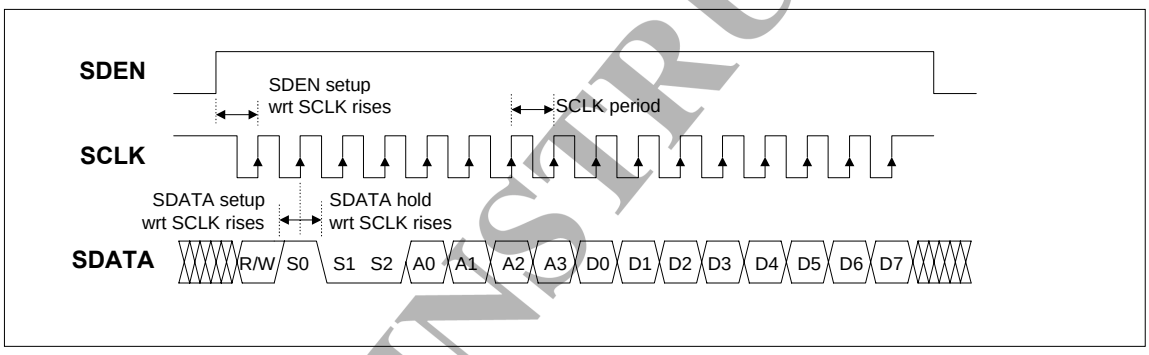


FIGURE 2: Serial Port Timing

TABLE 3: Serial Port Bit Map

Reg	A3:A0	S2:S0	D7	D6	D5	D4	D3	D2	D1	D0
ID	0000	001	0	1	0	0	1	1	0	1
HS/IMR	0001	001	IMR4	IMR3	IMR2	IMR1	IMR0	HS2	HS1	HS0
WRITE	0010	001	BNK0	X	X	IW4	IW3	IW2	IW1	IW0
TA	0011	001	TAC	TA6	TA5	TA4	TA3	TA2	TA1	TA0
MODE	0100	001	WTDD	X	BNK1	Res	MRM	GAIN	XIDL	XSLP
WERR	0101	001	WBD1	WBD0	WCB2	WCB1	WCB0	USC2	USC1	USC0
FLT	0110	001	X	TF_F_L	TF_S	TF_O	MR_S	MR_O	VFLT	X

Register map not displayed in order of bit transfer.
ID register is read only.
X = Not Used
All Data bits are set to 0 at reset condition, i.e. power-up or voltage fault condition, except ID register.

SERIAL PORT REGISTER DEFINITIONS

Addresses are shown MSB first and are formatted as: A3,A2,A1,A0,S2,S1,S0. Serial port Read/Write bit is not shown.

ID REGISTER (READ ONLY REGISTER)

Address = 0000 001

BIT	NAME	DESCRIPTION
7:0	VID	Set to meet customer's requirements = 0100 1101

HS/IMR REGISTER

Address = 0001 001

BIT	NAME	DESCRIPTION
7:3	IR4:0	MR bias current setting, see Read Mode description for bias equation. LSB = 0.24 mA 11111 = maximum MR bias current (9.56 mA) 00000 = minimum MR bias current (2.12 mA)
2:0	HS2:HS0	Head Select bits, see Tables 3 for head select bit map. HS2 = 0 for SR1731BBA, 4-channel device

WRITE REGISTER

Address = 0010 001

BIT	NAME	DESCRIPTION
7	BNK0	Servo Bank control bit, operate in conjunction with BNK1 in Mode Register 1 = Servo Bank mode (both BNK0 and BNK1 must be 1 to enable Servo) 0 = Servo Bank mode off Note: if both BNK0 and BNK1 are set high while R/XW is high, the preamp will go into Read-Inactive mode.
6:5	N/C	Not Connected
4:0	IW4:0	Write current magnitude, see Write Mode description for equation LSB = 1.5 mA 11111 = maximum write current (59.95 mA) 00000 = minimum write current (15.00 mA)

TA REGISTER
Address = 0011 001

BIT	NAME	DESCRIPTION
7	TAC	Thermal Asperity Fast Recovery Enable 1 = Fast recovery mode enabled (low corner frequency shift) 0 = Fast recovery mode disabled
6:0	TA6:0	Thermal Asperity Threshold/Enable. DAC also used to set DBHV threshold when MRM = 1. 000 0000 = Thermal Asperity Detection Disabled 000 0001 = 6 mV (Thermal Asperity Detection Enabled) ---------- 111 1111 = 762 mV (Thermal Asperity Detection Enabled) Note: MRM=1 overrides the TAD mode and sets the preamp in the Digital Buffer Head Voltage (DBHV) measurement mode.

MODE REGISTER
Address = 0100 001

BIT	NAME	DESCRIPTION
7	WTDD	Write transition detector disable. Used for TI internal testing. 1 = Disable write data frequency detector 0 = Enable write data frequency detector (normal mode)
6	X	Not Connected
5	BNK1	Servo Bank control bit, operate in conjunction with BNK0 in Write Register 1 = Servo Bank mode (both BNK0 and BNK1 must be 1 to enable Servo) 0 = Servo Bank mode off Note: if both BNK0 and BNK1 are set high while R/XW is high, the preamp will go in the Read-Inactive mode.
4	Res	Reserved. User setting = 0. If set to 1 it will increase the Write Current Boost Delay.
3	MRM	MR Measurement Mode 1 = Enables MR measurement mode. Activates DBHV 0 = Disables MR measurement mode
2	Gain	Read Amplifier Gain select 1 = 112 V/V 0 = 79.4 V/V
1	XIDL	Idle Control Bit 0 = Idle mode enabled
0	XSLP	Sleep control bit 0 = Sleep mode enabled.

WERR REGISTER
Address = 0101 001

BIT	NAME	DESCRIPTION
7:5	WBD1:0	Write Current Boost Delay Control
4:3	WCB2:0	Write Current Boost Control
2:0	USC2:0	Write Current Undershoot Control

FLT REGISTER
Address = 0110 001

NOTE: User must write 00h to register to clear faults. See Fault Operation description for details on fault reporting.

BIT	NAME	DESCRIPTION
7	X	Not Connected
6	TF_F_L	Write Data Frequency Low
5	TF_S	Write Head Short to Ground
4	TF_O	Write Head Open (detected and latched in the read mode, but reported in the write mode)
3	MR_S	MR Head Short
2	MR_O	MR Head Open
1	VFLT	Low VCC or VEE
0	X	Not Connected

TABLE 4. Head Selection, 4 Channel Version

HS1	HS0	READ/WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	X
0	1	1	0,1
1	0	2	2,3
1	1	3	All heads

NOTE: HS2 must be low for proper read operation.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RREF	O	External resistor connection to set DAC reference current, Rref = 2.0K
VCC	I	+5V Supply
VEE	I	-5V Supply
GND		Ground
RDX, RDY	O	Differential MR head Read Data Output
WDX, WDY	I	Differential PECL Write Data Input, a transition of (WDX-WDY) toggles the direction of the head current. The recommended differential voltage must be present during WRITE mode at all times (i.e. do not short both terminals to same voltage potential during WRITE mode).
R/XW	I	Read / Write control input with internal pull-up. A low selects write mode.
XIMRON	I	MR current ON when low. TTL, with internal pull-up.
FLT	O	Open-collector output. Read mode: a low indicates a read fault Write mode: a high indicates a write fault MRM mode: A high indicates the MR head voltage is lower than the TA DAC threshold.
SDATA	I/O	Serial port data Input, CMOS with pull down
SCLK	I	Serial port clock input, CMOS with pull down
SDEN	I	Serial port enable input, CMOS with pull down
HRnX	I/O	MR read head input X connection
HRnY	I/O	MR read head input Y connection
HWnX	O	Inductive write head X connection
HWnY	O	Inductive write head Y connection

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may result in permanent damage to the device

PARAMETER		RATING
DC Supply Voltage	VCC VEE	-0.3 to +7 VDC -6 to 0.3 VDC
Logic Input Voltage	(All except WDX,WDY) TTL (WDX,WDY) PECL	-0.3 to VCC +0.3 VDC 0 to VCC VDC
Write Current	Iw	80 mA
Write Head Voltage	Vwh	Vee-0.3 V to Vcc+0.3V
MR bias Current	Imr	20 mA
Read head voltage (diff)	Vmr	0 to 0.8V
Output Current	FLT RDX/RDY	+8 mA -10 mA
Operating Junction Temperature	Tj	+135°C
Storage Temperature	Tstg	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage	VCC VEE	4.5 to 5.5 VDC -4.5 to -5.5 VDC
Ambient Temperature	Ta	0 to 70°C
Reference Resistor,	Rref	2.0 KΩ
Write head load range	Lh	0 to 200 nH
Write head resistance range	Rh	5 to 20 Ω
Read head range	Rmr	25 to 80 Ω
Package thermal resistance, 38 TSSOP/DBT	ΘjA	66°C/W

NOMINAL OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage	VCC VEE	4.5 to 5.5 VDC -4.5 to -5.5 VDC
Ambient Temperature	Ta	0 to 70°C
Reference Resistor,	Rref	2.0 KΩ
Write Current, single head write	Iw	40 mA
Write head load range	Lh	90 nH
Write head resistance range	Rh	11 Ω
Read head range	Rmr	45 Ω
MR bias current	Imr	6.0 mA

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. Rmr = 45 Ω, Imr=6.0 mA, Iw=40.3 mA, Lh = 90 nH, Rh = 11 Ω,Ch = 2 pF, WCB = 001, USC = 101

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	ICC	Read Imr off		36	40	mA
		Read Imr on		73	92	mA
		Write Imr off		89	108	mA
		Write Imr on		95	118	mA
		Servo (2 channel), Iw=25mA Vcc = 4.5 V		TBD	TBD	mA
		Servo (4 channel), Iw=25mA Vcc = 4.5 V		211	264	mA
		Idle		19	22	mA
		Sleep		19	22	mA
VEE Supply Current	IEE	Read Imr off		50	60	mA
		Read Imr on		84	109	mA
		Write Imr off		112	140	mA
		Write Imr on		124	150	mA
		Servo (2 channel), Iw=25mA Vcc = 4.5 V		TBD	TBD	mA
		Servo (4 channel), Iw=25mA Vcc = 4.5 V		211	264	mA
		Idle		19	22	mA
		Sleep		19	21	mA
VCC/-VEE Fault		Fault detected	3.65	3.78	3.9	V
		Fault removed	3.75	3.98	4.1	V
POR VCC Voltage		Reset removed		1.8	2.1	V

DIGITAL INPUTS AND OUTPUTS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input High Voltage	V_{IH1}	CMOS	2.0			VDC
Input Low Voltage	V_{IL1}	CMOS			0.8	VDC
Input High Current	I_{IH1}	V_{IH1} =2.0V			160	µA
Input Low Current	I_{IL1}	V_{IL1} =0.8V		0		µA
Input High Voltage	V_{IH3}	PECL	2.0		Vcc-0.6	VDC
Input Low Voltage	V_{IL3}	PECL	1.2		V_{IH3}-0.2	VDC
Input Δ Voltage			0.2	0.6	1.8	VDC
Input High Current	I_{IH3}	V_{IH3} =4.0V		5	100	µA
Input Low Current	I_{IL3}	V_{IL3} =3.2V		5	100	µA
Differential Input Resistance		WDX/WDY		130		Ω
Output High Current	I_{OH}	FLT V_{OH} =VCC			50	µA
Output Low Voltage	V_{OL}	FLT I_{OL} =2mA			0.4	V

SERIAL PORT TIMING, READBACK

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		100			nS
SCLK Low Time	T_{CKL}		28			nS
SCLK High Time	T_{CKH}		28			nS
Enable to SCLK	T_{SENS}		18			nS
SCLK to Disable	T_{SENH}		TBD			nS
Data Set-up Time	T_{DS}		6			nS
Data Hold Time	T_{DH}		6			nS
SDEN min. Low Time	T_{SL}		TBD			nS

SERIAL PORT TIMING, WRITE ONLY

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C		25			nS
SCLK Low Time	T_{CKL}		10			nS
SCLK High Time	T_{CKH}		10			nS
Enable to SCLK	T_{SENS}		9			nS
SCLK to Disable	T_{SENH}		TBD			nS
Data Set-up Time	T_{DS}		3			nS
Data Hold Time	T_{DH}		3			nS
SDEN min. Low Time	T_{SL}		25			nS

CURRENT DAC REFERENCE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Voltage Reference	Vref		1.9	2.0	2.1	V
Reference R Range	Rref			2.0		KΩ
Reference Current	Iref			1		mA

TAD/DBHV CHARACTERISTICS (READ MODE ONLY)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TAD/DBHV Threshold DAC Range	Recommended range for DBHV measurement only is 150-200mV. No restrictions on the TAD threshold.	6		762	mV
TAD/DBHV Threshold DAC Resolution			7		bit
TAD/DBHV Threshold DAC LSB			6		mV
DBHV Tolerance (independent of Imr)	Includes both the TAD/DBHV Threshold DAC tolerance and DBHV comparator tolerance.	-12		12	%
TAD Tolerance (independent of Imr)	Includes both the TAD/DBHV Threshold DAC tolerance and the TAD comparator tolerance.	0		40	%

NOTE: The TAD and DBHV comparators are two independent and completely different circuits.

READ CHARACTERISTICS

Rmr = 45 Ω, Imr = 6.0 mA

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance	Recommended	25	45	80	Ω
MR Bias Current	Typical range	2.12		9.56	mA
MR Bias Current Resolution			5		bit
LSB	Rref = 2 KΩ		24		µA
MR Current Tolerance	MR DAC range 5 – 31 MR DAC range 0 – 4	-8 –12		+8 +12	% %
MR Head DC Voltage Range				0.8	V
Unselected Head Current				15	µA
Input Resistance	Differential, Imr = 5.0 mA		500		Ω
Differential Voltage Gain	R_{MR} = 45Ω, Imr = 5.0 mA 1 mV p-p @ 20MHz GAIN = 0 GAIN = 1	 67 95	 79.4 112	 91 129	 V/V V/V
Bandwidth	Lower -3dB Lower -3dB, Fast recovery Higher -1dB Higher -3dB, Rmr = 45	 300	1.0 3.5 230	1.5 450	MHz MHz MHz MHz
Input Voltage Noise	R_{MR} = 45, Imr = 5.0 BW =10 to 100 MHz		0.70		nV/√Hz
Input Current Noise	R_{MR} = 45, Imr = 5.0 BW =10 to 100 MHz		13		pA/√Hz
Dynamic Range	Gain falls to 90% @ 5 MHz	8			mV
Output Offset Voltage		-250		250	mV
Output Current			2.8		mA
Output Voltage	RDX,RDY		VCC – 1.6		V
Output Resistance	Single-ended	24	40	64	Ω
PSRR	@ 25 MHz, no bypass caps	TBD	40		dB
Channel Separation	@ 25 MHz, no bypass caps	TBD	30		dB
CMRR	@ 25 MHz, no bypass caps	TBD	40		dB
I/O Rejection	WDX, WDY, SDEN, SCLK, SDATA, R/XW,XIMRON, FLT @ 25 MHz, no bypass caps	TBD	55		dB

WRITE/SERVO CHARACTERISTICS

Iw=40 mA, Lh = 90 nH, Rh = 11 Ω,Ch = 1/2/1 pF, WCB = 001, USC =101, WBD =11

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range	Typical	15.75	40	62.25	mA
Write Current Resolution			5		bit
LSB			1.5		mA
Write Current Accuracy	DC conditions	-8		+8	%
Boost Current Range	DC conditions	15		55	mA
Boost Current Resolution			3		bits
Boost Current LSB			9		mA
Boost Current Accuracy	DC conditions	-8		+8	%
Boost Delay Resolution			2		bits
Undershoot Current Resolution			3		bits
Differential Head Swing	Open Head,	7.5			Vpp
Unselected Head Current	DC Transient			100 1	µA mA pk
Common Mode head Voltage	Selected head, read mode		0		V
Common Mode head Voltage	Unselected head, all modes except selected head, Idle		0.5		V
Damping resistor	See note		1.6		KΩ
WDX/WDY Input Resistance	Internal Termination		130		Ω

NOTE: This is the DC resistance across head, it is not the primary writer damping control. Device uses active overshoot/undershoot control for writer

SWITCHING CHARACTERISTICS

Rmr = 45 Ω, Imr = 6.0 mA,Iw=40 mA, Lh = 80 nH, Rh = 11 Ω,Ch = 1/2/1 pF, WCB = 001, USC =101, WBD =11

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Write to read	R/XW	90% signal envelope, ±30mV DC. XIMRON= 0		300	480	ns
Write to Read	R/XW	10% of Iw, single head write			20	ns
		10% of Iw, servo bank write			20	ns
Read to write	R/XW	90% of Iw, single head read			20	ns
	R/XW	90% of Iw, servo bank write	5	18	35	ns
Idle to read		90% signal envelope, ±30mV DC			13	µs
Read-Inactive to Read-Active		90% signal envelope, ±30mV DC (XIMRON 1 to 0 toggle)		2	4	µs
Write to idle		10% of Iw			20	ns
Head Switching	HSn	90% signal envelope, ±30mV DC			13	µs
Write Current rise/fall time		Lh=80nH, Iw=40 mA, Rh = 11Ω, ACB = 100, 10% to 90%		0.8	0.9	ns
Write Current undershoot		% of Iw steady state, WCB = 000 USC = 000 USC = 111		 30 0		 % %
Write Current overshoot		% of Iw steady state, USC = 101, WBD = 101 WCB = 000 WCB= 111		 54 132		 % %
Write Current settling time		95% to 105% of Iw steady state WCB = 000, USC = 101			8	ns
Head Current delay	TD3	50% of WD to 50% of Iw			5	nS
Write Current asymmetry		Propagation delay difference		100		pS

HEAD UNSAFE DETECTION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FLT low to high, TD1	No write data transition		500		µS
FLT high to low, TD2			20		nS
Write data frequency	Valid transient detector		160	TBD	MHz
	Valid Open detector			TBD	MHz
MR head open threshold		800	1000	1250	mV
MR head short threshold			35	60	mV

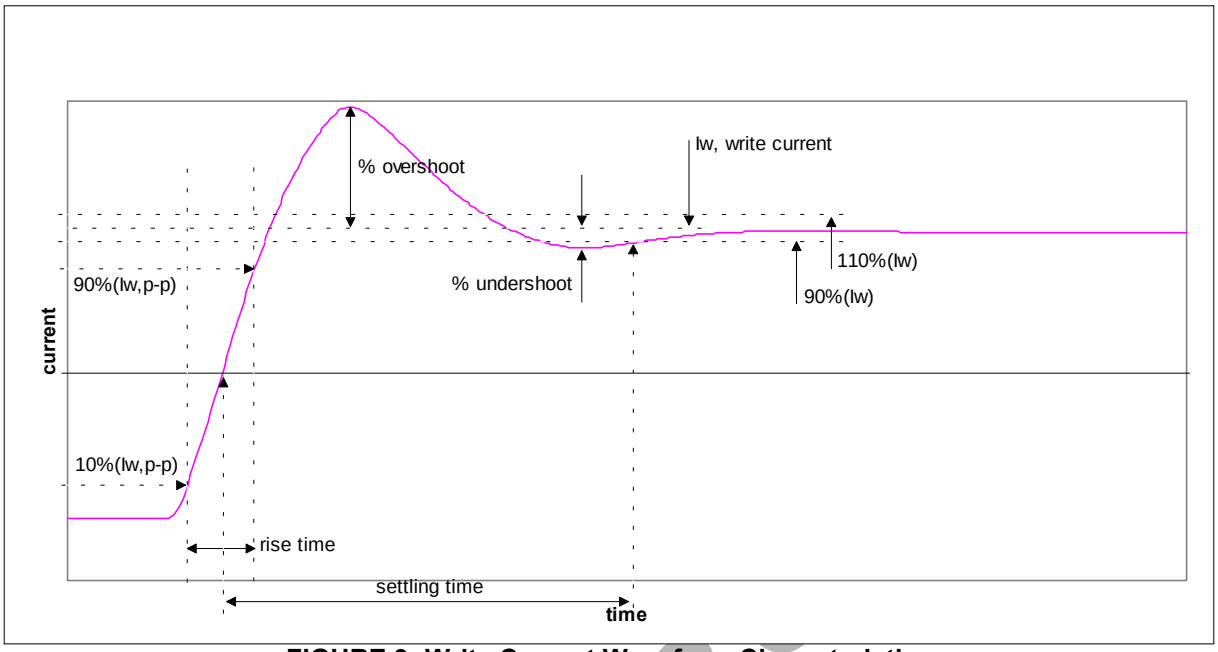


FIGURE 3: Write Current Waveform Characteristics

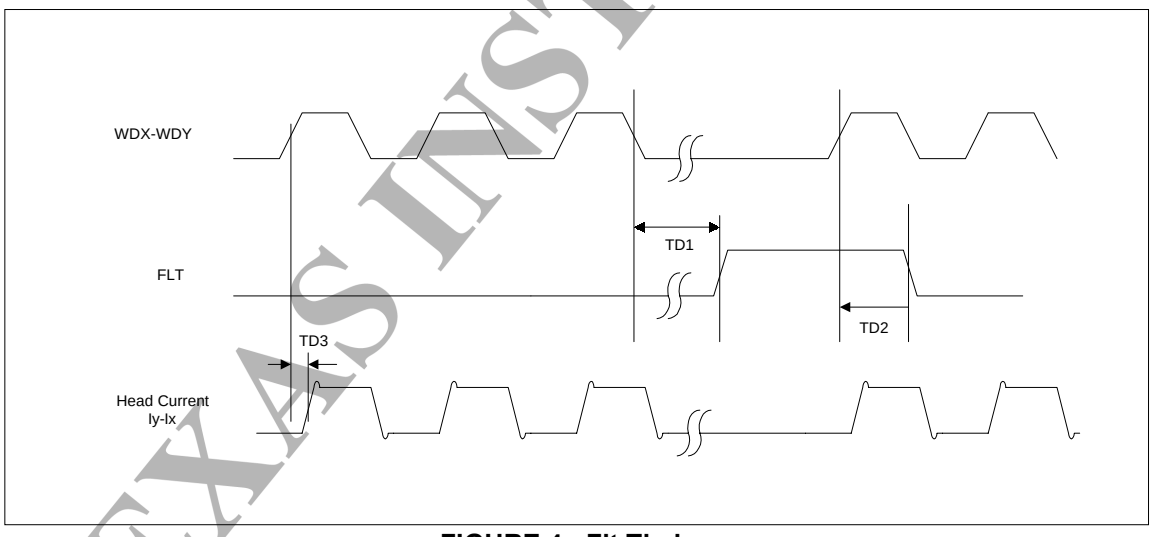
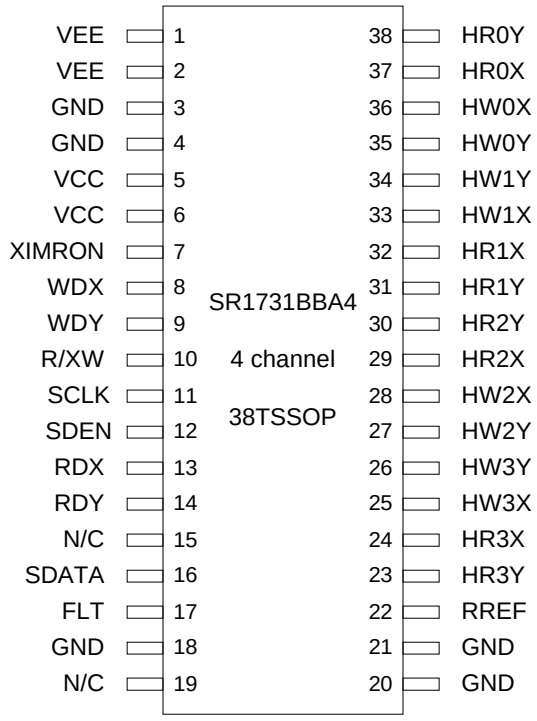


FIGURE 4: FIt Timing

PACKAGE PIN DESIGNATIONS



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Abridged Version

SR1760A
+5/-5V 4-CHANNEL MR READ/WRITE DEVICE

Prototype

May, 2000

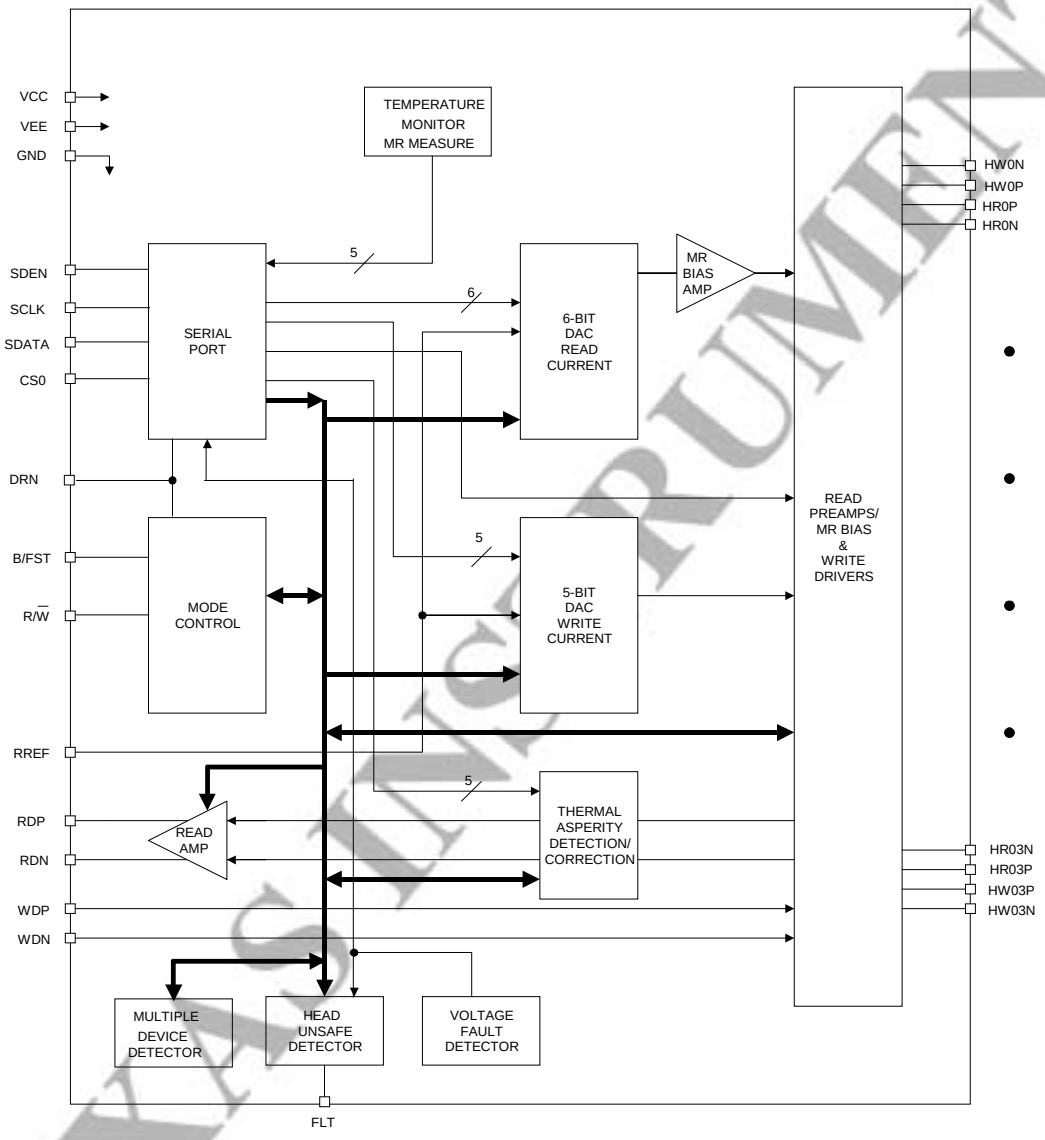
DESCRIPTION

The TI SR1760ACA4 is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. The reader architecture is MR voltage bias/voltage sense, current bias/voltage sense and will support a user data rate of up to 700 Mbits/sec. A read/write capable serial port is provided to enable the implementation of on-chip MR bias and Write current DACs. The device provides a write driver, low-noise read amplifier, serial port controlled head selection, write current, MR read bias current and read and write fault detection circuitry for up to four channels. The device requires +5V and -5V and comes in die form or 48-pin TQFP package.

FEATURES

- **+5V ±10%, -5V ±10% supplies**
- **Supply voltage fault monitor**
- **MR head resistance range = 25 – 80Ω**
- **MR bias current range =2.5 – 10mA (6-bit)**
- **Programmable read gain = 41, 44 and 47 dB @ RMR=45Ω**
- **Programmable read bandwidth, 400MHz min (lower –3dB, higher –3dB and high frequency boost)**
- **Read input voltage noise = 0.55 nV/√Hz @RMR=0**
- **Read input current noise = 10 pA/√Hz @RMR=45 IMR=5mA**
- **MR measurement mode**
- **Write to read recovery = TBD ns (to 10mV of baseline)**
- **Write current rise/fall time = 550ps (nominal, 10-90%,Iw=50mA,Lh=45nH, Rh=16Ω, C=1pf)**
- **Programmable write current range = 10 – 50mA 0-pk (5-bit)**
- **3V compatible analog and digital interface**
- **Voltage or current mode PECL write data input**
- **Thermal asperity detection and correction**
- **Temperature monitor**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

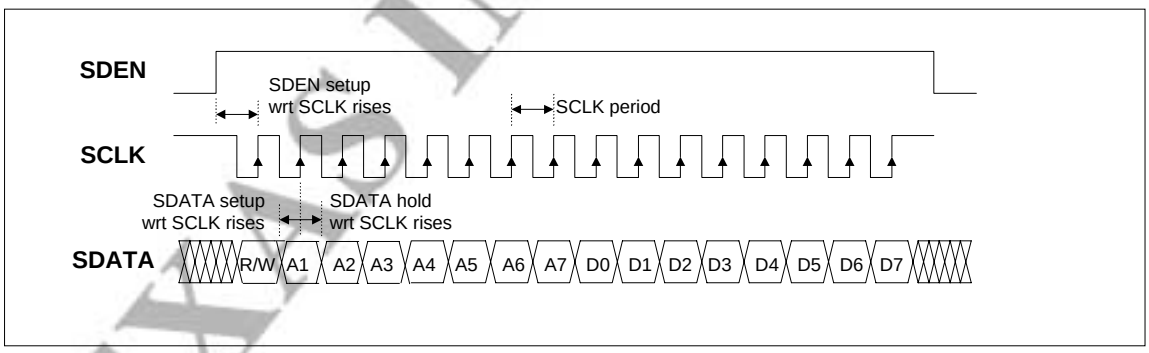
The TI SR1760ACA4 addresses up to 4 four-terminal MR heads providing write drive or read bias and amplification. The selection of the chip is done via controls CS0, CS1 and STWN in conjunction with the serial interface address bits A1 and A2. CS0 is a device pin and has an internal pull up resistor. CS1 is internally tied to a low level for the SR1760ACA4. Serial port bit STWN activates servo track writing and is located in Register 0. CS0 and CS1 must be matched by two address bits A1 and A2 respectively for a preamp to be selected. The three-line serial data interface, with both read/write capabilities, is used to control head selection, write current, MR bias current, and mode control. The serial data port includes 10 read/write capable data registers and 1 read-only ID register. The three serial interface pins, SDEN, SDATA and SCLK, have internal pull-down resistors.

SERIAL INTERFACE OPERATION

The serial data port is used to control head selection, bankwrite, write current, MR head resistance measurement, MR bias current, read gain, and operational mode. The serial port bit map is shown in Table 5.

A complete data transfer is sixteen (16) bits long: eight (8) address bits and eight (8) data bits. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit (A0) is the R/W bit which is high for a read operation. The next two bits (A1,A2) are the device select bits and must match the CS0,CS1 pins respectively in order for the preamp to respond to the command. CS1 is internally set = 0 on the 4 channel versions. The following five bits (A3-A7) are the address bits and the last eight (D0-D7) are the data bits. (See Serial Port Bit Map).

Asserting the serial port enable line SDEN (TTL) initiates a transfer, SDATA (TTL) is clocked into the internal shift register by the rising edge of SCLK (TTL). A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

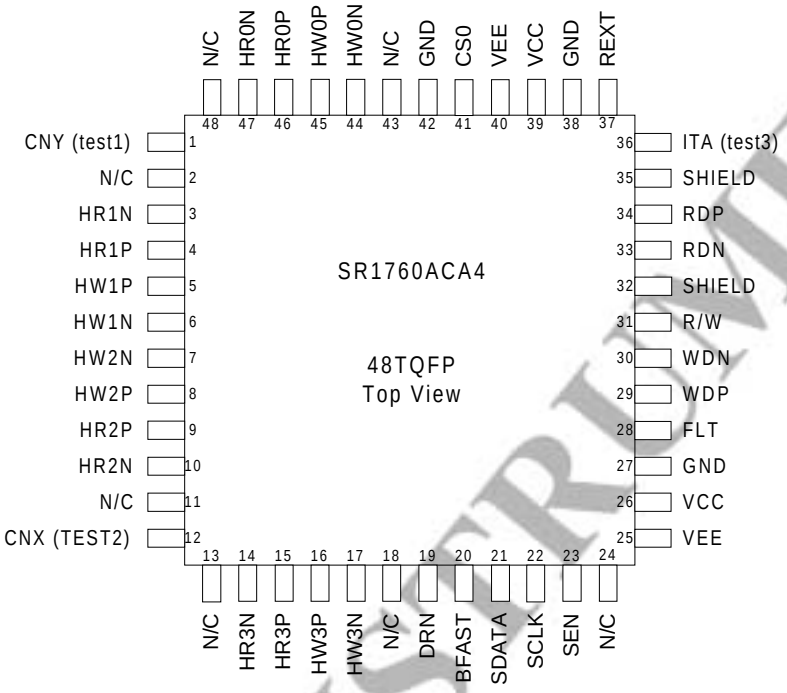


PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RWN	input*	Read/Write: a high level enables the read mode. Internal pull up.
SEN	input*	Serial Enable line. Active High. Internal pull down.
SCLK	input*	Serial Clock line. 40 MHz max.
SDAT	input*	Serial Data line. Bi-directional interface
FLT	output*	Fault active high in write mode, low in read mode. Open collector.
WDP, WDN	input*	Differential PECL or current mode write data inputs
HR0P-HR3P	input	MR head connections, positive end
HR0N-HR3N	input	MR head connections, negative end
HW0P-HW3P	output	Write head connections, positive end
HW0N-HW3N	output	Write head connections, negative end
RDP, RDN	output*	Read Data, Differential read signal outputs
Rext	output	Voltage global reference for the biassing circuits
CS0	input	Chip Select
VEE	input*	-5V supply
GND	input*	Ground
VCC	input*	+5V supply
BFAST	input*	Controls reader passband or enables the Imr generator depending on the state of BFCTL bit from Reg.01. Internal pull down.
DRN	input*	Selects the dummy head or performs a system reset depending on the state of RSTDMY bit from Reg.09. Internal pull up.
CNX, CNY, ITA	Test	TI Test pins. User setting = n/c

* When more than one device is used, these signals can be wire OR'd together
WDP and WDN should not be wire OR'ed if used in current mode

PACKAGE PIN DESIGNATIONS



Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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2000

THIN-FILM HEAD READ/WRITE

Return to the Table of Contents

SSI 32R2410R/12R
+5 V, 2-, 4-Channel Thin Film Read/Write Device

February 1998

DESCRIPTION

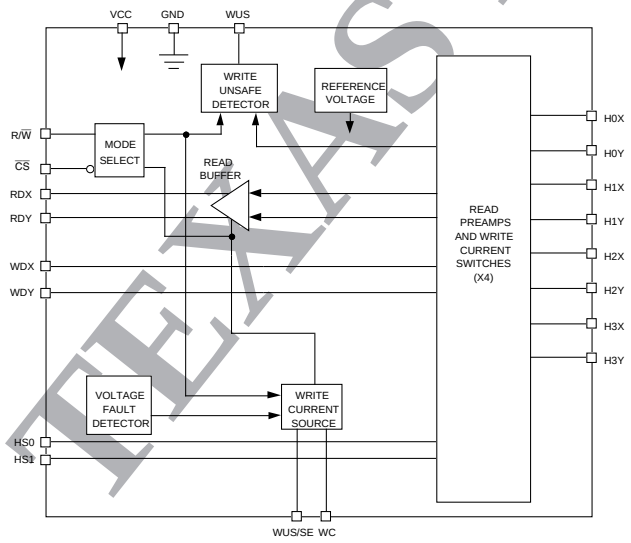
The SSI 32R2410R/12R are BiCMOS monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2410R/12R option provides internal 350 Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance. The device also offers multiple channel "servo bank write" capability to assist in servo writing operations.

The SSI 32R2410R/12R requires only a +5 V power supply and are available in a variety of packages.

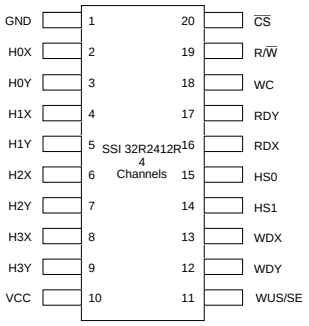
FEATURES

- **+5 V ±10% supply**
- **Low power**
  - **PD = 150 mW read mode (nominal)**
  - **PD = 1.0 mW idle (nominal)**
- **High Performance:**
  - **Read mode gain = 285, 350 V/V**
  - **Input noise = 0.45 nV/√Hz (nominal)**
  - **Input capacitance = 6 pF (nominal)**
  - **Write current range = 3-20 mA**
  - **Nominal write current (10 mA) rise/fall time = 2.3 ns (nominal) (0.5 μH head)**
  - **Head voltage swing = 8 Vp-p (nominal)**
- **Servo bank write capability**
- **Self switching damping resistance**
- **Write unsafe detection**
- **Pin compatible with the SSI 32R2210R/11R/12R**
- **Power supply fault protection**
- **Head short to ground protection**
- **Differential ECL-like (SSI 32R2410R/12R) or**
- **Write data flip-flop (SSI 32R2410R) or no flip-flop (SSI 32R2412R)**

BLOCK DIAGRAM



PIN DIAGRAM



20-Lead SOV, SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32R2410R/12R have the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pull-down resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	WUS/SE	MODE
0	0	*	Single Channel Write (see Table 2)
0	0	**	Servo Write
0	1	X	Single Channel Read (see Table 2)
1	X	X	Idle

* WUS/SE is a WUS output unless pulled above VCC.

** Servo write mode is activated through the WUS pin as described in the servo write mode section.

TABLE 2: Head Select

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

TABLE 3: Head Select in Servo Write Mode*

HEAD SELECT ADDRESS		HEAD SELECTED IN
HS1	HS0	SERVO WRITE MODE
0	0	0, 1
0	1	0, 1
1	0	0, 1, 2, 3
1	1	0, 1, 2, 3

* NOTE: For 2-channel parts, heads 0 & 1 are selected in servo write mode, independent of head select address.

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2410R/12R as a current switch and activates the Write Unsafe (WUS) detector circuitry. On the SSI 32R2410R, head current is toggled between the X and Y side of the selected head on each low to high transition of WD-$\overline{WD}$. Note that a preceding read to write transition or idle to write transition initializes the write data flip-flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. With the SSI 32R2412R, head current is toggled between the X and Y side of the head on each WDX–WDY transition. When the potential of WDX is higher than WDY, the potential on the X side of the head is higher than the Y side (HNY is sinking current). The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \bullet \frac{Vwc}{Rwc} = K \diagup Rwc$$

where Aw is the write current gain.

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

Where:
$$I\,x,y = \frac{Iw}{1+Rh/Rd}$$

Rh = head resistance plus external wire resistance; and

Rd = damping resistance.

In write mode a damping resistor is switched in across the Hx, Hy ports. With no current boost, the values are 2.6 kΩ, 800 Ω, 500 Ω and 350 Ω. With current boost the values are 500 Ω, 350 Ω, 275 Ω and 225 Ω.These values are selectable by bond option on SSI 32R2410R/12R only.

SERVO WRITE MODE

This mode allows for writing to multiple channels at once, which is useful during servo formatting.

To enable servo write mode follow these steps:

(1) Place the device in the read mode (R/W high).

(2) Set the head select lines to an address that corresponds to the bank of heads desired for servo write (see Table 3).

(3a) If SE pin is available, make it low.

(3b) If SE pin is not available, pull the WUS output above VCC by sourcing 5 mA of current into the pin. Two ways to source this current are: (a) use a voltage source set to VCC +1.9 V limited to 5 mA current, or (b) use a resistor tied between WUS and a supply above VCC to source the current. With 5 mA of current, WUS will rise to approximately VCC +1.5 V.

(4) Allow at least 1 µs set-up.

(5) While maintaining steps (2) and (3) above make R/W low, placing the device in servo write mode.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power start-up regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The SSI 32R2410R/12R provides a head short to ground protection circuit in write mode. If the selected head is shorted to ground the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port. Note that any unselected head is pulled to ground through internal circuitry. In the idle mode, all heads are similarily pulled to ground.

In read mode, current out of the selected head port will not exceed 3 mA if the head is shorted to ground.

WRITE UNSAFE

Upon entering write mode, WUS is initialized low. Any of the following conditions will be indicated as a high level on the Write Unsafe (WUS) open collector output.

- Write data frequency too low
- Device in read mode
- Device not selected
- No head current
- Open head
- Head short to ground

WRITE UNSAFE (continued)

To insure no false WUS trigger, the DC head resistance should be less than 100 Ω. The open head detect circuit is also disabled when write data frequency is above 5 MHz to prevent false WUS detect.

WD frequency too low is detected if the write data frequency falls below 1 MHz. Consult the WUS safe to unsafe timing for range of frequency detection.

Device in read mode, device in servo write mode and chip disabled will flag WUS if R/$\overline{W}$ is high, if servo write mode is activated, or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

Head opened will flag WUS if Rh = ∞ and the write data frequency is less than 5 MHz.

Head short to ground is described in the preceding paragraph.

READ MODE

The read mode configures the SSI 32R2410R/12R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in idle or write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from write to read mode. Note also that the write current source is deactivated for both the read and idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

PIN DESCRIPTION

CONTROL/STATUS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	CHIP SELECT INPUT: A logical low level enables the device. This pin has an internal pull-up.
R/$\overline{W}$†	I	READ/WRITE: A logical high level enables read mode. A logical low level enables write mode. This pin has an internal pull-up.
HS0, HS1	I	HEAD SELECT: Decoded address (internal pull-down) selects one of 4 channels (see Table 2).
WUS/SE†	I/O	WRITE UNSAFE/SERVO ENABLE: When in servo bank write mode, pulling this pin above VCC enables servo bank write (see servo write mode section). Otherwise, a high level indicates an unsafe writing condition (see WUS section).
$\overline{SE}$	I	SERVO ENABLE: A logic low enables servo write mode.
WC†	I	WRITE CURRENT: A resistor to ground from WC sets the write current through the recording head.

HEAD TERMINAL CONNECTIONS

H0X-H3X H0Y-H3Y	I	X, Y Head Connections

DATA INPUT/OUTPUT

WD, $\overline{WD}$† (SSI 32R2410R)	I	DIFFERENTIAL WRITE DATA IN: A positive transition of WD-$\overline{WD}$ changes the direction of current in the recording head.
WDX, WDY (SSI 32R2412R)	I	DIFFERENTIAL WRITE DATA IN: Each transition of WDX–WDY changes the direction of current in the recording head.
RDX, RDY†	O	DIFFERENTIAL READ DATA OUT: Emitter follower output.

POWER

VCC	I	+5 V Power Supply
GND	I	Ground

† When more than one read/write device is used, signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC	-0.3 to 6 VDC
Write Current	Iw	65 mA
Digital Input Voltage	Vin	-0.3 to VCC +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC +0.3 VDC
WUS Pin Voltage	Vwus	7.5 VDC
Output Current RDX,RDY	Io	-10 mA
WUS		7.5 Vdc
Storage Temperature		-65 to +150° C

SERVO BANK WRITE MODE CONSTRAINTS

Operation beyond ratings in servo bank mode may permanently damage the device.

DC Supply Voltage	VCC	4.5–5.0 Vdc
Junction Temperature	Tj	+135° C
Ambient Temperature	Ta	Less than 30° C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC	5 ± 10%V
Operating Junction Temperature	Tj	0 to ± 125° C
Head Load Range	Lh	0.4 ± 1.0 µH

TEST CONDITIONS

Recommended operating conditions apply.

Write Current	Iw	10 mA
Head Inductance	Lh	0.5 µH
Head Resistance	Rh	30 Ω
Head Capacitance	Ch	3.0 pF
WD Frequency		5 MHz
WD, $\overline{WD}$ Rise/Fall Time	SSI 32R2410R	1 ns
WDX, WDY Rise/Fall Time	SSI 32R2412R	1 ns

POWER DISSIPATION

Recommended operating conditions apply.

PARAMETER	CONDITION		MIN	NOM	MAX	UNIT
VCC Supply Current	Read Mode	Iw = 10 mA		33	45	mA
	Write Mode	Iw = 10 mA		33	40	mA
	Servo Mode	Iw = 10 mA 4 channel		77	110	mA
	Idle Mode			0.07	1	mA
VCC Power Dissipation	Read Mode	Iw =10 mA		165	248	mW
	Write Mode	Iw = 10 mA		165	220	mW
	Idle Mode			0.35	5.5	mW
	Servo Mode	Iw = 10 mA 4 channel		385	605	mW

DIGITAL INPUTS

Input Low Voltage.	Vil				0.8	VDC
Input High Voltage,	Vih		2.0			VDC
Input Low Current $\overline{CS}$	Iil	Vil = 0.8 V	-400	-15		µA
Input Low Current $\overline{CS}$	Iih	Vih = 2.0 V		-15	100	µA
Input Low Current, R/$\overline{W}$, $\overline{SE}$	Iil	Vil = 0.8 V	-400	-30		µA
Input High Current, R/$\overline{W}$, $\overline{SE}$	Iih	Vih = 2.0 V		-30	100	µA
Input Low Current, HSO, HS1	Iil	Vil = 0.8 V	-400	20		µA
Input High Current, HSO, HS1	Iih	Vih = 2.0 V		20	100	µA
Input High Current, WDX, WDY, WD, $\overline{WD}$	Iih			2	50	µA
Input Low Current, WDX, WDY, WD, $\overline{WD}$	Iil		-20	0	20	µA
WUS Output Low Voltage,	Vol	Iol = 2 mA max		0.2	0.5	VDC
WUS Output High Current,	Ioh	Voh = Vcc		0.2	100	µA
Input High Voltage, WDX, WDY, WD, $\overline{WD}$	Vih		VCC-1.1		VCC-0.4	V
Input Diff, WDX, WDY, WD, $\overline{WD}$	Vih-Vil				0.4	V

ELECTRICAL SPECIFICATIONS (continued)

WRITE CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range		3		20	mA
Write Current Voltage Vwc		1.90	2	2.10	V
Write Current Gain Aw	Iw = Aw • Vwc/Rwc	22.5	25	28.5	mA/mA
Write Current Constant "K"	Iw = K/Rwc	45	48	56	V
Differential Head Voltage Swing	open head, Iw = 20 mA	7	8		Vp-p
Write Current Matching	shorted head	-5	0	5	%
WD, $\overline{WD}$ Minimum Pulse Width		1			ns
Unselected Head Voltage			0	0.1	VDC
			0	0.2	mA

WRITE FAULT PROTECTION

Write test conditions apply unless specified otherwise.

VCC Fault Voltage	Vcc threshold where write is inhibited	3.6	3.9	4.2	V
WD Minimum Frequency	frequency threshold where WUS flags	380	500	700	kHz
Safe to Unsafe	see TD1 in Figure 1	0.6	1.0	1.6	µs
Unsafe to Safe	see TD2 in Figure 1		150	200	ns

READ CHARACTERISTICS

Test conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVp-p @1 MHz SSI 2410RX/12RX	250	285	330	V/V
		SSI 2410RY/12RY	290	350	410	V/V
Voltage BW	-1 dB	|Zs| < 5 Ω, Vin = 1 mVp-p	40	55		MHz
	-3 dB		75	92		MHz
Input Noise Voltage		BW = 20 MHz, Lh = 0, Rh = 0		0.52	0.68	nV/√Hz
Differential Input Capacitance		Vin = 1 mVp-p, f = 5 MHz	2	5.5	10	pF
Differential Input Resistance		Vin = 1 mVp-p, f = 5 MHz	450	685		Ω
Dynamic Range- Gain Compression		AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	6		mVp-p
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVp-p @ 5 MHz	50	75		dB
Power Supply Rejection Ratio		100 mVp-p @ 5 MHz on VCC, shorted head	50	70		dB
Channel Separation		Unselected channels driven with Vin = 0 VDC + 100 mVp-p, @ 5 MHz	50	65		dB
Output Offset Voltage		Lh = 0, Rh = 0	-250		+250	mV
Single-Ended Output Resistance		f = 5 MHz		20	50	Ω
Output Current		AC coupled load, RDX to RDY	3.4	4		mA
RDX, RDY Common Mode Output Voltage			VCC-1.8 V	VCC -2.4	VCC-3 V	VDC

ELECTRICAL SPECIFICATIONS (continued)

SWITCHING CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Read to Write R/$\overline{W}$	R/$\overline{W}$ to 90% of write current		15	50	ns
Write to Read	R/$\overline{W}$ to 90% of 100 mV read signal envelope		120	200	ns
Idle to Read $\overline{CS}$	CS to 90% of 100 mV 10 MHz read signal envelope		120	400	ns
Write to Read	To 10% Iw		10	50	ns
Write to Idle	To 10% Iw		50	100	ns
Read to Idle	To 10% V (Rdx, y)		50	100	ns
Head to any Head	To 90% Iw		50	100	ns
Head to Head (Read)	To 90% of 100 mV 10 MHz read signal envelope		200	215	ns
WD to Ix - Iy (TD3)	From 50% points (Lh = 0, Rh = 0)		3.3	8.0	ns
Asymmetry	WDI has 1 ns rise/fall time (Lh = 0, Rh = 0)	-0.5	0	0.5	ns
Rise/Fall Time	10% to 90% points Iw = 10 mA, Rh = 0, Lh = 0		1	2	ns
	Iw = 10 mA, Rh = 30Ω, Lh = 0.5 µH		2.3	2.8	ns

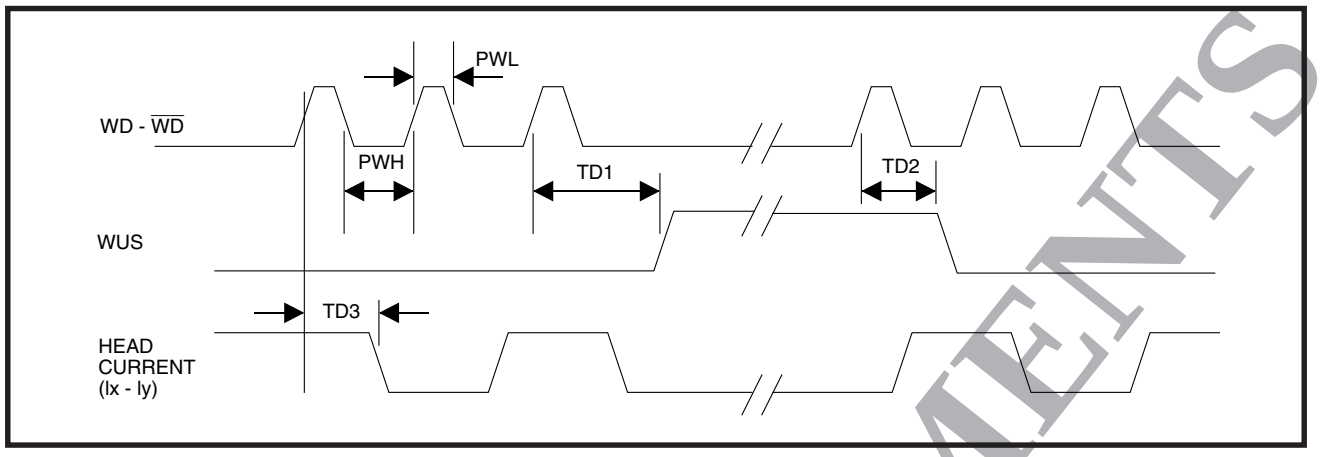


FIGURE 1: SSI 32R2410R Write Mode Timing Diagram

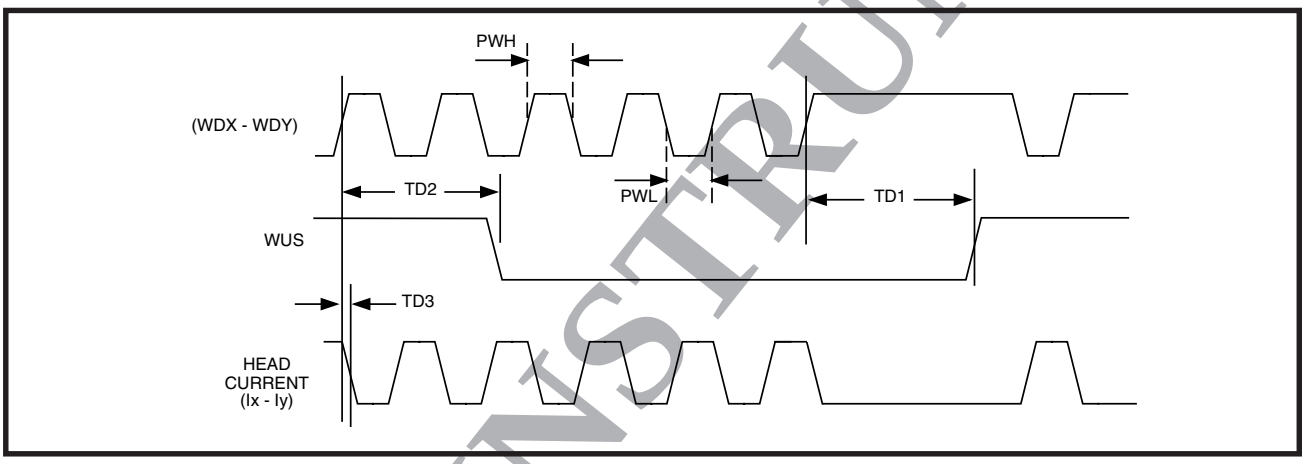


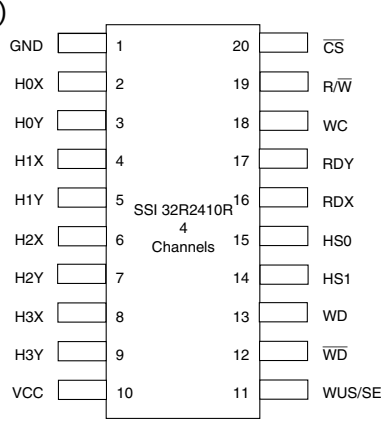
FIGURE 2: SSI 32R2412R Write Mode Timing Diagram

SSI 32R2410R/12R
+5 V, 2-, 4-Channel Thin Film Read/Write Device

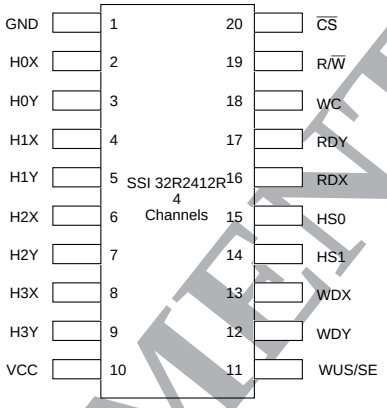
CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS

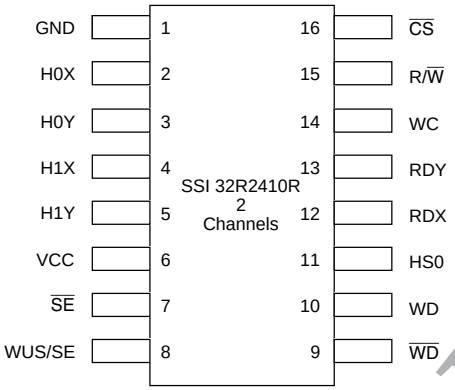
(Top View)



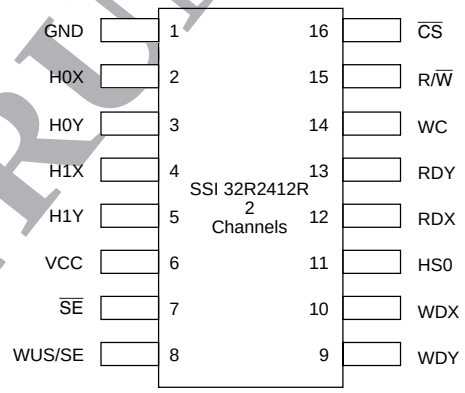
20-Lead SOV, VTSOP



20-Lead SOV, VTSOP



16-Lead SON, VTSOP



16-Lead SON, VTSOP

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32R2410R	20-VTSOP, 4ch	32R2410RX-4CVT	32R2410RX-4
	Die sales	32R2410RY-4CI	32R2410RY-4CI
	20-SOV, 4ch	32R2410RY-4CV	32R2410RY-4CV
SSI 32R2412R	16-SON, 2ch	32R2412RX-2CN	32R2412RX-2
	16-VTSOP, 2ch	32R2412RX-2CVT	32R2412RX
	20-SOV, 4ch	32R2412RX-4CV	32R2412RX-4
	20-VTSOP, 4ch	32R2412RX-4CVT	32R2412RX-4
	20-SOV, 4ch	32R2412RY-4CV	32R2412RY-4

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

TLS21H62

5 V Thin-Film 2-Channel Low-Noise Read/Write Preamplifiers

Preproduction

April 1999

DESCRIPTION

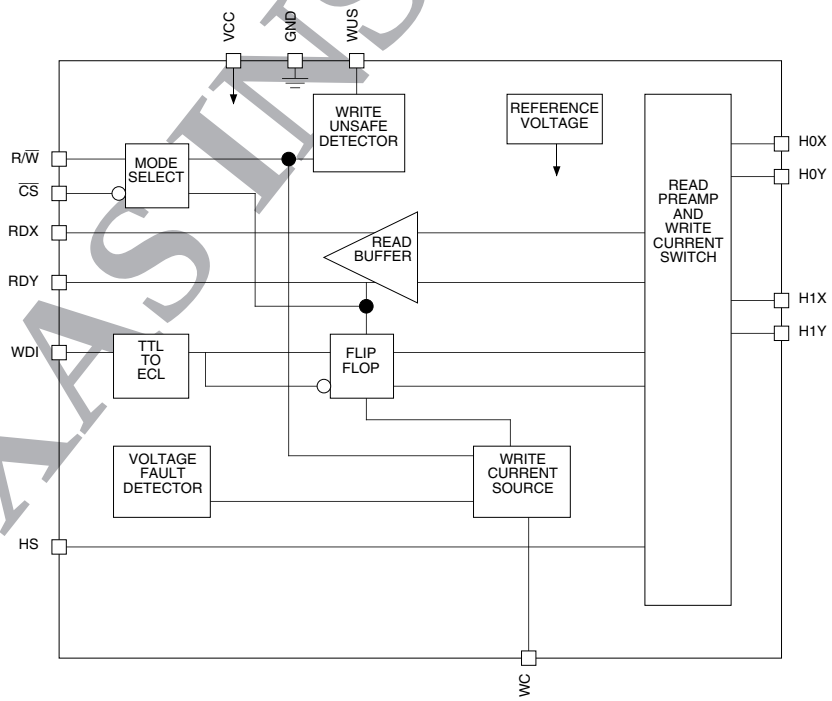
The TLS21H62 is a BiCMOS, monolithic preamplifier family designed for two-terminal thin-film or MIG recording heads. The device provides data protection circuitry for both channels with low-noise read paths and write-current controls. When deactivated, the device enters an idle mode that reduces power dissipation to 0.5 mW. The write current generator is disabled during power sequencing to provide power supply fault protection.

During write and idle modes, the RDX and RDY lines are put into a high impedance state in order to improve system write-to-read and idle-to-read recovery times. Isolated damping resistors effectively switch out the resistance during read operations by Schottky diode.

FEATURES

- **5 V ±10 % Power supply**
- **Low power dissipation:**
  - **Read mode .... 115 mW typ**
  - **Idle mode .... 0.5 mW typ**
- **High performance:**
  - **Read mode gain .... 300 V/V typ**
  - **Input noise .... 0.50 nV/√Hz typ**
  - **Input capacitance .... 8.5 pF typ**
  - **Write current range .... 5 mA to 15 mA**
- **Designed for two-terminal thin-film or metal-in-gap (MIG) recording head**
- **Programmable write-current source**
- **Power supply fault protection**
- **Write unsafe detection**
- **Schottky - isolated damping resistor**
- **Power up/down protection**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

The device functions as a read amplifier or write driver for the selected head and has the capability of addressing two, two-terminal thin-film or metal-in-gap (MIG) recording heads. R/$\overline{W}$ and $\overline{CS}$ are connected to internal pull-up resistors. An Internal pull-down resistor is connected to HS.

TABLE 1: Head Select for TLS21H62

HS	HEAD
0	0
1	1

TABLE 2: Mode Select for TLS21H62

R/$\overline{W}$	$\overline{CS}$	MODE
0	0	Write
1	0	Read
X	1	Idle

Read Mode

Read mode is selected by taking $\overline{CS}$ low and R/$\overline{W}$ high. The head select input HS selects the appropriate head. In read mode, the device operates as a low-noise differential amplifier that deactivates the write current generator. The read-data outputs RDX and RDY are emitter-follower driven and should be externally AC coupled to the load. The read mode recovery time is reduced by putting RDX and RDY into high-impedance states during write and idle modes, maintaining the voltages on the AC coupling capacitors. The damping resistor is isolated by diodes that effectively remove the resistor from the circuit during the read mode.

Write Mode

Write mode is selected by taking both $\overline{CS}$ and R/$\overline{W}$ low. The head select input HS selects the appropriate head. In write mode, the circuit acts as a current switch and write current toggles between the X and Y directions of the head. Write current is toggled on the high-to-low transition of the WDI input for TLS21H62-3 PW.

A preceding read or idle mode initializes the write data flip-flop to pass write current from the Y side to the X side of the head.

During the write mode, the high output level turns the diode on which switches the damping resistor into the circuit. The value of the write current is given by:

$$I_W = K_W / R_{WC} = 50/R_{WC}$$

Where:

K_W = write current constant

R_{WC} = external resistor connects WC pin to GND pin

Ix-Iy (FF) = write current

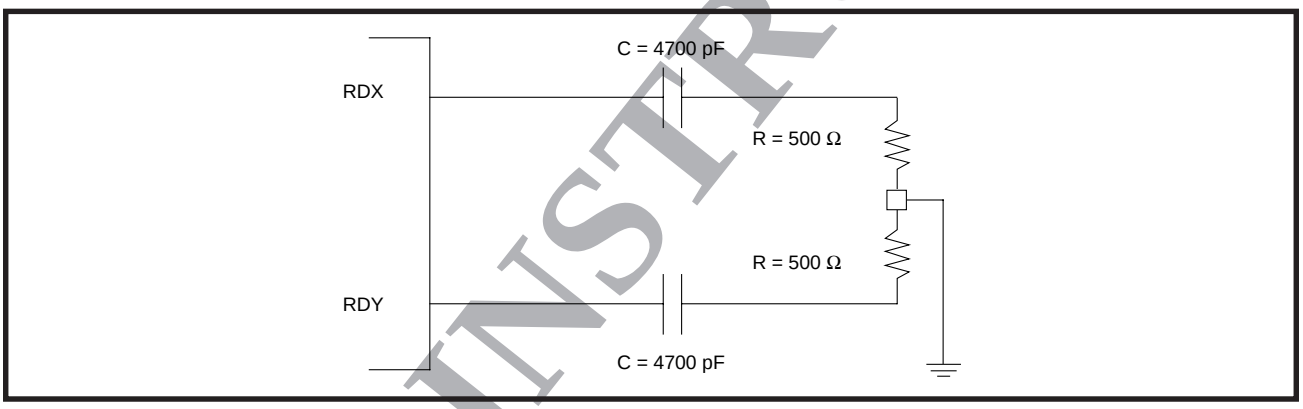


FIGURE 1: AC Load For RDX,RDY

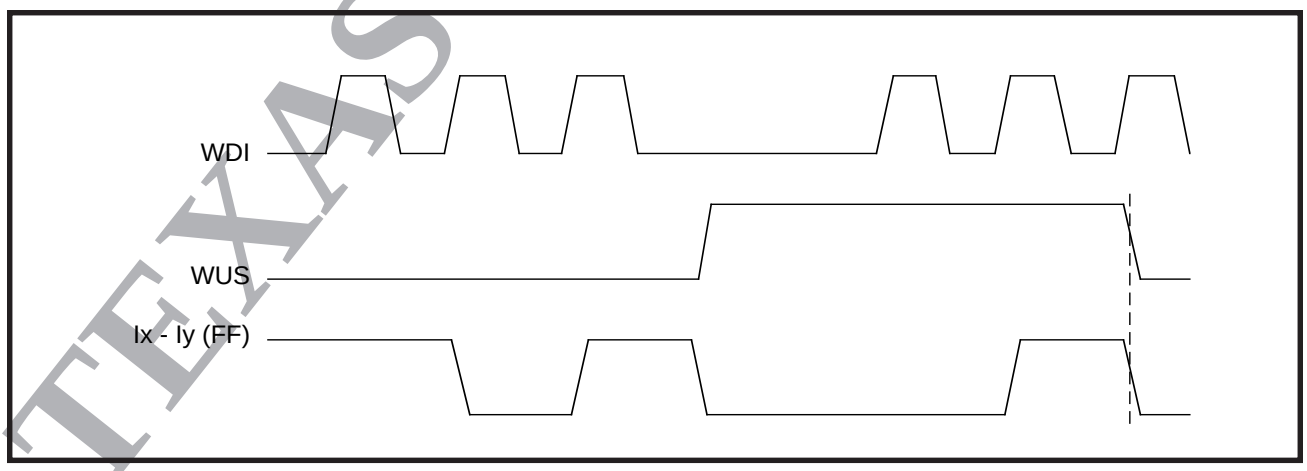


FIGURE 2: Write Mode Timing Diagram

CIRCUIT OPERATION (continued)

Idle mode

Idle mode is selected by taking $\overline{CS}$ high. The internal write-current generator and write-unsafe detector are deactivated. The read outputs can be wire-ORed and a single write-current programming resistor can be used to select write current for a multi-device application. This device is specially designed for low-power dissipation in the idle mode.

Fault Detection

A voltage-fault detection circuit is provided to disable the write-current generator during power startup or voltage fault in any mode. Any of the following conditions causes WUS to go high, indicating a fault.

- Write current is zero
- Device is read mode
- Frequency on WDI is too low
- Device not selected
- Head short to ground
- Head open
- Low Vcc

One positive transition on WDI is required to clear WUS after the all fault condition except Frequency on WDI is too low is removed.

Frequency fault will clear after detecting a safe frequency; therefore, at least one complete period is required for clear this fault. Once safe frequency is detected, one negative transition on toggled WDI will clear this fault.

The head open fault will detect when Rh = ∞ and the write data frequency is less than 10 MHz.

PIN DESCRIPTION

TLS21H62 TERMINAL FUNCTIONS (16-PIN TSSOP)

NAME	TYPE	DESCRIPTION
GND	-	GND
H0X	I/O	X - Head Connection
H0Y	I/O	Y - Head Connection
H1X	I/O	X - Head Connection
H1Y	I/O	Y - Head Connection
WUS	I/O	Write Unsafe
WDI	I	Write Data In - TTL input
VCC	-	VCC
HS	I	Head Select
RDX	O	Read Data - Positive Differential Output
RDY	O	Read Data - Negative Differential Output
WC	I	Write Current Set - Can be wired ORed when more than one device is used
R/$\overline{W}$	I	Read /Write Set High for Read Mode
$\overline{CS}$	I	Chip Select: High inhibits chip

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE
(Unless otherwise noted) Operation outside these rating limits may cause permanent damage to this devise.

PARAMETER		RATING
Supply voltage range, Vcc (See Note 1)		-0.3 V to 6 V
Input Voltage Range, Vi (digital)		-0.3 V to Vcc + 0.3 V
Head port voltage range		-0.3 V to Vcc + 0.3 V
Write current		65 mA
Output current, Io:	RDX, RDY	-10 mA
	WUS	12 mA
WUS pin voltage		-0.3 to 8 V
Continuous total dissipation		See Dissipation Rating Table
Operating free-air temperature range		0°C to 70°C
Storage temperature range		-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260°C

Note 1: All voltage values are with respect to the GND terminal

DISSIPATION RATING TABLE

POWER	$T_A \leq 25°C$ POWER RATING	DEBRATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PW(16TSSOP)	616 mW	4.90 mW/°C	384 mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply voltage	Vcc		4.5	5	5.5	V
High level input voltage	V_{IH}		2	3.5	Vcc	V
Low level input voltage	V_{IL}		0	0.4	0.8	V
WDI high level input voltage (TTL)			2	3.5	Vcc	V
WDI low level input voltage (TTL)			0	0.4	0.8	V
Load resistance seen at RDX,RDY of preamp, differential			500			Ω
Thin-film write head inductance				1		µH
Thin-film write head resistance				30		Ω
Write current			5		15	mA
Operating free-air temperature	T_A		0		70	°C
Operating virtual junction temperature	T_J		25		110	°C

ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS
(Unless otherwise noted) All TTL inputs: $\overline{CS}$, R/$\overline{W}$, HS0-HS2, WDI; All TTL outputs: WUS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
TTL “L” lev. output voltage	Vol	Io = 2 mA			0.5	V
TTL “H” lev. output current	Ioh	V = 5 V			20	µA
TTL “L” lev. input voltage	Vil		-0.3		0.8	V
TTL “H” lev. input voltage	Vih		2		Vcc + 0.3	V
TTL “L” lev. input current (Pull up resistor: XCS,R/XW)	Iil1	Vil = 0.8 V	-750	-420		µA
TTL “H” lev. input current (Pull up resistor: XCS,R/XW)	Iih1	Vih = 2 V	-560	-300		µA
TTL “L” lev. input current (Pull down resistor: HS0-3)	Iil2	Vil = 0.8 V		25	40	µA
TTL “H” lev. input current (Pull down resistor: HS0-3)	Iih2	Vih = 2 V		60	100	µA
WDI input high current	I_{IH}	Vin = 2 V			100	µA
WDI input low current	I_{IL}	Vin = 0.8 V	-3			mA
WDI input high voltage	V_{IH}	TTL	2			V
WDI input low voltage	V_{IL}	TTL			0.8	V

ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS
(Unless otherwise noted) All TTL inputs: $\overline{CS}$, R/$\overline{W}$, HS0-HS2, WDI; All TTL outputs: WUS

Supply current	I_{CC}	Read mode		24	30	mA
		Write mode		15 + 1.1 Iw	21 + 1.1 Iw	mA
		Idle mode		0.1	0.2	mA
Power dissipation		Read mode		115.5	180	mA
		Write mode		75 + 5.5 Iw	115.5 + 7.7 Iw	mW
		Idle mode		0.5	1.1	mW

ELECTRICAL SPECIFICATIONS (continued)

WRITE ELECTRICAL CHARACTERISTICS

I_W = 15 mA, L_h = 1 mH, R_h = 30 Ω, fw = 5 MHz, C_L(RDX,RDY) < 20 pF, R_L(RDX,RDY) = 1 kΩ, WDI tr/tf = 1 ns (Unless otherwise noted)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Voltage at WC	V_{WC}			2.5		V
Iwc to head current gain	A_I			20		mA/mA
Write current constant	Kw		48	50	52	V
Write output current	I_W		5		15	mA
Write current variation	ΔI_W	I_W = 5 mA to 15 mA	-4		+4	%
Differential head voltage swing		Iw = 15 mA	3.4	5		Vp-p
		Open head	4.2	5.6		Vp-p
Unselected head voltage					0.1	VDC
Unselected head current	I_X-I_Y	DC			0.2	mA
Differential output capacitance	C_OD				25	pF
Differential output resistance	R_OD	Without damping	4			kΩ
		With damping	280	350	420	Ω
Output Impedance RDX, RDY		Write mode		Hi-Z		
WDI pulse width		High	10			ns
		Low	5			ns
Unselected head impedance				50		Ω
Head current		Vcc fault			±200	µA

READ ELECTRICAL CHARACTERISTICS

Output offset voltage	Voo				±300	mV
Differential voltage amplification	A_{VD}	Vi(p-p) = 1 mV at 1 MHz, $R_{L(RDX,RDY)}$ = 1 kΩ	260	300	340	V/V
Dynamic range		AC input voltage where gain falls to 90% of its small signal gain values, f = 5 MHz	2	5		mVp-p
Input bias current	I_{IB}				180	µA
Output current	I_O	AC coupled load, RDX,RDY	1	2		mA
Input noise voltage	Vn	BW = 15 MHz, L_h = 0, R_h = 0		0.50	0.75	nV/√Hz
Input noise current	In			3.5		pA/√Hz
Bandwidth	BW	Vi(p-p) = 1 mV at 1 MHz, |Zs|< 5 Ω (-1 dB)	35			MHz
		(-3 dB)	65			MHz
Common mode rejection ratio	CMRR	f = 5 MHz	54	75		dB

READ ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Channel separation	SP	f = 5 MHz	54	72		dB
Power supply rejection ratio	PSRR	f = 5 MHz	50	60		dB
Differential input capacitance	Cid	f = 5 MHz		8.5	12	pF
Differential input resistance	Rid	f = 5 MHz	500			Ω
RDX,RDY common mode output voltage	V_{OCM}	Read mode		Vcc - 2.6		V
Output resistance (single ended)	R_O	f = 5 MHz		20	50	Ω

SWITCHING CHARACTERISTICS OVER FULL RANGES OF OPERATING CONDITIONS
I_W = 15 mA, L_h = 1 µH, R_h = 30 Ω, f_{DATA} = 5 MHz, C_L< 20 pF, WDI tr/tf = 1 ns (Unless otherwise noted)

R/$\overline{W}$ to read	t_{WR}	To 90% of 100 mV		0.4	0.6	µs
R/$\overline{W}$ to write	t_{RW}	To 90% of I_W		0.1	0.3	µs
$\overline{CS}$ to unselect write	t_{CSW}	To 10% of I_W		0.6	1	µs
$\overline{CS}$ to select read	t_{CSR}	To 90% of 100 mV		0.6	1	µs
HS0-3 to any head	t_{HS}	To 90% of 100 mV		0.2	0.6	µs
WUS Safe to unsafe (delay)	t_{d1}	WDI freq too low	0.6	2	3.6	µs
WUS Unsafe to safe (delay)	t_{d2}	Fault cleared		0.2	0.6	
WUS Unsafe to safe (delay) * (WDI freq too low)	t_{d2}	Fault cleared		1.1	2.1	µs
WDI to (I_X-I_Y)	t_{WR}	L_h = 0 µH, R_h = 0 Ω		8	11	ns
Head current pulse asymmetry	t_{SYM}	L_h = 0 µH, R_h = 0 Ω			1	ns
Head current rise/fall time	t_r,t_f	L_h = 1 µH, R_h = 30 Ω		7.5	10	ns

*Device will clear the WDI too low fault condition by detecting minimum frequency (at least one complete period cycle.)

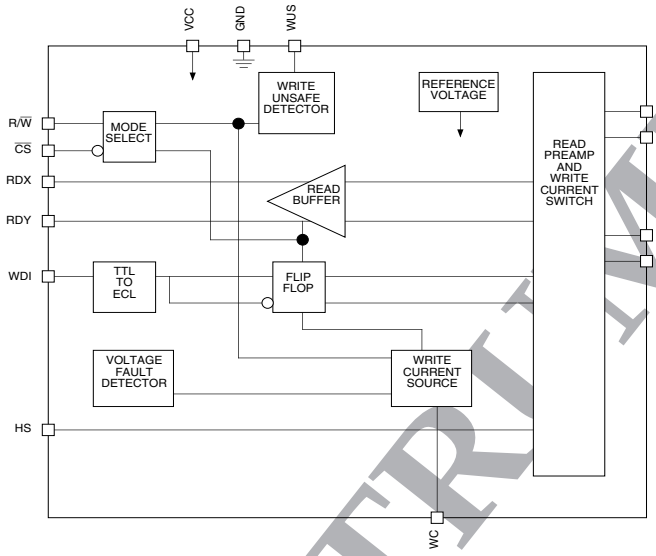
WUS SWITCHING CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Low Vcc threshold (hysteresis)	Fault detected	3.3	3.5	3.7	V
	Fault removed	3.5	3.7	3.9	V
WDI freq. for safe condition		1000			kHz
WDI freq. too low detection time	Safe to unsafe	0.6	2	3.6	µs
	Unsafe to safe		1.1	2.1	µs

TLS21H62
5 V Thin-Film 2-Channel
Low-Noise Read/Write Preamplifiers

PACKAGE PIN DESIGNATIONS

(Top View)



TLS21H62
16-Pin TSSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

Preproduction: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

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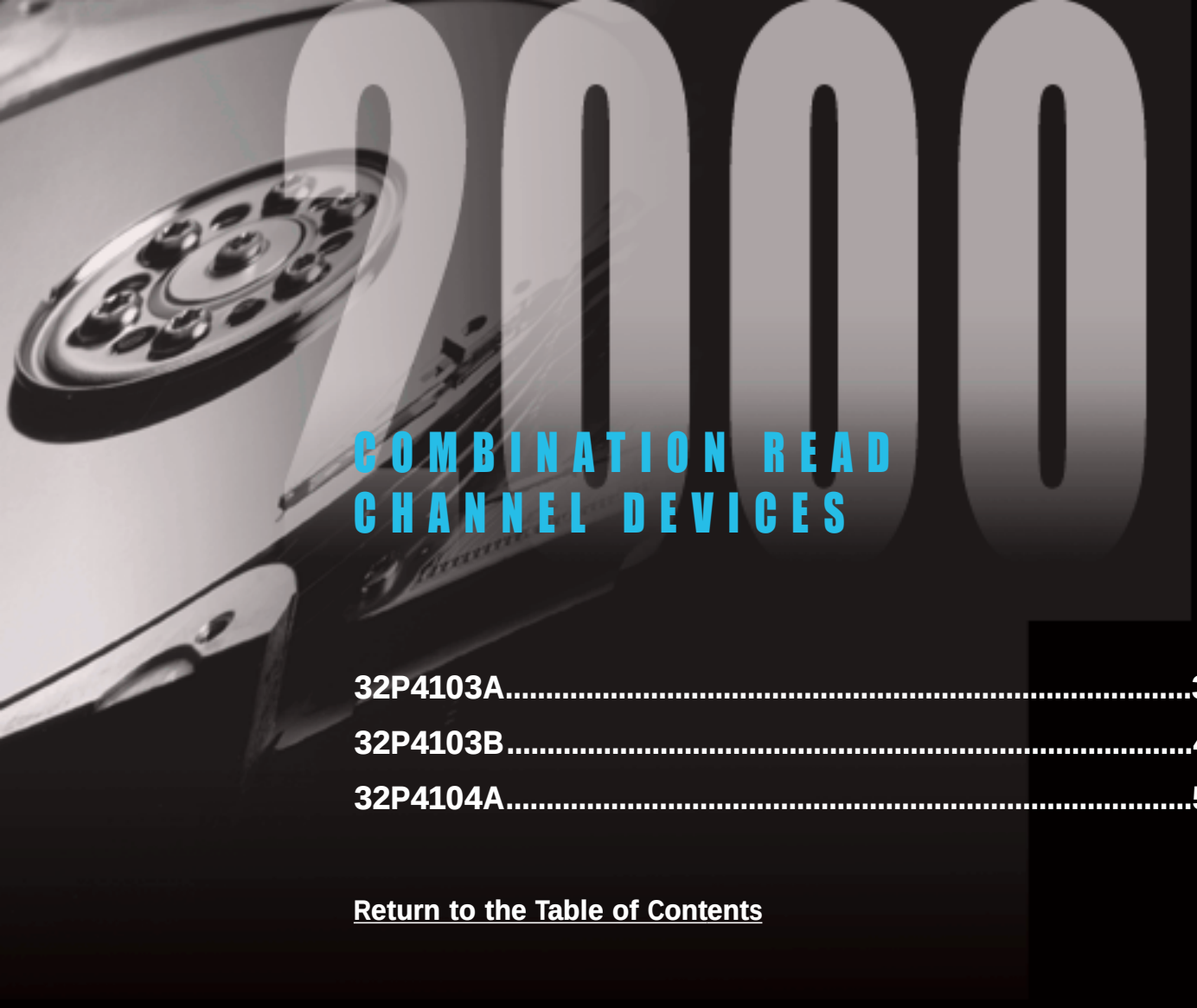

2000

COMBINATION READ CHANNEL DEVICES

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Texas Instruments

SSI 32P4103A

PRML Read Channel with EPR4, 16/17 (0,6/8) ENDEC, 4-Burst Servo

April 1999

DESCRIPTION

The SSI 32P4103A is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Extended Partial Response Class 4 (EPR4) read channel for zoned recording hard disk drive systems with data rates from 80 to 240 Mbps.

Functional blocks include AGC, programmable filter, adaptive transversal filter, 1+D filter, full EPR4 Viterbi detector, 16/17 (0,6/8) GCR ENDEC, data synchronizer, time base generator, thermal asperity detection and compensation, and FWR peak capture servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones.

The part requires a single +5 V power supply.

The SSI 32P4103A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 80 to 240 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for EPR4 equalization**
- **Five tap transversal filter with adaptive or programmable tap weight**
- **Thermal asperity management for dual stripe MR heads**
- **Silicon Systems Proprietary 16/17[0,6/8] GCR ENDEC**
- **Data Scrambler/Descrambler**
- **Programmable two level write precompensation**
- **Register programmable dynamic power management (<10 mW power down mode)**
- **Digital Channel Quality Monitor**
- **Byte wide bi-directional NRZ data interface**
- **Serial interface port for access to internal program storage registers including serial port buffer for interface to preamp**
- **Single 5 V ± 10% power supply**
- **Small footprint 100-pin and deep downset TQFP package**

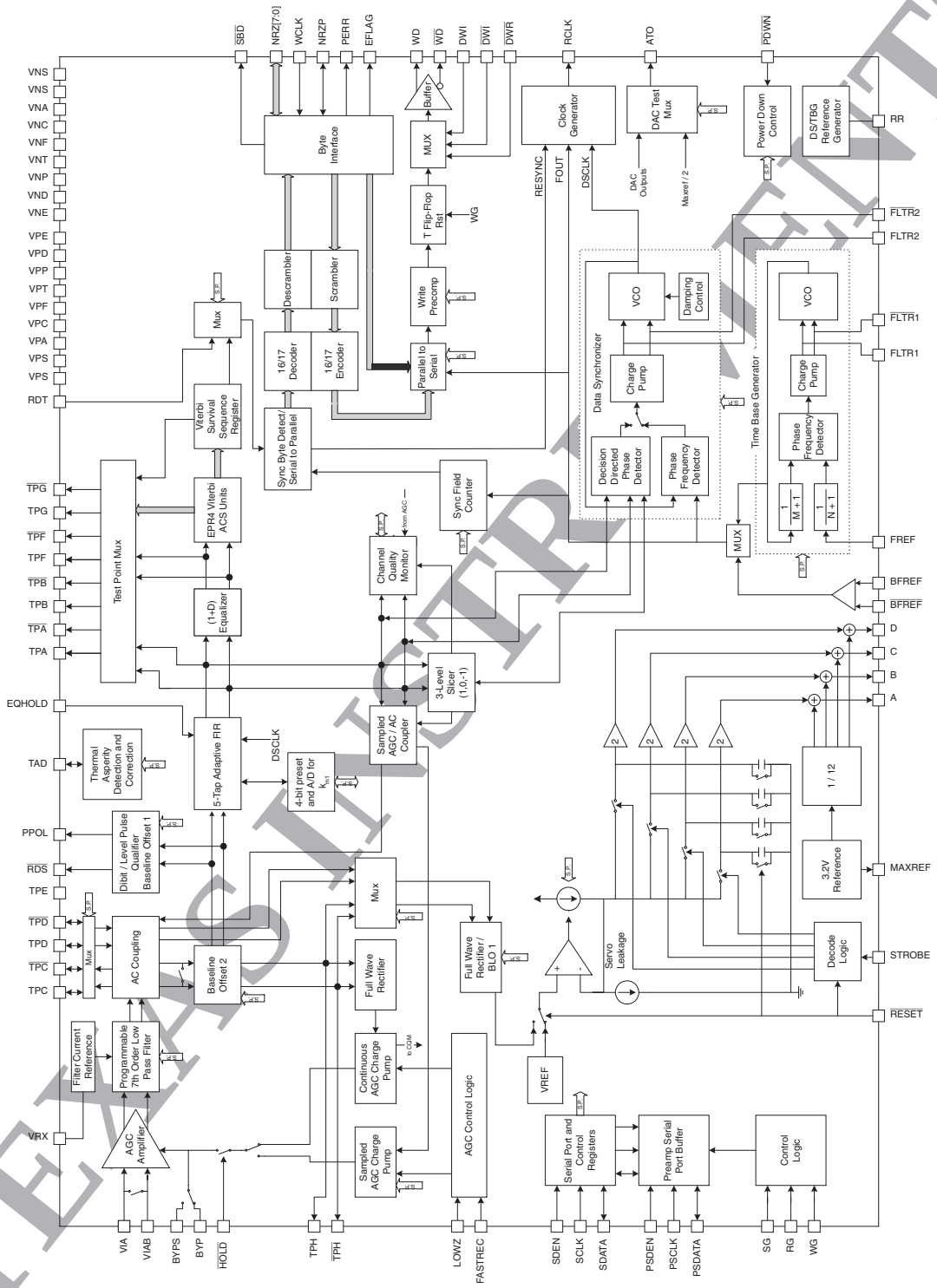
AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents for data reads**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Low Z input switch with gain squelch**
- **AGC hold, fast recovery, and AGC input impedance control signals**
- **Wide bandwidth, precision full-wave rectifier**
- **2-bit DAC to control AGC voltage in servo mode between 1.1 and 1.4 V**

FILTER/EQUALIZER

- **Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:**
  - **Channel filter and pulse slimming equalization for coarse equalization to PR4**
  - **Programmable cutoff frequency from 10 to 64 MHz**
  - **Programmable boost /equalization of 0 to 15 dB**
  - **Programmable “zeros” equalization to fix time asymmetry**

BLOCK DIAGRAM



FILTER/EQUALIZER (continued)

- ±0.7 ns group delay variation from 0.3 Fc to Fc, with Fc = 64 MHz
- Low Z switch for fast offset recovery at the filter output, on-chip direct-coupling at input and output to eliminate external AC-coupling capacitors.
- Five tap transversal filter for fine equalization to EPR4 with self adapting or programmable symmetric taps
- Equalization hold input
- Asymmetry factor output

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to EPR4
- Register programmable hysteresis, window or dibit qualification for servo reads
- Adjustable baseline shift of PPOL & RDS and Quantizer threshold to compensate for pulse asymmetry due to MR head

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 240 • 17/16 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 16/17 GCR ENDEC
- Register programmable to 240 Mbit/s operation
- Fast Acquisition, sampled data phase lock loop
- Zero Phase Restart (ZPR for fast acquisition with 5 bit tuning DAC
- 5 bit A/D tuning for ZPR DAC in TestZPR mode
- Decision directed clock recovery from data samples
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- Byte wide NRZ data interface
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync word detection
- Dual sync word detection (“or” type) with programmable pads in between 2 sync words
- Dual header mode option

SERVO

- 4-burst Peak Detect servo capture with A, B, C, D outputs
- Internal hold capacitors
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Programmable charge pump current
- Wide bandwidth, precision full-wave rectifier
- Servo Calibration output available
- Programmable Baseline Offset

THERMAL ASPERITY DETECTION AND SUPPRESSION

- Programmable Thermal Asperity with Erasure Flag
- AGC hold and PLL hold over during TA event with programmable duration
- Programmable HiY

FUNCTIONAL DESCRIPTION

The SSI 32P4103A implements a complete high performance EPR4 read channel, including an AGC, programmable filter / equalizer, adaptive transversal filter, Viterbi pulse qualifier, time base generator, data separator with 16,17 ENDEC and scrambler/ descrambler, and FWR servo, that supports data rates up to 240 Mbps.

A serial port is provided to write control data to and read from the internal program storage registers.

AGC CIRCUIT

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input to the sampled data processor while the input from the Read/Write preamplifier varies. The circuit consists of an AGC loop that includes an AGC amplifier, charge pump, programmable continuous time filter, and a precise, wide band, full wave rectifier. Depending upon whether the read is of a servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to common mode noise.

The behavior of the AGC circuit, prior to the vcolock, is controlled by 3 pins ($\overline{\text{HOLD}}$, LOWZ, FASTREC) and the control register bits (TC and TCS Registers and AGCT bit of CM1 Register). The device supports two modes of operations: externally timed or self timed. For the former, AGCT bit of CM1 should be “0” and for the latter “1”. The first three pins listed above determine the hold low-Z, and fast recovery periods.

For the external timed mode of operation the 3 pins listed above provide complete control of all of the timings.

For the self timed mode the 3 pins should be deasserted, i.e., $\overline{\text{HOLD}}$ = high, LOWZ = low, and FASTREC = low. TC and TCS Registers provide complete timings. However, it should be noted that any assertion at $\overline{\text{HOLD}}$, LOWZ, FASTREC will override the self timed mode of operation. With AGCT bit of CM1 set high, the low-Z and fast timings are generated by a circuit which counts the periods of TBG reference frequency (FREF). They are triggered by various conditions of the WG/$\overline{\text{WG}}$, SG and $\overline{\text{PDWN}}$ inputs. This mode of operation is supplied to simplify the generation

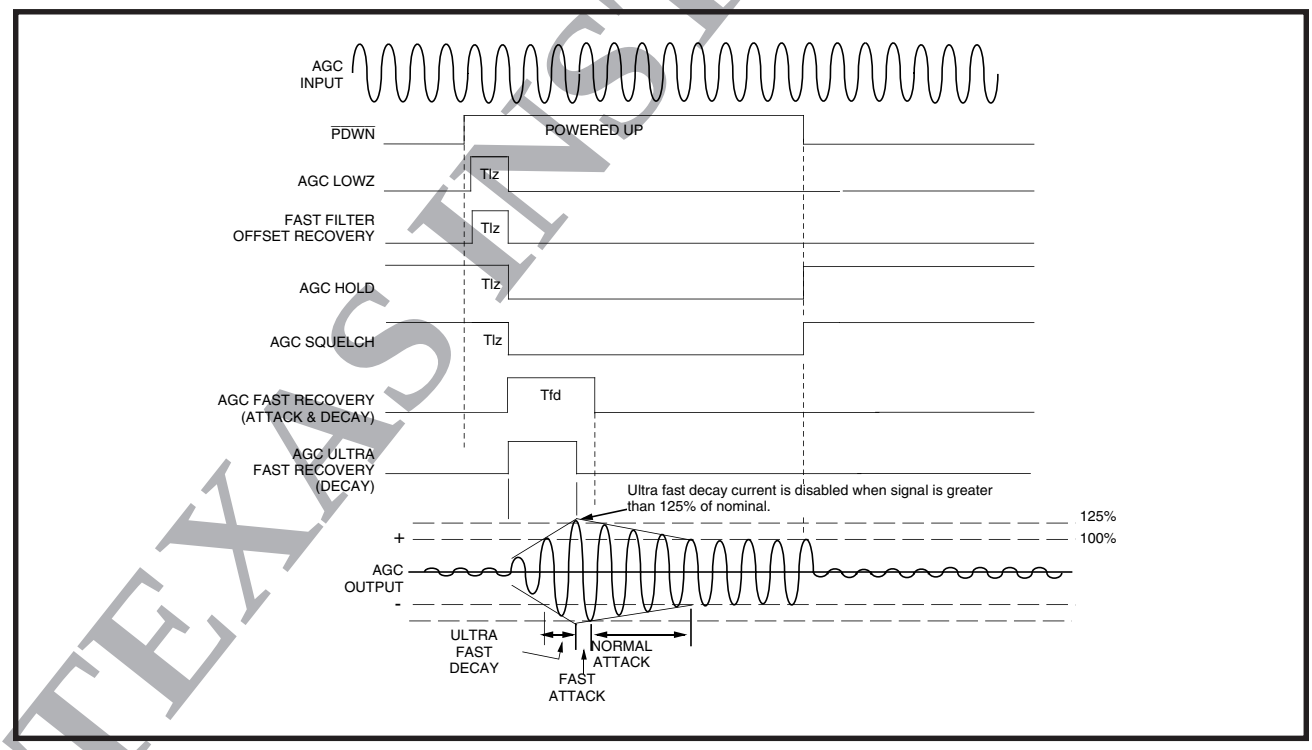


FIGURE 1: AGC Internal Timing Diagram, Power-on Mode

of the mode control signals. The timings for data mode and servo mode are independently controlled by bits in the Time Control Register (TC) and the Time Control Register for Servo (TCS). The TCS Register controls the low-Z (Tlzs) and fast recovery (Tfds) times when in servo mode and the TC Register controls these times (Tlz, Tfd) when not in servo mode. Additionally, the AGC timing following servo gate"Úalling edges can be tied to the TC or TCS controls as set by the CQM3:SGBTMR bit. The TC and TCS Registers define the internal AGC timing as a multiple number of FREF (reference clock) periods. For higher frequency reference clocks the AGC timings can be doubled using the N:FREFPS Register bit.

The low-Z mode is triggered at power-up, at each transition of SG, and at the falling edge of WG. The low-Z mode which follows the SG transitions does not force a low impedance condition at the AGC input pins. The fast recovery mode immediately follows the end of each low-Z mode. In servo mode, when the fast recovery has timed-out, the AGC automatically goes into Hold for the remaining duration of the SG input signal. This allows the servo burst amplitudes to be captured without any interference from the AGC loop. The $\overline{\text{HOLD}}$ input pin can still be asserted at any time to initiate the hold mode.

Ultra fast recovery mode begins whenever fast recovery mode starts, and ends when the signal at DP/DN reaches 125% of the programmed value. This is initiated by setting the OFDC bits in the TC Register (TC:UFDC).

After the sync field count (SFC) as set by SLC:SFC the AGC enters the sampled-AGC mode in which the AGC charge pump is controlled by the error between the measured "one" values and the ideal value. This mode is automatically entered into after achieving PLL lock in read mode.

LOW_Z, FAST RECOVERY, HOLD AND NORMAL PERIODS

During the Hold period, the AGC gain is held constant subject only to leakage currents at the BYP pins. The value of the capacitors placed at these pins should be selected to give adequate droop performance when in Hold mode as well as to insure the stability of the AGC loop when not in Hold mode. This mode should be asserted over the servo bursts.

During the Low-Z period, the AGC amplifier input resistance is reduced to allow quick recovery of the AGC amplifier input ac-coupling capacitors. (Also, the time constant of the internal AC coupling network at the filter outputs is reduced (fast filter offset recovery) to 300 ns from 5 µs or 1.5 µs depending upon the state of LZCTR bit in TCS. The duration of this period can also be extended to the end of Fast Recovery by appropriately setting MISC2:FDFLOWZ. The low-Z period also forces AGC gain to reduce to almost 0V/V (AGC squelch). This mode should be activated during and for a short time after a write operation. It should also be activated for a short time after each transition of the SG input or after initial power up.

In the Fast Recovery period, the attack and decay currents are increased to allow faster recovery of the proper AGC level. During this period, in either external or self timed mode, the Ultra Fast Recovery may be effected by appropriately setting TC:UFDC. This will allow an extremely rapid increase of AGC amplifier gain. This mode shuts itself off when the signal at DP/DN reaches the 125% point.

During the Normal period (i.e., the period other than low-Z, fast recovery or hold prior to vcolock), the normal attack and decay currents are used to maintain a constant signal level at the qualifier inputs.

LOW_Z, FAST RECOVERY, HOLD AND NORMAL PERIODS (continued)

AGC Operation in Servo Read Mode

During servo reads, the AGC loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (CBYPS) which is referenced to VPA (positive supply). The dual rate charge pump drives CBYPS with currents that force the differential peak to peak voltage at the filter output (DP/DN) to a programmed peak to peak voltage. Attack currents lower the voltage at BYPS, which reduces the amplifier gain. Decay currents raise the voltage at BYPS, which increases the amplifier gain. The sensitivity of the amplifier gain to changes in the BYPS voltage is about 38 dB/V. When the voltage at BYPS is equal to VRC (bandgap voltage output pin), the gain from AGC input to DP/DN will be about 24.9 dB. The charge pump is continuously driven by the instantaneous voltage at DP/DN. When the signal at DP/DN is greater than 100% of the programmed AGC level, the normal attack current (Ia) of 416 µA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, the fast attack current (Iaf) of 3.54 µA is used to reduce the gain very quickly. This dual rate approach allows the AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A normal decay current (Id) of 26 µA acts to increase the amplifier gain when the signal at DP/DN is less than 100% of the programmed AGC level. The large ratio (416 µA:26 µA) of the normal attack and normal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. Unfortunately, this implies that the AGC loop will not be able to quickly increase its gain if required to do so. A fast recovery mode is provided to allow the AGC gain to be rapidly increased in order to reduce the recovery time between mode switches. In the fast recovery mode, the decay current is increased by a factor of 8 to 208 µA (Idfr) and the attack current is increased by a factor of 4.18 to 1.42 µA (Iafr). This has the effect of speeding up the AGC loop by a factor somewhere between 4 and 8 times.

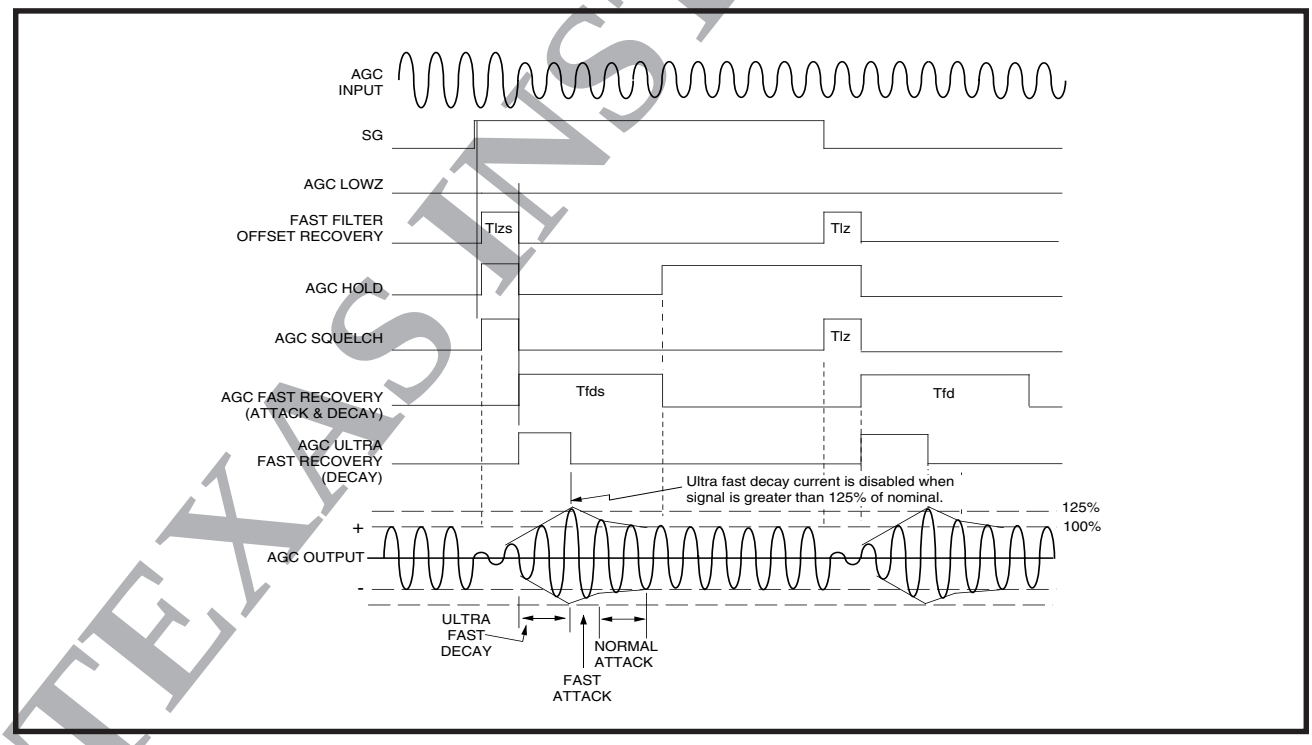


FIGURE 2: AGC Internal Timing Diagram - Servo Mode

When the CM1:AGCT (self-time) bit is set low, the AGC mode control is determined by the LOWZ and FASTREC input pins. This mode of operation is supplied for maximum application specific flexibility. It is recommended that the FASTREC be asserted when the AGC fields from a sector are being read. Typically, this will be just after each transition of SG (Servo Gate), after power up, and after WG is de-asserted. For example, if CBYPS is 500 pF and FASTREC is asserted for 0.5 µs in Servo mode, the voltage at BYPS can increase at most by 0.5 µs • 208 µA/500 pF = 208 mV, which will allow the gain to increase by 6 dB in that time. If FASTREC is asserted for 0.5 µs in non-Servo mode and CBYPD is 1000 pF, then the voltage at BYPS can increase at most by 0.5 µs • 208 µA/1000 pF = 104 mV, which will allow the gain to increase by 3 dB in that time. It is recommended that LOWZ be asserted for 0.5 µs just prior to any assertion of FASTREC in order to quickly null out any internal DC offsets. (However, it is possible to assert both LOWZ and FASTREC simultaneously in order to reduce sector overhead as much as possible. This should be evaluated under actual operating conditions.) The rising edge of FASTREC may also be used to initiate ultra fast recovery. See the AGC description section above.

In servo mode, the programmed AGC level may be adjusted between 1.10 and 1.40 Vppd by programming the two AGCDAC bits in the LDS Register. This allows the servo demodulator dynamic range to be adjusted a small amount.

AGC Operation in Data Read Mode

For data reads, the loop described above is used until the data synchronizer is locked to the incoming VCO preamble except that the CBYP hold capacitor is used instead of CBYPS. After the data PLL is locked, the AGC loop is switched to include the AGC amplifier with a sampled charge pump, the programmable continuous time filter, and the sampling 5-tap equalizer to more accurately control the signal amplitude into the Viterbi

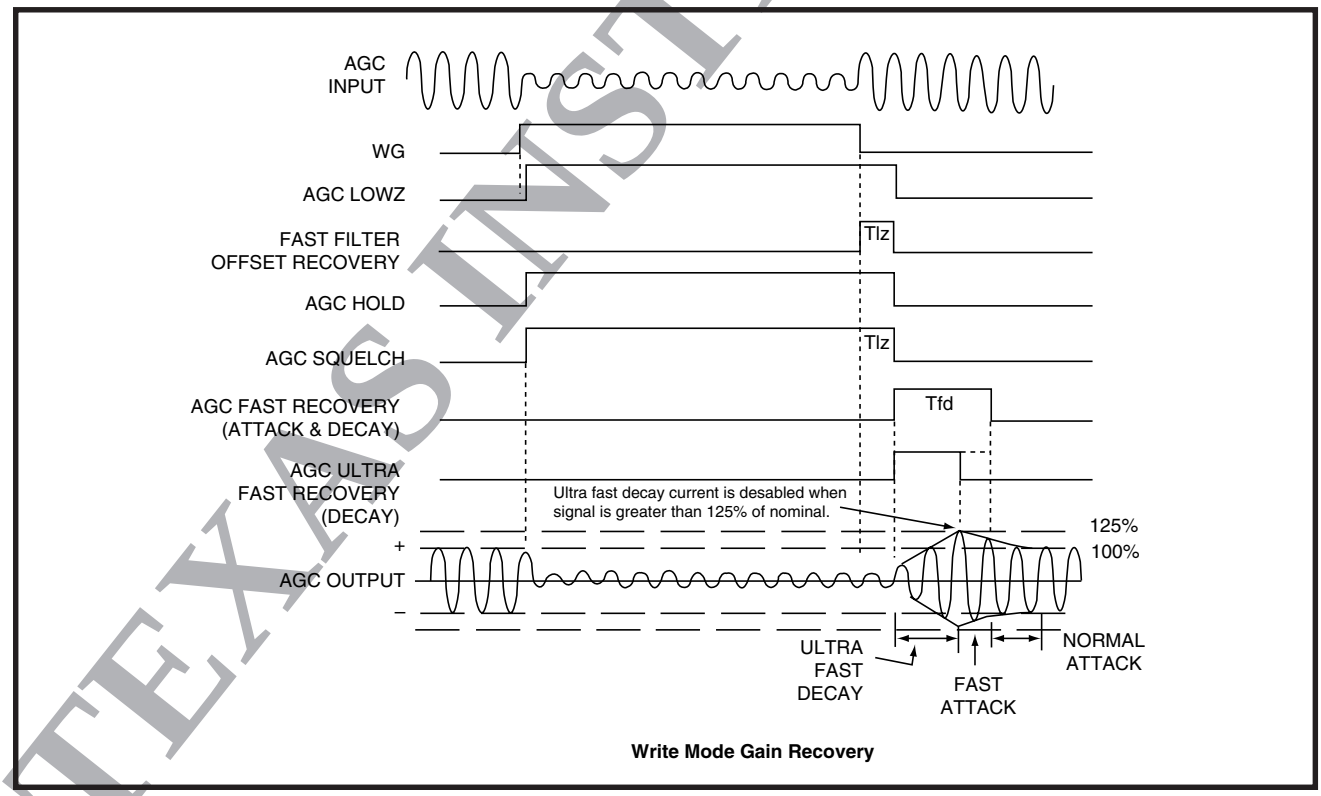


FIGURE 3: AGC Internal Timing Diagram- Write Mode

AGC Operation in Data Read Mode (continued)

qualifier. In this sampled AGC mode, a symmetrical attack and decay charge pump is used. The "1" sample amplitudes are sampled, held, and compared to a threshold to generate the error current. The maximum charge pump current value can be programmed from the SLC Register to 0, 20, 40, or 60 μA. This current will be proportional to the Data Rate Register value.

SERVO DEMODULATOR CIRCUIT

Servo functionality is provided by two separate circuits: the servo demodulator circuit, and the dual level pulse qualifier circuit. To support embedded servo applications, the SSI 32P4103A provides separate programmable registers for servo mode filter cutoff frequency, boost, and qualification threshold. The values programmed in these registers are selected upon entry into servo mode (SG=1). Either the normal or differentiated filter signal can be routed to the servo demodulator by setting CM2:SERI.

Also the RDS pulse polarity and its nominal pulse width are each one bit programmable via SERI and PWCTR bits both in CM2 Register, respectively.

The servo demodulator circuit captures four separate servo bursts and provides an amplified and offset version of the voltages captured for each at the A, B, C, and D output pins respectively. The circuit uses a "Soft Landing" charge pump with programmable initial charge current to charge each of the internal 10 pF burst hold capacitors. The "Soft Landing" charge pump architecture prevents the hold capacitor from being charged to a voltage greater than the actual instantaneous peak voltage at the full wave rectifier output. Internal burst hold capacitors are provided to reduce external component count. Burst capture control is provided by the STROBE and $\overline{\text{RESET}}$ input pins. The initial charge pump current can be set to one of the four values using the CM2:SBCC0,1 bits. In addition to the A, B, C, and D outputs pins, the circuit provides a maximum reference voltage at the MAXREF output pin. This reference voltage represents the maximum voltage that can be achieved at the A, B, C, and D output pins with a 1.4 Vpp signal at the filter output and is typically used as the reference voltage for an external A/D converter.

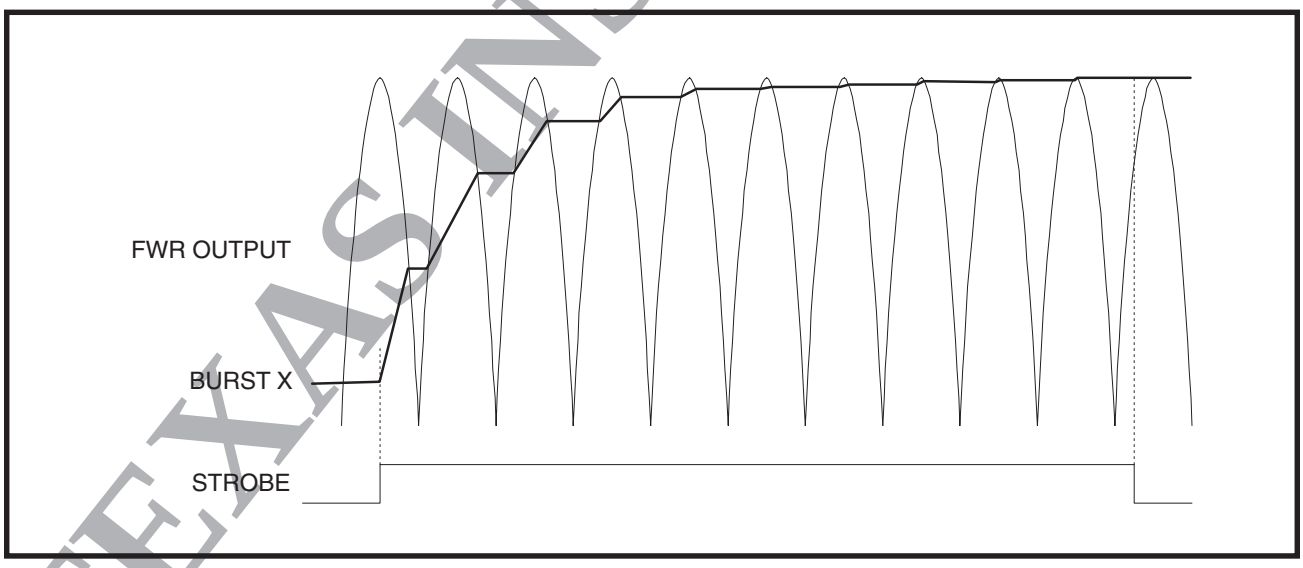


FIGURE 4: Servo Burst Acquisition

Burst Capture

Burst capture is controlled by the signal applied to the STROBE input pin and an internal counter. The first pulse on the STROBE input pin causes the A burst hold capacitor to be charged by the charge pump. The capacitor charges for as long as the STROBE input is high or until the capacitor voltage reaches the peak voltage at the full wave rectifier output. On the falling edge of the STROBE signal, the internal counter is incremented. The next 3 STROBE pulses will charge the B, C, and D, hold capacitors respectively. After the falling edge of the fourth strobe, the counter is reset to zero and the burst capture sequence can be repeated. The counter is also reset when the $\overline{\text{RESET}}$ input transitions low.

The voltage level on each hold capacitor is amplified by a factor of 3.33 and summed with a 0.27 V DC reference to create the A, B, C, and D output signals. A 1.4 V pp differential voltage at the DP/DN pins will result in 1.4 • 0.6 • 3.33 = 2.80 V peak burst amplitude (i.e. servo gain = 2.0). The MAXREF output pin is a nominal 3.2 V and is internally divided by 12 to create the DC baseline of 0.27 V. To minimize any channel to channel mismatch it is recommended that the reset voltages be first measured and stored to be later subtracted from the burst voltages. Alternately by using a special servo calibration mode by setting FCS(bit7) to 1 the reset voltage of each channel can be added to a reference voltage sum of which is roughly equal to Maxref/2 and brought to the corresponding burst pin. This could then be used to calibrate the servo. In this mode no strobing is necessary. Nominal voltage is given by 2.3 V • 2/11 • 10/3 + Vol (=0.27 V) = 1.664 V and this approximates the on-track servo voltage of 0.7 V • FWR gain (=2.0) + Vol (=0.27) = 1.67 V.

All four of the internal hold capacitors are discharged when the $\overline{\text{RESET}}$ input is driven low. The $\overline{\text{RESET}}$ input overrides the STROBE signal. STROBE and $\overline{\text{RESET}}$ are not gated with SG.

The maximum charge pump current can be selected as 40,80,120 or 160 µA by setting the servo burst charge current (SBCC0:1) bits in the CM2 Register. The "Soft Landing" technique reduces the charge pump current as the error between the voltage on the hold capacitor and the full wave rectifier output becomes smaller. This reduces the possibility of overcharging the capacitor during the comparator's propagation delay period.

A small leakage current is applied to the capacitor being charged during each strobe period to make the captured voltage less sensitive to noise and strobe timing. The magnitude of this current is 1/450 of the charge current.

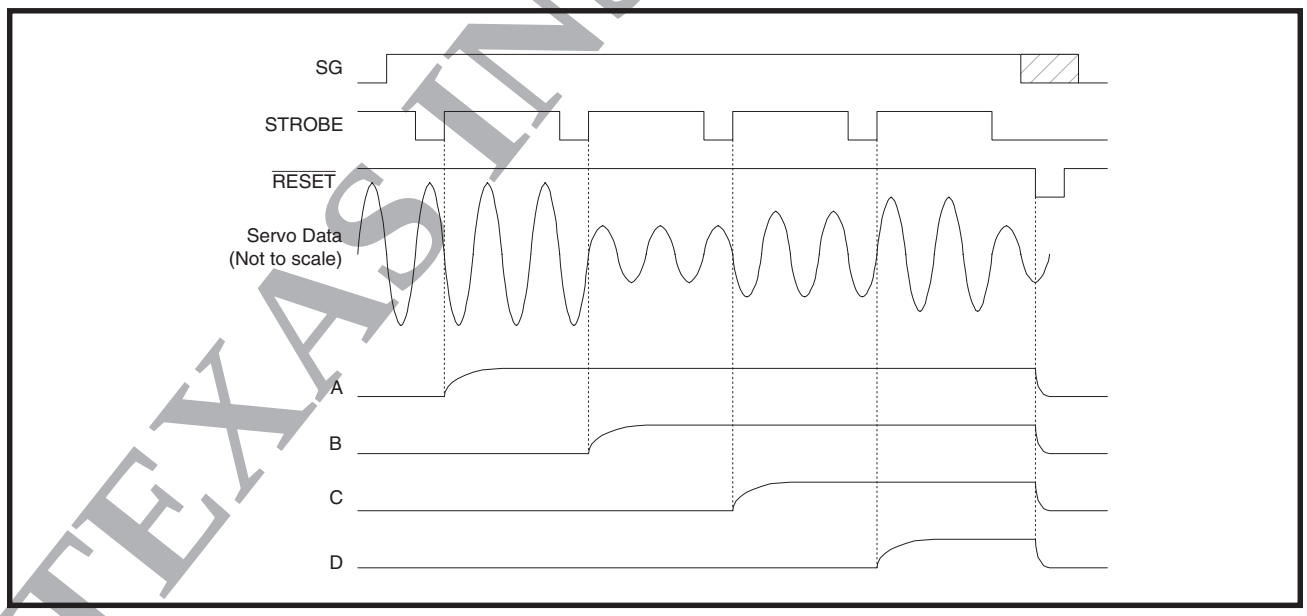


FIGURE 5: Servo burst capture timing

FUNCTIONAL DESCRIPTION (continued)

PULSE QUALIFICATION CIRCUIT

This device utilizes two different types of pulse qualification, one for servo reads and the other for data reads.

QUALIFIER

Servo Read Mode

During servo reads (SG high) either a hysteresis or window or dibit type of pulse qualifier is used. The level qualification thresholds are set by a 6-bit DAC which is controlled by the LDS Register. The DAC is referenced to a fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable CM4:ALE does not affect this DAC's reference. The $\overline{RDS}$ and the PPOL outputs of the level qualifier indicate a qualified servo pulse and the polarity of the pulse, respectively. The $\overline{RDS}$ and PPOL outputs are only active when the SG input is high.

Dibit Qualifier Mode

(CM2:DIBDEN = 1; CM2:PDM = 0; STM2:DIBITPOL)

In the dibit qualifier mode, the normal Window Qualifier detected pulses, as described above, are further time interval qualified prior to clocking out a pulse at RDS. See the corresponding timing diagram of Figure 7. If a threshold qualified pulse is detected after a prolonged period of absence of pulses (this interval equal to the output pulse width of the internal Retriggerable One Shot, or Tr) the Retriggerable One Shot is triggered, but not the RDS output pulse. Then, if and only if a subsequent threshold qualified pulse of opposite polarity is detected within the Tr period, this second pulse is allowed to clock a pulse out at the RDS output, whose negative polarity asserted output pulse width is set by the Nonretriggerable One Shot. If another threshold qualified pulse occurs of the same polarity of a previous pulse which most recently triggered the Retriggerable One Shot, within the Tr interval, this one shot will retrigger so that its output pulse will be extended beyond this time by an additional Tr, and permit another opposite polarity pulse to clock a pulse out at RDS if it occurs within this new Tr period. Thus the dibit qualifier mode detects dibit pairs if the interval between the positive and negative polarity pulses of the dibit pulse pair is Tr or less. The first pulse of the dibit arms the detector, and the second clocks out the pulse at RDS if it was opposite in polarity from the first and within Tr of the first, and can be set the polarity of the first transition before Dibit detect signal by DIBITPOL bit.

If a continuous pulse stream (such as servo preamble) is encountered such that the interval between successive same polarity pulses is less than Tr, the Retriggerable One Shot will continuously retrigger so that the threshold qualified pulses of opposite polarity from those that are retriggering this one shot will repeatedly clock out pulses at RDS. The polarity that repeatedly retriggers the time discriminating Retriggerable One shot is that which occurred first after a period (> Tr) of absence of pulses prior to the continuous burst.

The dibit time interval discrimination pulse width Tr can be varied with the DBT[2:0] Register bits in DBT. Implied frequency is the full cycle frequency whose period is 2x(Tr). The scaling is approximately a linear progression in terms of Tr.

Data Read Mode

In data read mode (RG high), the same dual level qualifier as was used for servo reads, is used for ensuring pulse polarity changes during VCO sync field counting. The qualification thresholds are set by a 6-bit DAC which is controlled by or the LD Register. The DAC is referenced to a fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the CM4 Register does not affect the DAC's reference until the sync field count has been reached. The $\overline{RDS}$ and the PPOL outputs of the level qualifier are not active in data read mode. Pulse polarity transition count is performed in hysteresis mode only.

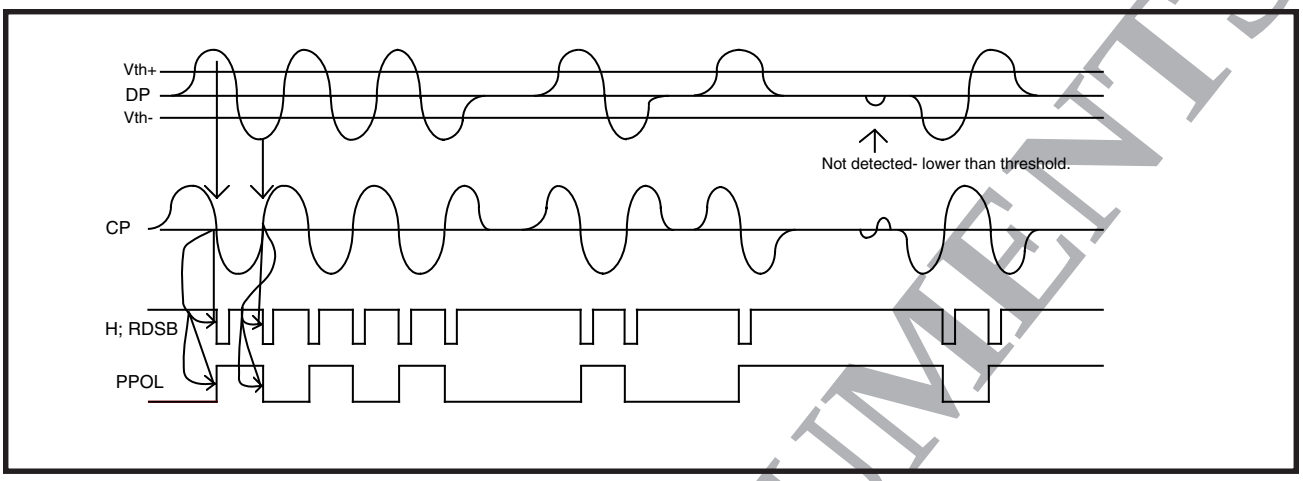


FIGURE 6: Window Qualifier

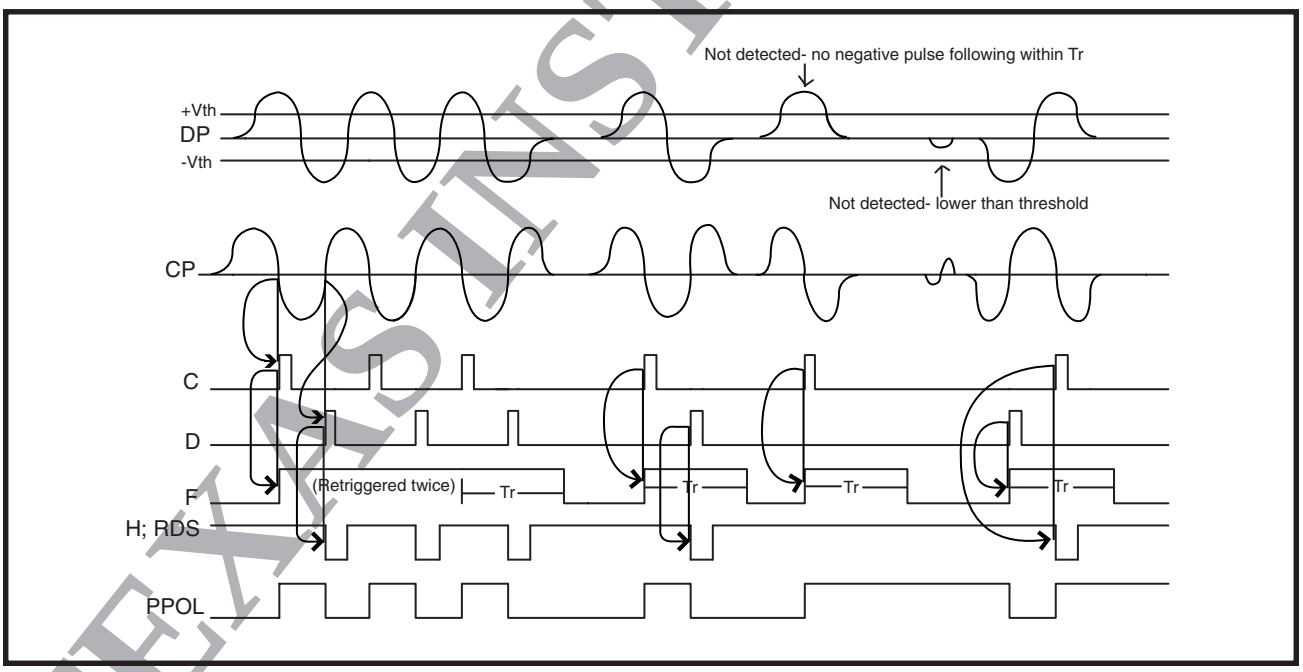


FIGURE 7: Dibit Qualifier Mode

PULSE QUALIFICATION CIRCUIT (continued)

3-Level Slicer

The determination of whether a sample is a "one" or a "zero" is performed by a dedicated, dual mode, threshold comparator (3-level slicer). The slicer's threshold levels are determined by the value, Lth, programmed in the LD Register. The fixed level threshold before the sync field count (SFC) has been reached will be 1.4 times the threshold level after SFC since this is the ratio of the peak signal to the sampled “1” signal amplitude for PR4. The dual mode nature of this comparator allows the selection of either symmetric fixed or independent self adapting (+) and (-) thresholds by programming the adaptive level enable CM4:ALE.

The adaptive reference allows the specification of the threshold value to be a percentage of an averaged peak value. When adaptive mode is selected, the fixed thresholds are used until SFC has been reached, then the adaptive levels are internally enabled. The time constant of a single pole filter that controls the rate of adaptation is programmable by the CM4:TC.

Baseline Offset

The baseline offset is included to compensate for the amplitude asymmetry of the incoming signal from the preamp. There are two modes of baseline offset available in this device - Mode 1 and Mode 2.

In Mode 1, the baseline shift is not applied to the DP/DN in the conventional AGC feedback path, so the AGC always regulates the amplitude of unshifted signal. Differential baseline offset can be applied to the DP/DN signal input of the Qualifier prior to threshold qualification. The magnitude of this baseline shift is controlled by the SBO bits in the BLO Register for the servo mode qualifier. The polarity of this shift is controlled by the BOSP bit in the BLO Register. The shift is positive when the BOSP = 1. The magnitude of the baseline offset is 4 • SBO (mV). The same baseline shift magnitude can be applied to the input of the servo demodulator section of the chip by enabling the SOC bit of the BLO Register. Otherwise, the servo demodulator path is not offset regardless of the offset setting of the Qualifier. Unlike the Qualifier, the servo demodulator can apply this shift to either filter normal output or filter differentiated output as set by the SERI bit of the CM2 Register. This is controlled by BLOS Register.

In Mode 2, the baseline shift is introduced at the output of DP/DN filter output and therefore the AGC regulates the amplitude of the shifted signal. In this mode, there are two 8 bit registers, BLOD and BLOS, for data and servo mode, respectively. The magnitude of the negative shift is given by 2.5 mV • BLOSD,S[6:0] for the maximum of 317.5 mV, the magnitude of the positive shift is given by 2.374 • BLOSD + 11.654 for the maximum of 313.1 mV and the magnitude by BOSDP and BOSSP. The shifted signal is observable at TPH, $\overline{\text{TPH}}$ pins.

EPR4 VITERBI DETECTOR

The EPR4 channel dibit response is described by:

$$EPR4(D) = (1-D)(1+D)^2$$

where D denotes unit delay in the Z domain.

The sampled data signals coming out from the FIR filter are equalized to a PR4 response, attaining three separate signal levels: +1, 0, -1. To convert the PR4 waveform to EPR4 waveform, a (1 + D) filter is used. Data exiting the (1 + D) filter will now attain five separate signal levels: +2, +1, 0, -1, -2.

Figure 10 shows the state transition diagram of an EPR4 channel. The state variables denote the state of the write current in the magnetic head and the value on the transition edges are the channel outputs. Unlike a PR4 channel, the EPR4 channel cannot be interleaved into two independent (1-D), two state channels. To decode the state transitions from the channel outputs, an eight-state Viterbi detector is required.

The SSI 32P4103A implements a full eight-state EPR4 Viterbi trellis detector. To increase data rate, signal processing is interleaved such that signal processing is done at one half of the code rate.

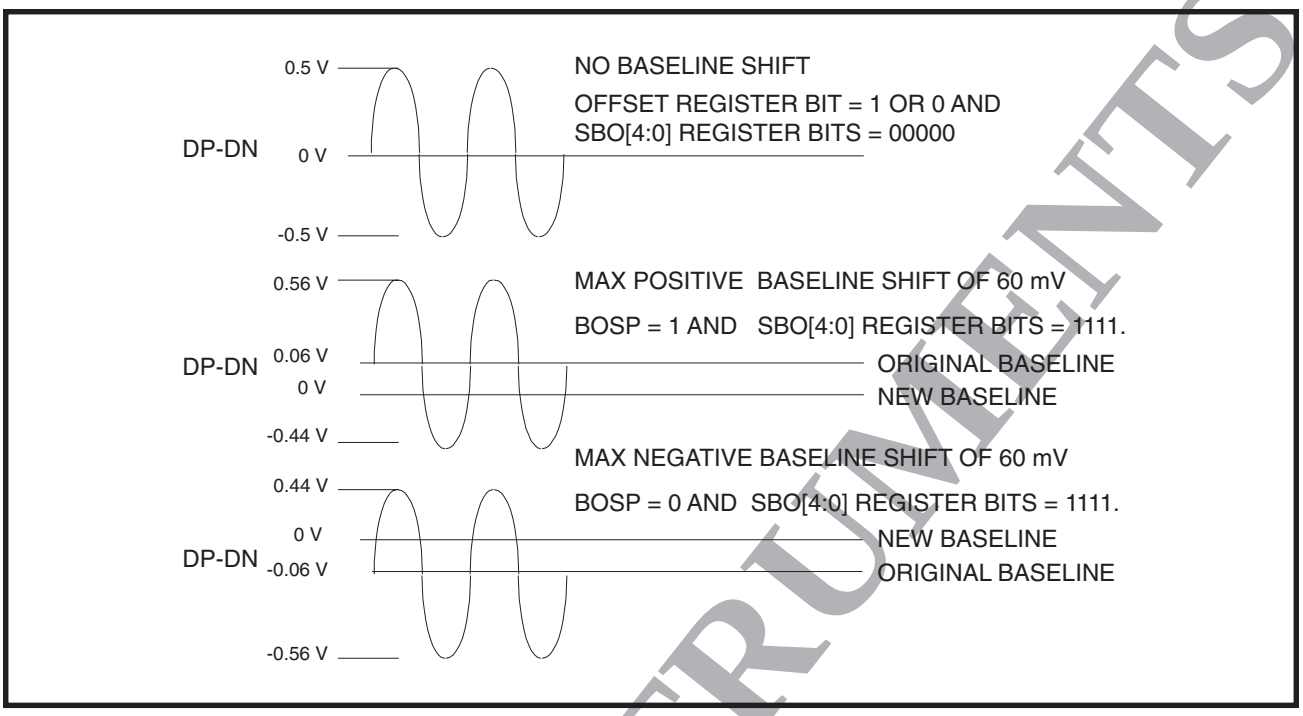


FIGURE 8: Mode 1 Baseline Offset Control

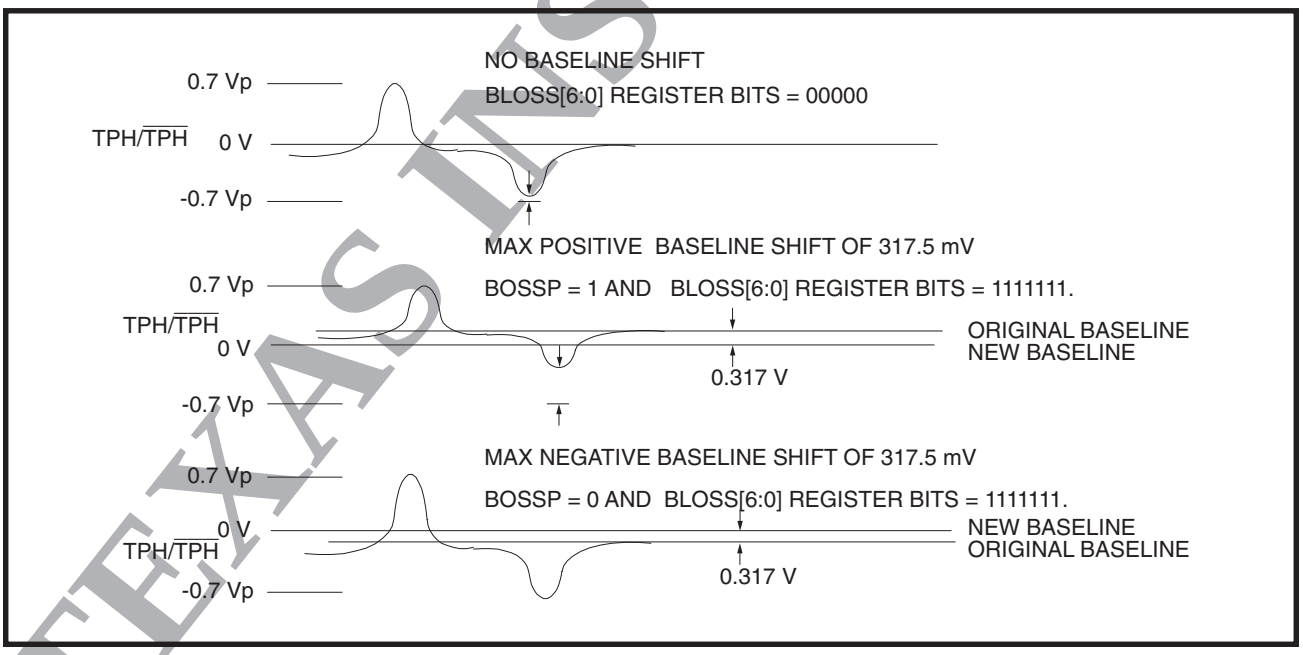


FIGURE 9: Mode 2 Baseline Offset Control

EPR4 VITERBI DETECTOR (continued)

The Viterbi detector equations implemented in SSI 32P4103A are listed below:

$m_k(S0) = \max \{M00, M01\}$

$m_k(S1) = \max \{M10, M11\}$

$m_k(S2) = \max \{M20, M21\}$

$m_k(S3) = \max \{M30, M31\}$

$m_k(S4) = \max \{M40, M41\}$

$m_k(S5) = \max \{M50, M51\}$

$m_k(S6) = \max \{M60, M61\}$

$m_k(S7) = \max \{M70, M71\}$

where

$M00 = m_{k-1}(S0) + 0.5 - A,$
$M01 = m_{k-1}(S4) - y_k - A$

$M10 = m_{k-1}(S0) + y_k - A,$
$M11 = m_{k-1}(S4) + 0.5 - A$

$M20 = m_{k-1}(S1) + y_k - A,$
$M21 = m_{k-1}(S5) + 0.5 - A$

$M30 = m_{k-1}(S1) + 2y_k - 1.5 - A,$
$M31 = m_{k-1}(S5) + y_k - A$

$M40 = m_{k-1}(S2) - y_k - A,$
$M41 = m_{k-1}(S6) - 2y_k - 1.5 - A$

$M50 = m_{k-1}(S2) + 0.5 - A,$
$M51 = m_{k-1}(S6) - y_k - A$

$M60 = m_{k-1}(S3) + 0.5 - A,$
$M61 = m_{k-1}(S7) - y_k - A$

$M70 = m_{k-1}(S3) + y_k - A,$
$M71 = m_{k-1}(S7) + 0.5 - A$

In the above equations, mk and yk are the state metric values and the EPR4 sample values at time k. In each cycle, updates to the eight state metrics are required by selecting between two contesting values. These contesting values, M's, are computed by adding branch metrics values to existing state metrics. Branch metrics measure the probability of different state transitions in the trellis diagram and is formed by linear combinations of channel sample values, y's, and certain constant values. Each state metric update requires additions, comparisons and select operations and are thus known as ACS (Add-Compare-Select). In the above equations, a common mode term A is subtracted from each metric expression. This is necessary to avoid the metric build up.

Also note that in the expressions for metrics, the first subscript refers to the metric State and the second to the data being detected.

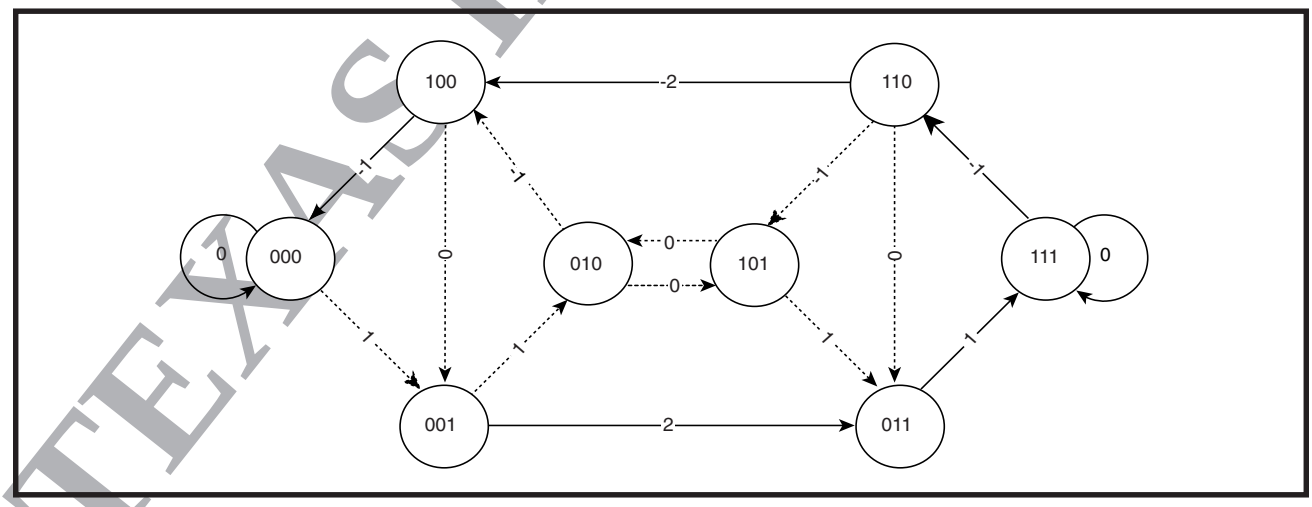


FIGURE 10: State Transition Diagram for EPR4 channel

VITERBI DETECTOR CIRCUIT

The EPR4 Viterbi detector is enabled only during read mode and only after the sync field count (SFC) has been achieved. The block diagram from the EPR4 Viterbi Detector is shown in Figure 11. This circuit has two significant blocks, one that feeds the other. The first block consists of the eight ACS (Add-Compare-Select) units and the second consists of the survival sequence registers. Each ACS unit stores and updates one of the eight state metrics, mk, every cycle as described by the equations described. To constrain the signal dynamic range, feedback normalizations are done as a common term, A, is subtracted from each metric. Each ACS unit will also determine which of the two incoming path metric values (M_{SB}) is larger. Every two clock cycles the ACS selection information is sent to its associated survival register as two-bits at a one-half rate. The signal processing through the ACS units is carried out in the analog sampled data domain to allow high speed and low power Viterbi detector implementation.

The survival register, on receiving the 2-bit selection information from its ACS unit, will mux in and shift the correct decoded data sequence from 1 of the 4 survival registers connected at its input. In SSI 32P4103A, each survival register is 12 bits long. In a noiseless channel, the outputs of all eight survival registers should give identical 16/17 encoded data. However, in a noisy environment, the outputs of these survival register could be different. To derive the optimum detected data each cycle, the data outputs from the survival register having the largest state metric are selected and are fed to the sync pattern detector and decoder.

The branch metric constant in the Viterbi equations are derived from an on-chip bandgap voltage reference. The same bandgap is also used to define the equalization targets for the FIR block. Therefore, these branch metric constants will track the Viterbi

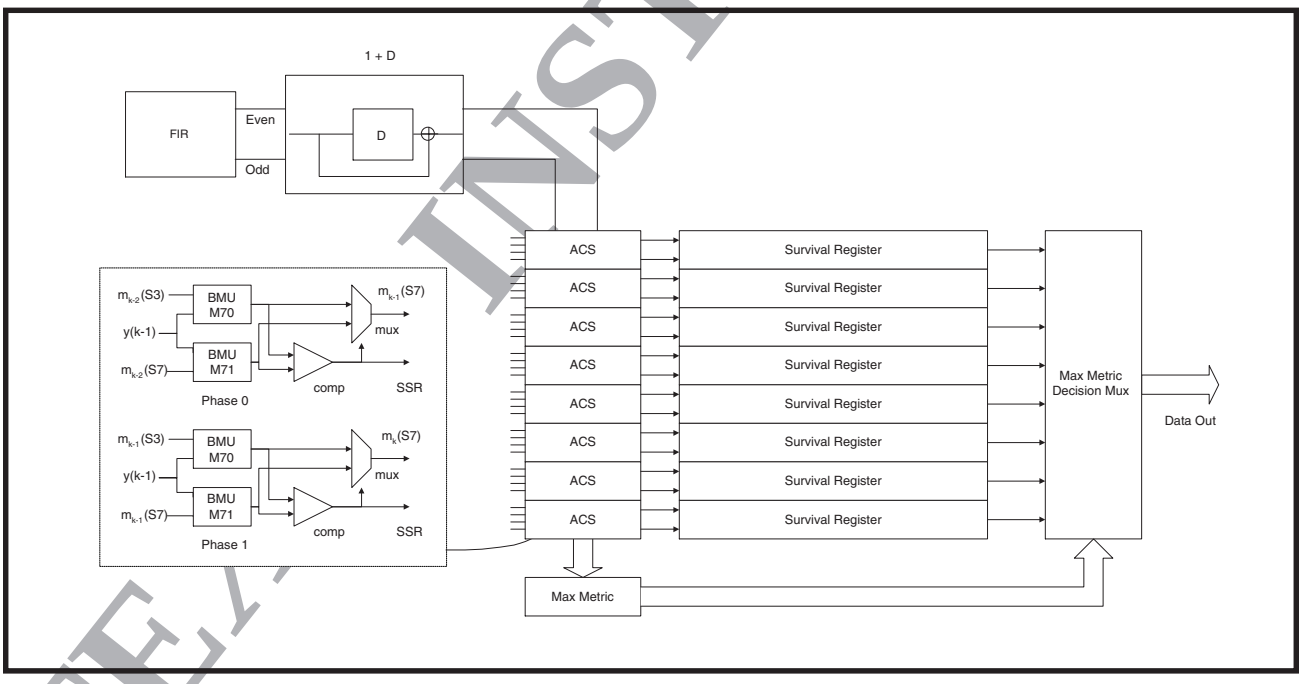


FIGURE 11: EPR4 Viterbi Block Diagram with the 1 + D Filter

VITERBI DETECTOR CIRCUIT (continued)

equalization targets with varying operating conditions. The branch metric constants are formed by multiplying integer values with Vpk and Vnk. The following table shows the relationship between the constant values in the Viterbi equations above and Vpk and Vnk.

Constant	Voltage
-1.5	-3 • Vnk
0.5	Vpk

Vpk and Vnk, are set as percentages of the '+1','-1" PR4 equalization targets by two 4-bit DACs controlled by bit D7:D4 and D3:D0 in serial port register VEPR4 Register according to the following equation:

$$Vnk = 0.5 \bullet \{1.0 \pm (D7:D4) \bullet 2.5\%\}$$

$$Vpk = 0.5 \bullet \{1.0 \pm (D3:D0) \bullet 2.5\%\}$$

where (D7:D4) and (D3:D0) are in two's complement form

DEFECT SCAN MODE

In this mode of operation a pair of raw decisions are generated by the 3-level slicer at the FIR output. The threshold for this slicing can be adjusted via Data Threshold Register. When Defect scan mode is activated, the timing recovery loop is forced to accept only ±1 decisions and thus is not affected by the Data Threshold Register setting.

This mode can be used to scan the disk media for defects as follows. The user can write 2T patterns in the area under test by putting the chip in write mode while holding the NRZ interface low. In read mode, the user should activate the defect scan mode. Note that, because the channel is in defect scan mode, there is no sync pattern detection search after assertion of SFC. A data flag can be enabled by setting DR:DSB. When enabled, the NRZ1 pin is toggled at sync field count as set by SLC:SFC.

For defect scan testing, a VCO synchronization pattern (1,1,-1,-1) may be written onto a track, then read back and checked for low amplitude pulses. The synchronization pattern is written by asserting WG and holding the NRZ input pins low for the duration of the write sequence. To read the pattern and check for low amplitude pulses, set the defect scan test mode using the LD:DSCAN bit. When RG is asserted, the data separator PLL will lock to the preamble pattern, and the NRZ pins will go to a low state. After sync field count, low amplitude pulses will be detected and a "1" will be transmitted to the NRZ7 pin. The "1" will be held for one RCLK cycle, so that it can be detected by the controller. In the presence of a continuous error condition, the NRZ7 output will produce a continuous 1. The normal byte-wide read mode NRZ setup and hold times apply to NRZ7 in the defect scan mode.

The $\overline{SBD}$ is asserted low after vcolock is generated, and is held until RG goes low. $\overline{SBD}$ to RCLK rising, TSDL spec applies to this mode.

PROGRAMMABLE FILTER CIRCUIT

General Description

The on-chip, continuous time, low pass filter has register programmable cutoff and boost settings, and provides both normal and differentiated outputs. It is a 7th order filter that provides a 0.05° phase equiripple response. The group delay is relatively constant up to twice the cutoff frequency. For pulse slimming, a two zero programmable boost equalization is provided with no degradation to the group delay performance. The differentiated output is created by a single-pole, single-zero differentiator. The filter zeros can be adjusted asymmetrically about zero to compensate for MR head slope asymmetry. The asymmetry is adjusted using the FBS:FGD bits.

The programmable bandwidth and equalization characteristics of the filter are controlled by 3 internal DACs(FC,FB and FGD) in data mode and 2 internal DACs(FCS and FBS) in servo mode. The registers for these DACs are programmed through the serial port. The current reference for the DACs is set using a single external resistor connected from pin RX (=10.2 kΩ, 1%) to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. This establishes excellent temperature stability for the filter. The cutoff and boost values for servo reads are automatically switched when servo mode is entered.

The filter transfer function is normalized to 1.0 rad/s and given below:

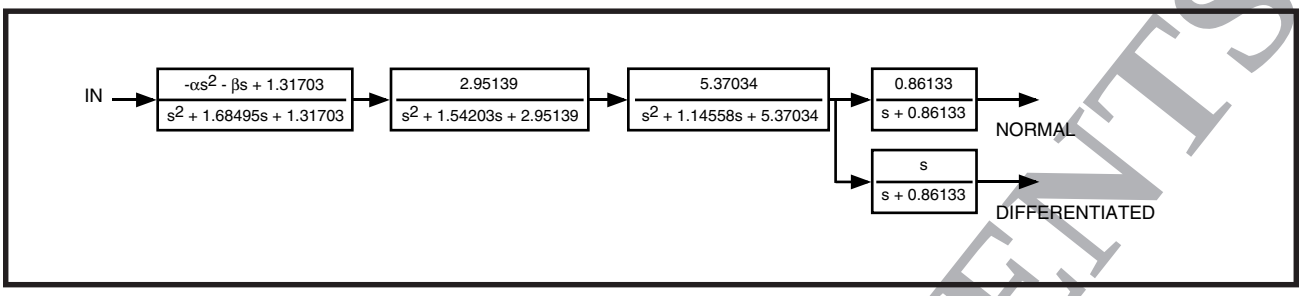


FIGURE 12: Filter Transfer Function

Shown also are theoretical magnitude response at no boost and 15 dB boost with $\Delta\%$ = 0%, and group delay response at $\Delta\%$ = -30%,0% 30% with no boost.

Alpha and the boost in dB are related by:

$$\alpha = 1.31703 \bullet (10^{dB/20} - 1)$$

Beta and $\Delta\%$ are related by: $\beta = 0.04183 \bullet \Delta\%$.

To denormalize the response to fc multiply the frequency by 2 pF, and divide the group delay response by 2 pF. For example if fc = 30 MHz, multiply the frequency axis by $1.885 \bullet 10^8$ for rad/s conversion or by $30 \bullet 10^6$ for Hz conversion. For the group delay, divide the delay numbers by $1.885 \bullet 10^8$. The delay of 3.18 s translates to 16.87 ns.

Five definitions are introduced for the discussion below:

Cutoff Frequency: The cutoff frequency is the -3 dB low pass bandwidth with no boost & group delay equalization, i.e. $\alpha = 0$ and $\beta = 0$.

Actual Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha = 0$ and/or $\beta = 0$

Alpha Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha = 0$ and without group delay equalization. In general, the actual boost with group delay equalization is higher than the alpha boost. However, with >3 dB alpha boost, the difference is minimal.

Group Delay $\Delta\%$: The group delay $\Delta\%$ is the percentage change in absolute group delay at DC with respect to that without equalization applied (β =0)

Group Delay Variation: The group delay variation is the change in group delay from DC to the cutoff frequency.

Cutoff Control

The programmable cutoff frequency from 10 to 64 MHz is set by the 7 bit linear FC DAC. The filter cutoff is set by the Data Cutoff Register in non-servo mode and is set by the Servo Cutoff Register in servo mode. The cutoff frequency is set as:

$$FC(MHz) = FC \bullet 0.4959 + 1.0022$$
$$18 \leq FC \leq 127.$$

The filter cutoff (FC) is defined as the -3 dB bandwidth with no boost applied. When boost/equalization is applied, the actual -3 dB point will move up. The ratio of actual -3 dB bandwidth to the programmed cutoff is tabulated below as a function of applied boost at the normalized frequency of 1.0 rad/s. To denormalize, multiply frequency by 2 pF.

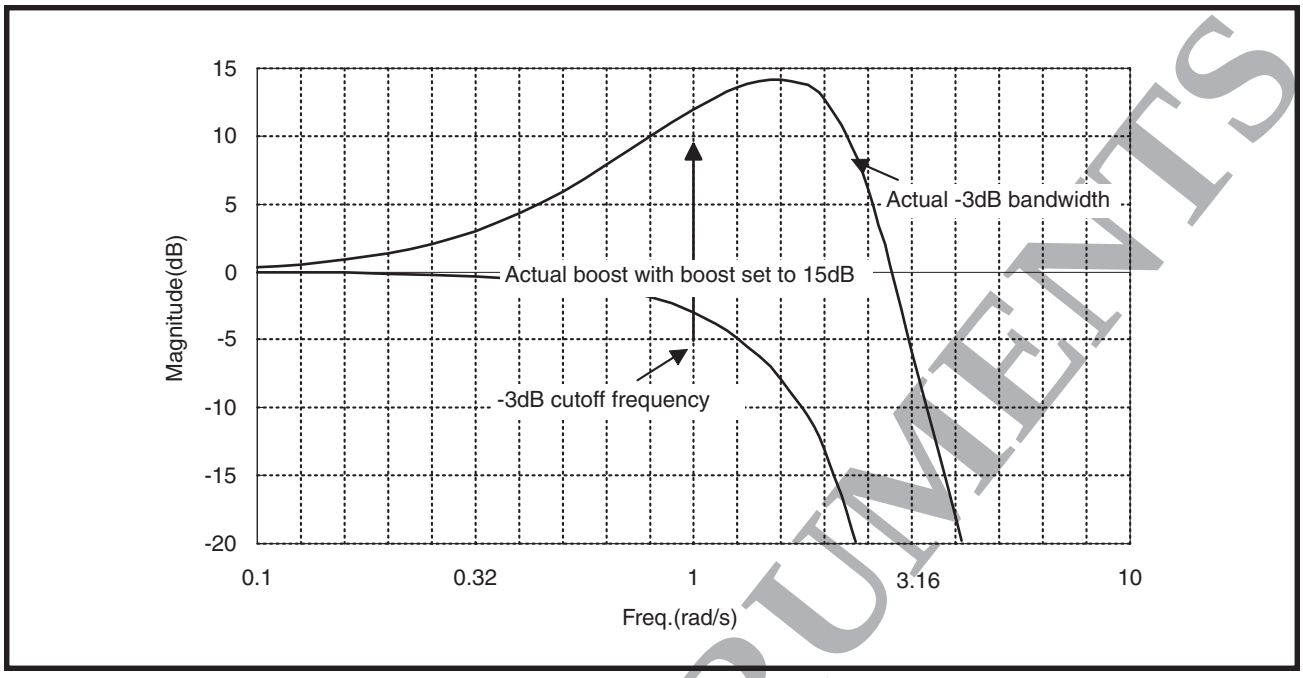


FIGURE 13: Filter Magnitude Response (Δ% = 0)

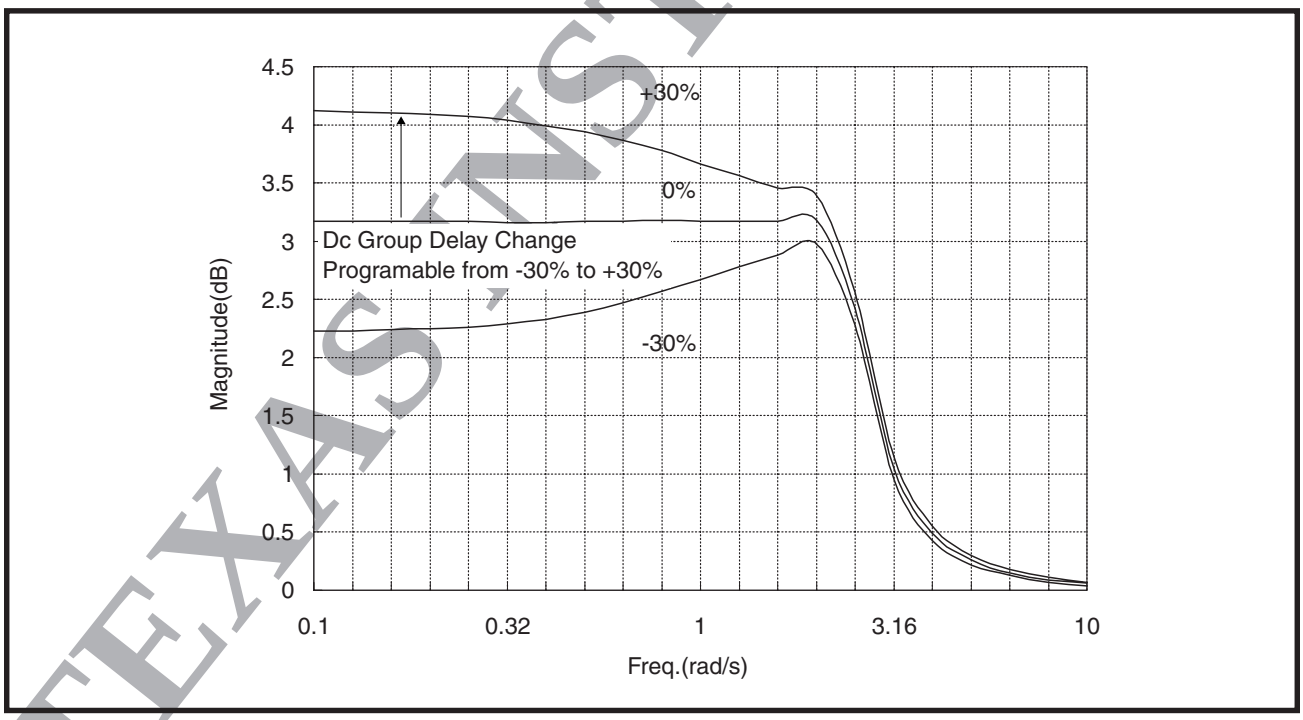


FIGURE 14: Filter Group Delay Response (Boost = 0 dB)

PROGRAMMABLE FILTER CIRCUIT (continued)

TABLE 1: Filter Magnitude Response

Freq. (rad/s)	Magnitude						
	Bst = 0db	3db	6db	9db	11db	13db	15db
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0
0.10	-0.03	0.00	0.05	0.12	0.19	0.26	0.36
0.20	-0.13	0.02	0.21	0.48	0.72	1.00	1.35
0.30	-0.28	0.04	0.47	1.04	1.52	2.08	2.74
0.40	-0.49	0.07	0.80	1.73	2.48	3.35	4.32
0.50	-0.75	0.10	1.18	2.51	3.53	4.67	5.92
0.60	-1.07	0.13	1.59	3.30	4.58	5.97	7.44
0.70	-1.45	0.15	2.00	4.08	5.59	7.17	8.83
0.80	-1.90	0.13	2.38	4.80	6.50	8.25	10.05
0.90	-2.42	0.08	2.71	5.44	7.30	9.19	11.1
1.00	-3.01	-0.01	2.99	5.99	7.99	9.99	11.99
2.00	-13.13	-4.67	0.81	5.22	7.84	10.31	12.66
3.00	-35.67	-22.21	-15.71	-10.88	-8.09	-5.52	-3.08

TABLE 2: Filter Group Delay Response w / Boost = 0 dB

Freq. (rad/s)	Delay (sec)						
	-30%	-20%	-10%	0%	10%	20%	30%
0.00	-2.22	-2.54	-2.86	-3.18	-3.49	-3.81	-4.13
0.10	-2.23	-2.54	-2.86	-3.17	-3.49	-3.81	-4.12
0.20	-2.25	-2.54	-2.85	-3.17	-3.48	-3.79	-4.09
0.30	-2.28	-2.55	-2.85	-3.16	-3.48	-3.78	-4.04
0.40	-2.33	2.56	-2.85	-3.17	-3.47	-3.76	-3.99
0.50	-2.39	-2.59	-2.86	-3.17	-3.47	-3.74	-3.94
0.60	-2.45	-2.62	-2.86	-3.17	-3.48	-3.73	-3.89
0.70	-2.52	-2.65	-2.87	-3.18	-3.48	-3.71	-3.78
0.80	-2.57	-2.67	-2.88	-3.18	-3.47	-3.68	-3.78
0.90	-2.62	-2.69	-2.88	-3.17	-3.46	-3.65	-3.72
1.00	-2.67	-2.71	-2.88	-3.17	-3.45	-3.62	-3.66
2.00	-2.98	-2.94	-2.95	-3.18	-3.41	-3.42	-3.39
3.00	-1.16	-1.13	-1.10	-1.27	-1.43	-1.41	-1.37

PROGRAMMABLE FILTER CIRCUIT (continued)

TABLE 3: Ratio of Actual -3 dB Bandwidth to Cutoff Frequency.

Boost (dB)	Group delay						
	±0%	±5%	±10%	±15%	±20%	±25%	±30%
0	1.00	1.01	1.06	1.16	1.31	1.47	1.62
1	1.19	1.21	1.28	1.38	1.50	1.62	1.74
2	1.49	1.51	1.56	1.63	1.71	1.79	1.87
3	1.79	1.80	1.83	1.87	1.91	1.96	2.01
4	2.03	2.04	2.05	2.07	2.09	2.11	2.14
5	2.20	2.20	2.21	2.22	2.23	2.24	2.25
6	2.32	2.32	2.33	2.33	2.34	2.34	2.35
7	2.42	2.42	2.42	2.43	2.43	2.44	2.44
8	2.51	2.51	2.51	2.51	2.51	2.52	2.52
9	2.59	2.59	2.59	2.59	2.59	2.59	2.59
10	2.66	2.66	2.66	2.66	2.66	2.66	2.67
11	2.73	2.73	2.73	2.73	2.73	2.73	2.73
12	2.80	2.80	2.80	2.80	2.80	2.80	2.80
13	2.86	2.86	2.86	2.86	2.86	2.86	2.86
14	2.93	2.93	2.93	2.93	2.93	2.93	2.93
15	3.00	3.00	3.00	3.00	3.00	3.00	3.00

TABLE 4: Actual Boost vs Alpha Boost & Group Delay Change at w = 1.0 rad / s

Boost (dB)	Group delay						
	±0%	±5%	±10%	±15%	±20%	±25%	±30%
0	0.00	0.11	0.42	0.89	1.47	2.12	2.81
1	1.00	1.09	1.33	1.72	2.21	2.76	3.36
2	2.00	2.07	2.27	2.58	2.99	3.45	3.97
3	3.00	3.05	3.21	3.47	3.80	4.19	4.63
4	4.00	4.04	4.17	4.38	4.65	4.97	5.34
5	5.00	5.03	5.14	5.30	5.52	5.79	6.10
6	6.00	6.03	6.11	6.24	6.42	6.64	6.89
7	7.00	7.02	7.09	7.19	7.34	7.51	7.72
8	8.00	8.02	8.07	8.15	8.27	8.41	8.58
9	9.00	9.01	9.05	9.12	9.22	9.33	9.47
10	10.00	10.01	10.04	10.10	10.17	10.27	10.38
11	11.00	11.01	11.03	11.08	11.14	11.21	11.30
12	12.00	12.01	12.03	12.06	12.11	12.17	12.24
13	13.00	13.01	13.02	13.05	13.09	13.14	13.19
14	14.00	14.00	14.02	14.04	14.07	14.11	4.15
15	15.00	15.00	15.01	15.03	15.06	15.09	15.12

Boost Control

The programmable alpha boost from 0 to 15 dB is set by the 7 bit linear FB DAC in data mode or 2 bit linear FBS DAC in servo mode. The alpha boost in data mode is set as:

$$\text{Boost(dB)} = 20\log(0.04345 \bullet FB - 0.0000337 \bullet FC \bullet FB + 1) \quad 0 \le FB \le 127$$

The programmed alpha boost is the magnitude gain at the cutoff frequency with no group delay equalization. When finite group delay equalization is applied, the actual boost is higher than programmed alpha boost. However, the difference becomes negligible when the programmed alpha boost is >3 dB. The table below tabulates the actual boost at $\omega = 1.0$ as function of the applied alpha boost & group delay equalization.

In servo mode, the 2-bit FBS Register controls the boost as:

$$\text{Boost(dB)} = FBS \bullet 2.0$$

That is, the boost in servo mode can be changed in 2 dB steps from 0 to 6 dB.

Group Delay Equalization

The group delay $\Delta\%$ can be programmed between -30% to +30% by the 6-bit linear FGD DAC. The FGD Register holds the 6-bit DAC control value. The group delay $\Delta\%$ is set as:

$$\text{Group Delay } \Delta\% = 0.9783 \bullet (FGD4{:}0) - 0.665\%, \text{ where FGD5 = sign and } 0 \le FGD[4{:}0] \le 31.$$

The group delay $\Delta\%$ is defined to be the percentage change of the absolute group delay due to equalization from the absolute group delay without equalization at DC. Tabulated below is the normalized group delay response as a function of β at 0 dB and 15 dB boost. To denormalize to f, multiply frequency and divide the delay by 2 pF. Note that $\Delta\%$ is not dependent on alpha setting; the group delay variation is. Shown in Table 5 is the group delay at boost set to 15 dB. For the boost = 0 dB case see Table 2.

TABLE 5: Filter Group Delay Response (Boost = 15 dB)

Freq. (rad/s)	Delay (sec)						
	-30%	-20%	-10%	0%	10%	20%	30%
0.0	-2.22	-2.54	-2.86	-3.18	-3.49	-3.81	-4.13
0.1	-2.35	-2.62	-2.90	-3.17	-3.45	-3.73	-4.00
0.2	-2.63	-2.80	-2.99	-3.17	-3.35	-3.53	-3.71
0.3	-2.90	-2.98	-3.07	-3.16	-3.26	-3.34	-3.43
0.4	-3.08	-3.11	-3.14	-3.16	-3.19	-3.22	-3.24
0.5	-3.20	-3.19	-3.18	-3.17	-3.16	-3.14	-3.14
0.6	-3.26	-3.23	-3.20	-3.17	-3.14	-3.11	-3.09
0.7	-3.28	-3.25	-3.21	-3.18	-3.14	-3.10	-3.07
0.8	-3.29	-3.25	-3.22	-3.18	-3.14	-3.10	-3.06
0.9	-3.28	-3.25	-3.21	-3.17	-3.13	-3.10	-3.06
1.0	-3.27	-3.24	-3.20	-3.17	-3.13	-3.09	-3.06
2.0	-3.22	-3.21	-3.20	-3.18	-3.17	-3.15	-3.14
3.0	-1.29	-1.28	-1.28	-1.27	-1.26	-1.25	-1.25

FUNCTIONAL DESCRIPTION (continued)

INTERNAL AC COUPLING

The conventional ac coupling at the filter/qualifier interface is now replaced by a pair of feedback circuits, one for the normal and one for the differentiated filter outputs. The offset of each of the filter outputs are sensed, integrated, and fed back to the filter output stage. The feedback loop forces the filter output offset nominally to zero. In the normal read mode (LOWZ = 0), the integration time constant is set at 6 µs until the internal pulse counter reaches SFC. The operation of the counter is discussed in more detail in the "Acquisition of DS VCO Sync" section. When the counter reaches SFC, the offset sensing is switched to the sampled data processor (SDP) and the time constant is reduced to 125 ns (effectively 250 ns due to the fact that zero's only occur at less than a half of the time during equalizer training). The SDP generates an offset voltage by sampling only the zeros that are qualified in the 3-level slicer. This ensures that the sampled zero voltage level, not the filter output, will be offset free.

When LOWZ = 1, the integration time constant is reduced to roughly 300 ns to quickly absorb the dc offset of the filter. The switch-over from continuous to sampled data can be disabled by setting PD:ACSWT = 1. In this case the ac coupling will continue to derive offset from continuous filter output.

The integration time constant is increased by a factor of 4, to 0.5 µs, after the synch byte has been detected, to make the offset correction less dependent on data pattern. Note that the effective time constant is greater than 1.0 µs again due to the fact that the zero's only occur less than 50% of the time, depending on the data pattern.

The integration time constant is reverted back to its original value in the event of thermal asperity, if the fast offset nulling bit(MISC1:FOSNUL = 1) is set, on the falling edge of TAD signal till the end of Hi-Y period.

QASYM QUALITY FACTOR

Amplitude asymmetry quality factor, Qasym, is generated by sampling all "ones" and lowpass filtering them with a time constant set by bits 5,6 of CM4 Register. In the presence of amplitude asymmetry, the average of all "ones" will be a good indication of amplitude asymmetry. This is then buffered and differentially multiplexed to the ATO buffer. The differential signal is converted to a single-ended signal referenced to an internally generated reference voltage Vref = Maxref/2 = 1.6 V nominally. The time constant is doubled at SFC.

The amplitude asymmetry of the incoming read signal can be monitored at the ATO pin when selected by the ASEL bits in the PD Register and can be used as a guide to setting MR element currents in the preamp.

Qasym can be placed in hold mode after the training sequence by setting the FRZQASM bit in CM4 and will hold its value for several microseconds in hold mode.

Also the asymmetry measure can be used to modify the Data Level Threshold (3-level slicer) and EPR4 constants via serial port control. This correction of the Data Level Threshold and EPR4 constants can enabled by setting CM4:QalvlEN and FIR2:QaeprEN, respectively. Also, the asymmetry correction magnitude is programmable via a pair of 3bit DACs, CM4:QaLVL and FIR2:QaEPR.

ADAPTIVE EQUALIZER CIRCUIT

Up to 7 dB of cosine equalization for fine shaping of the incoming read signal to the PR4 target is provided by a 5 tap, sampled analog, transversal filter. There are basically two modes of operations: One is to use the self adapting feature of the equalizer and the other to force a fixed symmetrical coefficient from the serial port. This mode selection is controlled by AEE bit in SLC Register.

The adaptive equalizer zero forcing algorithm adjusts the KM1 (inner tap coefficients) gain by integrating the equalization error of “zero” samples. After sync field count is reached, with SLC:AEE=1, the FIR equalizer will adapt to a special training pattern (NRZ:91A0h; Encoded:12324h). Adaptation can be left enabled past sync byte detection into the user data by appropriately setting SLC:AED. If the adaptive equalizer is enabled over data the integration time constant can be increased by 7 times for lower noise sensitivity by setting SLC:AEGS. When a training pattern is used along with the KM1 preset function the adaptive equalizer integration time constant may also be increased 7x in the training fields by setting DRC:LOWEQG. It should be noted that the KM1 preset setting of the FIR1:KM1PS will be used as a starting point for adaptation. The setting of 0000 for FIR1:KM1PS means that adaptation starts from zero gain setting for KM1. Only negative KM1 gain settings can be entered into the serial port.

With SLC:AEE = 0, the equalizer will simply reflect the gain setting at KM1 bits and remain fixed.

Additionally, there is a mode which will initiate A/D conversion of the tap weight following the adaptation for readout to the serial port. This mode can be selected by setting SLC:AEQADC to 1. This mode can be most useful in applications where overhead imposed by training field must be minimized. In this mode the channel would write consecutive training bytes in the user data section following the sync byte(s) and simply read out the A/D converted 4 bits word in the FIR1 Register after RG deassertion. The A/D conversion will commence at the end of read and will take at most 16 µs. The A/D converted word (4 bits) is made available in FIR1[7:4] and reset upon serial port read. This A/D output may then be used as the KM1 preset value (FIR1:KM1PS).

The multiplier coefficients for the adaptive taps can be held for up to 10 µs typical if the EQHOLD input is brought high in read mode after sync byte detect has occurred.

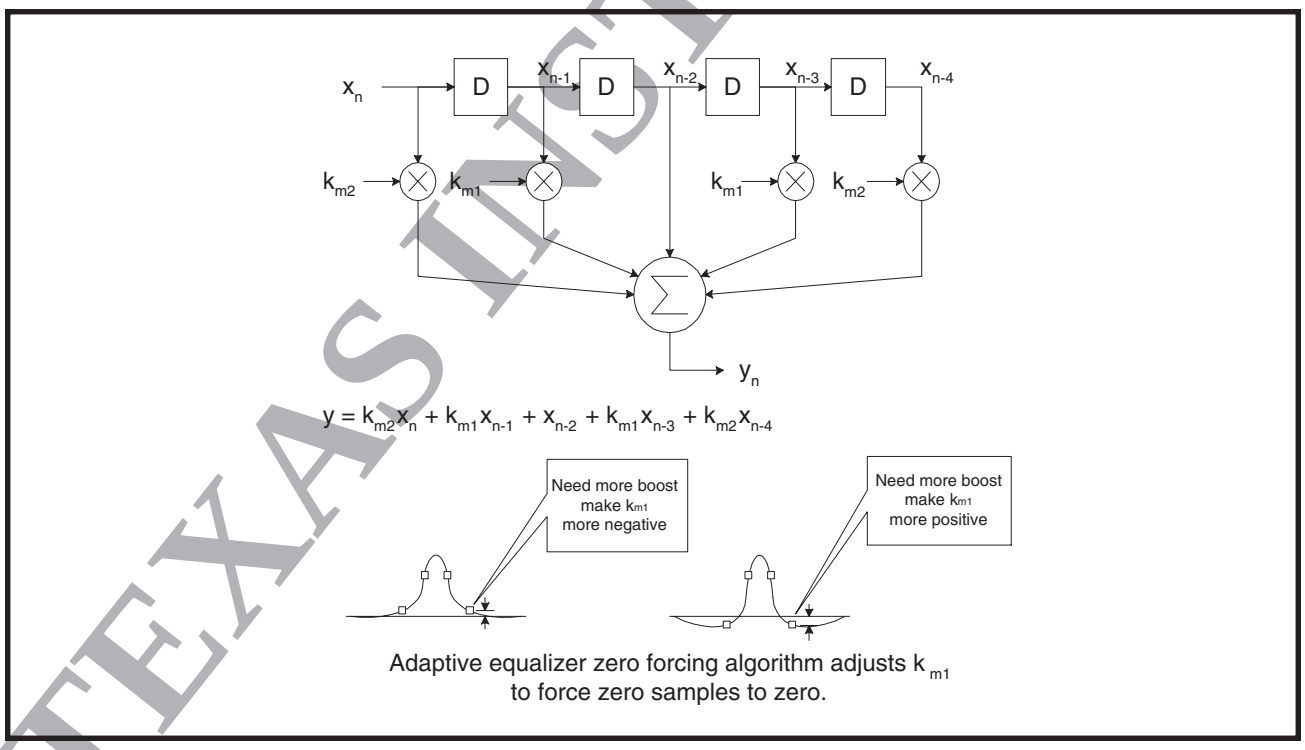


FIGURE 15 : Adaptive Equalizer Block Diagram

FUNCTIONAL DESCRIPTION (continued)

DIGITAL CHANNEL QUALITY MONITOR

The primary purpose of the Channel Quality Monitor, or CQM, is to monitor the channel quality and facilitate the tuning of user controlled parameters. Additionally, it can be used to adjust the setting for BLOS by monitoring the number of AGC comparator outputs by setting CQM3:CQMCTRL=100b.

In the primary mode, any one of three types of quality factors can be selected by appropriately setting CQM3:CQMCTRL. When set = x01b, the CQM counter is incremented whenever an inconsistency maxmet state transition event is found in the EPR4 detector. When set to x10, the CQM counter is incremented whenever the M2SB(2nd MSB) of maxmet decision appropriately delayed to match the delay thru the Survival Path Reg. does not agree with the Sur.Path Register output. When set to x11, the CQM counter is incremented whenever the MSB of maxmet decision appropriately delayed to match the delay thru the Sur.Path.Reg. does not agree with the Sur.Path Register output. In all three case, the count is integrated by a 16-bit counter.

These quality factors will have different correlation to the actual BER. In all cases, however, the lower the count, the better the BER.

To tune the channel, the user may observe the count and adjust parameters in the direction of reducing this count.

The count begins when either the sync byte detect (SBD) or the sync field count (SFC) signal is detected, as programmed by CQM3 bit 2. A timing diagram of the operation is shown below in Figure 16: CQM Timing Diagram.

When RG is de-asserted, the 16-bit counter value is written back to registers CQM1[7:0] & CQM2[7:0], and can be read out through the serial port. The action of reading the CQM1 Register resets the 16-bit counter. Therefore CQM2 should be read prior to CQM1.

In the additional mode, the full-wave rectified AGC signal peaks are detected and fed to the CQM counter. The count begins on the Servo hold and continues until the first rising edge of the Strobe signal. This mode is intended to be used in BLOS adjustment.

The table below summarizes the CQM control bits in CQM mode and normal operation (where the CQM is disabled).

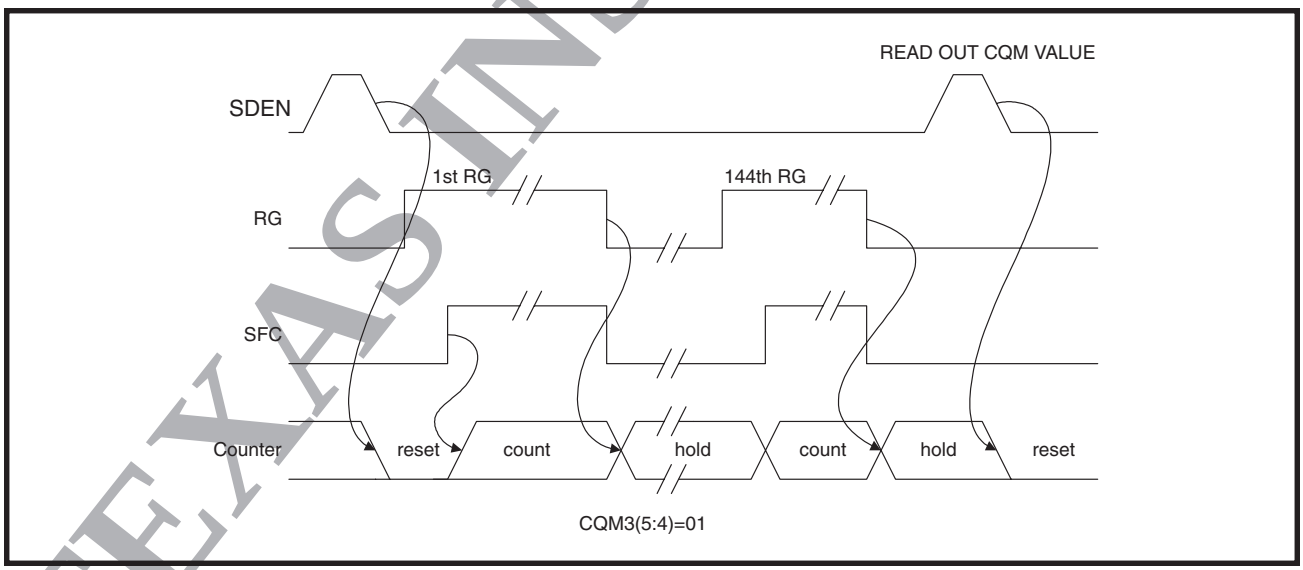


FIGURE 16: CQM Timing Diagram

TABLE 6: CQM Modes of Operation

Serial Port Register	CQM mode setting	Utility
CM3[2-0]	Mode selection	When SURVSEL = 0; 000 = Disable CQM function, x01 = Counts Maxmet inconsistency events in CQM counter, x10 = Counts Maxmet M2SB inconsistency events in CQM counter, x11 = Counts Maxmet MSB inconsistency events in CQM counter, In the above three cases the counter starts from SBD(x = 0) or VCOLOCK (x = 1). 100 = CQM input from AGC comparator intended for use in BLOS adjustment
CQM3[5-4]	When counting FIR samples, defines the accumulation periods in terms of RG cycles	00 = 1 RG period 01 = 144 RG periods 10 = 528 RG periods 11 = 1008 RG periods
CQM1[7:0] & CQM2[7:0]	16-bit counter value (read only)	Read only

TIME BASE GENERATOR CIRCUIT

The time base generator (TBG) is a PLL based circuit that provides a programmable reference frequency to the data separator for constant density recording applications. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N, and DR Registers. The TBG output frequency, Fout, should be programmed as close as possible to ((17/16) • NRZ Data Rate). The time base also supplies the timing reference for write precompensation so that the precompensation tracks the reference time base period.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to reduce the effects of common mode noise.

In read, write and idle modes, the programmable time base generator is used to provide a stable reference frequency for the data separator. In the write and idle modes, the TBG output (divided by 2), when selected by the CM Register TP bits, can be monitored at the TPF and $\overline{\text{TPF}}$ test pins. In the read mode, the TBG output should not be selected for output on the test pins to minimize the possibility of jitter in the data separator PLL.

The reference frequency is programmed using the M and N Registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

F_{TBG} = FREF [(M + 1) / (N + 1)]

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The DR Register must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N Registers only after the DR Register is updated.

TIME BASE GENERATOR CIRCUIT (continued)

The DR Register value directly affects the following parameters:

- center frequency of the time base generator VCO,
- center frequency of the data separator VCO,
- phase detector gain of the time base generator phase detector,
- phase detector gain of the data separator phase detector,

The reference current for the DR DAC is set by a fixed external resistor, RR, connected between the RR pin and ground.

RR = 8.06 kΩ for 240 Mbit/s operation.

DATA SEPARATOR CIRCUIT

The Data Separator circuit provides complete encoding, decoding, and synchronization for 16/17 (0,6/8) GCR data. In data read mode, the circuit performs clock recovery, framing/sync byte detection, decoding, descrambling, and NRZ interface conversion. In the write mode, the circuit generates the VCO sync field, scrambles and converts the NRZ data into 16/17 (0,6/8) GCR format, proceeds the data, and performs write precompensation.

The circuit consists of five major functional blocks: the data synchronizer, 16/17 ENDEC, NRZ scrambler / descrambler, NRZ interface, and write precompensation.

Zero Phase Restart

Circuitry is included to speed up the initial acquisition of DSPLL (Data Separator Phase Lock Loop). Following the assertion of RG, the sampling clock for DSPLL will be held until the sampling clock lines up with the preamble pattern. This will reduce phase error at the beginning of DSPLL acquisition. When this is done the acquisition time of the DSPLL will be dramatically reduced. The threshold at which the sampling clock is released is controlled by the settings in ZPRDAC[4:0]

During TestZPR = 1 mode, the DSPLL loop will be open and the phase error will be integrated between the time the sampling clock is restarted until vcolock. This value is then held to RG deassertion and can be read back. The read back value will be in sign and magnitude format. The DAC setting must be adjusted until this integrated phase error is minimized.

Data Synchronizer

The data synchronizer uses a fully integrated, fast acquisition, PLL to recover the code rate clock from the incoming read data. To achieve fast acquisition, the data synchronizer PLL uses two separate phase detectors to drive the loop. A decision-directed phase detector is used in the read mode and phase-frequency detector is used in the idle, servo, and write modes.

In the read mode the decision-directed timing recovery updates the PLL by comparing amplitudes of adjacent “one” samples or comparing the “zero” sample magnitude to ground for the entire sample period. A special (non IBM) algorithm is used to prevent “hang up” during the acquisition phase. The determination of whether a sample is a "one" or a "zero" is performed by the 3-level slicer.

The gain of the phase detector is reduced by a factor of 5 after the SFC to reduced the bandwidth of the loop. This increases the immunity of the loop from noise during data.

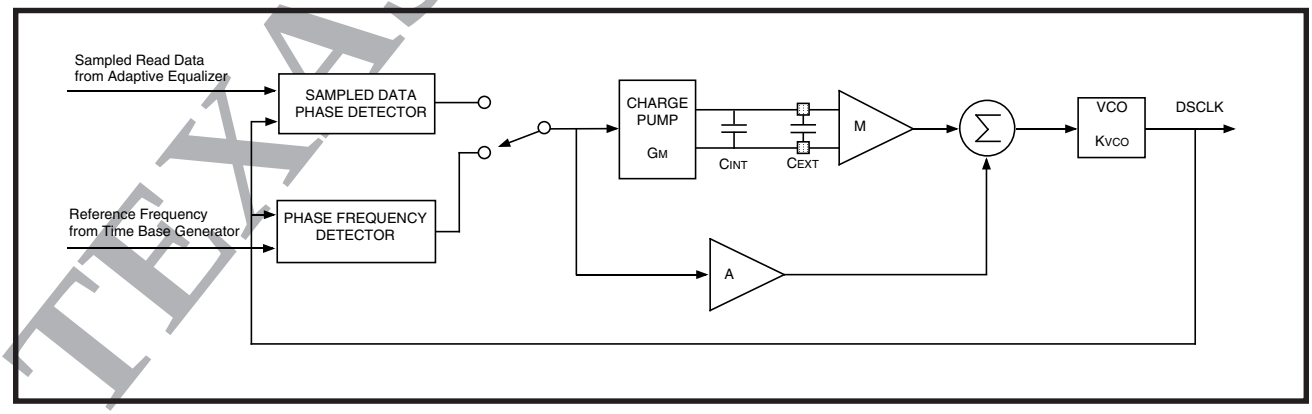


FIGURE 17: Data separator phase-locked loop block diagram

In the write and idle modes the non-harmonic phase-frequency detector is continuously enabled, thus maintaining both phase and frequency lock to the time base generator's VCO output signal, FTBG. The polarity and width of the detector's output current pulses correspond to the direction and magnitude of the phase error.

The two phase detector outputs are mixed into a single differential charge pump which drives the loop filter directly. The loop filter requires an external capacitor. The loop damping ratio is programmed by bits 6 - 0 in the DRC Register. The programmed damping ratio is independent of data rate.

In write mode, the TBG output is used to clock the encoder, precoder, and write precompensation circuits. The output of the precompensation circuit goes to the write data flip-flop which generates the write data (WD, $\overline{WD}$) outputs.

ENDEC

The ENDEC implements a Silicon Systems proprietary 16/17 (0,6/8) Group Code Recording (GCR) algorithm. The code has a minimum of no zeros between ones and a maximum of six and eight zeros between ones for the noninterleaved and interleaved samples, respectively. During write operations the encoder portion of the ENDEC converts two bytes of data, scrambled or unscrambled, to 17 bit parallel code words that are then converted to serial format. In data read operation, after the code word boundary has been detected in the viterbi qualified serial data stream, the data is converted to 17 bit parallel form and the decoder portion of the ENDEC converts the 17 bit code words to two bytes of NRZ format.

Sync Word

The SSI 32P4103A uses a dual sync word scheme (SB1 and SB2, each 17-bit long) to reduce the probability that a single error event will cause the sync byte to be missed. SB1 and SB2 are NRZ:91B1h, or 12335h encoded and NRZ:9103h or 12343h encoded, respectively. Only the last 9 bits of the 17-bit word are bit by bit checked against the last 9 bits of SB1 and SB2 for detection. Since this will provide separation of 8 bits between the two 9-bit words that are checked for sync word detection, a single error event, which typically causes 4 consecutive bits errors, will not overlap both. Additionally a programmable number of pads (as set by CM3:STRB) can be placed between the two sync words to combat problems encountered during thermal asperity events.

The first sync byte (SB1) is optional. Since the SSI 32P4103A looks for either sync word, the absence of the SB1 is not an error.

When CM1:TRSQ is set, the training/sync byte sequence is generated with an internal state machine. Once SSI 32P4103A receives all FFh NRZ pattern from HDC after write gate is asserted, the internal state machine automatically generates one equalizer training pattern (91A0h, NRZ or 12324h encoded) first sync word (SB1), one equalizer training pattern and second sync word (SB2). The SSI 32P4103A needs only one FFh NRZ pattern in order to trigger the internal state machine, the following seven bytes do not need to be FFh pattern, since they are ignored.

TABLE 7: Summary of Training and Sync Byte

Sync Word	NRZ	(16/17) [0,6/8] Encoded
TRAINING	91A0h	12324h
SB1	91B1h	12335h
SB2	9103h	12343h

Additional discussion of sync byte generation and detection is in the “Description of Operating Modes” section.

Dual Header

The purpose of the dual header is to allow for a more robust sync byte detection against TA events during preamble period which may cause false PLL locking. This mode is invoked when both RCVRM1 & RCVRM0 bits in the MISC1 Register are set to 1. In this mode, the user may write secondary preamble pattern(plus additional training pattern, if desired) between two sync words. The user can write a secondary preamble pattern using NRZ = FE7Fh. The total words(17bits) of secondary preamble pattern (including any additional training pattern written) has to match the setting of CM3:STRB(5:0), 0 - 31 words. During the read, if the channel is unable to detect the first sync word due to a TA event before the timer (whose duration in bytes is set by STM2:BYTEDLY[6:0] bits) runs out, the internal read gate is automatically toggled once over the secondary preamble pattern, and the process of the PLL locking sequence and the detection of a second sync word begins. The user has to set the appropriate number of bytes in BYTEDYL[6:0] of Register STM2 corresponding to the time period from the rising edge

DATA SEPARATOR CIRCUIT (continued)

of RG to when the internal read is to be toggled so that the internal read gate toggles at or around the beginning of secondary preamble written. Refer Figure 30 and Figure 31.

Scrambler/Descrambler

The scrambler/descrambler circuit is provided to reduce fixed pattern effects on the channel's performance. It is enabled or disabled using CM1:SD. In write mode, if enabled, the circuit scrambles each NRZ byte of data before passing it to the encoder. Only user data, i.e. the NRZ data following the second sync byte, is scrambled. In data read mode, only the decoded NRZ data after the second sync byte is descrambled. The scrambler polynomial is H(X) = 1 xor X3 xor X10. The scrambler block diagram is shown in Figure 10. The scrambler is effectively clocked 8 times for each NRZ byte time, and the X2 through X9 outputs are XOR'd with the NRZ data (X2 is the LSB, and is XOR'd with NRZ0).

When the scrambler is enabled, the initial state of the scrambler is 3FFh, all ones, (or 2AAh depending upon CM3:SEED) , and the X output vector is FFh. The SEED bit is provided to allow the scrambler seed to be switched on alternating tracks if desired. At the next NRZ byte, the scrambler has been clocked 8 times, the scrambler state is 31Ch and the X output vector is C7h. The X output vector repeats every 1023 byte times.

When the scrambler is disabled, the flip-flops are preloaded with zeros, and the scrambler state (and the X vector) remains at zero. When this is XOR'd with the data, the data is unchanged.

Note that the scrambler and descrambler must be active during the normal read cycle to avoid errors caused by constant pattern effects.

NRZ Interface

As each NRZ byte is input to the SSI 32P4103A, its parity is checked against the controller supplied parity bit NRZP. If an error is detected, the PERR output pin goes high.

In data read mode, the NRZ data will be presented to the controller near the falling edge of RCLK so that it can be latched by the controller on the rising edge of RCLK. When RG goes high, the selected NRZ interface will output low data until the sync byte has been detected. The first non-zero data presented will be the sync byte (69h). The NRZ interface is at a high impedance state when not in data read mode. An even parity bit, NRZP, is generated for each output byte.

The duty cycle of the RCLK is varied as shown in the following diagram: It consists of a 5 Tc low period followed by three 4 Tc periods of alternating polarities.

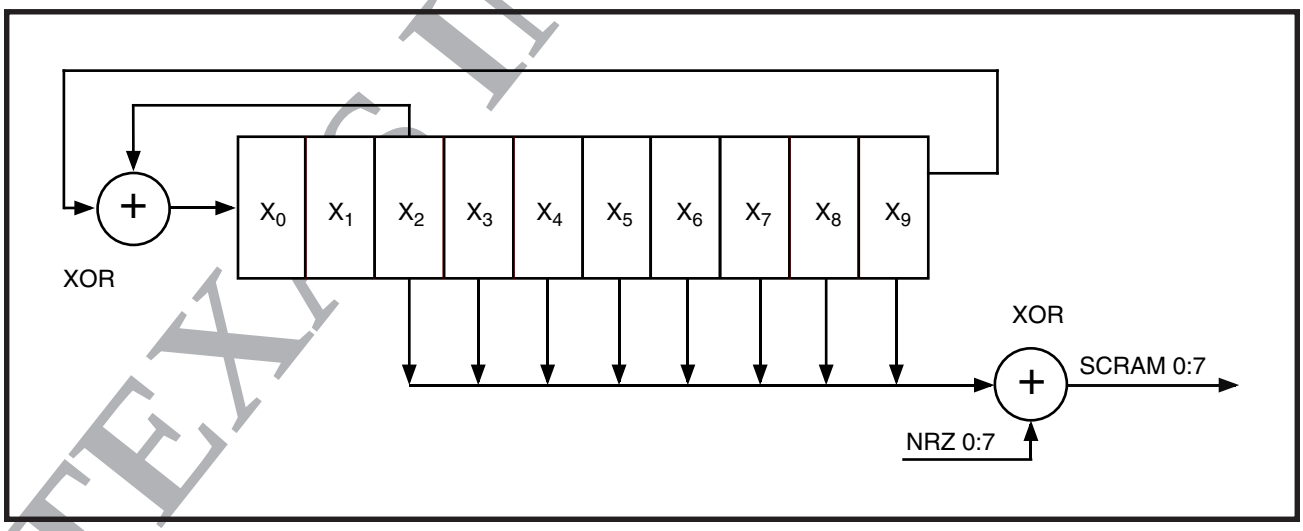


FIGURE 18: Scrambler block diagram

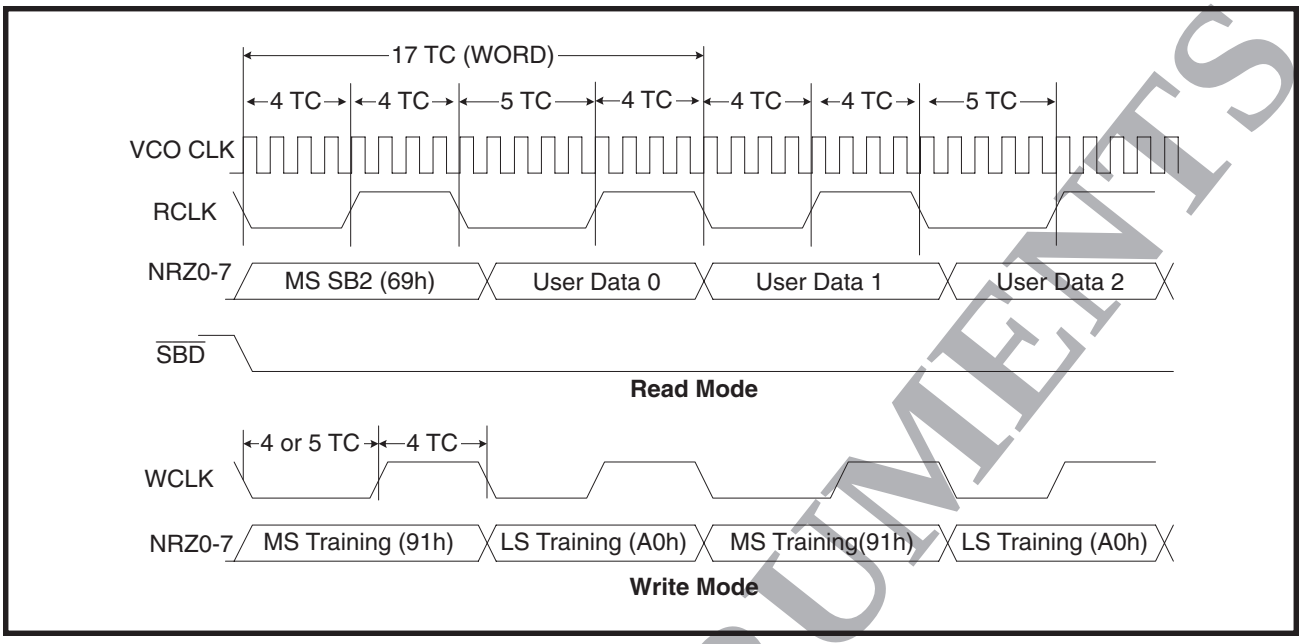


FIGURE 19: RCLK and WCLK vs. NRZ Data

Write Data Output, Precoder

In write mode, the encoded data at the ENDEC output is latched into a shift register, then shifted serially through the precoder and write precompensation circuits.

The encoded data is shifted into the precoder MSB first, LSB last. Prior to the first valid data from the encoder (the first byte of the training sequence), ones are clocked into the precoder. The precoder function is $1/(1 \oplus D^2)$. The precoder block diagram is shown below.

Write Precompensation

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognized specific write data patterns and can add delays in the time position of write data bits to counteract the magnetic nonlinearity effects. The magnitude of the time shift is programmable via WP Register and is proportional to the time base generator VCO period (TVCO).

SSI 32P4103A offers two independent levels of write current precompensation, Level 1 and Level 2. Level 1 is the extent of write precompensation applied to the second of the two consecutive transition in the late direction. Level 2 is the amount of precompensation applied to the second of the two transitions when transitions are two code periods (TVCO) apart. Level 3 is the precompensation applied to the third of three consecutive transitions. The magnitude of the primary and secondary precompensations, Level 1 and Level 2, are controlled by WPC1(lower 4) bits and WPC2(upper 4) bits of WP Register, respectively. Level 3 precompensation is derived as the difference between Level 1 and Level 2. The third level of precompensation reverts back to the primary precompensation by setting WP:WPC2 to 0h.

The write data flip-flop is included in the SSI 32P4103A, there should be no write data flip-flop in a read/write chip connected to the SSI 32P4103A.

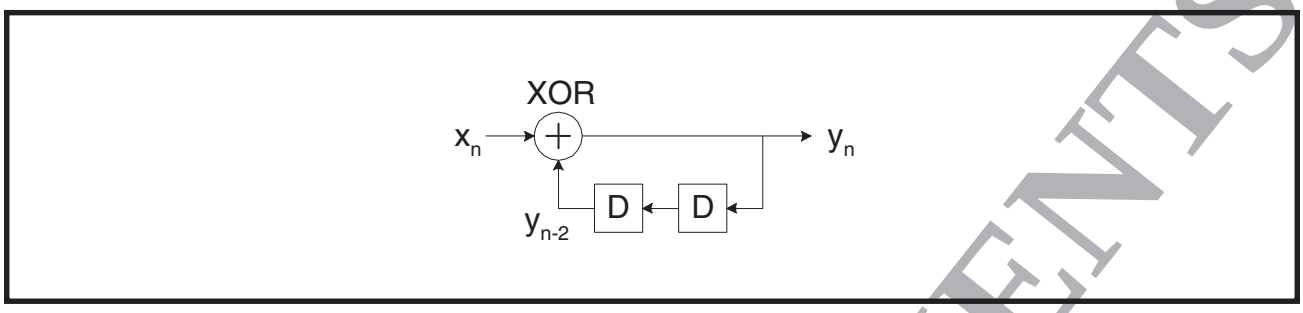


FIGURE 20: Precoder block diagram

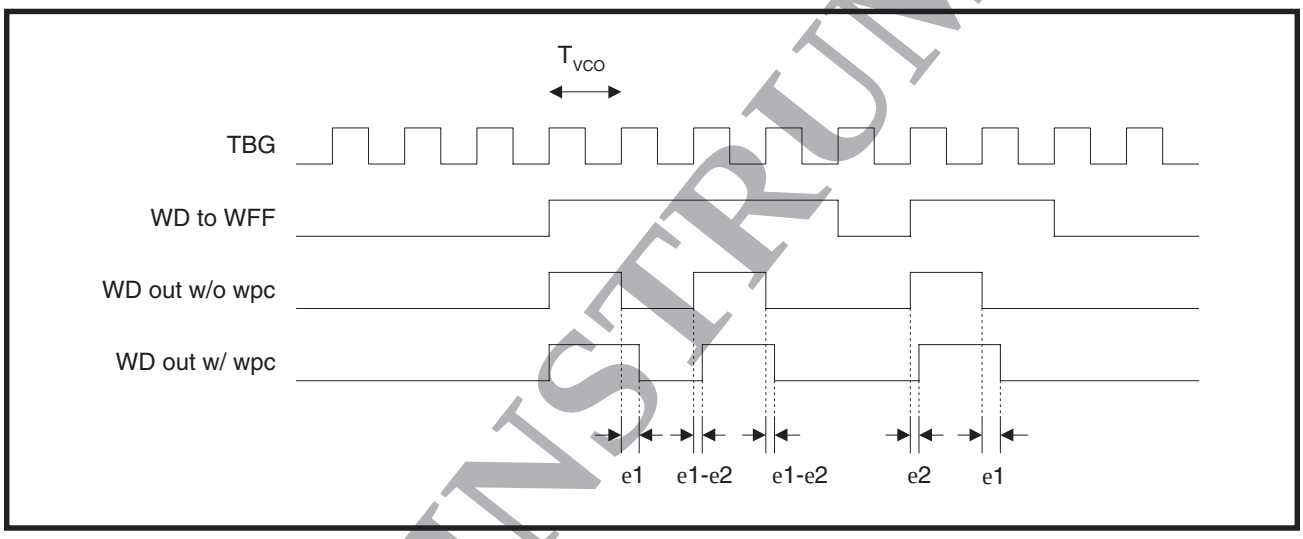


FIGURE 21: 3-Level Write Precompensation

DATA SEPARATOR CIRCUIT (continued)

TABLE 8: 3-Level Write Precompensation Algorithm

Interaction	WD input to Write F/F			Magnitude of Precompensation
	n-2	n-1	n	
No precompensation	0	0	1	0
One transition apart	0	1	1	Level 1
Two transitions apart	1	0	1	Level 2
Both one AND two transitions apart	1	1	1	Level 3

SERIAL PORT CIRCUIT

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the 39 internal registers of the SSI 32P4103A. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/$\overline{W}$ bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits contain the three device select bits, S0:S2, and the four address bits, A0:A3, which determine the internal register to be accessed. The entire byte is considered to be the Register String ID and is referred to in the following format: A3, A2, A1, A0, S2, S1, S0, R/$\overline{W}$.

The second byte contains the programming data. In read mode (R/$\overline{W}$=1) the SSI 32P4103A will output the register contents of the selected address. In write mode (R/$\overline{W}$=0) the device will load the selected register with data presented on the SDATA pin.

Additionally included is a serial port buffer for interface to the preamp. This will eliminate the need for an additional IC on the drive for buffering of the preamps serial port pins. There are three serial port bits (PSP1,2 and 3) assigned to control the transfer of serial data in this mode to and from the preamps serial port pins (PSDEN, PSCLK, PSDATA). In the default mode (PSP1,2,3=0) the PSDEN, PSCLK, and PSDATA are driven directly when SDEN is high AND RG=WG=SG=0. When PSP1=1, this transfer is disabled and the pins are in a Hi-Z state. Whenever this transfer mode is disabled, via SDEN, RG, WG, or SG, the three preamp serial port output pins are tri-stated (PSP2=0) or driven low (PSP2=1) depending upon the state of PSP2 bit. During a serial port transfer, if the R/$\overline{W}$ bit is '1', the SSI 32P4103A will detect if the following select bits, S0, S1, S2 are '100'. If so, the PSDATA pin is turned into an input following the 8th clock cycle and drives the SDATA output until the SDEN falling edge.

The PSP3 bit sets the preamp serial port buffer into TI mode of write operation. In this mode, the three outputs are not enabled unless R/$\overline{W}$, S0, S1, S2 bits are detected as '0100'. When detected, the three outputs are enabled AFTER the first 8 clock cycles of serial port transfer. Otherwise, the outputs are disabled. Note in TI mode, the serial port transfer to the preamp is only through the 8 data bits following the first 8 clock cycles.

During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in the electrical specifications section. Figure 22 shows the serial port interface timing.

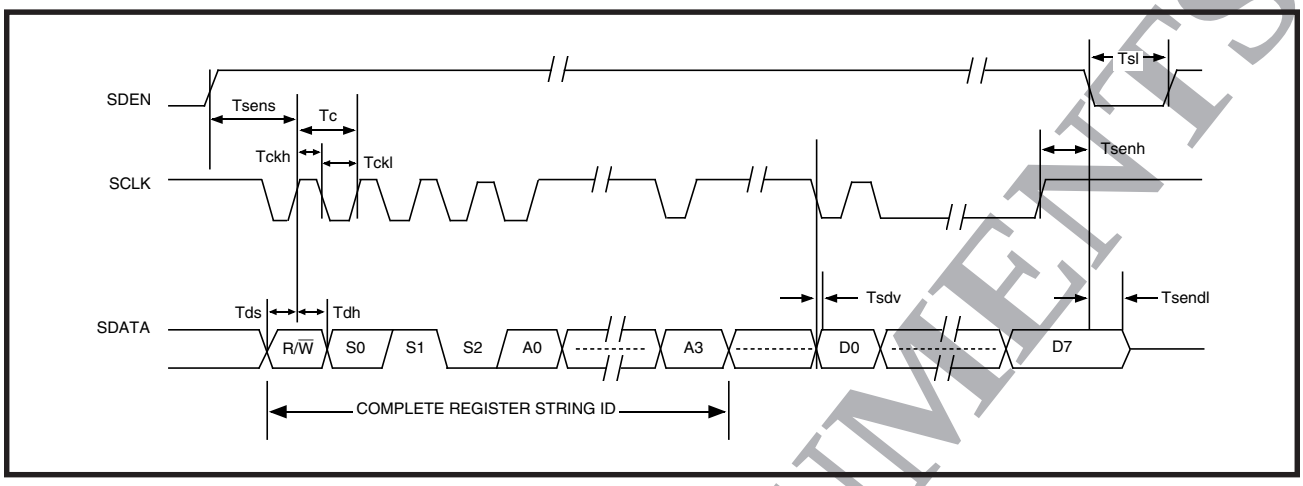


FIGURE 22: Serial Port Interface Timing

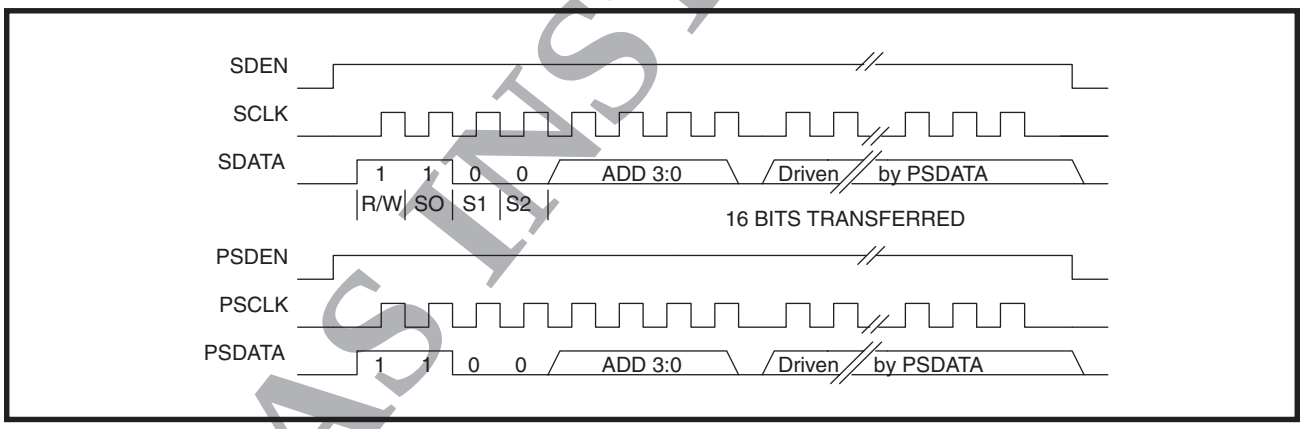


FIGURE 23: Preamp Serial Port Buffer Read Operation

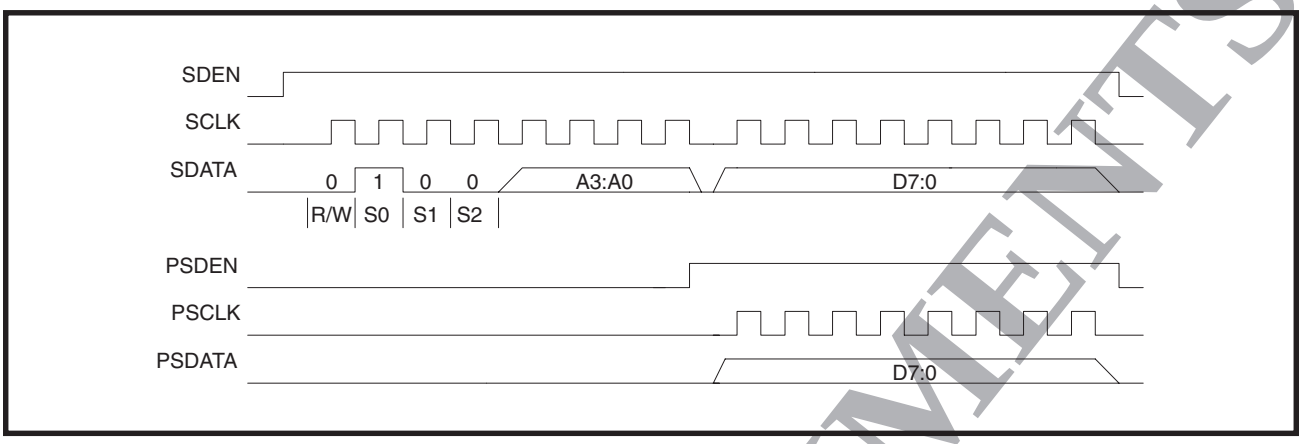


FIGURE 24: Preamp Serial Port Buffer TI Mode Write Operation

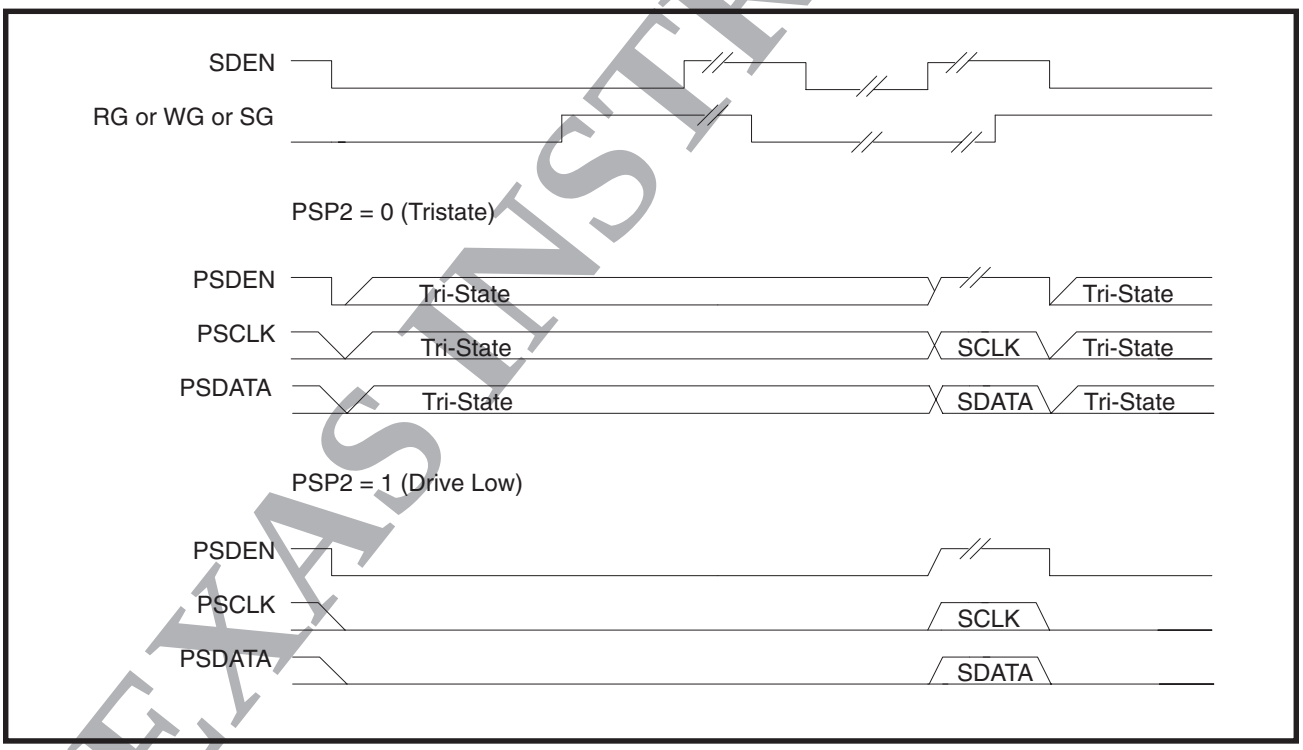


FIGURE 25: Preamp Serial Port Buffer Tristate Operation

FUNCTIONAL DESCRIPTION (continued)

THERMAL ASPERITY DETECTION AND SUPPRESSION

A thermal asperity event appears to the read channel as a sudden (10's of ns) base line shift of the incoming read signal followed by an exponential (300 to 500 ns time constant) decay. These events can occur in either direction. The magnitude of an asperity is defined as follows:

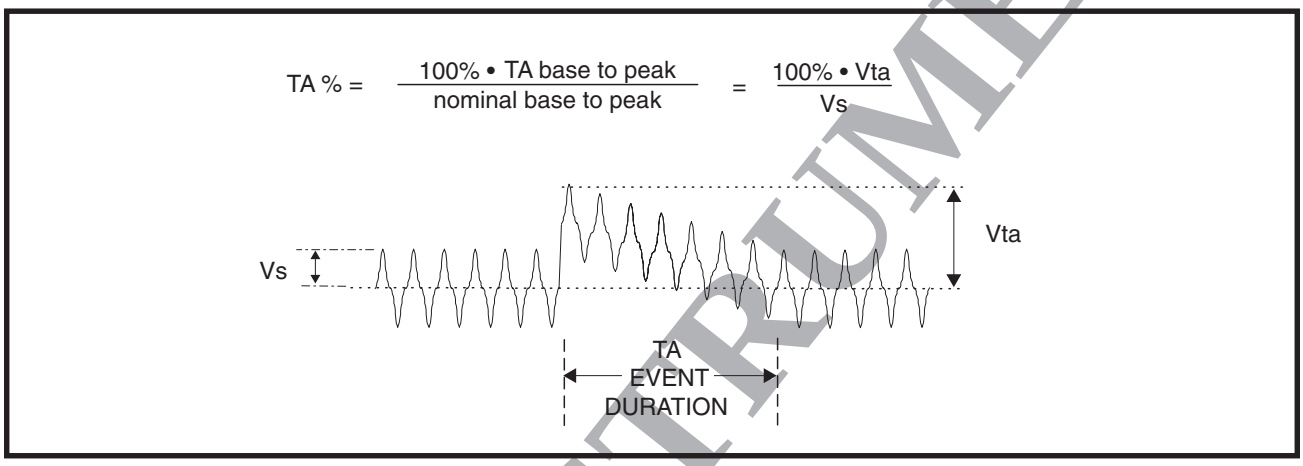


FIGURE 26: Thermal Asperity Definition

The thermal asperity detection and suppression circuitry in the SSI 32P4103A is designed to accommodate TA magnitudes as large as 500% while keeping the burst error length less than 5 bytes.

Thermal Asperity Detection Circuit

A thermal asperity can be detected using the on-chip detector (TAIO = 0) or an external detector may be used (TAIO = 1). Pin TAD is therefore an output if TAIO = 0 and an input if TAIO = 1. If an external detector is used, TAD has positive polarity (TAD = 1 indicates that an asperity has been detected).

The thermal asperity detector monitors the signal at the low-pass filter's output (DP/DN) with a threshold comparator. This comparator is very similar to the comparators used for level pulse qualification. Under normal conditions, the signal at this point should be about 1.4 Vp-p (0.7 Vpk). A thermal asperity will cause a sudden shift in the baseline voltage which will trip the threshold comparator. The threshold setting is programmable from +0.75 Vpk to +1.5 Vpk with 4 bits of resolution. This corresponds to a percent threshold setting from 107% to 214% of the nominal zero to peak voltage swing. When the signal crosses this threshold, the TAD signal is asserted. When the signal crosses the opposite polarity Level Qualifier threshold, the TAD signal is reset.

In order to keep the detection circuit from triggering on the normal AGC transient response, the detection circuit is held reset whenever the Low-Z or Fast Recovery modes are activated and during the period from RG rising to completion of Sync Field Count.

Thermal Asperity detection must be enabled by FB:ENTAD. The user should then program the TAth Register to set the detection threshold. It should be set high enough to avoid false triggering.

Thermal Asperity Suppression Circuit

NRZ errors caused by thermal asperity events are unavoidable. The suppression measures listed below are intended to limit the duration of the errors at the NRZ output. The suppression methods can only be activated when in Read mode (RG = high) after SFC or in Servo mode (SG = high).

But other modes can be selected by bits 5-3 of TA1 Register. TA1:TAIDLE is provided to allow TA detection and suppression (w/o PLL Hold) in IDLE mode, TA1:TARG is provided to allow TA detection and suppression in Read mode (RG=high), and LD:TARGB is provided to allow the data AGC to be held from the falling edge of RG to the SFC of the following RG.

If both SG and RG are high at the same time, the servo mode of operation will be asserted. If an asperity occurs within 4 µs (3,2 or 1 µs, depending on TA3:HIYTMR[1:0]) before the leading edge of RG or SG, the suppression measures will go active when RG or SG goes high and remain active for the indicated duration from the leading edge of TAD. At power-up, all the suppression features will be disabled and must be enabled via the serial port.

Dynamic Hi-Y

When the TAD signal goes active, the input admittance of the VGA amplifier can be quickly set to a higher value. This allows the high-pass corner at the VIA/$\overline{\text{VIA}}$ pins to be increased. If the AC-coupling capacitor at the VIA pin is C, and Yin is the differential input conductance between VIA and $\overline{\text{VIA}}$, then Fhp = 2•Yin/(2 • π • C). By moving Fhp to a higher frequency, the low frequency characteristic of the thermal asperity can be quickly attenuated. The input admittance will have a fast turn-on (<100 ns), slow turn-off (about 1 µs) characteristic to minimize glitches going in to the AGC amplifier. The Fhp frequency should be proportional to the NRZ data rate. Three serial port bits allow 8 different values of input admittance to be programmed, TA3:YIN bits control the admittance in non-servo mode and MISC2:YINS bits control it in servo mode. A serial port bit (MISC1:FOSNUL) is provided to enable a fast filter output offset cancellation during a TA event.

The duration of the Dynamic Hi-Y state will be 1 to 4 µs following the leading edge of TAD programmable from TA3 Register. A static Hi-Y mode is also available in which the Hi-Y condition will be asserted as defined by HYES bits in TA2 Register. This mode should prove useful in a “re-try” mode of thermal asperity suppression. The Dynamic Hi-Y can also be totally disabled via the serial port.

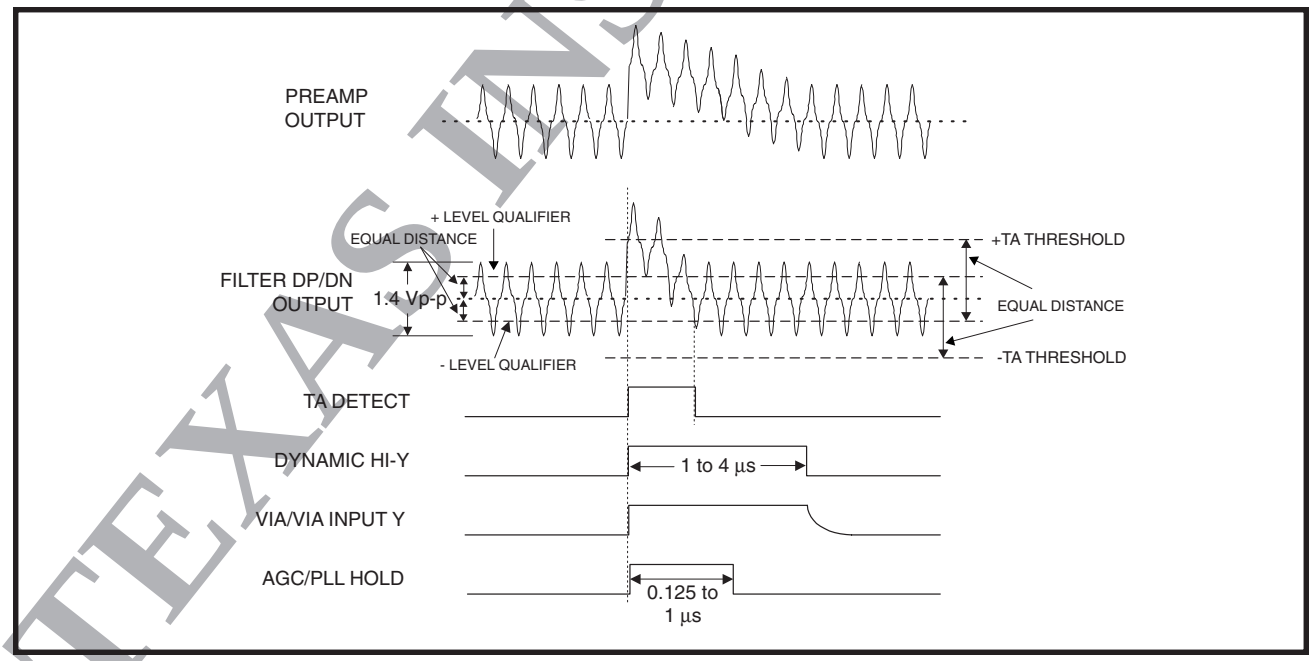


FIGURE 27: Thermal Asperity Suppression

THERMAL ASPERITY DETECTION AND SUPPRESSION (continued)

AGC/PLL Hold

The signal at DP/DN should not be used for adaptive AGC, equalization, timing extraction, or offset correction until the proper baseline has been restored. Therefore, all of these functions may be suspended for a programmable time period when a thermal asperity is detected. The hold time may be programmed (TA3:TATMR) from 0.125 µs to 1 µs with a 0.125 µs resolution. The user should program this time period to match the signal recovery time in the Dynamic Hi-Y mode. If this time period is set too long, there is a risk of losing the proper timing relationship in the PLL. The PLL hold function is also controlled by TA1:PLLHE. For a 00 setting the PLL hold is disabled over the TA event. A 01 setting enables the PLL hold time as described above but a 10 setting holds the PLL only for the time that the TA detect is high. TA1:TAPLLGS allows the PLL gain to be reduced during a TA event.

The AGC and AC_Coupling hold functions are enabled by TA1:AGCHE. The AGC hold function itself can be manually controlled by asserting the $\overline{\text{HOLD}}$ input pin. The PLL and Equalizer hold function can be manually controlled by asserting the EQ/PLLHOLD input pin. A serial port bit (SLC:AED) is provided to force equalizer hold following sync byte detect.

Error Flag (or Erasure Flag)

The error flag circuitry monitors the level slicer output from the sampled data processor. A run of 5 or 6 same polarity “1” samples indicates the occurrence of an asperity. This sets an internal error flag which marks the corresponding NRZ data as being corrupted. The circuit looks for an opposite polarity “1” to start the process of resetting the error flag. When an opposite polarity “1” is detected, an internal counter begins to count 6 internal clock periods. If a run of 3 or 4 positive “1” samples occurs during this count down, the counter starts over. If the counter is able to reach 6 without being restarted, the error flag is allowed to reset itself. The signal is output at the NRZP pin as selected by TM2:TSTSL.

The error flag signal is used to mark the potentially corrupted NRZ data. The signal should aid the external error correction circuitry in recovering the data during a thermal asperity event. The TAD and EFLAG signals can be mixed onto the RDS and PPOL pins when SG=0 by enabling BLO:RDSMUX.

Applying Thermal Asperity Detection and Suppression

The TA detection threshold should be set low enough to flag any asperity which can cause an error burst longer than the ECC can handle. When an asperity is detected, it is recommended that dynamic Hi-Y, AGC/PLLHOLD, and Error Flag monitoring be applied. This will give the best probability of “on-the-fly” asperity correction. The duration of AGC/PLLHOLD should be just long enough to prevent corrupt data from disturbing any of these control loops. The static Hi-Y mode is included to allow asperity correction on a “retry” basis.

Thermal Asperity Monitoring at TPE Pin

The TPE pin is for various test and verification purposes. One of them is to monitor the thermal asperity time-out signal for suppression. The truth table for the TPE output at various register bit settings is shown in the Power Down Register bit definition section. Both Hi-Y and AGCHOLD_TA periods are programmable.

OPERATING MODES

The fundamental operating modes of the SSI 32P4103A. are controlled by the SERVO GATE (SG), READ GATE (RG), and WRITE GATE (WG) input pins. The exclusive assertion of any these inputs causes the device to enter that mode. If none of these inputs is asserted, the device is in idle mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The overriding mode takes effect immediately.

RG and SG are asynchronous inputs and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to flushing data through the encode and write precompensation circuits. A minimum of 6 bytes is required to flush these circuits.

Idle Mode Operation

If SG, RG, and WG are not active, the SSI 32P4103A is in idle mode. In idle mode, the time base generator (TBG) and the data separator PLL are running, and the data separator PLL is phase-frequency locked to the TBG output. The AGC, continuous time filter, and pulse qualifiers are active, but the outputs of the pulse qualifiers are disabled. The continuous time filter uses the programmed values in the data mode Registers (FC, FB) for cutoff frequency and boost. The AGC operation is the same as in the VCO preamble portion of a data read.

Servo Mode Operation

If SG is high, the device is in the servo mode. This mode is the same as idle except that the filter cutoff and boost settings are switched from the data mode Registers to the servo mode Registers (FCS, FBS), the AGC is switched to servo mode, and the $\overline{\text{RDS}}$ and PPOL and outputs are enabled. The assertion of SG causes read mode, write mode, and the Power Down Register settings for the front end to be overridden.

Write Mode Operation

The SSI 32P4103A supports three different write modes; normal write mode, direct write mode 1 and direct write mode 2. The direct write modes require that either the DWDR bit in the CM1 Register, or the $\overline{\text{DWR}}$ pin be active. All three write modes require that the data separator be powered on.

The WG pin operation can be inverted by setting the WGP bit in the CM1 Register. When CM1:WGP is low, WG is active high. When CM:WGP is high, WG is active low. Throughout this specification, WG is referred to as active high.

Normal Write Mode

The SSI 32P4103A. is in the normal write mode if WG is high, $\overline{\text{DWR}}$ is high, and the DWDR bit in the CM1 Register is low. A minimum of one NRZ byte (RCLK) time period must elapse after RG goes low before WG can be set high. The data separator PLL is phase-frequency locked to the TBG VCO output (FOUT) in this mode.

In normal write mode, the circuit first auto generates the VCO sync pattern, training patterns and sync bytes, and finally scrambles the incoming NRZ data from the controller, encodes it into 16/17 GCR formatted data, precodes it, precompensates it, feeds it to a write data toggle flip-flop, and outputs it to the preamp for storage on the disk. The write data flip-flop is reset when WG goes low.

The write data outputs remain active after WG goes low, with the active pull down current reduced by a factor of 7 to save power. Since the write data flip-flop is reset when WG goes low, the WD outputs go to a zero state when WG is low.

Direct Write Mode 1

In this mode, the RCLK period is changed from 17/2 FOUT clock periods to 8 FOUT clock periods, with a 4/4 duty cycle. NRZ data from the byte-wide interface bypasses the input latch, the scrambler, and the 16/17 encoder, and is latched directly into the parallel to serial shift register. The serial data bypasses the precoder, but is precompensated before going to the write data flip-flop and then to the WD/$\overline{\text{WD}}$ output pins. The NRZ input data may be changed, provided that the controller outputs data no later than 12 ns after the falling edge of RCLK. Operation with changing NRZ data is only guaranteed up to a maximum user data rate of 240 Mbit/s . Direct write mode #1 is entered by setting CM1:DWDR.

Direct Write Mode 2

In this direct write mode, the input at the DWI/$\overline{\text{DWI}}$ pins directly toggles the write data flip-flop which drives the WD/$\overline{\text{WD}}$ output pins. No WCLK is required in this mode, and the WD/$\overline{\text{WD}}$ output is not resynchronized. Direct write mode #2 is entered by driving the $\overline{\text{DWR}}$ input low.

Data Read Mode Operation

Data read mode is initiated by setting the Read Gate (RG) input pin high. This action causes the data synchronizer to begin acquisition of the clock from the incoming VCO sync pattern. To achieve this, the data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the sample clock. This PLL is normally locked to the time base generator output, but when Read Gate input (RG) goes high, the PLL's reference input is switched to the filtered incoming read signal.

A minimum of 8 pad bytes should be written to the disk to flush the read mode circuits.

DESCRIPTION OF OPERATING MODES (continued)

Direct Read Mode

The SSI 32P4103A supports direct read mode. In this mode, the RCLK period is set to 8 FOUT periods with a 4/4 duty cycle. A direct read operation is initiated in the same manner as a normal read. At assertion of RG, the DSVCO starts tracking the VCO sync pattern and the SFC counter starts counting incoming '1's. The direct read process continues analogous to the normal read up to the sync byte detect sequence. The sync byte detect sequence is the same. The same 9 LSB bits of the 12335h(SB1) or 12343h(SB2) is detected to determine the byte boundaries and initiate the read operation.

After sync byte detection, the direct read is unique from that point in that data is converted to 8-bit parallel (byte) data and passed directly to the NRZ output pins. No decoding is performed, and no de-scrambling.

This mode is enabled by asserting RG with the DWDR bit (CM1:bit0) set.

Force Frame Mode

In read mode, if a defect occurs around the sync byte in such a way that the device can not detect the sync byte, then there is no way to recover the data in that sector. Force frame mode is a method to attempt to recover the data even without being able detect the sync byte. This is done by setting the read recovery mode (RCVRM) MISC1:bits 7:6 to 10b in the serial port. When this occurs, a special read mode is invoked.

In force frame mode, an alternative sync byte detect circuitry is enabled. The read begins as normal. When read gate is asserted, a byte (8 VCO clocks) counter whose value is set by STM2:BYTEDLY is started. When it has counted down to zero it sets an internal Force-Frame-Detect signal (FFrmDET). After FFrmDET goes high, a small three bit counter (T2VCODLY) begins counting VCO/2 clocks. This three bit counter is programmed by setting bits 6,5 and 4 of the STM1 Register. When the T2VCODLY counter has counted down the number of VCO/2 clocks, the sync-byte-detect is forced on the device. The odd or even interleave is chosen by STM1:ODDEVEN. Then, 2-bit data is converted/transferred to the endec properly, the data begins being decoded, de-scrambled (if the register bit is set), and starts coming out the NRZ outputs.

When the correct bit/interleave position is found, the byte out of the NRZ outputs is the 69h sync byte followed by the correct data. From this point on, the scrambler is enabled and the decode process continues normally.

Acquisition of DS VCO Sync

The Read Gate (RG) input can be asserted high, initiating the remainder of the read sequence. When RG is asserted an internal counter begins counting the pulses that are qualified by the dual level pulse qualifier from the polarity changes of the incoming 1,1, -1,-1,1,1 read back pattern defined by the VCO sync field. When the count reaches 4 (4 VCO clocks after RG is asserted), the internal read gate is asserted and the DS PLL input is switched from the TBG VCO output to the sampled data input. This is also the point at which the DS PLL phase detector is switched from the phase-frequency detector to the decision directed phase detector. The counter continues counting until a count value of sync field count (SFC), programmed with SLC:SFC, is reached. When the counter reaches SFC, the data synchronizer PLL is assumed to be locked and settled (VCO lock). Also at SFC, the phase detector gain switch and the AGC mode switch occur. To allow for different preamble lengths, SFC can be set to 16, 32, 48, 64, 80, 96 or 128 from the SLC Register. These values for SFC may be thought of as the number of code clock periods in the sync field, but they actually represent twice the number of incoming polarity changes required.

VCO Lock, PD Gain, AGC Mode Switch, and Code Word Boundary Detector Enable

At SFC, one of two phase tracking methods will be chosen depending on the Enable Phase Detector Gain Switching (GS) bit in the CM1 Register. When the CM1:GS bit is high, the phase detector gain is reduced by a factor of 5 (or 10) after the SFC count is reached. When the CM1:GS bit is low, no phase detector gain switching takes place. MISC2:GS10 sets the gain shift factor of 5 or 10.

Also at SFC, the AGC feedback will be switched from the continuous time full-wave rectifier to sampled data feedback.

At SFC, the DS VCO is assumed locked to the incoming read samples, and an internal VCO LOCK signal is generated. This signal switches the RCLK generator source from the TBG output (FOUT) to the

DS VCO clock. VCO LOCK also enables the sync byte detection circuitry to detect the last 9 of 17-bit word decode boundaries. Both the framing and sync byte detection is done at the same time. These boundaries are defined by SB1 and SB2. RCLK may stop toggling for up to a maximum of 1 RCLK time period during the FOUT to DS VCO switchover. No short duration glitches will occur on RCLK during the switchover.

When the sync byte detection circuitry finds the proper code word boundary, RCLK is resynchronized to guarantee that RCLK is in sync with the 17-bit code words. RCLK may stop toggling for up to a maximum of 2 RCLK time periods during resynchronization. RCLK will not glitch and will not toggle during the resynchronization time. Also at the code word boundary detect, the internal 17-bit code words are allowed to pass to the ENDEC for decoding. Decoding occurs until read gate is deasserted.

Adaptive Equalizer Training Sequence

When SLC:AEE=1, in a normal write sequence, a minimum of 4 bytes consisting of NRZ 91, A0H, 91, A0H followed by two bytes each of 91, B1H (SB1) and 91, 03H (SB2) with programmable (0 to 63) number of 91, A0H sequence must be written between SB1 and SB2. The 91, A0H bytes are 16/17 encoded and precoded during write mode to produce the adaptive equalizer training pattern. During read mode, this sequence is used to adaptively train the transversal filter in a zero forcing manner. The error at the FIR filter output is integrated to derive the inner tap weight multiplying coefficient, Km1. It is anticipated that the continuous time filter will be used for coarse equalization and that transversal filter will be used adaptively for fine tuning. This will reduce Km's range and accuracy requirements. Since there are encoded user data patterns that will not produce an equalizer correction error, an equalization hold during data mode can be selected from the SLC Register. After the training pattern, if the loop is active during data (SLC:AED=1), the equalizer loop gain will be reduced by ≅ 7 if SLC:AEGS = 1. The loop's integration time constant is made inversely proportional to the selected data rate.

If AEQADC = 1, the tap weight will be, at the deassertion of RG, A/D converted and written to the serial port for subsequent readout. The A/D converted word will be reset upon the serial port read.

When AEE = 0, no adaptation of the equalizer will take place. The KM1PS setting in the FIR1 Register will set the equalizer inner taps.

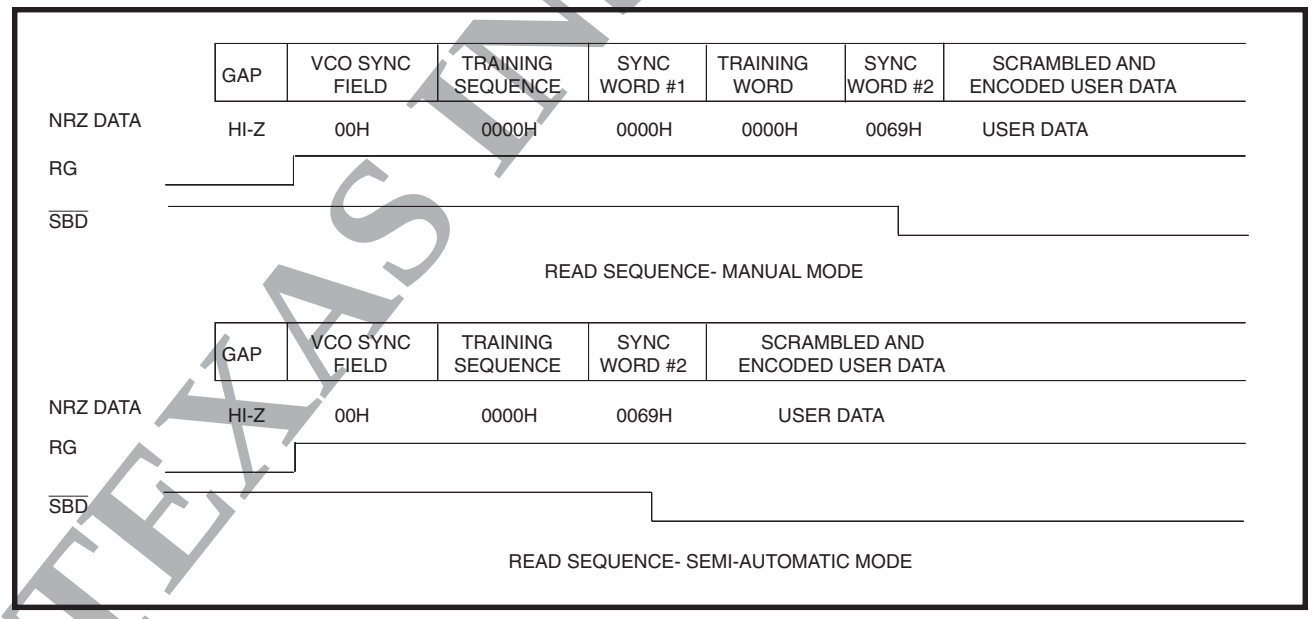


FIGURE 28 : Read Sequence

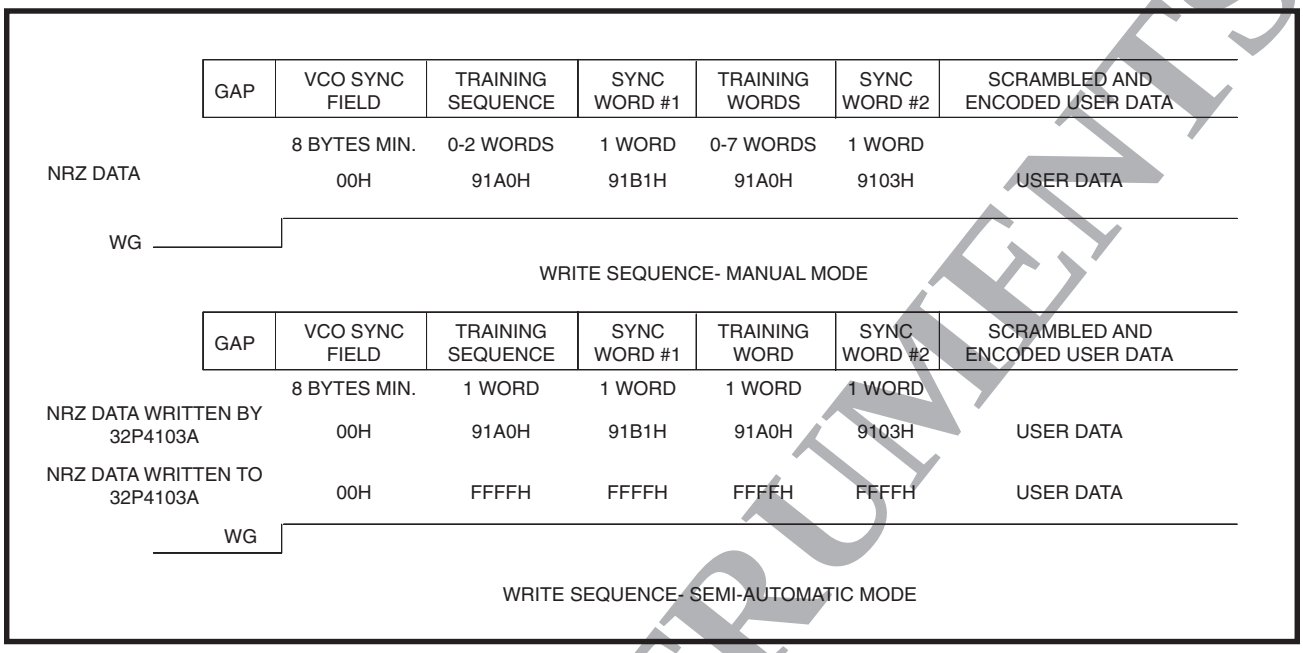


FIGURE 29 : Write Sequence

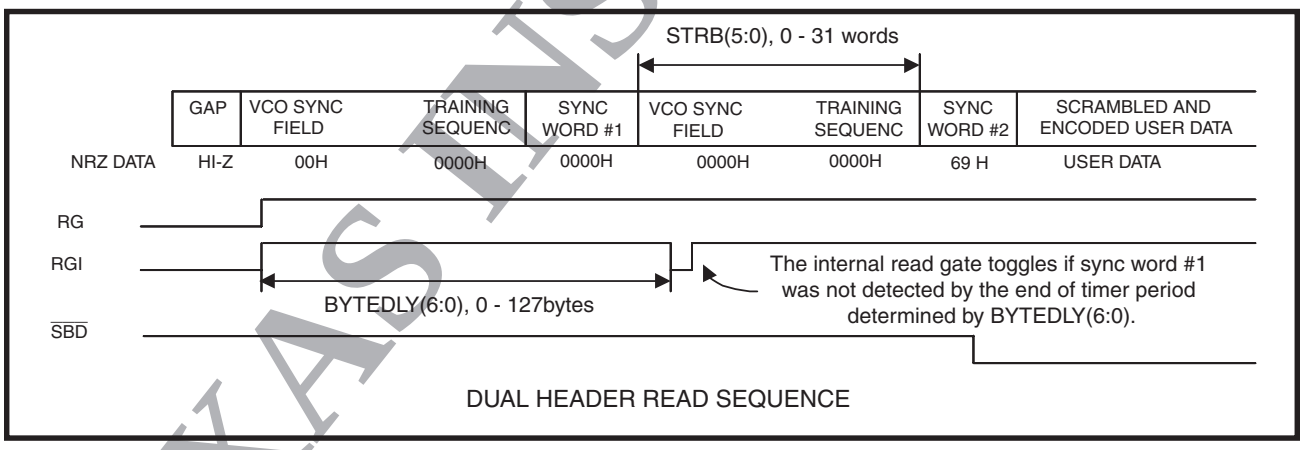


FIGURE 30 : Dual Header Read

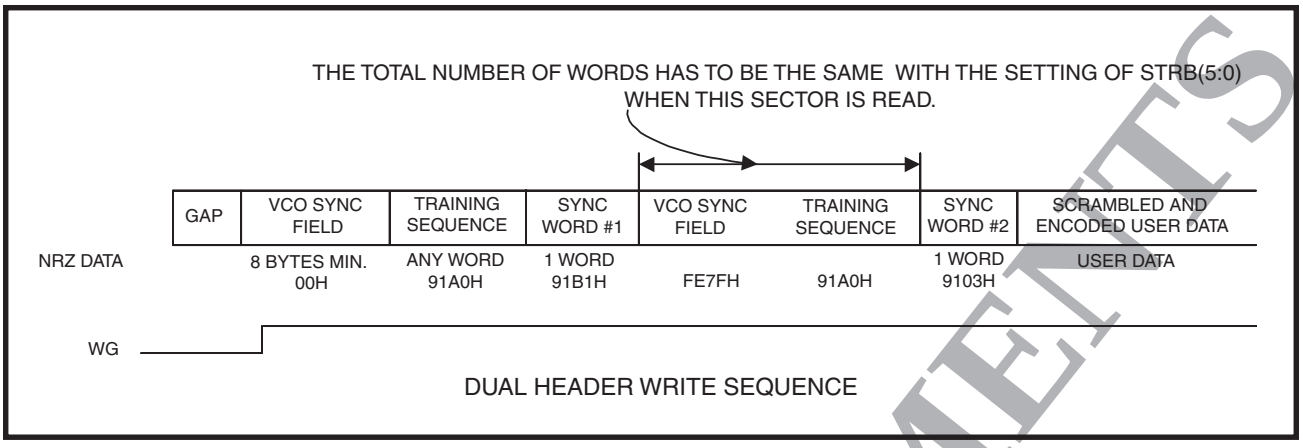


FIGURE 31 : Dual Header Write

OPERATING MODES (continued)

Sync Byte Detect and NRZ Output

The SSI 32P4103A uses a dual sync byte scheme to provide more robust sync byte detection. The sync byte detection circuit looks for either of two sync bytes (SB1 or SB2). There are two operational modes supported in this device: One is the normal dual sync byte mode as depicted in Figure 28 and the other is the Dual Header scheme in Figure 30. The primary purpose of the Dual Header mode is to deal with the event of thermal asperity before the detection of SB1 can occur, and allows recovery from it with the aid of an additional PLL sync field written between two sync words.

In the normal mode, the NRZ outputs are held low before the sync byte output. Detection circuitry for both SB1 and SB2 are simultaneously enabled. When sync byte is detected, the sync byte detect ($\overline{SBD}$) pin goes low and 69h is output at the NRZ interface. If SB1 is detected and SB2 is missed, the $\overline{SBD}$ output will go low 2 bytes + number of pads (programmed between the two sync bytes) later and 69h will be the first non-zero byte output to the NRZ interface. The next byte output on the NRZ interface is the first byte of user data. $\overline{SBD}$ will remain low and user data will continue to be output until RG is deasserted, at which point $\overline{SBD}$ goes high and the NRZ outputs go to a high impedance state. The normal mode is activated by setting MISC1:RCVRM[1:0] = 00.

In the dual header mode, a timer is set off upon the assertion of RG whose duration is programmable via STM2:BYTEDLY[6:0]. If SB1 is not detected within that time period, RG is internally toggled and the detection circuitry for SB2 only (but not SB1) is enabled. This mode is activated by setting MISC1: RCRVM[1:0] = 11.

In both cases it is important that a correct number of words between two sync bytes be entered into CM3:STRB[5:0] bits. It must match the actual number of pads written between the two sync bytes.

POWER DOWN OPERATION

There are two modes of power management available - static and dynamic. The first (static) mode of power management is done via PD Register bits and the second (dynamic) mode by bits 1,2,3,4 of MISC1 Register.

For the static mode the states of the PD Register bits and the $\overline{\text{PDWN}}$ and SG inputs determine the power management. The individual sections of the chip can be powered down or up using the PD Register. A high level in a PD Register bit disables that section of the circuit. The power down information from the PD Register takes effect immediately after the SDEN pin goes low. The truth table for the various operation under static mode is shown below:

TABLE 9: Servo and Power Down Operation Under Static Mode

	SG, $\overline{\text{PDWN}}$			
	1,1	**1,0**	**0,1**	**0,0**
AGC, Filter, Servo	ON	OFF	R	OFF
Data Separator	R	OFF	R	OFF
Time base Generator	R	OFF	R	OFF
Serial Port	ON	ON	ON	ON
R = Controlled by register bit. (Register bit =1 turns circuits OFF, Register bit = 0 turns circuits ON)				

For the dynamic power management of the SSI 32P4103A bits 1, 2, 3, 4 of MISC1 Register are used to dynamically turn on and off various sections of the device, unless inhibited by PD Register bits. Bit 4 of MISC1 Register controls the power management of the front end, such as qualifier, filter differentiated output stage, servo demodulator and sampled data processor. Bit 3 dictates power management associated with the backend - primarily of the write circuitry. Bits 1 and 2 controls how long the servo section is kept powered on after SG goes inactive. Recovery from idle to various mode is fast enough such that it is transparent to the user. The following table shows the power management of the dynamic mode.

When the $\overline{\text{PDWN}}$ input is low, the chip goes into full power down (sleep) mode regardless of the PD or MISC Register settings or the state of the SG input. When $\overline{\text{PDWN}}$ is high, SG will force the AGC, filter, and pulse qualifier circuits (front end) to be active by overriding the PD bit in the PD Register. The back end Power Down Register bits, which include the Data Separator and Timebase Generator are not affected by the SG input.

TABLE 10: Power Management - Dynamic Mode when invoked by MISC1:4,3,2,1

	SG,RG,WG			
	0,0,0	**1,x,x**	**0,1,x**	**0,0,1**
	Idle	**Servo**	**Read**	**Write**
Pd_Qualifier	Off	ON	On till vcolock	Off
Servo Demodulator(MISC:2,1)	Off	ON	Off	Off
SDP except PLL(MISC:4)	Off	Off	On	Off
Write Precomp (MISC:3)	Off	Off	Off	On
All other circuitry	R	R	R	R
R = Controlled by PD Register bits.				

TABLE 11: REGISTER BIT ASSIGNMENT SUMMARY TABLE

Throughout this document, RR:BB refers to bit BB inRegister RR. As an example, PD:TB refers to bit TB inRegister PD.

REG #	REGISTER NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0D7
PD	Power Down	00000100=04h	TPC/D/E[1:0]		ASEL[1:0]		ACSWT	TB<0>	DS<0>	PD<0>
FC	Filter cutoff, data mode	00010100=14h	T_SPC<0>	FC[6:0] Filter cutoff frequency, data mode						
FCS	Filter cutoff, servo mode	00100100=24h	SVCAL	FCS[6:0] Filter cutoff frequency, servo mode						
FB	Filter boost, data mode	00110100=34h	ENTAD	FB[6:0] Filter boost, data mode						
FBS	Filter boost, servo mode, Filter asym. zero adjust	01000100=44h	FBS[1:0] Filter boost, servo mode		FGD[5:0] Filter asymmetric zero adjust					
EPR4	EPR4 Detector Conts Reg	01010100=54h	EPR4 Constant (-1.5) <0000>				EPR4 Constant (+0.5) <0000>			
LD	Data level detector Vth Ctrl	01100100=64h	DSCAN <0>	TARGB	LD[5:0] Data level threshold, data mode					
LDS	Data Level Detector Vth, servo mode	01110100=74h	SAGCL[1:0]		LDS[5:0] Data level threshold, servo mode					
TM1	Test Mode Register 1	10000100=84h	EFR <0>	ECP<0>	TP[3:1] <000>			BYPSR <0>	DT<0>	UT<0>
TM2	Test Mode Register 2	10010100=94h	ACCPLDE <0>	RDTAGC <0>	IOMAP <0>	DIFFBF <0>	ENTRST <0>	SBAND <0>	TSTSL <00>	
N	Time base N counter	10100100=A4h	FREFPS<0>	N[6:0] Time base generator N counter value <19 decimal>						
M	Time base M counter	10110100=B4h	M[7:0] Time base generator M counter value <212 decimal>							
DR	Data rate	11000100=C4	DSB <0>	DR[6:0] Data rate value <109						
WP	Write precomp magnitude	11010100=D4h	WPC2 [3:0] <0000>				WPC1[3:0] <0000>			
SLC	AGC, equalizer sample loop sequence control	11100100=E4h	SFC[2:0] Sync field length			AEGS Equalizer switching <1>	AED Adapt equalizer on data <1>	AEE<0> Adaptive equalizer enable	AGC[1:0] <10> <10> AGC charge pump current	
DRC	Damping ratio control	11110100=F4h	LOWEQG	DRC[6:0] Damping ratio						
FIR1	FIR KM1 Register	00000110=06h	KM1AD[3:0] <Read Only>				KM1PS[3:0] <0000>			
FIR2	FIR KM2 Register	00010110=16h	QaeprEn<1>	QaERP[2:0] Viterbi Mod. DAC <0100>			KM2[3:0] <0100>			
CM1	Mode Control 1	00100110=26h	RCLK2X<0>	AGCT	WGP<0>	TRSQ<0>	BT<0>	SD<0>	GS<0>	DWDR<0>
CM2	Mode Control 2	00110110=36h	<0>LGAIN	<Open>	SBCC[1:0]		PWCTR	PDM	DIBDEN<0>	SERI <0>
CM3	Control Mode Register 3	01000110=46h	FERA <0>	Seed <0>	STRB[5:0] <00000>					
CM4	Control Mode Register 4	01010110=56h	ALE <1>	LEVEL/Qasym TC <00>		FRZQASYM <1>	QalvlEn<1>	QaLVL[2:0] Level Th. Mod. DAC <000>		
TA1	Thermal Asperity 1	01100110=66h	TADE	TAIO <0>	TAIDLE	TARG	AGCHE <0>	PLLGS <0>	PLLHE[1:0] <00>	
TA2	Thermal Asperity 2	01110110=76h	HYED <0>	HYES [1:0] <00>		SVHY <0>	TATH [3:0] <1111>]			

TABLE 11: REGISTER BIT ASSIGNMENT SUMMARY TABLE

Throughout this document, RR:BB refers to bit BB inRegister RR. As an example, PD:TB refers to bit TB inRegister PD.

REG #	REGISTER NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
TA3	Thermal Asperity 3	10000110=86h	HYTMR[1:0] <00>		YIN [2:0] <111>			TATMR [2:0] <110>		
BLO	Base Line Offset	10010110=96h	RDSMUX	SOC <0>	BOSP <0>	SBO[4:0] <00000>				
DBT	Dibit	10100110=A6h	DBT[2:0] (Dibit Enable Time) <000>			SSI Test Mode <00000>				
CQM1	Channel Quality Monitor Register 1	10110110=B6h	CQMQ[15:8](ReadOnly)							
CQM2	Channel Quality Monitor Register 2	11000110=C6h	CQMQ[7:0](ReadOnly)							
CQM3	Channel Quality Monitor Register 3	11010110=D6h	SGBTMR	PLSEN	CQMRGT <00> <0>		SURVSEL <0>	CQMCTRL/SURVSTA <000>		
TC	Time Control Register	11100110=E6h	UFDC [1:0] <10>		LZT [2:0] <100>			FRT [2:0]<100>		
TCS	Time Control Register for Servo	11110110=F6h	LZCTR	UFDSEL	LZT [2:0]<100>			FRT [2:0]<100>		
STM1	Special Test Register 1	00001000=08h	ODDEVEN <0>	T2VCODLY[2:0] <000>			FRCSUR <0>	TSURV <0>	MET07R <0>	CNSTENB <0>
STM2	Special Test Register 2	00011000=18h	DIBITPOL	BYTEDLY[6:0] <0000000>						
BLOD	Base Line Offset - Data	00101000=28h	BOSDP <0>	BLOSD[6:0]						
BLOS	Base Line Offset - Servo	00111000=38h	BOSSP <0>	BLOSS[6:0]						
MISC1	Misc. Register 1	01001000=48h	RCVRM[1:0] <00>		RPMEb <0> EPR4 Read Power Managmnt	RPMSb <0> SDP Read Power Managmnt	WPMb <0> Write Power Managemnt	SVPMb <00> Servo Power Management		FOSNUL <0>
MISC2	Misc. Register 2	01011000=58h	PSP1<0>	PSP2<0>	PSP3<0>	YINS[2:0]			GS10	FDFLOWZ
ZPR	Zero Phase Restart	01101000 = 68h	AEQADC <0>	Test ZPR <0>	POL Read Only	ZPRDAC[4:0]				
ID_SM	ID (Read Only)	11111000=F8h	ID_SM [7:0]							

Note: <0000 0000> is the default 8-bit values for the register. Register address is in 8-bit (1 byte) designation.

REGISTER DESCRIPTIONS

SERIAL PORT REGISTER DEFINITIONS

Throughout the specification, the notation RR:BB is used, where RR is the register, and BB is the bit in the register. For example, PD:DS denotes the DS bit in the PD Register. Addresses are shown MSB first.

Power Down (PD)
Address = 0000 0100 = 04h

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7 - 6</td><td>TPC/D/E/H[1:0]</td><td>
TPC/TPD Control:
<table>
<tr><th>FC:T_SPC</th><th>SG</th><th>PD[7:6]</th><th>TPC/$\overline{TPC}$</th><th>TPD/$\overline{TPD}$</th><th>TPH/$\overline{TPH}$</th></tr>
<tr><td>0</td><td>0</td><td>XX</td><td>Disabled</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>1X</td><td>(Dp/Dn)out</td><td>(Cp/Cn)out</td><td>(DpDn)blos.out</td></tr>
<tr><td>0</td><td>1</td><td>0X</td><td>Disabled</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>1</td><td>X</td><td>00</td><td>Disabled</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>1</td><td>X</td><td>01</td><td>(Dp/Dn)in</td><td>(Cp/Cn)in</td><td>(DpDn)blos.out</td></tr>
<tr><td>1</td><td>X</td><td>10</td><td>(Dp/Dn)out</td><td>(Cp/Cn)out</td><td>(Dp/Dn)blos out</td></tr>
<tr><td>1</td><td>X</td><td>11</td><td>(AGC)out</td><td>(AGC)out</td><td>Disabled</td></tr>
</table>
TPE Control:
<table>
<tr><th>FC:T_SPC</th><th>CM1:AGCT</th><th>HYED</th><th>AGCHE</th><th>PD[7:6]</th><th>TPE/$\overline{TPE}$</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>X</td><td>XX</td><td>Disabled</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>X</td><td>00</td><td>Disabled</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>X</td><td>01,10,11</td><td>Disabled</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>X</td><td>01</td><td>FLOW_Z</td></tr>
<tr><td></td><td></td><td></td><td></td><td>10</td><td>$\overline{FDCO}$</td></tr>
<tr><td></td><td></td><td></td><td></td><td>11</td><td>$\overline{UFDC}$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>01,10,11</td><td>Hi-Y</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>01,10,11</td><td>AGCHOLD_TA</td></tr>
</table>
Note: Dp/Dn = Normal filter
Cp/Cn = Differentiated filter
(AGC) out = Filter bypassed
</td></tr>
<tr><td>5 - 4</td><td>ASEL[1:0]</td><td>Output select for ATO test point
00 = ATO Buffer shut down
01 = DAC Output enabled
10 = Amplitude asymmetry factor enabled
11 = Reference voltage (~MAXREF/2)</td></tr>
<tr><td>3</td><td>ACSWT</td><td>Internal ac coupler switch over at vcolock:
0 = Enables switch over to sampled data mode at vcolock
1 = Always in continuous mode</td></tr>
<tr><td>2</td><td>TB</td><td>Time base generator power down</td></tr>
<tr><td>1</td><td>DS</td><td>Data separator power down</td></tr>
<tr><td>0</td><td>PD</td><td>AGC, Filter, pulse detector, and servo power down</td></tr>
</table>

Bits 2 - 0: 1 = power down; 0 = power up

Data Filter Cutoff Register (FC)
Address = 0001 0100 = 14h

BIT	NAME	DESCRIPTION
7	T_SPC	Controls test points as shown in PD register definition
6 - 0	FC[6:0]	Filter cutoff frequency in non-servo mode $44 \leq FC \leq 127_{dec}$ Filter cutoff frequency = 1.0022 + 0.4959 • FC_DAC

Servo Filter Cutoff Register (FCS)
Address = 0010 0100 = 24h

7	SVCAL	Servo calibration mode: 0 = No calibration 1 = Calibration enabled
6 - 0	FCS[6:0]	Filter cutoff frequency in servo mode $18 \leq FCS \leq 43_{dec}$ Servo filter cutoff frequency = 1.0022 + 0.4959 • FCS_DAC

Data Mode Filter Boost Register (FCS)
Address = 0011 0100 = 34h

7	ENTAD	Enable thermal asperity detection 0 = Disable 1 = Enable
6 - 0	FB[6:0]	Filter boost setting in non-servo mode $0 \leq FB \leq 127$ dec Boost (dB) = 20 • Log(0.04345 • FB - 0.0000337 • FB • FC +1)

Filter Asymmetric Zero and Servo Mode Filter Boost Register (FBS)
Address = 0100 0100 = 44h

7 - 6	FBS[1:0]	Filter boost setting in servo mode, $0 \leq FBS \leq 3_{dec}$
5	FGDP	Filter group delay equalization polarity: 0 = Negative 1 = Positive
4 - 0	FGD[4:0]	Filter group delay equalization magnitude Group delay Δ% = 0.9783 • FGD4:0 - 0.665

EPR4 Detector Constant Register (VEPR4)
Address = 0101 0100 = 54h

7 - 4	“-1.5” Constant	0000 - Nominal Value = -1.5 in 2.5% increments (2’s compliment) 0111 = -1.5 • (1.0 + 7 • 2.5%) = - 1.7625 1000 = -1.5 • (1.0 - 8 • 2.5%) = - 1.2000
3 - 0	“+0.5” Constant	0000 - Nominal Value = +0.5 in 2.5% increments (2’s compliment 0111 = +0.5 • (1.0 + 7 • 2.5%) = 0.5875 1000 = +0.5 • (1.0 - 8 • 2.5%) = 0.4000

REGISTER DESCRIPTIONS (continued)

Data Level Threshold Register (LD)
Address = 0110 0100 = 64h

BIT	NAME	DESCRIPTION
7	DSCAN	When in read, defect scan enable 1 = FIR output is sliced and decisions mixed into the output of the survival register. Any dropout is detected and flagged by the NRZ7 pin in read mode. 0 = Normal operation when in write 0 = Normal 1 = “0” fed to precoder until valid pattern; forces the precoder to a known state, i.e., no write data till training.
6	TARGB	Data AGC hold from RGB to SFC 0 = Normal 1 = Data AGC held from the falling edge of RG to SFC of the next read
5 - 0	LD[5:0]	Data level qualification threshold voltage CM4: ALE = 0 (Fixed levels) Lth = 10.7996 • LD + 4.8604 [mV] before SFC Lth = 7.636 • LD + 3.4368 $16 \leq LD \leq 48$ dec after SFCC M4:ALE = 1 (Adaptive levels) after SFC Lth(%) = 1.574 • LD

Servo Level Threshold Register (LDS)
Address = 0111 0100 = 74h

7 - 6	SAGCL[1:0]	Servo mode AGC level control 00 = 1.40 Vppd 01 = 1.30 Vppd 10 = 1.20 Vppd 11 = 1.10 Vppd
5 - 0	LDS[5:0]	Servo level qualification threshold voltage LSth = 10.1316 • LDS + 12.6516 [mV]

Test Mode Register 1 (TM1)
Address = 1000 0100= 84h

BIT	NAME	DESCRIPTION				
7	EFR	Sample clock source: 0 = Sample clock is from the DS VCO, normal operation 1 = Sample clock is from the TBG output, a test mode				
6	ECP	0 = Normal 1 = Enable charge pump test				
5-3	TP[3:1]	Multiplexed test point selection				
		Function	**TPA, $\overline{\text{TPA}}$**	**TPB, $\overline{\text{TPB}}$**	**TPF, $\overline{\text{TPF}}$**	**TPG, $\overline{\text{TPG}}$**
	0 0 0	Test Points Off	high impedance	high impedance	high impedance	high impedance
	0 0 1	1+D EPR4 samples	(1+D) Phase 1	(1+D) Phase 0	high impedance	high impedance
	0 1 0	PR4 Eq.,Veq and PhDet	FIR Phase 0	FIR Phase 0	Equalizer Control (KM1)	Phase Detect Out
	0 1 1	PR4 Eq., VCO/2 or TBG	FIR Phase 0	FIR Phase 0	DS VCO/2 if RG=1 TBG Fout if RG=0	Phase Detect out
	1 0 0	SURVout, Max Decsn	SURVout before XOR	SURVout	Maximum Metric Decision MSB, 2nd MSB ,LSB, Hi_Z	
	1 0 1	Metric Outputs	Met0, Met1	Met2,Met3	Met4,Met5	Met6,Met7
	1 1 0	Met.Out & Max.Decsn	Met0, Met1	Met2,Met3	Maximum Metric Decision MSB, 2nd MSB ,LSB Hi_Z	
	1 1 1	Met.Out	Met0, Met1	Met2,Met3	high impedance	high impedance
2	BYPSR	Bypass survival path register 0 = Normal; 1 = Bypass during read 0 = Normal; 1 = Bypass precoder during write				
1	DT	1 = TBG Phase detector pump down continuous pump down, for test use only: FLTR1 sinks current; $\overline{\text{FLTR1}}$ sources current 0 = Normal operating mode				
0	UT	1 = TBG Phase detector pump up continuous pump up, for test use onlyFLTR1 sources current; $\overline{\text{FLTR1}}$ sinks current 0 = Normal operating mode				

REGISTER DESCRIPTIONS (continued)

Test Mode Register 2 (TM2)
Address = 1001 0100= 94h

BIT	NAME	DESCRIPTION
7	ACCPLDE	AC Coupler disable: 0 = Normal, 1 = Disabled only for test.
6	RDTAGC	Enable VRDT MUX input and fix AGC gain at 24 dB 0 = Normal 1 = Mux VRDT input to decoder and Fix AGC gain at 24 dB
5	IOMAP	I/O Mapping 0 = Disable 1 = Enable
4	DIFFBF	Bypass TBG using high speed pecl differential buffer 0 = Disable ; 1 = Enable bypass
3	ENTRST	Enable the re-synchronization of internal RCLK by the rising edge of RG for read mode and WG for write mode.The write data pattern stream always begins at the same position from the rising edge of write gate. 0 = Disable;1 = Enable
2	SBAND	Dual 'AND' type sync byte detection. Sync byte is occurred when both sync bytes (91B1H & 9103H) is correctly detected. 0 = Normal operation (Dual 'OR' type detection), Default 1 = Enable dual 'AND' type detection. (TEST mode)
1 - 0	TSTSL[1:0]	ENDEC Internal signals can be monitored from NRZP pin by set of these control bits. 00 = PARITY output (default) 01 = Framing detect (& Sync. byte detect) signal from DIF. 10 = VCOLKDb 11 = EFLAG.

N Counter Register (N)
Address = 1010 0010 = A4h

7	FREFPS	0 = No fref prescaling normal operation 1 = Fref divided by 2 for internal AGC timings, intended for use when Fref > 25MHz
6 - 0	N[6:0]	N Counter: $2 \le N \le 127$

M Counter Register (M)
Address = 1011 0100 = B4h

7 - 0	M[7:0]	M Counter: $2 \le M \le 255$, $F_{TBG} = FREF \bullet \left[\frac{M + 1}{N + 1}\right]$

Data Rate Register (DR)
Address = 1100 0100 = C4h

BIT	NAME	DESCRIPTION
7	DSB	NRZ Flag at start of defect scan mode 0 = Normal operation 1 = Toggle NRZ1 for one RCLK time period to indicate beginning of defect scan mode at SFC
6 - 0	DR[6:0]	Data rate DAC value. $0 \leq DR \leq 127$ F_{vco} (MHz) = 17/16 Data Rate F_{vco} (MHz) = 9.1339 + 2.4151 • DR_DAC

Write Precomp Register (WP)
Address = 1101 0100 = D4h

7 - 4	WPC2[3:0]	Level 2 write precomp magnitude 0 -17% in linear increments; 0000 implies no Level 2 precompensation
3 - 0	WPC1[3:0]	Level 1 write precomp magnitude 0 - 34% in linear increments; Level 1 must be greater than or equal to Level 2

Sample Loop Control Register (SLC)
Address = 1110 0100 = E4h

7 - 5	SFC[1:0]	Sync field count -actual length of synch field must be greater than SFC specified here by at least one byte SFC Sync Field Count 000 16 001 32 010 48 011 64 100 80 101 96 110 112 111 128
4	AEGS	Adaptive equalizer loop time constant shift 0 = Equalizer loop time constant is the same in preamble and data fields 1 = Equalizer loop time constant is increased by ≅ 7X in the data field relative to the preamble field, i.e. loop gain is reduced to ≅ 1/7
3	AED	Enable adaptive equalizer on data field (Only valid if AEE bit = 1) 1 = Adaptive equalizer in use after sync byte detect 0 = Adaptive equalizer disabled after sync byte detect

Sample Loop Control Register (SLC) (continued)
Address = 1110 0100 = E4h

BIT	NAME	DESCRIPTION
2	AEE	Enable adaptive equalizer 1 = Adaptive equalizer enabled for use in preamble field, and after the preamble field if AED bit = 1 0 = Adaptive equalizer disabled
1 - 0	AGC[1:0]	AGC Charge pump current in sampled AGC mode AGC Charge pump current = $\pm 2.66 \cdot 10^{-6} \cdot AGC \cdot DR/RR$

Damping Ratio Control Register (DRC)
Address = 1111 0100 = F4h

7	LOQEQG	Force low equalizer gain 0 = Normal 1 = Equalizer adaptation gain always low (i.e., 7x time constant)
6 - 0	DRC6:0]	Damping amplifier gain A = DRC • (0.7/127) Damping ratio = $\frac{A \cdot KVCO \cdot 0.25}{2\,\omega_n}$

FIR TAP Coefficient Register 1 (FIR1)
Address = 0000 0110 = 06h

7 - 4	Km1AD[3:0]	A/D Converted Km1 values made available at the end of A/D conversion; reset after the serial port read.
3 - 0	Km1PS[3:0]	Km1 Preset: (default <0100>)If AEE = 0, Km1 is forced into the equalizer as a fixed weight; Only negative gain settings are allowed. 0000 = Tap gain is nominally zero 1111 = Largest negative gain. If AEE = 1, Km1 setting is used as a starting point for adaptation.

FIR TAP Coefficient Register 2 (FIR2)
Address = 0001 0110 = 16h

7	QaeprEN	0 = No amplitude asym. correction on EPR4 Viterbi 1 = Correction as defined in QaEPR[2:0] Dac below
6 - 4	QaEPR[2:0]	Asym. correction amount of EPR4 Viterbi detector in 12.5% increment (2's compliment) 011 = Nominal • (1+ 3 • 12.5%) = 1.375 • nominal 000 = Nominal correction factor 100 = Nominal • (1- 5 • 12.5%) = 0.500 • nominal
3 - 0	Km2[3:0]	Equalizer outer tap multiplier gain (default <0100>) Km2 = 0.01875 • Km2, where Km2 is in 2's compliment. Gain range is -0.15 to +0.13125 with resolution of 0.01875.

Mode Control 1 Register (CM1)
Address = 0010 0110 = 26h

BIT	NAME	DESCRIPTION
7	RCK2X	0 = Rclk drive at 1x 1 = Rclk drive at 2x
6	AGCT	AGC Timing control (default <0>) 0: AGC Timing externally generated 1: AGC Timing internally generated
5	WGP	Write gate polarity. 1 = Inverted ($\overline{WG}$); 0 = Noninverted (WG)
4	TRSQ	Training sequence generation control 0: Training sequence and sync byte generated externally 1: Training sequence and sync byte generated internally, STRB(2:0) must be 001.
3	BT	Bypass time base generator 1 = Data synchronizer reference frequency is FREF input 0 = Data synchronizer reference frequency is TBG output
2	SD	Scrambler disable 1 = Disabled 0 = Enabled
1	GS	DS Phase detector gain switching 1 = Disabled (gain stays high after SFC) 0 = Enabled
0	DWDR	Enable direct write from byte-wide NRZ 1 = Enabled 0 = Disabled Also if in read mode 1 = Enable direct read mode(bypass decoder, descrambler) 0 = Disabled.

Mode Control 2 Register (CM2)
Address = 0011 0110 = 36h

7	LGAIN	0 = Normal 1 = Force DSPLL into low gain mode (no gear shift)
6		Factory reserved bits must set to 0.
5 - 4	SBCC[1:0]	Initial servo current SBCC Initial Current (µA) 00 40 01 80 10 120 11 160
3	PWCTR	$\overline{RDS}$ Output pulse width. 0 = 15 ns; 1 = 27 ns
2	PDM	Pulse detector mode 1 = Hysteresis qualifier 0 = Window qualifier

Mode Control 2 Register (CM2) (continued)
Address = 0011 0110 = 36h

BIT	NAME	DESCRIPTION
1	Dibit Detect Enable	0 = Disabled 1 = Enabled
0	SERI	Servo input and RDS output polarity control 0: Normal filter outputs routed to servo; $\overline{RDS}$ - active low 1: Differentiated filter outputs routed to servo; RDS - active high

Mode Control 3 Register (CM3)
Address = 0100 0110 = 46h

7	FERA	Enable/force illegal pattern detection/error flag even without thermal asperity detect. 0 = Disable 1 = Force illegal pattern detection, even if thermal asperity detect is not present
6	SEED	0 = Scrambler seed is 3FFh 1 = Scrambler seed is 2AAh
5 - 0	STRB[5:0]	Set the number of 17bit long pads between two sync bytes. In Write mode, STRB[5:0]h of pads should be written between two sync bytes. No pad is written between two sync bytes when STRB[5:0] = 0.

Mode Control 4 Register (CM4)
Address = 0101 0110 = 56h

7	ALE	Enable adaptive level qualification in decision directed phase detector 0 = Always use fixed level qualification 1 = Switch to adaptive mode at vcolock
6 - 5	TC[2:1]	Adaptive level qualification threshold time constant for decision directed phase detector and qasym factor time constant (both valid After SFC): TC2 TC1 Time Constant 0 0 150 ns 0 1 300 ns 1 0 450 ns 1 1 600 ns
4	FRZQASYM	Freeze qasym acquisition at SFC
3	QalvlEN	0 = No amplitude asym correction on level threshold or 3-level slicer 1 = Correction as defined in QaLVL[2:0] DAC below
2 - 0	QaLVL[2:0]	Asym. correction amount of level threshold in 12.5% increment (2's compliment) 011 = Nominal • (1+ 3 • 12.5%) = 1.375 • nominal 000 = Nominal correction factor 100 = Nominal • (1- 4 • 12.5%) = 0.500 • nominal

Thermal Asperity Register 1 (TA1)
Address = 0110 0110 = 66h

BIT	NAME	DESCRIPTION
7	TADE	Enable TA detect when RG or SG is high 0 = TAD is enabled only when RG or SG is high 1 = TAD is enabled and always ready
6	TAIO	Thermal asperity detect (TAD) pin input/output select 0 = Internal TAD output 1 = External TAD input
5	TAIDLE	Thermal asperity idle mode control 0 = No TA detection or suppression in idle mode 1 = TA Detection and suppression in idle mode
4	TARG	Thermal asperity detection and suppression between RG and RGB 0 = TA Detection and suppression from SFC to falling RG. 1 = TA Detection and suppression from rising RG to falling RG
3	AGCHE	AGC and AC_Coupler Hold Enable: 0 = Normal operation 1 = Hold AGC gain and AC_Coupler over thermal asperity
2	TAPLLGS	Control gear shift in TA event: 0 = Normal operation 1 = Gearshift PLL over thermal asperity
1 - 0	PLLHE[1:0]	PLL Hold control: 00 = Normal operation 01 = Hold PLL over thermal asperity 10 = Hold PLL during TAD 11 = Deassert internal PLLHOLD signal by the falling edge of internal ERROR FLAG

Thermal Asperity Register 2 (TA2)
Address = 0111 0110 = 76h

7	HYED	Hi-Y Enable, dynamic mode 0 = Disable Hi-Y over thermal asperity detect 1 = Invoke Hi-Y as defined by HYTMR, when RG = 1 and thermal asperity is detected (on-the-fly mode)
6 - 5	HYES[1:0]	Hi-Y Enable, static mode 00 = Normal operation (No activation of Hi-Y) 01 = Invoke Hi-Y when SG = L (retry mode) 10 = Invoke Hi-Y when SG = H (retry mode) 11 = Invoke Hi-Y.
4	SVHY	Hi-Y In servo mode 0 = De-activate Hi-Y on TA detect in servo mode 1 = Activate Hi-Y on TA detect in servo mode as defined in HYTMR
3 - 0	TATH[3:0]	Thermal asperity threshold voltage control: threshold voltage (mV) = 50 • TATH + 750 $0 \le TATH \le 15$

REGISTER DESCRIPTIONS (continued)

Thermal Asperity Register 3 (TA3)
Address = 1000 0110 = 86h

BIT	NAME	DESCRIPTION
7 - 6	HYTMR[1:0]	Hi-Y Period = 0.959 • HYTMR + 0.927 µs
5 - 3	YIN[2:0]	Dynamic high admittance control in non-servo mode (SG = Low). Yin (Siemens) = 1/724 + YIN/2520 + 1/10k, $0 \le YIN \le 7$
2 - 0	TATMR[2:0]	PLL/AGC Hold time duration during thermal asperity T_{hold} (µs) = 0.158 + 0.117 • TATMR, $0 \le TATMR \le 7$

Base Line Offset Register (BLO)
Address = 1001 0110 = 96h

7	RDSMUX	TAD, EFLAG Mux'd onto RDS, PPOL pins 0 = Mux TAD and EFLAG onto RDS and PPOL pins when SG = 0 1 = Use TAD and NRZP pins only,
6	SOC	Servo offset control from SBO 0 = Qualifier only 1 = Demodulator and qualifier
5	BOSP	Baseline offset polarity: 0 = Negative 1 = Positive
4 - 0	SBO [4:0]	Database line offset BOSP controls polarity differential offset = 4 • SBO [4:0] (mV)

Dibit Detector Time Constant (DBT)
Address = 1010 0110 = A6h

7 - 5	Dibit Enable Time DBT[2:0]	DBT[2:0]	Ret.OS.Pulse.Width	Implied Frequency
		000	42 ns	11.9 MHZ
		001	80 ns	6.25 MHZ
		010	120 ns	4.16 MHZ
		011	160 ns	3.12 MHZ
		100	190 ns	2.63 MHZ
		101	220 ns	2.27 MHZ
		110	245 ns	2.04 MHZ
		111	280 ns	1.79 MHZ
4 - 0	SSI Test Mode			

Channel Quality Monitor Register 1 (CQM1)
Address = 10110110 = B6h

BIT	NAME	DESCRIPTION
7 - 0	CQMQ[15:8]	Channel quality monitor counter (MSB 8 bits) read only bits. reading this register initilizes internal CQM counter.

Channel Quality Monitor Register 2 (CQM2)
Address = 11000110 = C6h

7-0	CQMQ[7:0] Read Only Bits.	Channel quality monitor counter (LSB 8 bits)

Channel Quality Monitor Register 3 (CQM3)
Address = 1101 0110= D6h

7	SGBTMR	0 = Normal 1 = Allows servo timings on the falling edge of SG
6	PLSEN	0 = Normal 1 = Allows servo pulses to come out even during STROBE
5 - 4	CQMRGT	CQM RG Time or SG time (when CQMCTRL = 100) 00 = Accumulate the CQM count over 1 RG (or SG) period 01 = Accumulate the CQM count over 144 RG (or SG) periods 10 = Accumulate the CQM count over 526 RG (or SG) periods 11 = Accumulate the CQM count over 1008 RG(or SG) periods
3	SURVSEL	0 = Normal 1 = Forces the selection of surv. path at its output by SURVSTA below
2 - 0	CQMCTRL/ SURVSTA	When SURVSEL=0; 000 = Disable CQM function, x01 = Counts maxmet inconsistency events in CQM counter, x10 = Counts Maxmet M2SB inconsistency events in CQM counter, x11 = Counts maxmet MSB inconsistency evnets in CQM counter, In the above three cases the counter starts from SBD(x=0) or VCOLOCK (x=1). 100 = CQM input from AGC comparator intended for use in BLOS adjustment

REGISTER DESCRIPTIONS (continued)

Time Control Register (TC)
Address = 1110 0110 = E6h

BIT	NAME	DESCRIPTION
7 - 6	UFDC[1:0]	Enable ultra fast decay current Ultra fast decay current (µA) = 0.72 • UFDC[1:0]
5 - 3	LZT[2:0]	Low-Z time LZT2 LZT1 LZT0 FREF periods 0 0 0 2 0 0 1 3 0 1 0 5 0 1 1 7 1 0 0 10 1 0 1 13 1 1 0 16 1 1 1 20
2 - 0	FRT[2:0]	Fast recovery time FRT2 FRT1 FRT0 FREF periods 0 0 0 4 0 0 1 6 0 1 0 10 0 1 1 14 1 0 0 20 1 0 1 26 1 1 0 32 1 1 1 40

Time Control Register for Servo (TCS)
Address = 1111 0110 = F6h

7	LZTCR	0 = 15 : 1 ratio ; Rindiff = 8.3 Ω : 0.55 Ω at VIA/$\overline{\text{VIA}}$ 1 = 5 : 1 ratio ; Rindiff = 2.7 Ω : 0.55 Ω at VIA/$\overline{\text{VIA}}$
6	UFDSEL	0 = Only during SG high; 1 = Always use ultra fast decay
5 - 3	LZTS[2:0]	Low-Z time in servo mode LZTS2 LZTS1 LZTS0 FREF periods 0 0 0 2 0 0 1 3 0 1 0 5 0 1 1 7 1 0 0 10 1 0 1 13 1 1 0 16 1 1 1 20

Time Control Register for Servo (TCS) (continued)
Address = 1111 0110 = F6h

BIT	NAME	DESCRIPTION
2 - 0	FRTS[2:0]	Fast recovery time in servo mode FRTS2 FRTS1 FRTS0 FREF periods 0 0 0 4 0 0 1 6 0 1 0 10 0 1 1 14 1 0 0 20 1 0 1 26 1 1 0 32 1 1 1 40

Special Test Mode Register 1 (STM1)
Address = 00001000= 08h

7	ODDEVEN	Forced synch byte detection ODD/EVEN control The even or odd order of the force sync. byte can be controlled by this bit. 0 = Detect at EVEN 1 = Detect at ODD.
6 - 4	T2VCODLY	Forced synch byte detection 2Tvco delay count 00 = Disable, Normal The delayed SFC signal (by BYTEDLY[6:0]) is delayed number of T2VCODLY[2:0] (0 to 7) by 2Tvco clock. This in conjunction with the ODDEVEN bit, enables the control of the occurrence of sync.byte detection in the proper 2Tvco period.
3	FRCSUR	When TSURV = 1: 0 = Force survival path register input to zero 1 = Force survival path register input to one
2	TSURV	0 = Normal 1 = Test Survival path register as dictated by FRCSUR bit
1	MET07R	0 = Normal 1 = Resets all metric states except for state “0” and “7” and common mode feedback is derived off “0” and “7” metric states
0	CNSTENB	0 = Normal 1 = EPR4 Metric constants to zero

REGISTER DESCRIPTIONS (continued)

Special Test Mode Register 2 (STM2)
Address = 00011000= 18h

BIT	NAME	DESCRIPTION
7	DIBITPOL	Set the polarity of first transition before dibit detect signal. 0 = Set the first transition to negative. 1 = Set the first transition to positive.
6 - 0	BYTEDLY[6:0]	Forced sync byte detection byte delay count When RCVRM[1:0]=11 AND if SB#1 is NOT detected before the time period given by BYTEDLY[6:0] (0 to 127) byte clocks after the RG assertion expires, RG is internally reasserted and starts looking for SB#2. When RCVRM[1:0]=10, this, in conjunction with T2VCODLY[2:0] bits and ODDEVEN bit, allows precise placement of sync.byte detection.

Base Line Offset - Data Mode- Register (BLOD)
Address = 0010 1000= 28h

7	BOSDP	Baseline offset polarity: 0 = Negative offset 1 = Positive offset
6 - 0	BLOSD[6:0]	Magnitude of offset Blos = 2.5 mV • [6:0], BOSDP = 0 Blos = 2.374 mV • [6:0], BOSDP = 1

Base Line Offset - Servo Mode- Register (BLOS)
Address = 0011 1000= 38h

7	BOSSP	Baseline offset polarity: 0 = Negative offset 1 = Positive offset
6 - 0	BLOSS[6:0]	Magnitude of offset Blos = 2.5 mV • [6:0], BOSSP = 0 Blos = 2.374 mV • [6:0], BOSSP = 1

Misc. Register 1
Address = 0100 1000= 48h

BIT	NAME	DESCRIPTION
7 - 6	RCVRM[1:0]	Read recovery mode: 00 = Normal conventional single header mode. (Default) 01 = Reserved (test mode) 10 = Enable force framing mode 11 = Enable read recovery (dual header) read mode
5	RPMEb	EPR4 Read power management: 0 = on; 1 = off (normal)
4	RPMSb	SDP Read power management: 0 = on; 1 = off (normal)
3	WPMb	Write power management: 0 = on; 1 = off (normal)
2 - 1	SVPMb	Servo power management: 00 = Servo power shutdown 32 fref clock periods after $\overline{SG}$ 01 = Servo power shutdown 64 fref clock periods after $\overline{SG}$ 10 = Servo power shutdown 128 fref clock periods after $\overline{SG}$ 11 = No servo power management (normal)
0	FOSNUL	Enables special fast offset null mode from the falling edge of TAD to the end of HiY period 0 = Disabled 1 = Enabled

Misc. Register 2
Address = 0101 1000= 58h

7	PSP1	Preamp serial port transfer function thru PSDATA, PSCLK, and PSDATA pins: 0 = Normal: allows serial port transfer if SDEN = 1 and RG = WG = SG = 0 1 = Disable serial port transfer (Hi-Z on outputs)
6	PSP2	Preamp serial port output control when disabled. 0 = Tri-state; 1 = Drive low
5	PSP3	Envoke TI mode of serial port transfer (Write) 0 = Normal; 1 = TI mode (See serial port description.)
4 - 2	YINS[2:0]	Dynamic high admittance control in servo mode (SG = High). Yin (Siemens) = YINS/2230 + 1/10,000, $0 \leq YIN \leq 7$
1	GS10	DS PLL Gear shift factor: 0 = 5, 1 = 10
0	FDFLOWZ	Filter fast offset correction (Lowz) time extension in AGC internal timing mode. 0 = LowZ time will extend to the end of FASTREC when AGCT=1. 1 = Normal: LowZ time is until the rising edge of FASTREC

REGISTER DESCRIPTIONS (continued)

ZPR Register
Address = 0101 1000 = 68h

BIT	NAME	DESCRIPTION
7	AEQADC	ADC done at the end of RG for readout at the serial port (when AEQADC = 1, read power management must be disabled, RPM = 1, to be fixed in metal
6	TestZPR	Invokes TestZPR mode 0 = Normal 1 = DSPLL loop is forced open and phase error be accumulated until vcolock time for A/D at the deassertion of RG.
5	POL	Read only; indicates polarity of the accumulated phase error; the remaining 5 bits of the A/D conversion reside in FIR Register.
4 - 0	ZPRDAC [4:0]	The starting point of the ZPR circuit is dictated by these bits; in 2's compliment.

ID_SM ID Register (Read Only)
Address = 1111 1000 = F8h

7 - 0	ID_SM	Chip ID writing DAh resets all registers to default

PIN DESCRIPTIONS

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA		AGC/Filter analog circuit supply
VPF		Time base generator PLL digital circuit supply
VPT		Time base generator analog supply
VPP		Data separator PLL analog circuit supply
VPD		TTL Buffer I/O digital supply
VPC		Internal ECL, CMOS logic digital supply
VPS (x2)		Sampled data processor and EPR4 detector supply
VNA (x2)		AGC/Filter analog circuit ground
VNF		Time base generator PLL digital circuit ground
VNT		Time base generator analog ground
VND		TTL Buffer I/O digital ground
VNC		Internal ECL, CMOS logic digital ground
VNS (x3)		Data separator PLL, sampled data processor and EPR4 detector ground

ANALOG INPUT PINS

VIA, $\overline{\text{VIA}}$		AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins

ANALOG OUTPUT PINS

TPA, $\overline{\text{TPA}}$		TEST PINS: Emitter output test points. Various signals are multiplexed to these test points by the TP bits in the TM1 Register. The signals include the equalizer control voltage and output, various timing loop control signals and the viterbi survival Register outputs. The test points are provided to show how the signal is being processed. Internal “pull down” resistors to ground are provided . To save power when not in test mode, the TP bits must be set to “0”.
TPB, $\overline{\text{TPB}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the other phase of the interleaved signals (set by TM1:TP bits)
TPC, $\overline{\text{TPC}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the normal outputs of the continuous time filter or AGC output. These pins may also be driven with DP/DN like signals for back end testing (set by PD:TPC bits)
TPD,$\overline{\text{TPD}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the differentiated output of the continuous time filter or AGC output. These pins may also be driven with CP/CN like signals for back end testing. (set by PD:TPC bits)
TPE		TEST PINS: Emitter output test point similar to TPA. FWR output when enabled. (set by PD:TPC bits)

ANALOG OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
TPF, $\overline{\text{TPF}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the other phase of the interleaved signals. (set by TM1:TP bits)
TPG, $\overline{\text{TPG}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the other phase of the interleaved signals. (set by TM1:TP bits)
TPH, $\overline{\text{TPH}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the DP/DN signal after the application of base line offset. (set by PD:TPC bits)
ATO		ANALOG TEST OUT: This test point output provides a monitor of the equalizer quality signal, the amplitude asymmetry signal, and the DAC outputs. The selected output is determined by the ASEL bits in the PD Register. If the DAC outputs are selected, the last DAC written to by the serial control Register is the DAC monitored. Signal at ATO is referenced to Vcc/2 or ATO reading at ASEL set to 11. 00 powers down ATO buffer.
A, B, C, D		SERVO OUTPUTS: These outputs are the amplified and offset versions of the voltages captured on the servo hold capacitors. They are offset by an internally generated 0.27 V baseline. In servo calibration mode (FC:T_SPC=1, PD:TPC=0) Vol's + reference voltage ªMaxref/2 are brought to these pins.
MAXREF		SERVO REFERENCE OUTPUT: +3.2 V DC reference voltage that represents the maximum output voltage for the A, B, C, and D outputs. Can be used as the reference for an external A/D converter.

ANALOG CONTROL PINS

BYP		The data AGC integrating capacitor, CBYP, is connected between BYP and VPA. This pin is used in non-servo mode (SG = 0).
BYPS		The servo AGC integrating capacitor, CBYPS, is connected between BYPS and VPA. This pin is used when in servo read mode (SG = 1).
FLTR1, $\overline{\text{FLTR1}}$		TBG PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components.
FLTR2, $\overline{\text{FLTR2}}$		DS PLL LOOP FILTER: Differential connection points for the data separator PLL loop filter capacitor.
RR		CURRENT REFERENCE RESISTOR INPUT: For 240 Mbps. operation an external 8.06 kΩ 1% resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and the time base generator DACs. 8.06 kΩ 1% resistor should be used for 240 Mbps. operation.
RX		FILTER REFERENCE RESISTOR INPUT: An external 10.2 kΩ 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter DACs.
VRC		AGC REFERENCE VOLTAGE: VRC is a bandgap derived reference referred to VPA1.

DIGITAL INPUT PINS

NAME	TYPE	DESCRIPTION
LOWZ		LOW-Z mode INPUT: TTL compatible control pin which, when pulled high, the input impedance is reduced to allow rapid recovery of the input coupling capacitor, the internal AC coupling time constant is reduced to 250 ns, and the AGC gain is squelched. When pulled low, keeps the AGC amplifier and filter input impedance high. An open pin is a logic high.
FASTREC		FAST RECOVERY: TTL compatible control pin which, when pulled high, puts the AGC charge pump in the fast recovery mode. An open pin is a logic high.
$\overline{\text{PDWN}}$		POWER DOWN CONTROL: CMOS compatible power control pin. When set to logic low, the entire chip is in sleep mode with all circuitry, except the serial port, shut down. This pin should be set to logic high in normal operating mode. Selected circuitry can be shut down using the PD Register. There is no default value for this pin.
$\overline{\text{HOLD}}$		AGC HOLD CONTROL INPUT: TTL compatible control pin which, when pulled low, holds the AGC amplifier gain constant by turning off the AGC charge pump. The AGC loop is active when this pin is either at high or open.
EQHOLD		EQUALIZER HOLD CONTROL INPUT: TTL compatible control pin which, when pulled high causes the present adaptive equalizer tap weights to be held until the input is set low. An open pin is at logic high.
FREF		REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an ac coupled ECL signal. When the EFR bit in the CT Register is set, FREF replaces the VCO as the input to the data separator.
WCLK		WRITE CLOCK: TTL compatible input that latches in the data at the selected NRZ interface on the rising edge. Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. An open pin is at logic high.
RG		READ GATE: TTL compatible input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the read mode/address detect sequences. A low level selects the time base generator output. An open pin is at logic high.
WG		WRITE GATE: TTL compatible input that, when pulled high, enables the write mode. An open pin is at logic high.
SG		SERVO GATE: TTL compatible input that, when pulled high, enables the servo read mode. An open pin is at logic high.
VRDT		VITERBI READ DATA: A TTL or ac coupled PECL compatible input to the data separator back end, for testing purposes only. This pin is controlled by the VRDT bit in the CT Register.

DIGITAL INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{DWR}}$		DIRECT WRITE mode 2 ENABLE: Enables DWI, $\overline{\text{DWI}}$ inputs to the write data flip-flop when input is low. TTL levels. Open pin is at logic high.
DWI, $\overline{\text{DWI}}$		DIRECT WRITE INPUTS: Inputs connect to the toggle input of the write data flip-flop when $\overline{\text{DWR}}$ is low. PECL input levels. Can be left open.
BFREF, $\overline{\text{BFREF}}$		BYPASS FREF INPUTS: High speed differential PECL input buffer for use in bypassing the TBG.
STROBE		SERVO STROBE INPUT: Active high enable for charging an individual hold capacitor during a servo burst capture. The falling edge of STROBE will increment an internal counter that determines which of the four hold capacitors will be charged during the next strobe pulse. TTL levels. Open pin is at logic high.
$\overline{\text{RESET}}$		RESET CONTROL INPUT: Active low reset for discharging of the four internal servo burst hold capacitors for channels A, B, C, and D. TTL input levels. Open pin is at logic high.

DIGITAL BI-DIRECTIONAL PINS

NRZ0-7		BYTE WIDE NRZ DATA PORT: TTL compatible bi-directional input / output. Input to the encoder when WG is high. Output from the decoder when RG is high.
NRZP		NRZ DATA PARITY BIT: Active when in Byte Wide mode. TTL compatible bi-directional input / output. Generates even read parity when RG is high, and accepts even write parity when WG is high. Can be left open if not used. Also a multiplexed test point set by TM2:TSTSL
TAD		Thermal Asperity Detect Pin

DIGITAL OUTPUT PINS

RCLK		READ REFERENCE CLOCK: A multiplexed clock source used by the controller, . When RG is low, RCLK is synchronized to the time base generator output, F_{TBG}. When RG goes high, RCLK remains synchronized to F_{TBG} until the SFC is reached. At that time, RCLK is synchronized to the data separator VCO. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. TTL output levels.
$\overline{\text{SBD}}$		SYNC BYTE DETECT: Transitions low upon detection of sync byte. This transition is synchronized to the sync byte. Once it transitions low, $\overline{\text{SBD}}$ remains low until RG goes low, at which point it returns high. CMOS output.
WD, $\overline{\text{WD}}$		WRITE DATA: Write data flip-flop output. The data is automatically re-synchronized (independent of the delay between RCLK and WCLK) to the reference clock F_{TBG}, except in Direct Write mode 2. Differential PECL output levels.

DIGITAL OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{RDS}}$(RDS)		SERVO READ DATA: Read Data Pulse output for servo read data. Active low CMOS output. Output active when SG is high, and high when SG is low.
PPOL		SERVO READ DATA POLARITY: Read Data Pulse polarity output for servo read data. Active high CMOS output. Negative pulse = low, positive pulse = high. Output active when SG is high.
PERR		PARITY ERROR DETECT: Transitions high when a parity error is detected at the byte wide NRZ interface. CMOS output.

SERIAL PORT PINS

SCLK		SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. CMOS input levels.
SDATA		SERIAL DATA: Input/output pin for serial data; 8 address bits first followed by 8 data bits. The address and data bits are entered LSB first, MSB last. CMOS input/output levels.
SDEN		SERIAL DATA ENABLE: A high level input enables data loading. The data is internally parallel latched when this input goes low. CMOS input levels.
PSCLK		SERIAL DATA CLOCK: to preamp: Positive edge triggered clock output for the serial data transfer to preamp. CMOS output levels.
PSDATA		SERIAL DATA to preamp: Input/output pin for serial data; 8 address bits first followed by 8 data bits. The address and data bits are entered LSB first, MSB last. CMOS input/output levels.
PSDEN		SERIAL DATA ENABLE to preamp: A high level output to preamp enables data loading. CMOS input levels.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Positive 5.0 V supply voltage (Vp)	-0.5 to +7 V
Storage temperature	-65 to +150 °C
Solder vapor bath	215 °C, 90 s, 2 times
Junction operating temperature	+135 °C
Output pins	±10 mA
Analog pins	±10 mA
Voltage applied to other pins	-0.3 V to Vp + 0.3 V

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5 V < POSITIVE SUPPLY VOLTAGE < 5.5 V 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

POWER SUPPLY CURRENT AND POWER DISSIPATION

Outputs and test points open for all power tests. Test points disabled (TP bits in CT Register set to zero). Maximum Data rate. VP = 5.0 V RDPWR = WRPWR = 1 is assumed for power management.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ICC (VPn) Typical @ 5.0 V Max @ 5.5 V	Ta = 70 °C RG = 1 Without power management With power management During idle		 362 363 286	 450	 mA
PWR Power dissipation normal operating modes	Ta = 70 °C RG=1 Without power management With power management During idle		 1810 1810 1430	 2200 2200 1950	 mW
PWR, Pulse detector, filter off PD:PD = 1	Ta = 70 °C		780	975	mW
PWR, Data separator off PD:DS = 1	Ta = 70 °C		465	565	mW

POWER SUPPLY CURRENT AND POWER DISSIPATION (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PWR, Data separator & TBG Off PD:DS, PD:TB = 1	Ta = 70 °C		425	515	mW
Power up delay	From power up to all internal biaspoints stable, not tested on ATE			5.0	µs
Sleep mode	$\overline{\text{PDWN}}$ = low		2.5	10	mW
Recovery from idle mode: Under power management from RG active to SDP fully on from SG active to Pd_Qual fully on from WG active to write fully on			 30 50 10		ns

DIGITAL INPUTS

TTL COMPATIBLE INPUTS

Input low voltage (VIL)	Functional test on ATE			0.8	V
Input high voltage (VIH)	Functional test on ATE	2.0			V
Input low current (IIL)	VIL = 0.4 V			-0.4	mA
Input high current (IIH)	VIH = 2.4 V			100	µA

VRDT AND FREF INPUTS

Input low voltage (VIL)	Functional test on ATE			0.8	V
Input high voltage (VIH)	Functional test on ATE	2.4			V
Input low current (IIL)	VIL = 0.4 V			-0.2	mA
Input high current (IIH)	VIH = 2.4 V			500	µA

CMOS COMPATIBLE INPUTS
VPC = 5 V

Input low voltage (VIL)	Functional test on ATE			1.5	V
Input high voltage (VIH)	Functional test on ATE	3.5			V

PSEUDO ECL COMPATIBLE INPUTS

Input low voltage, VIL	For ref. only, no ATE	VPA-2.0		VIH-0.25	V
Input high voltage, VIH	For ref. only, no ATE	VPA-1.1		VPA-0.4	V
Input current	For ref. only, no ATE	-100		+100	µA

ELECTRICAL SPECIFIICATIONS (continued)

DIGITAL OUTPUTS

CMOS OUTPUTS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output low voltage	IOL = +2 µA			0.45	V
Output high voltage	IOH = -100 µA	0.7•VPD			V

DIGITAL DIFFERENTIAL OUTPUTS (WD, $\overline{WD}$)

Output low voltage, VOLD	Iol = -2 µA	VPD2-2.1		VOHD-0.3	V
Output high voltage, VOHD	Ioh = -2 µA	VPD2-1.4		VPD2-0.5	V
Output sink current	WG = highz		-3.5		mA

TEST POINT OUTPUT LEVELS ATO BUFFER CHARACTERISTICS

Unless otherwise specified, measured at AO pin, each loaded with 5 pF. For reference only, no ATE test.

Reference voltage	ASEL[1:0]=[0 0],	Typ.-130 m	MAXREF/2	Typ.+130 m	V
Swing	From reference voltage Rload ≥ 10 kΩ	+1.2/-0.6			V
Source impedance			50		Ω
Drive capability	± refers to source/sink	+2/-2	+5/-3		mA

TPC/D/E BUFFER CHARACTERISTICS

Unless otherwise specified, measured at pin, each loaded with 5 pF. (Reference only - no ATE)

Swing	Rload ≥ 10kΩ	1.0		Vps-1.5	V
Source impedance			45		Ω
Output current		-3/+0.8			mA
Common voltage			2.5		V
TPC/$\overline{TPC}$, TPD/$\overline{TPD}$ Input bias voltage	Recommended input condition		VPA-1.5		V

TPA/B/F/G BUFFER CHARACTERISTICS

Unless otherwise specified, measured at pin, each loaded with 5 pF. (Reference only - no ATE)

Swing	Rload ≥ 10 kΩ		0.8		Vppd
Gain			0.9		V/V
Source impedance			45		Ω
Output current	Source only		-3/+1		mA
Common voltage	Equalizer output		VPA-1.7 -2 Vbe		V

SERIAL PORT TIMING
For reference only, no ATE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SCLK Data clock period, (TC)	Write operation	12.5			ns
	Read operation	40			ns
SCLK Low time, (TCKL)	SCLK Input < 10% Vcc	4			ns
SCLK High time, (TCKH)	SCLK Input > 90% Vcc	4			ns
Enable to SCLK, (TSENS)		9			ns
SCLK to disable, (TSENH)		9			ns
Data set-up time, (TDS)	Write operation	3			ns
Data hold time, (TDH)	Write operation	3			ns
SDEN Min. low time, (TSL)		25			ns
SCLK Fall to data valid (TSDV)	Read operation SCLK rise/fall time = 3 ns max load on SDATA less than 25 pF	2		17	ns
SDATA Hold time, (TSDH)	Read operation	20			ns
SDEN Fall to SDATA tristate (TSDTRI)	Read operation			20	ns

AGC CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

AGC AMPLIFIER
The input signals are AC coupled to VIA and $\overline{\text{VIA}}$. Integrating capacitor C_{BYP} = 1000 pF, is connected between BYP and VPA. Integrating capacitor C_{BYPS} = 1000 pF, is connected between BYPS and VPA. Unless otherwise specified, the output is measured differentially at TPC/$\overline{\text{TPC}}$ set to output DP/DN, Fin = 5 MHz, the filter frequency Fc = max and the filter boost at Fc = 0 dB. All specifications apply equally to servo and read mode prior to SFC.

TPC/$\overline{\text{TPC}}$ Voltage (When enabled to output the filter DP/DN signal)	VIA = 20 to 250 m Vppd 1,1,-1,-1,--- pattern 5 MHz ≤ Fc ≤ 40 MHz, Fin=Fc, Boost = 0 to 13 dB	1.19	1.4	1.61	Vppd
Gain range	±50 µA forced into BYP	3		64	V/V
Gain sensitivity	BYP voltage change		33.4		dB/V
Differential input resistance	LOWZ = low, LZCTR = 0	5.8	7.6	10.8	kΩ
	LOWZ = low, LZCTR = 1	1.6	2.9	4.1	kΩ
	LOWZ = high, LZCTR =X	235	702	1085	Ω
Single-ended input resistance No ATE, reference only	LOWZ = low, LZCTR = 0 ± 100 µA		6.5		kΩ
	LOWZ = low, LZCTR = 1 ± 100 µA		1.9		kΩ
	LOWZ = high, LZCTR = 1 ± 250 µA		520		Ω

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output offset voltage change	Δ offset = |(offset at Gain = 64) - (offset at Gain = 3)|			200	mV
Input noise voltage	Gain = 24 dB Ω/Gain Fix mode Rs = 0 Ω		14	19	nV/√Hz
CMRR	Gain = 24 dB Ω/Gain Fix mode	33			dB
PSRR	Gain = 24 dB Ω/Gain Fix mode not tested on ATE	31			dB
TPC/$\overline{\text{TPC}}$ Voltage servo mode	SG = 1, SAGCL = 00	1.16	1.4	1.61	Vpdd
	SG = 1, SAGCL = 01	1.07	1.3	1.50	Vppd
	SG = 1, SAGCL = 10	0.97	1.2	1.38	Vppd
	SG = 1, SAGCL = 11	0.93	1.1	1.26	Vppd

AGC CONTROL SECTION

The input signals are DC coupled into TPC/$\overline{\text{TPC}}$, TPC/$\overline{\text{TPC}}$ enabled to drive DP/DN.RR = 8.06 kΩ

TPC/$\overline{\text{TPC}}$TPD/$\overline{\text{TPD}}$ common mode input voltage	For test only		VPA-1.5		V
Normal decay current, Id TPC = $\overline{\text{TPC}}$	FASTREC = low, SG = low	-31.2	-26	-20.8	µA
Servo mode normal decay current	FASTREC = low, SG = high TPC=$\overline{\text{TPC}}$	-31.2	-26	-20.8	µA
Fast rec decay current, Idf	FASTREC = high TPC = $\overline{\text{TPC}}$,	7 • Id	8 • Id	9 • Id	µA
Normal attack current, Ia	|TPC-$\overline{\text{TPC}}$| = 0.7875 V FASTREC = low	-20 • Id	-16 • Id	-13 • Id	µA
Fast attack current, Iaf	|TPC-$\overline{\text{TPC}}$| = 1.00 V, FASTREC = low	-163 • Id	-136 • Id	-108 • Id	µA
Fast rec attack current, Iafr	|TPC-$\overline{\text{TPC}}$| = 0.7875 FASTREC=HIGH	-81• Id	-59 • Id	-47 • Id	µA
Sample data AGC peak charge current DR/RR	0 < AGC < 3 34 <DR <127 AGC = SLC bits 1,0	-20%	$-2.66 \cdot 10^{-6}$ • AGC • DR/RR	+20%	A/V
Sample data AGC peak discharge current	DR = Data rate register	-20%	$+2.66 \cdot 10^{-6}$ • AGC • DR/RR	+20%	A/V
BYP/BYPS Pin leakage current	$\overline{\text{HOLD}}$ = low at gain = 3 and gain = 64	-70		+50	nA
VRC Reference voltage	Ioad = -50 µA /+500 µA	VPA - 3		VPA - 1.7	V

PULSE QUALIFIER CHARACTERISTICS

DUAL LEVEL QUALIFIER

Unless otherwise specified, a 100 m Vpp @ 15 MHz sine wave input is AC coupled into VIA/$\overline{\text{VIA}}$. Fc set to 127, boost at Fc = 0 dB. * implied not directly testable.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Data level threshold, Lth	ALE = 0 Before SFC, Lth = 10.7996 • LD + 4.8604 *After SFC Lth = 7.636 • LD + 3.4368 ALE = 1 Lth = 10.7996 • LD + 4.8604 for 16 ≤ LD ≤ 48 No ATE Test	Lth - 11%	Lth	Lth + 11%	%
Servo level threshold	Prior to SFC LSth = 10.1316 • LS + 12.6516 16 ≤ LS ≤ 48	LSth - 11%	LSth	LSth + 11%	V
$\overline{\text{RDS}}$ Pulse width low voltage	PWCTR = 0	7.7	15	20	ns
	PWCTR = 1	16.8	27	35	ns
PPOL to $\overline{\text{RDS}}$ delay time	PPOL rise/fall to $\overline{\text{RDS}}$ fall, measured at 1.5V crossing	4.5		12	ns
PPOL/RDS Rise time,	0.8 V to 2. V, CL ≤ 15 pF			8	ns
PPOL/RDS Rise time,	0.8 V to 2.4 V, $_{CL}$ ≤ 40 pF, ATE			10	ns
PPOL/RDS Fall time	2.4 V to 0.8 V, CL ≤ 15 pF			6	ns
PPOL/RDS Fall time	2.4 V to 0.8 V, CL ≤ 40 pF,ATE			8	ns

DIBIT PULSE QUALIFIER CHARACTERISTICS

Unless otherwise specified, a 100 m Vpp @ 15 MHz sine wave input is AC coupled into VIA/$\overline{\text{VIA}}$. Fc set to 127, boost at Fc = 0 dB. DIBITEN = 1.

Dibit discrimination Time interval Tr Note: Tr increment progression subject to change.	DBT [2:0] Register bits (Bits 6 - 4)				
	000	-80%	40 ns	+80%	ns
	001	-80%	65 ns	+80%	ns
	010	-80%	90 ns	+80%	ns
	011	-80%	115 ns	+80%	ns
	100	-80%	140 ns	+80%	ns
	101	-80%	165 ns	+80%	ns
	110	-80%	190 ns	+80%	ns
	111	-80%	215 ns	+80%	ns

ELECTRICAL SPECIFICATIONS (continued)

BASELINE OFFSET

See General for input conditions unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
BASELINE SHIFT TOLERANCE	SG = Low Blos = 2.374 mV • BLOSD + 11.656 SG = High Blos = 2.374 mV • BLOSS + 11.656 0 ≤ YIN ≤ 127	-15%		+15%	

THERMAL ASPERITY

See General for input conditions unless otherwise specified.

Thermal asperity threshold, TAth	TAth [mV] = 50 • TATH + 750 0 ≤ TATH ≤ 15	-13%	TAth	+13%	mV
Dynamic Hi-Y admittance yin at VIN/VINB	Yin [Siemens] = 1/724 + YIN/2520 0 ≤ YIN ≤ 7	-13%	Yin	+13%	Siemens
Hi-Y Period T_{Hi-Y}	T_{Hi-Y} = 0.959 • HYTMR + 0.927 0 ≤ HYTMR ≤ 3	-13%	T_{Hi-Y}	+13%	µs
PLL/AGC Hold period TA_{hold}	TA_{hold} = 0.117 • TATMR + 0.158 0 ≤ TATMR ≤ 7	-13%	TA_{hold}	+13%	µs

QASYM FACTOR

Unless otherwise specified, measured at AO pin, each loaded with 5 pF. VIA-$\overline{VIA}$ = Lorentzian pulses with 10% asymmetry. Asymmetry (%) = $((V_{+1}-V_{-1})/(V_{+1}+V_{-1})) \bullet 100$, where V_{+1} = positive “1” sample value, V_{-1} = negative “1” sample value.

Reference voltage	ASEL[1:0] = [0 0],	Typ.-130m	MAXREF/2	Typ.+130m	V
Qasym at ATO	No ATE, reference only		700		mV

INTERNAL AC COUPLER CHARACTERISTICS

Unless otherwise specified, measured at TPC/$\overline{TPC}$ or TP/$\overline{TPD}$ pins, each loaded with 5 pF.

Offset voltage	ACD = 0		5	±35	mV
Low_Z time constant	LOWZ = 1; LZCTR = X, No ATE		0.3		µs
Non Low_Z time constant	LOWZ = 0: LZCTR = 0 LZCTR = 1		5.0 1.5		µs

PROGRAMMABLE FILTER CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply. The input signals are AC coupled to VIA and $\overline{VIA}$. RX = 10.2 kΩ from VRX pin to GND. All specifications identical for identical data and servo register settings. Output signals are measured at TPC/$\overline{TPC}$ for ON, TPD/$\overline{TPD}$ for OD. VRDT = high, $\overline{HOLD}$ = low.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Filter cutoff range, Fcr	Fc (MHz) = 0.4959 • FC + 1.0022, 18 ≤ FC ≤ 127 0 dB Boost		10MHz to 64 MHz		MHz
Filter Fc accuracy, Fca	44 ≤ FC ≤127 18 ≤ FC ≤ 43	-15 -20		+15 +20	%
OD gain to ON gain mismatch	Fin = 0.67 • Fc 0 dB Boost	-30		+30	%
Boost @ Fc	Boost = 20Log[0.04345 • FB - 0.0000337 • FB • FC +1] 0 ≤ FB ≤ 127		0 to 15		dB
Boost accuracy	Set for Boost = 15 dB	-2		+2	dB
	Set for Boost = 9 dB	-1.7		+1.7	dB
Servo boost accuracy	@5 and 14 MHz		FBSx2		
TGD Variation (No boost) measured at ON/$\overline{ON}$ outputs	Fc = 64 Mhz F = 0.3 Fc to Fc, 0 dB Boost	-700		+700	ps
	Fc = 23 MHz to 64 MHz F = 0.3 Fc to Fc, 0 dB Boost	-5		+5	%
	Fc = 23 MHz to 64 Mhz F = Fc to 1.75 Fc, 0 dB Boost	-6		+6	%
TGD Variation (Maximum boost) Measured at ON/$\overline{ON}$ outputs	Fc = 64 Mhz F = 0.3 Fc to Fc; FB=127	-700		+700	ps
	Fc = 23 MHz to 64 Mhz F = 0.3 Fc to Fc; FB = 127	-5		+5	%
	Fc = 23 MHz to 64 Mhz F = Fc to 1.75 Fc, FB = 127	-6		+6	%

PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Group delay equalization accuracy (asymmetrical)	Fc = 23-64 MHz Boost = 0 dBD Δ% = 0.9783 • FGD - 0.665		± 5		%
ON - $\overline{ON}$ Filter output dynamic range	THD = 2.5% max Fin = 0.67 Fc	1.4			Vp-p
Dp/Dn Output noise voltage, no boost. no ATE test	BW = 100 MHz, Rs = 50 Ω mode Fc = 127; FB = 0,FBS = 0, Gain = 24 dB Ω/fixed gain mode	0.9	3	5.1	mVrms
Dp/Dn Output noise voltage, max. boost.	BW = 100 MHz, Rs = 50 Ω Fc = 127; FB = 127,FBS = 0, Gain = 24 dB Ω/fixed gain mode	8.3	17.0	26.7	mVrms

TRANSVERSAL FILTER CHARACTERISTICS

Km1 Range *	No ATE; Reference only	±0.15	±0.26		
Km1 Gain drift	EQHOLD = 1Hold time ≤ 1ms		0.015	0.05	V/V/µs
Km2 Accuracy: Range and resolution	4 bit resolution, 2's compliment Range = -0.15 to + 0.13125 Resolution = 0.01875 Tested at both extremes of 7h and 8h	±20% -0.01		±20% + 0.01	%
Km1 A/D Accuracy	Preset to N ≤ 16 & A/D to M	M = N-1	M = N	M = N+1	
*Km1 and VC - $\overline{VC}$ are approximately related by: Km1 = 0.018 • DR • (VC - $\overline{VC}$), where DR = DR register setting however Km1 can not be directly tested.					

TIME BASE GENERATOR CHARACTERISTICS

RR = 8.06 kΩ 1% tolerance, from RR pin to GND for 240 Mbit/s operation respectively.

FREF Input range	CM1:BT = 0	6		50	MHz
	CM1:BT = 1, TM1:EFR = 1			130	MHz
FREF Input range	CM1:BT = 0, TM2:DIFFBF = 1			225	MHz
FREF Input pulse width	CM1:BT = 0	10			ns
F_{TBG} Output frequency range		85		255	MHz
F_{TBG} Jitter	> 10K Samples; not ATE tested, guranteed by design		30	200	ps_{RMS}
M Counter range	ATE Functional test only	2		255	
N Counter range	ATE Functional test only	2		127	

TIME BASE GENERATOR CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCO Center frequency, F_{TBG}	V(FLTR1 - $\overline{FLTR}$) = 0 V Fo = (2.4151 • DR + 9.1339) MHz	0.80 F_O		1.20 F_O	MHz
VCO Dynamic range	-2.0 V ≤ V(FLTR1 - $\overline{FLTR}$) ≤ 2.0 V, F_{TBG} = 80 MHz	+25			%
VCO Control gain, K_{VCO}	$\omega\iota = 2\pi \bullet F_{TBG}$ -1.0 V ≤ V(FLTR1 - $\overline{FLTR}$) ≤ 1.0 V	0.12 • $\omega\iota$	0.18• $\omega\iota$	0.24 • $\omega\iota$	rad/(V-s)
Phase detector gain, KD	KDO = 4.0175 • DR + 3.2741 for RR = 8.06 kΩ	0.72KDO		1.22KDO	µA/rad
K_{VCO} • KD product accuracy		-28		+28	%

DATA SEPARATOR CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

READ MODE

Read clock rise time, TRRC	0.8 V to 2.4 V, C_L ≤ 15 pF			10	ns
Read clock fall time, TFRC	2.4 V to 0.8 V, C_L ≤ 15 pF			10	ns
RCLK Pulse width, TRP	Except during re-sync	4/9 TORC -5		4/9 TORC +5	ns
NRZx Out set-up and hold time, TNS, TNH		13			ns
$\overline{SBD}$ Set-up and hold time TSBS		13			ns

WRITE DATA OUTPUT

Write data output rise time, TRWD	20% to 80% points 2 kΩ to GND, CL ≤ 15 pF			3	ns
Write data output fall time, TFWD	80% to 20% points 2 kΩ to GND, CL ≤ 15 pF			3	ns
WD Jitter	Preamble pattern, guaranteed by design and characterization		90	200	ps_{RMS}

ELECTRICAL SPECIFIICATIONS (continued)

WRITE MODE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write clock rise time, TRWC	0.8 to 2.0 V input conditions			10	ns
Write clock fall time, TFWC	2.0 to 0.8 V input conditions			8	ns
NRZx Set-up time, TSNRZ	Functional test only	10			ns
NRZx Hold time, THNRZ	Functional test only	3			ns
PERR Propagation delay from rising edge of WCLK, Tperr	1.5 V to 1.5 V,CL ≤ 15 pF			41	ns

WRITE PRECOMPENSATION

Write precomp time shift, TPC as a % of T_{TBG}, or (%)wpc=TPC/ T_{TBG},	Relative to WPC1 = 0, repeating 03_h in direct write mode 1 ≤ WPC1 ≤ 13 WPC1 = 15, ATE test only on functionality at WPC1 = 15	1.89 • WPC1-2 23.5	2.1 • WPC1 30	2.31 • WPC1+3 36	%
	Level 2 Precomp 1 ≤ WPC2 ≤ 13 WPC2 = 15, WPC1 = 0	0.85 • WPC2-2 11	1 • WPC2 15.5	1.15 • WPC2+3 21	%
	Level 3 Precomp 1 ≤ WPC2 ≤ 15 ATE test only functionality at WPC = 15	0.18 • WPC2-0.5	0.9 • WPC2	1.08 • WPC2+3	%

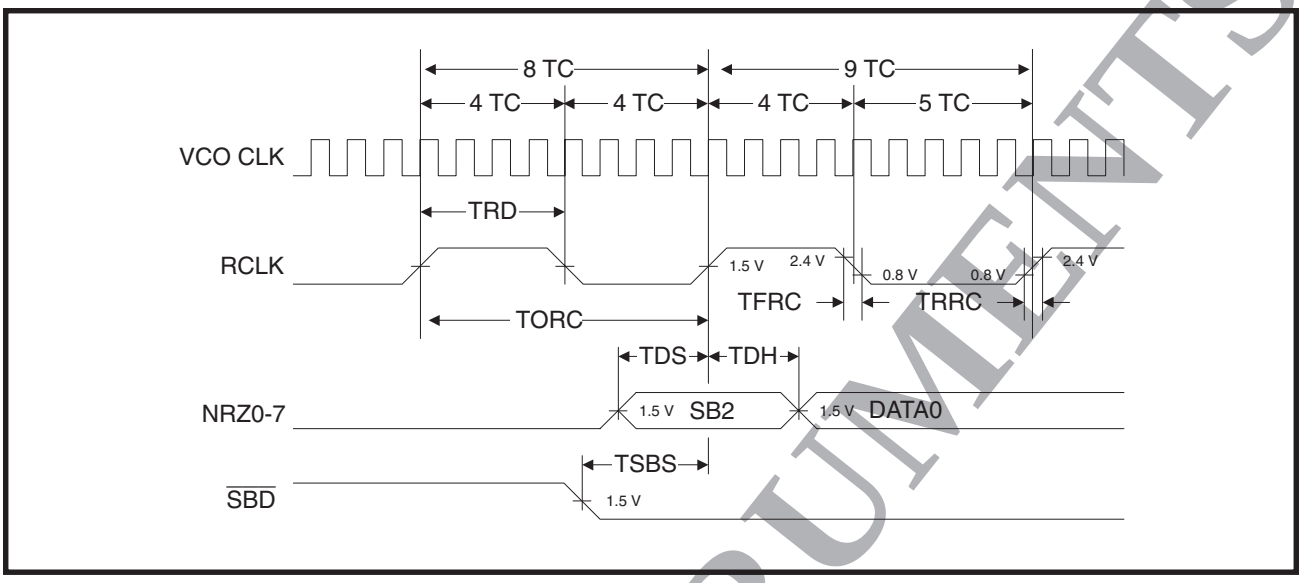


FIGURE 32: Read mode NRZ interface timing

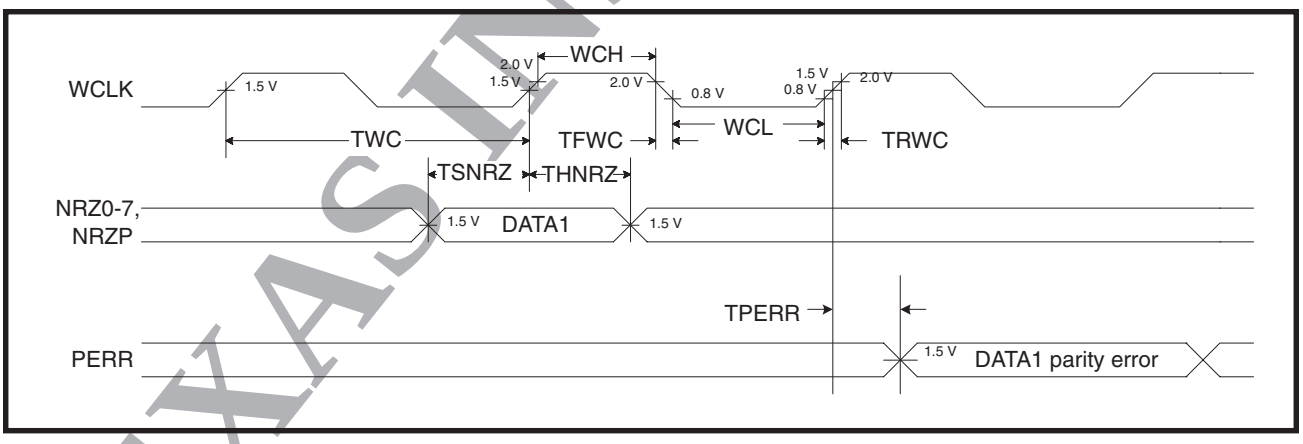


FIGURE 33: Write mode NRZ interface timing

ELECTRICAL SPECIFIICATIONS (continued)

DATA SYNCHRONIZER PLL

RR = 8.06 kΩ 1% tolerance, from RR pin to GND for 240 Mbps operation.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCO Center frequency, F_{VCO}	V(FLTR1 - $\overline{FLTR1}$) = 0 V FO = (2.4151 • DR + 9.1339) MHz	0.80 • FO		1.20 • FO	ns
VCO Dynamic range in each direction	-7.0 V ≤ V(FLTR2 - $\overline{FLTR2}$) ≤ 0.7 V for DR = 127 -2.1 V ≤ V(FLTR2 - $\overline{FLTR2}$) ≤ 2.1 V for DR = 42	+25			%
VCO Control gain & M M • K_{VCO}	ωi = 2π F_{VCO} M=3.4 • (DR/127) -0.25 V ≤ V(FLTR2 - FLTR2) ≤ +0.25 V	0.11ωi M		0.26 ωi M	rad/(V-s)
Charge pump transconductance	Gm = 403 µA/V during synchronization gear shift factor, for reference only, not ATE tested:when 610	0.45 Gm		1.55 Gm	A/V
Damping amplifier gain, A • Kvco product accuracy	A = 0.7 • (DRC/127) DRC = Damping Ratio Control register setting	-30		+30	%
Idle mode phase detector gain, KDI	KDI = 0.15 Gm • M		KDI		µA/rad
Gm • M • K_{VCO} product accuracy		-28		+28	%

SERVO CHARACTERISTICS

Unless otherwise specified: A 15 MHz sine wave is input into the DP/DN inputs (PD:TPC/D/E = '01';CM2: SERI = 0). STROBE and $\overline{RESET}$ durations are 1.0 µs CM2:SBCC = "10".

MAXREF Output voltage	Isource = 0 µA	3.06	3.21	3.42	V
MAXREF Load regulation	Isource = 0 to 0.15 µA			40	mV
A, B, C, D Output low voltage,Vol	Isink = 0.2 µA, $\overline{RESET}$ = low	120	250	420	mV
A, B, C, D Calibration reference output = Vol+refereceªMaxref/2	Isink = 0.2 µA, calibration voltage with FCS(bit7) = 1	1.33	1.54	1.77	V
A, B, C, D Output swing Voh-Vol	DP/DN = 1.4 Vp-p	2.62	2.81	3.07	V
A, B, C, D Output resistance	Isource/Isink = 0.2 µA			50	Ω

SERVO CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
A, B, C, D Gain	0.3 V ≤ DP-DN ≤ 1.4 V	1.90	2.04	2.27	V/V
	0.1 V ≤ DP-DN ≤ 0.3 V	1.43		2.27	V/V
Hold droop	STROBE = low $\overline{\text{RESET}}$ = high			0.5	mV/µs
Channel to channel swing mismatch	DP-DN = 0.75 Vpp In either normal or self calibration mode			95	mV
Burst Capture time	Output ≥ 95% of final value			0.5	µs
Burst reset time	DP-DN = 1.4 Vpp Output ≤ 5% of final value from $\overline{\text{RESET}}$ fall			0.5	µs
STROBE to STROBE width		20			ns

Table 12: Mode Control

WG	RG	SG	MODE	DESCRIPTION
0	0	0	Idle mode	DS VCO Locked to FTBG. NRZ1-0 tri-stated.
0	1	0	Data read mode	DS PLL Acquisition, adaptive equalizer training, code word boundary search and detect, decode, sync byte detect, and NRZ data output. DS VCO switched from FTBG to RD after preamble detect. RCLK gen. input switched from FTBG to DS VCO. RCLK re-synchronized to RD at code word boundary detect. NRZ1-0 active.
1	0	0	Data write mode	Write mode preamble insertion and data write. DS VCO locked to FTBG. RCLK synchronized to FTBG. WD and $\overline{\text{WD}}$ active. NRZ1-0 tri-stated.
1	1	0	Read override	RG Overrides WG which causes any write in progress to cease and data read mode to be entered.

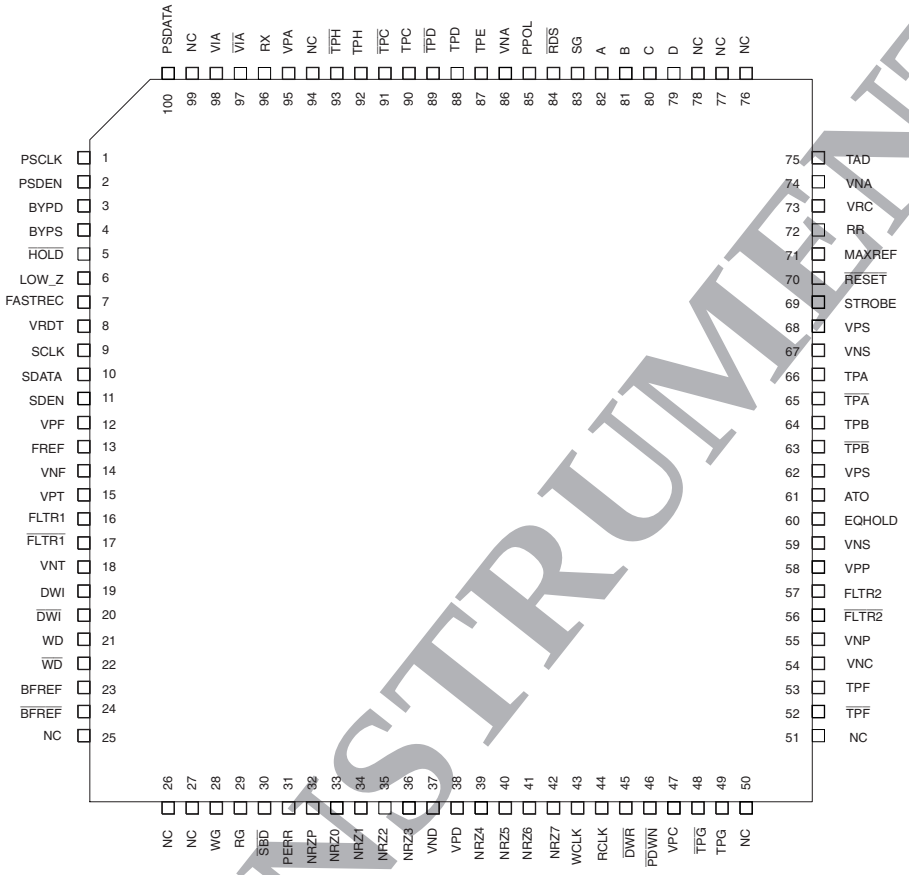
DIAGNOSTIC/OPTMIZATION TEST MODES

Some disk drive diagnostic test and operating optimization may be performed by observing the Equalizer and AGC Control voltages and measuring their change with different conditions. For example, the Equalizer Control Voltage ("0" sample values) is affected by the Continuous Time Filter/Equalizer setting, the head flying height, and the head gap length. The KM1 A/D function may be used to monitor flying height changes. The AGC Control Voltage ("1" sample values) are also affected by the previously mentioned factors and by magnetic nonlinearities. The effectiveness of Write Precomp compensating the nonlinearities could be evaluated by observing the AGC Control Voltage difference of a maximum transition dibit pattern with a pattern with minimum transitions.

SSI 32P4103A
PRML Read Channel with EPR4, 16/17 (0,6/8) ENDEC, 4-Burst Servo

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead TQFP
Deep downset

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32P4103A 100-Lead TQFP Deep Downset	32P4103A-CGE	32P4103A-CGE

Preproduction: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SSI 32P4103B

PRML Read Channel with EPR4, 16/17 (0,6/8) ENDEC, 4-Burst Servo

February 1999

DESCRIPTION

The SSI 32P4103B is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Extended Partial Response Class 4 (EPR4) read channel for zoned recording hard disk drive systems with data rates from 80 to 240 Mbps.

Functional blocks include AGC, programmable filter, adaptive transversal filter, 1+D filter, full EPR4 Viterbi detector, 16/17 (0,6/8) GCR ENDEC, data synchronizer, time base generator, thermal asperity detection and compensation, and FWR area detect servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones.

The part requires a single +5 V power supply.

The SSI 32P4103B utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 80 to 240 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for EPR4 equalization**
- **Five tap transversal filter with adaptive or programmable tap weight**
- **Thermal asperity management for dual stripe MR heads**
- **Silicon Systems Proprietary 16/17[0,6/8] GCR ENDEC**
- **Data Scrambler/Descrambler**
- **Programmable two level write precompensation**
- **Register programmable dynamic power management (<5 mW power down mode)**
- **Digital Channel Quality Monitor**
- **Byte wide bi-directional NRZ data interface**
- **Serial interface port for access to internal program storage registers including serial port buffer for interface to preamp**
- **Single 5 V ± 10% power supply**
- **Small footprint 100-pin deep downset TQFP package**

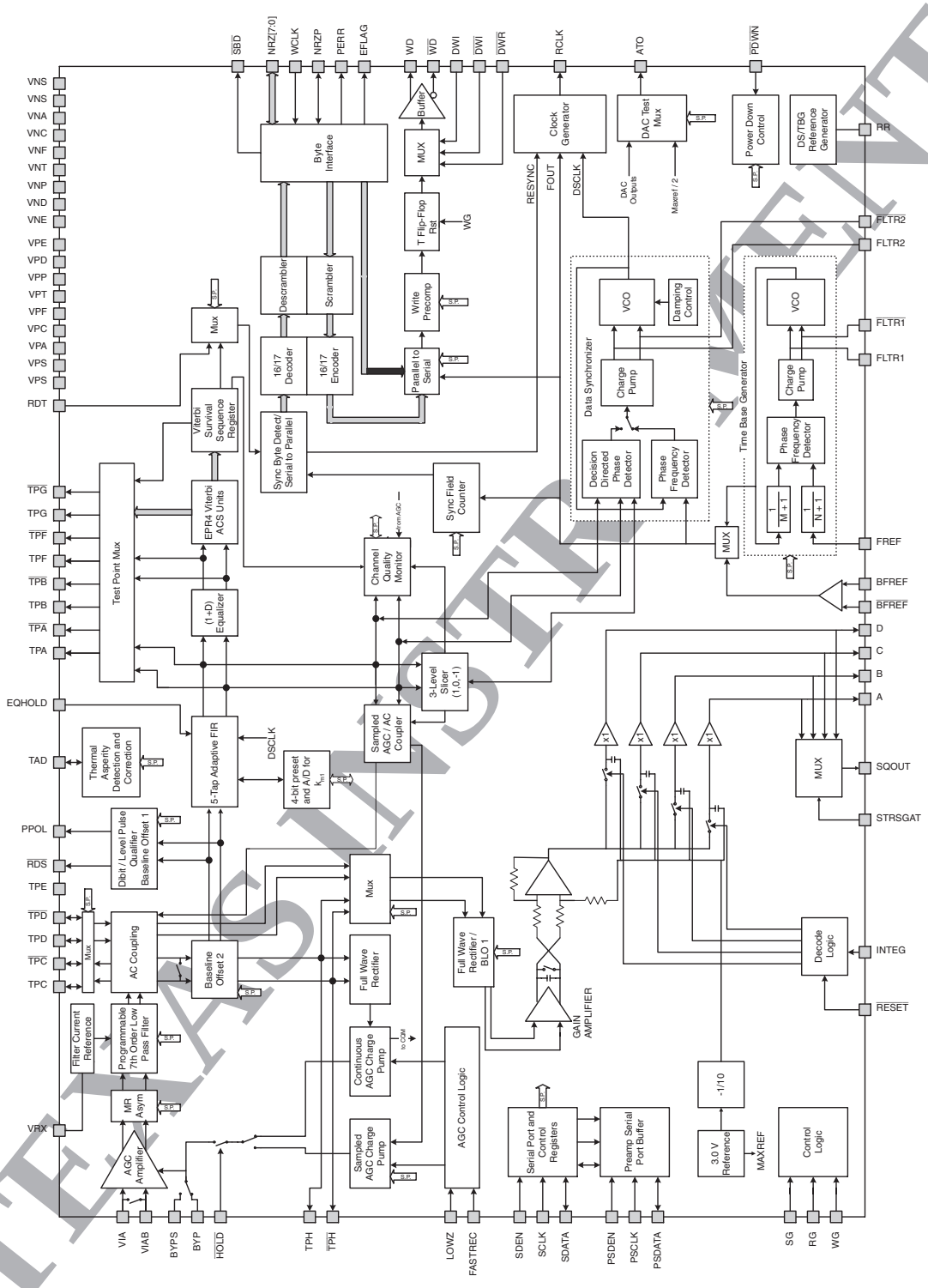
AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents for data reads**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Low Z input switch with gain squelch**
- **AGC hold, fast recovery, and AGC input impedance control signals**
- **Wide bandwidth, precision full-wave rectifier**
- **2-bit DAC to control AGC voltage in servo mode between 1.1 and 1.4 V**

FILTER/EQUALIZER

- **Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:**
  - **Channel filter and pulse slimming equalization for coarse equalization to PR4**
  - **Programmable cutoff frequency from 10 to 64 MHz**
  - **Programmable boost /equalization of 0 to 15 dB**
  - **Programmable “zeros” equalization to fix time asymmetry**

BLOCK DIAGRAM



FILTER/EQUALIZER (continued)

- ±0.7 ns group delay variation from 0.3 Fc to Fc, with Fc = 64 MHz
- Low Z switch for fast offset recovery at the filter output, on-chip direct-coupling at input and output to eliminate external AC-coupling capacitors.
- Five tap transversal filter for fine equalization to EPR4 with self adapting or programmable symmetric taps
- Equalization hold input
- Asymmetry factor output
- MR Asymmetry correction

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to EPR4
- Register programmable hysteresis, window or dibit qualification for servo reads
- Adjustable baseline shift of PPOL & RDS and Quantizer threshold to compensate for pulse asymmetry due to MR head

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 240 • 17/16 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 16/17 GCR ENDEC
- Register programmable to 240 Mbit/s operation
- Fast Acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- Byte wide NRZ data interface
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync word detection
- Dual sync word detection ("or" type) with programmable pads in between 2 sync words
- Dual header mode option

SERVO

- 4-burst Area Detect servo capture with A, B, C, D outputs
- ABCD outputs clamp at MAXREF
- Internal hold capacitors
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- 3 bits of fine gain control to accommodate for a wide range of pulse densities into the area detector
- Wide bandwidth, precision full-wave rectifier
- Servo Calibration output available
- Programmable Baseline Offset

THERMAL ASPERITY DETECTION AND SUPPRESSION

- Programmable Thermal Asperity with Erasure Flag
- AGC hold and PLL hold over during TA event with programmable duration
- Programmable HiY

FUNCTIONAL DESCRIPTION

The SSI 32P4103B implements a complete high performance EPR4 read channel, including an AGC, programmable filter / equalizer, adaptive transversal filter, Viterbi pulse qualifier, time base generator, data separator with 16,17 ENDEC and scrambler/ descrambler, and FWR servo, that supports data rates up to 240 Mbps.

A serial port is provided to write control data to and read from the internal program storage registers.

AGC CIRCUIT

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input to the sampled data processor while the input from the Read/Write preamplifier varies. The circuit consists of an AGC loop that includes an AGC amplifier, charge pump, programmable continuous time filter, and a precise, wide band, full wave rectifier. Depending upon whether the read is of a servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to common mode noise.

The behavior of the AGC circuit, prior to the vcolock, is controlled by 3 pins ($\overline{\text{HOLD}}$, LOWZ, FASTREC) and the control register bits (TC and TCS Registers and AGCT bit 6 of CM1 Register). The device supports two modes of operations: externally timed or self timed. For the former, AGCT bit of CM1 should be “0” and for the latter “1”. The first three pins listed above determine the hold low-Z, and fast recovery periods.

For the external timed mode of operation the 3 pins listed above provide complete control of all of the timings.

For the self timed mode the 3 pins should be deasserted, i.e., $\overline{\text{HOLD}}$ = high, LOWZ = low, and FASTREC = low. TC and TCS Registers provide complete timings. However, it should be noted that any assertion at $\overline{\text{HOLD}}$, LOWZ, FASTREC will override the self timed mode of operation. With AGCT bit of CM1 set high, the low-Z and fast timings are generated by a circuit which counts the periods of TBG reference frequency (FREF). They are triggered by various conditions of the WG/$\overline{\text{WG}}$, SG and $\overline{\text{PDWN}}$ inputs. This mode of operation is supplied to simplify the generation

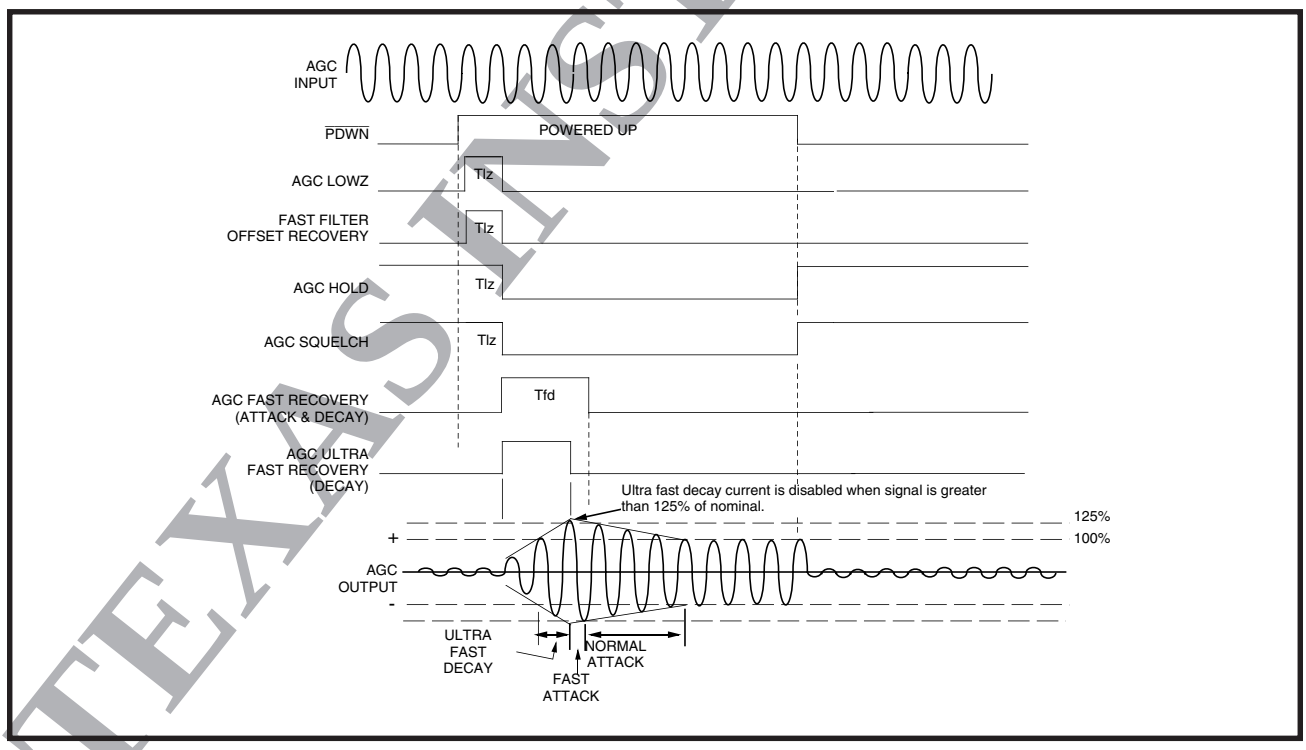


FIGURE 1: AGC Internal Timing Diagram, Power-on Mode

of the mode control signals. The timings for data mode and servo mode are independently controlled by bits in the Time Control Register (TC) and the Time Control Register for Servo (TCS). The TCS Register controls the low-Z (Tlzs) and fast recovery (Tfds) times when in servo mode and the TC Register controls these times (Tlz, Tfd) when not in servo mode. Additionally, the AGC timing following servo gate"Úalling edges can be tied to the TC or TCS controls as set by the CQM3:SGBTMR bit. The TC and TCS Registers define the internal AGC timing as a multiple number of FREF (reference clock) periods. For higher frequency reference clocks the AGC timings can be doubled using the N:FREFPS Register bit.

The low-Z mode is triggered at power-up, at each transition of SG, and at the falling edge of WG. The low-Z mode which follows the SG transitions does not force a low impedance condition at the AGC input pins. The fast recovery mode immediately follows the end of each low-Z time specified by the LZT or LZTS setting, but the low-Z mode will be invoked until the end of the fast recovery time specified by the FRT (read/idle mode) or FTRS (servo mode) setting if the FDFLOWZ bit = 0. If FDFLOWZ = 1, the low-Z time ends at the start of the fast recovery mode. In servo mode, when the fast recovery has timed-out, the AGC automatically goes into Hold for the remaining duration of the SG input signal. This allows the servo burst amplitudes to be captured without any interference from the AGC loop. The $\overline{\text{HOLD}}$ input pin can still be asserted at any time to initiate the hold mode.

Ultra fast recovery mode begins whenever fast recovery mode starts, and ends when the signal at DP/DN reaches 125% of the programmed value. This is initiated by setting the OFDC bits in the TC Register (TC:UFDC).

After the sync field count (SFC) as set by SLC:SFC the AGC enters the sampled-AGC mode in which the AGC charge pump is controlled by the error between the measured "one" values and the ideal value. This mode is automatically entered into after achieving PLL lock in read mode.

LOW_Z, FAST RECOVERY, HOLD AND NORMAL PERIODS

During the Hold period, the AGC gain is held constant subject only to leakage currents at the BYP pins. The value of the capacitors placed at these pins should be selected to give adequate droop performance when in Hold mode as well as to insure the stability of the AGC loop when not in Hold mode. This mode should be asserted over the servo bursts. In servo mode, when the fast recovery has timed out, the AGC automatically goes into hold for the remaining duration of the SG input signal. This allows the servo burst amplitudes to be captured without any interference from the AGC loop. The $\overline{\text{HOLD}}$ input pin can still be asserted at any time to initiate the HOLD mode.

During the Low-Z period, the AGC amplifier input resistance is reduced to allow quick recovery of the AGC amplifier input ac-coupling capacitors. (Also, the time constant of the internal AC coupling network at the filter outputs is reduced (fast filter offset recovery) to 300 ns from 5 µs or 1.5 µs depending upon the state of LZCTR bit in TCS. The duration of this period can also be extended to the end of Fast Recovery by appropriately setting MISC2:FDFLOWZ. The low-Z period also forces AGC gain to reduce to almost 0V/V (AGC squelch). This mode should be activated by asserting LOWZ pin during and for a short time after a write operation. It should also be activated for a short time after each transition of the SG input or after initial power up.

In the Fast Recovery period, the attack and decay currents are increased to allow faster recovery of the proper AGC level. During this period, in either external or self timed mode, the Ultra Fast Recovery may be effected by appropriately setting TC:UFDC. This will allow an extremely rapid increase of AGC amplifier gain. This mode shuts itself off when the signal at DP/DN reaches the 125% of the programmed value. For this mode to be invoked in read/idle mode as well as servo mode, the UFDSEL bit (TCS 6) must = 1.

During the Normal period (i.e., the period other than low-Z, fast recovery or hold prior to vcolock), the normal attack and decay currents are used to maintain a constant signal peak level at the qualifier inputs.

LOW_Z, FAST RECOVERY, HOLD AND NORMAL PERIODS (continued)

AGC Operation in Servo Read Mode

During servo reads, the AGC loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (CBYPS) which is referenced to VPA (positive supply). The dual rate charge pump drives CBYPS with currents that force the differential peak to peak voltage at the filter output (DP/DN) to a programmed peak to peak voltage. Attack currents lower the voltage at BYPS, which reduces the amplifier gain. Decay currents raise the voltage at BYPS, which increases the amplifier gain. The sensitivity of the amplifier gain to changes in the BYPS voltage is about 38 dB/V. When the voltage at BYPS is equal to VRC (bandgap voltage output pin), the gain from AGC input to DP/DN will be about 24.9 dB. The charge pump is continuously driven by the instantaneous voltage at DP/DN. When the signal at DP/DN is greater than 100% of the programmed AGC level, the normal attack current (Ia) of 416 µA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, the fast attack current (Iaf) of 3.54 µA is used to reduce the gain very quickly. This dual rate approach allows the AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A normal decay current (Id) of 26 µA acts to increase the amplifier gain when the signal at DP/DN is less than 100% of the programmed AGC level. The large ratio (416 µA:26 µA) of the normal attack and normal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. Unfortunately, this implies that the AGC loop will not be able to quickly increase its gain if required to do so. A fast recovery mode is provided to allow the AGC gain to be rapidly increased in order to reduce the recovery time between mode switches. In the fast recovery mode, the decay current is increased by a factor of 8 to 208 µA (Idfr) and the attack current is increased by a factor of 4.18 to 1.42 µA (Iafr). This has the effect of speeding up the AGC loop by a factor somewhere between 4 and 8 times.

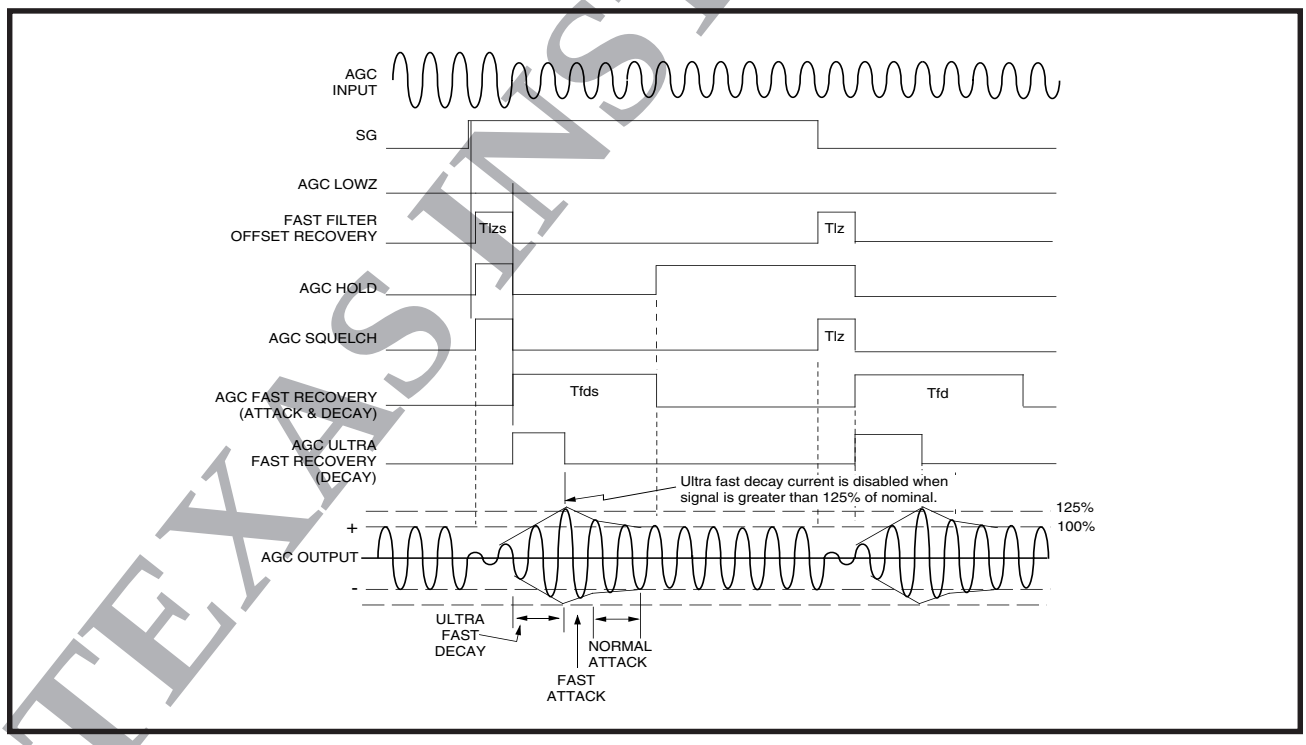


FIGURE 2: AGC Internal Timing Diagram - Servo Mode

When the CM1:AGCT (self-time) bit is set low, the AGC mode control is determined by the LOWZ and FASTREC input pins. This mode of operation is supplied for maximum application specific flexibility. It is recommended that the FASTREC be asserted when the AGC fields from a sector are being read. Typically, this will be just after each transition of SG (Servo Gate), after power up, and after WG is de-asserted. For example, if CBYPS is 500 pF and FASTREC is asserted for 0.5 µs in Servo mode, the voltage at BYPS can increase at most by 0.5 µs • 208 µA/500 pF = 208 mV, which will allow the gain to increase by 6 dB in that time. If FASTREC is asserted for 0.5 µs in non-Servo mode and CBYPD is 1000 pF, then the voltage at BYPS can increase at most by 0.5 µs • 208 µA/ 1000 pF = 104 mV, which will allow the gain to increase by 3 dB in that time. It is recommended that LOWZ be asserted for 0.5 µs just prior to any assertion of FASTREC in order to quickly null out any internal DC offsets. (However, it is possible to assert both LOWZ and FASTREC simultaneously in order to reduce sector overhead as much as possible. This should be evaluated under actual operating conditions.) The rising edge of FASTREC may also be used to initiate ultra fast recovery. See the AGC description section above.

In servo mode, the programmed AGC level may be adjusted between 1.10 and 1.40 Vp-pd by programming the two AGCDAC bits in the LDS Register. This allows the servo demodulator dynamic range to be adjusted a small amount.

AGC Operation in Data Read Mode

For data reads, the loop described above is used until the data synchronizer is locked to the incoming VCO preamble except that the CBYP hold capacitor is used instead of CBYPS. After the data PLL is locked, the AGC loop is switched to include the AGC amplifier with a sampled charge pump, the programmable continuous time filter, and the sampling 5-tap equalizer to more accurately control the signal amplitude into the Viterbi

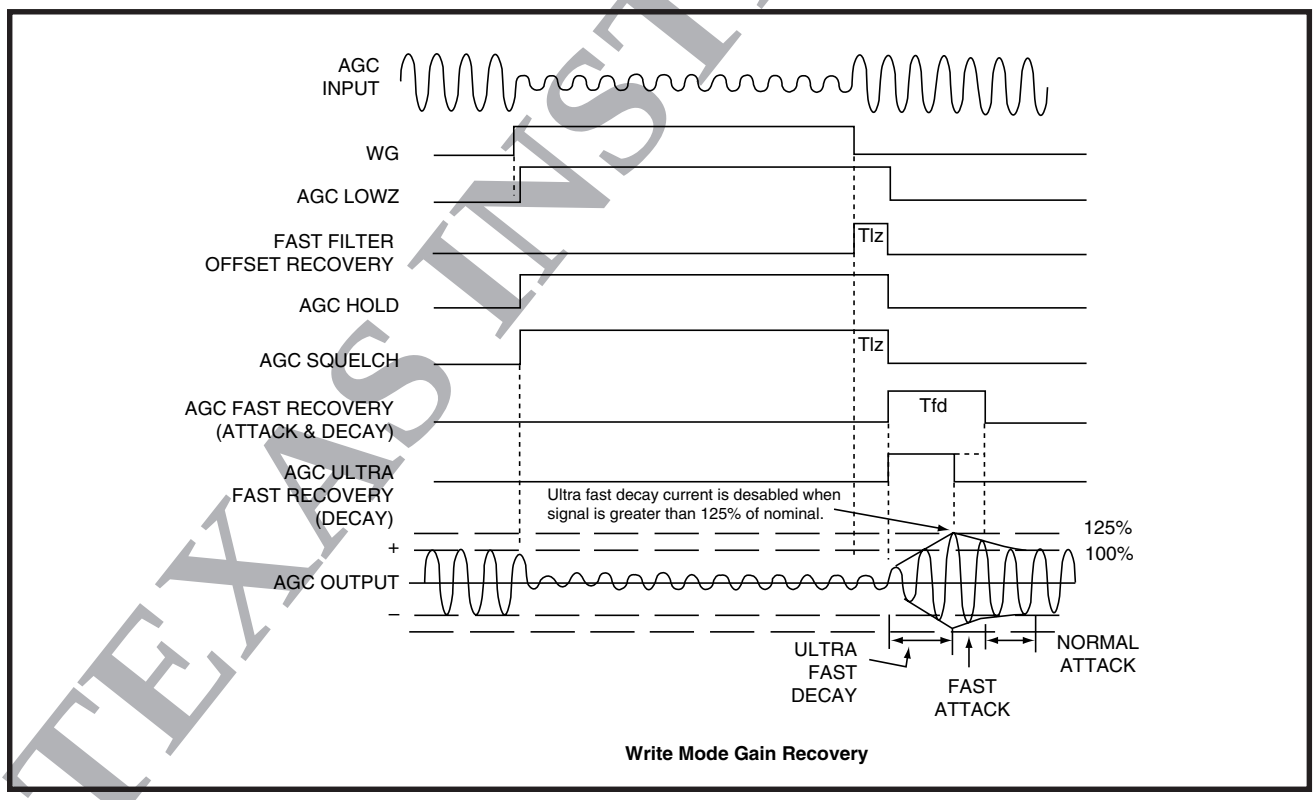


FIGURE 3: AGC Internal Timing Diagram- Write Mode

AGC Operation in Data Read Mode (continued)

qualifier. In this sampled AGC mode, a symmetrical attack and decay charge pump is used. The "1" sample amplitudes are sampled, held, and compared to a threshold to generate the error current. The maximum charge pump current value can be programmed from the SLC Register to 0, 1, 2 or 3 times the sample mode discharge current which is proportional to the Data Rate Register value.

AGC Operation from Write Mode

Low-Z, hold, and squelch modes are asserted immediately when write mode is entered (WG asserted). When WG is de-asserted, low-Z mode is extended until the end of the low-Z time, concurrently with hold mode and squelch mode. Fast filter offset recovery is also initiated until the end of the low-Z timing which follows the deassertion of WG. This is followed by the onset of fast recovery mode, during which the gain of the AGC is rapidly increased. If ultra-fast recovery is enabled, it turns off when the output signal has increased to 125% of the nominal output level. This is followed by attack modes which reduce the gain to its nominal level.

SERVO DEMODULATOR CIRCUIT

Servo functionality is provided by two separate circuits: the servo demodulator circuit, and the dual level pulse qualifier circuit. To support embedded servo applications, the SSI 32P4103B provides separate programmable registers for servo mode filter cutoff frequency, boost, and qualification threshold. The values programmed in these registers are selected upon entry into servo mode (SG pin asserted to logic high). Either the normal or differentiated filter signal can be routed to the servo demodulator by setting CM2:SERI.

Also the RDS pulse polarity and its nominal pulse width are each one bit programmable via SERI and PWCTR bits both in CM2 Register, respectively.

The servo demodulator circuit captures four separate servo bursts and provides an amplified and offset version of the voltages captured for each at the A, B, C, and D output pins respectively. Internal burst hold capacitors are provided to reduce external component count. Burst capture control is provided by the INTEG and $\overline{\text{RESET}}$ input pins. In addition to the A, B, C, and D outputs pins, the circuit provides a maximum reference voltage at the MAXREF output pin. This reference voltage represents the maximum voltage that can be achieved at the A, B, C, and D output pins with a 1.4 Vp-p signal at the filter output and is typically used as the reference voltage for an external A/D converter. The integrator gain can be set to one of eight values using CM2:IGAIN[2:0]

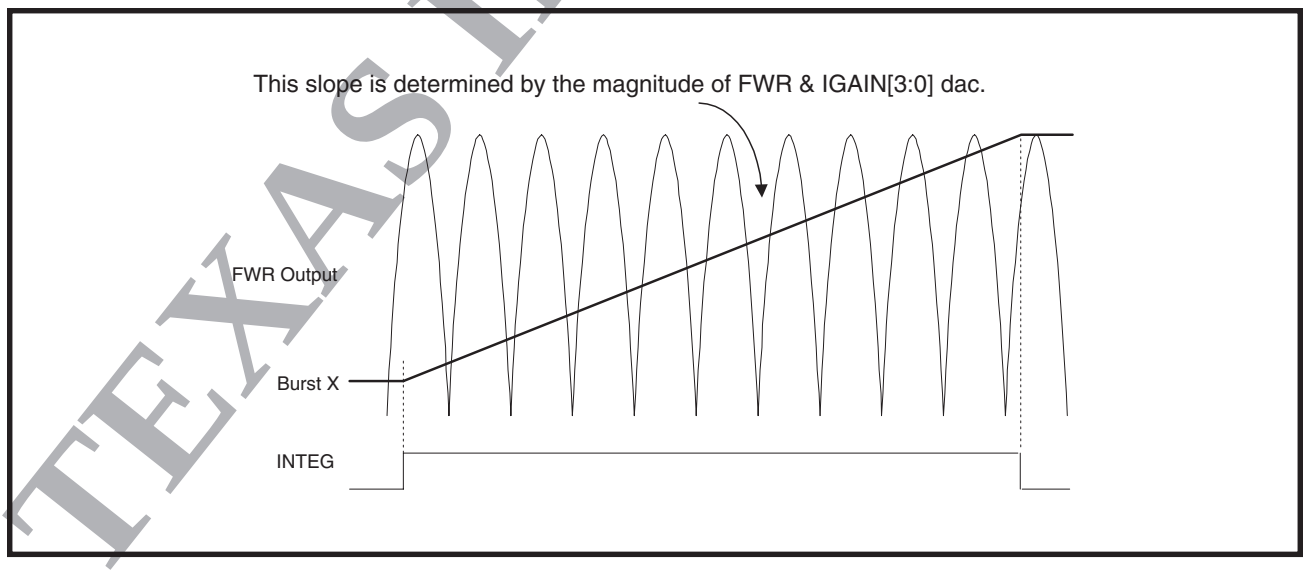


FIGURE 4: Servo Burst Acquisition

Burst Capture

Burst capture is controlled by the signal applied to the INTEG input pin and an internal counter. The first pulse on the INTEG input pin causes the A burst hold capacitor to be charged by the integrator. The capacitor charges for as long as the INTEG input is high. On the falling edge of the INTEG signal, the internal counter is incremented. The next 3 INTEG pulses will charge the B, C, and D, hold capacitors respectively. After the falling edge of the fourth INTEG, the counter is reset to zero and the burst capture sequence can be repeated. The counter is also reset when the $\overline{\text{RESET}}$ input transitions low.

The voltage level on each hold capacitor is buffered on top of the 0.3 V DC reference to create the A, B, C, and D output signals. A 1.4 V pp differential voltage at the DP/DN pins will result in 1.4 • (1.6 + 0.1 • IGAIN)+ 0.30 V. The MAXREF output pin is a nominal 3.0 V and is internally divided by 10 to create the DC baseline of 0.3 V. Note: A,B,C,D ouputs may not exceed MAXREF. To minimize any channel to channel mismatch it is recommended that the reset voltages be first measured and stored to be later subtracted from the burst voltages. Alternately by using a special servo calibration mode by setting FCS:SVCAL to 1 the reset voltage of each channel can be added to a reference voltage sum of which is roughly equal to MAXREF/2 and brought to the corresponding burst pin. This could then be used to calibrate the servo. In this mode no INTEG is necessary. Nominal voltage is MAXREF/2 = 1.5 V.

All four of the internal hold capacitors are discharged when the $\overline{\text{RESET}}$ input is driven low. The $\overline{\text{RESET}}$ input overrides the INTEG signal. INTEG and $\overline{\text{RESET}}$ are not gated with SG. To support embedded servo applications, a high performance area detecting servo demodulator circuit is provided. This circuit automatically calculates the time voltage integral of the signal a filter output. The servo burst amplitudes are measured by detecting the area underneath the pulses. The differential output at Filter out is first full wave rectified to produce a signal whose amplitude is proportional to the absolute value of the input differential signal. The resulting signal is then integrated over a period of time defined by the INTEG input pulse. The path from filter output to the integrator output is fully differential to minimize susceptibility to common-mode noise sources. All bursts are processed by the same rectifier, integrator, and gain stage so that channel-to-channel gain and offset mismatches are eliminated.

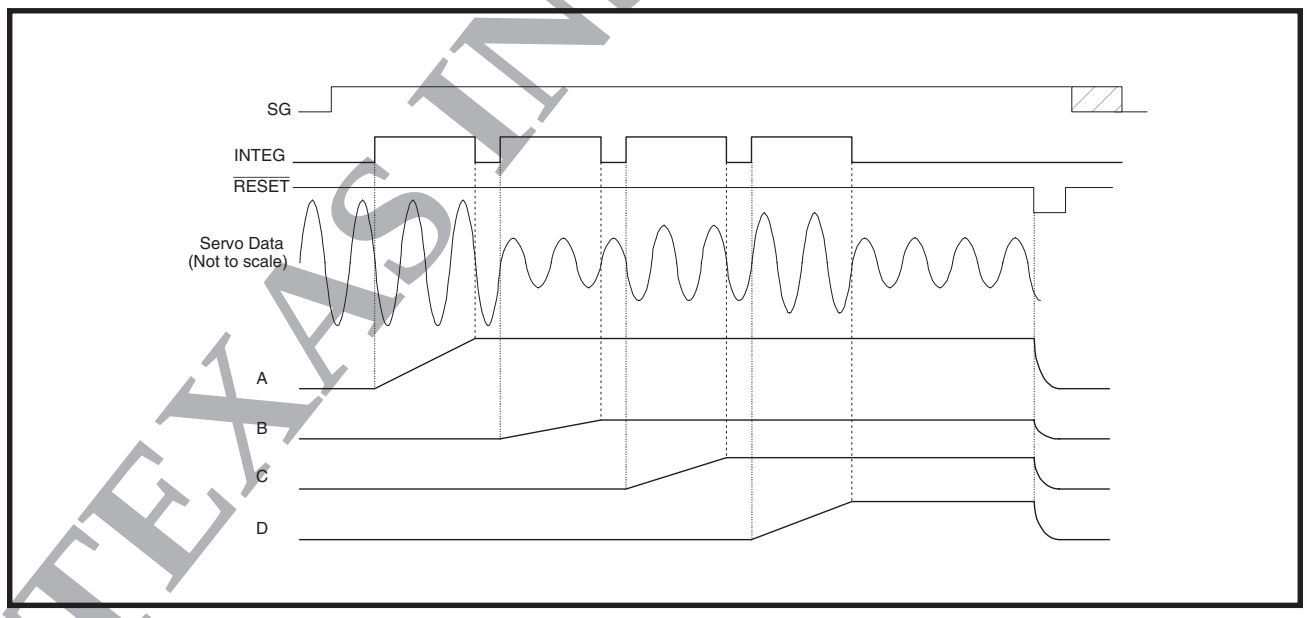


FIGURE 5: Servo Burst Capture Timing

FUNCTIONAL DESCRIPTION (continued)

QUALIFICATION CIRCUIT

This device utilizes two different types of pulse qualification, one for servo reads and the other for data reads.

QUALIFIER

Servo Read Mode

During servo reads (SG high) either a hysteresis or window or dibit type of pulse qualifier is used. The level qualification thresholds are set by a 6-bit DAC which is controlled by the LDS Register. The DAC is referenced to a fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable CM4:ALE does not affect this DAC's reference. The $\overline{RDS}$ and the PPOL outputs of the level qualifier indicate a qualified servo pulse and the polarity of the pulse, respectively. The $\overline{RDS}$ and PPOL outputs are only active when the SG input is high.

Dibit Qualifier Mode

(CM2:DIBDEN = 1; CM2:PDM = 0; CM2:DIBITPOL)

In the dibit qualifier mode, the normal Window Qualifier detected pulses, as described above, are further time interval qualified prior to clocking out a pulse at RDS. See the corresponding timing diagram of Figure 7. If a threshold qualified pulse is detected after a prolonged period of absence of pulses (this interval equal to the output pulse width of the internal Retriggerable One Shot, or Tr) the Retriggerable One Shot is triggered, but not the RDS output pulse. Then, if and only if a subsequent threshold qualified pulse of opposite polarity is detected within the Tr period, this second pulse is allowed to clock a pulse out at the RDS output, whose negative polarity asserted output pulse width is set by the Nonretriggerable One Shot. If another threshold qualified pulse occurs of the same polarity of a previous pulse which most recently triggered the Retriggerable One Shot, within the Tr interval, this one shot will retrigger so that its output pulse will be extended beyond this time by an additional Tr, and permit another opposite polarity pulse to clock a pulse out at RDS if it occurs within this new Tr period. Thus the dibit qualifier mode detects dibit pairs if the interval between the positive and negative polarity pulses of the dibit pulse pair is Tr or less. The first pulse of the dibit arms the detector, and the second clocks out the pulse at RDS if it was opposite in polarity from the first and within Tr of the first, and can be set the polarity of the first transition before Dibit detect signal by DIBITPOL bit.

If a continuous pulse stream (such as servo preamble) is encountered such that the interval between successive same polarity pulses is less than Tr, the Retriggerable One Shot will continuously retrigger so that the threshold qualified pulses of opposite polarity from those that are retriggering this one shot will repeatedly clock out pulses at RDS. The polarity that repeatedly retriggers the time discriminating Retriggerable One shot is that which occurred first after a period (> Tr) of absence of pulses prior to the continuous burst.

The dibit time interval discrimination pulse width Tr can be varied with the DBT[2:0] Register bits in ASYM. Implied frequency is the full cycle frequency whose period is 2x(Tr). The scaling is approximately a linear progression in terms of Tr.

Dibit Qualifier TR Test Output Mode

With DIBDEN = 1, PDM = 1, the dibit time discrimination interval Tr described above is output at the RDS output for test. Note that since RDS is normally used in servo mode, PDM should be set to 0 if DIBDEN = 1 for normal operation.

Data Read Mode

In data read mode (RG high), the same dual level qualifier as was used for servo reads, is used for ensuring pulse polarity changes during VCO sync field counting. The qualification thresholds are set by a 6-bit DAC which is controlled by or the LD Register. The DAC is referenced to a fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the CM4 Register does not affect the DAC's reference until the sync field count has been reached. The $\overline{RDS}$ and the PPOL outputs of the level qualifier are not active in data read mode. Pulse polarity transition count is performed in hysteresis mode only.

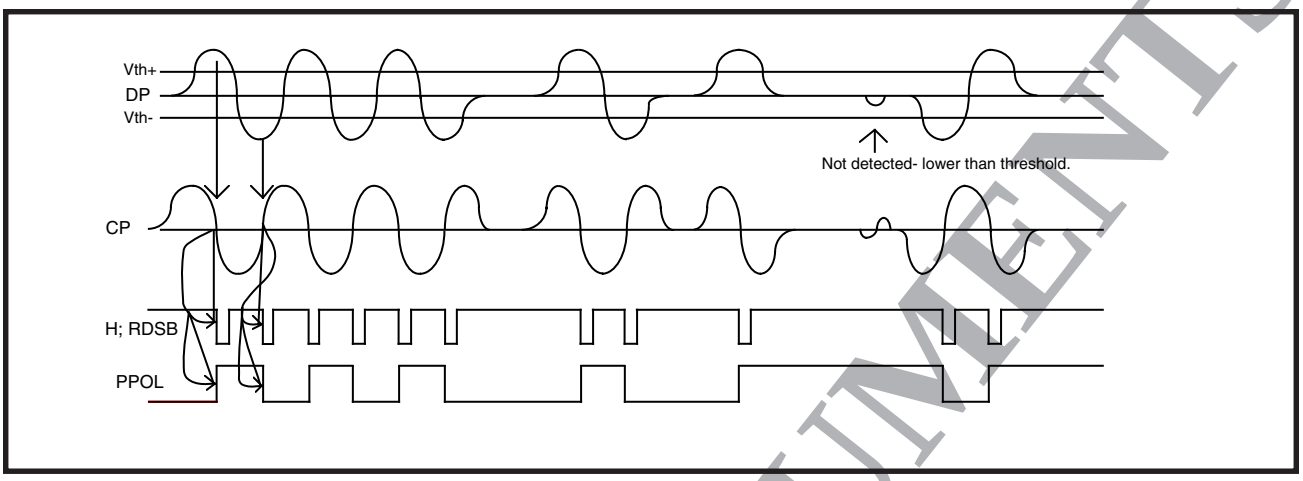


FIGURE 6: Window Qualifier

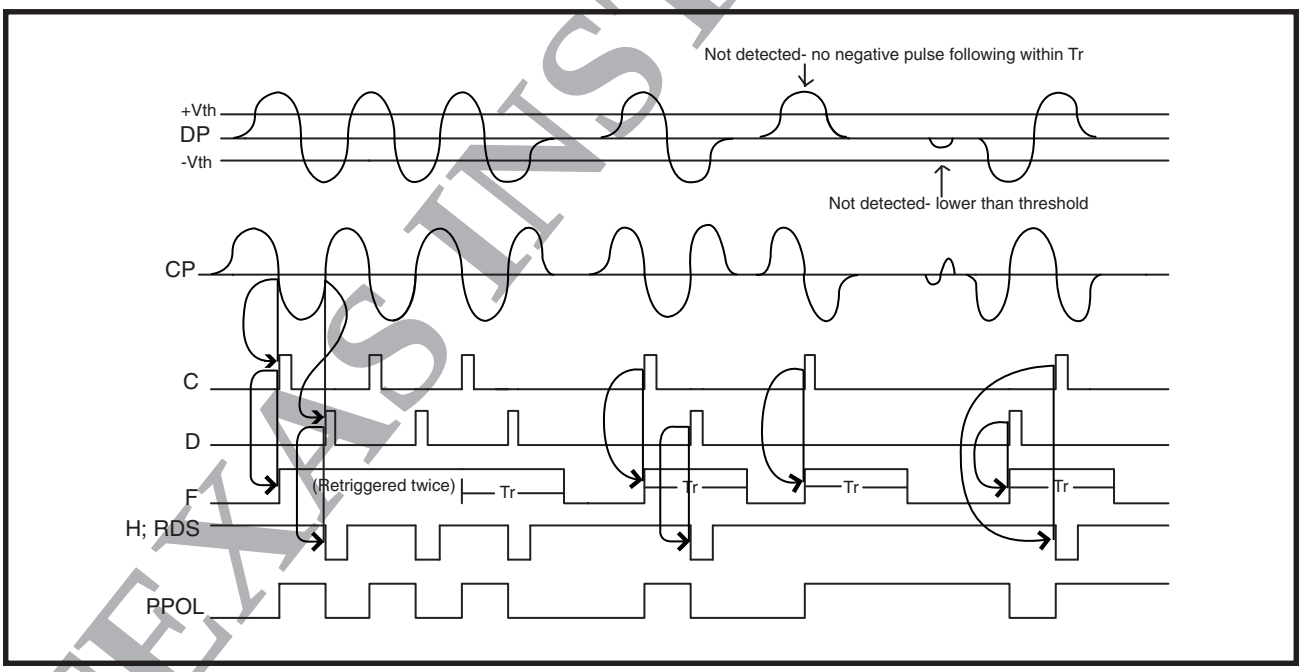


FIGURE 7: Dibit Qualifier Mode

PULSE QUALIFICATION CIRCUIT (continued)

3-Level Slicer

The determination of whether a sample is a "one" or a "zero" is performed by a dedicated, dual mode, threshold comparator (3-level slicer). The slicer's threshold levels are determined by the value, Lth, programmed in the LD Register. The fixed level threshold before the sync field count (SFC) has been reached will be 1.4 times the threshold level after SFC since this is the ratio of the peak signal to the sampled “1” signal amplitude for PR4. The dual mode nature of this comparator allows the selection of either symmetric fixed or independent self adapting (+) and (-) thresholds by programming the adaptive level enable CM4:ALE.

The adaptive reference allows the specification of the threshold value to be a percentage of an averaged peak value. When adaptive mode is selected, the fixed thresholds are used until SFC has been reached, then the adaptive levels are internally enabled. The time constant of a single pole filter that controls the rate of adaptation is programmable by the CM4:TC.

Baseline Offset

The baseline offset is included to compensate for the amplitude asymmetry of the incoming signal from the preamp. There are two modes of baseline offset available in this device - Mode 1 and Mode 2.

The baseline shift is introduced at the output of DP/DN filter output and therefore the AGC regulates the amplitude of the shifted signal. In this mode, there are two 8 bit registers, BLOD and BLOS, for data and servo mode, respectively. The magnitude of the negative shift is given by 2.5 mV • BLOSD,S[6:0] for the maximum of 317.5 mV, the magnitude of the positive shift is given by 2.374 • BLOSD + 11.654 for the maximum of 313.1 mV and the magnitude by BOSDP and BOSSP. The shifted signal is observable at TPH, $\overline{\text{TPH}}$ pins.

EPR4 VITERBI DETECTOR

The EPR4 channel dibit response is described by:

$$\text{EPR4}(D) = (1-D)(1+D)^2$$

where D denotes unit delay in the Z domain.

The sampled data signals coming out from the FIR filter are equalized to a PR4 response, attaining three separate signal levels: +1, 0, -1. To convert the PR4 waveform to EPR4 waveform, a (1 + D) filter is used. Data exiting the (1 + D) filter will now attain five separate signal levels: +2, +1, 0, -1, -2.

Figure 9 shows the state transition diagram of an EPR4 channel. The state variables denote the state of the write current in the magnetic head and the value on the transition edges are the channel outputs. Unlike a PR4 channel, the EPR4 channel cannot be interleaved into two independent (1-D), two state channels. To decode the state transitions from the channel outputs, an eight-state Viterbi detector is required.

The SSI 32P4103B implements a full eight-state EPR4 Viterbi trellis detector. To increase data rate, signal processing is interleaved such that signal processing is done at one half of the code rate.

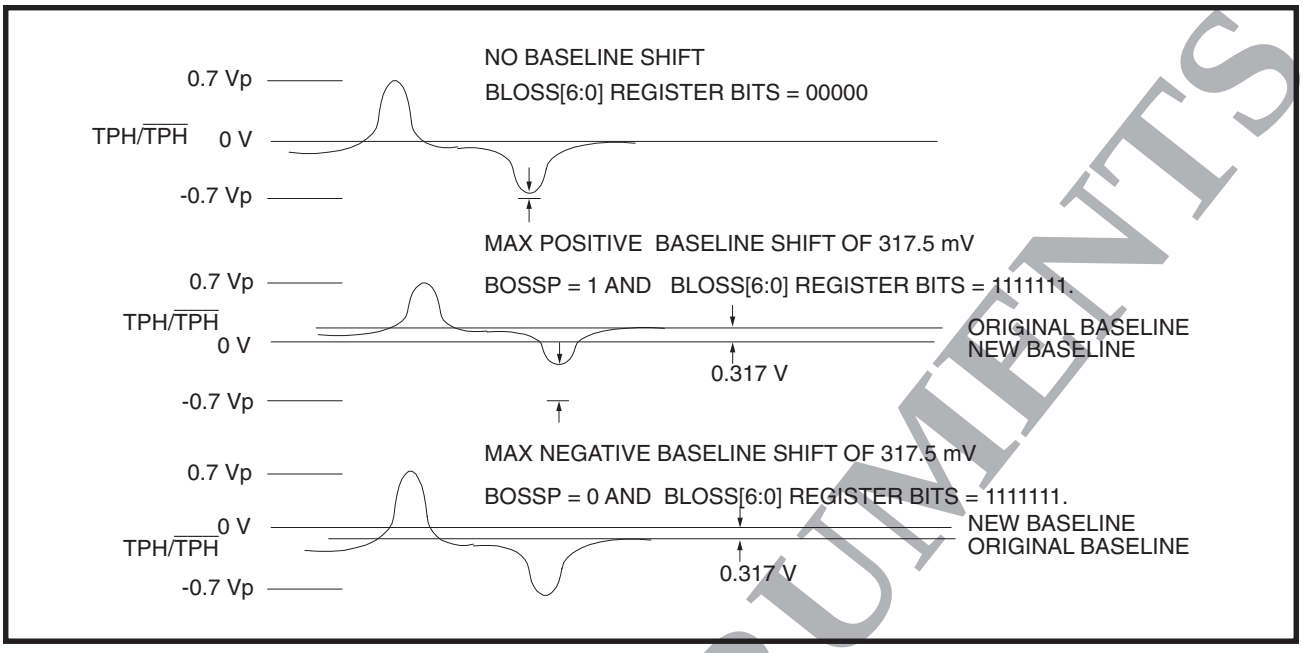


FIGURE 8: Baseline Offset Control in Servo Mode

EPR4 VITERBI DETECTOR (continued)

The Viterbi detector equations implemented in SSI 32P4103B are listed below:

$m_k(S0) = \max \{M00, M01\}$

$m_k(S1) = \max \{M10, M11\}$

$m_k(S2) = \max \{M20, M21\}$

$m_k(S3) = \max \{M30, M31\}$

$m_k(S4) = \max \{M40, M41\}$

$m_k(S5) = \max \{M50, M51\}$

$m_k(S6) = \max \{M60, M61\}$

$m_k(S7) = \max \{M70, M71\}$

where

$M00 = m_{k-1}(S0) + 0.5 - A,$
$M01 = m_{k-1}(S4) - y_k - A$

$M10 = m_{k-1}(S0) + y_k - A,$
$M11 = m_{k-1}(S4) + 0.5 - A$

$M20 = m_{k-1}(S1) + y_k - A,$
$M21 = m_{k-1}(S5) + 0.5 - A$

$M30 = m_{k-1}(S1) + 2y_k - 1.5 - A,$
$M31 = m_{k-1}(S5) + y_k - A$

$M40 = m_{k-1}(S2) - y_k - A,$
$M41 = m_{k-1}(S6) - 2y_k - 1.5 - A$

$M50 = m_{k-1}(S2) + 0.5 - A,$
$M51 = m_{k-1}(S6) - y_k - A$

$M60 = m_{k-1}(S3) + 0.5 - A,$
$M61 = m_{k-1}(S7) - y_k - A$

$M70 = m_{k-1}(S3) + y_k - A,$
$M71 = m_{k-1}(S7) + 0.5 - A$

In the above equations, mk and yk are the state metric values and the EPR4 sample values at time k. In each cycle, updates to the eight state metrics are required by selecting between two contesting values. These contesting values, M's, are computed by adding branch metrics values to existing state metrics. Branch metrics measure the probability of different state transitions in the trellis diagram and is formed by linear combinations of channel sample values, y's, and certain constant values. Each state metric update requires additions, comparisons and select operations and are thus known as ACS (Add-Compare-Select). In the above equations, a common mode term A is subtracted from each metric expression. This is necessary to avoid the metric build up.

Also note that in the expressions for metrics, the first subscript refers to the metric State and the second to the data being detected.

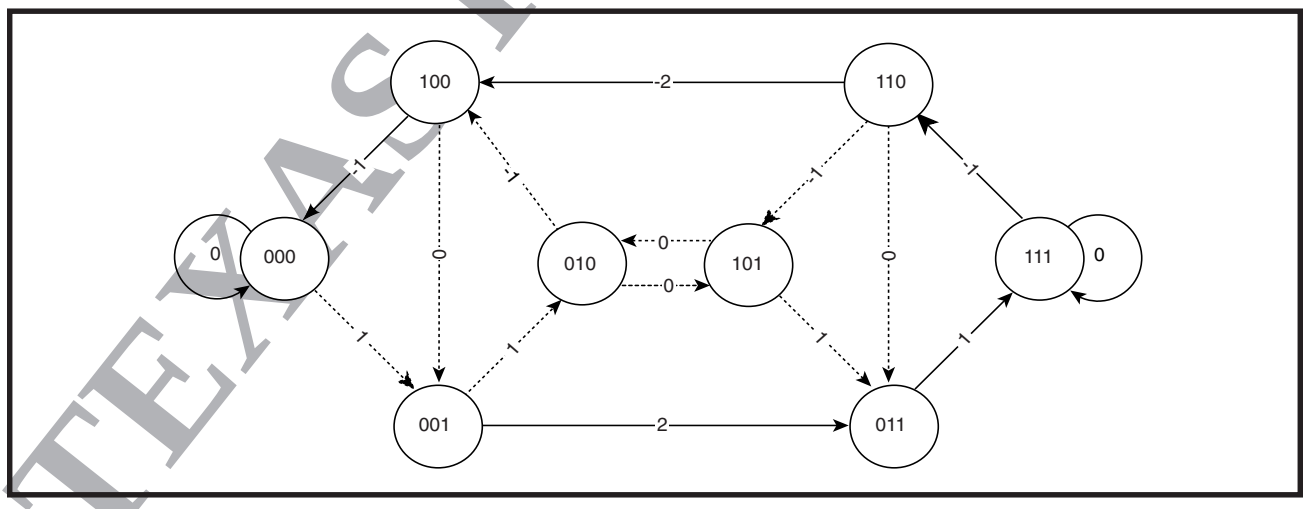


FIGURE 9: State Transition Diagram for EPR4 channel

VITERBI DETECTOR CIRCUIT

The EPR4 Viterbi detector is enabled only during read mode and only after the sync field count (SFC) has been achieved. The block diagram from the EPR4 Viterbi Detector is shown in Figure 10. This circuit has two significant blocks, one that feeds the other. The first block consists of the eight ACS (Add-Compare-Select) units and the second consists of the survival sequence registers. Each ACS unit stores and updates one of the eight state metrics, mk, every cycle as described by the equations described. To constrain the signal dynamic range, feedback normalizations are done as a common term, A, is subtracted from each metric. Each ACS unit will also determine which of the two incoming path metric values (M_{SB}) is larger. Every two clock cycles the ACS selection information is sent to its associated survival register as two-bits at a one-half rate. The signal processing through the ACS units is carried out in the analog sampled data domain to allow high speed and low power Viterbi detector implementation.

The survival register, on receiving the 2-bit selection information from its ACS unit, will mux in and shift the correct decoded data sequence from 1 of the 4 survival registers connected at its input. In SSI 32P4103B, each survival register is 12 bits long. In a noiseless channel, the outputs of all eight survival registers should give identical 16/17 encoded data. However, in a noisy environment, the outputs of these survival register could be different. To derive the optimum detected data each cycle, the data outputs from the survival register having the largest state metric are selected and are fed to the sync pattern detector and decoder.

The branch metric constant in the Viterbi equations are derived from an on-chip bandgap voltage reference. The same bandgap is also used to define the equalization targets for the FIR block. Therefore, these branch metric constants will track the Viterbi

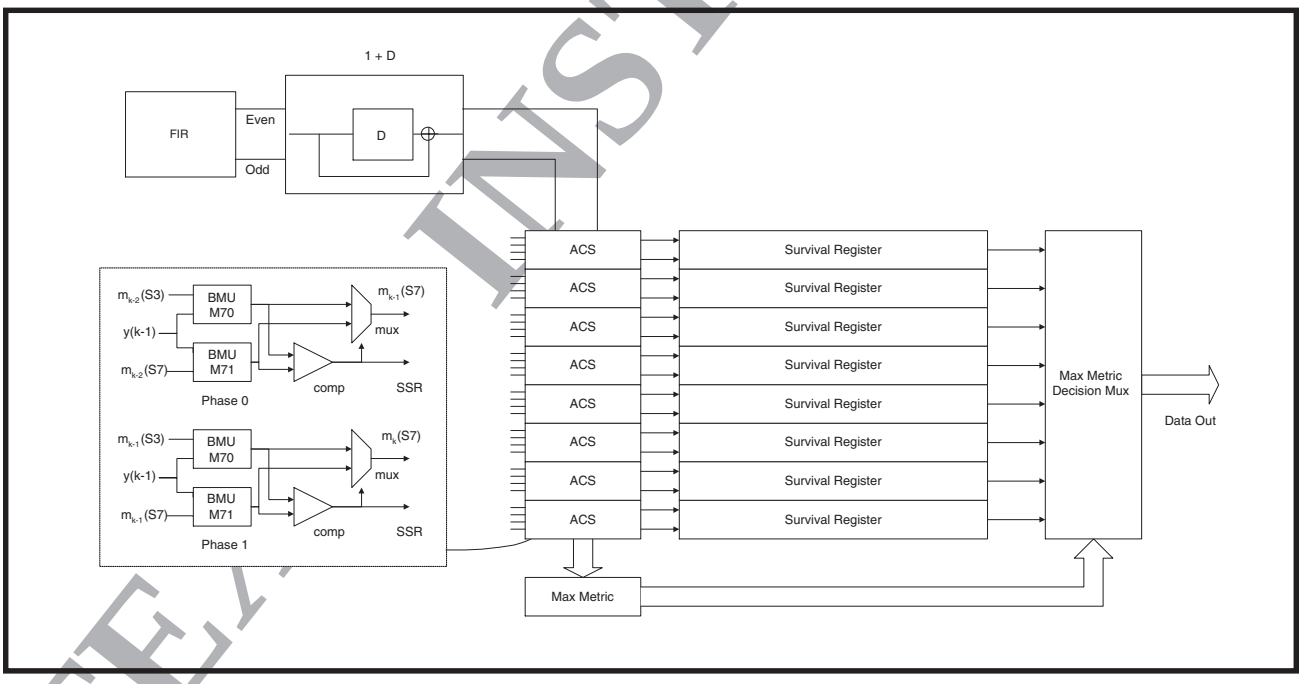


FIGURE 10: EPR4 Viterbi Block Diagram with the 1 + D Filter

VITERBI DETECTOR CIRCUIT (continued)

equalization targets with varying operating conditions. The branch metric constants are formed by multiplying integer values with Vpk and Vnk. The following table shows the relationship between the constant values in the Viterbi equations above and Vpk and Vnk.

Constant	Voltage
-1.5	-3 • Vnk
0.5	Vpk

Vpk and Vnk, are set as percentages of the '+1','-1" PR4 equalization targets by two 4-bit DACs controlled by bit D7:D4 and D3:D0 in serial port register VEPR4 Register according to the following equation:

$$Vnk = 0.5 \bullet \{1.0 \pm (D7:D4) \bullet 2.5\%\}$$

$$Vpk = 0.5 \bullet \{1.0 \pm (D3:D0) \bullet 2.5\%\}$$

where (D7:D4) and (D3:D0) are in two's complement form

DEFECT SCAN MODE

In this mode of operation a pair of raw decisions are generated by the 3-level slicer at the FIR output. The threshold for this slicing can be adjusted via Data Level Threshold Register (LD). When Defect scan mode is activated, the timing recovery loop is forced to accept only ±1 decisions and thus is not affected by the Data Level Threshold Register setting. Note, however, that the AC coupler reference must be selected to be the continuous time output, since there are no '0' updates from the slicer. Therefore, ser the ACSWT bit to 1 for defect scan mdoe.

This mode can be used to scan the disk media for defects as follows. The user can write 2T patterns in the area under test by putting the chip in write mode while holding the NRZ interface low. In read mode, the user should activate the defect scan mode. Note that, because the channel is in defect scan mode, there is no sync pattern detection search after assertion of SFC. A data flag can be enabled by setting DR:DSB. When enabled, the NRZ1 pin is toggled at sync field count as set by SLC:SFC.

For defect scan testing, a VCO synchronization pattern (1,1,-1,-1) may be written onto a track, then read back and checked for low amplitude pulses. The synchronization pattern is written by asserting WG and holding the NRZ input pins low for the duration of the write sequence. To read the pattern and check for low amplitude pulses, set the defect scan test mode using the N:DSCAN bit. When RG is asserted, the data separator PLL will lock to the preamble pattern, and the NRZ pins will go to a low state. After sync field count, low amplitude pulses will be detected and a "1" will be transmitted to the NRZ7 pin. The "1" will be held for one RCLK cycle, so that it can be detected by the controller. In the presence of a continuous error condition, the NRZ7 output will produce a continuous 1. The normal byte-wide read mode NRZ setup and hold times apply to NRZ7 in the defect scan mode.

The $\overline{SBD}$ is asserted low after vcolock is generated, and is held until RG goes low. $\overline{SBD}$ to RCLK rising, TSDL spec applies to this mode.

PROGRAMMABLE FILTER CIRCUIT

General Description

The on-chip, continuous time, low pass filter has register programmable cutoff and boost settings, and provides both normal and differentiated outputs. It is a 7th order filter that provides a 0.05° phase equiripple response. The group delay is relatively constant up to twice the cutoff frequency. For pulse slimming, a two zero programmable boost equalization is provided with no degradation to the group delay performance. The differentiated output is created by a single-pole, single-zero differentiator. The filter zeros can be adjusted asymmetrically about zero to compensate for MR head slope asymmetry. The asymmetry is adjusted using the FBS:FGD bits.

The programmable bandwidth and equalization characteristics of the filter are controlled by 3 internal DACs(FC,FB and FGD) in data mode and 2 internal DACs(FCS and FBS) in servo mode. The registers for these DACs are programmed through the serial port. The current reference for the DACs is set using a single external resistor connected from pin RX (=10.2 kΩ, 1%) to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. This establishes excellent temperature stability for the filter. The cutoff and boost values for servo reads are automatically switched when servo mode is entered.

The filter transfer function is normalized to 1.0 rad/s and given below:

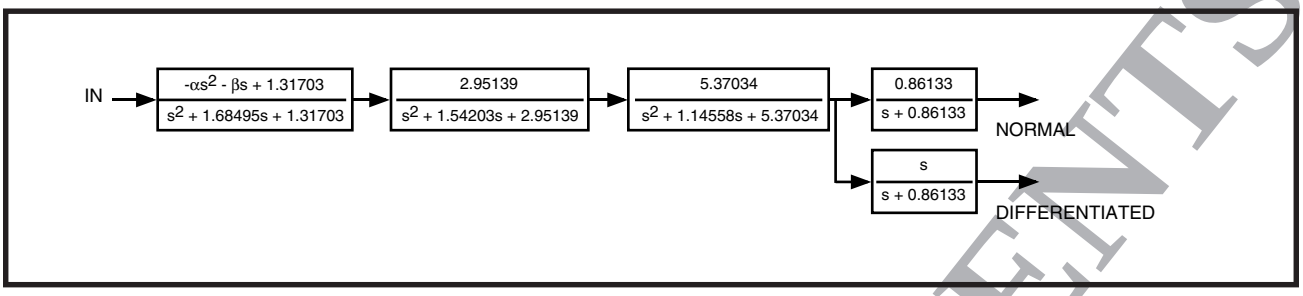


FIGURE 11: Filter Transfer Function

Shown also are theoretical magnitude response at no boost and 15 dB boost with $\Delta\%$ = 0%, and group delay response at $\Delta\%$ = -30%,0% 30% with no boost.

Alpha and the boost in dB are related by:

$$\alpha = 1.31703 \bullet (10^{dB/20} - 1)$$

Beta and $\Delta\%$ are related by: $\beta = 0.04183 \bullet \Delta\%$.

To denormalize the response to fc multiply the frequency by 2 pF, and divide the group delay response by 2 pF. For example if fc = 30 MHz, multiply the frequency axis by $1.885 \bullet 10^8$ for rad/s conversion or by $30 \bullet 10^6$ for Hz conversion. For the group delay, divide the delay numbers by $1.885 \bullet 10^8$. The delay of 3.18 s translates to 16.87 ns.

Five definitions are introduced for the discussion below:

Cutoff Frequency: The cutoff frequency is the -3 dB low pass bandwidth with no boost & group delay equalization, i.e. $\alpha = 0$ and $\beta = 0$.

Actual Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha = 0$ and/or $\beta \neq 0$

Alpha Boost: The amount of peaking in magnitude response at the cutoff frequency due to $\alpha = 0$ and without group delay equalization. In general, the actual boost with group delay equalization is higher than the alpha boost. However, with >3 dB alpha boost, the difference is minimal.

Group Delay $\Delta\%$: The group delay $\Delta\%$ is the percentage change in absolute group delay at DC with respect to that without equalization applied (β =0)

Group Delay Variation: The group delay variation is the change in group delay from DC to the cutoff frequency.

Cutoff Control

The programmable cutoff frequency from 10 to 64 MHz is set by the 7 bit linear FC DAC. The filter cutoff is set by the Data Cutoff Register in non-servo mode and is set by the Servo Cutoff Register in servo mode. The cutoff frequency is set as:

$$FC(MHz) = FC \bullet 0.49586 + 1.00219$$
$$18 \leq FC \leq 127.$$

The filter cutoff (FC) is defined as the -3 dB bandwidth with no boost applied. When boost/equalization is applied, the actual -3 dB point will move up. The ratio of actual -3 dB bandwidth to the programmed cutoff is tabulated below as a function of applied boost at the normalized frequency of 1.0 rad/s To denormalize, multiply frequency by 2 pF.

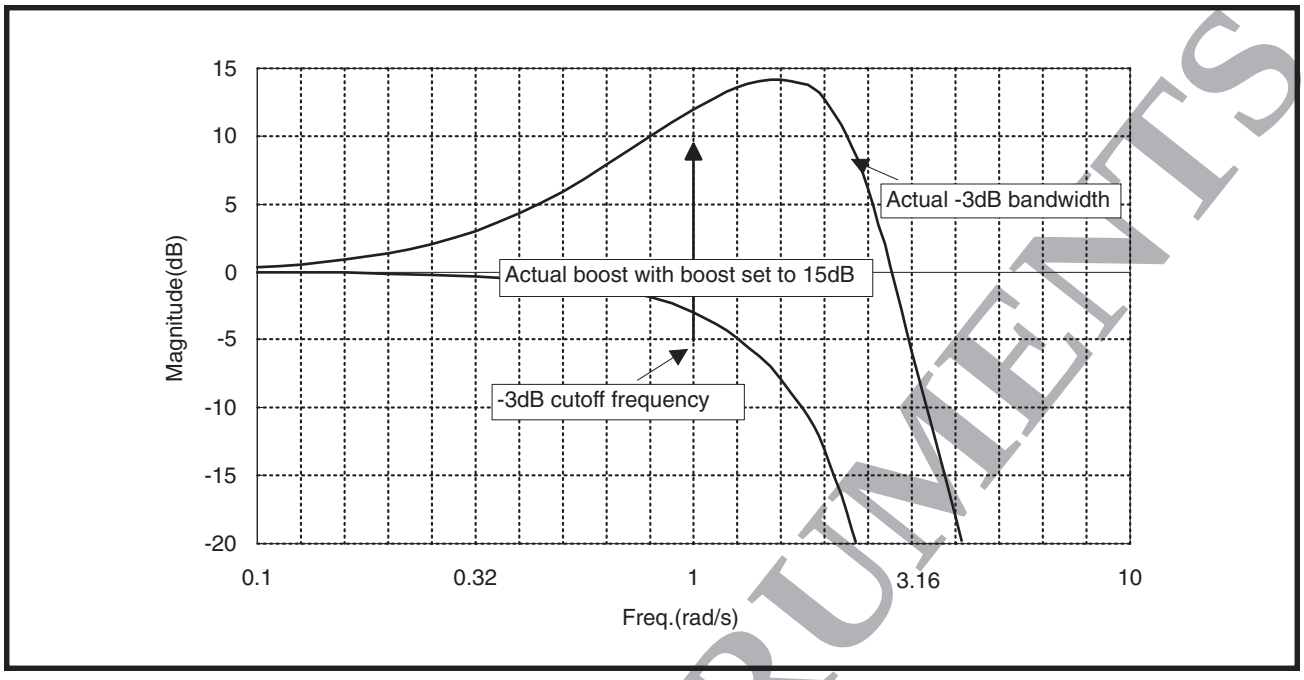


FIGURE 12: Filter Magnitude Response (Δ% = 0)

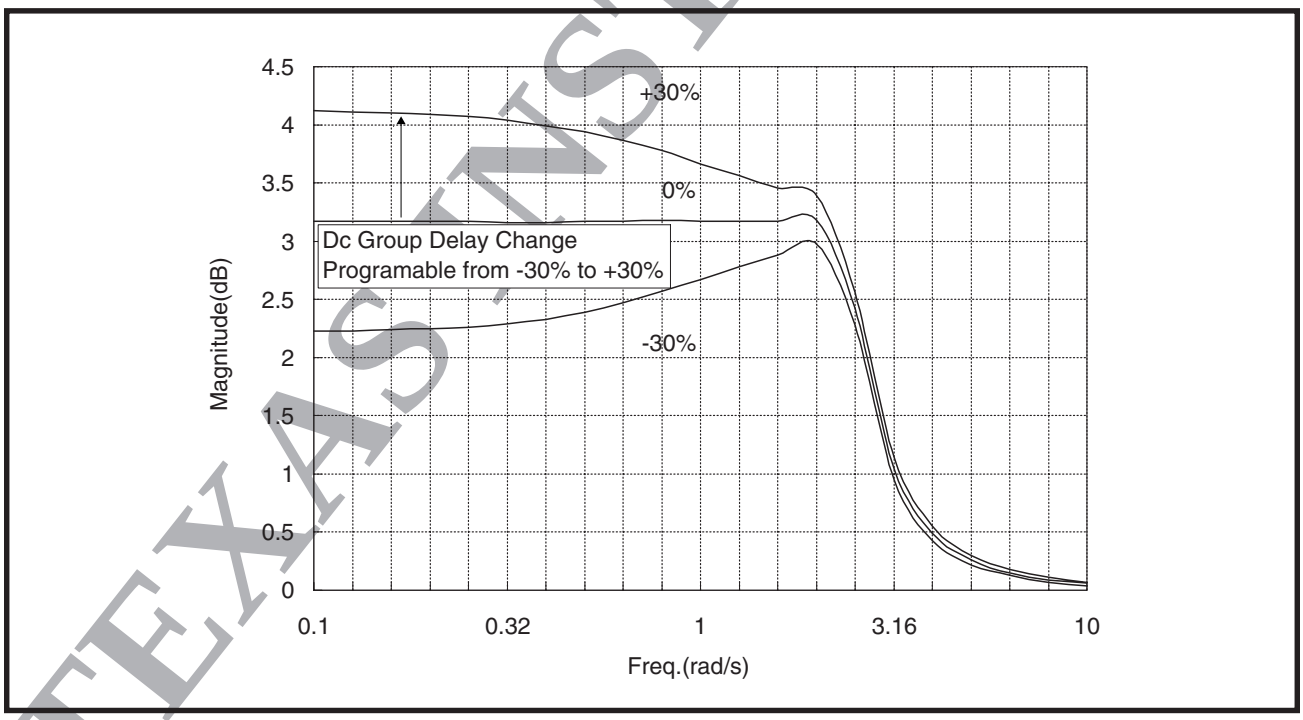


FIGURE 13: Filter Group Delay Response (Boost = 0 dB)

PROGRAMMABLE FILTER CIRCUIT (continued)

TABLE 1: Filter Magnitude Response

Freq. (rad/s)	Magnitude						
	Bst = 0db	3db	6db	9db	11db	13db	15db
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0
0.10	-0.03	0.00	0.05	0.12	0.19	0.26	0.36
0.20	-0.13	0.02	0.21	0.48	0.72	1.00	1.35
0.30	-0.28	0.04	0.47	1.04	1.52	2.08	2.74
0.40	-0.49	0.07	0.80	1.73	2.48	3.35	4.32
0.50	-0.75	0.10	1.18	2.51	3.53	4.67	5.92
0.60	-1.07	0.13	1.59	3.30	4.58	5.97	7.44
0.70	-1.45	0.15	2.00	4.08	5.59	7.17	8.83
0.80	-1.90	0.13	2.38	4.80	6.50	8.25	10.05
0.90	-2.42	0.08	2.71	5.44	7.30	9.19	11.1
1.00	-3.01	-0.01	2.99	5.99	7.99	9.99	11.99
2.00	-13.13	-4.67	0.81	5.22	7.84	10.31	12.66
3.00	-35.67	-22.21	-15.71	-10.88	-8.09	-5.52	-3.08

TABLE 2: Filter Group Delay Response w/Boost = 0 dB

Freq. (rad/s)	Delay (sec)						
	-30%	-20%	-10%	0%	10%	20%	30%
0.00	-2.22	-2.54	-2.86	-3.18	-3.49	-3.81	-4.13
0.10	-2.23	-2.54	-2.86	-3.17	-3.49	-3.81	-4.12
0.20	-2.25	-2.54	-2.85	-3.17	-3.48	-3.79	-4.09
0.30	-2.28	-2.55	-2.85	-3.16	-3.48	-3.78	-4.04
0.40	-2.33	2.56	-2.85	-3.17	-3.47	-3.76	-3.99
0.50	-2.39	-2.59	-2.86	-3.17	-3.47	-3.74	-3.94
0.60	-2.45	-2.62	-2.86	-3.17	-3.48	-3.73	-3.89
0.70	-2.52	-2.65	-2.87	-3.18	-3.48	-3.71	-3.78
0.80	-2.57	-2.67	-2.88	-3.18	-3.47	-3.68	-3.78
0.90	-2.62	-2.69	-2.88	-3.17	-3.46	-3.65	-3.72
1.00	-2.67	-2.71	-2.88	-3.17	-3.45	-3.62	-3.66
2.00	-2.98	-2.94	-2.95	-3.18	-3.41	-3.42	-3.39
3.00	-1.16	-1.13	-1.10	-1.27	-1.43	-1.41	-1.37

PROGRAMMABLE FILTER CIRCUIT (continued)

TABLE 3: Ratio of Actual -3 dB Bandwidth to Cutoff Frequency.

Boost (dB)	Group delay						
	±0%	±5%	±10%	±15%	±20%	±25%	±30%
0	1.00	1.01	1.06	1.16	1.31	1.47	1.62
1	1.19	1.21	1.28	1.38	1.50	1.62	1.74
2	1.49	1.51	1.56	1.63	1.71	1.79	1.87
3	1.79	1.80	1.83	1.87	1.91	1.96	2.01
4	2.03	2.04	2.05	2.07	2.09	2.11	2.14
5	2.20	2.20	2.21	2.22	2.23	2.24	2.25
6	2.32	2.32	2.33	2.33	2.34	2.34	2.35
7	2.42	2.42	2.42	2.43	2.43	2.44	2.44
8	2.51	2.51	2.51	2.51	2.51	2.52	2.52
9	2.59	2.59	2.59	2.59	2.59	2.59	2.59
10	2.66	2.66	2.66	2.66	2.66	2.66	2.67
11	2.73	2.73	2.73	2.73	2.73	2.73	2.73
12	2.80	2.80	2.80	2.80	2.80	2.80	2.80
13	2.86	2.86	2.86	2.86	2.86	2.86	2.86
14	2.93	2.93	2.93	2.93	2.93	2.93	2.93
15	3.00	3.00	3.00	3.00	3.00	3.00	3.00

TABLE 4: Actual Boost vs Alpha Boost & Group Delay Change at w = 1.0 rad/s

Boost (dB)	Group delay						
	±0%	±5%	±10%	±15%	±20%	±25%	±30%
0	0.00	0.11	0.42	0.89	1.47	2.12	2.81
1	1.00	1.09	1.33	1.72	2.21	2.76	3.36
2	2.00	2.07	2.27	2.58	2.99	3.45	3.97
3	3.00	3.05	3.21	3.47	3.80	4.19	4.63
4	4.00	4.04	4.17	4.38	4.65	4.97	5.34
5	5.00	5.03	5.14	5.30	5.52	5.79	6.10
6	6.00	6.03	6.11	6.24	6.42	6.64	6.89
7	7.00	7.02	7.09	7.19	7.34	7.51	7.72
8	8.00	8.02	8.07	8.15	8.27	8.41	8.58
9	9.00	9.01	9.05	9.12	9.22	9.33	9.47
10	10.00	10.01	10.04	10.10	10.17	10.27	10.38
11	11.00	11.01	11.03	11.08	11.14	11.21	11.30
12	12.00	12.01	12.03	12.06	12.11	12.17	12.24
13	13.00	13.01	13.02	13.05	13.09	13.14	13.19
14	14.00	14.00	14.02	14.04	14.07	14.11	4.15
15	15.00	15.00	15.01	15.03	15.06	15.09	15.12

Boost Control

The programmable alpha boost from 0 to 15 dB is set by the 7 bit linear FB DAC in data mode or 2 bit linear FBS DAC in servo mode. The alpha boost in data mode is set as:

$$\text{Boost(dB)} = 20\log(-0.0000337 \bullet FB \bullet FC + 0.043448 \bullet FB + 1) \quad 0 \le FB \le 127$$

The programmed alpha boost is the magnitude gain at the cutoff frequency with no group delay equalization. When finite group delay equalization is applied, the actual boost is higher than programmed alpha boost. However, the difference becomes negligible when the programmed alpha boost is >3 dB. The table below tabulates the actual boost at $\omega = 1.0$ as function of the applied alpha boost & group delay equalization.

In servo mode, the 2-bit FBS Register controls the boost as :

$$\text{Boost(dB)} = FBS \bullet 3.0.$$

That is, the boost in servo mode can be changed in 2 dB steps from 0 to 6 dB.

Group Delay Equalization

The group delay Δ% can be programmed between -30% to +30% by the 6-bit linear FGD DAC. The FGD Register holds the 6-bit DAC control value. The group delay Δ% is set as:

$$\text{Group Delay } \Delta\% = 0.9783 \bullet (FGD4{:}0) - 0.665\%, \text{ where } FGD5 = \text{sign and } 0 \le FGD[4{:}0] \le 31.$$

The group delay Δ% is defined to be the percentage change of the absolute group delay due to equalization from the absolute group delay without equalization at DC. Tabulated below is the normalized group delay response as a function of β at 0 dB and 15 dB boost. To denormalize to f, multiply frequency and divide the delay by 2 pF. Note that Δ% is not dependent on alpha setting; the group delay variation is. Shown in Table 5 is the group delay at boost set to 15 dB. For the boost = 0 dB case see Table 2.

TABLE 5: Filter Group Delay Response (Boost = 15 dB)

Freq. (rad/s)	Delay (sec)						
	-30%	-20%	-10%	0%	10%	20%	30%
0.0	-2.22	-2.54	-2.86	-3.18	-3.49	-3.81	-4.13
0.1	-2.35	-2.62	-2.90	-3.17	-3.45	-3.73	-4.00
0.2	-2.63	-2.80	-2.99	-3.17	-3.35	-3.53	-3.71
0.3	-2.90	-2.98	-3.07	-3.16	-3.26	-3.34	-3.43
0.4	-3.08	-3.11	-3.14	-3.16	-3.19	-3.22	-3.24
0.5	-3.20	-3.19	-3.18	-3.17	-3.16	-3.14	-3.14
0.6	-3.26	-3.23	-3.20	-3.17	-3.14	-3.11	-3.09
0.7	-3.28	-3.25	-3.21	-3.18	-3.14	-3.10	-3.07
0.8	-3.29	-3.25	-3.22	-3.18	-3.14	-3.10	-3.06
0.9	-3.28	-3.25	-3.21	-3.17	-3.13	-3.10	-3.06
1.0	-3.27	-3.24	-3.20	-3.17	-3.13	-3.09	-3.06
2.0	-3.22	-3.21	-3.20	-3.18	-3.17	-3.15	-3.14
3.0	-1.29	-1.28	-1.28	-1.27	-1.26	-1.25	-1.25

FUNCTIONAL DESCRIPTION (continued)

INTERNAL AC COUPLING

The conventional ac coupling at the filter/qualifier interface is now replaced by a pair of feedback circuits, one for the normal and one for the differentiated filter outputs. The offset of each of the filter outputs are sensed, integrated, and fed back to the filter output stage. The feedback loop forces the filter output offset nominally to zero. In the normal read mode (LOWZ = 0), the integration time constant is set at 6 μs until the internal pulse counter reaches SFC. The operation of the counter is discussed in more detail in the "Acquisition of DS VCO Sync" section. When the counter reaches SFC, the offset sensing is switched to the sampled data processor (SDP) and the time constant is reduced to 125 ns (effectively 250 ns due to the fact that zero's only occur at less than a half of the time during equalizer training). The SDP generates an offset voltage by sampling only the zeros that are qualified in the 3-level slicer. This ensures that the sampled zero voltage level, not the filter output, will be offset free.

When LOWZ = 1, the integration time constant is reduced to roughly 300 ns to quickly absorb the dc offset of the filter. The switch-over from continuous to sampled data can be disabled by setting PD:ACSWT = 1. In this case the ac coupling will continue to derive offset from continuous filter output.

The integration time constant is increased by a factor of 4, to 0.5 μs, after the synch byte has been detected, to make the offset correction less dependent on data pattern. Note that the effective time constant is greater than 1.0 μs again due to the fact that the zero's only occur less than 50% of the time, depending on the data pattern.

The integration time constant is reverted back to its original value in the event of thermal asperity, if the fast offset nulling bit(MISC1:FOSNUL = 1) is set, on the falling edge of TAD signal till the end of Hi-Y period.

QASYM QUALITY FACTOR

Amplitude asymmetry quality factor, Qasym, is generated by sampling all "ones" and lowpass filtering them with a time constant set by bits 5,6 of CM4 Register. In the presence of amplitude asymmetry, the average of all "ones" will be a good indication of amplitude asymmetry. This is then buffered and differentially multiplexed to the ATO buffer. The differential signal is converted to a single-ended signal referenced to an internally generated reference voltage Vref = Maxref/2 = 1.6 V nominally. The time constant is doubled at SFC.

The amplitude asymmetry of the incoming read signal can be monitored at the ATO pin when selected by the ASEL bits in the PD Register and can be used as a guide to setting MR element currents in the preamp.

Qasym can be placed in hold mode after the training sequence by setting the FRZQASM bit in CM4 and will hold its value for several microseconds in hold mode.

Also the asymmetry measure can be used to modify the Data Level Threshold (3-level slicer) and EPR4 constants via serial port control. This correction of the Data Level Threshold and EPR4 constants can enabled by setting CM4:QalvlEN and FIR2:QaeprEN, respectively. Also, the asymmetry correction magnitude is programmable via a pair of 3bit DACs, CM4:QaLVL and FIR2:QaEPR.

ASYMMETRY CANCELLATION CIRCUIT

A circuitry is included between the AGC amplifier and the continuous time filter input to take out the amplitude asymmetry. The cancellation is performed by squaring the input signal and then subtracting it from the signal. The extent of cancellation is controlled by ASYM(3:0) and the polarity by ASYMP bits in the ASYM Register. It is designed to cancel 2α% of amplitude asymmetry, where α = DAC setting between 0 and 15. Thus the amplitude asymmetry of up to 30% can be canceled by this circuitry. The recommended use of this circuitry is to do a rough adjustment with it against amplitude asymmetry and let the QaeprEn and QaEPR bits mentioned above do the remaining cancellation.

ADAPTIVE EQUALIZER CIRCUIT

The purpose of the adaptive equalizer is to adjust the KM1 value so as to force "zero" samples to zero volts. This modifies the pulse shape of an ideal PR4 waveform.

Up to 7 dB of cosine equalization for fine shaping of the incoming read signal to the PR4 target is provided by a 5 tap, sampled analog, transversal filter. There are basically two modes of operations: One is to use the self adapting feature of the equalizer and the other to force a fixed symmetrical coefficient from the serial port. This mode selection is controlled by AEE bit in SLC Register.

The adaptive equalizer zero forcing algorithm adjusts the KM1 (inner tap coefficients) gain by integrating the equalization error of “zero” samples. After sync field count is reached, with SLC:AEE = 1, the FIR equalizer will adapt to a special training pattern (NRZ:91A0h; Encoded:12324h). Adaptation can be left enabled past sync byte detection into the user data by appropriately setting SLC:AED. If the adaptive equalizer is enabled over data the integration time constant can be increased by 7 times for lower noise sensitivity by setting SLC:AEGS. When a training pattern is used along with the KM1 preset function the adaptive equalizer integration time constant may also be increased 7x in the training fields by setting DRC:LOWEQG. It should be noted that the KM1 preset setting of the FIR1:KM1PS will be used as a starting point for adaptation. The setting of 0000 for FIR1:KM1PS means that adaptation starts from zero gain setting for KM1. Only negative KM1 gain settings can be entered into the serial port.

With SLC:AEE = 0, the equalizer will simply reflect the gain setting at KM1 bits and remain fixed.

Additionally, there is a mode which will initiate A/D conversion of the tap weight following the adaptation for readout to the serial port. This mode can be selected by setting SLC:AEQADC to 1. This mode can be most useful in applications where overhead imposed by training field must be minimized. In this mode the channel would write consecutive training bytes in the user data section following the sync byte(s) and simply read out the A/D converted 4 bits word in the FIR1 Register after RG deassertion. The A/D conversion will commence at the end of read and will take at most 16 µs. The A/D converted word (4 bits) is made available in FIR1[7:4] and reset upon serial port read. This A/D output may then be used as the KM1 preset value (FIR1:KM1PS).

The multiplier coefficients for the adaptive taps can be held for up to 10 µs typical if the EQHOLD input is brought high in read mode after sync byte detect has occurred.

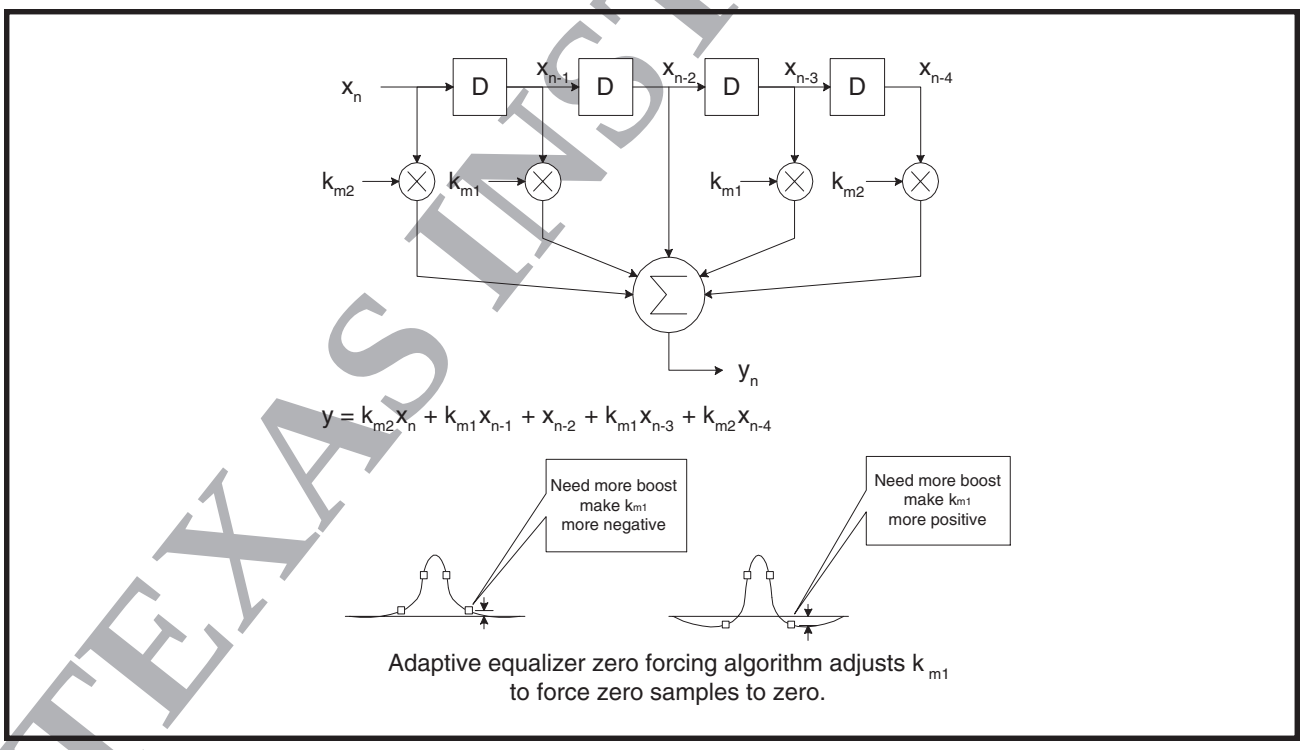


FIGURE 14 : Adaptive Equalizer Block Diagram

FUNCTIONAL DESCRIPTION (continued)

DIGITAL CHANNEL QUALITY MONITOR

The primary purpose of the Channel Quality Monitor, or CQM, is to monitor the channel quality and facilitate the tuning of user controlled parameters. Additionally, it can be used to adjust the setting for BLOS by monitoring the number of AGC comparator outputs by setting CQM3:CQMCTRL=100b.

In the primary mode, any one of three types of quality factors can be selected by appropriately setting CQM3:CQMCTRL. When set = x01b, the CQM counter is incremented whenever an inconsistency maxmet state transition event is found in the EPR4 detector. When set to x10, the CQM counter is incremented whenever the M2SB(2nd MSB) of maxmet decision appropriately delayed to match the delay thru the Survival Path Reg. does not agree with the Sur.Path Register output. When set to x11, the CQM counter is incremented whenever the MSB of maxmet decision appropriately delayed to match the delay thru the Sur.Path.Reg. does not agree with the Sur.Path Register output. In all three case, the count is integrated by a 16-bit counter.

These quality factors will have different correlation to the actual BER. In all cases, however, the lower the count, the better the BER.

To tune the channel, the user may observe the count and adjust parameters in the direction of reducing this count.

The count begins when either the sync byte detect (SBD) or the sync field count (SFC) signal is detected, as programmed by CQM3 bit 2. A timing diagram of the operation is shown below in Figure 15: CQM Timing Diagram.

When RG is de-asserted, the 16-bit counter value is written back to registers CQM1[7:0] & CQM2[7:0], and can be read out through the serial port. The action of reading the CQM1 Register resets the 16-bit counter. Therefore CQM2 should be read prior to CQM1.

In the additional mode, the full-wave rectified AGC signal peaks are detected and fed to the CQM counter. The count begins on the Servo hold and continues until the first rising edge of the Strobe signal. This mode is intended to be used in BLOS adjustment.

Table 6 summarizes the CQM control bits in CQM mode and normal operation (where the CQM is disabled).

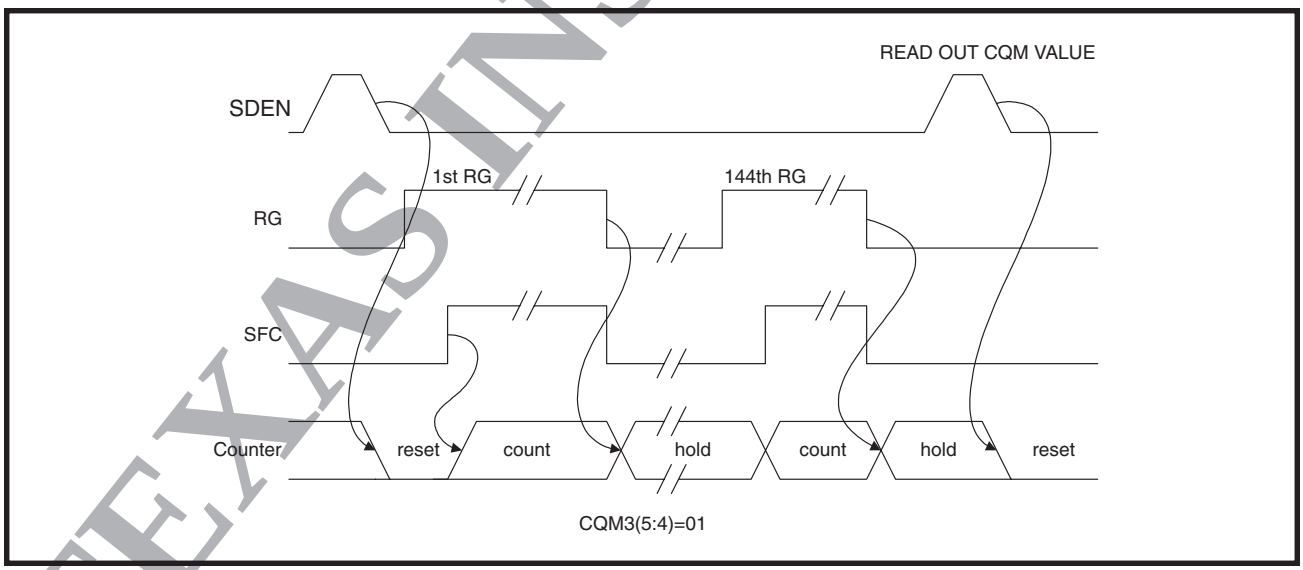


FIGURE 15 : CQM Timing Diagram

TABLE 6: CQM Modes of Operation

Serial Port Register	CQM mode setting	Utility
CM3[2-0]	Mode selection	When SURVSEL = 0; 000 = Disable CQM function, x01 = Counts Maxmet inconsistency events in CQM counter, x10 = Counts Maxmet M2SB inconsistency events in CQM counter, x11 = Counts Maxmet MSB inconsistency events in CQM counter, In the above three cases the counter starts from SBD(x=0) or VCOLOCK (x=1). 100 = CQM input from AGC comparator intended for use in BLOS adjustment
CQM3[5-4]	When counting FIR samples, defines the accumulation periods in terms of RG cycles	00 = 16 RG period 01 = 144 RG periods 10 = 528 RG periods 11 = 1008 RG periods
CQM1[7:0] & CQM2[7:0]	16-bit counter value (read only)	Read only

TIME BASE GENERATOR CIRCUIT

The time base generator (TBG) is a PLL based circuit that provides a programmable reference frequency to the data separator for constant density recording applications. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N, and DR Registers. The TBG output frequency, Fout, should be programmed as close as possible to ((17/16) • NRZ Data Rate). The time base also supplies the timing reference for write precompensation so that the precompensation tracks the reference time base period.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to reduce the effects of common mode noise.

In read, write and idle modes, the programmable time base generator is used to provide a stable reference frequency for the data separator. In the write and idle modes, the TBG output (divided by 2), when selected by the CM Register TP bits, can be monitored at the TPF and $\overline{\text{TPF}}$ test pins. In the read mode, the TBG output should not be selected for output on the test pins to minimize the possibility of jitter in the data separator PLL.

The reference frequency is programmed using the M and N Registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

F_{TBG} = FREF [(M + 1) / (N + 1)]

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The DR Register must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N Registers only after the DR Register is updated.

TIME BASE GENERATOR CIRCUIT (continued)

The DR Register value directly affects the following parameters:

- center frequency of the time base generator VCO,
- center frequency of the data separator VCO,
- phase detector gain of the time base generator phase detector,
- phase detector gain of the data separator phase detector,

The reference current for the DR DAC is set by a fixed external resistor, RR, connected between the RR pin and ground.

RR = 10.0 kΩ for 240 Mbit/s operation.

DATA SEPARATOR CIRCUIT

The Data Separator circuit provides complete encoding, decoding, and synchronization for 16/17 (0,6/8) GCR data. In data read mode, the circuit performs clock recovery, framing/sync byte detection, decoding, descrambling, and NRZ interface conversion. In the write mode, the circuit generates the VCO sync field, scrambles and converts the NRZ data into 16/17 (0,6/8) GCR format, proceeds the data, and performs write precompensation.

The circuit consists of five major functional blocks: the data synchronizer, 16/17 ENDEC, NRZ scrambler / descrambler, NRZ interface, and write precompensation.

Data Synchronizer

The data synchronizer uses a fully integrated, fast acquisition, PLL to recover the code rate clock from the incoming read data. To achieve fast acquisition, the data synchronizer PLL uses two separate phase detectors to drive the loop. A decision-directed phase detector is used in the read mode and phase-frequency detector is used in the idle, servo, and write modes.

In the read mode the decision-directed timing recovery updates the PLL by comparing amplitudes of adjacent “one” samples or comparing the “zero” sample magnitude to ground for the entire sample period. A special (non IBM) algorithm is used to prevent “hang up” during the acquisition phase. The determination of whether a sample is a "one" or a "zero" is performed by the 3-level slicer.

The gain of the phase detector is reduced by a factor of 5 after the SFC to reduced the bandwidth of the loop. This increases the immunity of the loop from noise during data.

In the write and idle modes the non-harmonic phase-frequency detector is continuously enabled, thus maintaining both phase and frequency lock to the time base generator's VCO output signal, FTBG. The polarity and width of the detector's output current pulses correspond to the direction and magnitude of the phase error.

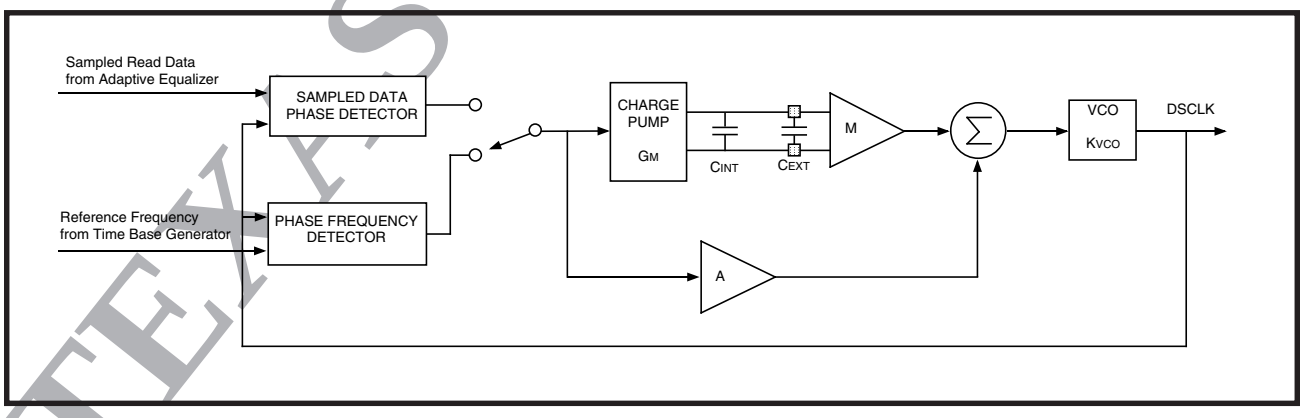


FIGURE 16: Data separator phase-locked loop block diagram

The two phase detector outputs are mixed into a single differential charge pump which drives the loop filter directly. The loop filter requires an external capacitor. The loop damping ratio is programmed by bits 6 - 0 in the DRC Register. The programmed damping ratio is independent of data rate.

In write mode, the TBG output is used to clock the encoder, precoder, and write precompensation circuits. The output of the precompensation circuit goes to the write data flip-flop which generates the write data (WD, $\overline{WD}$) outputs.

ENDEC

The ENDEC implements a Silicon Systems proprietary 16/17 (0,6/8) Group Code Recording (GCR) algorithm. The code has a minimum of no zeros between ones and a maximum of six and eight zeros between ones for the noninterleaved and interleaved samples, respectively. During write operations the encoder portion of the ENDEC converts two bytes of data, scrambled or unscrambled, to 17 bit parallel code words that are then converted to serial format. In data read operation, after the code word boundary has been detected in the viterbi qualified serial data stream, the data is converted to 17 bit parallel form and the decoder portion of the ENDEC converts the 17 bit code words to two bytes of NRZ format.

Sync Word

The SSI 32P4103B uses a dual sync word scheme (SB1 and SB2, each 17-bit long) to reduce the probability that a single error event will cause the sync byte to be missed. SB1 and SB2 are NRZ:91B1h, or 12335h encoded and NRZ:9103h or 12343h encoded, respectively. Only the last 9 bits of the 17-bit word are bit by bit checked against the last 9 bits of SB1 and SB2 for detection. Since this will provide separation of 8 bits between the two 9-bit words that are checked for sync word detection, a single error event, which typically causes 4 consecutive bits errors, will not overlap both. Additionally a programmable number of pads (as set by CM3:STRB) can be placed between the two sync words to combat problems encountered during thermal asperity events.

The first sync byte (SB1) is optional. Since the SSI 32P4103B looks for either sync word, the absence of the SB1 is not an error.

When CM1:TRSQ is set, the training/sync byte sequence is generated with an internal state machine. Once SSI 32P4103B receives all FFh NRZ pattern from HDC after write gate is asserted, the internal state machine automatically generates one equalizer training pattern (91A0h, NRZ or 12324h encoded) first sync word (SB1), one equalizer training pattern and second sync word (SB2). The SSI 32P4103B needs only one FFh NRZ pattern in order to trigger the internal state machine, the following seven bytes do not need to be FFh pattern, since they are ignored.

TABLE 7: Summary of Training and Sync Byte

Sync Word	NRZ	(16/17) [0,6/8] Encoded
TRAINING	91A0h	12324h
SB1	91B1h	12335h
SB2	9103h	12343h

Additional discussion of sync byte generation and detection is in the “Description of Operating Modes” section.

Dual Header

The purpose of the dual header is to allow for a more robust sync byte detection against TA events during preamble period which may cause false PLL locking. This mode is invoked when both RCVRM1 & RCVRM0 bits in the MISC1 Register are set to 1. In this mode, the user may write secondary preamble pattern(plus additional training pattern, if desired) between two sync words. The user can write a secondary preamble pattern using NRZ = FE7Fh. The total words(17bits) of secondary preamble pattern (including any additional training pattern written) has to match the setting of CM3:STRB(5:0), 0 - 31 words. During the read, if the channel is unable to detect the first sync word due to a TA event before the timer (whose duration in bytes is set by STM2:BYTEDLY[6:0] bits) runs out, the internal read gate is automatically toggled once over the secondary preamble pattern, and the process of the PLL locking sequence and the detection of a second sync word begins. The user has to set the appropriate number of bytes in BYTEDYL[6:0] of Register STM2 corresponding to the time period from the rising edge of RG to when the internal read is to be toggled so that the internal read gate toggles at or around the beginning of secondary preamble written. Refer Figure 29 and Figure 30.

DATA SEPARATOR CIRCUIT(continued)

Scrambler/Descrambler

The scrambler/descrambler circuit is provided to reduce fixed pattern effects on the channel's performance. It is enabled or disabled using CM1:SD. In write mode, if enabled, the circuit scrambles each NRZ byte of data before passing it to the encoder. Only user data, i.e. the NRZ data following the second sync byte, is scrambled. In data read mode, only the decoded NRZ data after the second sync byte is descrambled. The scrambler polynomial is H(X) = 1 xor X3 xor X10. The scrambler block diagram is shown in Figure 9. The scrambler is effectively clocked 8 times for each NRZ byte time, and the X2 through X9 outputs are XOR'd with the NRZ data (X2 is the LSB, and is XOR'd with NRZ0).

When the scrambler is enabled, the initial state of the scrambler is 3FFh, all ones, (or 2AAh depending upon CM3:SEED) , and the X output vector is FFh. The SEED bit is provided to allow the scrambler seed to be switched on alternating tracks if desired. At the next NRZ byte, the scrambler has been clocked 8 times, the scrambler state is 31Ch and the X output vector is C7h. The X output vector repeats every 1023 byte times.

When the scrambler is disabled, the flip-flops are preloaded with zeros, and the scrambler state (and the X vector) remains at zero. When this is XOR'd with the data, the data is unchanged.

Note that the scrambler and descrambler must be active during the normal read cycle to avoid errors caused by constant pattern effects.

NRZ Interface

As each NRZ byte is input to the SSI 32P4103B, its parity is checked against the controller supplied parity bit NRZP. If an error is detected, the PERR output pin goes high.

In data read mode, the NRZ data will be presented to the controller near the falling edge of RCLK so that it can be latched by the controller on the rising edge of RCLK. When RG goes high, the selected NRZ interface will output low data until the sync byte has been detected. The first non-zero data presented will be the sync byte (69h). The NRZ interface is at a high impedance state when not in data read mode. An even parity bit, NRZP, is generated for each output byte.

The duty cycle of the RCLK is varied as shown in the following diagram: It consists of a 5 Tc low period followed by three 4 Tc periods of alternating polarities.

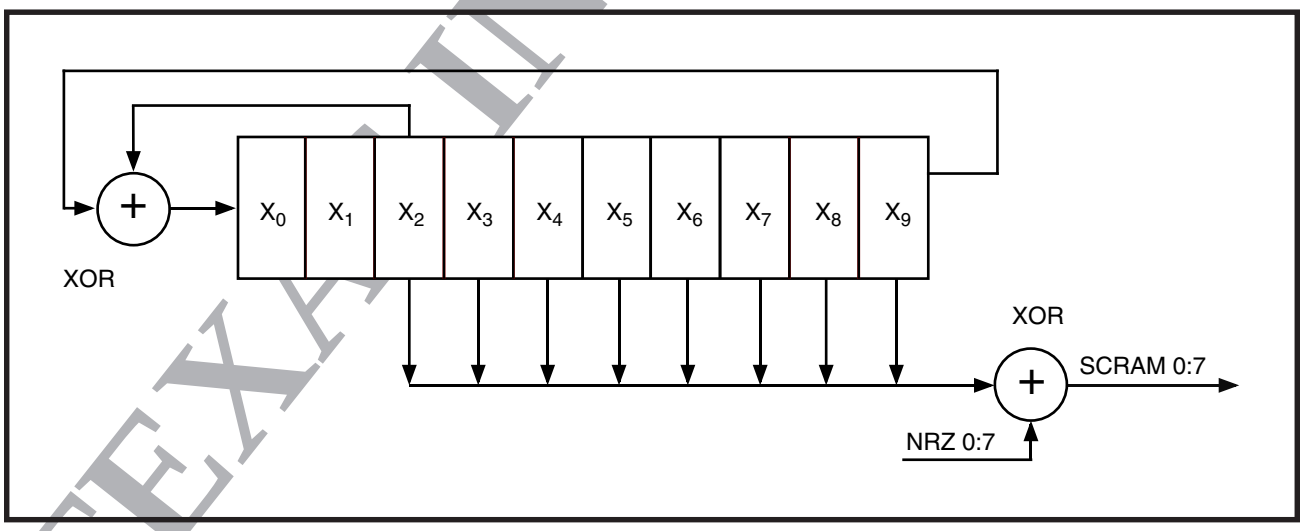


FIGURE 17: Scrambler block diagram

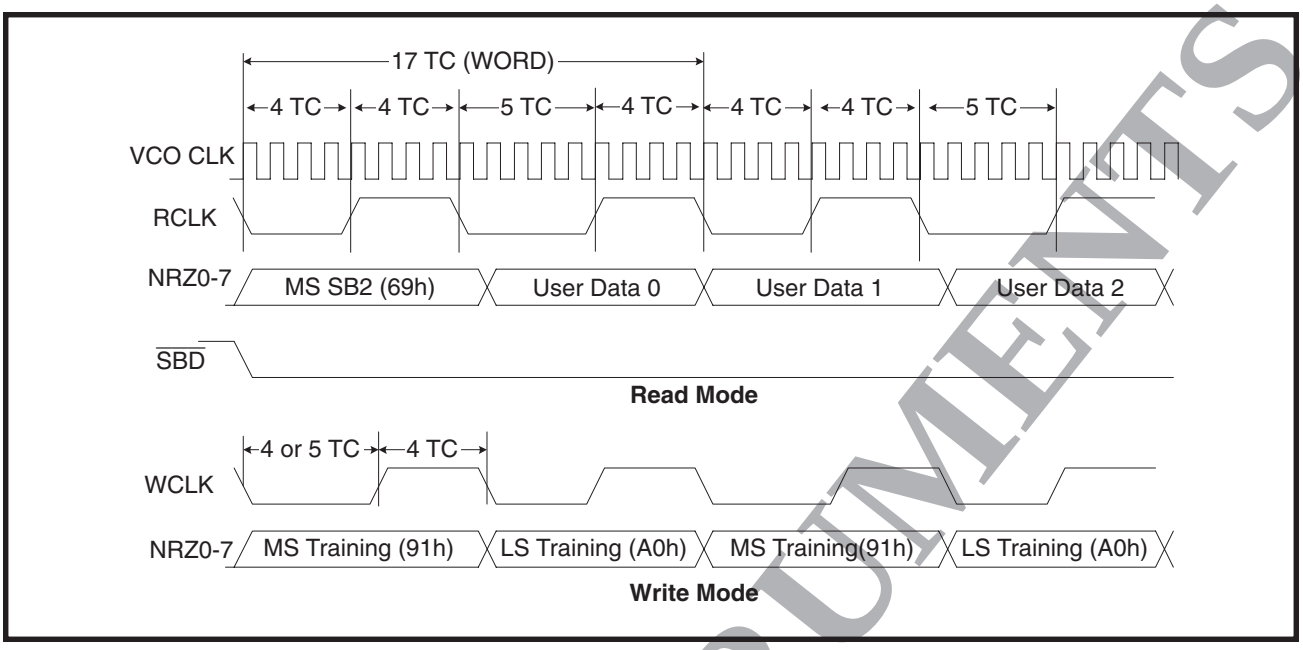


FIGURE 18: RCLK and WCLK vs. NRZ Data

Write Data Output, Precoder

In write mode, the encoded data at the ENDEC output is latched into a shift register, then shifted serially through the precoder and write precompensation circuits.

The encoded data is shifted into the precoder MSB first, LSB last. Prior to the first valid data from the encoder (the first byte of the training sequence), ones are clocked into the precoder. The precoder function is $1/(1 \oplus D^2)$. The precoder block diagram is shown in Figure 19.

Write Precompensation

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognized specific write data patterns and can add delays in the time position of write data bits to counteract the magnetic nonlinearity effects. The magnitude of the time shift is programmable via WP Register and is proportional to the time base generator VCO period (TVCO).

SSI 32P4103B offers two independent levels of write current precompensation, Level 1 and Level 2. Level 1 is the extent of write precompensation applied to the second of the two consecutive transition in the late direction. Level 2 is the amount of precompensation applied to the second of the two transitions when transitions are two code periods (TVCO) apart. Level 3 is the precompensation applied to the third of three consecutive transitions. The magnitude of the primary and secondary precompensations, Level 1 and Level 2, are controlled by WPC1(lower 4) bits and WPC2(upper 4) bits of WP Register, respectively. Level 3 precompensation is derived as the difference between Level 1 and Level 2. The third level of precompensation reverts back to the primary precompensation by setting WP:WPC2 to 0h.

The write data flip-flop is included in the SSI 32P4103B, there should be no write data flip-flop in a read/write chip connected to the SSI 32P4103B.

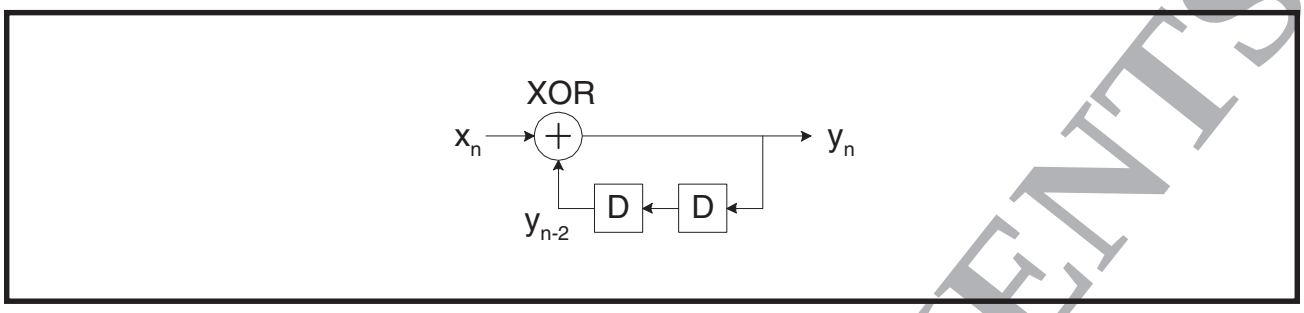


FIGURE 19: Precoder block diagram

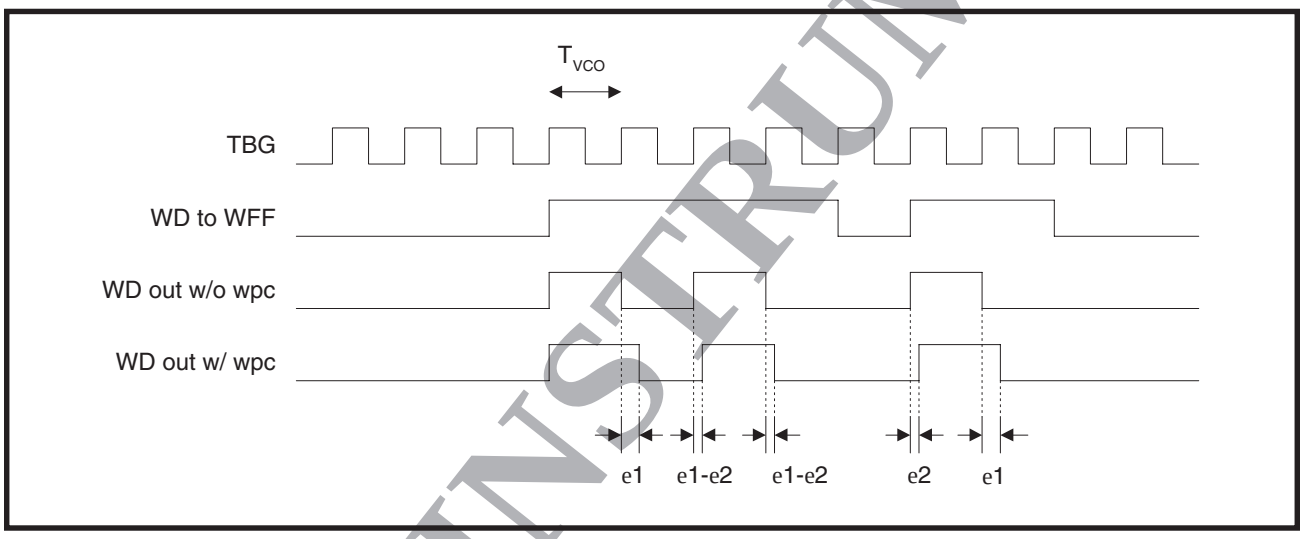


FIGURE 20: 3-Level Write Precompensation

DATA SEPARATOR CIRCUIT

(continued)

TABLE 8: 3-Level Write Precompensation Algorithm

Interaction	WD input to Write F/F			Magnitude of Precompensation
	n-2	n-1	n	
No precompensation	0	0	1	0
One transition apart	0	1	1	Level 1
Two transitions apart	1	0	1	Level 2
Both one AND two transitions apart	1	1	1	Level 3

SERIAL PORT CIRCUIT

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the 39 internal registers of the SSI 32P4103B. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/$\overline{W}$ bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits contain the three device select bits, S0:S2, and the four address bits, A0:A3, which determine the internal register to be accessed. The entire byte is considered to be the Register String ID and is referred to in the following format: A3, A2, A1, A0, S2, S1, S0, R/$\overline{W}$.

The second byte contains the programming data. In read mode (R/$\overline{W}$=1) the SSI 32P4103B will output the register contents of the selected address. In write mode (R/$\overline{W}$=0) the device will load the selected register with data presented on the SDATA pin.

Additionally included is a serial port buffer for interface to the preamp. This will eliminate the need for an additional IC on the drive for buffering of the preamps serial port pins. There are three serial port bits (PSP1,2 and 3) assigned to control the transfer of serial data in this mode to and from the preamps serial port pins (PSDEN, PSCLK, PSDATA). In the default mode (PSP1,2,3=0) the PSDEN, PSCLK, and PSDATA are driven directly when SDEN is high AND RG=WG=SG=0. When PSP1=1, this transfer is disabled and the pins are in a Hi-Z state. Whenever this transfer mode is disabled, via SDEN, RG, WG, or SG, the three preamp serial port output pins are tri-stated (PSP2=0) or driven low (PSP2=1) depending upon the state of PSP2 bit. During a serial port transfer, if the R/$\overline{W}$ bit is '1', the SSI 32P4103B will detect if the following select bits, S0, S1, S2 are '100'. If so, the PSDATA pin is turned into an input following the 8th clock cycle and drives the SDATA output until the SDEN falling edge.

The PSP3 bit sets the preamp serial port buffer into TI mode of write operation. In this mode, the three outputs are not enabled unless R/$\overline{W}$, S0, S1, S2 bits are detected as '0100'. When detected, the three outputs are enabled AFTER the first 8 clock cycles of serial port transfer. Otherwise, the outputs are disabled. Note in TI mode, the serial port transfer to the preamp is only through the 8 data bits following the first 8 clock cycles.

During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in the electrical specifications section. Figure 21 shows the serial port interface timing.

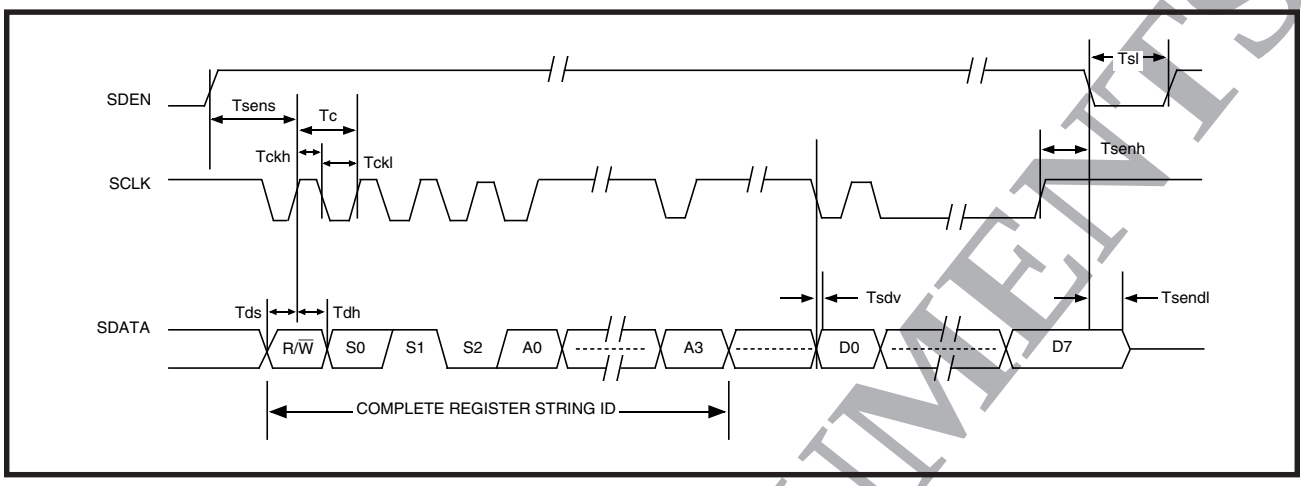


FIGURE 21: Serial port interface timing

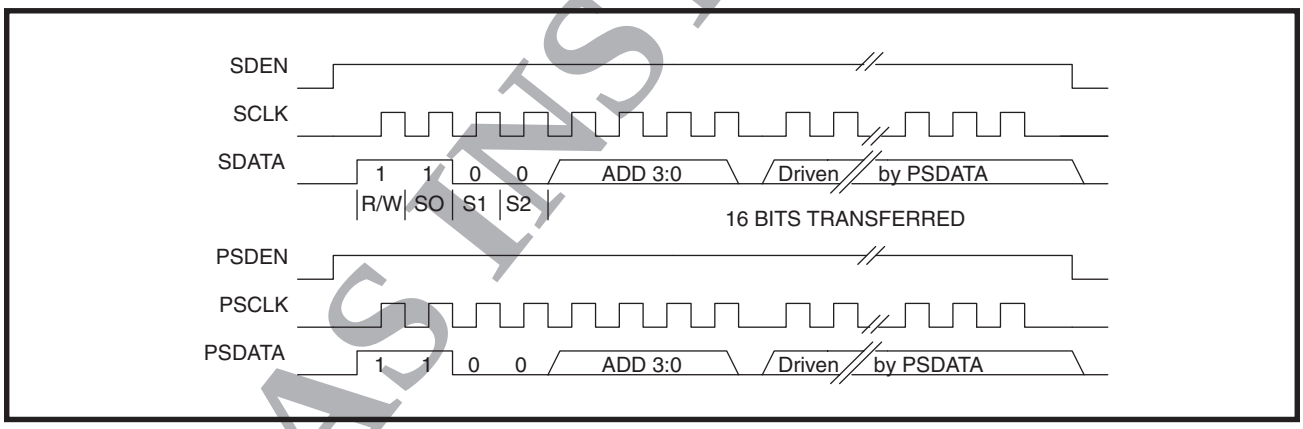


FIGURE 22: Preamp serial port buffer read operation

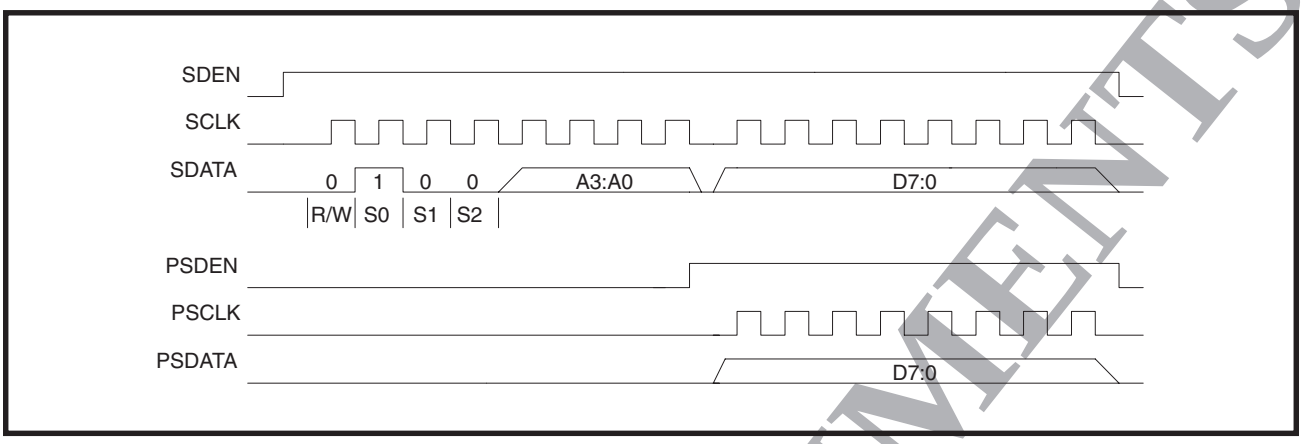


FIGURE 23: Preamp serial port buffer TI mode write operation

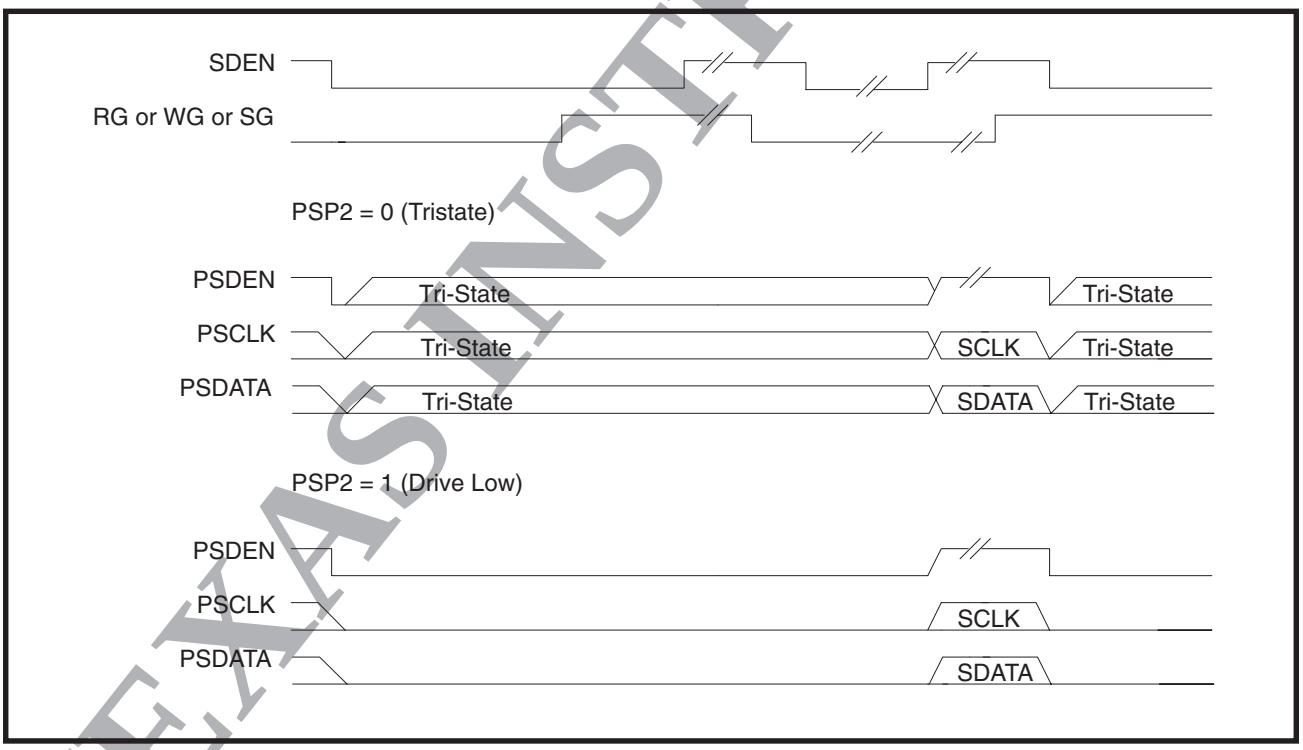


FIGURE 24: Preamp serial port buffer tristate operation

FUNCTIONAL DESCRIPTION (continued)

THERMAL ASPERITY DETECTION AND SUPPRESSION

A thermal asperity event appears to the Read Channel as a sudden (10's of ns) base line shift of the incoming read signal followed by an exponential (300 to 500 ns time constant) decay. These events can occur in either direction. The magnitude of an asperity is defined as follows:

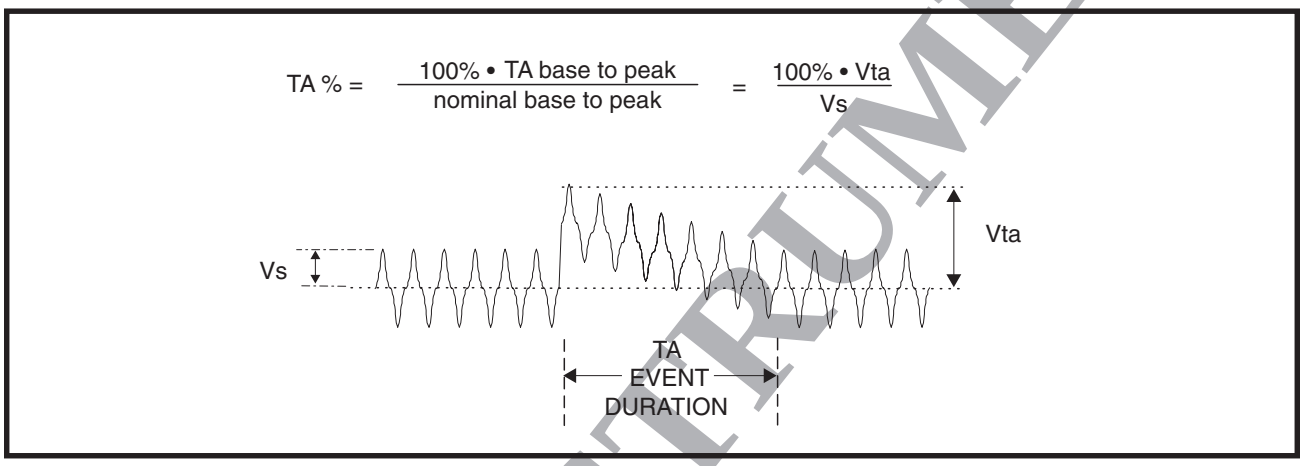


FIGURE 25: Thermal Asperity Definition

The Thermal Asperity detection and suppression circuitry in the SSI 32P4103B is designed to accommodate TA magnitudes as large as 500% while keeping the burst error length less than 5 bytes.

Thermal Asperity Detection Circuit

A thermal asperity can be detected using the on-chip detector (TAIO = 0) or an external detector may be used (TAIO = 1). Pin TAD is therefore an output if TAIO = 0 and an input if TAIO = 1. If an external detector is used, TAD has positive polarity (TAD = 1 indicates that an asperity has been detected).

The thermal asperity detector monitors the signal at the low-pass filter's output (DP/DN) with a threshold comparator. This comparator is very similar to the comparators used for level pulse qualification. Under normal conditions, the signal at this point should be about 1.4 Vp-p (0.7 Vpk). A thermal asperity will cause a sudden shift in the baseline voltage which will trip the threshold comparator. The threshold setting is programmable from +0.75 Vpk to +1.5 Vpk with 4 bits of resolution. This corresponds to a percent threshold setting from 107% to 214% of the nominal zero to peak voltage swing. When the signal crosses this threshold, the TAD signal is asserted. When the signal crosses the opposite polarity Level Qualifier threshold, the TAD signal is reset.

In order to keep the detection circuit from triggering on the normal AGC transient response, the detection circuit is held reset whenever the Low-Z or Fast Recovery modes are activated and during the period from RG rising to completion of Sync Field Count.

Thermal Asperity detection must be enabled by FB:ENTAD. The user should then program the TAth Register to set the detection threshold. It should be set high enough to avoid false triggering.

Thermal Asperity Suppression Circuit

NRZ errors caused by thermal asperity events are unavoidable. The suppression measures listed below are intended to limit the duration of the errors at the NRZ output. The suppression methods can only be activated when in Read mode (RG = high) after SFC or in Servo mode (SG = high).

But other modes can be selected by bits 5-3 of TA1 Register. TA1:TAIDLE is provided to allow TA detection and suppression (w/o PLL Hold) in IDLE mode, TA1:TARG is provided to allow TA detection and suppression in Read mode (RG=high), and LD:TARGB is provided to allow the data AGC to be held from the falling edge of RG to the SFC of the following RG.

If both SG and RG are high at the same time, the servo mode of operation will be asserted. If an asperity occurs within 4 µs (3,2 or 1 µs, depending on TA3:HIYTMR[1:0]) before the leading edge of RG or SG, the suppression measures will go active when RG or SG goes high and remain active for the indicated duration from the leading edge of TAD. At power-up, all the suppression features will be disabled and must be enabled via the serial port.

Dynamic Hi-Y

When the TAD signal goes active, the input admittance of the VGA amplifier can be quickly set to a higher value. This allows the high-pass corner at the VIA/$\overline{\text{VIA}}$ pins to be increased. If the AC-coupling capacitor at the VIA pin is C, and Yin is the differential input conductance between VIA and $\overline{\text{VIA}}$, then Fhp = 2•Yin/(2 • π • C). By moving Fhp to a higher frequency, the low frequency characteristic of the thermal asperity can be quickly attenuated. The input admittance will have a fast turn-on (<100 ns), slow turn-off (about 1 µs) characteristic to minimize glitches going in to the AGC amplifier. The Fhp frequency should be proportional to the NRZ data rate. Three serial port bits allow 8 different values of input admittance to be programmed, TA3:YIN bits control the admittance in non-servo mode and MISC2:YINS bits control it in servo mode. A serial port bit (MISC1:FOSNUL) is provided to enable a fast filter output offset cancellation during a TA event.

The duration of the Dynamic Hi-Y state will be 1 to 4 µs following the leading edge of TAD programmable from TA3 Register. A static Hi-Y mode is also available in which the Hi-Y condition will be asserted as defined by HYES bits in TA2 Register. This mode should prove useful in a "re-try" mode of thermal asperity suppression. The Dynamic Hi-Y can also be totally disabled via the serial port. Also Ultra Hi-Y (set YIN = 111 and enable extra lowz mode) and Squelch can be activated after TAD by UHIY(TA4_5) and SQEN(TA4_5) bits. The duration of both modes can be set by SQTMR[1:0] (TA4_1-0). In servo mode (SG = High), both modes can be disabled by SGUHY(TA4_2) bit.

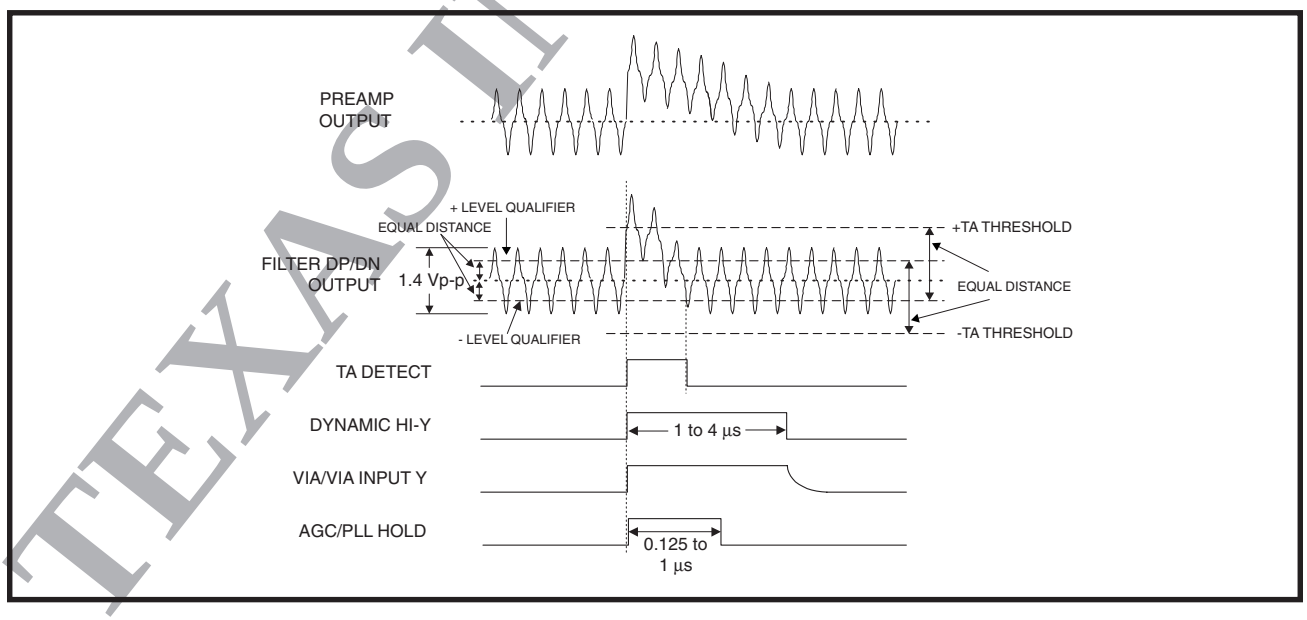


FIGURE 26: Thermal Asperity Suppression

THERMAL ASPERITY DETECTION AND SUPPRESSION (continued)

AGC/PLL Hold

The signal at DP/DN should not be used for adaptive AGC, equalization, timing extraction, or offset correction until the proper baseline has been restored. Therefore, all of these functions may be suspended for a programmable time period when a thermal asperity is detected. The hold time may be programmed (TA3:TATMR) from 0.125 µs to 1 µs with a 0.125 µs resolution. The user should program this time period to match the signal recovery time in the Dynamic Hi-Y mode. If this time period is set too long, there is a risk of losing the proper timing relationship in the PLL. The PLL hold function is also controlled by TA1:PLLHE. For a 00 setting the PLL hold is disabled over the TA event. A 01 setting enables the PLL hold time as described above but a 10 setting holds the PLL only for the time that the TA detect is high. TA1:TAPLLGS allows the PLL gain to be reduced during a TA event.

The AGC and AC_Coupling hold functions are enabled by TA1:AGCHE. The AGC hold function itself can be manually controlled by asserting the $\overline{\text{HOLD}}$ input pin. The PLL and Equalizer hold function can be manually controlled by asserting the EQ/PLLHOLD input pin. A serial port bit (SLC:AED) is provided to force equalizer hold following sync byte detect.

Error Flag (or Erasure Flag)

The error flag circuitry monitors the level slicer output from the sampled data processor. A run of 5 or 6 same polarity “1” samples indicates the occurrence of an asperity. This sets an internal error flag which marks the corresponding NRZ data as being corrupted. The circuit looks for an opposite polarity “1” to start the process of resetting the error flag. When an opposite polarity “1” is detected, an internal counter begins to count 6 internal clock periods. If a run of 3 or 4 positive “1” samples occurs during this count down, the counter starts over. If the counter is able to reach 6 without being restarted, the error flag is allowed to reset itself. The signal is output at the NRZP pin as selected by TM2:TSTSL. The error flag can also be seen on the PPOL pin when RDSMUX - 0 and SG = low.

The error flag signal is used to mark the potentially corrupted NRZ data. The signal should aid the external error correction circuitry in recovering the data during a thermal asperity event. The TAD and EFLAG signals can be mixed onto the RDS and PPOL pins when SG=0 by enabling BLO:RDSMUX.

Applying Thermal Asperity Detection and Suppression

The TA detection threshold should be set low enough to flag any asperity which can cause an error burst longer than the ECC can handle. When an asperity is detected, it is recommended that dynamic Hi-Y, AGC/PLLHOLD, and Error Flag monitoring be applied. This will give the best probability of “on-the-fly” asperity correction. The duration of AGC/PLLHOLD should be just long enough to prevent corrupt data from disturbing any of these control loops. The static Hi-Y mode is included to allow asperity correction on a “retry” basis.

Thermal Asperity Monitoring at TPE Pin

The TPE pin is for various test and verification purposes. One of them is to monitor the thermal asperity time-out signal for suppression. The truth table for the TPE output at various register bit settings is shown in the Power Down Register bit definition section. Both Hi-Y and AGCHOLD_TA periods are programmable.

Ultra Hi-Y Mode Admittance Measurement

Admittance in Ultra Hi-Y mode can be measured by setting by PD_7-6 = 01, T_SPC(FC_7) = 1, SG = RG = Low, WG = High, LOWZ = High, UHIY(TA4_5) and UHIY2(MISC4_5) Inputs/bits.

OPERATING MODES

The fundamental operating modes of the SSI 32P4103B. are controlled by the SERVO GATE (SG), READ GATE (RG), and WRITE GATE (WG) input pins. The exclusive assertion of any these inputs causes the device to enter that mode. If none of these inputs is asserted, the device is in idle mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The overriding mode takes effect immediately.

RG and SG are asynchronous inputs and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to flushing data through the encode and write precompensation circuits. A minimum of 6 bytes is required to flush these circuits.

Idle Mode Operation

If SG, RG, and WG are not active, the SSI 32P4103B is in idle mode. In idle mode, the time base generator (TBG) and the data separator PLL are running, and the data separator PLL is phase-frequency locked to the TBG output. The AGC, continuous time filter, and pulse qualifiers are active, but the outputs of the pulse qualifiers are disabled. The continuous time filter uses the programmed values in the data mode Registers (FC, FB) for cutoff frequency and boost. The AGC operation is the same as in the VCO preamble portion of a data read.

Servo Mode Operation

If SG is high, the device is in the servo mode. This mode is the same as idle except that the filter cutoff and boost settings are switched from the data mode Registers to the servo mode Registers (FCS, FBS), the AGC is switched to servo mode, and the $\overline{\text{RDS}}$ and PPOL and outputs are enabled. The assertion of SG causes read mode, write mode, and the Power Down Register settings for the front end to be overridden.

Write Mode Operation

The SSI 32P4103B supports three different write modes; normal write mode, direct write mode 1 and direct write mode 2. The direct write modes require that either the DWDR bit in the CM1 Register, or the $\overline{\text{DWR}}$ pin be active. All three write modes require that the data separator be powered on.

The WG pin operation can be inverted by setting the WGP bit in the CM1 Register. When CM1:WGP is low, WG is active high. When CM:WGP is high, WG is active low. Throughout this specification, WG is referred to as active high.

Normal Write Mode

The SSI 32P4103B. is in the normal write mode if WG is high, $\overline{\text{DWR}}$ is high, and the DWDR bit in the CM1 Register is low. A minimum of one NRZ byte (RCLK) time period must elapse after RG goes low before WG can be set high. The data separator PLL is phase-frequency locked to the TBG VCO output (FOUT) in this mode.

In normal write mode, the circuit first auto generates the VCO sync pattern, training patterns and sync bytes, and finally scrambles the incoming NRZ data from the controller, encodes it into 16/17 GCR formatted data, precodes it, precompensates it, feeds it to a write data toggle flip-flop, and outputs it to the preamp for storage on the disk. The write data flip-flop is reset when WG goes low.

The write data outputs remain active after WG goes low, with the active pull down current reduced by a factor of 7 to save power. Since the write data flip-flop is reset when WG goes low, the WD outputs go to a zero state when WG is low.

Direct Write Mode 1

In this mode, the RCLK period is changed from 17/2 FOUT clock periods to 8 FOUT clock periods, with a 4/4 duty cycle. NRZ data from the byte-wide interface bypasses the input latch, the scrambler, and the 16/17 encoder, and is latched directly into the parallel to serial shift register. The serial data bypasses the precoder, but is precompensated before going to the write data flip-flop and then to the WD/$\overline{\text{WD}}$ output pins. The NRZ input data may be changed, provided that the controller outputs data no later than 12 ns after the falling edge of RCLK. Operation with changing NRZ data is only guaranteed up to a maximum user data rate of 240 Mbit/s . Direct write mode #1 is entered by setting CM1:DWDR.

Direct Write Mode 2

In this direct write mode, the input at the DWI/$\overline{\text{DWI}}$ pins directly toggles the write data flip-flop which drives the WD/$\overline{\text{WD}}$ output pins. No WCLK is required in this mode, and the WD/$\overline{\text{WD}}$ output is not resynchronized. Direct write mode #2 is entered by driving the $\overline{\text{DWR}}$ input low.

Data Read Mode Operation

Data read mode is initiated by setting the Read Gate (RG) input pin high. This action causes the data synchronizer to begin acquisition of the clock from the incoming VCO sync pattern. To achieve this, the data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the sample clock. This PLL is normally locked to the time base generator output, but when Read Gate input (RG) goes high, the PLL's reference input is switched to the filtered incoming read signal.

A minimum of 8 pad bytes should be written to the disk to flush the read mode circuits.

OPERATING MODES (continued)

Direct Read Mode

The SSI 32P4103B supports direct read mode. In this mode, the RCLK period is set to 8 FOUT periods with a 4/4 duty cycle. A direct read operation is initiated in the same manner as a normal read. At assertion of RG, the DSVCO starts tracking the VCO sync pattern and the SFC counter starts counting incoming '1's. The direct read process continues analogous to the normal read up to the sync byte detect sequence. The sync byte detect sequence is the same. The same 9 LSB bits of the 12335h(SB1) or 12343h(SB2) is detected to determine the byte boundaries and initiate the read operation.

After sync byte detection, the direct read is unique from that point in that data is converted to 8-bit parallel (byte) data and passed directly to the NRZ output pins. No decoding is performed, and no de-scrambling.

This mode is enabled by asserting RG with the DWDR bit (CM1:bit0) set.

Force Frame Mode

In read mode, if a defect occurs around the sync byte in such a way that the device can not detect the sync byte, then there is no way to recover the data in that sector. Force frame mode is a method to attempt to recover the data even without being able detect the sync byte. This is done by setting the read recovery mode (RCVRM) MISC1:bits 7:6 to 10b in the serial port. When this occurs, a special read mode is invoked.

In force frame mode, an alternative sync byte detect circuitry is enabled. The read begins as normal. When read gate is asserted, a byte (8 VCO clocks) counter whose value is set by STM2:BYTEDLY is started. When it has counted down to zero it sets an internal Force-Frame-Detect signal (FFrmDET). After FFrmDET goes high, a small three bit counter (T2VCODLY) begins counting VCO/2 clocks. This three bit counter is programmed by setting bits 6,5 and 4 of the STM1 Register. When the T2VCODLY counter has counted down the number of VCO/2 clocks, the sync-byte-detect is forced on the device. The odd or even interleave is chosen by STM1:ODDEVEN. Then, 2-bit data is converted/transferred to the endec properly, the data begins being decoded, de-scrambled (if the register bit is set), and starts coming out the NRZ outputs.

When the correct bit/interleave position is found, the byte out of the NRZ outputs is the 69h sync byte followed by the correct data. From this point on, the scrambler is enabled and the decode process continues normally.

Acquisition of DS VCO Sync

The Read Gate (RG) input can be asserted high, initiating the remainder of the read sequence. When RG is asserted an internal counter begins counting the pulses that are qualified by the dual level pulse qualifier from the polarity changes of the incoming 1,1, -1,-1,1,1 read back pattern defined by the VCO sync field. When the count reaches 4 (4 VCO clocks after RG is asserted), the internal read gate is asserted and the DS PLL input is switched from the TBG VCO output to the sampled data input. This is also the point at which the DS PLL phase detector is switched from the phase-frequency detector to the decision directed phase detector. The counter continues counting until a count value of sync field count (SFC), programmed with SLC:SFC, is reached. When the counter reaches SFC, the data synchronizer PLL is assumed to be locked and settled (VCO lock). Also at SFC, the phase detector gain switch and the AGC mode switch occur. To allow for different preamble lengths, SFC can be set to 64, 80, 96 or 128 from the SLC Register. These values for SFC may be thought of as the number of code clock periods in the sync field, but they actually represent twice the number of incoming polarity changes required.

VCO Lock, PD Gain, AGC Mode Switch, and Code Word Boundary Detector Enable

At SFC, one of two phase tracking methods will be chosen depending on the Enable Phase Detector Gain Switching (GS) bit in the CM1 Register. When the CM1:GS bit is high, the phase detector gain is reduced by a factor of 5 (or 10) after the SFC count is reached. When the CM1:GS bit is low, no phase detector gain switching takes place. MISC2:GS10 sets the gain shift factor of 5 or 10.

Also at SFC, the AGC feedback will be switched from the continuous time full-wave rectifier to sampled data feedback.

At SFC, the DS VCO is assumed locked to the incoming read samples, and an internal VCO LOCK signal is generated. This signal switches the RCLK generator source from the TBG output (FOUT) to the

DS VCO clock. VCO LOCK also enables the sync byte detection circuitry to detect the last 9 of 17-bit word decode boundaries. Both the framing and sync byte detection is done at the same time. These boundaries are defined by SB1 and SB2. RCLK may stop toggling for up to a maximum of 1 RCLK time period during the FOUT to DS VCO switchover. No short duration glitches will occur on RCLK during the switchover.

When the sync byte detection circuitry finds the proper code word boundary, RCLK is resynchronized to guarantee that RCLK is in sync with the 17-bit code words. RCLK may stop toggling for up to a maximum of 2 RCLK time periods during resynchronization. RCLK will not glitch and will not toggle during the resynchronization time. Also at the code word boundary detect, the internal 17-bit code words are allowed to pass to the ENDEC for decoding. Decoding occurs until read gate is deasserted.

Adaptive Equalizer Training Sequence

When SLC:AEE=1, in a normal write sequence, a minimum of 4 bytes consisting of NRZ 91, A0H, 91, A0H followed by two bytes each of 91, B1H (SB1) and 91, 03H (SB2) with programmable (0 to 63) number of 91, A0H sequence must be written between SB1 and SB2. The 91, A0H bytes are 16/17 encoded and precoded during write mode to produce the adaptive equalizer training pattern. During read mode, this sequence is used to adaptively train the transversal filter in a zero forcing manner. The error at the FIR filter output is integrated to derive the inner tap weight multiplying coefficient, Km1. It is anticipated that the continuous time filter will be used for coarse equalization and that transversal filter will be used adaptively for fine tuning. This will reduce Km's range and accuracy requirements. Since there are encoded user data patterns that will not produce an equalizer correction error, an equalization hold during data mode can be selected from the SLC Register. After the training pattern, if the loop is active during data (SLC:AED=1), the equalizer loop gain will be reduced by ≅ 7 if SLC:AEGS = 1. The loop's integration time constant is made inversely proportional to the selected data rate.

If AEQADC = 1, the tap weight will be, at the deassertion of RG, A/D converted and written to the serial port for subsequent readout. The A/D converted word will be reset upon the serial port read.

When AEE = 0, no adaptation of the equalizer will take place. The KM1PS setting in the FIR1 Register will set the equalizer inner taps.

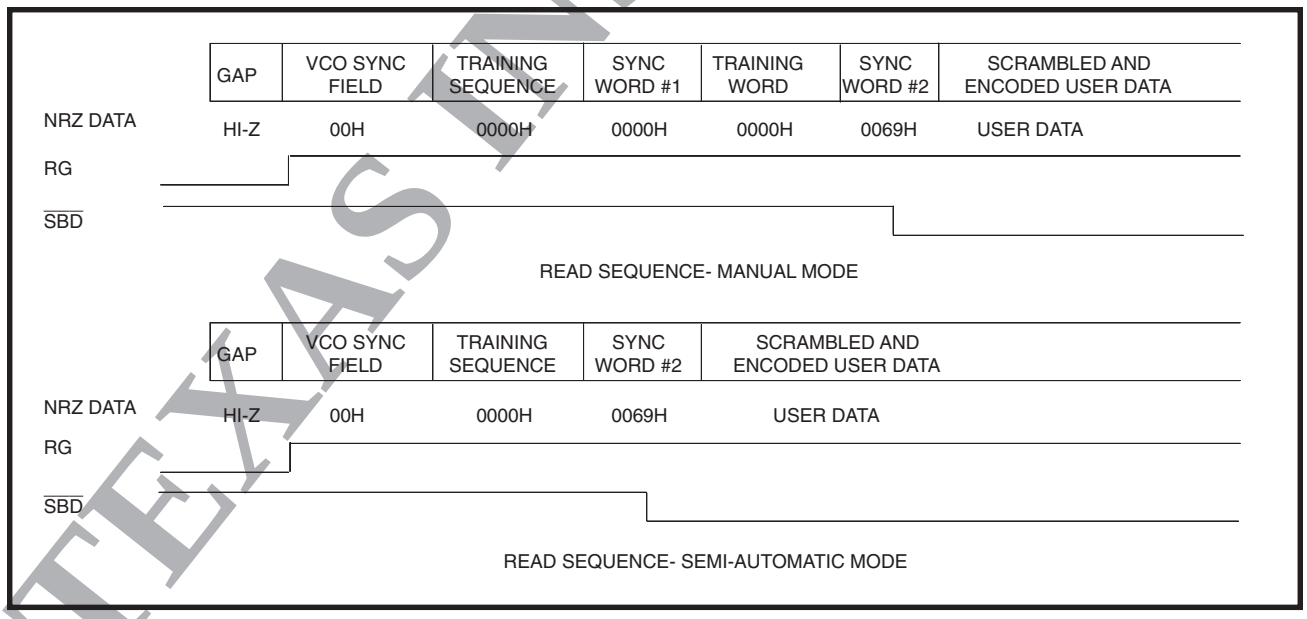


FIGURE 27 : Read Sequence

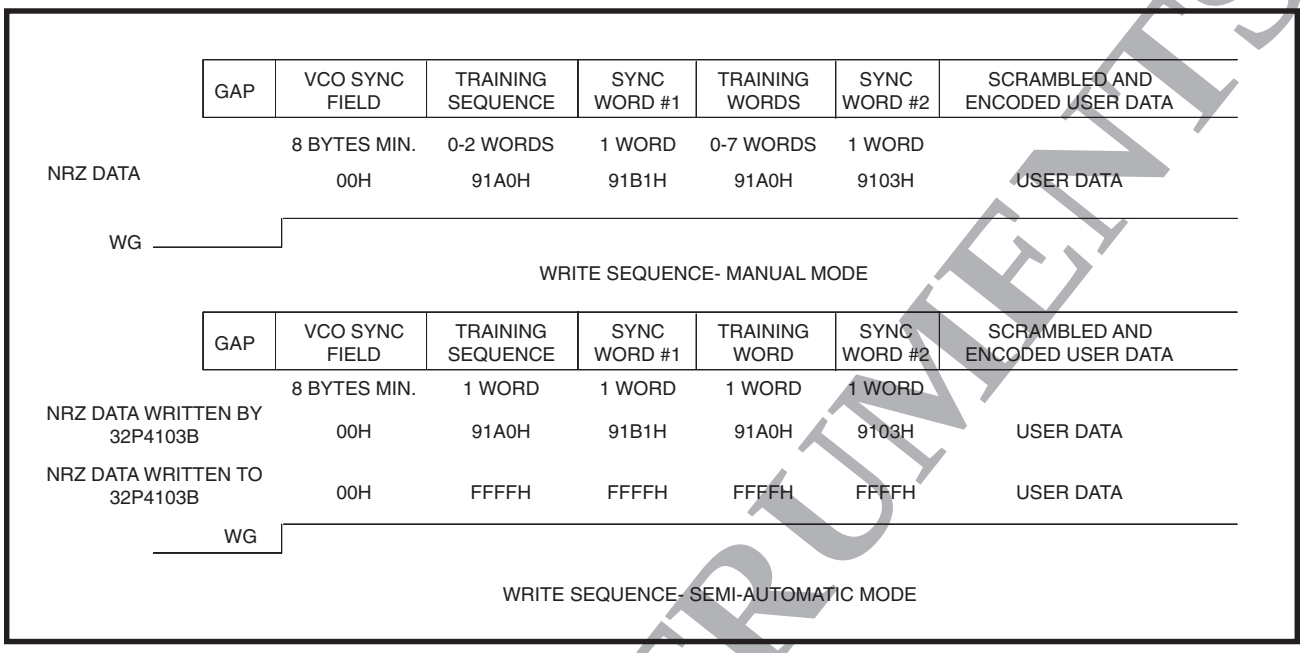


FIGURE 28 : Write Sequence

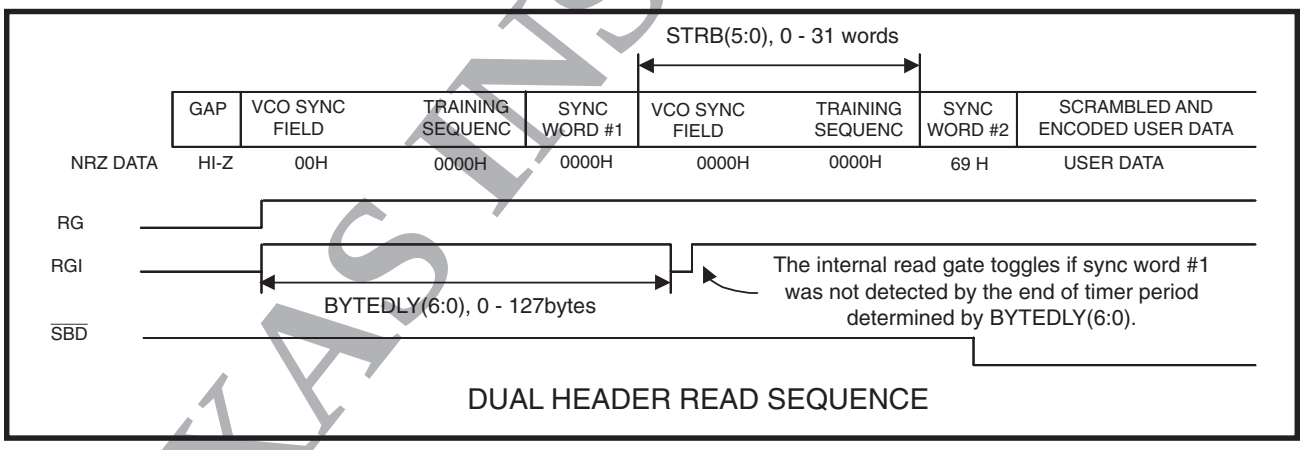


FIGURE 29 : Dual Header Read

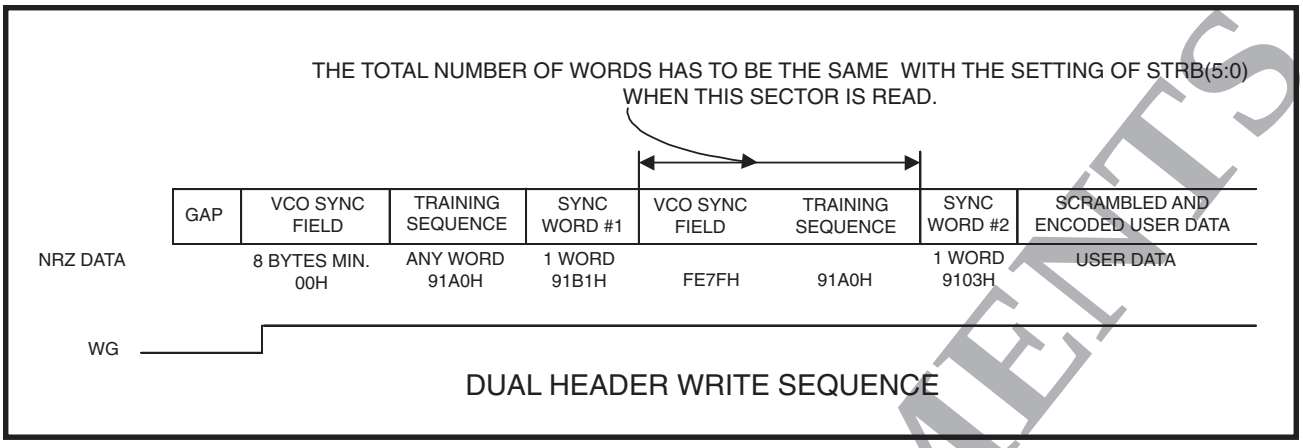


FIGURE 30 : Dual Header Write

OPERATING MODES (continued)

Sync Byte Detect and NRZ Output

The SSI 32P4103B uses a dual sync byte scheme to provide more robust sync byte detection. The sync byte detection circuit looks for either of two sync bytes (SB1 or SB2). There are two operational modes supported in this device: One is the normal dual sync byte mode as depicted in Figure 27 and the other is the Dual Header scheme in Figure 29. The primary purpose of the Dual Header mode is to deal with the event of thermal asperity before the detection of SB1 can occur, and allows recovery from it with the aid of an additional PLL sync field written between two sync words.

In the normal mode, the NRZ outputs are held low before the sync byte output. Detection circuitry for both SB1 and SB2 are simultaneously enabled. When sync byte is detected, the sync byte detect ($\overline{SBD}$) pin goes low and 69h is output at the NRZ interface. If SB1 is detected and SB2 is missed, the $\overline{SBD}$ output will go low 2 bytes + number of pads (programmed between the two sync bytes) later and 69h will be the first non-zero byte output to the NRZ interface. The next byte output on the NRZ interface is the first byte of user data. $\overline{SBD}$ will remain low and user data will continue to be output until RG is deasserted, at which point $\overline{SBD}$ goes high and the NRZ outputs go to a high impedance state. The normal mode is activated by setting MISC1:RCVRM[1:0] = 00.

In the dual header mode, a timer is set off upon the assertion of RG whose duration is programmable via STM2:BYTEDLY[6:0]. If SB1 is not detected within that time period, RG is internally toggled and the detection circuitry for SB2 only (but not SB1) is enabled. This mode is activated by setting MISC1: RCRVM[1:0] = 11.

In both cases it is important that a correct number of words between two sync bytes be entered into CM3:STRB[5:0] bits. It must match the actual number of pads written between the two sync bytes.

POWER DOWN OPERATION

There are two modes of power management available - static and dynamic. The first (static) mode of power management is done via PD Register bits and the second (dynamic) mode by bits 1,2,3,4 of MISC1 Register.

For the static mode the states of the PD Register bits and the $\overline{\text{PDWN}}$ and SG inputs determine the power management. The individual sections of the chip can be powered down or up using the PD Register. A high level in a PD Register bit disables that section of the circuit. The power down information from the PD Register takes effect immediately after the SDEN pin goes low. The truth table for the various operation under static mode is shown below:

servo section is kept powered on after SG goes inactive. Recovery from idle to various mode is fast enough such that it is transparent to the user. The following table shows the power management of the dynamic mode. Note that dynamic power management is not recommended for optimum BER (bit error rat) performance.

When the $\overline{\text{PDWN}}$ input is low, the chip goes into full power down (sleep) mode regardless of the PD or MISC1 Register settings or the state of the SG input. When $\overline{\text{PDWN}}$ is high, SG will force the AGC, filter, and pulse qualifier circuits (front end) to be active by overriding the PD bit in the PD Register. The back end Power Down Register bits, which include the Data Separator and Timebase Generator are not affected by the SG input.

TABLE 9: Servo and Power Down Operation Under Static Mode

	SG, $\overline{\text{PDWN}}$			
	1,1	**1,0**	**0,1**	**0,0**
AGC, Filter, Servo	ON	OFF	R	OFF
Data Separator	R	OFF	R	OFF
Time base Generator	R	OFF	R	OFF
Serial Port	ON	ON	ON	ON
R = Controlled by register bit. (Register bit =1 turns circuits OFF, Register bit = 0 turns circuits ON)				

For the dynamic power management of the SSI 32P4103B bits 1, 2, 3, 4 of MISC1 Register are used to dynamically turn on and off various sections of the device, unless inhibited by PD Register bits. Bit 4 of MISC1 Register controls the power management of the sampled data processor. Bit 3 dictates power management associated with the backend - primarily of the write circuitry. Bits 1 and 2 controls how long the

TABLE 10: Power Management - Dynamic Mode when invoked by MISC1:4,3,2,1

	SG,RG,WG			
	0,0,0	**1,x,x**	**0,1,x**	**0,0,1**
	Idle	**Servo**	**Read**	**Write**
Pd_Qualifier (RDS/PPOL portion)	Off	ON	Off	Off
Servo Demodulator(MISC:2,1)	Off	ON	Off	Off
SDP except PLL(MISC:4)	Off	Off	On	Off
Write Precomp (MISC:3)	Off	Off	Off	On
All other circuitry	R	R	R	R
R = Controlled by PD Register bits.				

REGISTER BIT ASSIGNMENT SUMMARY TABLE

Throughout this document, RR:BB refers to bit BB inRegister RR. As an example, PD:TB refers to bit TB inRegister PD.

REG #	REGISTER NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0D7
PD	Power Down	00000100=04h	TPC/D/E[1:0]		ASEL[1:0]		ACSWT<0>	TB<0>	DS<0>	PD<0>
FC	Filter cutoff, data mode	00010100=14h	T_SPC<0>	FC[6:0] Filter cutoff frequency, data mode<127 decimal>						
FCS	Filter cutoff, servo mode	00100100=24h	SVCAL<0>	FCS[6:0] Filter cutoff frequency, servo mode<23 decimal>						
FB	Filter boost, data mode	00110100=34h	ENTAD<0>	FB[6:0] Filter boost, data mode<14 decimal>						
FBS	Filter boost, servo mode, Filter asym. zero adjust	01000100=44h	FBS[1:0] Filter boost, servo mode<00>		FGD[5:0] Filter asymmetric zero adjust<0 decimal>					
EPR4	EPR4 Detector Conts Reg	01010100=54h	EPR4 Constant (-1.5) <0000>				EPR4 Constant (+0.5) <0000>			
LD	Data level detector Vth Ctrl	01100100=64h	DSCAN <0>	TARGB<0>	LD[5:0] Data level threshold, data mode<32 decimal>					
LDS	Data Level Detector Vth, servo mode	01110100=74h	SAGCL[1:0]		LDS[5:0] Data level threshold, servo mode<32 decimal>					
TM1	Test Mode Register 1	10000100=84h	EFR <0>	ECP<0>	TP[3:1] <000>			BYPSR <0>	DT<0>	UT<0>
TM2	Test Mode Register 2	10010100=94h	ACCPLDE <0>	RDTAGC <0>	IOMAP <0>	DIFFBF <0>	ENTRST <0>	SBAND <0>	TSTSL <00>	
N	Time base N counter	10100100=A4h	FREFPS<0>	N[6:0] Time base generator N counter value <19 decimal>						
M	Time base M counter	10110100=B4h	M[7:0] Time base generator M counter value <212 decimal>							
DR	Data rate	11000100=C4	DSB <0>	DR[6:0] Data rate value <109						
WP	Write precomp magnitude	11010100=D4h	WPC2 [3:0] <0000>				WPC1[3:0] <0000>			
SLC	AGC, equalizer sample loop sequence control	11100100=E4h	AEQADC <0>	SFC[1:0] Sync field length		AEGS Equalizer switching <1>	AED Adapt equalizer on data <1>	AEE<0> Adaptive equalizer enable	AGC[1:0]<10> AGC charge pump current	
DRC	Damping ratio control	11110100=F4h	LOWEQG	DRC[6:0] Damping ratio<70 decimal>						
FIR1	FIR KM1 Register	00000110=06h	KM1AD[3:0] <Read Only>				KM1PS[3:0] <0000>			
FIR2	FIR KM2 Register	00010110=16h	QaeprEn<1>	QaERP[2:0] Viterbi Mod. DAC <0000>			KM2[3:0] <0100>			
CM1	Mode Control 1	00100110=26h	RCLK2X<0>	AGCT<1>	WGP<0>	TRSQ<0>	BT<0>	SD<0>	GS<0>	DWDR<0>
CM2	Mode Control 2	00110110=36h	DIBITPOL<0>	IGAIN[2:0] <100>			PWCTR <0>	PDM <0>	DIBDEN<0>	SERI <0>
CM3	Control Mode Register 3	01000110=46h	FERA <0>	Seed <0>	STRB[5:0] <00000>					
CM4	Control Mode Register 4	01010110=56h	ALE <1>	LEVEL/Qasym TC <00>		FRZQASYM <1>	QalvlEn<1>	QaLVL[2:0] Level Th. Mod. DAC <000>		
TA1	Thermal Asperity 1	01100110=66h	TADE<0>	TAIO <0>	TAIDLE <0>	TARG <0>	AGCHE <0>	PLLGS <0>	PLLHE[1:0] <00>	
TA2	Thermal Asperity 2	01110110=76h	HYED <0>	HYES [1:0] <00>		SVHY <0>	TATH [3:0] <1111>]			

REG #	REGISTER NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
TA3	Thermal Asperity 3	10000110=86h	HYTMR[1:0] <00>		YIN [2:0] <111>			TATMR [2:0] <110>		
TA4	Thermal Asperity 4	10010110 = 96h	RDSMUX <1>	FADIS <0>	UHIY <0>	SQEN <0>	FOSNUL <0>	SGUHY <0>	SQTMR[1:0] <00>	
ASYM	Asemmetry	10100110=A6h	DBT[2:0] (Dibit Enable Time) <000>			ASYMPOL<0>		ASYM <0000>		
CQM1	Channel Quality Monitor Register 1	10110110=B6h	CQMQ[15:8](ReadOnly)							
CQM2	Channel Quality Monitor Register 2	11000110=C6h	CQMQ[7:0](ReadOnly)							
CQM3	Channel Quality Monitor Register 3	11010110=D6h	SGBTMR	PLSEN	CQMRGT <00> <0>		SURVSEL <0>	CQMCTRL/SURVSTA <000>		
TC	Time Control Register	11100110=E6h	UFDC [1:0] <10>		LZT [2:0] <100>			FRT [2:0]<100>		
TCS	Time Control Register for Servo	11110110=F6h	LZCTR<0>	UFDSEL<0>	LZT [2:0]<100>			FRT [2:0]<100>		
STM1	Special Test Register 1	00001000 = 08h	TC8DLY[6:5] <00>		SPLITFF[1:0] <00>		FRCSUR <0>	TSURV<0>	MET07R <0>	CNSTENB <0>
STM2	Special Test Register 2	00011000 = 18h	TC8DLY[4:0] <00000>					TC2DLY[2:0] <00>		ODDEVEN <0>
BLOD	Base Line Offset - Data	00101000=28h	BOSDP <0>		BLOSD[6:0]					
BLOS	Base Line Offset - Servo	00111000=38h	BOSSP <0>		BLOSS[6:0]					
MISC1	Misc. Register 1	01001000=48h	RCVRM[1:0] <00>		RPMEb <0> EPR4 Read Power Managmnt	RPMSb <0> SDP Read Power Managmnt	WPMb <0> Write Power Managemnt	SVPMb <00> Servo Power Management		FOmpEn <1>
MISC2	Misc. Register 2	01011000=58h	PSP1<0>	PSP2<0>	PSP3<0>		YINS[2:0]		GS10	FDFLOWZ
ID_SM	ID (Read Only)	11111000=F8h	ID_SM [7:0] <00110101>							

Note: <0000 0000> is the default 8-bit values for the register. Register address is in 8-bit (1 byte) designation.

REGISTER DESCRIPTION

SERIAL PORT REGISTER DEFINITIONS

Throughout the specification, the notation RR:BB is used, where RR is the register, and BB is the bit in the register. For example, PD:DS denotes the DS bit in the PD Register. Addresses are shown MSB first.

Power Down (PD)
Address = 0000 0100 = 04h

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7 - 6</td><td>TPC/D/E/H[1:0]</td><td>
TPC/TPD Control:
<table>
<tr><th>FC:T_SPC</th><th>SG</th><th>PD[7:6]</th><th>TPC/$\overline{\text{TPC}}$</th><th>TPD/$\overline{\text{TPD}}$</th><th>TPH/$\overline{\text{TPH}}$</th></tr>
<tr><td>0</td><td>0</td><td>XX</td><td>Disabled</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>1X</td><td>(Dp/Dn)out</td><td>(Cp/Cn)out</td><td>(DpDn)blos.out</td></tr>
<tr><td>0</td><td>1</td><td>0X</td><td>Disabled</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>1</td><td>X</td><td>00</td><td>Disabled</td><td>Disabled</td><td>Disabled</td></tr>
<tr><td>1</td><td>X</td><td>01</td><td>(Dp/Dn)in</td><td>(Cp/Cn)in</td><td>(DpDn)blos.out</td></tr>
<tr><td>1</td><td>X</td><td>10</td><td>(Dp/Dn)out</td><td>(Cp/Cn)out</td><td>(Dp/Dn)blos out</td></tr>
<tr><td>1</td><td>X</td><td>11</td><td>(AGC)out</td><td>(AGC)out</td><td>Disabled</td></tr>
</table>
TPE Control:
<table>
<tr><th>FC:T_SPC</th><th>CM1:AGCT</th><th>HYED</th><th>AGCHE</th><th>PD[7:6]</th><th>TPE/$\overline{\text{TPE}}$</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>X</td><td>XX</td><td>Disabled</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>X</td><td>00</td><td>Disabled</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>X</td><td>01,10,11</td><td>Disabled</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>X</td><td>01</td><td>FLOW_Z</td></tr>
<tr><td></td><td></td><td></td><td></td><td>10</td><td>$\overline{\text{FDCO}}$</td></tr>
<tr><td></td><td></td><td></td><td></td><td>11</td><td>$\overline{\text{UFDC}}$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>01,10,11</td><td>Hi-Y</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>01,10,11</td><td>AGCHOLD_TA</td></tr>
</table>
Note: Dp/Dn = Normal filter
Cp/Cn = Differentiated filter
(AGC) out = Filter bypassed
</td></tr>
<tr><td>5 - 4</td><td>ASEL[1:0]</td><td>Output select for ATO test point
00 = ATO Buffer shut down
01 = DAC Output enabled
10 = Amplitude asymmetry factor enabled
11 = Reference voltage (~MAXREF/2)</td></tr>
<tr><td>3</td><td>ACSWT</td><td>Internal ac coupler switch over at vcolock:
0 = Enables switch over to sampled data mode at vcolock
1 = Always in continuous mode</td></tr>
<tr><td>2</td><td>TB</td><td>Time base generator power down</td></tr>
<tr><td>1</td><td>DS</td><td>Data separator power down</td></tr>
<tr><td>0</td><td>PD</td><td>AGC, Filter, pulse detector, and servo power down</td></tr>
</table>

Bits 2 - 0: 1 = power down; 0 = power up

Data Filter Cutoff Register (FC)
Address = 0001 0100 = 14h

BIT	NAME	DESCRIPTION
7	T_SPC	Controls test points as shown in PD register definition
6 - 0	FC[6:0]	Filter cutoff frequency in non-servo mode $18 \leq FC \leq 127_{dec}$ Filter cutoff frequency = 1.00219 + 0.49586 • FC_DAC

Servo Filter Cutoff Register (FCS)
Address = 0010 0100 = 24h

7	SVCAL	Servo calibration mode: 0 = No calibration 1 = Calibration enabled
6 - 0	FCS[6:0]	Filter cutoff frequency in servo mode $18 \leq FCS \leq 43_{dec}$ Servo filter cutoff frequency = 1.00219 + 0.49586 • FCS_DAC

Data Mode Filter Boost Register (FB)
Address = 0011 0100 = 34h

7	ENTAD	Enable thermal asperity detection 0 = Disable 1 = Enable
6 - 0	FB[6:0]	Filter boost setting in non-servo mode 0 ≤ FB ≤ 127 dec Boost (dB) = 20 • Log(0.043448 • FB - 0.0000337 • FB • FC +1)

Filter Asymmetric Zero and Servo Mode Filter Boost Register (FBS)
Address = 0100 0100 = 44h

7 - 6	FBS[1:0]	Filter boost setting in servo mode, $0 \leq FBS \leq 3_{dec}$
5 - 0	FGD[4:0]	Filter group delay equalization magnitude Group delay Δ% = 0.9783 • FGD4:0 - 0.665

EPR4 Detector Constant Register (VEPR4)
Address = 0101 0100 = 54h

7 - 4	“-1.5” Constant	0000 - Nominal Value = -1.5 in 2.5% increments (2’s compliment) 0111 = -1.5 • (1.0 + 7 • 2.5%) = - 1.7625 1000 = -1.5 • (1.0 - 8 • 2.5%) = - 1.2000
3 - 0	“+0.5” Constant	0000 - Nominal Value = +0.5 in 2.5% increments (2’s compliment 0111 = +0.5 • (1.0 + 7 • 2.5%) = 0.5875 1000 = +0.5 • (1.0 - 8 • 2.5%) = 0.4000

REGISTER DESCRIPTION (continued)

Data Level Threshold Register (LD)
Address = 0110 0100 = 64h

BIT	NAME	DESCRIPTION
7	DSCAN	When in read, defect scan enable 1 = FIR output is sliced and decisions mixed into the output of the survival register. Any dropout is detected and flagged by the NRZ7 pin in read mode. 0 = Normal operation when in write 0 = Normal 1 = “0” fed to precoder until valid pattern; forces the precoder to a known state, i.e., no write data till training.
6	TARGB	Data AGC hold from RGB to SFC 0 = Normal 1 = Data AGC held from the falling edge of RG to SFC of the next read
5 - 0	LD[5:0]	Data level qualification threshold voltage CM4: ALE = 0 (Fixed levels) Lth = 10.7996 • LD + 4.8604 [mV] before SFC Lth = 7.636 • LD + 3.4368 $16 \leq LD \leq 48$ dec after SFCC M4:ALE = 1 (Adaptive levels) after SFC Lth(%) = 1.574 • LD

Servo Level Threshold Register (LDS)
Address = 0111 0100 = 74h

7 - 6	SAGCL[1:0]	Servo mode AGC level control 00 = 1.40 Vp-pd 01 = 1.30 Vp-pd 10 = 1.20 Vp-pd 11 = 1.10 Vp-pd
5 - 0	LDS[5:0]	Servo level qualification threshold voltage LSth = 11.1 • LDS - 4.2 [mV]

Test Mode Register 1 (TM1)
Address = 1000 0100= 84h

BIT	NAME	DESCRIPTION				
7	EFR	Sample clock source: 0 = Sample clock is from the DS VCO, normal operation 1 = Sample clock is from the TBG output, a test mode				
6	ECP	0 = Normal 1 = Enable charge pump test				
5-3	TP[3:1]	Multiplexed test point selection				
		Function	**TPA, $\overline{\text{TPA}}$**	**TPB, $\overline{\text{TPB}}$**	**TPF, $\overline{\text{TPF}}$**	**TPG, $\overline{\text{TPG}}$**
	0 0 0	Test Points Off	high impedance	high impedance	high impedance	high impedance
	0 0 1	1+D EPR4 samples	(1+D) Phase 1	(1+D) Phase 0	high impedance	high impedance
	0 1 0	PR4 Eq.,Veq and PhDet	FIR Phase 0	FIR Phase 0	Equalizer Control (KM1)	Phase Detect Out
	0 1 1	PR4 Eq., VCO/2 or TBG	FIR Phase 0	FIR Phase 0	DS VCO/2 if RG=1 TBG Fout if RG=0	Phase Detect out
	1 0 0	SURVout, Max Decsn	SURVout before XOR	SURVout	Maximum Metric Decision MSB, 2nd MSB ,LSB, Hi_Z	
	1 0 1	Metric Outputs	Met0, Met1	Met2,Met3	Met4,Met5	Met6,Met7
	1 1 0	Met.Out & Max.Decsn	Met0, Met1	Met2,Met3	Maximum Metric Decision MSB, 2nd MSB ,LSB Hi_Z	
	1 1 1	Met.Out	Met0, Met1	Met2,Met3	high impedance	high impedance
2	BYPSR	Bypass survival path register 0 = Normal; 1 = Bypass during read 0 = Normal; 1 = Bypass precoder during write				
1	DT	1 = TBG Phase detector pump down continuous pump down, for test use only: FLTR1 sinks current; $\overline{\text{FLTR1}}$ sources current 0 = Normal operating mode				
0	UT	1 = TBG Phase detector pump up continuous pump up, for test use onlyFLTR1 sources current; $\overline{\text{FLTR1}}$ sinks current 0 = Normal operating mode				

REGISTER DESCRIPTION (continued)

Test Mode Register 2 (TM2)
Address = 1001 0100= 94h

BIT	NAME	DESCRIPTION
7	ACCPLDE	AC Coupler disable: 0 = Normal, 1 = Disabled only for test.
6	RDTAGC	Enable VRDT MUX input and fix AGC gain at 24 dB 0 = Normal 1 = Mux VRDT input to decoder and Fix AGC gain at 24 dB
5	IOMAP	I/O Mapping 0 = Disable 1 = Enable
4	DIFFBF	Bypass TBG using high speed pecl differential buffer 0 = Disable ; 1 = Enable bypass
3	ENTRST	Enable the re-synchronization of internal RCLK by the rising edge of RG for read mode and WG for write mode.The write data pattern stream always begins at the same position from the rising edge of write gate. 0 = Disable;1 = Enable
2	SBAND	Dual 'AND' type sync byte detection. Sync byte is occurred when both sync bytes (91B1H & 9103H) is correctly detected. 0 = Normal operation (Dual 'OR' type detection), Default 1 = Enable dual 'AND' type detection. (TEST mode)
1 - 0	TSTSL[1:0]	ENDEC Internal signals can be monitored from NRZP pin by set of these control bits. 00 = PARITY output (default) 01 = Framing detect (& Sync. byte detect) signal from DIF. 10 = VCOLKDb 11 = EFLAG.

N Counter Register (N)
Address = 1010 0010 = A4h

7	FREFPS	0 = No fref prescaling normal operation 1 = Fref divided by 2 for internal AGC timings, intended for use when Fref > 25MHz
6 - 0	N[6:0]	N Counter: $2 \le N \le 127$

M Counter Register (M)
Address = 1011 0100 = B4h

7 - 0	M[7:0]	M Counter: $2 \le M \le 255$, $F_{TBG} = FREF \bullet \left[\frac{M + 1}{N + 1}\right]$

Data Rate Register (DR)
Address = 1100 0100 = C4h

BIT	NAME	DESCRIPTION
7	DSB	NRZ Flag at start of defect scan mode 0 = Normal operation 1 = Toggle NRZ1 for one RCLK time period to indicate beginning of defect scan mode at SFC
6 - 0	DR[6:0]	Data rate DAC value. $0 \leq DR \leq 127$ F_{vco} (MHz) = 17/16 Data Rate F_{vco} (MHz) = 8.5849 + 2.2947 • DR_DAC

Write Precomp Register (WP)
Address = 1101 0100 = D4h

7 - 4	WPC2[3:0]	Level 2 write precomp magnitude 0 -17% in linear increments; 0000 implies no Level 2 precompensation
3 - 0	WPC1[3:0]	Level 1 write precomp magnitude 0 - 34% in linear increments; Level 1 must be greater than or equal to Level 2 and not set to zero

Sample Loop Control Register (SLC)
Address = 1110 0100 = E4h

7	AEQADC	ADC done at the end of RG for readout at the serial port 0 = Normal mode (disabled) 1 = Enabled
6 - 5	SFC[1:0]	Sync field count -actual length of synch field must be greater than SFC specified here by at least one byte SFC Sync Field Count 00 64 01 80 10 96 11 128
4	AEGS	Adaptive equalizer loop time constant shift 0 = Equalizer loop time constant is the same in preamble and data fields 1 = Equalizer loop time constant is increased by ≅ 7X in the data field relative to the preamble field, i.e. loop gain is reduced to ≅ 1/7
3	AED	Enable adaptive equalizer on data field (Only valid if AEE bit = 1) 1 = Adaptive equalizer in use after sync byte detect 0 = Adaptive equalizer disabled after sync byte detect

Sample Loop Control Register (SLC) (continued)
Address = 1110 0100 = E4h

BIT	NAME	DESCRIPTION
2	AEE	Enable adaptive equalizer 1 = Adaptive equalizer enabled for use in preamble field, and after the preamble field if AED bit = 1 0 = Adaptive equalizer disabled
1 - 0	AGC[1:0]	AGC Charge pump current in sampled AGC mode AGC Charge pump current = $\pm 3.2 \cdot 10^{-6} \cdot AGC \cdot DR/RR$

Damping Ratio Control Register (DRC)
Address = 1111 0100 = F4h

7	LOQEQG	Force low equalizer gain 0 = Normal 1 = Equalizer adaptation gain always low (i.e., 7x time constant)
6 - 0	DRC6:0]	Damping amplifier gain A = DRC • (0.7/127) Damping ratio = $\frac{A \cdot KVCO \cdot 0.25}{2\,\omega_n}$

FIR TAP Coefficient Register 1 (FIR1)
Address = 0000 0110 = 06h

7 - 4	Km1AD[3:0]	A/D Converted Km1 values made available at the end of A/D conversion; reset after the serial port read.
3 - 0	Km1PS[3:0]	Km1 Preset: (default <0100>)If AEE = 0, Km1 is forced into the equalizer as a fixed weight; Only negative gain settings are allowed. 0000 = Tap gain is nominally zero 1111 = Largest negative gain. If AEE = 1, Km1 setting is used as a starting point for adaptation.

FIR TAP Coefficient Register 2 (FIR2)
Address = 0001 0110 = 16h

7	QaeprEN	0 = No amplitude asym. correction on EPR4 Viterbi 1 = Correction as defined in QaEPR[2:0] Dac below
6 - 4	QaEPR[2:0]	Asym. correction amount of EPR4 Viterbi detector in 12.5% increment (2's compliment) 011 = Nominal • (1+ 3 • 12.5%) = 1.375 • nominal 000 = Nominal correction factor 100 = Nominal • (1- 5 • 12.5%) = 0.500 • nominal
3 - 0	Km2[3:0]	Equalizer outer tap multiplier gain (default <0100>) Km2 = 0.01875 • Km2, where Km2 is in 2's compliment. Gain range is -0.15 to +0.13125 with resolution of 0.01875.

Mode Control 1 Register (CM1)
Address = 0010 0110 = 26h

BIT	NAME	DESCRIPTION
7	RCK2X	0 = Rclk drive at 1x 1 = Rclk drive at 2x
6	AGCT	AGC Timing control (default <0>) 0: AGC Timing externally generated 1: AGC Timing internally generated
5	WGP	Write gate polarity. 1 = Inverted ($\overline{WG}$); 0 = Noninverted (WG)
4	TRSQ	Training sequence generation control 0: Training sequence and sync byte generated externally 1: Training sequence and sync byte generated internally, STRB(2:0) must be 001.
3	BT	Bypass time base generator 1 = Data synchronizer reference frequency is FREF input 0 = Data synchronizer reference frequency is TBG output
2	SD	Scrambler disable 1 = Disabled 0 = Enabled
1	GS	DS Phase detector gain switching 1 = Disabled (gain stays high after SFC) 0 = Enabled
0	DWDR	Enable direct write from byte-wide NRZ 1 = Enabled 0 = Disabled Also if in read mode 1 = Enable direct read mode(bypass decoder, descrambler) 0 = Disabled.

Mode Control 2 Register (CM2)
Address = 0011 0110 = 36h

7	DIBITPOL	Set the polarity of first transition before Dibit detect signal 0 = Set the first transition to negative. 1 = Set the first transition to positive.
6 - 4	IGAIN[2:0]	Interegator gain control Gain (V/Vp-pd) = 1.6 + 0.1 • IGAIN, $0 \leq IGAIN \leq 7$
3	PWCTR	$\overline{RDS}$ Output pulse width. 0 = 15 ns; 1 = 27 ns
2	PDM	Pulse detector mode 1 = Hysteresis qualifier 0 = Window qualifier

Mode Control 2 Register (CM2) (continued)
Address = 0011 0110 = 36h

BIT	NAME	DESCRIPTION
1	DIBDEN	0 = Dibit detect disabled 1 = Dibit detect enabled
0	SERI	Servo input and RDS output polarity control 0: Normal filter outputs routed to servo; $\overline{\text{RDS}}$ - active low 1: Differentiated filter outputs routed to servo; RDS - active high

Mode Control 3 Register (CM3)
Address = 0100 0110 = 46h

7	FERA	Enable/force illegal pattern detection/error flag even without thermal asperity detect. 0 = Disable 1 = Force illegal pattern detection, even if thermal asperity detect is not present
6	SEED	0 = Scrambler seed is 3FFh 1 = Scrambler seed is 2AAh
5 - 0	STRB[5:0]	Set the number of 17bit long pads between two sync bytes. In Write mode, STRB[5:0]h of pads should be written between two sync bytes. No pad is written between two sync bytes when STRB[5:0] = 0.

Mode Control 4 Register (CM4)
Address = 0101 0110 = 56h

7	ALE	Enable adaptive level qualification in decision directed phase detector 0 = Always use fixed level qualification 1 = Switch to adaptive mode at vcolock
6 - 5	TC[2:1]	Adaptive level qualification threshold time constant for decision directed phase detector and qasym factor time constant (both valid After SFC): TC2 TC1 Time Constant 0 0 150 ns 0 1 300 ns 1 0 450 ns 1 1 600 ns
4	FRZQASYM	Freeze qasym acquisition at SFC
3	QalvlEN	0 = No amplitude asym correction on level threshold or 3-level slicer 1 = Correction as defined in QaLVL[2:0] DAC below
2 - 0	QaLVL[2:0]	Asym. correction amount of level threshold in 12.5% increment (2's compliment) 011 = Nominal • (1+ 3 • 12.5%) = 1.375 • nominal 000 = Nominal correction factor 100 = Nominal • (1- 4 • 12.5%) = 0.500 • nominal

Thermal Asperity Register 1 (TA1)
Address = 0110 0110 = 66h

BIT	NAME	DESCRIPTION
7	TADE	Enable TA detect when RG or SG is high 0 = TAD is enabled only when RG or SG is high 1 = TAD is enabled and always ready
6	TAIO	Thermal asperity detect (TAD) pin input/output select 0 = Internal TAD output 1 = External TAD input
5	TAIDLE	Thermal asperity idle mode control 0 = No TA detection or suppression in idle mode 1 = TA Detection and suppression in idle mode
4	TARG	Thermal asperity detection and suppression between RG and RGB 0 = TA Detection and suppression from SFC to falling RG. 1 = TA Detection and suppression from rising RG to falling RG
3	AGCHE	AGC and AC_Coupler Hold Enable: 0 = Normal operation 1 = Hold AGC gain and AC_Coupler over thermal asperity
2	TAPLLGS	Control gear shift in TA event: 0 = Normal operation 1 = Gearshift PLL over thermal asperity
1 - 0	PLLHE[1:0]	PLL Hold control: 00 = Normal operation 01 = Hold PLL over thermal asperity 10 = Hold PLL during TAD 11 = Deassert internal PLLHOLD signal by the falling edge of internal ERROR FLAG

Thermal Asperity Register 2 (TA2)
Address = 0111 0110 = 76h

7	HYED	Hi-Y Enable, dynamic mode 0 = Disable Hi-Y over thermal asperity detect 1 = Invoke Hi-Y as defined by HYTMR, when RG = 1 and thermal asperity is detected (on-the-fly mode)
6 - 5	HYES[1:0]	Hi-Y Enable, static mode 00 = Normal operation (No activation of Hi-Y) 01 = Invoke Hi-Y when SG = L (retry mode) 10 = Invoke Hi-Y when SG = H (retry mode) 11 = Invoke Hi-Y.
4	SVHY	Hi-Y In servo mode 0 = De-activate Hi-Y on TA detect in servo mode 1 = Activate Hi-Y on TA detect in servo mode as defined in HYTMR
3 - 0	TATH[3:0]	Thermal asperity threshold voltage control: threshold voltage (mV) = 51.59 • TATH + 697 $0 \leq TATH \leq 15$

REGISTER DESCRIPTION (continued)

Thermal Asperity Register 3 (TA3)
Address = 1000 0110 = 86h

BIT	NAME	DESCRIPTION
7 - 6	HYTMR[1:0]	Hi-Y Period = 0.943 • HYTMR + 1.0757 µs
5 - 3	YIN[2:0]	Dynamic high admittance control in non-servo mode (SG = Low). Yin (Siemens) = 1/720 + YIN/2538, 0 ≤ YIN ≤ 7
2 - 0	TATMR[2:0]	PLL/AGC Hold time duration during thermal asperity T_{hold} (µs) = 0.12 • TATMR + 0.273, 0 ≤ TATMR ≤ 7

Thermal Asperity Register 4 (TA4)
Address = 1001 0110 = 96h

7	RDSMUX	TAD, EFLAG Mux'd onto RDS, PPOL pins 0 = Mux TAD and EFLAG onto RDS and PPOL pins when SG = 0 1 = Use TAD and NRZP pins only,
6	FADIS	Fast Attack disable during FastRec = Low 0 = Normal 1 = Fast Attack disable during FastRec = Low
5	UHIY	Ultra Hi-Y mode enable bit 0 = Normal 1 = Ultra Hi-Y enable during UHIY/SQEN period. Sets Hi-Y to 111 and Low_Z in AGC.
4	SQEN	Squelch enable 0 = Normal 1 = Squelch enable during UHIY/SQEN period.
3	FOSNUL	Enables Special Fast Offset Null mode from the falling edge of TAD to the end of HiY period 0 = Normal 1 = Fast Offset Null enable
2	SGUHY	Enable Ultra Hi-Y and Squelch during SG = High 0 = Normal 1 = Ultra Hi-Y and Squelch enable during SG = High
1-0	SQTMR[1:0]	UHIY/Squelch time duration during thermal asperity. $T_{UHIY/SQ}$[µSec] = 0.16 + 0.12 • SQTMR

Amplitude Asymmetry Correction and Dibit Detector Time Constant (ASYM)
Address = 1010 0110 = A6h

BIT	NAME	DESCRIPTION
7 - 5	Dibit Enable Time DBT[2:0]	DBT[2:0] Ret.OS.Pulse.Width Implied Frequency 000 42 ns 11.9 MHZ 001 80 ns 6.25 MHZ 010 120 ns 4.16 MHZ 011 160 ns 3.12 MHZ 100 190 ns 2.63 MHZ 101 220 ns 2.27 MHZ 110 245 ns 2.04 MHZ 111 280 ns 1.79 MHZ
4	ASYMP	0 = Positive: Reduce the positive peak to negative peak level 1 = Negative: Negative peak larger than positive peak
3-0	ASYM(3:0)	Amplitude asymmetry correction magnitude. Asymmetry Correction (%) = 2 • ASYM, 0 ≤ ASYM ≤ 15

Channel Quality Monitor Register 1 (CQM1)
Address = 10110110 = B6h

7 - 0	CQMQ[15:8]	Channel quality monitor counter (MSB 8 bits) read only bits. reading this register initilizes internal CQM counter.

Channel Quality Monitor Register 2 (CQM2)
Address = 11000110 = C6h

7-0	CQMQ[7:0] Read Only Bits.	Channel quality monitor counter (LSB 8 bits)

Channel Quality Monitor Register 3 (CQM3)
Address = 1101 0110= D6h

7	SGBTMR	0 = Normal 1 = Allows servo timings on the falling edge of SG
6	PLSEN	0 = Normal 1 = Allows servo pulses to come out even during STROBE
5 - 4	CQMRGT	CQM RG Time or SG time (when CQMCTRL = 100) 00 = Accumulate the CQM count over 16 RG (or SG) period 01 = Accumulate the CQM count over 144 RG (or SG) periods 10 = Accumulate the CQM count over 526 RG (or SG) periods 11 = Accumulate the CQM count over 1008 RG(or SG) periods

Channel Quality Monitor Register 3 (CQM3) (continued)

BIT	NAME	DESCRIPTION
3	SURVSEL	0 = Normal 1 = Forces the selection of surv. path at its output by SURVSTA below
2 - 0	CQMCTRL/ SURVSTA	When SURVSEL=0; 000 = Disable CQM function, x01 = Counts maxmet inconsistency events in CQM counter, x10 = Counts Maxmet M2SB inconsistency events in CQM counter, x11 = Counts maxmet MSB inconsistency evnets in CQM counter, In the above three cases the counter starts from SBD(x=0) or VCOLOCK (x=1). 100 = CQM input from AGC comparator intended for use in BLOS adjustment

Time Control Register (TC)
Address = 1110 0110 = E6h

7 - 6	UFDC[1:0]	Enable ultra fast decay current Ultra fast decay current (µA) = 0.72 • UFDC[1:0]
5 - 3	LZT[2:0]	Low-Z time LZT2 LZT1 LZT0 FREF periods 0 0 0 2 0 0 1 3 0 1 0 5 0 1 1 7 1 0 0 10 1 0 1 13 1 1 0 16 1 1 1 20
2 - 0	FRT[2:0]	Fast recovery time FRT2 FRT1 FRT0 FREF periods 0 0 0 4 0 0 1 6 0 1 0 10 0 1 1 14 1 0 0 20 1 0 1 26 1 1 0 32 1 1 1 40

Time Control Register for Servo (TCS)
Address = 1111 0110 = F6h

BIT	NAME	DESCRIPTION
7	LZTCR	0 = 15 : 1 ratio ; Rindiff = 8.3 Ω : 0.55 Ω at VIA/$\overline{\text{VIA}}$ 1 = 5 : 1 ratio ; Rindiff = 2.7 Ω : 0.55 Ω at VIA/$\overline{\text{VIA}}$
6	UFDSEL	0 = Only during SG high; 1 = Always use ultra fast decay
5 - 3	LZTS[2:0]	Low-Z time in servo mode LZTS2 LZTS1 LZTS0 FREF periods 0 0 0 2 0 0 1 3 0 1 0 5 0 1 1 7 1 0 0 10 1 0 1 13 1 1 0 16 1 1 1 20
2 - 0	FRTS[2:0]	Fast recovery time in servo mode FRTS2 FRTS1 FRTS0 FREF periods 0 0 0 4 0 0 1 6 0 1 0 10 0 1 1 14 1 0 0 20 1 0 1 26 1 1 0 32 1 1 1 40

Special Test Mode Register 1 (STM1)
Address = 00001000= 08h

7-6	TC8DLY[6:5]	Additional Forced Synch Byte Detection Byte Delay Count bit. See the description bit 7-3 of STM2 Register for detail function
5 - 4	SPLITFF[1:0]	Split Forced Framing control 00 = Enable Forced framing detection at ALL read cycle (Default) 01 = Enable Forced framing detection at only EVEN read cycle 10 = Enable Forced framing detection at only ODD read cycle 11 = Reserved
3	FRCSUR	When TSURV = 1: 0 = Force survival path register input to zero 1 = Force survival path register input to one

Special Test Mode Register 1 (STM1) (continued)

BIT	NAME	DESCRIPTION
2	TSURV	0 = Normal 1 = Test Survival path register as dictated by FRCSUR bit
1	MET07R	0 = Normal 1 = Resets all metric states except for state “0” and “7” and common mode feedback is derived off “0” and “7” metric states
0	CNSTENB	0 = Normal 1 = EPR4 Metric constants to zero

Special Test Mode Register 2 (STM2)
Address = 00011000= 18h

7 - 3	TC8DLY[4:0]	Forced Synch Byte Detection Byte Delay Count When RCRVM[1:0] = 11 AND if SB#1 is NOT detected before the time period given by TC8DLY[6:0] (0 to 127) byte clocks after the RG assertion expires, RG is internally reasserted and starts looking for SB#2. When RCRVM[1:0] = 10, this, in conjunction with TC2DLY[1:0] bits and ODDEVEN bit, allows precise placement of Sync.Byte Detection.
2 - 1	TC2DLY[1:0]	Forced Synch Byte Detection 2Tvco Delay Count 00 = Disable, Normal The delayed SFC signal (by TC8DLY[6:0]) is delayed number TC2DLY[1:0] (0 to 3) by 2Tvco clock. This would, in conjunction with the ODDEVEN bit, enable the control of the occurrence of Sync.Byte Detection in the proper 2Tvco period.
0	ODDEVEN	Forced Synch Byte Detection ODD/EVEN control The even or odd order of the force sync. byte can be controlled by this bit. 0 = Detect at ODD 1 = Detect at EVEN

Base Line Offset - Data Mode- Register (BLOD)
Address = 0010 1000= 28h

7	BOSDP	Baseline offset polarity: 0 = Negative offset 1 = Positive offset
6 - 0	BLOSD[6:0]	Magnitude of offset Blos = 2.37 • BLOSD + 8.46

Base Line Offset - Servo Mode- Register (BLOS)
Address = 0011 1000= 38h

BIT	NAME	DESCRIPTION
7	BOSSP	Baseline offset polarity: 0 = Negative offset 1 = Positive offset
6 - 0	BLOSS[6:0]	Magnitude of offset Blos = 2.37 • BLOSS + 8.46

Misc. Register 1
Address = 0100 1000= 48h

7 - 6	RCVRM[1:0]	Read recovery mode: 00 = Normal conventional single header mode. (Default) 01 = Reserved (test mode) 10 = Enable force framing mode 11 = Enable read recovery (dual header) read mode
5	RPMEb	EPR4 Read power management: 0 = on; 1 = off (normal)
4	RPMSb	SDP Read power management: 0 = on; 1 = off (normal)
3	WPMb	Write power management: 0 = on; 1 = off (normal)
2 - 1	SVPMb	Servo power management: 00 = Servo power shutdown 32 fref clock periods after $\overline{SG}$ 01 = Servo power shutdown 64 fref clock periods after $\overline{SG}$ 10 = Servo power shutdown 128 fref clock periods after $\overline{SG}$ 11 = No servo power management (normal)
0	FdmpEn	Enables fast Dmpq gain during 8Tc's after RG 0 = Disabled 1 = Enabled

Misc. Register 2
Address = 0101 1000= 58h

7	PSP1	Preamp serial port transfer function thru PSDATA, PSCLK, and PSDATA pins: 0 = Normal: allows serial port transfer if SDEN = 1 and RG = WG = SG = 0 1 = Disable serial port transfer (Hi-Z on outputs)
6	PSP2	Preamp serial port output control when disabled. 0 = Tri-state; 1 = Drive low
5	PSP3	Envoke TI mode of serial port transfer (Write) 0 = Normal; 1 = TI mode (See serial port description.)
4 - 2	YINS[2:0]	Dynamic high admittance control in servo mode (SG = High). Yin (Siemens) = YINS/2230 + 1/10,000, $0 \le YIN \le 7$

Misc. Register 2 (continued)

BIT	NAME	DESCRIPTION
1	GS10	DS PLL Gear shift factor: 0 = 5, 1 = 10
0	FDFLOWZ	Filter fast offset correction (Lowz) time extension in AGC internal timing mode. 0 = LowZ time will extend to the end of FASTREC when AGCT=1. 1 = Normal: LowZ time is until the rising edge of FASTREC

ID_SM ID Register (Read Only)
Address = 1111 1000 = F8h

7 - 0	ID_SM	Chip ID writing DAh resets all registers to default

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA		AGC / Filter analog circuit supply
VPF		Time base generator PLL digital circuit supply
VPT		Time base generator analog supply
VPP		Data separator PLL analog circuit supply
VPD		TTL Buffer I/O digital supply
VPC		Internal ECL, CMOS logic digital supply
VPS (x2)		Sampled data processor and EPR4 detector supply
VNA (x2)		AGC / Filter analog circuit ground
VNF		Time base generator PLL digital circuit ground
VNT		Time base generator analog ground
VND		TTL Buffer I/O digital ground
VNC		Internal ECL, CMOS logic digital ground
VNS (x3)		Data separator PLL, sampled data processor and EPR4 detector ground

ANALOG INPUT PINS

VIA, $\overline{\text{VIA}}$		AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins

ANALOG OUTPUT PINS

TPA, $\overline{\text{TPA}}$		TEST PINS: Emitter output test points. Various signals are multiplexed to these test points by the TP bits in the TM1 Register. The signals include the equalizer control voltage and output, various timing loop control signals and the viterbi survival Register outputs. The test points are provided to show how the signal is being processed. Internal “pull down” resistors to ground are provided . To save power when not in test mode, the TP bits must be set to “0”.
TPB, $\overline{\text{TPB}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the other phase of the interleaved signals (set by TM1:TP bits)
TPC, $\overline{\text{TPC}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the normal outputs of the continuous time filter or AGC output. These pins may also be driven with DP/DN like signals for back end testing (set by PD:TPC bits)
TPD,$\overline{\text{TPD}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the differentiated output of the continuous time filter or AGC output. These pins may also be driven with CP/CN like signals for back end testing. (set by PD:TPC bits)
TPE		TEST PINS: Emitter output test point similar to TPA. FWR output when enabled. (set by PD:TPC bits)

ANALOG OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
TPF, $\overline{\text{TPF}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the other phase of the interleaved signals. (set by TM1:TP bits)
TPG, $\overline{\text{TPG}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the other phase of the interleaved signals. (set by TM1:TP bits)
TPH, $\overline{\text{TPH}}$		TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. The pins are used to look at the DP/DN signal after the application of base line offset. (set by PD:TPC bits)
ATO		ANALOG TEST OUT: This test point output provides a monitor of the equalizer quality signal, the amplitude asymmetry signal, and the DAC outputs. The selected output is determined by the ASEL bits in the PD Register. If the DAC outputs are selected, the last DAC written to by the serial control Register is the DAC monitored. Signal at ATO is referenced to Vcc/2 or ATO reading at ASEL set to 11. 00 powers down ATO buffer.
A, B, C, D		SERVO OUTPUTS: These outputs are the amplified and offset versions of the voltages captured on the servo hold capacitors. They are offset by an internally generated 0.27 V baseline. In servo calibration mode (FC:T_SPC=1, PD:TPC=0) Vol's + reference voltage ªMaxref/2 are brought to these pins.
MAXREF		SERVO REFERENCE OUTPUT: +3.0 V DC reference voltage that represents the maximum output voltage for the A, B, C, and D outputs. Can be used as the reference for an external A/D converter.

ANALOG CONTROL PINS

BYPD		The data AGC integrating capacitor, CBYP, is connected between BYP and VPA. This pin is used in non-servo mode (SG = 0).
BYPS		The servo AGC integrating capacitor, CBYPS, is connected between BYPS and VPA. This pin is used when in servo read mode (SG = 1).
FLTR1, $\overline{\text{FLTR1}}$		TBG PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components.
FLTR2, $\overline{\text{FLTR2}}$		DS PLL LOOP FILTER: Differential connection points for the data separator PLL loop filter capacitor.
RR		CURRENT REFERENCE RESISTOR INPUT: For 240 Mbps. operation an external 10.0 kΩ 1% resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and the time base generator DACs. 10.0 kΩ 1% resistor should be used for 240 Mbps. operation.
RX		FILTER REFERENCE RESISTOR INPUT: An external 10.2 kΩ 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter DACs.
VRC		AGC REFERENCE VOLTAGE: VRC is a bandgap derived reference referred to VPA1.

DIGITAL INPUT PINS

NAME	TYPE	DESCRIPTION
LOWZ		LOW-Z mode INPUT: TTL compatible control pin which, when pulled high, the input impedance is reduced to allow rapid recovery of the input coupling capacitor, the internal AC coupling time constant is reduced to 250 ns, and the AGC gain is squelched. When pulled low, keeps the AGC amplifier and filter input impedance high. An open pin is a logic high.
FASTREC		FAST RECOVERY: TTL compatible control pin which, when pulled high, puts the AGC charge pump in the fast recovery mode. An open pin is a logic high.
$\overline{\text{PDWN}}$		POWER DOWN CONTROL: CMOS compatible power control pin. When set to logic low, the entire chip is in sleep mode with all circuitry, except the serial port, shut down. This pin should be set to logic high in normal operating mode. Selected circuitry can be shut down using the PD Register. There is no default value for this pin.
$\overline{\text{HOLD}}$		AGC HOLD CONTROL INPUT: TTL compatible control pin which, when pulled low, holds the AGC amplifier gain constant by turning off the AGC charge pump. The AGC loop is active when this pin is either at high or open.
EQHOLD		EQUALIZER HOLD CONTROL INPUT: TTL compatible control pin which, when pulled high causes the present adaptive equalizer tap weights to be held until the input is set low. An open pin is at logic high.
FREF		REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an ac coupled ECL signal. When the EFR bit in the CT Register is set, FREF replaces the VCO as the input to the data separator.
WCLK		WRITE CLOCK: TTL compatible input that latches in the data at the selected NRZ interface on the rising edge. Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. An open pin is at logic high.
RG		READ GATE: TTL compatible input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the read mode/address detect sequences. A low level selects the time base generator output. An open pin is at logic high.
WG		WRITE GATE: TTL compatible input that, when pulled high, enables the write mode. An open pin is at logic high.
SG		SERVO GATE: TTL compatible input that, when pulled high, enables the servo read mode. An open pin is at logic high.
VRDT		VITERBI READ DATA: A TTL or ac coupled PECL compatible input to the data separator back end, for testing purposes only. This pin is controlled by the VRDT bit in the CT Register.

DIGITAL INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{DWR}$		DIRECT WRITE mode 2 ENABLE: Enables DWI, $\overline{DWI}$ inputs to the write data flip-flop when input is low. TTL levels. Open pin is at logic high.
DWI, $\overline{DWI}$		DIRECT WRITE INPUTS: Inputs connect to the toggle input of the write data flip-flop when $\overline{DWR}$ is low. PECL input levels. Can be left open.
BFREF, $\overline{BFREF}$		BYPASS FREF INPUTS: High speed differential PECL input buffer for use in bypassing the TBG.
INTEG		SERVO INTEG INPUT: Active high enable for charging an individual hold capacitor during a servo burst capture. The falling edge of INTEG will increment an internal counter that determines which of the four hold capacitors will be charged during the next integ pulse. TTL levels. Open pin is at logic high.
$\overline{RESET}$		RESET CONTROL INPUT: Active low reset for discharging of the four internal servo burst hold capacitors for channels A, B, C, and D. TTL input levels. Open pin is at logic high.

DIGITAL BI-DIRECTIONAL PINS

NRZ0-7		BYTE WIDE NRZ DATA PORT: TTL compatible bi-directional input / output. Input to the encoder when WG is high. Output from the decoder when RG is high.
NRZP		NRZ DATA PARITY BIT: Active when in Byte Wide mode. TTL compatible bi-directional input / output. Generates even read parity when RG is high, and accepts even write parity when WG is high. Can be left open if not used. Also a multiplexed test point set by TM2:TSTSL
TAD		Thermal Asperity Detect Pin

DIGITAL OUTPUT PINS

RCLK		READ REFERENCE CLOCK: A multiplexed clock source used by the controller, . When RG is low, RCLK is synchronized to the time base generator output, F_{TBG}. When RG goes high, RCLK remains synchronized to F_{TBG} until the SFC is reached. At that time, RCLK is synchronized to the data separator VCO. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. TTL output levels.
$\overline{SBD}$		SYNC BYTE DETECT: Transitions low upon detection of sync byte. This transition is synchronized to the sync byte. Once it transitions low, $\overline{SBD}$ remains low until RG goes low, at which point it returns high. CMOS output.
WD, $\overline{WD}$		WRITE DATA: Write data flip-flop output. The data is automatically re-synchronized (independent of the delay between RCLK and WCLK) to the reference clock F_{TBG}, except in Direct Write mode 2. Differential PECL output levels.

DIGITAL OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{RDS}}$(RDS)		SERVO READ DATA: Read Data Pulse output for servo read data. Active low CMOS output. Output active when SG is high, and high when SG is low.
PPOL		SERVO READ DATA POLARITY: Read Data Pulse polarity output for servo read data. Active high CMOS output. Negative pulse = low, positive pulse = high. Output active when SG is high.
PERR		PARITY ERROR DETECT: Transitions high when a parity error is detected at the byte wide NRZ interface. CMOS output.

SERIAL PORT PINS

SCLK		SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. CMOS input levels.
SDATA		SERIAL DATA: Input/output pin for serial data; 8 address bits first followed by 8 data bits. The address and data bits are entered LSB first, MSB last. CMOS input/output levels.
SDEN		SERIAL DATA ENABLE: A high level input enables data loading. The data is internally parallel latched when this input goes low. CMOS input levels.
PSCLK		SERIAL DATA CLOCK: to preamp: Positive edge triggered clock output for the serial data transfer to preamp. CMOS output levels.
PSDATA		SERIAL DATA to preamp: Input/output pin for serial data; 8 address bits first followed by 8 data bits. The address and data bits are entered LSB first, MSB last. CMOS input/output levels.
PSDEN		SERIAL DATA ENABLE to preamp: A high level output to preamp enables data loading. CMOS input levels.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING	UNITS
Positive 5.0 V supply voltage (Vp)	-0.5 to +7	V
Storage temperature	-65 to +150	°C
Solder vapor bath	215 °C, 90 s, 2 times	-
Junction operating temperature	+135	°C
Output pins	+,- 10	mA
Analog pins	+,- 10	mA
Voltage applied to other pins	-0.3 V to Vp + 0.3	V

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5 V < POSITIVE SUPPLY VOLTAGE < 5.5 V, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

POWER SUPPLY CURRENT AND POWER DISSIPATION

Outputs and test points open for all power tests. Test points disabled (TP bits in CT Register set to zero). Maximum Data rate. VP = 5.0 V RDPWR = WRPWR = 1 is assumed for power management.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
ICC (VPn) Typical @ 5.0 V Max @ 5.5 V	Ta = 70 °C RG = 1 Without power management With power management During idle		 358 359 286	 456 456 360	mA
PWR Power dissipation normal operating modes	Ta = 70 °C RG=1 Without power management With power management During idle		 1976 1971 1589	 2300 2300 1978	mW
PWR, Pulse detector, filter off PD:PD = 1	Ta = 70 °C		826	1009	mW
PWR, Data separator off PD:DS = 1	Ta = 70 °C		568	667	mW

POWER SUPPLY CURRENT AND POWER DISSIPATION (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
PWR, Data separator & TBG Off PD:DS, PD:TB = 1	Ta = 70 °C		528	616	mW
Power up delay	From power up to all internal biaspoints stable, not tested on ATE			5.0	µs
Sleep mode	$\overline{\text{PDWN}}$ = low		0.66	5	mW
Recovery from idle mode: Under power management from RG active to SDP fully on from SG active to Pd_Qual fully on from WG active to write fully on			 30 50 10		ns

DIGITAL INPUTS

TTL COMPATIBLE INPUTS

Input low voltage (VIL)	Functional test on ATE			0.8	V
Input high voltage (VIH)	Functional test on ATE	2.0			V
Input low current (IIL)	VIL = 0.4 V	-0.4			mA
Input high current (IIH)	VIH = 2.4 V			100	µA

VRDT AND FREF INPUTS

Input low voltage (VIL)	Functional test on ATE			0.8	V
Input high voltage (VIH)	Functional test on ATE	2.4			V
Input low current (IIL)	VIL = 0.4 V	-0.2			mA
Input high current (IIH)	VIH = 2.4 V			500	µA

CMOS COMPATIBLE INPUTS
VPC = 5 V

Input low voltage (VIL)	Functional test on ATE			1.5	V
Input high voltage (VIH)	Functional test on ATE	3.5			V
Input leakage	Vin = GND, Vcc	-1		+1	µA

PSEUDO ECL COMPATIBLE INPUTS

Input low voltage, VIL	For ref. only, no ATE	VPA-2.0		VIH-0.25	V
Input high voltage, VIH	For ref. only, no ATE	VPA-1.1		VPA-0.4	V
Input current	For ref. only, no ATE	-100		+100	µA

ELECTRICAL SPECIFIICATIONS (continued)

DIGITAL OUTPUTS

CMOS OUTPUTS

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Output low voltage	IOL = +2 µA			0.45	V
Output high voltage	IOH = -100 µA	0.7•VPD			V

DIGITAL DIFFERENTIAL OUTPUTS (WD, $\overline{WD}$)

Output low voltage, VOLD	Iol = -2 µA	VPD2-2.1		VOHD-0.3	V
Output high voltage, VOHD	Ioh = -2 µA	VPD2-1.4		VPD2-0.5	V
Output sink current	WG = highz		-3.5		mA

TEST POINT OUTPUT LEVELS ATO BUFFER CHARACTERISTICS

Unless otherwise specified, measured at AO pin, each loaded with 5 pF. For reference only, no ATE test.

Reference voltage	ASEL[1:0]=[0 0],	Typ.-130 m	MAXREF/2	Typ.+130 m	V
Swing	From reference voltage Rload ≥ 10 kΩ	+1.2/-0.6			V
Source impedance			50		Ω
Drive capability	± refers to source/sink	+2/-2	+5/-3		mA

TPC/D/E BUFFER CHARACTERISTICS

Unless otherwise specified, measured at pin, each loaded with 5 pF. (Reference only - no ATE)

Swing	Rload ≥ 10kΩ	1.0		Vps-1.5	V
Source impedance			45		Ω
Output current		-3/+0.8			mA
Common voltage			2.5		V
TPC/$\overline{TPC}$, TPD/$\overline{TPD}$ Input bias voltage	Recommended input condition		VPA-1.5		V

TPA/B/F/G BUFFER CHARACTERISTICS

Unless otherwise specified, measured at pin, each loaded with 5 pF. (Reference only - no ATE)

Swing	Rload ≥ 10 kΩ		0.8		Vp-pd
Gain			0.9		V/V
Source impedance			45		Ω
Output current	Source only		-3/+1		mA
Common voltage	Equalizer output		VPA-1.7 -2 Vbe		V

SERIAL PORT TIMING
For reference only, no ATE

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
SCLK Data clock period, (TC)	Write operation	12.5			ns
	Read operation	40			ns
SCLK Low time, (TCKL)	SCLK Input < 10% Vcc	4			ns
SCLK High time, (TCKH)	SCLK Input > 90% Vcc	4			ns
Enable to SCLK, (TSENS)		9			ns
SCLK to disable, (TSENH)		9			ns
Data set-up time, (TDS)	Write operation	3			ns
Data hold time, (TDH)	Write operation	3			ns
SDEN Min. low time, (TSL)		25			ns
SCLK Fall to data valid (TSDV)	Read operation SCLK rise/fall time = 3 ns max load on SDATA less than 25 pF	2		17	ns
SDATA Hold time, (TSDH)	Read operation	20			ns
SDEN Fall to SDATA tristate (TSDTRI)	Read operation			20	ns

AGC CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

AGC AMPLIFIER
The input signals are AC coupled to VIA and $\overline{\text{VIA}}$. Integrating capacitor C_{BYP} = 1000 pF, is connected between BYP and VPA. Integrating capacitor C_{BYPS} = 1000 pF, is connected between BYPS and VPA. Unless otherwise specified, the output is measured differentially at TPC/$\overline{\text{TPC}}$ set to output DP/DN, Fin = 5 MHz, the filter frequency Fc = max and the filter boost at Fc = 0 dB. All specifications apply equally to servo and read mode prior to SFC.

TPC/$\overline{\text{TPC}}$ Voltage (When enabled to output the filter DP/DN signal)	VIA = 20 to 250 m Vp-pd 1,1,-1,-1,--- pattern 5 MHz ≤ Fc ≤ 40 MHz, Fin=Fc, Boost = 0 to 13 dB	1.19	1.4	1.61	Vp-pd
Gain range	±50 µA forced into BYP	3		64	V/V
Gain sensitivity	BYP voltage change		38		dB/V
Differential input resistance	LOWZ = low, LZCTR = 0	5.8	8.3	10.8	kΩ
	LOWZ = low, LZCTR = 1	1.7	2.1	4.0	kΩ
	LOWZ = high, LZCTR =X	250	715	1100	Ω
Single-ended input resistance No ATE, reference only	LOWZ = low, LZCTR = 0 ± 100 µA		6.5		kΩ
	LOWZ = low, LZCTR = 1 ± 100 µA		1.9		kΩ
	LOWZ = high, LZCTR = 1 ± 250 µA		520		Ω

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Output offset voltage change	Δ offset = |(offset at Gain = 64) - (offset at Gain = 3)|			200	mV
Input noise voltage	Gain = 24 dB Ω/Gain Fix mode Rs = 0 Ω Not ATE tested		14	19	nV/√Hz
CMRR	not ATE tested Gain = 24 dB Ω/ Gain Fix mode	35			dB
PSRR	Gain = 24 dB Ω/Gain Fix mode not tested on ATE	36			dB
TPC/$\overline{\text{TPC}}$ Voltage servo mode	SG = 1, SAGCL = 00	1.16	1.4	1.61	Vpdd
	SG = 1, SAGCL = 01	1.07	1.3	1.50	Vp-pd
	SG = 1, SAGCL = 10	0.97	1.2	1.38	Vp-pd
	SG = 1, SAGCL = 11	0.93	1.1	1.26	Vp-pd

AGC CONTROL SECTION

The input signals are DC coupled into TPC/$\overline{\text{TPC}}$, TPC/$\overline{\text{TPC}}$ enabled to drive DP/DN.RR = 10.0 kΩ

TPC/$\overline{\text{TPC}}$TPD/$\overline{\text{TPD}}$ common mode input voltage	For test only		VPA-1.5		V
Normal decay current, Id TPC = $\overline{\text{TPC}}$	FASTREC = low, SG = low	-25	-20	-15	µA
Servo mode normal decay current	FASTREC = low, SG = high TPC=$\overline{\text{TPC}}$	-25	-20	-15	µA
Fast rec decay current, Idf	FASTREC = high TPC = $\overline{\text{TPC}}$,	7 • Id	8 • Id	9 • Id	µA
Normal attack current, Ia	|TPC-$\overline{\text{TPC}}$| = 0.7875 V FASTREC = low	-21 • Id	-17 • Id	-13 • Id	µA
Fast attack current, Iaf	|TPC-$\overline{\text{TPC}}$| = 1.00 V, FASTREC = low	-165 • Id	-147 • Id	-107 • Id	µA
Fast rec attack current, Iafr	|TPC-$\overline{\text{TPC}}$| = 0.7875 FASTREC=HIGH	-81• Id	-64 • Id	-45 • Id	µA
Sample data AGC peak charge current DR/RR	0 < AGC < 3 34 <DR <127 AGC = SLC bits 1,0	-20%	$-3.2 \cdot 10^{-6}$ • AGC • DR/RR	+20%	A/V
Sample data AGC peak discharge current	DR = Data rate register	-20%	$+3.2 \cdot 10^{-6}$ • AGC • DR/RR	+20%	A/V
BYP/BYPS Pin leakage current	$\overline{\text{HOLD}}$ = low at gain = 3 and gain = 64	-70		+50	nA
VRC Reference voltage	Ioad = -50 µA /+500 µA	VPA - 2.87		VPA - 1.7	V

PULSE QUALIFIER CHARACTERISTICS

DUAL LEVEL QUALIFIER

Unless otherwise specified, a 100 m Vp-p @ 15 MHz sine wave input is AC coupled into VIA/$\overline{\text{VIA}}$. Fc set to 127, boost at Fc = 0 dB. * implied not directly testable.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Data level threshold, Lth	ALE = 0 Before SFC, Lth = 11.1 • LD - 4.2 *After SFC Lth = 7.636 • LD + 3.4368 ALE = 1 Lth = 10.7996 • LD + 4.8604 for 16 ≤ LD ≤ 48 No ATE Test	Lth - 11%	Lth	Lth + 11%	%
Servo level threshold	Prior to SFC LSth = 11.1 • LDS - 4.2 16 ≤ LS ≤ 48	LSth - 11%	LSth	LSth + 11%	V
$\overline{\text{RDS}}$ Pulse width low voltage	PWCTR = 0	7.7	15	20	ns
	PWCTR = 1	16.8	27	35	ns
PPOL to $\overline{\text{RDS}}$ delay time (window mode)	PPOL rise/fall to $\overline{\text{RDS}}$ fall, measured at 1.5V crossing	2.5		10	ns
PPOL/RDS Rise time,	0.8 V to 2. V, CL ≤ 15 pF			8	ns
PPOL/RDS Rise time,	0.8 V to 2.4 V, $_{CL}$ ≤ 40 pF, ATE			10	ns
PPOL/RDS Fall time	2.4 V to 0.8 V, CL ≤ 15 pF			6	ns
PPOL/RDS Fall time	2.4 V to 0.8 V, CL ≤ 40 pF,ATE			8	ns

DIBIT PULSE QUALIFIER CHARACTERISTICS

Unless otherwise specified, a 100 m Vp-p @ 15 MHz sine wave input is AC coupled into VIA/$\overline{\text{VIA}}$. Fc set to 127, boost at Fc = 0 dB. DIBITEN = 1.

Dibit discrimination Time interval Tr	DBT [2:0] Register bits (Bits 6 - 4 of NGM Reg)				
	000	-80%	40	+80%	ns
Note: Tr increment progression subject to change.	001	-80%	65	+80%	ns
	010	-80%	90	+80%	ns
	011	-80%	115	+80%	ns
	100	-80%	140	+80%	ns
	101	-80%	165	+80%	ns
	110	-80%	190	+80%	ns
	111	-80%	215	+80%	ns

ELECTRICAL SPECIFICATIONS (continued)

BASELINE OFFSET

See General for input conditions unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
BASELINE SHIFT TOLERANCE	SG = Low/High Blos = 2.3687 mV • BLOSS + 8.4642 0 ≤ YIN ≤ 127	-15%		+15%	

THERMAL ASPERITY

See General for input conditions unless otherwise specified.

Thermal asperity threshold, TAth	TAth [mV] = 51.59 • TATH + 697, 0 ≤ TATH ≤ 15	-13%	TAth	+13%	mV
Dynamic Hi-Y admittance yin at VIN/VINB	Yin [Siemens] = 1/720 + YIN/2538 0 ≤ YIN ≤ 7	-13%	Yin	+13%	Siemens
Hi-Y Period T_{Hi-Y}	T_{Hi-Y} = 0.94319 • HYTMR + 1.0757, 0 ≤ HYTMR ≤ 3	-13%	T_{Hi-Y}	+13%	µs
PLL/AGC Hold period TA_{hold}	TA_{hold} = 0.12 • TATMR + 0.273, 0 ≤ HYTMR ≤ 3	-13%	TA_{hold}	+13%	µs

QASYM FACTOR

Unless otherwise specified, measured at AO pin, each loaded with 5 pF. VIA-$\overline{VIA}$ = Lorentzian pulses with 10% asymmetry. Asymmetry (%) = $((V_{+1}-V_{-1})/(V_{+1}+V_{-1}))$ • 100, where V_{+1} = positive “1” sample value, V_{-1} = negative “1” sample value.

Reference voltage	ASEL[1:0] = [0 0],	Typ.-0.13	MAXREF/2	Typ.+0.13	V
Qasym at ATO	No ATE, reference only		700		mV

INTERNAL AC COUPLER CHARACTERISTICS

Unless otherwise specified, measured at TPC/$\overline{TPC}$ or TP/$\overline{TPD}$ pins, each loaded with 5 pF.

Offset voltage	ACD = 0, AGC gain from 3 V/V to 64V/V, FCDAC = 44 to 127	-35	5	+35	mV
	Open input AGC (no signal) FCDAC = 50	-50		+50	mV
Low_Z time constant	LOWZ = 1; LZCTR = X, No ATE		0.3		µs
Non Low_Z time constant	LOWZ = 0: LZCTR = 0 LZCTR = 1, No ATE		5.0 1.5		µs

PROGRAMMABLE FILTER CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply. The input signals are AC coupled to VIA and $\overline{VIA}$. RX = 10.2 kΩ from VRX pin to GND. All specifications identical for identical data and servo register settings. Output signals are measured at TPC/$\overline{TPC}$ for ON, TPD/$\overline{TPD}$ for OD. VRDT = high, $\overline{HOLD}$ = low.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Filter cutoff range, Fcr	Fc (MHz) = 0.49586 • FC + F_0, F_0 = 1.00219 18 ≤ FC ≤ 127 0 dB Boost		10 MHz to 64 MHz		MHz
Filter Fc accuracy, Fca	44 ≤ FC ≤127 18 ≤ FC ≤ 43	-15 -20		+15 +20	%
OD gain to ON gain mismatch	Fin = 0.67 • Fc 0 dB Boost	-30		+30	%
Boost @ Fc	Boost = 20Log[-0.0000337 • FB • FC + 0.043448 • FB +1] 0 ≤ FB ≤ 127		0 to 15		dB
Boost accuracy	Set for Boost = 15 dB	-2		+2	dB
	Set for Boost = 9 dB	-1.7		+1.7	dB
Servo boost accuracy	@5 and 14 MHz		FBS • 3		
TGD Variation (No boost) measured at ON/$\overline{ON}$ outputs	Fc = 54 Mhz F = 0.3 Fc to Fc, 0 dB Boost	-700		+700	ps
	Fc = 19 MHz to 64 MHz F = 0.3 Fc to Fc, 0 dB Boost	-5		+5	%
	Fc = 19 MHz to 64 Mhz F = Fc to 1.75 Fc, 0 dB Boost Not tested on ATE	-6		+6	%
TGD Variation (Maximum boost) Measured at ON/$\overline{ON}$ outputs	Fc = 54 Mhz F = 0.3 Fc to Fc; FB=127	-700		+700	ps
	Fc = 19 MHz to 64 Mhz F = 0.3 Fc to Fc; FB = 127	-5		+5	%
	Fc = 19 MHz to 64 Mhz F = Fc to 1.75 Fc, FB = 127	-6		+6	%

PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Group delay equalization accuracy (asymmetrical)	Fc = 19-64 MHz Boost = 0 dBD Δ% = 0.9783 • FGD - 0.665 No ATE		± 5		%
ON - $\overline{ON}$ Filter output dynamic range	THD = 2.5% max Fin = 0.67 Fc	1.4			Vp-p
Dp/Dn Output noise voltage, no boost. no ATE test	BW = 100 MHz, Rs = 50 Ω mode Fc = 127; FB = 0,FBS = 0, Gain = 24 dB Ω/fixed gain mode, no ATE	0.9	3	5.1	mVrms
Dp/Dn Output noise voltage, max. boost.	BW = 100 MHz, Rs = 50 Ω Fc = 127; FB = 127,FBS = 0, Gain = 24 dB Ω/fixed gain mode, no ATE	8.3	17.0	26.7	mVrms

TRANSVERSAL FILTER CHARACTERISTICS (Note: Unless otherwise specified, not tested on ATE.)

Km1 Range *	No ATE; Reference only	±0.15	±0.26		V/V
Km1 Gain drift	EQHOLD = 1Hold time ≤ 1ms		0.015	0.05	V/V/µs
Km2 Accuracy: Range and resolution	4 bit resolution, 2's compliment Range = -0.15 to + 0.13125 Resolution = 0.01875 Tested at both extremes of 7h and 8h	±20% -0.01		± 20% + 0.01	%
Km1 A/D Accuracy	Preset to N ≤ 16 & A/D to M	M = N-1	M = N	M = N+1	
*Km1 and VC - $\overline{VC}$ are approximately related by: Km1 = 0.018 • DR • (VC - $\overline{VC}$), where DR = DR register setting however Km1 can not be directly tested.					

TIME BASE GENERATOR CHARACTERISTICS

RR = 10.0 kΩ 1% tolerance, from RR pin to GND for 240 Mbit/s operation respectively.

FREF Input range	CM1:BT = 0	6		50	MHz
	CM1:BT = 1, CT:EFR = 1			130	MHz
FREF Input range	CM1:BT = 0, TM2:DIFFBF = 1			225	MHz
FREF Input pulse width	CM1:BT = 0	10			ns
F_{TBG} Output frequency range		85		255	MHz
F_{TBG} Jitter	> 10K Samples; not ATE tested, guranteed by design		30	200	ps_{RMS}
M Counter range	ATE Functional test only	2		255	
N Counter range	ATE Functional test only	2		127	

TIME BASE GENERATOR CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
VCO Center frequency, F_{TBG}	V(FLTR1 - $\overline{FLTR}$) = 0 V Fo = (2.2947 • DR + 8.5849) MHz	0.80 F_O		1.20 F_O	MHz
VCO Dynamic range	-2.0V ≤ V(FLTR1 - $\overline{FLTR}$) ≤ 2.0 V, F_{TBG} = 80 MHz	+25			%
VCO Control gain, K_{VCO}	$\omega\iota = 2\pi \bullet F_{TBG}$ -1.0 V ≤ V(FLTR1 - $\overline{FLTR}$) ≤ 1.0 V	0.12 • ωι	0.18• ωι	0.24 • ωι	rad/(V-s)
Phase detector gain, KD	KDO = 3.9205 • DR + 3.3779 for RR = 10 kΩ	0.72KDO		1.22KDO	µA/rad
K_{VCO} • KD product accuracy		-28		+28	%

DATA SEPARATOR CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

READ MODE

Read clock rise time, TRRC	0.8 V to 2.4 V, C_L ≤ 15 pF			10	ns
Read clock fall time, TFRC	2.4 V to 0.8 V, C_L ≤ 15 pF			10	ns
RCLK Pulse width, TRP	Except during re-sync	4/9 TORC -5		4/9 TORC +5	ns
NRZx Out set-up and hold time, TNS, TNH		16			ns
$\overline{SBD}$ Set-up and hold time TSBS		14			ns

WRITE DATA OUTPUT

Write data output rise time, TRWD	20% to 80% points 2 kΩ to GND, CL ≤ 15 pF			3	ns
Write data output fall time, TFWD	80% to 20% points 2 kΩ to GND, CL ≤ 15 pF			3	ns
WD Jitter	Preamble pattern, guaranteed by design and characterization		90	200	ps_{RMS}

DATA SEPARATOR CHARACTERISTICS (continued)

WRITE MODE

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Write clock rise time, TRWC	0.8 to 2.0 V input conditions			10	ns
Write clock fall time, TFWC	2.0 to 0.8 V input conditions			8	ns
NRZx Set-up time, TSNRZ	Functional test only	10			ns
NRZx Hold time, THNRZ	Functional test only	3			ns
PERR Propagation delay from rising edge of WCLK, Tperr	1.5 V to 1.5 V,CL ≤ 15 pF			41	ns

WRITE PRECOMPENSATION

Write precomp time shift, TPC as a % of T_{TBG}, or (%)wpc=TPC/ T_{TBG},	Relative to WPC1 = 0, repeating 03_h in direct write mode $1 \le WPC \le 13$ WPC1 = 15, ATE test only on functionality at WPC1 = 15	1.8 • WPC1-2 23	2.01 • WPC1 30	2.21 • WPC1+2 37	%
	Level 2 Precomp ATE functional test only WPC1 = 0	0.97 • WPC2-2 13.7	1.08 • WPC2 16.6	1.19 • WPC2+2 20.2	%
	Level 3 Precomp $1 \le WPC2 \le 15$ ATE test only functionality at WPC = 15	0.84 • WPC3-4	1.05 • WPC3	1.26 • WPC3+6	%

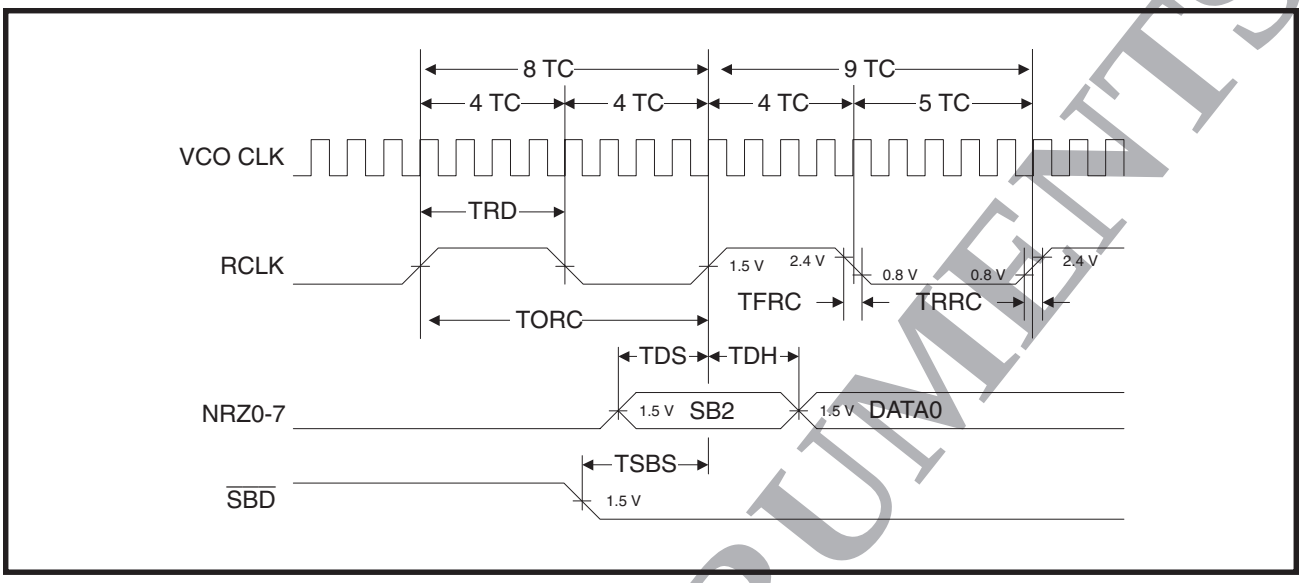


FIGURE 31: Read mode NRZ interface timing

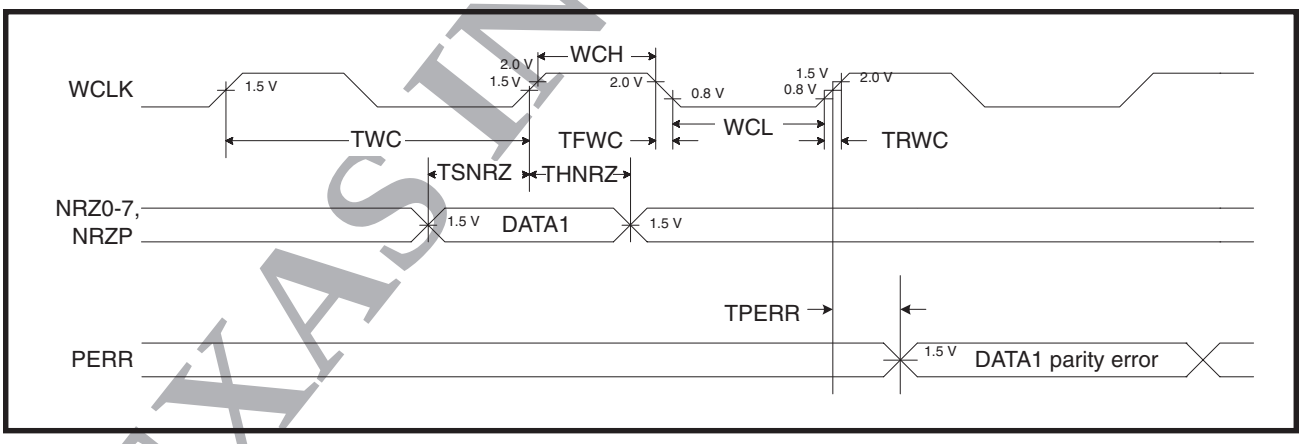


FIGURE 32: Write mode NRZ interface timing

ELECTRICAL SPECIFIICATIONS (continued)

DATA SYNCHRONIZER PLL

RR = 10.0kΩ 1% tolerance, from RR pin to GND for 240 Mbps operation.

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
VCO Center frequency, F_{VCO}	V(FLTR1 - $\overline{FLTR1}$) = 0 V FO = (2.2947 • DR + 8.5849) MHz	0.80 • FO		1.20 • FO	ns
VCO Dynamic range in each direction	-7.0 V ≤ V(FLTR2 - $\overline{FLTR2}$) ≤ 0.7 V for DR = 127 -2.1 V ≤ V(FLTR2 - $\overline{FLTR2}$) ≤ 2.1 V for DR = 42	+25			%
VCO Control gain & M M • K_{VCO}	ωi = 2π F_{VCO} M=3.89 • (DR/127) -0.25 V ≤ V(FLTR2 - FLTR2) ≤ +0.25 V	0.11ωi M		0.26 ωi M	rad/(V-s)
Charge pump transconductance	Gm = 499 µA/V during synchronization gear shift factor, for reference only, not ATE tested:when 610	0.5 Gm		1.4 Gm	A/V
Damping amplifier gain, A • Kvco product accuracy	A = 0.7 • (DRC/127) DRC = Damping Ratio Control register setting	-30		+30	%
Idle mode phase detector gain, KDI	KDI = 0.15 Gm • M		KDI		µA/rad
Gm • M • K_{VCO} product accuracy		-28		+28	%

SERVO CHARACTERISTICS

Unless otherwise specified: A 15 MHz sine wave is input into the DP/DN inputs (PD:TPC/D/E = '01';CM2: SERI = 0). STROBE and $\overline{RESET}$ durations are 1.0 µs CM:SBCC = "10".

MAXREF Output voltage	Isource = 0 µA	2.8	3.00	3.2	V
MAXREF Load regulation	Isource = 0 to 0.15 µA			40	mV
A, B, C, D Output low voltage,Vol	Isink = 0.2 µA, $\overline{RESET}$ = low	170	270	370	mV
A, B, C, D & SQOUT calibration reference output = Maxref/2	Isink = 0.2 mA, FCS(bit7) = 1		1.50		V
A, B, C, D Output resistance	Isource/Isink = 0.2 µA			50	Ω

SERVO CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Servo Gain (A, B, C, D)	10 periods of a 10 MHz 0.3 V ≤ VIA - $\overline{VIA}$ ≤ 1.1 V SGAIN = 1.6 + 0.1 • IGAIN 0 ≤ IGAIN ≤ 15	SGAIN-20%	SGAIN	SGAIN+20%	V/V
Servo Gain, low input (A, B, C, D)	10 periods of a 10 MHz 0.1 V ≤ VIA - $\overline{VIA}$ ≤ 0.3 V SGAIN = 1.6 + 0.1 • IGAIN 0 ≤ IGAIN ≤ 15	SGAIN-35%	SGAIN	SGAIN+35%	V/V
Hold droop	INTEG = low $\overline{RESET}$ = high			0.5	mV/µs
Channel to channel swing mismatch	DP-DN = 0.75 Vp-p In either normal or self calibration mode			80	mV
Burst Capture time	Output ≥ 95% of final value			0.5	µs
Burst reset time	DP-DN = 1.4 Vp-p Output ≤ 5% of final value from $\overline{RESET}$ fall			0.5	µs
INTEG to INTEG width		150			ns
$\overline{RESET}$ to INTEG delay	from rising $\overline{RESET}$ to rising INTEG	20			ns

TABLE 11: Mode Control

WG	RG	SG	MODE	DESCRIPTION
0	0	0	Idle mode	DS VCO Locked to FTBG. NRZ1-0 tri-stated.
0	1	0	Data read mode	DS PLL Acquisition, adaptive equalizer training, code word boundary search and detect, decode, sync byte detect, and NRZ data output. DS VCO switched from FTBG to RD after preamble detect. RCLK gen. input switched from FTBG to DS VCO. RCLK re-synchronized to RD at code word boundary detect. NRZ1-0 active.
1	0	0	Data write mode	Write mode preamble insertion and data write. DS VCO locked to FTBG. RCLK synchronized to FTBG. WD and $\overline{WD}$ active. NRZ1-0 tri-stated.
1	1	0	Read override	RG Overrides WG which causes any write in progress to cease and data read mode to be entered.

ELECTRICAL SPECIFIICATIONS (continued)

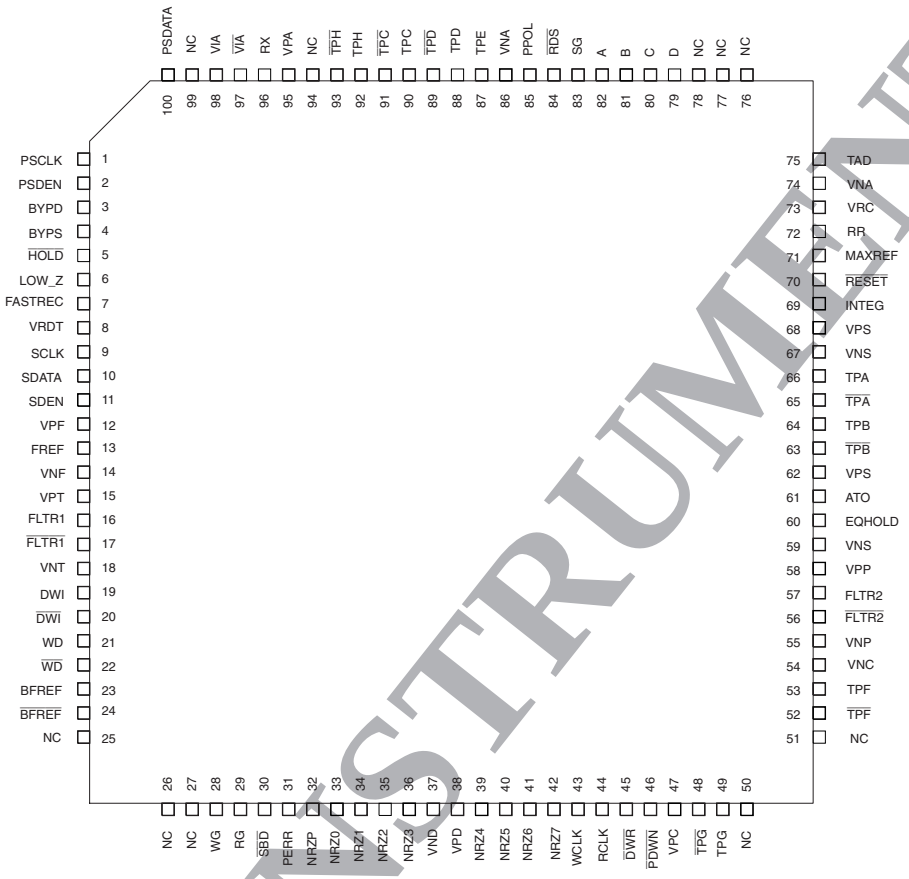
DIAGNOSTIC/OPTMIZATION TEST MODES

Some disk drive diagnostic test and operating optimization may be performed by observing the Equalizer and AGC Control voltages and measuring their change with different conditions. For example, the Equalizer Control Voltage ("0" sample values) is affected by the Continuous Time Filter/Equalizer setting, the head flying height, and the head gap length. The KM1 A/D function may be used to monitor flying height changes. The AGC Control Voltage ("1" sample values) are also affected by the previously mentioned factors and by magnetic nonlinearities. The effectiveness of Write Precomp compensating the nonlinearities could be evaluated by observing the AGC Control Voltage difference of a maximum transition dibit pattern with a pattern with minimum transitions.

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead TQFP
Deep downset

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32P4103B 100-Lead TQFP Deep downset	32P4103B-CGE	32P4103B-CGE

Preproduction: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

Abridged Version

SSI 32P4104A

EPRML Read Channel w/16/17's ENDEC, 4-Burst Servo (A, B, C, D)

Prototype

February 1998

DESCRIPTION

The SSI 32P4104A is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Extended Partial Response Class 4(EPR4) 16/17's code read channel for zoned recording hard disk drive systems with data rates from 85 to 260 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 16/17's GCR ENDEC, data synchronizer, time base generator, servo data detector, and 4-burst servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc., are controlled by writing to the serial port registers so no external component changes are required to change zones.

The SSI 32P4104A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

- **Register programmable data rates from 85 to 260 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **Five tap transversal filter with adaptive PR4 equalization**
- **16/17's [0,6,8] GCR ENDEC**
- **Data scrambler/descrambler**
- **Presettable precoder state**
- **Low operating power (TBDmW typical at 5 V)**
- **Register programmable power management (<5 mW power down mode)**
- **8 bit NRZ data interface**
- **8-bit direct write and read modes automatically configured for RCLK = VCO/8**
- **Serial interface port for access to internal program storage registers**
- **Single power supply (5 V ± 10%)**
- **Small footprint 100-Lead TQFP package**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents for data reads**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Automatic AGC fast recovery and input low-z modes with programmable time durations**
- **Wide bandwidth, precision full-wave rectifier**
- **Optional internal timing disable and AGC direct control pins: LOW-Z, FASTREC, $\overline{\text{HOLD}}$**
- **2-bit DAC to control AGC voltage in servo mode between 1.1 and 1.4 V**

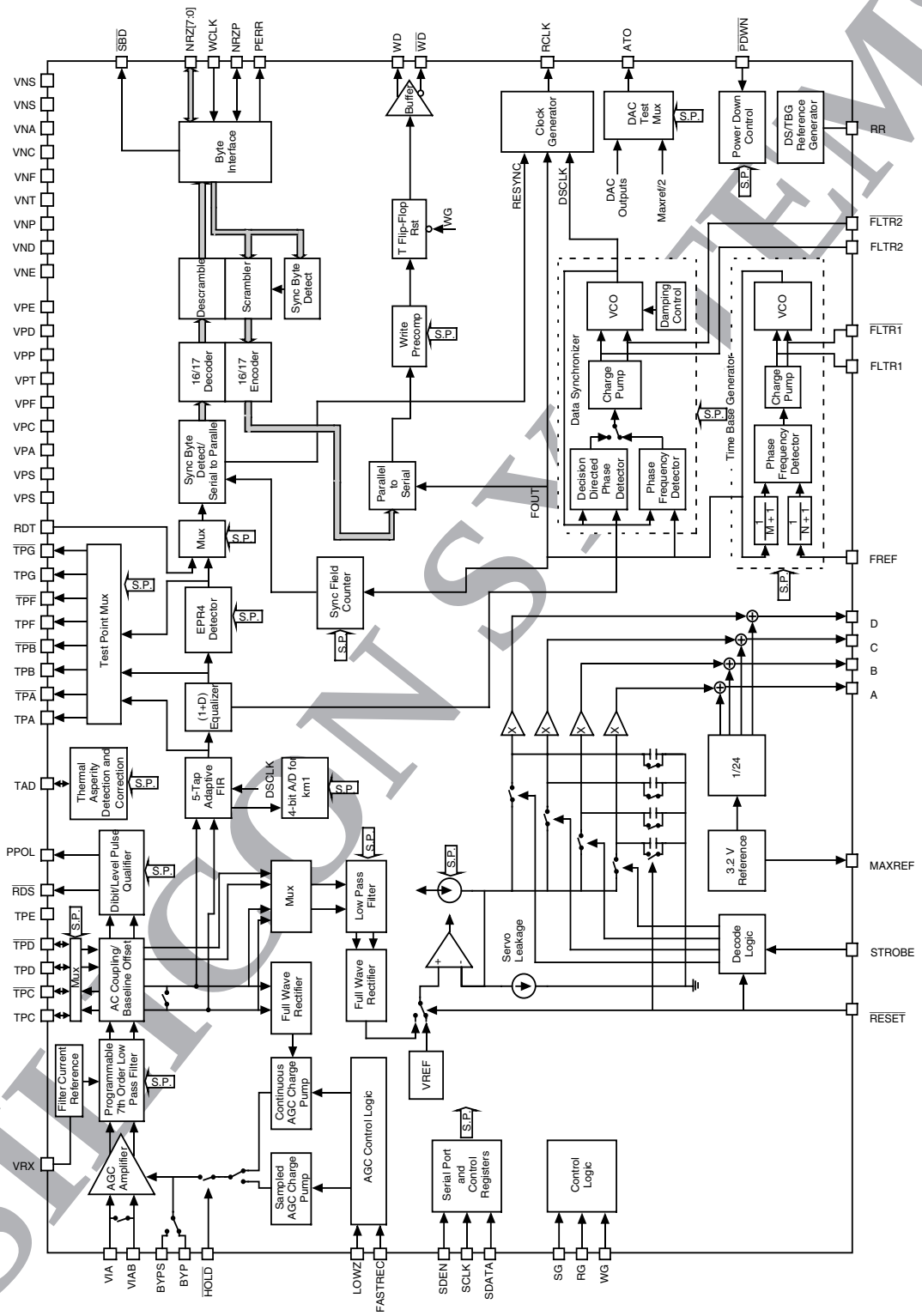
FILTER/EQUALIZER

- **Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:**
  - **Channel filter and pulse slimming equalization for equalization to PR4**
  - **Programmable cutoff frequency from 7 to 71 MHz**
  - **Programmable boost/equalization of 0 to 15 dB**
  - **Programmable asymmetrical zeros equalization to correct pulse shape asymmetry**
- **Five tap transversal filter provides:**
  - **Fine equalization to PR4**
  - **Self adapting symmetric tap coefficients**
  - **Presettable symmetric tap coefficients**
- **Additional (1+D) equalization to meet EPR4 target**
- **Low Z switch for fast offset recovery at the filter output**

(continued)

SSI 32P4104A
EPRML Read Channel w/16/17's
ENDEC, 4-Burst Servo (A, B, C, D)

BLOCK DIAGRAM



FILTER/EQUALIZER (continued)

- Equalizer hold input
- Amplitude asymmetry factor output
- Internal AC-coupling

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to EPR4
- Register programmable qualification thresholds for servo reads
- Selectable hysteresis or window qualification modes for servo reads
- Selectable dibit or pulse detect qualification modes for servo reads
- Programmable baseline offset for amplitude assymetry compensation

ERROR MEASUREMENT

- Digital channel quality monitor

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 276.25 MHz frequency output
- Independent M and N divide-by registers

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 16/17's GCR ENDEC
- Register programmable to 260 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from sampled PR4 target
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 8-bit NRZ data interface
- Data rate tracking, programmable write precompensation for non-linear transition shift
- Differential PECL write data output with power reduction
- Integrated sync byte detection, single byte or dual ("or" type)
- Programmable offset to compensate for MR head asymmetry
- Surface defect scan mode

SERVO

- 4-burst soft landing servo with A, B, C, D outputs
- Internal hold capacitors
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Wide bandwidth, precision full-wave rectifier with programmable offset to compensate for MR head asymmetry
- Servo calibration outputs
- Programmable baseline offset
- RDS and PPOL outputs for servo data recovery

THERMAL ASPERITY DETECTION/CORRECTION

- Analog front end thermal asperity detection and correction circuits
- Digital outputs for thermal asperity detection and error flag
- AGC and PLL hold over thermal asperity
- Programmable high admittance over thermal asperity

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

2000

PROGRAMMABLE ELECTRONIC FILTERS

Return to the Table of Contents

Texas Instruments

SSI 32F8101
Low-Power Programmable Filter

January 1996

DESCRIPTION

The SSI 32F8101 is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the f_c and Boost DACs.

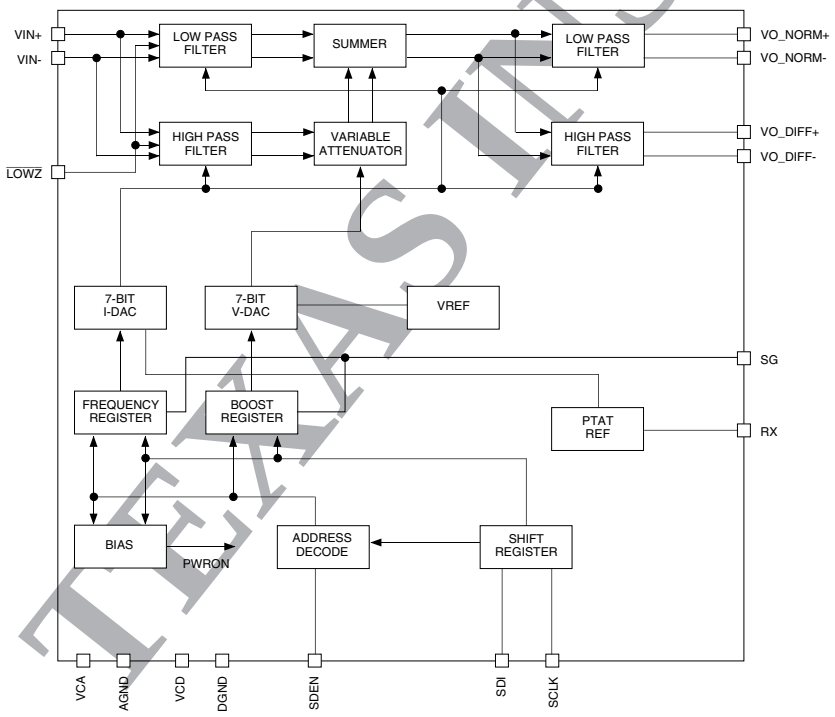
Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 14.6 dB nominally at maximum f_c, and is implemented using two symmetrical, real-axis zeroes. Both boost and f_c control do not affect the flat group delay response.

The SSI 32F8101 device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an idle mode for minimal power dissipation. The SSI 32F8101 is available in a 16-lead SON package.

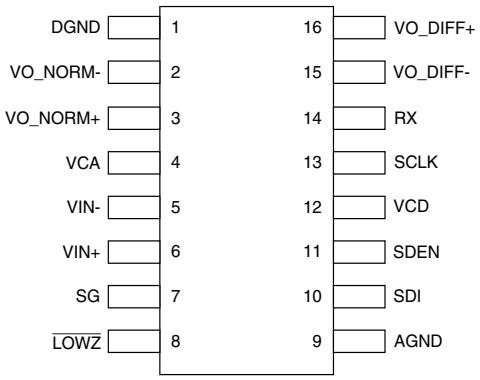
FEATURES

- **Programmable cutoff frequency 8.4 to 30 MHz**
- **Programmable boost/equalization of 0 to 14.6 dB**
- **Matched normal and differentiated outputs**
- **±15% f_c accuracy**
- **±2% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**
- **95 mW nominal power, <5 mW idle**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8101
Low-Power Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8101 programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $\omega c = 2\pi\, fc = 1$) are:

$Vnorm/Vi = 13.65983 \bullet [(-Ks^2 + 1.31703)/D(s)] \bullet AN$

and

$Vdiff/Vi = (Vnorm/Vi) \bullet (s/0.86133) \bullet AD$

Where D (s)=

$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)$

$(S^2 + 1.4558s + 5.37034)(s + 0.86133)$,

AN and AD are adjusted for a gain of 1 at $fs = (2/3)\, fc$.

FILTER OPERATION

Normally AC coupled differential signals are applied to the VIN± inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the VIN± inputs are placed into a Low-Z state when the $\overline{LOWZ}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 13.3 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$fc = 0.253 \bullet DACF - 2.218$ (MHz)

where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3 dB frequency.

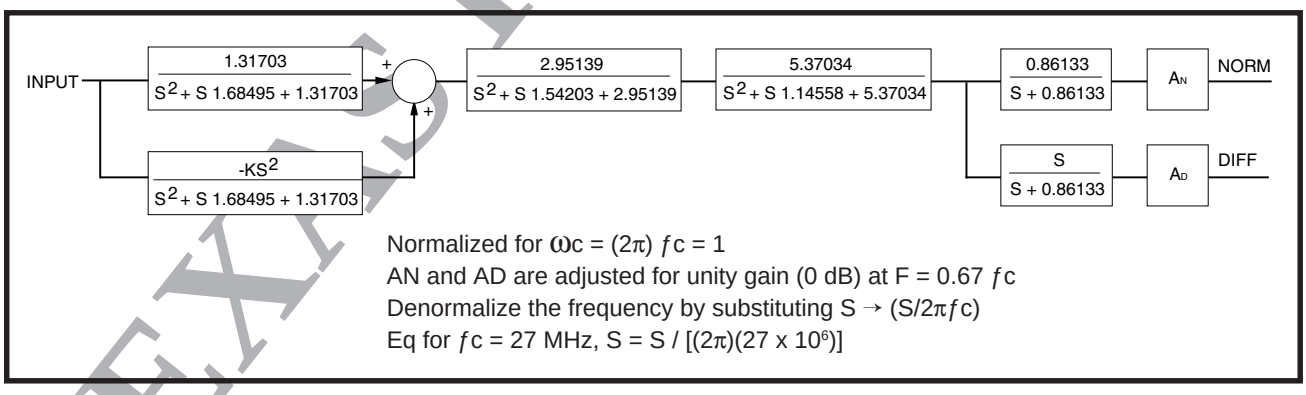


FIGURE 1: SSI 32F8101 Normalized Block Diagram

TABLE 1: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3 dB/fc	K
0	-3	no peak	no peak	1.00	0
1	-2	no peak	no peak	1.21	0.16
2	-1	no peak	no peak	1.50	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85
11	8	9.59	1.51	2.73	3.36
12	9	10.77	1.51	2.80	3.93
13	10	11.92	1.53	2.87	4.57
14	11	13.06	1.53	2.93	5.28
15	12	14.18	1.56	3.0	6.09

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f - 3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

   i.e., fc = 9 MHz when boost = 0 dB

   if boost is programmed to 5 dB then f - 3 dB = 19.8 MHz

   $f$peak = 11.07 MHz

4. $K = 1.31703 (10^{\frac{\text{BOOST (dB)}}{20}} - 1)$

FUNCTIONAL DESCRIPTION (continued)

BOOST / EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost =

$20 \log [(0.0239 \bullet DACB) + 7.6 \bullet 10^{-5} \bullet DACB \bullet DACF) + 1.132]$

where DACB = value in FBCR register.

For example, with the DAC set for maximum output (FBCR = 7F hex or 127) at the maximum cutoff frequency (DACF = 7F hex or 127) there will be 14.6 dB of boost added at the 3 dB frequency. This will result in +11 dB of signal boost above the 0 dB baseline.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 32F8101. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

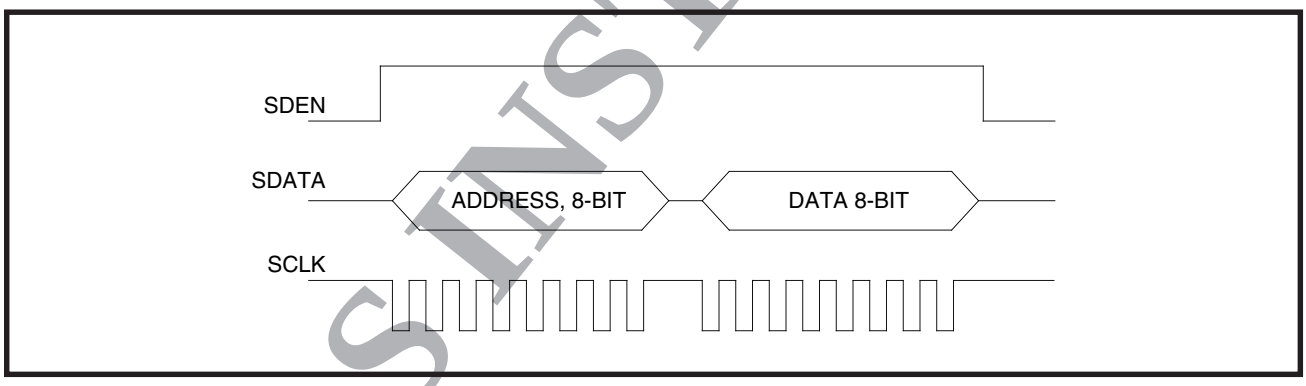


FIGURE 2: Serial Port Data Transfer Format

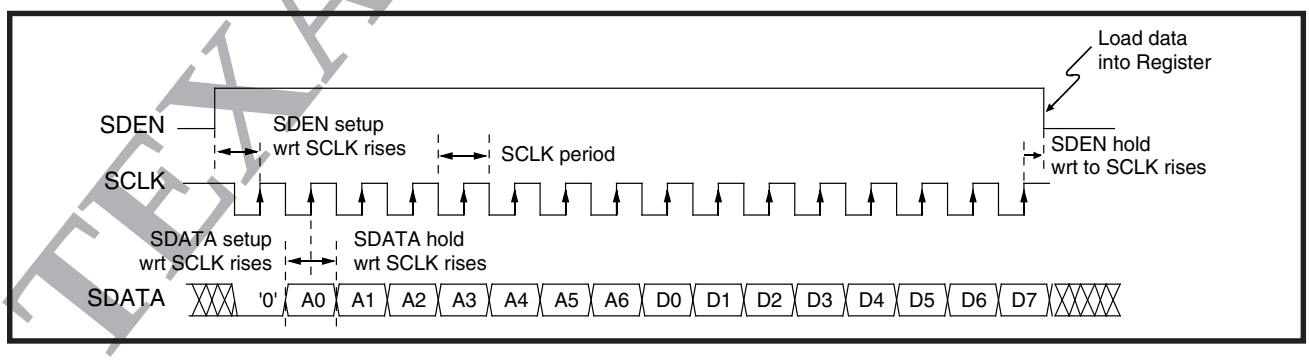


FIGURE 3: Serial Interface Timing Diagram - Writing Control Register

TABLE 2: Serial Port Register Mapping

REGISTER NAME	ADDRESS							R/W	D7	DATA BIT MAP						D0
	A6					A0										
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	--	--	FILTER 1=DISABLE 0=ENABLE	--	
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, DATA	0	0	0	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, SERVO	0	0	1	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0

* These bits are used only for testing. They should be programmed to 0 in actual operation.

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VCA	-	Filter analog power supply pin
VCD	-	Serial port power supply pin
AGND	-	Filter analog ground pin
DGND	-	Serial port digital ground pin

INPUT PINS

VIN+, VIN-	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
SG	I	SERVO GATE: TTL input when high enables servo frequency and boost registers to the control DACs. When low the data frequency and boost registers are enabled.
$\overline{\text{LOWZ}}$	I	LOW_Z CONTROL: TTL input when low reduces the filter input resistance. When high, the input is at high impedance state.

OUTPUT PINS

VO_DIFF+,	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated VO_DIFF- outputs. These outputs are normally AC coupled.
VO_NORM+,	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. VO_NORM- These outputs are normally AC coupled.
RX	-	REFERENCE RESISTOR INPUT: An external 13.3 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	I/O	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDI	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I/O	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.
Rx = 13.3 kΩ, Cx = 1000 pF from Rx pin to VCA. Input signals are AC-coupled into VIN±.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+135°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
ICC (VCA,D)	Output pins open DACF = 127 Boost = 0 dB		19	30	mA
PWR Power Dissipation	Output pins open DACF = 127 Boost = 0 dB		95	165	mW
Sleep Mode Power	PWRON = 1			5	mW

TTL COMPATIBLE INPUTS

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD	V
					+0.3	
Input low current	IIL	VIL = 0.4V	-0.4			mA
Input high current	IIH	VIH = 2.4V			100	µA

CMOS COMPATIBLE INPUTS

Input low voltage	Vp = 5V	-0.3		1.5	V
Input high voltage	Vp = 5V	3.5		VCD +0.3	V

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
SCLK period		Read from serial port	140			ns
		Write to serial port	100			ns
SCLK low time	TCKL	Read from serial port	60			ns
		Write to serial port	40			ns
SCLK high time	TCKH	Read from serial port	60			ns
		Write to serial port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SDEN low time	TSL		200			ns

PROGRAMMABLE FILTER CHARACTERISTICS

Filter cutoff range	fc @ -3 dB point fc (MHz) = 0.253 • DACF - 2.218, Boost = 0 dB 42 ≤ DACF ≤ 127		8.4 - 30		MHz
Filter cutoff accuracy	DACF = 42 and 127	-15		15	%
FNP, FNN differential gain AN	f = 0.67xfc, boost = 0 dB	0.7	1.0	1.25	V/V
FDP, FDN differential gain AD	f = 0.67xfc, boost = 0 dB	0.8 AN	1.0 AN	1.2 AN	V/V
Boost accuracy Boost = 20 log [(0.0239 • DACB) + (7.6 • 10^{-5} • DACB • DACF) + 1.132]	6.6 dB, DACF = 42, DACS = 37	-1.0		+1.0	dB
	7.5 dB, DACF = 127, DACS = 37	-1.0		+1.0	dB
	9.4 dB, DACF = 42, DACS = 67	-1.25		+1.25	dB
	10.6 dB, DACF = 127, DACS = 67	-1.25		+1.25	dB
	13.2 dB, DACF = 42, DACS = 127	1.5		+1.5	dB
	14.6 dB, DACF = 127, DACS = 127	-1.5		+1.5	dB
Data mode group delay variation, DACF = 0 to 127	f = 0.2 fc to fc, 42 ≤ DACF ≤ 127	-2		+2	%
	f = fc to 1.75 fc, 42 ≤ DACF ≤ 84	-3		+3	%
	85 ≤ DACF ≤ 127	-6.5		+6.5	%

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Data mode group delay variation, DACS = 0 to 127	DACF = 127 f = 0.2 fc to fc	-0.5		+0.5	ns
	DACF = 42 f = 0.2 fc to fc	-1.25		+1.25	ns
	DACF = 127 f = fc to 1.75fc	-1.5		+1.5	ns
	DACF = 42 f = fc to 1.75fc	-1.9		+1.9	ns
Filter differential output dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs	1			Vp-p
Filter differential input resistance	Normal	4			kΩ
	Low-Z		200	400	Ω
Filter differential input capacitance				7	pF
Output Noise Voltage: BW = 100 MHz, Rs = 50Ω					
differentiated output	fc = 30 MHz, boost = 0 dB		4.4	6.6	mV Rms
differentiated output	fc = 30 MHz, DACS = 127		7.7	11.6	mV Rms
normal output	fc = 30 MHz, boost = 0 dB		2.5	3.8	mV Rms
normal output	fc = 30 MHz, DACS = 127		3.7	5.6	mV Rms
Filter output sink current		0.5			mA
Filter output offset voltage		-200		200	mV
Filter output source current		2.0			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Ta = 127°C		800		mV
Rx resistance	1% fixed value		13.3		kΩ

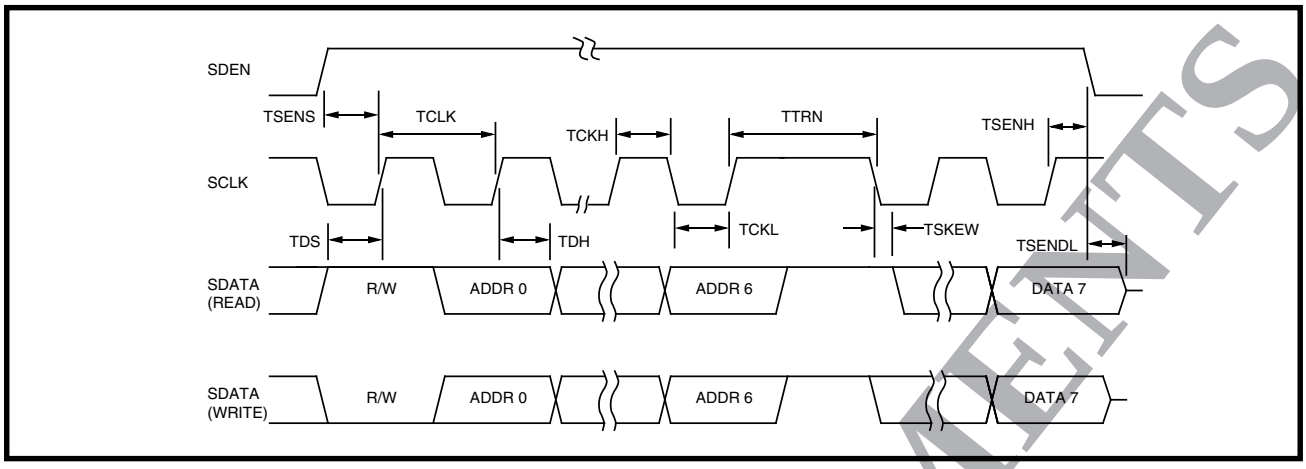
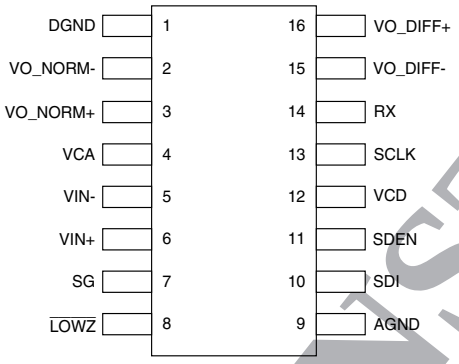


FIGURE 4: Serial Port Timing Information

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON

THERMAL CHARACTERISTICS: θja

16-lead SON	100° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32F8101 16-Lead SON	32F8101-CN	32F8101-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SSI 32F8102/8103/8104
Low-Power Programmable Filter

January 1998

DESCRIPTION

The 32F810X is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the fc and Boost DACs.

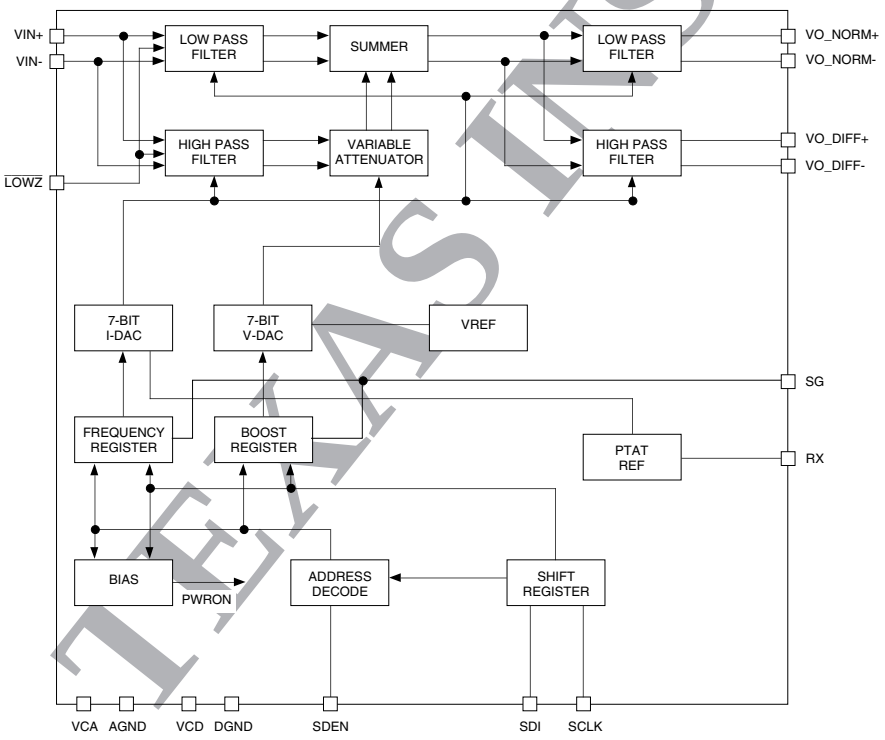
Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 14.3 dB nominally at maximum fc, and is implemented using two symmetrical, real-axis zeroes. Both boost and fc control do not affect the flat group delay response.

The 32F810X device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an idle mode for minimal power dissipation. The SSI 32F810X is available in a 16-lead SON package.

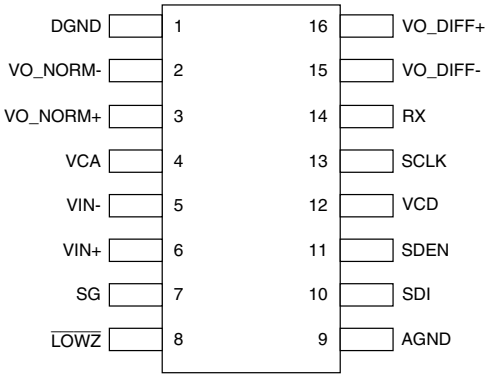
FEATURES

- **Programmable cutoff frequency:**
  - **32F8102 - 5.5 to 18 MHz**
  - **32F8103 - 3.7 to 12 MHz**
  - **32F8104 - 2.9 to 9 MHz**
- **Programmable boost/equalization of 0 to 14.3 dB**
- **Matched normal and differentiated outputs**
- **±15% fc accuracy**
- **±2% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**
- **95 mW nominal power, <5 mW idle**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F810X programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $\omega c = 2\pi f c = 1$) are:

$Vnorm/Vi = 13.65983 \bullet [(-Ks^2 + 1.31703)/D(s)] \bullet AN$

and

$Vdiff/Vi = (Vnorm/Vi) \bullet (s/0.86133) \bullet AD$

Where D (s)=

$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203\ s + 2.95139)$

$(S^2 + 1\ .4558s + 5.37034)(s + 0.86133),$

AN and AD are adjusted for a gain of 1 at $fs = (2/3)fc$.

FILTER OPERATION

Normally AC coupled differential signals are applied to the VIN± inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the VIN± inputs are placed into a Low-Z state when the $\overline{LOWZ}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 13.3 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$fc = 0.1474 \bullet DACF - 0.726$ (MHz) for the 32F8102
$fc = 0.09745 \bullet DACF - 0.376$ (MHz) for the 32F8103
$fc = 0.07198 \bullet DACF - 0.142$ (MHz) for the 32F8104
where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3 dB frequency.

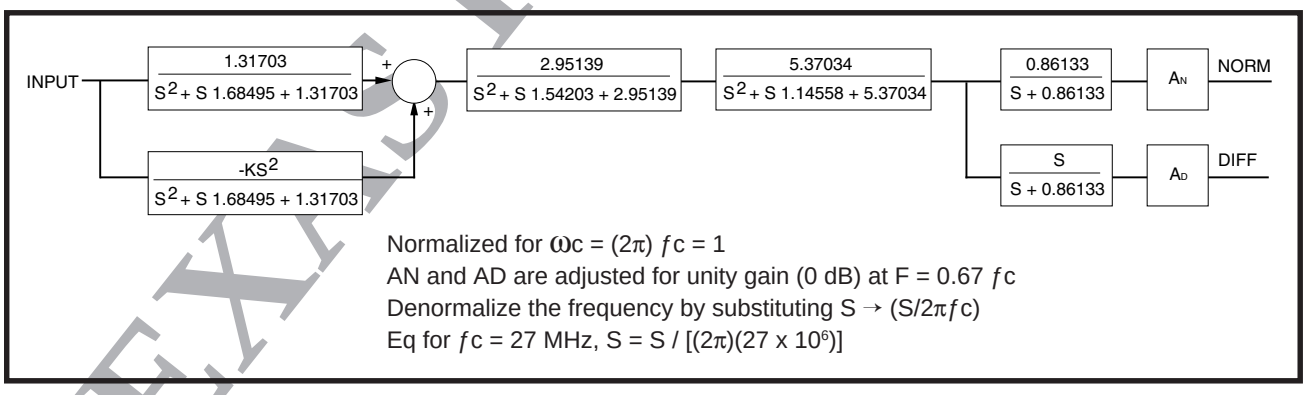


FIGURE 1: 32F8102/8103/8104 Normalized Block Diagram

TABLE 1: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	no peak	no peak	1.00	0
1	-2	no peak	no peak	1.21	0.16
2	-1	no peak	no peak	1.50	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85
11	8	9.59	1.51	2.73	3.36
12	9	10.77	1.51	2.80	3.93
13	10	11.92	1.53	2.87	4.57
14	11	13.06	1.53	2.93	5.28

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

4. $K = 1.31703 \left(10^{\frac{\text{BOOST (dB)}}{20}} - 1\right)$

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost (dB) = 20 • log [0.0239 • DACB + 7.6 • 10^{-5} • DACB • DACF + 1.132] for 32F8102

Boost (dB) = 20 • log [0.025 • DACB + 4.7 • 10^{-5} • DACB • DACF + 1.1] for 32F8103

Boost (dB) = 20 • log [0.0253 • DACB + 5.27 • 10^{-5} • DACB • DACF + 1.1] for 32F8104

where DACB = value in FBCR register.

For example, with the DAC set for maximum output (FBCR = 7F hex or 127) at the maximum cutoff frequency (DACF = 7F hex or 127) there will be 14 dB of boost added at the 3 dB frequency. This will result in +11 dB of signal boost above the 0 dB baseline.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the 32F810X. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

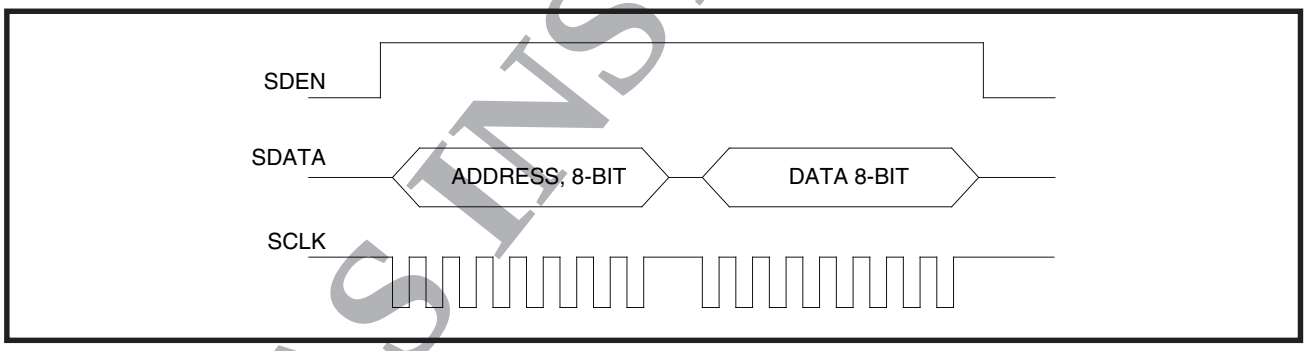


FIGURE 2: Serial Port Data Transfer Format

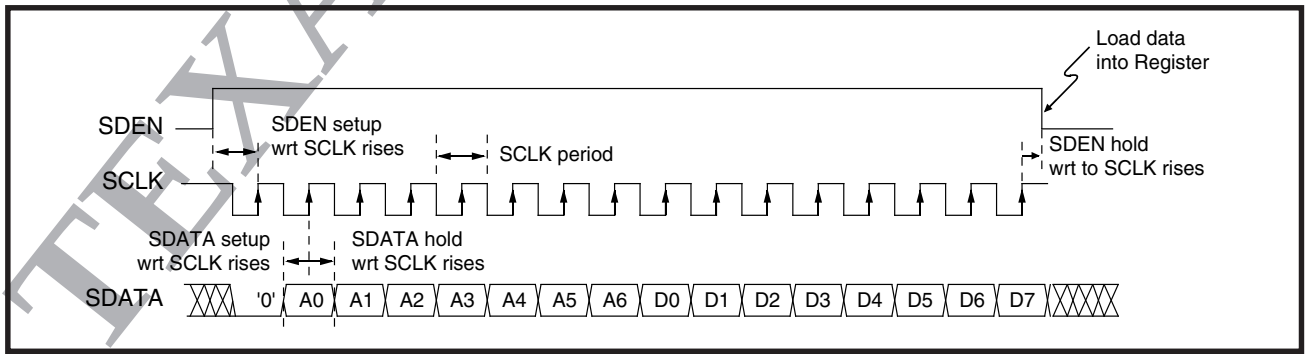


FIGURE 3: Serial Interface Timing Diagram - Writing Control Register

TABLE 2: Serial Port Register Mapping

REGISTER NAME	ADDRESS								DATA BIT MAP								
	A6						A0	R/W	D7								D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	--	--	--	FILTER 1=DISABLE 0=ENABLE	--	
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0	
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0	
FILTER BOOST, DATA	0	0	0	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0	
FILTER BOOST, SERVO	0	0	1	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0	

* These bits are used only for testing. They should be programmed to 0 in actual operation.

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VCA	-	Filter analog power supply pin
VCD	-	Serial port power supply pin
AGND	-	Filter analog ground pin
DGND	-	Serial port digital ground pin

INPUT PINS

VIN+, VIN-	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
SG	I	SERVO GATE: TTL input when high enables servo frequency and boost registers to the control DACs. When low the data frequency and boost registers are enabled.
$\overline{\text{LOWZ}}$	I	LOW_Z CONTROL: TTL input when low reduces the filter input resistance. When high, the input is at high impedance state.

OUTPUT PINS

VO_DIFF+, VO_DIFF-	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated outputs. These outputs are normally AC coupled.
VO_NORM+, VO_NORM-	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are normally AC coupled.
RX	-	REFERENCE RESISTOR INPUT: An external 13.3 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	I/O	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDI	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I/O	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 130°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.
Rx = 13.3 kΩ, Cx = 1000 pF from Rx pin to VCA. Input signals are AC-coupled into VIN±.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+130°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
ICC (VCA,D)	Output pins open DACF = 127 Boost = 0 dB		19	30	mA
PWR Power Dissipation	Output pins open DACF = 127 Boost = 0 dB		95	165	mW
Sleep Mode Power	PWRON = 1			5	mW

TTL COMPATIBLE INPUTS

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD +0.3	V
Input low current	IIL	VIL = 0.4V	-0.4			mA
Input high current	IIH	VIH = 2.4V			100	µA

CMOS COMPATIBLE INPUTS

Input low voltage	Vp = 5V	-0.3		1.5	V
Input high voltage	Vp = 5V	3.5		VCD +0.3	V

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
SCLK period		Read from serial port	140			ns
		Write to serial port	100			ns
SCLK low time	TCKL	Read from serial port	60			ns
		Write to serial port	40			ns
SCLK high time	TCKH	Read from serial port	60			ns
		Write to serial port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SDEN low time	TSL		200			ns

PROGRAMMABLE FILTER CHARACTERISTICS

Filter cutoff range (32F8102)	fc @ -3 dB point fc (MHz) = 0.1474 • DACF - 0.7258 42 ≤ DACF ≤ 127	5.5		18	MHz
Filter cutoff range (32F8103)	fc @ -3 dB point fc (MHz) = 0.09745 • DACF - 0.3756 42 ≤ DACF ≤ 127	3.7		12	MHz
Filter cutoff range (32F8104)	fc @ -3 dB point fc (MHz) = 0.07198 • DACF - 0.142 42 ≤ DACF ≤ 127	2.9		9	MHz
Filter cutoff accuracy	DACF = 42 and 127	-15		15	%
FNP, FNN differential gain AN	f = 0.67 • fc, boost = 0 dB	0.8	1.0	1.25	V/V
FDP, FDN differential gain AD	f = 0.67 • fc, boost = 0 dB	0.8 AN	1.0 AN	1.25 AN	V/V

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
Boost accuracy	DACF = 42, DACB = 37		-1.0		+1.0	dB
	DACF = 127, DACB = 37		-1.0		+1.0	dB
	DACF = 42, DACB = 67		-1.25		+1.25	dB
	DACF = 127, DACB = 67		-1.25		+1.25	dB
	DACF = 42, DACB = 127		1.5		+1.5	dB
	DACF = 127, DACB = 127		-1.5		+1.5	dB
Data mode group delay	f = 0.2 fc to fc		-2		+2	%
variation, DACF = 42 to 127, DACB = 0 to 127	f = fc to 1.75 fc		-4		+4	%
Data mode group delay	DACF = 127	32F8102	-0.75		+0.75	ns
variation, DACB = 0 to 127	f = 0.2 fc to fc	32F8103	-1.0		+1.0	ns
		32F8104	-1.25		+1.25	ns
	DACF = 42	32F8102	-2.5		+2.5	ns
	f = 0.2 fc to fc	32F8103	-3		+3	ns
		32F8104	-3.75		+3.75	ns
	DACF = 127	32F8102	-1.4		+1.4	ns
	f = fc to 1.75fc	32F8103	-1.5		+1.5	ns
		32F8104	-1.9		+1.9	ns
	DACF = 42	32F8102	-2.85		+2.85	ns
	f = fc to 1.75fc	32F8103	-3.75		+3.75	ns
		32F8104	-5.65		+5.65	ns
Filter differential output dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs		1			Vp-p
Filter differential input resistance	Normal		4			kΩ
	Low-Z			200	400	Ω
Filter differential input capacitance					7	pF

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Noise Voltage: BW = 100 MHz, Rs = 50Ω					
32F8102					
differentiated output	fc = 18 MHz, boost = 0 dB		4.1	6.2	mV Rms
differentiated output	fc = 18 MHz, DACS = 127		6.9	10.4	mV Rms
normal output	fc = 18 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	fc = 18 MHz, DACS = 127		3.2	4.8	mV Rms
32F8103					
differentiated output	fc = 12 MHz, boost = 0 dB		3.8	5.7	mV Rms
differentiated output	fc = 12 MHz, DACS = 127		6.5	9.8	mV Rms
normal output	fc = 12 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	fc = 12 MHz, DACS = 127		3.1	4.7	mV Rms
32F8104					
differentiated output	fc = 9 MHz, boost = 0 dB		3.6	5.4	mV Rms
differentiated output	fc = 9 MHz, DACS = 127		5.6	8.4	mV Rms
normal output	fc = 9 MHz, boost = 0 dB		2.0	3.0	mV Rms
normal output	fc = 9 MHz, DACS = 127		2.7	4.1	mV Rms
Filter output sink current		0.5			mA
Filter output offset voltage		-200		200	mV
Filter output source current		2.0			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Ta = 127°C		800		mV
Rx resistance	1% fixed value		13.3		kΩ

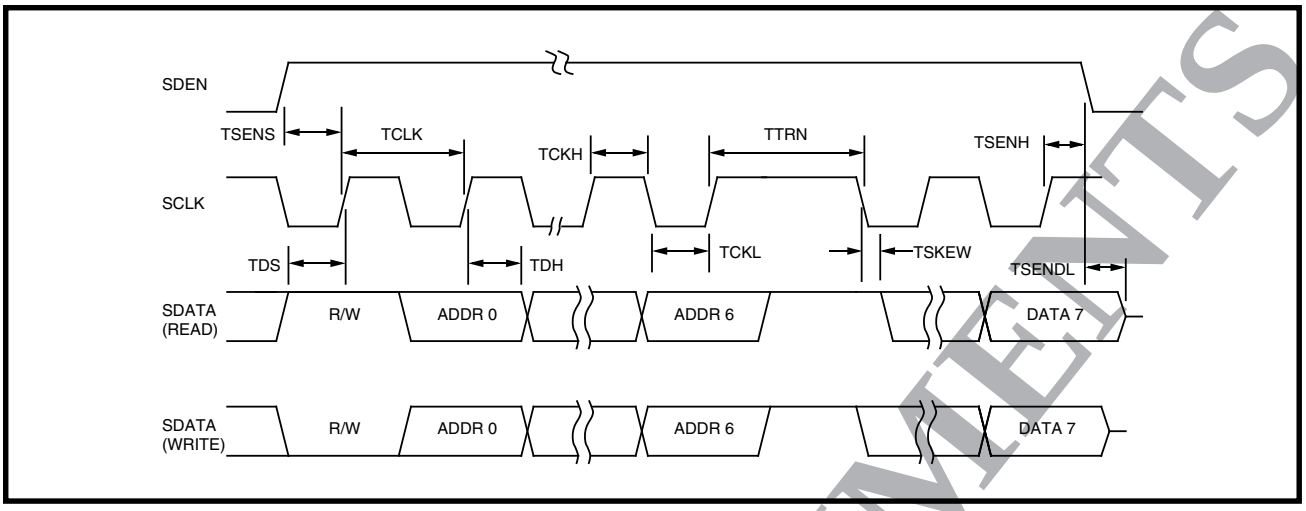


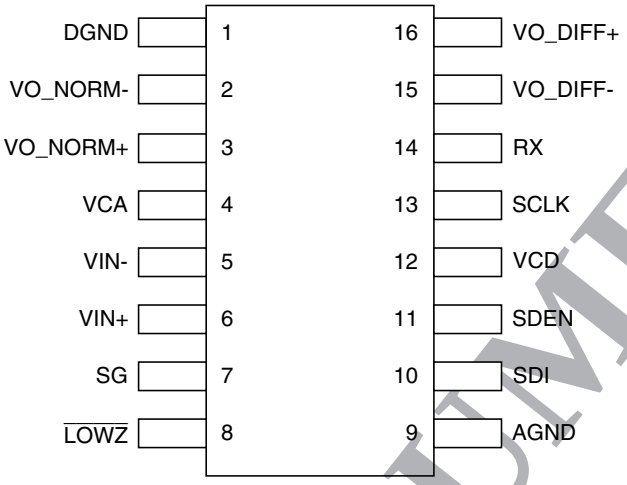
FIGURE 4: Serial Port Timing Information

PACKAGE PIN DESIGNATIONS

(Top View)

THERMAL CHARACTERISTICS: θja

16-lead SON	100° C/W



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8102	16-Lead SON	32F8102-CN	32F8102-CN
SSI 32F8103	16-Lead SON	32F8103-CN	32F8103-CN
SSI 32F8104	16-Lead SON	32F8104-CN	32F8104-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

HDD HEAD POSITIONING/ MOTOR CONTROL

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5-VOLT SERVO SPINDLE MOTOR CONTROL

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TLS2242
Servo-Combination Driver

March 1998

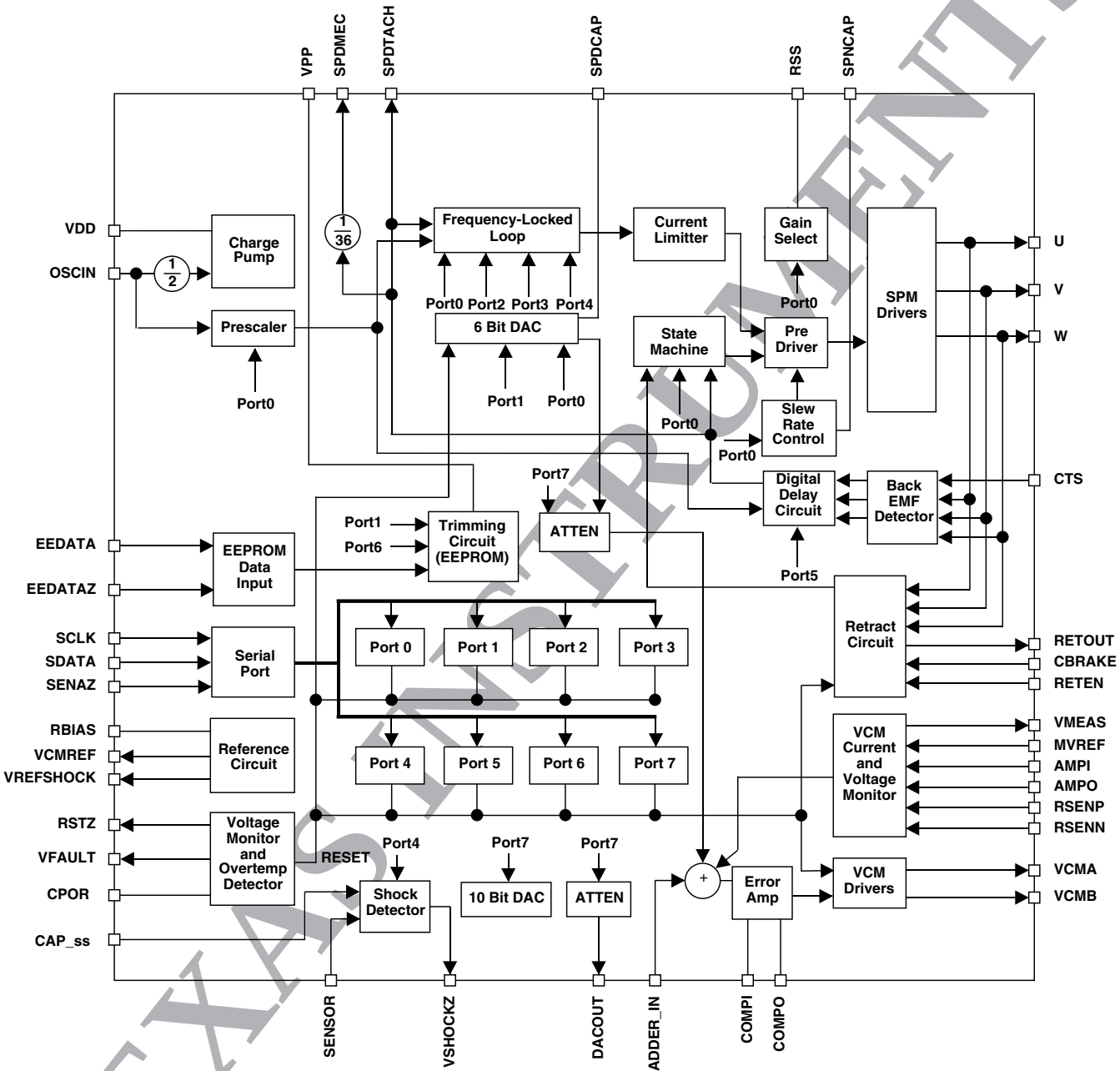
DESCRIPTION

The TLS2242 is a driver designed for use in 5 V hard-disk-drive (HDD) applications. The TLS2242 can drive a voice-coil motor (VCM) and spindle motor (SPM). Both the VCM and spindle sections are complete servo systems including power and predrivers requiring only a few additional discrete components for full functionality.

FEATURES

- **GENERAL**
  - **5 V operation**
  - **Serial Port Interface (20 Mbit/s data transfer rate)**
- **VOICE-COIL MOTOR (VCM) DRIVER**
  - **High efficiency drivers, 1.5 Ω on-state drain-source resistance (R_{DS}) total (worst case)**
  - **0.4 A capacity**
  - **3 gain ranges (1:2:8)**
  - **2 modes selectable for power-off Retract operation:**
    - **For CSS operation on-chip circuitry provides VCM voltage from spindle back electromotive force (EMF)**
    - **For ramp loading/unloading off-chip circuitry provides VCM voltage from spindle back EMF**
  - **10-bit DAC current control and 6-bit DAC for offset adjust control**
  - **Current and voltage monitor circuit for ramp loading**
  - **Sense resistor current control**
- **SPINDLE MOTOR DRIVER**
  - **High efficiency drivers, 1 Ω on-state R_{DS} total (worst case)**
  - **1 A capability**
  - **Digital commutation delay and blanking**
  - **Bipolar drive**
  - **Dynamic braking/power-off braking after retract**
  - **6-bit DAC for startup current control (also used as offset adjust for the VCM)**
  - **Driver slew rate control by setting an external capacitor**
  - **Frequency-locked loop (FLL) rotation speed control**
- **SHOCK DETECTION CIRCUIT**
  - **Shock sensor amplifier**
  - **On-chip low-pass filter (LPF) and shock detection voltage that is adjustable using serial port**
- **VOLTAGE MONITOR/VOLTAGE REFERENCE**
  - **Fault detector provides ±2% supply voltage tolerance**
  - **Reset circuit provides ±2% tolerance**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

SERIAL PORT

The serial port uses 16-bit data packets to program the eight internal registers of the TLS2242. Each data packet contains register address and control information.

VOICE-COIL MOTOR DRIVE

The VCM driver is a servo system for operating a VCM mechanism in an HDD unit. It consists of a full bridge power drive and a predriver. The power driver is an amplifier that uses an external sense resistor for current feedback. The predriver provides for external bandwidth limiting using discrete components for tailoring to particular mechanisms. Additional tailoring is provided through program control of the power-driver gain. Current command and offset inputs are made using the serial port interface control of the 10-bit and 6-bit digital-to-analog converters (DAC).

SPINDLE MOTOR DRIVE

The SPM driver system controls the spindle/disk assembly in a HDD. The servo system includes three identical power drivers and a predriver system. The three power drivers form the equivalent of a transconductance amplifier that has user selectable gain and slew rate. The predriver provides frequency lock servo control. A state machine controls the motor commutation sequence using the EXCOMM bit in serial port 0 or by the motor's back EMF zero crossings to advance the state machine.

SUPPORT FUNCTIONS

Support functions on the TLS2242 include a voltage monitor, charge pump, brake/retract, and shock detect circuits. Also included are a temperature monitor and two reference voltages. One reference voltage is used for an external analog-to-digital (A/D) converter and the other is used for the shock detect sensor.

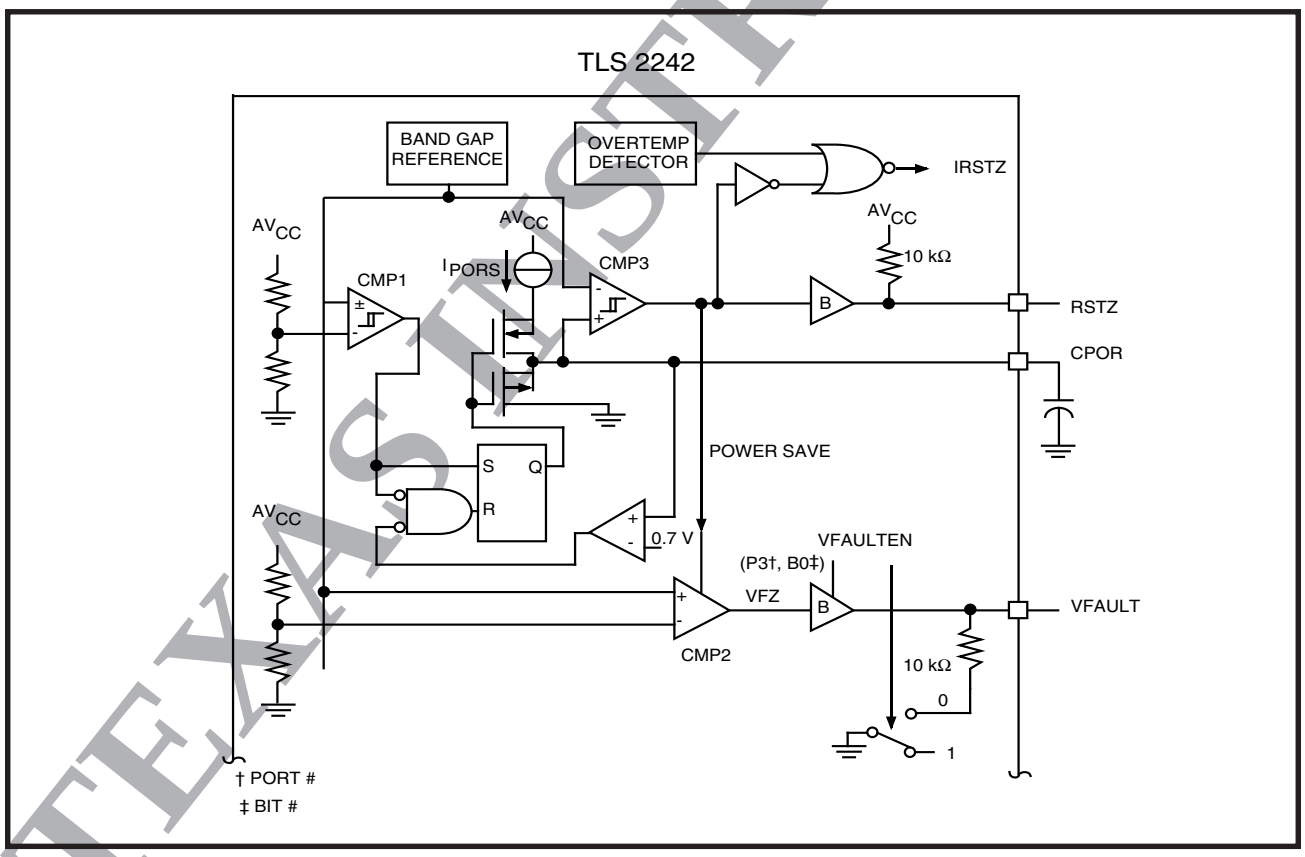


FIGURE 1: Voltage Monitor Circuit

FUNCTIONAL DESCRIPTION (continued)

VOLTAGE MONITOR

The voltage monitor generates an internal and an external power-on-reset (POR) signal. The internal signal is used as a general reset to retract the VCM actuator, and brake the SPM when power is turned off or a fault exists. A second external pin is provided for a capacitor that generates a power-on delay before the reset condition is released on power up.

CHARGE PUMP

The charge pump circuit generates a 10 V power source (pin 30, V_{DD}) from the external V_{CC} power source. This voltage is required for the SPM and VCM high–side, MOSFET gate controls and it powers internal circuits for the brake and retract functions during a power-fault condition. The V_{DD} pin allows connection of an external filter/storage capacitor.

BRAKE/RETRACT

The brake/retract function responds to a power fault by retracting the VCM when enabled by the RETEN pin. After a set delay, which allows the retract to complete, the brake signal activates the SPM braking circuits. External pins are provided for storing the SPM back EMF energy and for connecting a resistor (or short) between the VCM and the back EMF source.

SHOCK DETECTOR

A shock detector circuit is provided for external piezoelectric shock sensors. These signals are amplified and processed to produce a digital signal if the shock exceeds the selected limit as defined in the four shock-sensor bits of the port 4 register.

SERIAL PORT

The serial port is used to program the internal registers of the TLS2242 for all user-selectable functions.

Serial Port Timing

The serial port uses three control lines:

- SCLK (serial port clock)
- SDATA (serial port data)
- SENAZ (serial port enable, active low)

SDATA is the serial data signal and must be synchronous with the rising edge of SCLK. When SENAZ is high the input bit counter is reset. When SENAZ is low the next rising edge of SCLK begins loading SDATA into the 16-bit input data register. After the sixteenth clock the input register is transferred to the selected port register. SENAZ should return high between each 16-bit data transfer to ensure proper synchronization. The serial port timing and bit numbering are shown in Figure 2.

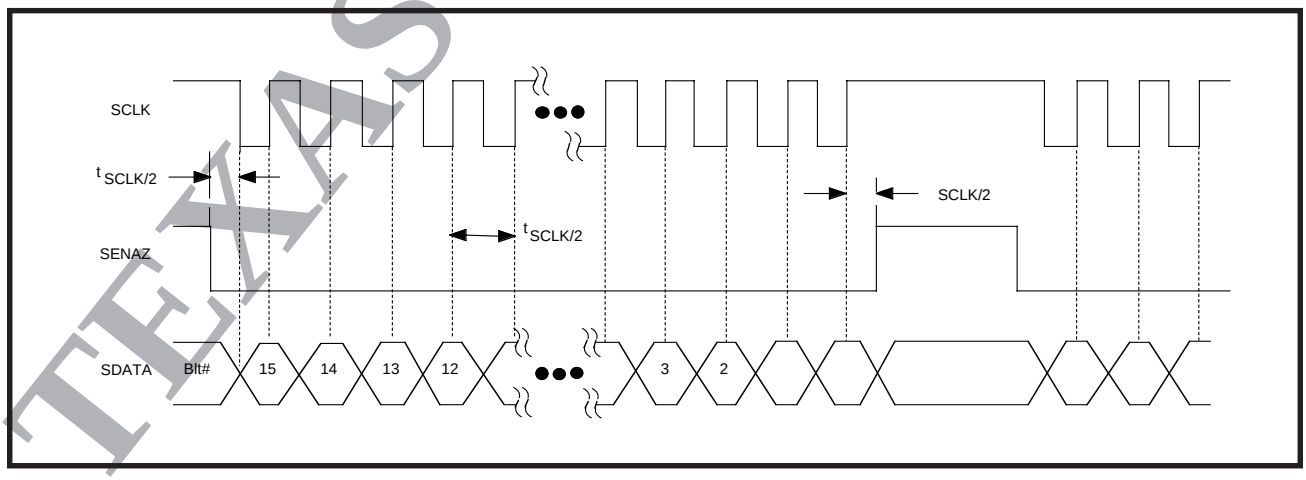


FIGURE 2: Serial Port Data Transfer

Port And Data Bit Definitions

The TLS2242 contains eight (seven of which are user programmable) internal registers that are programmed via the SCLK, SDATA, and SENAZ signals. A port address is determined by the TLS2242 by using data bits <15..13> as an address indicator to determine which port is selected. The following port address characteristics should be noted:

1. Port 7 is the only register accessed by setting PT3 = 1
2. Ports 2, 4 and 6 should only have to be set once after power-up under normal operation
3. Port 1, 3 and 5 are accessed by setting PT0 = 0, which is done by writing a 0 to bit <3> in Port 0
4. Port 2, 4 and 6 are accessed by setting PT0 = 1, which is done by writing a 1 to bit <3> in Port 0

TABLE 1: Internal Register Summary (See note)

This table summarizes the internal register contents.

Bit #	PORT 0	PORT1	PORT 2	PORT 3	PORT 4	PORT 5	PORT6	PORT 7
0	PS0	OFFSET0	RSD2	VFAULTENA	RSD0	PDT0	TI reserved	DAC0
1	PS1	OFFSET1	RSD3	TI reserved	RSD1	PDT1	TI reserved	DAC1
2	SPNENA	OFFSET2	RSD4	TI reserved	TI reserved	PDT2	TI reserved	DAC2
3	PT0	OFFSET3	RSD5	TI reserved	TI reserved	PDT3	TI reserved	DAC3
4	COMS	OFFSET4	RSD6	TI reserved	TI reserved	PDT4	TI reserved	DAC4
5	DACS	OFFSET5	RSD7	TI reserved	TI reserved	PDT5	TI reserved	DAC5
6	BRAKE	SPMCAS	RSD8	PVC0	TI reserved	PDT6	TI reserved	DAC6
7	HIZ	VCMOFFG	RSD9	PVC1	TI reserved	PDT7	TI reserved	DAC7
8	CCS	SELD6	RSD10	PVD0	DL0	PDT8	TI reserved	DAC8
9	SPMG	FLTZCRSENA	RSD11	PVD1	DL1	PDT9	TI reserved	DAC9
10	DT0	TI reserved	RSD12	SR	DL2	PDT10	TI reserved	VCMG0
11	DT1	TI reserved	RSD13	TI reserved	DL3	PDT11	TI reserved	VCMG1
12	EXCOMM	TI reserved	RSD14	TI reserved	TI reserved	SPDTACH_OUT	TI reserved	TI reserved
13	PT1	PT1	PT1	PT1	PT1	PT1	PT1	TI reserved
14	PT2	PT2	PT2	PT2	PT2	PT2	PT2	TI reserved
15	PT3	PT3	PT3	PT3	PT3	PT3	PT3	PT3

Note: TI reserved register bits must be programmed to 0.

Port 0	SPM control, power save
Port 1	6-bit DAC, SPM/VCM control, EEPROM
Port 2	Rotation speed setting 1
Port 3	FLL current control, slew rate control
Port 4	Rotation speed setting 2, rotation error setting, shock level setting
Port 5	Phase delay control, SPDTACH I/O control
Port 6	TEST circuit setting
Port 7	10-bit DAC data setting, DAC gain select

FUNCTIONAL DESCRIPTION (continued)

VOICE-COIL MOTOR CONTROL

The voice-coil motor (VCM) circuit is shown in Figure 3. It consists of a power and a predriver section. External connections are provided for a notch filter (if required by the HDD) and a compensation network to set gain, bandwidth, and phase response of the current amplifier.

VCM CURRENT MONITOR CIRCUIT

The VCM current montitor circuit provides an external output signal, VMEAS. Use the equation below to calculate the voltage of VMEAS.

$$VMEAS = \frac{R4}{R3}\left(I_{VCM}\, R_S \frac{R_2}{R_1} - V_{CM}\right) + V_{MR}$$

Where: $V_{VCM} = V_{RSENN}$ - VCMB

SPINDLE MOTOR CONTROL SYSTEM

The spindle motor system is a complete frequency-locked loop (FLL) speed feedback control system for controlling the speed of a three-phase brushless motor. It consists of two main sections: (1) speed control circuits and (2) phase winding commutation and current slewing circuits. The digital feedback signal, derived either internally from the back EMF zero crossings of the motor or externally from the data written on the disk, is compared to a digital reference signal. The error signal produced is then amplified and applied to the motor. The motor thus accelerates or decelerates until the two frequencies are the same. The power section of the spindle motor system converts the voltage at he SPDCAP to a proportional peak current level in the three spindle motor windings. It also performs the commutation and current slewing that allows the motor to be treated in the system as a simple dc motor. Control of the transconductance gain and slewing rate is programmed through the serial port.

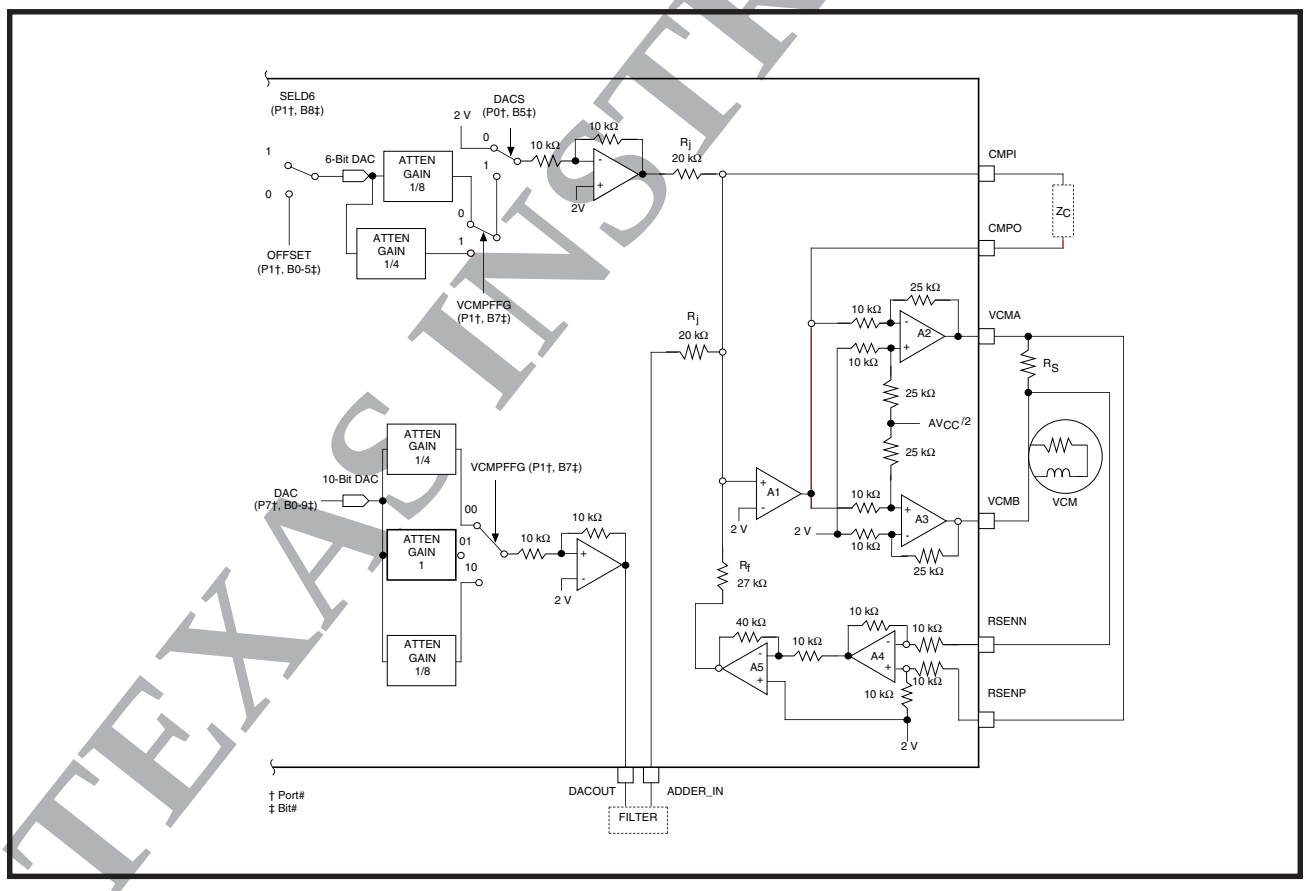


FIGURE 3: Voice-Coil Motor Control Circuit

Spindle Motor Current Control and Commutation Circuits

This system controls the amplitude and coil current slew rate in the three phase disk drive motor by controlling two phases while in steady state control and all three phases during commutations. Three sense FETs and six drivers (three pair of half H-bridges) are used to sense and control the steady state current through the coils, and control the current slew rate during commutations. The amplitude of the coil current is controlled by the low side drivers which operate in the MOS saturation region unless they are commutating or turned off. The high side drivers operate in the linear (resistive) region with their gates pulled to 5 V above the positive rail, unless they are commutating or turned off.

Frequency-Locked Loop Spindle Motor Speed Control Circuit

The speed control circuit for the TLS2242 is shown functionally in Figure 4. It consists of charge and discharge current sources that feed the external network connected to the SPDCAP pin, two sets of identical circuits consisting of velocity (frequency) comparator and a 15-bit preset counter, and a rotational signal generator.

Each comparator-counter pair controls the current sources for half the time period as determined by the timing signals from the rotation signal generator. The two current sources are individually controlled for four possible values by the PVC and PVD bits in Port 3. Because the voltage on the SPDCAP pin sets the desired output current level of the spindle motor predrive and control circuit, the FLL circuit controls the motor's torque, thus controlling the motor's speed.

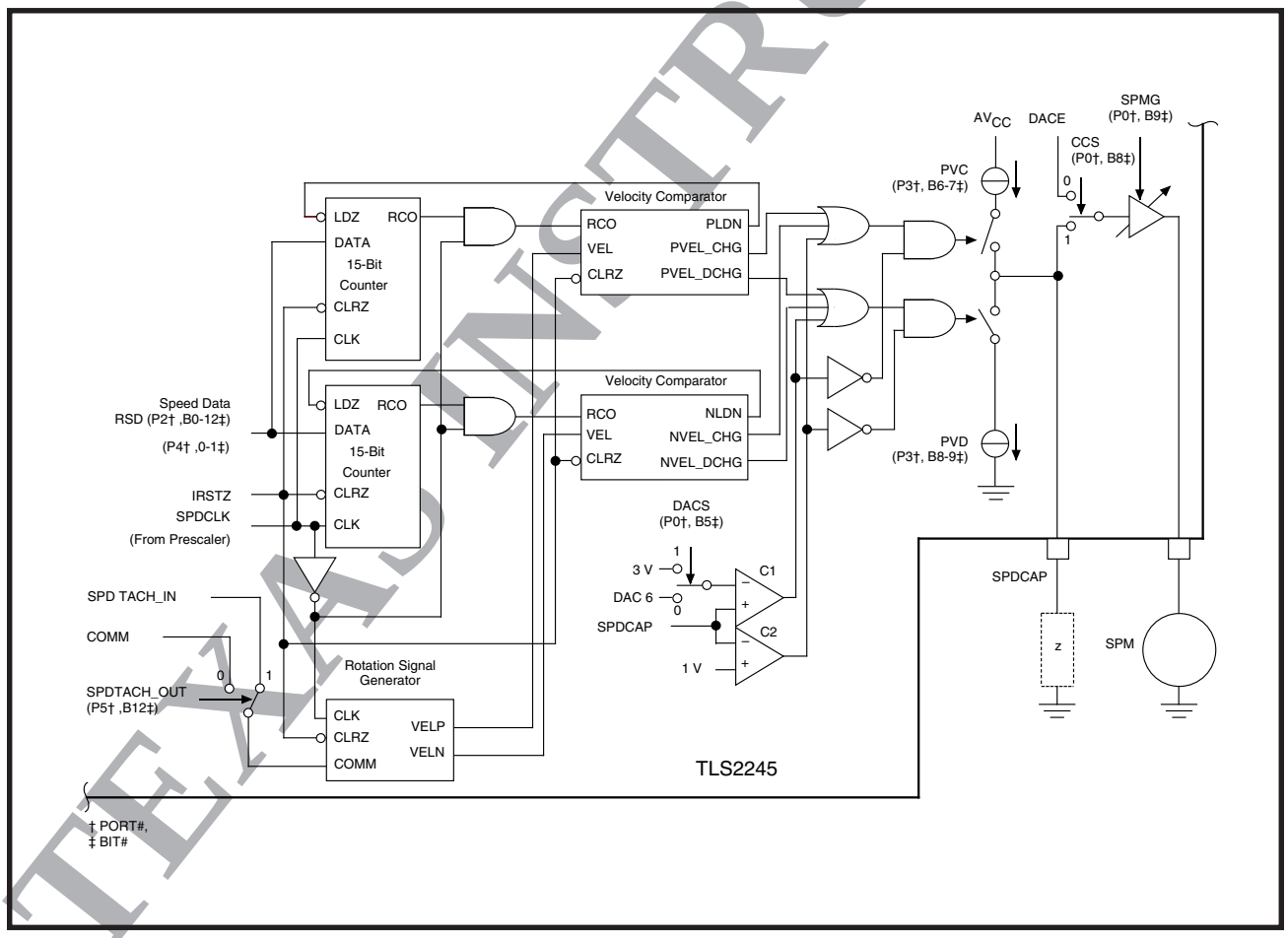


FIGURE 4: Frequency–Locked Loop Circuit

SPINDLE MOTOR CONTROL SYSTEM (continued)

Frequency Comparator

The frequency control circuit in Figure 4 consists of two identical frequency (velocity) comparator (or detector) circuits. They compare the frequency of two input signals, fref and ffb. The output is ideally proportional to the difference. The update rate for each of the frequency comparator circuits is once every 240° electrical degrees of motor rotation and the current output of each is summed at the SPDCAP pin. The total output over the full 240° period is thus twice the output of one of the frequency detectors. In other words, the overall detector gain is twice the gain of one detector over the 240° period.

SPDCAP Pin Compensation Network

To have a true frequency-locked loop speed control with no average frequency error there must be an integrator in the forward loop. The only place to do this in the TLS2242 is at the SPDCAP pin. If a simple capacitor is used, the system is unstable; therefore, a more complex network must be used. The simplest of these is a lead-lag network consisting of one resistor and two capacitors, as shown in Figure 5.

Speed Control Servo Loop Block Diagram

An overall speed control system block diagram is shown in Figure 6. The reference frequency, f_{ref}, is 1/T120. G_{fd} is the frequency discriminator gain factor. The motor transfer function, G_m, can usually be simplified to K_t/Js when the viscous damping constant, K_d, is small. $Z_{c(s)}$ is the compensation network, discussed in subsection 2.3.4, *SPDCAP Pin Compensation Network*, as found in the TLS 2242 Data Manual, connected to the SPDCAP pin. R_{ss} is the resistor connected to the RSS pin, which is 2 kΩ for nominal output current ranges. The power amplifier current gain, G_a, is selectable through the serial port as either 375 or 1500. The lower gain, corresponding to the 375 mA output current range, is sufficient for most HDD motors.

The generalized open loop gain is given in Figure 6.

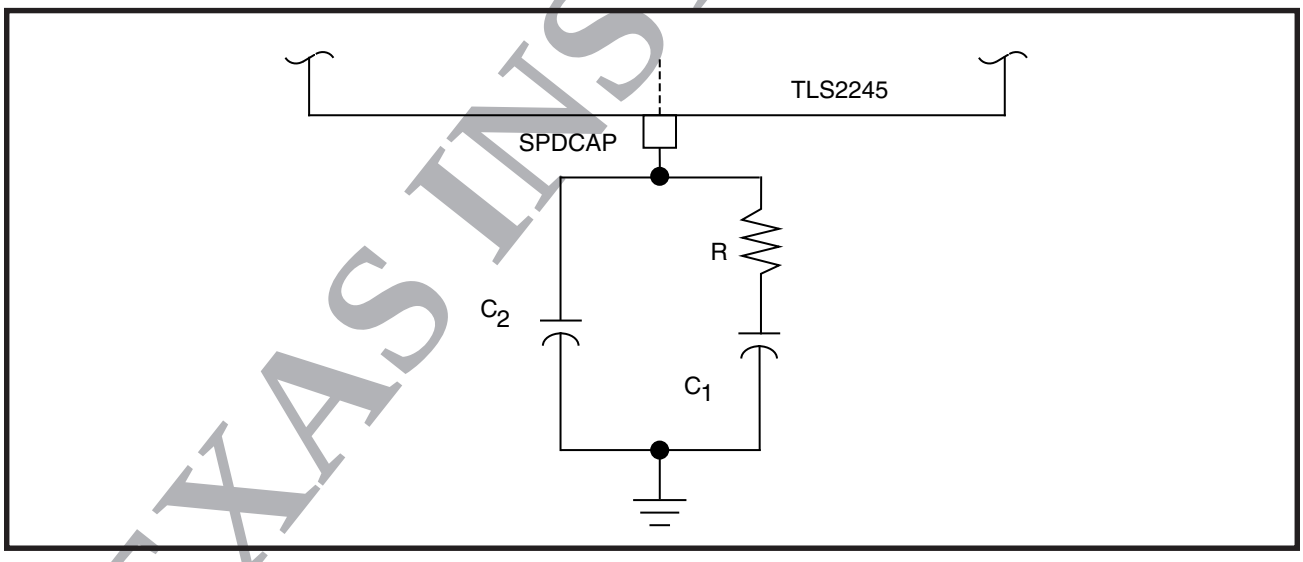


FIGURE 5: Lead-Lag Compensation Network

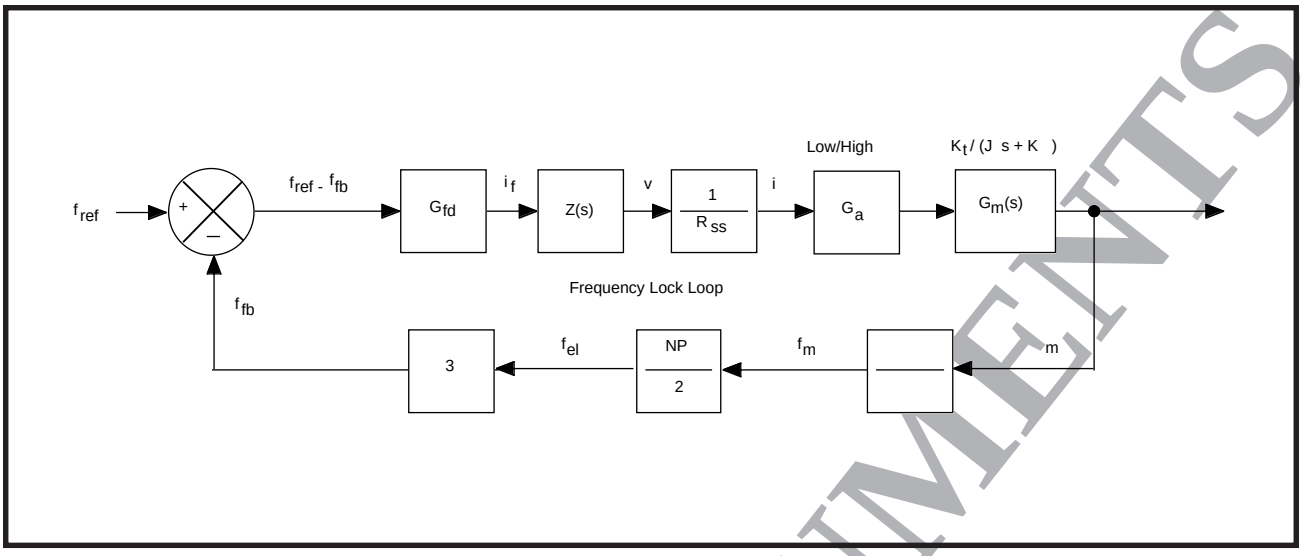


FIGURE 6: Speed Control Block Diagram

REGISTER DESCRIPTION

Port 0 Definition (SPM Control Circuit Mode Set/Power Save Control)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	PS0		Power save mode select 0 (see Power Save Mode Table)
1	PS1		Power save mode select 1
2	SPNENA	SPM	SPN enable
3	PT0		Port select address 0
4	COMS	SPM	1 : Hardware (back EMF) 0 : Software (EXCOMM)
5	DACS	SPM	6-bit DAC select. 1 : VCM 0 : SPM
6	BRAKE	SPM	Dynamic brake. 1 : Enable 0 : Disable
7	HIZ	SPM	All phase Hi-Z. 1 : Enable 0 : Disable
8	CCS	SPM/VCM	DAC/FLL mode control. 1 : FLL 0 : DAC
9	SPMG	SPM	Current gain select (see SPM Current Gain Table). 1 : GAIN1 0 : GAIN0
10	DT0	SPM	OSCIN prescaler divider 0 (see Prescaler Setting Table)
11	DT1	SPM	OSCIN prescaler divider 1 (see Prescaler Setting Table)
12	EXCOMM	SPM	Manual state machine advance
13	PT1		Port select address 1
14	PT2		Port select address 2
15	PT3		Port select address 3

Power Save Mode Select in Port 0

MODE SELECT	PS1	PS0	RESET CIRCUIT, BANDGAP REFERENCE	SPM CIRCUIT, CHARGE PUMP	VCM CIRCUIT, SHOCK SENSOR
MODE1	0	0	ON	OFF	OFF
MODE2	1	0	ON	ON	OFF
MODE3	1	1	ON	ON	ON

Prescaler Setting in Port 0

DT1	DT0	RATIO
0	0	1
0	1	2
1	0	4
1	1	8

SPM Current Gain

SPMG	GAIN
0	Low
1	High

Port 1 Definition (6-bit DAC / SPM Control)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	OFFSET0	SPM/VCM	6-bit DAC data (least significant bit (LSB))
1	OFFSET1	SPM/VCM	6-bit DAC data
2	OFFSET2	SPM/VCM	6-bit DAC data
3	OFFSET3	SPM/VCM	6-bit DAC data
4	OFFSET4	SPM/VCM	6-bit DAC data
5	OFFSET5	SPM/VCM	6-bit DAC data (most significant bit (MSB))
6	SPMCAS	SPM	1 : Cascode enable 0 : Cascode disable To improve gain accuracy in RUN mode
7	VCMOFFG	VCM	Selects 6-bit DAC attenuation. 0:1/8, 1:1/4
8	SELD6	VCM	Selects external/internal trim. 0:external, 1:internal
9	FLTZCRSENA	SPM	0:SPDTACH 1:Filtered back EMF
10–12	TI reserved		Set to 0
13	PT1		Port select address
14	PT2		Port select address
15	PT3		Port select address

Port 2 Definition (Rotation Control 1) (see Note 2)

0	RSD2	Spindle	Rotation speed data
1	RSD3	Spindle	Rotation speed data
2	RSD4	Spindle	Rotation speed data
3	RSD5	Spindle	Rotation speed data
4	RSD6	Spindle	Rotation speed data
5	RSD7	Spindle	Rotation speed data
6	RSD8	Spindle	Rotation speed data
7	RSD9	Spindle	Rotation speed data
8	RSD10	Spindle	Rotation speed data
9	RSD11	Spindle	Rotation speed data
10	RSD12	Spindle	Rotation speed data
11	RSD13	Spindle	Rotation speed data
12	RSD14	Spindle	Rotation speed data (MSB)
13	PT1		Port select address
14	PT2		Port select address
15	PT3		Port select address

NOTE 2: Low order (RSD0, RSD1) bits are in Port 4.

REGISTER DESCRIPTION (continued)

Port 3 Definition (Slew Rate / FLL Current Control)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	VFAULTENA	Voltage monitor	Enable voltage monitor output (pin 26) 1:Enable, 0:10 kΩ pulldown
1–5	TI reserved		Set to 0
6	PVC0	Spindle	FLL current control data (Velocity charge 0) (see table below)
7	PVC1	Spindle	FLL current control data (Velocity charge 1)
8	PVD0	Spindle	FLL current control data (Velocity discharge 0) (see table below)
9	PVD1	Spindle	FLL current control data (Velocity discharge 1)
10	SR	Spindle	Slew rate 1:on(slow), 0:off(fast)
11–12	TI reserved		Set to 0
13	PT1		Port select address
14	PT2		Port select address
15	PT3		Port select address

FLL Speed Control Charge Current Source in Port 3

PVC1	PVC0	VELOCITY CHARGE CURRENT (NOMINAL)
0	0	100 µA
0	1	200 µA
1	0	400 µA
1	1	800 µA

FLL Speed Control Discharge Current Source in Port 3

PVD1	PVD0	VELOCITY DISCHARGE CURRENT (NOMINAL)
0	0	100 µA
0	1	200 µA
1	0	400 µA
1	1	800 µA

Port 4 Definition (Rotation Control 2 / Shock Detection Level Set)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	RSD0	Spindle	Rotation speed data (LSB) (see Note 3)
1	RSD1		Rotation speed data
2–7	TI reserved		Set to 0
8	DL0	Shock sensor	Shock detection level (LSB) (see Port 7 Definition Table)
9	DL1	Shock sensor	Shock detection level
10	DL2	Shock sensor	Shock detection level
11	DL3	Shock sensor	Shock detection level (MSB)
12	TI reserved		Set to 0
13	PT1		Port select address
14	PT2		Port select address
15	PT3		Port select address

NOTE 3: High order (RSD <2..14>) bits are in port 2.

Port 5 Definition (Phase Delay Control)

0	PDT0	Spindle	Phase delay time (PDT) data (LSB)
1	PDT1	Spindle	Phase delay time data
2	PDT2	Spindle	Phase delay time data
3	PDT3	Spindle	Phase delay time data
4	PDT4	Spindle	Phase delay time data
5	PDT5	Spindle	Phase delay time data
6	PDT6	Spindle	Phase delay time data
7	PDT7	Spindle	Phase delay time data
8	PDT8	Spindle	Phase delay time data
9	PDT9	Spindle	Phase delay time data
10	PDT10	Spindle	Phase delay time data
11	PDT11	Spindle	Phase delay time data (MSB)
12	SPDTACH_OUT	Spindle	SPDTACH I/O select. 1: Input 0: Output
13	PT1		Port select address
14	PT2		Port select address
15	PT3		Port select address

Port 6 Definition

0–12	TI reserved		Set to 0
13	PT1		Port select address
14	PT2		Port select address
15	PT3		Port select address

REGISTER DESCRIPTION (continued)

Port 7 Definition (VCM 10-bit DAC / VCM Current Range Control)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	DAC0	VCM	10-bit DAC data
1	DAC1	VCM	10-bit DAC data
2	DAC2	VCM	10-bit DAC data
3	DAC3	VCM	10-bit DAC data
4	DAC4	VCM	10-bit DAC data
5	DAC5	VCM	10-bit DAC data
6	DAC6	VCM	10-bit DAC data
7	DAC7	VCM	10-bit DAC data
8	DAC8	VCM	10-bit DAC data
9	DAC9	VCM	10-bit DAC data
10	VCMG0	VCM	Gain Select data
11	VCMG1	VCM	Gain Select data
12–14	TI reserved		Set to 0
15	PT3		Port select address

VCM Gain Select in Port 7

VCMG1	VCMG0	GAIN
0	0	0.25
0	1	1
1	0	0.125
1	1	0.2 (see Note 4)

NOTE 4: Not tested. For information only.

PIN DESCRIPTION

Terminal Functions

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
SUPPLIES				
AV_{CC}	40		Power	5 V analog power supply
DV_{CC}	7		Power	5 V digital power supply
$VCMV_{CC}$	51		Power	VCM power supply (2 bond pads)
$SPNV_{CC}$	13,18		Power	Spindle power supply (2 bond pads)
AGND	1*,12,28*29,44,56*		Ground	Analog ground
DGND	10		Ground	Digital ground
VCMGND	48		Ground	VCM ground (2 bond pads)
SPNGND	16,20		Ground	Spindle ground (2 bond pads)
VPP	6		Power	5 V power supply and EEPROM programming voltage
MISCELLANEOUS				
RBIAS	31	—	Analog	Internal bias current setting
VDD	30	—	Analog	Charge-pump capacitor
OSCIN	4	I	Digital	Charge pump and commutating clock
VCM				
VCMA	50	O	Analog	VCM driver output A
VCMB	49	O	Analog	VCM driver output B
VCMVREF	34	O	Analog	2 V VCM reference output
CMPO	42	—	Analog	VCM current loop compensation filter
CMPI	41	—	Analog	VCM current loop compensation filter
DACOUT	43	O	Analog	DAC output (10 bit)
ADDER_IN	45	I	Analog	Adder input
RSENN	46	I	Analog	VCM negative current sense input
RSENP	47	I	Analog	VCM positive current sense input
AMPI	39	—	Analog	Gain-setting resistor connection
AMPO	38	—	Analog	Gain-setting resistor connection
MVREF	37	I	Analog	Reference voltage input
VMEAS	36	I	Analog	VCM current monitor output
RETOU	21	O	Analog	Retract voltage output
RETEN	8	I	Digital	Internal retract enable

NOTE: The symbol (*) indicates additional pins that can be used for heat sinking.

Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
VOLTAGE MONITOR				
RSTZ	53	O	Digital	Power-on reset output
CPOR	27	O	Analog	Power-on reset delay capacitor
VFAULT	26	O	Digital	Voltage fault output (enabled by VFAULTENA, otherwise 10 kΩ pulldown)
SERIAL PORT				
SCLK	55	I	Digital	Serial port input clock
SDATA	2	I	Digital	Serial port data
SENAZ	3	I	Digital	Serial port select (Active low)
SPINDLE MOTOR				
U	14	O	Analog	Spindle phase U output
V	17	O	Analog	Spindle phase V output
W	19	O	Analog	Spindle phase W output
CTS	11		Analog	Center tap sense
SPDTACH	5	I/O	Digital	SPDTACH_OUT = 1: Uses external input rather than internal zero-back-EMF crossings for speed information SPDTACH_OUT = 0: Spindle tachometer output using delayed-back-EMF-zero crossings
SPDCAP	9	—	Analog	SPM speed control compensation network connection
RSS	22	—	Analog	Maximum SPM current-limiting resistor
SPNCAP	23	—	Analog	Spindle slew-rate-control capacitor
CBRAKE	24	—	Analog	Timer capacitor for the brake-after-retract delay
SPDMEC	54	O	Digital	Index pulse
SHOCK DETECTION CIRCUIT				
VSHOCKZ	52	O	Digital	Shock detection output
SENSOR	32	I	Analog	Shock sensor Input
CAP_SS	33	I	Analog	Capacitor that sets high-pass filter cut-off frequency
VREFSHOCK	35	O	Analog	Shock sensor reference voltage output
PINS WITH NO CONNECTS				
NC	15	—		No internal connection

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER FREE-AIR TEMPERATURE RANGE
(unless otherwise noted)†

PARAMETER	RATING
Supply voltage range: Spindle motor, $SPNV_{CC}$ (see Note 1) .	-0.3 V to 6 V
Voice-coil motor, $VCMV_{CC}$ (see Note 1)	-0.3 V to 6 V
Bias supply voltage range: AV_{CC} , DV_{CC} (see Note 1) .	-0.3 V to 6 V
Input voltage range, V_I (see Note 2)	-0.3 V to 6 V
Spindle DC current, I_{S-DC} : U,V,W (see Note 3)	1.2 A
Spindle PEAK current, I_{S-PEAK} : U,V,W	1.5 A
VCM DC current, I_{V-DC} : VCMA, VCMB (see Note 3)	±0.5 A
VCM PEAK current, I_{V-PEAK} : VCMA, VCMB	±0.6 A
Package power dissipation, T_A = 70°C	0.94 W
Operating virtual junction temperature, T_J	≤150°C
Thermal resistance: junction-to case, $R_{\Theta JC}$	10°C/W
Junction-to-ambient, $R_{\Theta JA}$ (see Note 4)	85° C/W
Storage temperature range	-55°C to 125°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	250°C

NOTES: 1. All voltage values are with respect to ground.

2. Since VCMA, VCMB, VSENN, and VSENP are connected to inductive loads, particular care must be taken to not let these pins exceed 6 V. Snubbers or other voltage limiting devices may be required.

3. To be limited less than 2 seconds at 50% maximum duty cycle with proper heat sinking.

4. A lower $R_{\Theta JC}$ is attainable if the exposed pad is connected to a large copper ground plane.

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply voltage, DV_{CC} , AV_{CC} , $SPNV_{CC}$,$VCMV_{CC}$	See Note 5	4.5	5.0	5.5	V
Digital high-level input voltage SCLK, SDATA, SENA, SPDTACH V_{IH}		0.6 DV_{CC}		DV_{CC} +0.3	V
Low-level input voltage SCLK, SDATA, SENA, SPDTACH V_{IL}				0.3 DV_{CC}	V
Supply current Icc	MODE1		2	3	mA
See Notes 6 and 7	MODE2			13.6	mA
	MODE3			16.6	mA
High-level logic input current I_{IH}	See Note 7			1.0	µA
Low-level logic input current I_{IL}	See Note 7			-1.0	µA
Low-level output voltage V_{OL}	Io = 100 µA, See Note 7			0.4	V
High-level output voltage V_{OH}	Io = -100 µA, See Note 7	DV_{CC} - 0.5			V
Power-on reset delay time setting range, trdsr	trdsr = 1.07 C_{por}•10^6 See Note 8	1		150	ms
SPM current range		0		1.0	A
Startup current	See Note 9			1.0	A
Acceleration current Less than 3 seconds and duty cycle is 50%			0.5		A
Rotation current (after acceleration)	See Note 9			0.35	A
Slew rate (SR) control range	See Note 10	1	2	3	mA/µs
VCM current range		0		±0.4	A
OSCIN input frequency range	40 MHz prescale minumum = 2	8		40	MHz

RECOMMENDED OPERATING CONDITIONS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
OSCIN rise time				3	ns
OSCIN fall time				3	ns
R_{BIAS}	See Note 11	79.6	80	80.6	kΩ
R_{SS} output resistance	See Note 9	1	2.5	6	kΩ
Operating ambient temperature		0		70	°C

NOTES: 5. Chip is functional down to 4.02 V.

6. Select MODE1, 2, and 3 using PS0 and PS1 (See Register Description Table: Power Save Mode Select in Port 0). $I_{CC} = I_{DVCC} + I_{AVCC}$ (Power driver current is not included).

7. These are tested parameters.

8. C_{por} is chosen to provide enough time for the power supply to reach an operating level.

9. RSS sets the maximum SPM current. The RSS output voltage varies between 0 and 2 V. I_{max} = (Current Gain) _ $2/R_{SS}$, Current gain = high or low. (See Electrical Specification: Spindle Driver)

10. The minimum SR allowed at any given speed (RPM) and motor current (ISPM)i is limited by the minimum allowable off time, of any phase current, required in to ensure proper BEMF zero crossover detection. This minimum is 30° electrical which results in a minimum allowable slew time of 30° electrical. The following equation is for an N_P pole motor at a speed of N_{rpm} (rpm) : SR(A/s) > ISPM(A) N_P N_{rpm} (rpm)/10. Note that this minimum slew rate may or may not be within the recommended operating condition above.

11. Output current =1.6/R, minimum tolerance for R_{BIAS} is 1%.

ELECTRICAL SPECIFICATIONS (continued)

3.3 ELECTRICAL CHARACTERISTICS, AV_{CC} AND DV_{CC} = 5 V ± 10 %, T_A = 25 °C

The TLS2242 is designed for operation within the specifications of this section over a temperature range of 0°C to 75°C with AV_{CC} and DV_{CC} from 4.5 V to 5.5 V. Parameters are verified under these conditions on the qualification test material. Final production testing is performed to the specification in this section only at 5.0 V and 25°C.

VOLTAGE/TEMPERATURE MONITOR (SEE FIGURES 6 AND 1)

SYMBOL PARAMETER TEST

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Power-on reset threshold voltage	Vpor		4.00	4.09	4.18	V
Power-on reset hysteresis	Vh		50	100	150	mV
Minimum operating voltage	Vop			0.7	0.8	V
CPOR source current	Ipors		1.4	1.7	2	µA
Bandgap voltage	Vbgref	25°C	1.584	1.60	1.616	V
		75°C	1.56	1.60	1.63	V
CPOR “H” voltage	Vcporh		AV_{CC} - 0.5 V	AV_{CC}		V
CPOR discharge time (90% – 10%)	tdc	C = 0.1 µF			15	µs
Reset response time 1	trpd1			2	5	µs
Reset response time 2	trpd2			2	5	µs
Fault response time 1	tfpd1	see Note 12		2	5	µs
Fault response time 2	tfpd2		0			µs
Fault response time 3	tfpd3			2	5	µs
Power supply fault detection range	Vfault		4.06	4.17	4.28	V
Delta V (V_{fault} -V_{por})	dV		0.05	0.1	0.15	V
Thermal shutdown hysteresis	Tsdh	See Note 13	10	30	50	°C
Thermal shutdown temperature	Tsd	See Note 13	150	170	190	°C
Voltage at RBIAS pin	V_{RBIAS}	R_{BIAS} = 80 kΩ to GND	1.56	1.6	1.64	V

NOTES: 12. VFAULT signal is active 5 µs maximum after it is enabled through the serial port.
13. Not tested. They are determined by design characterization.

CHARGE PUMP

Charge pump output voltage	VDD	OSCIN = 40 MHz	9	10	11	V
Rise time	tvddon	CVDD = 680 nF OSCIN =10 MHz			50	ms
Fall time (see Note 14)	tvddoff	CVDD = 680 nF	5			s

NOTE 14: This is the time that VDD changes from 10 V to 5 V after power off.

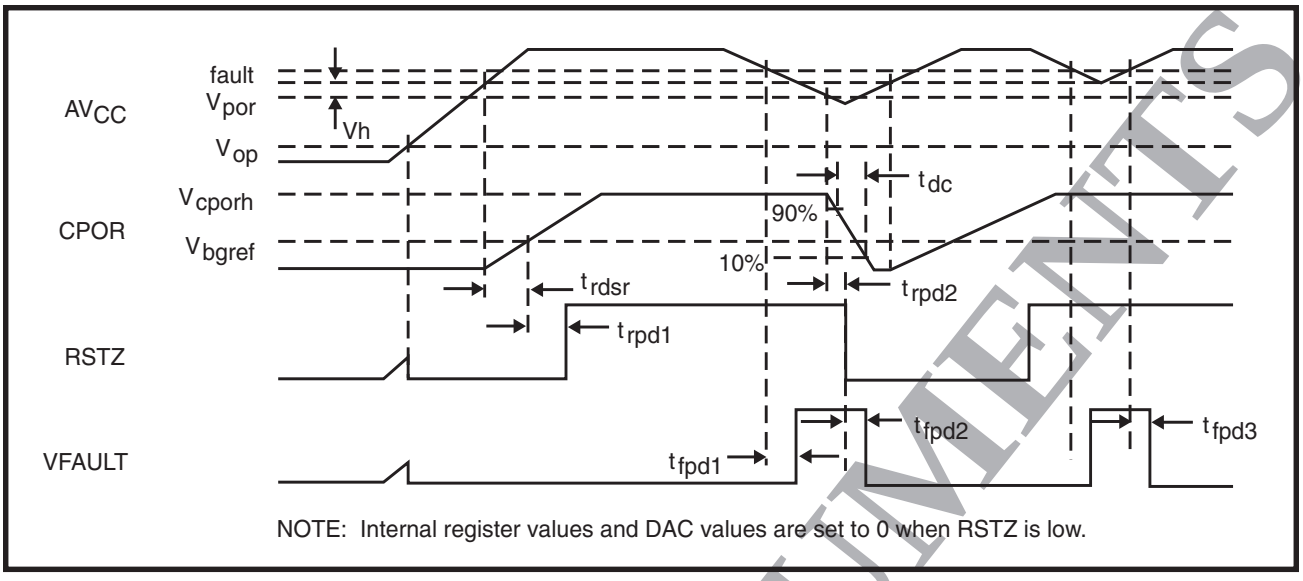


Figure 7. Voltage Monitor Timing Chart

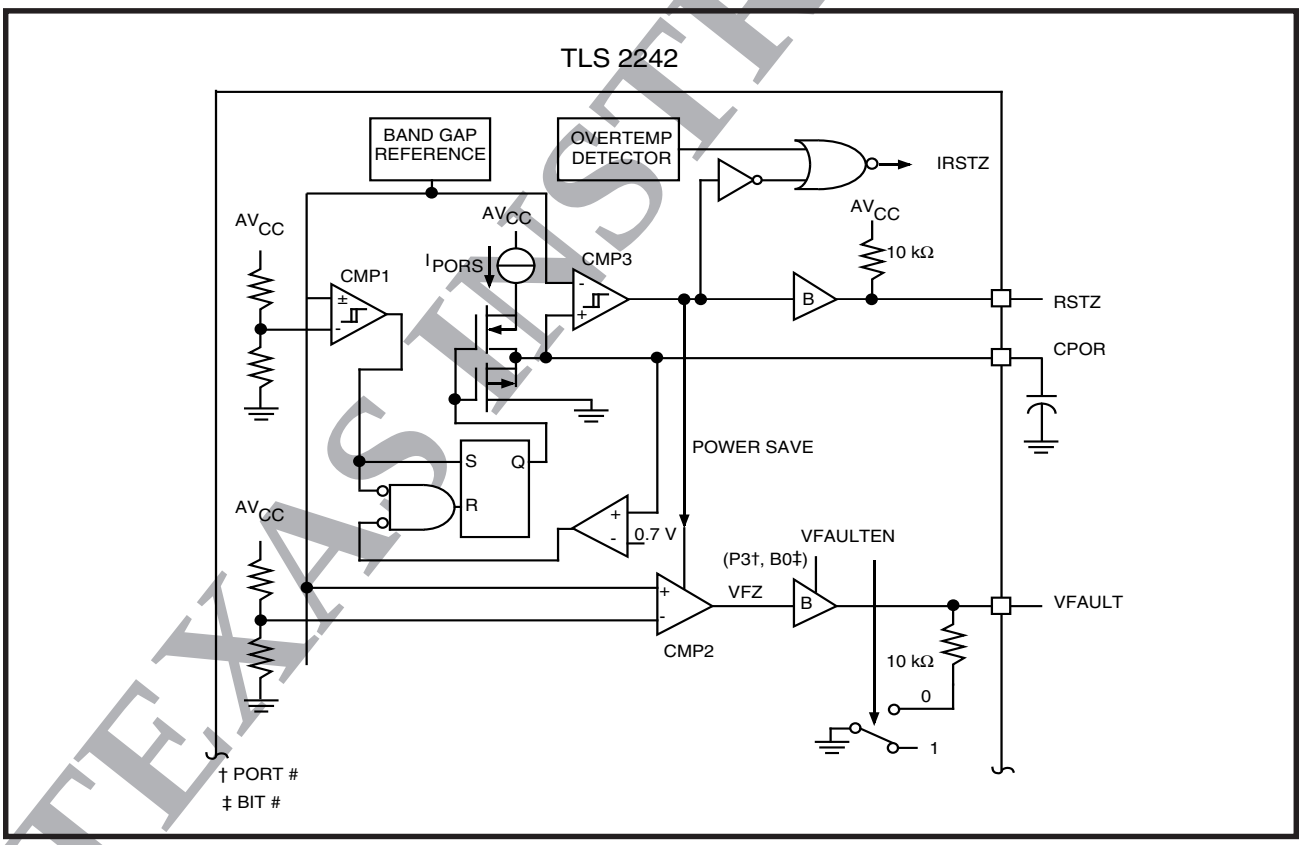


Figure 8. VCM Current Monitor Circuit

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT (SEE FIGURE 1 FOR DEFINITIONS)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Fclock clock frequency, SCLK	fsclk		1		20	MHz
Minimum pulse width, SCLK	tsclk		15			ns
SDATA setup time for SCLK	tdset	(see Note 15)	5			ns
SDATA hold time for SCLK	tdhold	(see Note 15)	5			ns
SENAZ setup time for SCLK	teset	(see Note 15)	5			ns
SENAZ hold time for SCLK	tehold	(see Note 15)	5			ns

NOTE 15: Time is measured from a SDATA or SENAZ state change to the rising edge of SCLK.

VCM RETRACT AND SPM BRAKE (See Register Description Table: Power Save Mode Selection Port 0)

Forward voltage across CR1, 2, or 3, plus, Retract MOS drain-to-source voltage (see Note 16)	Vfd +Vhds	ICRET = 70 mA			1.25	V
Voltage from drain to source (V_{DS}) of MOS low side driver	Vlds	ICRET = 70 mA			112	mV
Spindle motor brake delay (see Notes 17 and 18)	t_{BKDLY}	CBRAKE = 0.1 µF	0.06	0.1	0.14	s

NOTES: 16. Vfd and Vhds cannot be measured individually but only as a combined total of Vfd + Vhds. Vfd + Vhds is the average of the combined diode and MOS transistor voltage drop for each of the 3 diodes CR1, 2, or 3 measured one at a time.

17. The brake delay is measured as the active time of the RETOUT signal after V_{CC} power is removed. The brake delay for different values of CBRAKE is:

$$t_{BKDLY} \text{ (sec)} = KC_{BRAKE} \text{ (µF)}$$

Where:

K = 1 (s/µF) nominal

Range of K is 0.9 < K < 1.9

18. Specifications that are shaded are design goals. Final values are subject to negotiation.

VCM DRIVER AMPLIFIER (SEE FIGURE 3–6)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Total Rds(on) for HSD and LSD (see Note 19)	IVCM = 400 mA, T_A = 70°C		1.2	1.7	Ω
	IVCM = 400 mA, T_A = 25°C		1.1	1.6	Ω
Crossover distortion	ADDER_IN = 100 mVpk, f = 15 kHz, Z_C =10 kΩ, R_S = 0.75 Ω, R_L = 10 Ω			1	LSB
Transconductance loop bandwidth (3 dB)	ADDER_IN = 100 mVpk, R_S = 0.75 Ω, R_L = 10 Ω in lieu of motor, Z_C = 10 kΩ	15			kHz
VCM total offset current VCMOFC	SELD6 = 1, VCMOFFG = 0, V_{CC} = 5 V, DAC10 = 200h, R_S = 0.75 Ω	-5	0	+5	mA
VCM offset variation with respect to V_{CC} VCMOFV	SELD6 = 1, VCMOFFG = 0, V_{CC} = 4.5 to 5 V, DAC10 = 200h, RS = 0.75 Ω		0	1	mA

NOTE 19: Production test @ 25°C (Using Rds(on) from characterization data for 70°C).

ELECTRICAL SPECIFICATIONS (continued)

VCM 10-BIT DAC (See Note 20)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Resolution			10		Bits
Differential nonlinearity DNL (see Note 21)				±1/2	LSB
Integral nonlinearity INL				±5	LSB
Conversion time from -0.5 LSB to 0.5 LSB	(see Note 22)			2	µs
Supply rejection PSRR	AV_{CC} = ±5% f = 5 KHz	50			dB
Output impedance				50	Ω
Absolute attenuator gain AATG	1	-3%	1	3%	V/V
	1/4	-3%	0.25	3%	V/V
	1/8	-3%	0.125	3%	V/V
Relative attenuator gain RATG	1:0.125	-6%	8	6%	V/V
	1:0.25	-6%	4	6%	V/V
	0.25:0.125	-6%	2	6%	V/V

NOTES: 20. DAC output voltage range is from 1 V at min DAC to 3 V at max DAC.
21. Not tested. They are determined by design characterization.
22. Duration measured from DAC data input to VCM DAC output measured at SPDMEC (test) output pin.

VCM CURRENT/VOLTAGE MONITOR (See Register Description Table: Port 1 Definition)

Bandwidth (–1 dB)		300			KHz
MVREF input range VMVREF		2.57	2.70	2.83	V
VMEAS output voltage	Ro = 20k	0.5		AV_{CC} - 0.5	V
PSRR	f = 1 kHz	60			dB
Amplifier output current (I_O) (source or sink)				1	mA
Absolute resistor value, R3 thru R6	R	0.65R	R	1.35R	Ω
Output offset voltage (VMEASOSV = VMEAS - 2.5 V, see Functional Description: VCM Current Monitor Circuit) VMEASOSV	AMPI = AMPO, RSENN = VCMB = MVREF = 2.5 V	–100		+100	mV
Second stage gain (VMEAS6N = Δ VMEAS/ ΔVCMB, see Functional Description: VCM Current Monitor Circuit) VMEAS6N	AMPI = AMPO, RSENN = MVREF = 2.5 V, input at VCMB	3.8	4	4.2	V/V

VCM REFERENCE VOLTAGE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
$VCMV_{ref}$	I_L = 0 µA	1.98	2	2.02	V

SPINDLE DRIVER

Total FET resistance, each high-side/low-side combination (see Note 23) RON1	ISPN = 1.0 A T_A = 70°C		1	1.2	Ω
	ISPN = 1.0 A T_A = 25°C		0.9	1.1	Ω
SPM current (see Note 24)	RSS = 2 kΩ	0		1.0	A
SPM current gain SPMG0	SPMG = 0, SPMCAS = 1	350	525	700	mA/mA
SPM current gain SPMG1	SPMG = 0, SPMCAS = 0	250	400	550	mA/mA
	SPMG = 1, SPMCAS = 1	1500	1900	2300	mA/mA
	SPMG = 1, SPMCAS = 0	1100	1500	1900	mA/mA
Absolute slew rate SR	Port 3, bit 10 = 0 (see Notes 25 and 26)	1.3	1.8	2.3	mA/µs
Relative slew rate accuracy 1 HSD to HSD between phases	(see Notes 25 and 26)	-3		+3	%
Relative slew rate accuracy 2 LSD to LSD between phases	(see Notes 25 and 26)	-3		+3	%
Relative slew rate accuracy 3 HSD to HSD vs LSD to LSD	(see Notes 25 and 26)	-10		+10	%

NOTES: 23. Production test @ 25°C (Using Rds(on) from characterization data for 70°C).

24. Spindle current should be limited by the following equation.
AV_{CC} = VBEMF + ISPM • (RSPM + 1.0) + VSAT
Where:
AV_{CC} = Supply voltage
VBEMF = SPM back EMF voltage
ISPM = SPM current
VSAT = LSD saturation voltage and this voltage is dependent on ISPM.

25. The slew rate depends on the spindle motor parameters, peak current, and the value of the SPNCAP. The following are the parameters for the values given for SR: SPNCAP = 1 nf, ISPM = 100 mA, R_M = 4.8 Ω, L_M = 430 µH, RPM = 4000, and k_t = 83 g cm/A, PDT commutation delay = 100 µs.

26. These parameters cannot be measured. They are determined by design characterization.

ELECTRICAL SPECIFICATIONS (continued)

SPINDLE 6-BIT DAC (VCM OFFSET ADJUST DAC)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Resolution			6		Bits
Differential nonlinearity	Monotonic			±0.5	LSB
Conversion time	Full swing amplitude		28	40	µs
	1 LSB amplitude		2	3	µs

SPM BACK EMF PHASE COMPARATOR

Offset voltage		-10	0	10	mV
Response time	30 mVpk-pk input square wave @ 2 V			1	µs

SPM BACK EMF PHASE DELAY CIRCUIT

Prescaler divide ratio (see Note 27)		1		8	
Number of counter bits				12	Bits

NOTE: 27. Phase delay circuit counter frequency equals f = OSCIN/ratio. See Register Description: Prescaler Setting in Port 0.

FLL SPEED CONTROL CIRCUIT (See Note 28)

Velocity charge current	PVC1 = 0, PVC0 = 0, R_{BIAS} = 80 kΩ		100		µA
	PVC1 = 0, PVC0 = 1, R_{BIAS} = 80 kΩ		200		µA
	PVC1 = 1, PVC0 = 0, R_{BIAS} = 80 kΩ		400		µA
	PVC1 = 1, PVC0 = 1, R_{BIAS} = 80 kΩ		800		µA
Velocity discharge current	PVD1 = 0, PVD0 = 0, R_{BIAS} = 80 kΩ		100		µA
	PVD1 = 0, PVD0 = 1, R_{BIAS} = 80 kΩ		200		µA
	PVD1 = 1, PVD0 = 0, R_{BIAS} = 80 kΩ		400		µA
	PVD1 = 1, PVD0 = 1, R_{BIAS} = 80 kΩ		800		µA
Absolute accuracy, charge to discharge	For 100 and 200 µA			±15	%
	For 400 and 800 µA			±15	%
Relative accuracy, charge to discharge	For 100 and 200 µA			±25	%
	For 400 and 800 µA			±20	%

NOTE 28: These specifications do not include any error in R_{BIAS}. The current is inversely proportional to R_{BIAS}.

SHOCK DETECTION CIRCUIT (See Register Description: Prescaler Setting in Port 0)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Shock detection voltage (see Note 29)	DL3,DL2,DL1,DL0 = 0,0,0,0	0.8 • NOM	3.5	1.2 • NOM	mV0–p
	0,0,0,1	0.8 • NOM	4.0	1.2 • NOM	mV0–p
	0,0,1,0	0.8 • NOM	4.6	1.2 • NOM	mV0–p
	0,0,1,1	0.8 • NOM	5.3	1.2 • NOM	mV0–p
	0,1,0,0	0.8 • NOM	6.1	1.2 • NOM	mV0–p
	0,1,0,1	0.8 • NOM	7.0	1.2 • NOM	mV0–p
	0,1,1,0	0.8 • NOM	8.1	1.2 • NOM	mV0–p
	0,1,1,1	0.8 • NOM	9.3	1.2 • NOM	mV0–p
	1,0,0,0	0.8 • NOM	10.7	1.2 • NOM	mV0–p
	1,0,0,1	0.8 • NOM	12.3	1.2 • NOM	mV0–p
	1,0,1,0	0.8 • NOM	14.2	1.2 • NOM	mV0–p
	1,0,1,1	0.8 • NOM	16.3	1.2 • NOM	mV0–p
	1,1,0,0	0.8 • NOM	18.7	1.2 • NOM	mV0–p
	1,1,0,1	0.8 • NOM	21.5	1.2 • NOM	mV0–p
	1,1,1,0	0.8 • NOM	24.8	1.2 • NOM	mV0–p
	1,1,1,1	0.8 • NOM	28.5	1.2 • NOM	mV0–p
Input bias current, SENSOR input				±20	nA
Output offset voltage V_{OS} |Shockout–$V_{REFSHOCK}$[1] (see Register Description: Prescaler Setting in Port 0)	Gain at highest value (P4, B8 - 11 = 0, input connected as in Register Descripiton: Prescaler Setting with a short circuit replacing the sensor.			100	mV
HPF cut-off frequency	@ -3 dB, CI = 0.82 µF	20	30	45	Hz
LPF cut-off frequency	@ -3 dB (see Note 30)	2.5	3.1	3.5	KHz
VREFSHOCK voltage1 $V_{refshock}$[1]	I_{source} = 0 µA	1.96	2.0	2.04	V

NOTE: 29. ±35% variation over temperature range (0 - 70°C).

NOTE: 30. Input signal to result in shock error.

MECHANICAL DATA

The TLS2242 mechanical outline dimensions are shown in Figure 8.

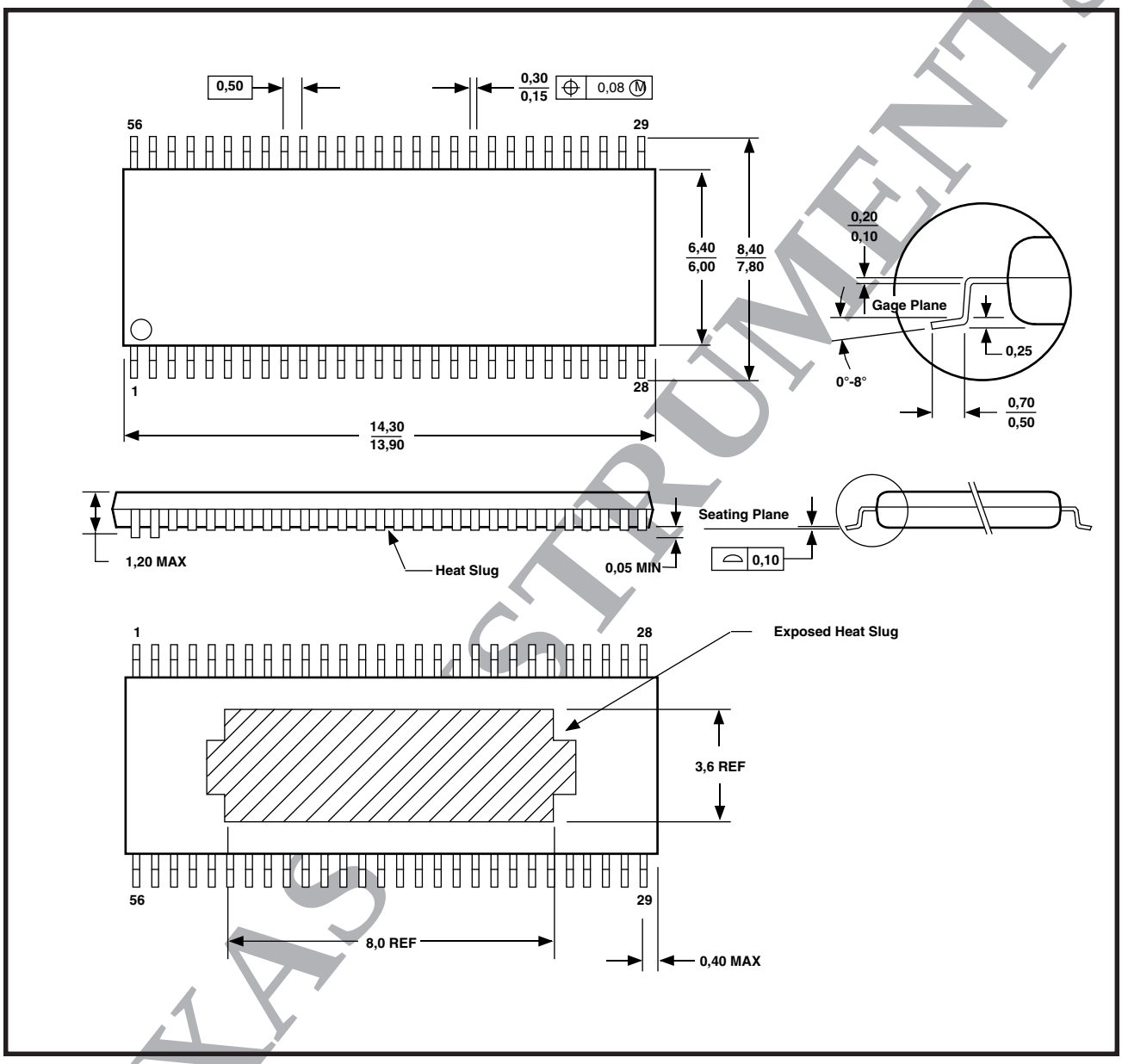


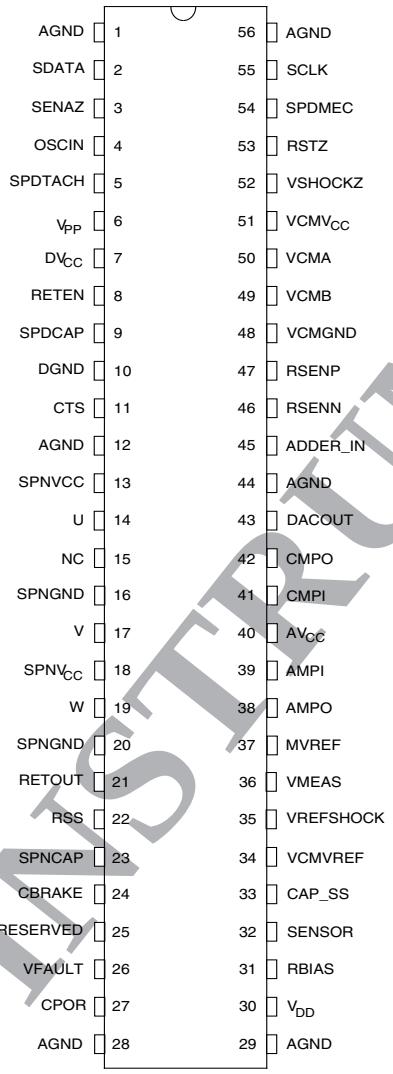
FIGURE 8: Mechanical Data

Notes:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with an exposed heat slug (HSL) on bottom

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



TLS2242

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TI TLS2242 56-Pin Servo-Combination Predriver	TLS2242CDLR	T2242CB

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

12-VOLT SERVO SPINDLE MOTOR CONTROL

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SSI 32H6826A
Advanced Servo & Spindle Predriver

Prototype

April 1998

DESCRIPTION

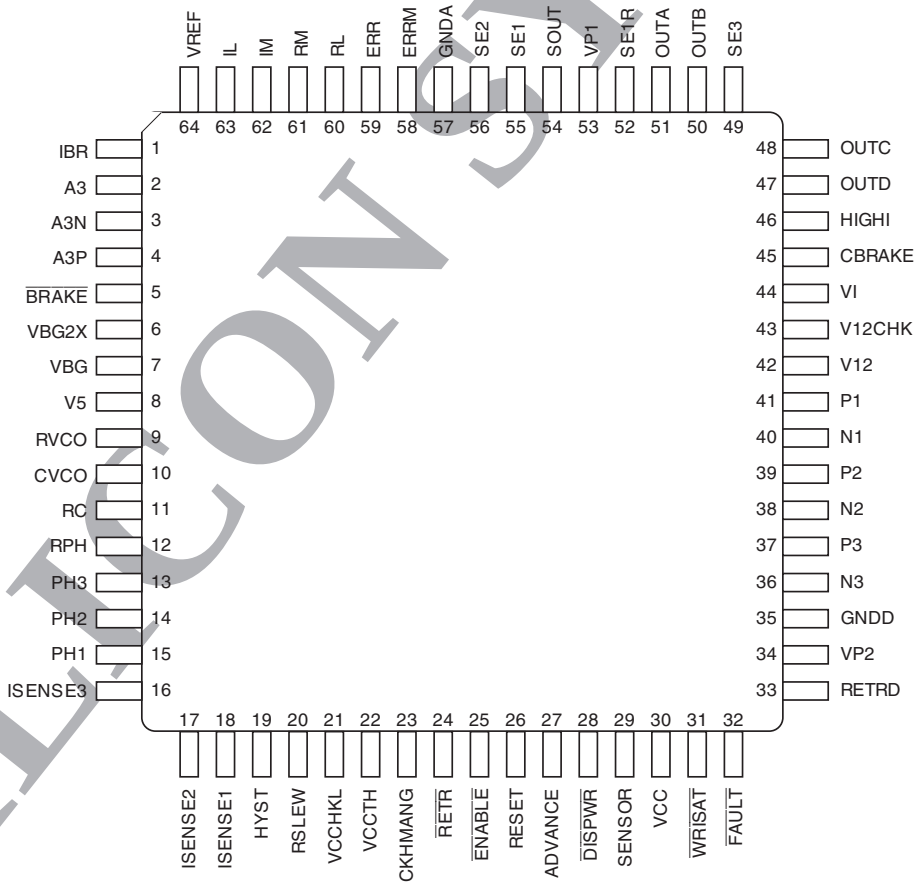
The SSI 32H6826A Advanced Servo and Spindle Predriver is designed to drive a 3-phase sensorless motor and a voice coil actuator with external MOS power devices. The SSI 32H6826A is an advanced version of the SSI 32H6825A actuator and spindle predriver.

The primary enhancement to the SSI 32H6825A is the SILENTSPIN™ spindle technology. This technology provides a PWM spindle motor driver with current waveforms which are optimized for quiet spindle operation.

FEATURES

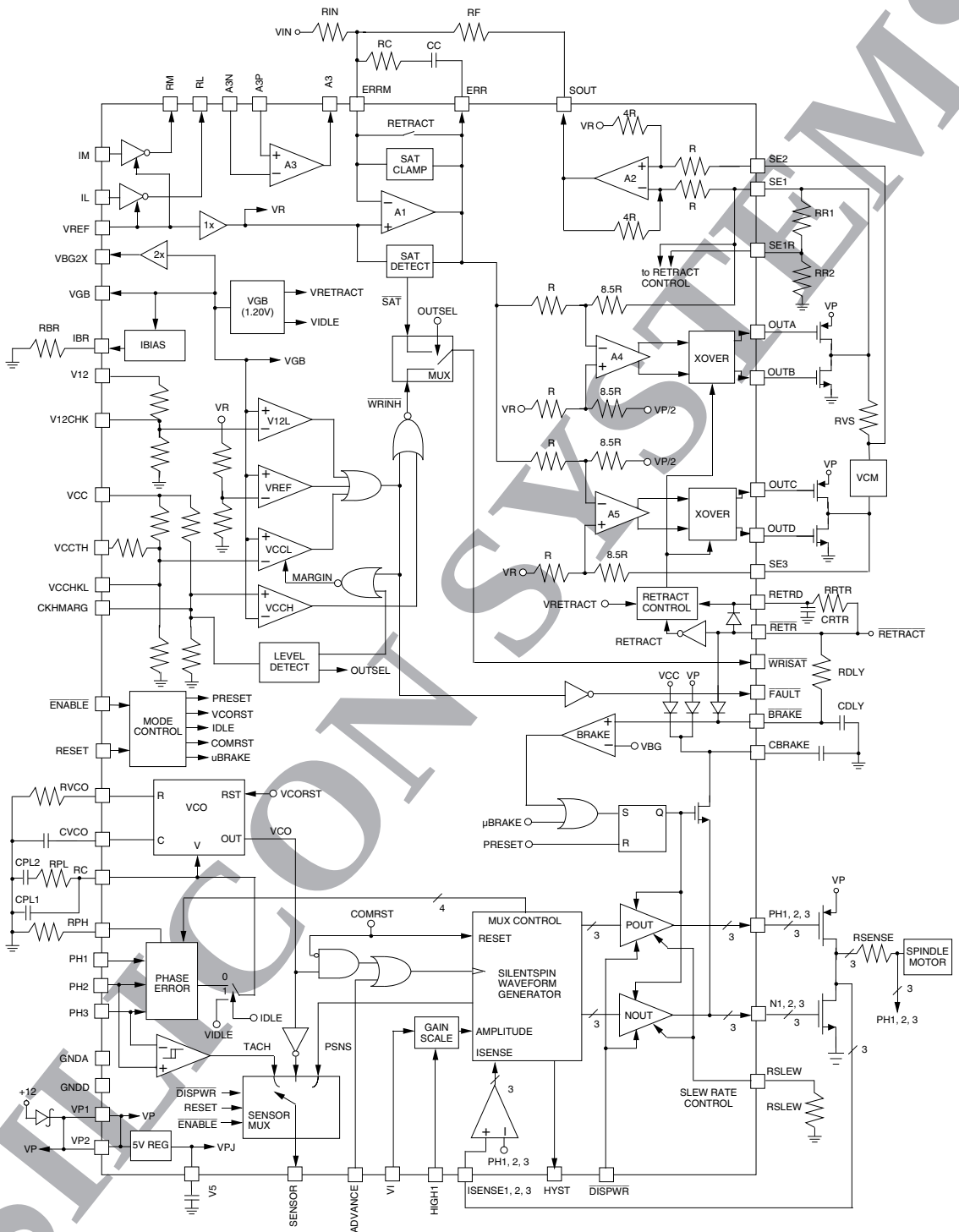
- **PWM spindle driver during start and run**
- **SILENTSPIN™ technology shapes the motor current to minimize acoustic noise**
- **Commutator is driven by a phase lock loop for high jitter immunity**
- **Small footprint 64-Lead TQFP package**
- **Microprocessor controlled spindle start-up**
- **Dual PWM DAC interface buffers**
- **Precision dual supply fault detection**
- **Dual level retract scheme with adjustable pulse-width**

PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 32H6826A functional block diagram contains an actuator predriver, a spindle predriver section, a voltage reference and monitor section, and dual PWM interface buffers.

ACTUATOR PREDRIVER

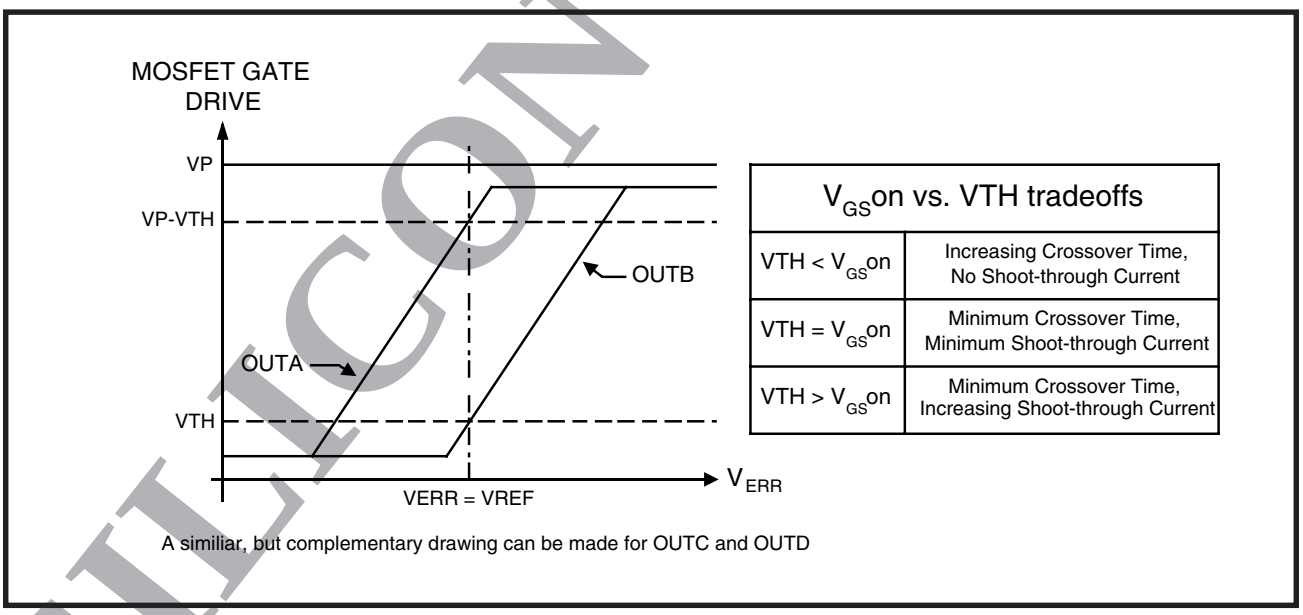
The actuator predriver serves as a transconductance amplifier by driving four power MOSFETs in an H-bridge configuration. It has two modes of operation, normal (linear) and retract. The retract mode is activated by an external command at $\overline{RETR}$. Otherwise, the device operates in linear mode. Referring to SSI 32H6826A block diagram, the actuator section consists of A1 through A5 the SAT detect, the SAT clamp, the retract control and the XOVER blocks. It is functionally similar to the SSI 32H6825. Error amplifier saturation detection is provided by a window comparator scheme that detects when the absolute value of ERR-VR exceeds 0.9 V nominal. The actuator predriver circuits are designed to operate with VREF = 5 V provided by connecting VREF to V5. The SSI 32H6826A has been enhanced to provide a dual level retract sequence.

Loop Compensation Amplifier

During linear operation, the acceleration signal is applied through A1. RC components may be used to provide loop compensation at this stage. The saturation detect circuit monitors amplifier A1. It senses that the error amplifier is being overdriven and activates the internal $\overline{SAT}$ signal. This signal can be steered to the open collector $\overline{WRISAT}$ output (see Table 2). The saturation clamp circuit clamps the error amplifier when it is being overdriven. This prevents the amplifier from fully saturating and provides a faster recovery if the positioner is driven beyond its maximum closed loop operation.

MOSFET Drivers

ERR, the output signal of A1, drives two precision amplifiers, each with a gain of 8.5. The first of these two amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed similarly from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a current sense resistor are connected in series between SE1 and SE3.



V_{GS}on vs. VTH tradeoffs	
VTH < V_{GS}on	Increasing Crossover Time, No Shoot-through Current
VTH = V_{GS}on	Minimum Crossover Time, Minimum Shoot-through Current
VTH > V_{GS}on	Minimum Crossover Time, Increasing Shoot-through Current

FIGURE 1: Crossover Protection

ACTUATOR PREDRIVER (continued)

Crossover Protection Blocks

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs , ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover seperation threshold VTH, illustrated in Figure 1, is the maximum drive on any MOSFET gate when the motor voltage changes sign.

Retract Function

The SSI 32H6826A incorporates a dual level retract scheme. When retract is initiated, a fixed voltage (level 1) is applied across the actuator to force a constant retract velocity. After an externally adjustable amount of time, a higher voltage (level 2) is briefly applied to the actuator. At the end of level 2, the actuator is floated (i.e. zero current).

The timing and amplitude of the level 2 phase can be adjusted with external components. R_{RTR}, C_{RTR}, and an internal discharge resistor which is activated during level 2 control the retract timing. When $\overline{RETR}$ is first lowered, R_{RTR} discharges C_{RTR} until the RETRD pin reaches the level 2 trigger threshold (nominally 0.85 V). At this time, the level 2 retract amplitude is applied to the acturator and the internal discharge resistor (nominally 32 K) quickly discharges C_{RTR}. When C_{RTR} has been discharged to half of the trigger voltage all retract current is turned off and the actuator is floated. The level 1 retract amplitude is internally fixed (0.85V nominal). During level 2 amplitude will be increased by the factor (1 + R_{R1}/ R_{R2}).

A second external RC delay is used between $\overline{RETR}$ and $\overline{BRAKE}$ to program the break delay and ensure the actuator has enough time to retract before the spindle is braked.

Current Sense Amplifier

Actuator current is sensed by a small series resistor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired current and the actual motor current.

ERRAMP Saturation Detect

This circuit senses that the error amplifier is being overdriven and activates the $\overline{SAT}$ open collector output.

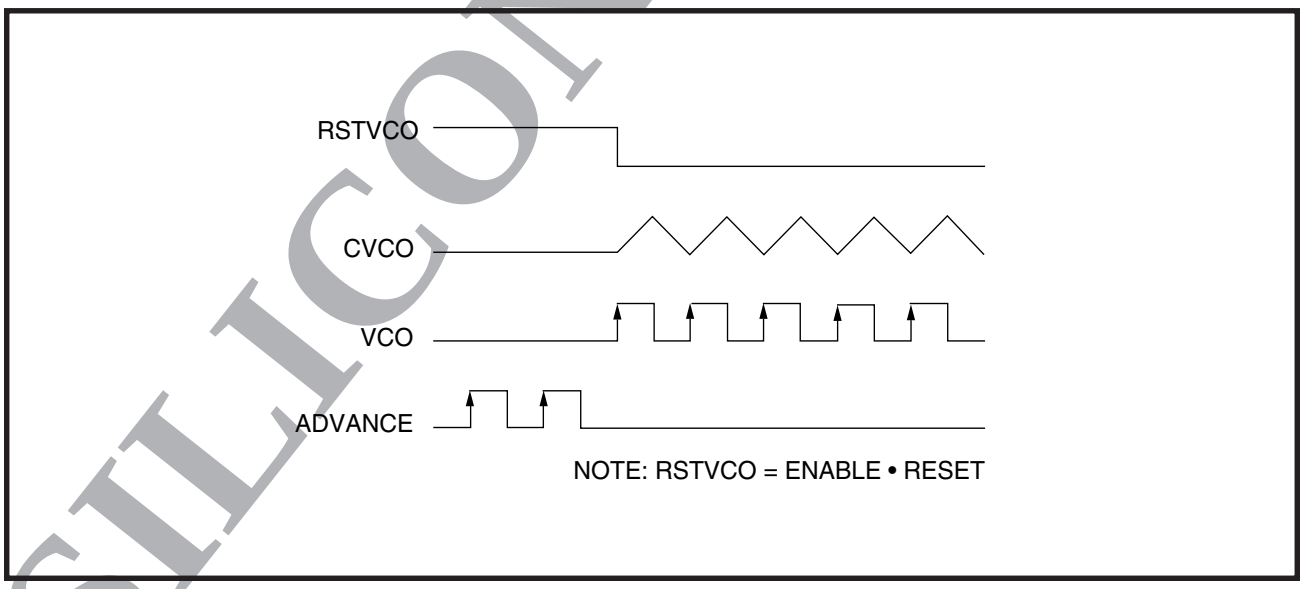


FIGURE 3: VCO Timing Relationship

SPINDLE PREDRIVER

The spindle section generates drive signals to three external MOSFET power bridges. It provides spindle motor current shaping, back emf monitoring to determine commutation phase, a phase locked loop to remove jitter from the commutation times, and a delayed spindle brake circuit. The current shaping circuit employs Silicon System's SILENTSPIN™ technology which minimizes acoustic noise.

SILENTSPIN™ Waveform Generator

The SILENTSPIN™ wave generator drives the spindle motor windings with properly phased current waveforms. In run mode, the generator is clocked by the VCO output. During start mode, the generator is clocked by external pulses supplied by the ADVANCE pin.

The analog signal at VI controls the peak amplitude of the current waveforms. With HIGHI high, when VI is 2.4 V, the peak current in each winding will correspond to 150 mV drop across each RSENSE resistor. When HIGHI is low, the peak current is reduced 4x to 37 mV across each RSENSE resistor.

Phase Error Amplifier

The PHASE ERROR circuit determines the phase error between the current and voltage in each winding. Depending on the result of the comparison and the phase of the commutator, a positive or negative pump current is applied to the RC pin.

The magnitude of the pump current at RC is the sum of a constant current and a current proportional to the VCO frequency. The constant current value is set by RPH which is biased to 1.2 V nominally. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on CVCO is nominally 2 V. The frequency formula is:

$$F_{VCO} = \frac{V_{RC}}{4 \bullet R_{VCO} \bullet C_{VCO}}$$

When the VCO is reset, the VCO output is forced low. The first VCO clock will occur immediately after the VCO exits reset. This timing relationship is shown in Figure 3.

NOUT and POUT

The NOUT and POUT outputs drive the gates of the N and P channel power FETs. Except during BRAKE, both the NOUT and the POUT drivers are switched with PWM. During BRAKE, the NFETs are turned on and the PFETs are turned off. To minimize electrical switching noise, the charge and discharge currents at NOUT and POUT can be adjusted with RSLEW. RSLEW is biased at 1.2V. The output current is 100x the current through RSLEW.

TABLE 1: Spindle Operating Modes

RESET	ENABLE	$\overline{\text{DISPWR}}$	MODE	SENSOR	RC	VCO	WAVEGEN
1	1	x	Preset	VCO	V_{IDLE}	Idle	Reset
0	1	x	Start	PSNS	V_{IDLE}	Reset	Run
0	0	1	Run	VCO	Run	Run	Run
0	0	0	Coast	TACH	Run	Run	Run
1	0	x	Brake	VCO	V_{IDLE}	Idle	Reset

SPINDLE PREDRIVER (continued)

Spindle Mode Table

The spindle driver modes are governed by the RESET, $\overline{\text{ENABLE}}$, and $\overline{\text{DISPWR}}$ inputs according to Table 1. As shown in the table, spindle braking is activated in "brake" mode. Spindle braking, whether activated by the mode controls or by a power failure is internally latched and is cleared only by asserting "preset" mode.

Sensor MUX

The sensor mux output is multiplexed from VCO, the VCO output; TACH, the PH2 and PH3 comparator; and PSNS, the position sense comparator. Its output is governed by the RESET, $\overline{\text{ENABLE}}$, and $\overline{\text{DISPWR}}$ inputs according to Table 1.

STARTING ALGORITHMS

The SSI 32H6826A supports two types of starting algorithms: a simple "preset and go" which may cause some reverse rotation, and a "position sense and go" which determines the starting position of the motor and avoids the reverse rotation.

Spindle Start - PRESET-AND-GO

This conventional start algorithm begins by asserting the preset mode. During this mode, while $\overline{\text{DISPWR}}$ is low, the motor will be forced to a known position. Also during this mode, the commutator is reset and the VCO idles. To begin rotating the motor, the µP asserts start mode and pulses ADVANCE at an accelerating rate until the idle frequency is reached. (If desired, the exact idle frequency can be measured by the µP during Preset.) Note that during start mode, the VCO is held reset to zero degrees. When the idle frequency is reached, instead of issuing the next ADVANCE pulse, the µP asserts run mode and keeps ADVANCE low. The VCO will immediately issue a clock and begin oscillating thus generating a phase continuous transition to internal commutation. The spindle will accelerate on its own in run mode. Spindle speed can be determined by measuring the SENSOR frequency.

$$FREQ_{RPM} = \frac{2 \bullet F_{VCO\ Hz}}{N_{Poles}}$$

Spindle Start - POSITION SENSE-AND-GO

This algorithm and the previous are the same except this one includes estimating the rotor position and then selecting an initial commutation state that is appropriate. The initial state can be selected so that no reverse rotation occurs. The rotor position is sensed by measuring the rise times of each winding with current in each direction. The VI pin is programmed to generate a current pulse whose rise time is measured by the difference in time from raising $\overline{\text{DISPWR}}$ to the corresponding rise of SENSOR while the spindle operating mode is set to start.

PRECISION VOLTAGE REFERENCE AND MONITOR

The voltage monitor section is new to this part. Circuitry is included to monitor VREF and the +5 V and +12 V supplies. The circuitry includes a voltage reference generator, VREF low comparator, VCC reset comparator, +12 V reset comparator, write inhibit (VCC high) comparator, and associated logic.

Band-Gap Voltage (VBG)

The voltage reference circuit generates a precision voltage reference VBG at 1.20 V. From VBG it also generates $V_{RETRACT}$ (nominally 0.82 V), V_{IDLE} (nominally 0.1 V), and several other internal voltage and current references.

Positioner Reference Voltage (V5)

A precision 5 V reference voltage connected to and bypassed at VREF to serve as the reference voltage for the actuator predriver circuits.

External Reference Voltage (VBG2X)

Twice the bandgap voltage. It can be used as a reference by external circuitry.

Fault Detect

Both supplies are individually divided down by on-chip resistor dividers and then compared to VBG. The VCC low side monitor includes a resistor attenuator connected to VCCTH which permits the exact trip point to be externally adjusted if necessary. When a low voltage is detected on either supply or on VREF, $\overline{\text{FAULT}}$ is pulled low. This signal can be used to initiate a servo head retract.

The threshold voltage of the VCC reset comparator will be pulled to a lower value if CKHMARG is pulled low (see Table 2) while $\overline{\text{FAULT}}$ is high. This allows the VCC reset comparator to be effectively disabled during power supply margin testing.

WRITE INHIBIT

A write inhibit function is also provided. When the +5 V supply is either above or below its specified limits or the +12 V supply falls below its threshold, the internal $\overline{\text{WRINH}}$ signal is pulled low. If CKHMARG has just a bypass capacitor, it will be at the proper level to select $\overline{\text{WRINH}}$ as the function of the $\overline{\text{WRISAT}}$ pin.

$\overline{\text{WRISAT}}$ MUX

The $\overline{\text{WRISAT}}$ pin is multiplexed from the internal $\overline{\text{WRINH}}$ and $\overline{\text{SAT}}$ signals. Its output is controlled by the input level of the CKHMARG pin as shown in Table 2. If CKHMARG is toggled between GND and VCC, $\overline{\text{SAT}}$ always appears at the $\overline{\text{WRISAT}}$ output, while the margin function is enabled and disabled. If CKHMARG has just a bypass capacitor on it, $\overline{\text{WRINH}}$ appears at the $\overline{\text{WRISAT}}$ pin.

PWM INTERFACE BUFFERS

Two PWM interface buffers accept digital PWM signals. These signals are rebuffered to generate clean digital signals with amplitude of VREF referenced to ground.

DIGITAL INPUTS

All digital inputs are pulled to ground with a 20 kΩ (nominal) resistor to ensure a known state during system power failure.

TABLE 2: Margin and $\overline{\text{WRISAT}}$ Modes

CKHMARG INPUT LEVEL	MARGIN FUNCTION	$\overline{\text{WRISAT}}$ OUTPUT
0 V to 0.5 V	Enabled	$\overline{\text{SAT}}$
0.5 V to 3 V	Disabled	$\overline{\text{WRINH}}$
3 V to 6 V	Disabled	$\overline{\text{SAT}}$

PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output

SUPPLIES

NAME	TYPE	DESCRIPTION
GNDD GNDA	GROUND	ANALOG AND DIGITAL GROUNDS: These pins are internally connected.
VCC	POWER	THE 5 V SUPPLY
VP1 VP2	POWER	THE 12 V SUPPLY: Diode protected from V12. This is also the bridge supply for the spindle and actuator FETs. VP1 and VP2 are shorted together.

ACTUATOR

VREF	AI	ACTUATOR VOLTAGE REFERENCE: All actuator analog signals are referenced to this voltage. VREF is buffered to generate the internal VR reference. A bypass capacitor should be connected as close to this pin as possible.
ERR	AO	POSITION ERROR: The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3 - SE1 = 17(ERR - VR)
ERRM	AI	POSITION ERROR INVERTING INPUT: Inverting input to the loop compensation amplifier.
SOUT	AO	MOTOR CURRENT SENSE OUTPUT: This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT - VR = 4(SE2 - SE1)
SE2	AI	MOTOR CURRENT SENSE INPUT: Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	AI	MOTOR VOLTAGE SENSE INPUT: This input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point from ERR is: SE1 - VR = -8.5(ERR - VR)
SE1R	AI	ALTERNATE SE1 CONNECTION TO THE RETRACT AMPLIFIER: This input is selected during the “pulse” phase of retract. An external resistor divider connected to this pin programs the retract amplitude during the “pulse” phase.
RETRD	AI	DELAYED RETRACT: When this input decays below the trigger level for the “pulse” phase, the retract amplifier selects SE1R as the feedback instead of SE1. It also activates a pull-down resistor connected to the RETRD. When RETRD has decayed to 50% of the trigger level, the “pulse’” phase of retract is terminated.

ACTUATOR (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{RETR}}$	DI	RETRACT: Active low, this digital input must be asserted by external circuitry to force an actuator retract.
SE3	AI	MOTOR VOLTAGE SENSE INPUT: This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3 - VR = 8.5(ERR - VR)
OUTA, OUTC	AO	P-FET DRIVE: Drive signal for a P channel MOSFET connected between one side of the motor and VP.
OUTB, OUTD	AO	N-FET DRIVE: Drive signal for an N channel MOSFET connected between one side of the motor and GND. Crossover protection circuitry ensures that the P and N channel devices connected to the same side of the motor are never enabled simultaneously.
A3P	AI	NON-INVERTING A3 INPUT: Positive input to A3, the uncommitted opamp.
A3N	AI	INVERTING A3 INPUT: Negative input to A3, the uncommitted opamp.
A3	AO	A3 OUTPUT: The output of A3, the uncommitted opamp.

SPINDLE

P1, P2, P3	AO	P CHANNEL SPINDLE FET DRIVERS: These pins are connected to the three P channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	AO	N CHANNEL SPINDLE FET DRIVERS: These pins are connected to the three N channel power MOSFETs in the spindle motor power bridge.
VI	AI	SPINDLE CURRENT CONTROL VOLTAGE: Determines the peak amplitude of the spindle motor drive currents.
HIGHI	DI	HIGH CURRENT MODE: When high, causes 2.4 V at VI to force a peak current of 150 mV across the sense resistors. When low, the current is reduced 4x. This input has a 20 K (minimum) pull-down resistor.
RSLEW	C	OUTPUT SLEW RATE CONTROL: Peak current at POUT and NOUT is 100x the current in RSLEW. The RSLEW pin is biased at 1.2 V.
HYST	C (Optional)	HYSTERESIS CONTROL: Although HYST is internally biased, it can be overridden with external components to increase or decrease the amount of hysteresis in the PWM modulator.
ISENSE1, ISENSE2, ISENSE3	AI	SPINDLE CURRENT SENSE: Connects to the spindle current sense resistors. The motor current in each winding is calculated by subtracting that winding's PH from its ISENSE.
PH1, PH2, PH3	AI	SPINDLE MOTOR TERMINALS: These pins are used to calculate the phase error in the PLL. They are also used, in conjunction with ISENSE 1, 2, 3 to calculate winding current.

SPINDLE (continued)

NAME	TYPE	DESCRIPTION
SENSOR	DO	SENSOR OUTPUT: Multiplexes three internal signals: VCO, the VCO output; TACH, the PH2 and PH3 comparator; and PSNS, the position sense comparator output according to the spindle mode table.
RVCO	C	VCO RESISTOR: Sets the speed range of the VCO. The voltage at RVCO is forced to track RC.
CVCO	C	VCO CAPACITOR: Sets the speed range of the VCO.
RC	C	PLL LOOP FILTER: Sets the time constant for the PLL in run mode. In all other modes, it is connected to a DC voltage, VIDLE. VIDLE determines the VCO frequency at which the transition from start mode to run mode should occur. The host microprocessor commands this transition by lowering $\overline{\text{ENABLE}}$.
RPH	C	PHASE ERROR CURRENT SET: The pump current in the phase error amplifier is the sum of the VCO current (through RVCO) and the current through RPH.
$\overline{\text{ENABLE}}$, RESET	DI	MODE CONTROLS: These pins control the spindle modes according to the mode table. Both pins have internal 20 K (minimum) pull-down resistors.
$\overline{\text{DISPWR}}$	DI	DISABLE POWER: A logic zero on this input turns off the high and low sides of the spindle drivers. A brake command will override $\overline{\text{DISPWR}}$. An internal pull-down resistor guarantees a logic 0 when $\overline{\text{DISPWR}}$ floats.
ADVANCE	DI	COMMUTATION ADVANCE: A rising edge on this pin will cause the SILENTSPIN™ generator to advance one step whenever RESET is low. While high, ADVANCE prevents other commutation clocks from occurring. ADVANCE has an internal 20 K (minimum) pull-down resistor.
$\overline{\text{BRAKE}}$	DI	BRAKE: Active low, this input is pulled low by an external RC to perform a delayed brake. Note that when BRAKE is asserted, it sets a latch that is cleared in the preset mode.
CBRAKE	C	BRAKE CAPACITOR: A large capacitor is connected to CBRAKE to supply the charge necessary to turn on the external NMOS power devices during brake.

PWM INTERFACE BUFFERS

IM,IL	DI	IM AND IL: The PWM inputs for the most significant and least significant portions of the PWM information. Note that the input logic levels are dependent on VREF.
RM,RL	DO	RM AND RL: The buffered PWM outputs for the most significant and least significant portions of the PWM information. Their peak to peak swing is VREF.

VOLTAGE REFERENCE AND FAULT DETECT

NAME	TYPE	DESCRIPTION
V12	AI	SYSTEM +12 V SUPPLY: The upper side connection of the resistor divider for +12 V reset comparator.
V12CHK	AI	+12 V RESET COMPARATOR INPUT: The input to the +12 V reset comparator and the connection to a bypass capacitor. V12 is divided down at this pin by an on-chip resistor divider and then compared to VBG. If V12CHK falls below VBG, $\overline{\text{FAULT}}$ and $\overline{\text{WRINH}}$ are asserted.
VCCHKL	AI	VCC RESET COMPARATOR INPUT: The input to the VCC reset comparator and the connection to a bypass capacitor. VCC is divided down at this pin by an on-chip resistor divider and then compared to VBG. If VCCHKL falls below VBG, $\overline{\text{FAULT}}$ and $\overline{\text{WRINH}}$ are asserted.
VCCTH	C	VCC RESISTOR DIVIDER: Normally left open. The VCCHKL trip point can be adjusted by connecting an external resistor to this pin.
CKHMARG	AI	COMBINED VCCHKH AND $\overline{\text{MARGIN}}$ INPUT: Multiple level input as shown in Table 2. The input to the write inhibit comparator and the connection to a bypass capacitor. VCC is divided down at this pin by an on-chip resistor divider and then compared to VBG. If CKHMARG exceeds VBG, $\overline{\text{WRINH}}$ will be pulled low. The CKHMARG level also controls the MARGIN function and the $\overline{\text{WRISAT}}$ output
VBG	AO	BANDGAP OUTPUT TEST POINT: A voltage reference output at 1.2 V. It is used internally as a reference voltage.
V5	C	5V REFERENCE OUTPUT: Connected to VREF for use as a reference voltage for the actuator predriver circuitry.
VBG2X	AO	EXTERNAL REFERENCE OUTPUT: Available for use as a reference by external circuitry.
IBR	C	BIAS RESISTOR: This resistor sets the internal bias currents of the analog circuitry.
$\overline{\text{FAULT}}$	DO	POWER FAULT: Active low, this open-collector output is asserted when a low condition is detected on either VREF or 5 V or 12 V. An internal 10 K pull-up resistor connects $\overline{\text{FAULT}}$ to VCC.
$\overline{\text{WRISAT}}$	DO	WRITE INHIBIT OR SATURATION DETECT: Active low, with an on-chip 10 kΩ pull-up resistor. Function is selected according to Table 2. $\overline{\text{WRINH}}$ is asserted when a low voltage condition is detected on VREF or the +5 V or +12 V supplies or an excessive voltage condition is detected on +5 V supply. $\overline{\text{SAT}}$ is asserted when the error amplifier (A1) has saturated and ERR is no longer proportional to the VCM voltage.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage may occur.)

PARAMETER	RATING
VP	0 to 14 V
VCC	0 to 7 V
IM, IL, RM, RL, IBR, V5, RVCO, CVCO, RC, RPH, HYST, RSLEW, VI, VREF, VBG, V12CHK, VBG2X, VCCHKL	0 to 6 V
CBRAKE, V12, N1, N2, N3, $\overline{\text{BRAKE}}$	0 to 15 V
PH1, PH2, PH3, ISENSE1, ISENSE2, ISENSE3, SE1, SE2, SE3, SE1R	-2 to VP +2
CKHMARG, VCCTH, $\overline{\text{RETR}}$, $\overline{\text{DISPWR}}$, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{FAULT}}$, SENSOR, HIGHI, $\overline{\text{WRISAT}}$	0 to 7
Voltage of ISENSEX with respect to PHX (ISENSEX - PHX)	2 V
All other pins	0 to VP
Storage temperature	-45 to 165° C
Solder temperature - 10 second duration	260° C

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VP	Normal Mode	9	11.6	13.2	V
	Retract Mode	4		14	V
VCC		4.5	5	5.5	V
VBG Capacitor			0.1		µF
VBG2X Capacitor			1		µF
VREF		4.75		5.25	V
IBR Resistor		11.8	12	12.2	kΩ
RVCO Resistor		24	25	26	kΩ
V5 Capacitor			1		µF
RSLEW Resistor		12			kΩ
VI		0		2.5	V
Operating Temperature		0		70	°C

DC CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VP Current				40	mA
VCC Current				2.0	mA
V12 Current				0.2	mA
VREF Current	RM = RL = Open			0.1	mA

A1, LOOP COMPENSATION AMPLIFIER

Input Bias Current				100	nA
Input Offset Voltage				±10	mV
Voltage Swing	wrt VREF	±1			V
Load Resistance	wrt VREF	10			kΩ
Load Capacitance				100	pF
Gain		60			dB
Unity Gain Bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB
Retract Switch Resistance, ERR with respect to ERRM	Retract Mode, VP > 9 V			2	kΩ

A2, CURRENT SENSE AMPLIFIER

Input Impedance	SE1	SE2 = VREF	2.6	5.5		kΩ
	SE2	SE1 = VREF	3.2	7.0		kΩ
Input Offset Voltage		SE1 = SE2 = VREF			3	mV
Output Voltage Swing		R_L = 20 K to VREF				
V_{OH}, wrt VREF		Vp ≥ 10.3 V	3			V
V_{OL}, wrt VREF		R_L = 20 K to VREF Vp ≥ 10.3 V			-3	V
Common Mode Range			-0.2		VP +0.2	V
Load Capacitance					100	pF
Output Impedance					25	Ω
Gain (SOUT - VREF) / (SE1 - SE2)		No DC Load	3.9	4	4.1	V/V
Unity Gain Bandwidth			0.5			MHz
CMRR			55			dB
PSRR			60			dB

ELECTRICAL SPECIFICATIONS (continued)

A3 AMPLIFIER

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Bias Current					100	nA
Input Offset Voltage					±10	mV
Voltage Swing	V_{OL}				1.4	V
	V_{OH}, wrt VP		- 3			V
Common Mode Range	V_{IL}				2.5	V
	V_{IH}, wrt VP		- 3			V
Load Resistance		to VREF	10			kΩ
Load Capacitance					100	pF
Gain			60			dB
Unity Gain Bandwidth			500			kHz
CMRR			60			dB
PSRR			60			dB

SATURATION DETECT

$\overline{SAT}$ Threshold	(|ERR-VR|)		0.8	0.9	1	V
Hysteresis				20		mA

PWM BUFFERS

ROUT	Pch				25	Ω
	Nch				25	Ω

ACTUATOR MOSFET DRIVERS

SE3 Input Impedance	to VREF	10	25		kΩ
OUTA, OUTC Voltage Swing	|IOUT| < 1 mA	1.5		VP -1	V
OUTB, OUTD Voltage Swing	|IOUT| < 1 mA	1		VP -1.5	V
VTH, Crossover Separation Threshold				1.6	V
Slew Rate, OUTA..D	CL ≤ 1000 pF	0.5			V/µs
Crossover Time	±300 mV step at ERR CL ≤ 1000 pF			5	µs
Output Impedance, OUTA..D			200		kΩ
Transconductance I(OUTA..D) / (ERR-VREF)			8		mA/V
Gain (SE3 - SE1) (ERR - VREF)		16	17.5	19	V/V

RETRACT CIRCUIT

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Retract Voltage, $V_{RETRACT}$	VP > 5 V, Level 1	0.7	0.82	1	V
RETRD Discharge Resistor	VP > 5 V, Level 2	22	32	42	kΩ
RETRD Trigger Voltages VT 1: level 1 to level 2	VP > 5 V, Level 1	0.75	0.85	0.95	V
VT 2: level 2 to float % of VT1	VP > 5 V, Level 2	45	50	55	%
RETRD Input Bias Current	Level 1			100	nA
SE1R Input Bias Current				100	nA

VCO (Unless otherwise specified, CVCO = 0.001 µF, RVCO = 25 kΩ)

Typical Frequency		$\frac{V_{RC}}{4 \bullet R_{VCO} \bullet C_{VCO}}$			Hz
Run Frequency	RC = 2 V	30.25	23.0	25.75	kHz
Idle Frequency	Mode = Reset	700	1100	1500	Hz
Reset Phase Error	RC = V_{IDLE}			18	°

TACH COMPARATOR

SENSOR Rising Edge Threshold	PH3 - PH2	30	100	170	mV
SENSOR Falling Edge Threshold	PH2 - PH3	30	100	170	mV

PHASE ERROR AMPLIFIER (unless otherwise specified, RVCO = 25 kΩ, RPH = not used)

V_{RC} (VIDLE)	Mode = Reset		100		mV
Typical Pump Current		$\left(\frac{V_{RC}}{R_{VCO}} + \frac{V_{RPH}}{R_{PH}}\right) + 3\,\mu$			A
Pump Current at RC Start Mode	V_{RC} = VIDLE, $R_{RPH} = \infty$		4.5		µA
Run Mode, at Speed	V_{RC} = 2 V		82		µA
Source/Sink Current Mismatch	V_{RC} = 2 V			5	%

PHASE ERROR AMPLIFIER (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
PH1 Input Offset	State B	PH2 = VP, PH3 = 0	-100		100	mV
	State E	PH2 = 0, PH3 = VP	-100		100	mV
PH2 Input Offset	State A	PH1 = VP, PH3 = 0	-100		100	mV
	State D	PH1 = 0, PH3 = VP	-100		100	mV
PH3 Input Offset	State F	PH1 = VP, PH2 = 0	-100		100	mV
	State C	PH1 = 0, PH2 = VP	-100		100	mV
RPH Voltage		R_{RPH} = 240 kΩ	2.1	2.4	2.7	V

BRAKING CIRCUIT

$\overline{\text{BRAKE}}$ Threshold	VP ≥ 4 V	1.0	1.2	1.4	V
$\overline{\text{BRAKE}}$ VP Threshold	$\overline{\text{BRAKE}}$ = 1.5 V			3.8	V
$\overline{\text{BRAKE}}$ Bias Current	$\overline{\text{BRAKE}}$ = 4.5 V			0.1	µA
CBRAKE Current-Run	Run Mode CBRAKE = VP			2	µA
CBRAKE Current-Brake	Brake Mode, VP = 0 CBRAKE = 10 V			0.2	µA

VREF MONITOR

VREF Fail Threshold	VREF Falling	1.4	1.55	1.7	V
Hysteresis			85		mV

VCC RESET COMPARATOR

Trip Voltage, Regular Mode	VCCTH = VCCHKL	4.22	4.35	4.48	V
(VCC Falling CKHMARG > 0.5 V)	VCCTH = 0	4.60	4.74	4.88	V
	VCCTH = VCC	3.46	3.57	3.68	V
Trip Voltage Reduction (VCC Falling, CKHMARG < 0.5 V)		10	14	18	%
Hysteresis		30	45	60	mV
Input Resistance at VCCTH		90	140	280	kΩ

VCC WRITE INHIBIT COMPARATOR

Trip Voltage	VCC Rising, 0.5 V < CKHMARG < 3 V	5.59	5.82	6.05	V
Hysteresis		50	80	120	mV
Input Resistance at CKHMARG			13		kΩ

+12V RESET COMPARATOR

PARAMETER	CONDITON	MIN	NOM	MAX	UNIT
Trip Voltage	V12 Falling	9.12	9.50	9.88	V
Hysteresis		50	70	100	mV
Input Resistance at V12CHK			14		kΩ

CKHMARG LEVEL DETECTOR

Transition Voltage, VLD1		0.46	0.5	0.54	V
Transition Voltage, VLD2		2.8	3.0	3.2	V

DIGITAL INPUTS (DISPWR, ADVANCE, RESET, ENABLE, RETR, HIGHI)

Input Voltage					
V_{IL}		0.8			V
V_{IH}				2	V
Input Bias Current				200	µA
Open Circut Voltage				0.4	V

PWM BUFFER INPUTS (IM, IL)

Input Voltage	VREF = 5 V				
V_{IL}		0.8			V
V_{IH}				4.2	V
Input Bias Current				100	nA

DIGITAL OUTPUT (SENSOR)

Output Voltage					
V_{OL}	I_{SINK} = 1 mA			0.4	V
V_{OH}, wrt VCC	I_{SOURCE} = 1 mA	-1			V

DIGITAL OUTPUT ($\overline{\text{FAULT}}$)

Output Voltage					
V_{OL}	I_{SINK} = 5 mA			0.4	V
V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-2	-1		V

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL OUTPUT ($\overline{\text{WRISAT}}$)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Output Voltage						
	V_{OL}	I_{SINK} = 1 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-2	-1		V

VBG OUTPUT

Output Voltage	No DC Load		1.20		V
Load Capacitance			0.1	0.2	µF

VBG2X

Output Voltage	No Load	2.25		2.50	V
Output Impedance	$I_{SOURCE} \leq$ 1 mA $I_{SINK} \leq$ 0.1 mA			30	Ω

V5 OUTPUT

Output Voltage	No DC Load	4.8	5	5.3	V
Load Capacitance			1	2	µF

NMOS MOTOR DRIVER OUTPUTS (N1, N2, N3)

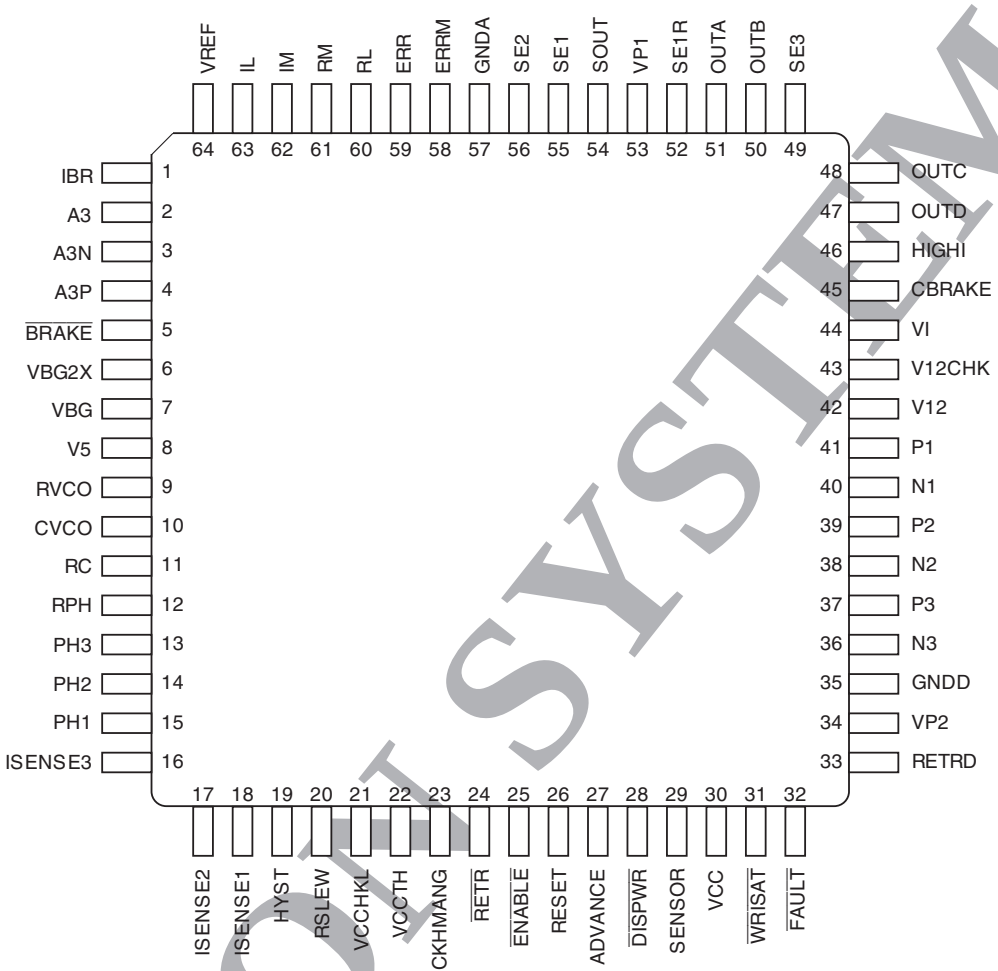
Source Current	VOUT = VP/2, RSLEW = 24 K		5		mA
Sink Current	VOUT = VP/2, RSLEW = 24 K		5		mA
Output High On Voltage	RSLEW = 24 K, I_{OH} = 1 mA	-2.0	-1.0	TBD	V
Output Low On Voltage	I_{OL} = 1 mA			0.5	V

PMOS MOTOR DRIVER OUTPUTS (P1, P2, P3)

Source Current	VOUT = VP/2, R_{SLEW} = 24 K		5		mA
Sink Current	VOUT = VP/2, R_{SLEW} = 24 K		5		mA
Output High On Voltage	I_{OH} = 1 mA	-0.5			V
Output Low On Voltage	R_{SLEW} = 24 K, I_{OL} = 1 mA			0.5	V

PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32H6829/6829A
Servo and Spindle Predriver

March 1997

DESCRIPTION

The SSI 32H6829 Servo and Spindle Predriver, a CMOS monolithic integrated circuit housed in a 64-lead TQFP package operates from +5 V and +12 V supplies. It is designed to drive a voice coil actuator and a 3-phase, Hall-sensorless motor with external power MOSFETs. The device is intended for use in 12 V disk drive applications.

The actuator driver includes a saturation detector to monitor the loop compensation amplifier for saturation, an uncommitted opamp for input signal conditioning, a voltage reference to provide a precise voltage level for internal PWM buffers, and reduced power dissipation.

The spindle driver includes a µP controlled startup ramp to replace the imprecise analog ramp, an external PWM input to allow PWM frequencies above the audible range, active pullup on the P driver, adjustable N-channel slew rate, and improved spindle brake performance.

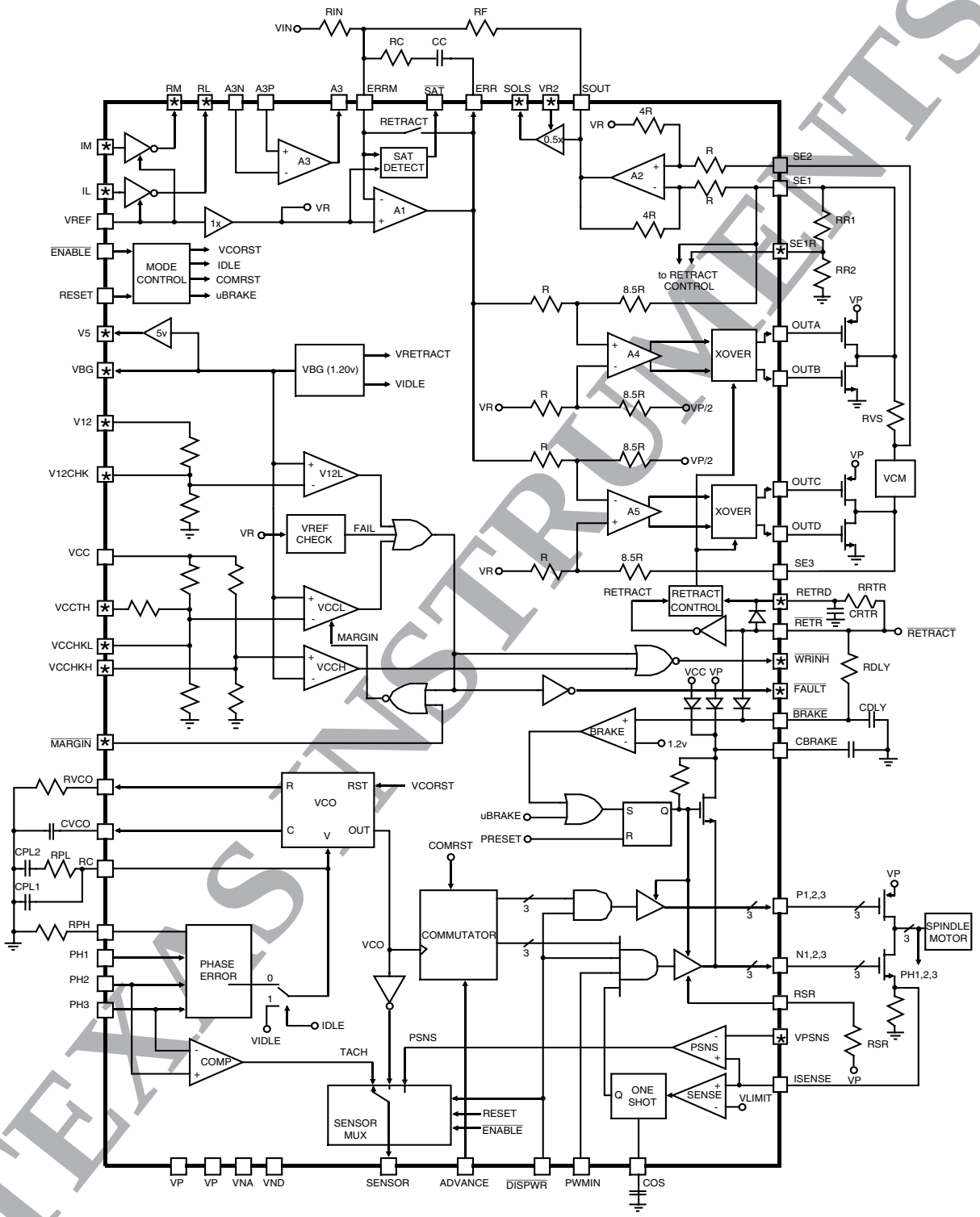
A precision low voltage monitor circuit is also added to monitor +5 V and +12 V supplies and to initiate servo head retracts during voltage faults.

The SSI 32H6829A is the SSI 32H6829 housed in a 48-lead TQFP package intended to be a drop-in, pin-for-pin replacement for the SSI 32H6825. As such the SSI 32H6829A does not implement the following functions of the SSI 32H6829: Voltage Reference, Voltage Fault, PWM Buffers, PSNS Comparator, and Dual Level Retract. Also, the 6825 $\overline{\text{WRPROT}}$ function is replaced with the similar but more useful $\overline{\text{SAT}}$ function.

FEATURES

- **Small footprint 64- or 48-lead TQFP package**
- **Spindle driver is PWM during run and start**
- **Commutator is driven by a phase lock loop for high jitter immunity**
- **Adjustable slew rate to minimize stress in the power MOSFETs**
- **Microprocessor controlled spindle startup**
- **Saturation detector to monitor loop compensation amplifier status**
- **Precision low voltage monitor circuitry for both +5 V and +12 V supplies, 32H6829 only**
- **Dual level retract scheme includes adjustable pulse mode, 32H6829 only**

BLOCK DIAGRAM



* Pins not available on SSi 32H6829A, SSi 32H6829 functions only.

FUNCTIONAL DESCRIPTION

The SSI 32H6829 contains an actuator predriver with PWM interface, a spindle predriver with PLL commutator, and a low voltage monitor circuit.

ACTUATOR PREDRIVER

The actuator predriver serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration. It has two modes of operation, normal (linear) and retract. The retract mode is activated by an external command at $\overline{\text{RETR}}$. Otherwise, the device operates in linear mode. It consists of a 5 V reference, A1 through A5, a saturation detector, and XOVER blocks. It is functionally similar to the 32H6825.

Positioner PWM Interface

The 5 V voltage reference provides a precision and stable voltage source for two on-chip PWM buffers and therefore eliminates logic swing uncertainty of PWM signals. The PWM buffer outputs are then filtered by an external RC low pass network constructed with the on-chip uncommitted opamp to generate an analog input.

Loop Compensation Amplifier

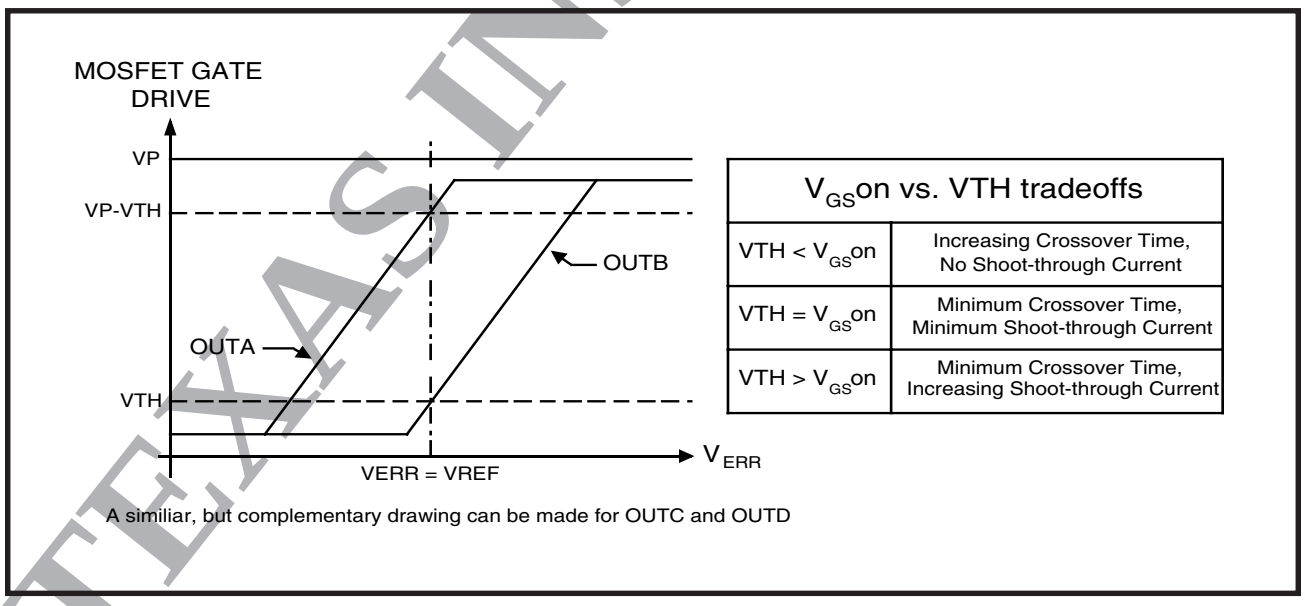
During linear operation, the acceleration signal is applied through amplifier A1. RC components may be used to provide loop compensation at this stage. The saturation detector monitors amplifier A1 and indicates when saturation is detected.

MOSFET Drivers

ERR, the output signal of A1, drives two precision amplifiers, each with a gain of 8.5. The first of these two amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed similarly from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a current sense resistor are connected in series between SE1 and SE3.

Crossover Protection Blocks

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold VTH, illustrated below, is the maximum drive on any MOSFET gate when the motor current changes sign.



V_{GS}on vs. VTH tradeoffs	
VTH < V_{GS}on	Increasing Crossover Time, No Shoot-through Current
VTH = V_{GS}on	Minimum Crossover Time, Minimum Shoot-through Current
VTH > V_{GS}on	Minimum Crossover Time, Increasing Shoot-through Current

FIGURE 1: Crossover Protection

ACTUATOR PREDRIVER (continued)

Retract Function

The 6829 incorporates a dual level retract scheme. When retract is initiated, a fixed voltage (level 1) is applied across the actuator to force a constant retract velocity. After an externally adjustable amount of time, a higher voltage (level 2) is briefly applied to the actuator. At the end of level 2, the actuator is floated (i.e., zero current).

The timing and amplitude of the level 2 phase can be adjusted with external components. RRTR, CRTR, and an internal discharge resistor which is activated during level 2 control the retract timing. When $\overline{\text{RETR}}$ is first lowered, RRTR discharges CRTR until the RETRD pin reaches the level 2 trigger threshold (nominally 0.85 V). At this time, the level 2 retract amplitude is applied to the actuator and the internal discharge resistor (nominally 32k) quickly discharges CRTR. When CRTR has been discharged to half of the trigger voltage all retract current is turned off and the actuator is floated. The level 1 retract amplitude is internally fixed (0.85 V nominal). During level 2, SE1R is fed back to the retract amplifier instead of SE1. Thus the level 2 amplitude will be increased by the factor (1 + RR1 / RR2).

A second external RC delay is used between $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ to program the brake delay and ensure the actuator has enough time to retract before the spindle is braked.

Current Sense Amplifier

Actuator current is sensed by a small series resistor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired current and the actual motor current. SOUT, referenced to VREF, is also connected to a level-shifter to generate SOLS, which is referenced to VR2.

PWM Inverters

Two PWM inverters powered from VREF are provided to generate power supply insensitive square waves from two pulse width modulation digital data streams. The two outputs may be weighted and summed into a low pass filter constructed with A3. To facilitate bonding to a 48-lead package, IL is pulled to ground with a 100k resistor. When the inverters are not used, IL may be floated, but IM must be tied to either ground or VREF.

SPINDLE PREDRIVER

The spindle driver section monitors spindle back-emf and generates drive signals to 3 MOSFET power bridges. It includes current limit, a back EMF monitoring circuit to determine optimal commutation points, a phase locked loop to properly phase the commutation times, and a delayed spindle brake circuit.

Commutator

The commutator drives the spindle motor windings in proper sequence to operate a 3-phase spindle motor. In run mode, the commutator is clocked by the VCO output. In start mode, the commutator is clocked by external pulses applied at the ADVANCE pin. The table below shows the commutator sequence and identifies which power FETs are on.

TABLE 1: Commutation Sequence

STATE	N1	N2	N3	P1	P2	P3
Reset	Off	On	Off	On	Off	On
A	Off	Off	On	On	Off	Off
B	Off	Off	On	Off	On	Off
C	On	Off	Off	Off	On	Off
D	On	Off	Off	Off	Off	On
E	Off	On	Off	Off	Off	On
F	Off	On	Off	On	Off	Off

Phase Error Amplifier

The phase error circuit compares the undriven winding voltage with the average of the winding voltages. Depending on the result of the comparison and the state of the commutator, a positive or negative current is applied to the RC pin. The table below shows which winding is undriven and the polarity of the output current when that winding is positive with respect to the average.

The phase error circuit is only used during run and coast modes. In all other modes, RC is forced to V_{IDLE}, an internally generated voltage that will cause the VCO to idle at approximately 1/20 of the run rate.

The magnitude of the current at RC is the sum of a constant current and a current proportional to the VCO frequency. The constant current value is set by RPH which is biased to 2.4 V nominally. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on CVCO is nominally 2 V. The frequency formula is:

$$F_{VCO} = \frac{V_{RC}}{8.0\ R_{VCO}\ C_{VCO}}$$

The VCO will be reset whenever $\overline{ENABLE}$ = High and RESET = Low. During VCO reset, the VCO output is forced low. The first VCO clock will occur immediately after the VCO exits reset. This timing relationship is shown in Figure 2.

One Shot

The one shot is triggered whenever ISENSE exceeds VLIMIT. When the one shot times out, it will remain high if ISENSE is still above VLIMIT. During the time the one shot output is high, the N drivers are turned off. This behavior implements PWM over-current limit, where the peak current is VLIMIT/R_{MS}.

TABLE 2: Undriven Winding and Polarity

COMMUTATOR	UNDRIVEN WINDING	POLARITY
A	PH2	Source
B	PH1	Sink
C	PH3	Source
D	PH2	Sink
E	PH1	Source
F	PH3	Sink

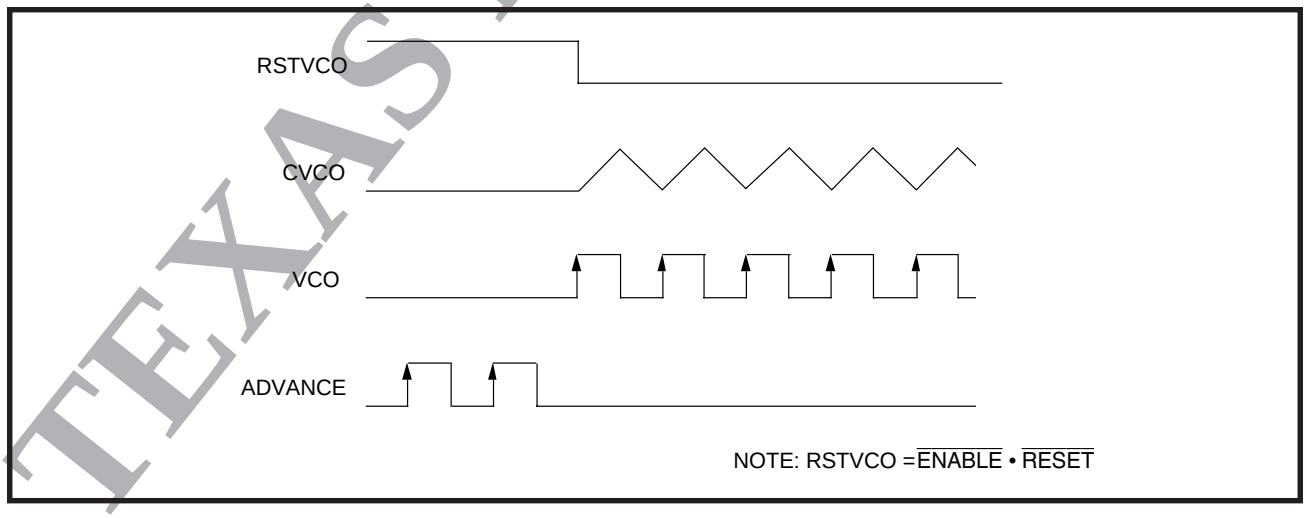


FIGURE 2: VCO Timing Diagram

SPINDLE PREDRIVER (continued)

NOUT and POUT

The NOUT drivers drive the gates of the N channel power FETs. They have an adjustable source current set by an external resistor at RSR. In brake mode, the NOUT drivers are disabled and all N channel power FETs are turned on. The POUT drivers drive the P channel power FETs. The POUT drivers are deactivated during brake but not during each PWM cycle.

Spindle Modes of Operation

The spindle driver modes of operation are governed by the RESET, $\overline{\text{ENABLE}}$, and $\overline{\text{DISPWR}}$ inputs according to Table 3. The brake mode, whether activated by $\overline{\text{ENABLE}}$ and RESET or by a power failure is internally latched and can only be turned off by asserting the preset mode.

LOW VOLTAGE MONITOR

Precision low voltage monitor circuitry is included to monitor VREF and both supplies, +5 V and +12 V. The circuitry includes a precision voltage reference generator, VCC reset comparator, +12 V reset comparator, write inhibit comparator, and associated logic.

The voltage reference circuit generates a precision voltage reference VBG at 1.2 V. From VBG, it also generates, $V_{RETRACT}$ (nominally 0.82 V), V_{IDLE} (nominally 0.1 V), VLIMIT (nominally 0.1 V), and several other internal voltage and current references.

Both supplies are individually divided down by on-chip resistor dividers and then compared to VBG. The VCC low side monitor includes a resistor attenuator connected to VCCTH which permits the exact trip point to be externally adjusted if necessary. When a low voltage is detected on either supply, $\overline{\text{FAULT}}$ is pulled low. The threshold voltage of VCC reset comparator will be pulled to a lower value if $\overline{\text{MARGIN}}$ is asserted while $\overline{\text{FAULT}}$ is high. This allows the VCC reset comparator to be effectively disabled during power supply margin testing.

A write inhibit function is also provided by the low voltage monitor circuitry. When +5 V supply is out of its specified limits or +12 V supply falls below its threshold, WRINH is pulled low.

DIGITAL INPUTS

To ensure a known state during system power failure, the digital inputs at $\overline{\text{DISPWR}}$, PWMIN, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{RETR}}$ are pulled to ground with a 20 kΩ (minimum) resistor, while the digital input at $\overline{\text{MARGIN}}$ is pulled to VCC with a 20 kΩ (minimum) resistor.

TABLE 3: Spindle Modes of Operation

RESET	$\overline{\text{ENABLE}}$	$\overline{\text{DISPWR}}$	MODE	SENSOR	RC	VCO	COMMUTATOR
1	1	X	Preset	$\overline{\text{VCO}}$	V_{IDLE}	Idle	Reset
0	1	X	Start	PSNS	V_{IDLE}	Reset	Run
0	0	1	Run	$\overline{\text{VCO}}$	Run	Run	Run
0	0	0	Coast	TACH	Run	Run	Run
1	0	X	Brake	$\overline{\text{VCO}}$	V_{IDLE}	Idle	Reset

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VND, VNA	Ground	Digital and Analog Grounds. They are shorted externally.
VCC	Supply	System 5 V power supply. Used by digital I/O circuits.
VP	Supply	The 12 V supply, diode protected from system 12 V. This is also the bridge supply for the spindle and actuator MOSFETs.

ACTUATOR PREDRIVER

VREF	Input (A)	ACTUATOR VOLTAGE REFERENCE: all actuator analog signals are referenced to this voltage, except SOLS.
ERRM	Input (A)	POSITION ERROR INVERTING INPUT: inverting input to the loop compensation amplifier.
ERR	Output (A)	POSITION ERROR: the loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3-SE1 = 17(ERR-VREF)
SOUT	Output (A)	MOTOR CURRENT SENSE OUTPUT: this output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF = 4(SE2-SE1)
SOLS	Output (A)	MOTOR CURRENT SENSE OUTPUT: this output provides a voltage equal to one half of SOUT and is referenced to VR2. SOLS-VR2 = 0.5(SOUT-VREF)
VR2	Input (A)	VOLTAGE REFERENCE: The reference for SOLS.
$\overline{\text{SAT}}$	Output (D)	SATURATION DETECT OUTPUT: active low, with an on-chip 10 kΩ pullup resistor. It is asserted when the current flowing through the summing node at ERRM exceeds the saturation detector limits.
SE2	Input (A)	MOTOR CURRENT SENSE INPUT: non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	Input (A)	MOTOR VOLTAGE SENSE INPUT: this input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor that is in series with the motor. The gain to this point from ERR is: SE1-VREF = -8.5(ERR-VREF)

ACTUATOR PREDRIVER (continued)

NAME	TYPE	DESCRIPTION
SE3	Input (A)	MOTOR VOLTAGE SENSE INPUT: this input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3-VREF = 8.5(ERR-VREF)
OUTA, OUTC	Output (A)	P-FET DRIVE: drive signal for a P-channel MOSFET connected between one side of the motor and VP.
OUTB, OUTD	Output (A)	N-FET DRIVE: drive signal for an N-channel MOSFET connected between one side of the motor and ground. Crossover protection circuitry ensures that the P- and N- channel devices connected to the same side of the motor are never enabled simultaneously.
V5	Output (A)	5 V REFERENCE OUTPUT: the output of the 5 V voltage reference.
RM, RL	Output (A)	PWM INVERTER OUTPUTS:these pins are connected to an external low pass filter network to generate the analog positioner input.
IM, IL	Input (D)	PWM INVERTER INPUTS: these pins are driven by PWM digital waveforms. IL is pulled down with an internal 100 k resistor. IM must not float, if unused it should be tied to VREF or GND.
A3P	Input (A)	NON-INVERTING A3 INPUT: positive input to A3, the uncommitted opamp.
A3N	Input (A)	INVERTING A3 INPUT: negative input to A3, the uncommitted opamp.
A3	Output (A)	A3 OUTPUT: the output of A3, the uncommitted opamp.

SPINDLE PREDRIVER

P1, P2, P3	Output (A)	P-CHANNEL SPINDLE FET DRIVERS:these pins are connected to the three P-channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	Output (A)	N-CHANNEL SPINDLE FET DRIVERS: these pins are connected to the three N-channel power MOSFETs in the spindle motor power bridge.
RSR	Component	SOURCE CURRENT LIMIT: an external resistor is connected between this pin and VP to set 1/20 of the peak current at N1,N2,N3.
ISENSE	Input (A)	SPINDLE CURRENT SENSE: connects to the high side of the spindle current sense resistor RMS.
VPSNS	Input (A)	SENSE COMPARATOR INPUT: the input to the Sense comparator. The comparator output is asserted when ISENSE exceeds VPSNS.
COS	Component	ONE SHOT CAPACITOR: sets the time delay in the one shot. The one shot is clocked whenever the current in the spindle exceeds a limit controlled by RMS.

SPINDLE PREDRIVER (continued)

NAME	TYPE	DESCRIPTION
PWMIN	Input (D)	PULSE WIDTH MODULATION INPUT: modulates the N-channel power MOSFETs to control spindle motor current. When low, the NMOSFETs are turned off.
$\overline{\text{DISPWR}}$	Input (D)	DISABLE POWER: active low, this input turns off the high and low sides of the spindle drivers. A brake command will over-ride $\overline{\text{DISPWR}}$. An internal pulldown resistor guarantees a logic low when $\overline{\text{DISPWR}}$ floats.
ADVANCE	Input (D)	COMMUTATION ADVANCE: a rising edge on this pin will cause the commutator to advance whenever RESET is low. While high, ADVANCE prevents other commutation clocks from occurring.
SENSOR	Output (D)	DIGITAL MUX OUTPUT: a totem pole output, which is multiplexed from the VCO output, the TACH comparator output and the sense comparator output according to Table 3.
RVCO	Component	VCO RESISTOR: sets the speed range of the VCO. The voltage at RVCO is forced to track RC.
CVCO	Component	VCO CAPACITOR: sets the speed range of the VCO.
RC	Component	PLL LOOP FILTER: sets the time constant for the PLL in run mode. In all other modes, it is connected to a DC voltage, V_{IDLE}. V_{IDLE} determines the VCO frequency at which crossover from Start to Run should occur (by lowering $\overline{\text{ENABLE}}$).
RPH	Component	PHASE ERROR CURRENT SET: the pump current in the phase error amplifier is the sum of the VCO current (through RVCO) and the current through RPH.
PH1, PH2, PH3	Input (A)	SPINDLE MOTOR TERMINALS: these pins are used to detect the phase error in the PLL.

LOW VOLTAGE MONITOR AND RETRACT

$\overline{\text{ENABLE}}$, RESET	Input (D)	MODE CONTROLS: these inputs control the spindle modes of operation according to Table 3.
VBG	Output (A)	BANDGAP VOLTAGE OUTPUT: a voltage reference output at 1.2 V. It is used internally as a reference voltage in the low voltage monitor circuitry.
VCCHKH	Input (A)	WRITE INHIBIT COMPARATOR INPUT: the input to the write inhibit comparator and the connection to a bypass capacitor. VCC is divided down at this pin by an on-chip resistor divider and then compared to VBG. If VCCHKH exceeds VBG, $\overline{\text{WRINH}}$ will be pulled low.
V12	Input (A)	SYSTEM +12 V SUPPLY: the upper side connection of the resistor divider for +12 V reset comparator.
V12CHK	Input (A)	+12 V RESET COMPARATOR INPUT: the input to the +12 V reset comparator and the connection to a bypass capacitor. V12 is divided down at this pin by an on-chip resistor divider and then compared to VBG. If V12CHK falls below VBG, $\overline{\text{FAULT}}$ and $\overline{\text{WRINH}}$ are asserted.
VCCTH	Component	VCC RESISTOR DIVIDER OUTPUT: the VCCHKL trip point can be adjusted by connecting an external VCC resistor divider to this pin.

LOW VOLTAGE MONITOR AND RETRACT (continued)

NAME	TYPE	DESCRIPTION
VCCHKL	Input (A)	VCC RESET COMPARATOR INPUT: the input to the VCC reset comparator and the connection to a bypass capacitor. If VCCHKL falls below VBG, $\overline{\text{FAULT}}$ and $\overline{\text{WRINH}}$ are asserted.
$\overline{\text{MARGIN}}$	Input (D)	MARGIN CONTROL INPUT: sets the threshold voltage of VCC reset comparator. It is set high by an internal pullup resistor under normal operation. If it is asserted low externally while $\overline{\text{FAULT}}$ is high, the threshold voltage of the comparator will be lowered.
$\overline{\text{FAULT}}$	Output (D)	POWER FAULT: active low, with an on-chip 10 kΩ pullup resistor. It is asserted when a low voltage condition is detected on either VREF, +5 V, or +12 V supply.
$\overline{\text{WRINH}}$	Output (D)	WRITE INHIBIT: active low, with an on-chip 10 kΩ pullup resistor. It is asserted when a low voltage condition is detected on either +5 V or +12 V supply or an excessive voltage condition is detected on +5 V supply.
SE1R	Input (A)	ALTERNATE SE1 CONNECTION TO THE RETRACT AMPLIFIER: this input is selected during the level 2 phase of retract. An external resistor divider connected to this pin programs the retract amplitude during the level 2 phase.
RETRD	Input (A)	DELAYED $\overline{\text{RETR}}$: when this input decays below the trigger level for level 2, the retract amplifier selects SE1R as the feedback instead of SE1. It also activates a pull down resistor connected to RETRD. When RETRD has decayed to 50% of the trigger level, the level 2 phase of retract is terminated.
$\overline{\text{RETR}}$	Input (D)	RETRACT: active low, this digital input must be asserted by external circuitry to force an actuator retract.
$\overline{\text{BRAKE}}$	Input (A)	BRAKE: active low, this input must be pulled low by external circuitry to perform a delayed brake.
CBRAKE	Component	BRAKE CAPACITOR: a large capacitor is connected to CBRAKE to provide pullup to the N-channel spindle MOSFETs during brake.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING
VP	0 to 14 V
VCC	0 to 7 V
IM, IL, RM, RL, V5, RVCO, CVCO, RC, RPH, PSNS, ISENSE, VREF, V12CHK	0 to 6 V
N1, N2, N3, CBRAKE, V12	0 to 15 V
PH1, PH2, PH3, SE1, SE1R, SE2, SE3	-2 to VP+2
$\overline{\text{RETR}}$, $\overline{\text{DISPWR}}$, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{FAULT}}$, SENSOR, $\overline{\text{WRINH}}$, PWMIN, $\overline{\text{SAT}}$, $\overline{\text{BRAKE}}$	0 to 7 V
All other pins	0 to VP
Storage temperature	-45 to 165° C
Solder temperature - 10 sec duration	260° C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VP	Normal Mode	9	12	13.2	V
	Retract/Brake Mode	3.5		14	V
VCC		4.5	5	5.5	V
VREF		4.5	5	5.2	V
VR2		2	2.49	3	V
Ambient temperature				70	°C
V_{RC} Dynamic Range			2	3	V
RVCO		11.8	12	12.2	kΩ

DC CHARACTERISTICS

VP current				40	mA
VCC current				2.5	mA
V12 current				2	mA
VR2 current	VR2 = 2.493 V SOUT = 2.5 V wrt VREF			0.5	mA
VREF current	SE2 = VREF			0.1	mA

ELECTRICAL SPECIFICATIONS (continued)

ACTUATOR PREDRIVER

A1, Loop Compensation Amplifier

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input bias current				100	nA
Input offset voltage				±10	mV
Voltage swing	wrt VREF	±1			V
Load resistance	wrt VREF	10			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB
Retract Switch Resistance	Retract Mode, VP > 9 V			1	kΩ

A2, Current Sense Amplifier

Input Impedance	SE1	SE2 = VREF	1.5	2.4		kΩ
Input Impedance	SE2	SE1 = VREF	3.2	4.2		kΩ
Input offset voltage		SE1 = SE2 = VREF			±3	mV
Output voltage swing	V_{OH}	wrt VREF, VP ≥ 10.3 V	+3			V
	V_{OL}	wrt VREF			-3	V
Common mode range	V_{IL}				-0.2	V
	V_{IH}		VP + 0.2			V
Load resistance		wrt VREF	20			kΩ
Load capacitance					100	pF
Output impedance					25	Ω
Gain (SOUT - VREF)/(SE2 - SE1)		No DC load	3.9	4	4.1	V/V
Unity gain bandwidth			0.5			MHz
CMRR			55			dB
PSRR			60			dB

A3, Amplifier

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input bias current				100	nA
Output offset voltage		-10		10	mV
Output voltage swing V_{OL}				1	V
V_{OH}, wrt VP		-2			V
Common mode range V_{IL}				1	V
V_{IH}, wrt VP		-3			V
Load resistance	wrt VREF	20			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB

SOLS Output (VREF = 5V)

Output voltage swing V_{OL}	wrt VR2			-1	V
V_{OH}	wrt VR2	1			V
Output offset voltage	SOUT = VREF	-35		10	mV
Load resistance	wrt VR2	20			kΩ
Load capacitance				100	pF
Output impedance				200	Ω
Gain (SOLS-VR2)/(SOUT-VREF)	No DC load	0.4875	0.5	0.52	V/V

5V Voltage Reference

Output impedance	I_{OUT} = 0 to 6 mA			20	Ω
Gain V5/VBG	No DC load	4.05	4.17	4.3	V/V
Load capacitance				0.1	µF

Saturation Detector

ERRM threshold current	$\overline{SAT}$ falling				
sink		5		20	µA
source		5		20	µA
Hysteresis			2.3		µA

ACTUATOR PREDRIVER (continued)

Actuator MOSFET Drivers

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SE3 Input impedance	to VREF	10	25		kΩ
OUTA, OUTC voltage swing	$\|I_{OUT}\|$ < 1 mA	1.5		VP-1	V
OUTB, OUTD voltage swing	$\|I_{OUT}\|$ < 1 mA	1		VP-1.5	V
VTH, crossover threshold				1.6	V
Slew rate, OUTA..D	CL < 1000 pF	0.5			V/µs
Crossover time	±300 mV step at ERR			5	µs
Output impedance, OUTA..D			80		kΩ
Transconductance I(OUTA..D)/(ERR-VREF)			8		mA/V
Gain (SE3-SE1)/(ERR-VREF)		16	17	18	V/V

Retract Circuit

Retract voltage, $V_{RETRACT}$	VP > 5 V, level 1	0.7	0.82	1	V
RETRD discharge resistor	VP > 5 V, level 2	22	32	42	kΩ
RETRD trigger voltages					
VT1: level 1 to level 2	VP > 5 V, level 1	0.80	0.9	1.00	V
VT2: level 2 to float	VP > 5 V, level 2	45	55	65	% of VT1
RETRD input bias current	level 1			100	nA
SE1R input bias current				100	nA

VREF Monitor

VREF fail threshold	VREF falling	1.4	1.55	1.7	V
Hysteresis			85		mV

PWM Buffers

ROUT Pch				35	Ω
ROUT Nch				35	Ω
IL pull down resistor			100		kΩ

SPINDLE PREDRIVER

VCO (Unless otherwise specified: C_{VCO} = 0.01 µF, R_{VCO} =12 kΩ)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Typical frequency			$\frac{V_{RC}}{8.0\ R_{VCO}\ C_{VCO}}$		Hz
Run Frequency	V_{RC} = 2 V	1925	2145	2420	Hz
Idle Frequency	Mode = Reset	70		180	Hz
Reset Phase Error	$V_{RC} = V_{IDLE}$			18	deg

Phase Error Amplifier (Unless otherwise specified: R_{VCO} = 12 kΩ, R_{RPH} = ∞)

$V_{RC}(V_{IDLE})$	Mode = Reset		100		mV
Pump Current at RC Start Mode	$V_{RC} = V_{IDLE}$, R_{RPH} = ∞		4.5		µA
Run Mode, at speed	V_{RC} = 2 V		82		µA
Source/Sink Current Mismatch	V_{RC} = 2 V			5	%
PH1 Input Offset, State B	PH2 = VP, PH3 = 0	-100		100	mV
PH1 Input Offset, State E	PH2 = 0, PH3 = VP	-100		100	mV
PH2 Input Offset, State A	PH1 = VP, PH3 = 0	-100		100	mV
PH2 Input Offset, State D	PH1 = 0, PH3 = VP	-100		100	mV
PH3 Input Offset, State F	PH1 = VP, PH2 = 0	-100		100	mV
PH3 Input Offset, State C	PH1 = 0, PH2 = VP	-100		100	mV
RPH Voltage	R_{RPH} = 120 kΩ		2.4		V

Motor Current Control

ISENSE threshold (VLIMIT)		90	100	110	mV
One shot off time	C_{OS} = 0.002 µF	10	25	40	µs

Braking Circuit

$\overline{\text{BRAKE}}$ threshold	VP = 4 V	1		1.4	V
$\overline{\text{BRAKE}}$ VP threshold	$\overline{\text{BRAKE}}$ = 1.6 V			3.8	V
Bias current at $\overline{\text{BRAKE}}$				0.1	µA
CBRAKE current - run	Run mode, CBRAKE = VP			2	µA
CBRAKE current - brake	Brake mode, VP = 0, CBRAKE = 10 V			0.2	µA

SPINDLE PREDRIVER (continued)

NMOS Motor Driver Outputs (N1, N2, N3)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Source current	V_{OUT} = 4 V, R_{RSR} = 50 kΩ	3		6	mA
	V_{OUT} = 4 V, R_{RSR} = 100 kΩ	2		4	mA
Sink current	V_{OUT} = 4 V	9		35	mA
Output Low voltage	I_{SINK} = 5 mA			1	V
Output High voltage, wrt VP	I_{SOURCE} = 0.1 mA	-2.5			V

PMOS Motor Driver Outputs (P1, P2, P3)

Source current	Vout = VP - 4 V	20			mA
Sink current	Vout = VP - 4 V	9		35	mA
Output Low voltage	Isink = 1 mA			1.5	V
Output High voltage, wrt VP	Isource = 5 mA, V_N = 6 V	-1			V

TACH Comparator

SENSOR rising edge threshold	PH3 - PH2	30	100	170	mV
SENSOR falling edge threshold	PH2 - PH3	30	100	170	mV

SENSE COMPARATOR

Input voltage offset	VPSNS = 0.1 V			±10	mV

VOLTAGE FAULT MONITOR

VBG Output

Output voltage	No DC Load		1.2		V
Load capacitance				0.1	µF

VCC Reset Comparator

Trip voltage, regular mode	VCCTH = VCCHKL	4.26	4.35	4.44	V
(VCC falling, $\overline{MARGIN}$ = VCC)	VCCTH = 0	4.55	4.74	4.90	V
	VCCTH = VCC	3.43	3.57	3.71	V
Trip voltage reduction (VCC falling, $\overline{MARGIN}$ = 0)		10	14	18	%
Hysteresis		30	45	60	mV
Input resistance at VCCTH		90	140	250	kΩ

VCC Write Inhibit Comparator ($\overline{MARGIN}$ = High)

Trip voltage	VCC rising	5.55	5.77	6	V
Hysteresis		50	85	120	mV
Input resistance at VCCHKH			13		kΩ

+12 V Reset Comparator ($\overline{\text{MARGIN}}$ = High)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Trip voltage	V12 falling	9.20	9.50	9.80	V
Hysteresis		60	80	100	mV
Input resistance at V12CHK			14		kΩ

DIGITAL I/O

Digital Input ($\overline{\text{DISPWR}}$, PWMIN, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{RETR}}$)

Input voltage	V_{IL}		0.8			V
	V_{IH}				2	V
Input bias current	I_{IH}	Vin = 4 V			200	µA
Open circuit voltage					0.4	V

Digital Input ($\overline{\text{MARGIN}}$)

Input voltage	V_{IL}		0.8			V
	V_{IH}				2	V
Input bias current	I_{IL}	V_{IN} = 0.5 V			300	µA
Open circuit voltage			2.4			V

Digital Output (SENSOR)

Output voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 1 mA	-1			V

Digital Output ($\overline{\text{FAULT}}$)

Output voltage	V_{OL}	I_{SINK} = 5 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-2	-1		V

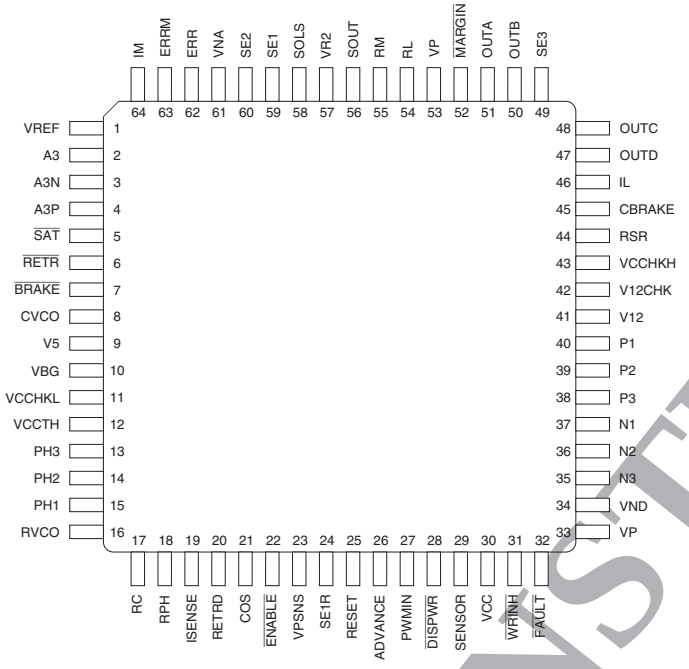
Digital Output ($\overline{\text{WRINH}}$, $\overline{\text{SAT}}$)

Output voltage	V_{OL}	I_{SINK} = 1 mA(0.7 mA for $\overline{\text{SAT}}$)			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-2	-1		V

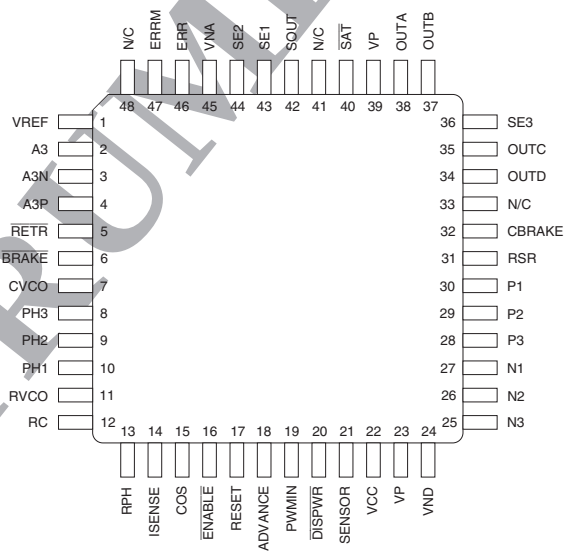
SSI 32H6829/6829A
Servo and
Spindle Predriver

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32H6829
64-Lead TQFP



32H6829A
48-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H6829A 48-Lead TQFP	32H6829A-CGT	32H6829A-CGT
SSI 32H6829 64-Lead TQFP	32H6829-CGT	32H6829-CGT

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SSI 32H6840
Advanced Servo and Spindle Predriver with DSP

Prototype

February 1996

DESCRIPTION

The SSI 32H6840 Advanced Servo and Spindle Predriver with DSP is a CMOS monolithic integrated circuit housed in a 128-lead QFP package, operates at five volts, provides control signals for external MOSFETs operating at twelve volts, and includes all key functionality necessary to implement the control of a hard disk drive spindle motor and head positioning servo. The device includes an industry standard compatible DSP core, data acquisition and conversion, predriver control of brushless, three-phase spindle motors without sensors using Silicon Systems' SilentSpin™ technology, predriver control of voice coil positioning motor, and power fault detection circuits. The integrated DSP is code compatible with the TMS320C25™ and includes internal program and data RAM.

FEATURES

- **Integrated TMS320C25™ code compatible 15 MIPS DSP core**
- **1568 words of configurable internal program and data memory**
- **Full external DSP bus for peripherals**
- **Relocatable on-chip peripheral paging**
- **Automatic wait state generation for external ROM, RAM, and peripherals**
- **1 μs, 10-bit A/D with 8 input MUX**
- **Two 10-bit voltage D/As with references**
- **16-bit D/A in cascade mode**
- **Auto and manual A/D convert modes**
- **SilentSpin™ spindle predriver**
- **12-bit pulse density PWM spindle D/A**
- **Spindle speed period counter**
- **Synchronized spindle master speed and phase counters**
- **Programmable brake delay**
- **Class B VCM predriver**
- **Error summing amplifier saturation detector**
- **Dual level retract for VCM**
- **Compatible with Silicon Systems' PRML Read Channel 32P49xx family**
- **Precision low voltage +5V and +12V monitors with velocity limited retract**
- **Extensive power saving modes**

SSI 32H6840
Advanced Servo and Spindle Predriver with DSP

BLOCK DIAGRAM

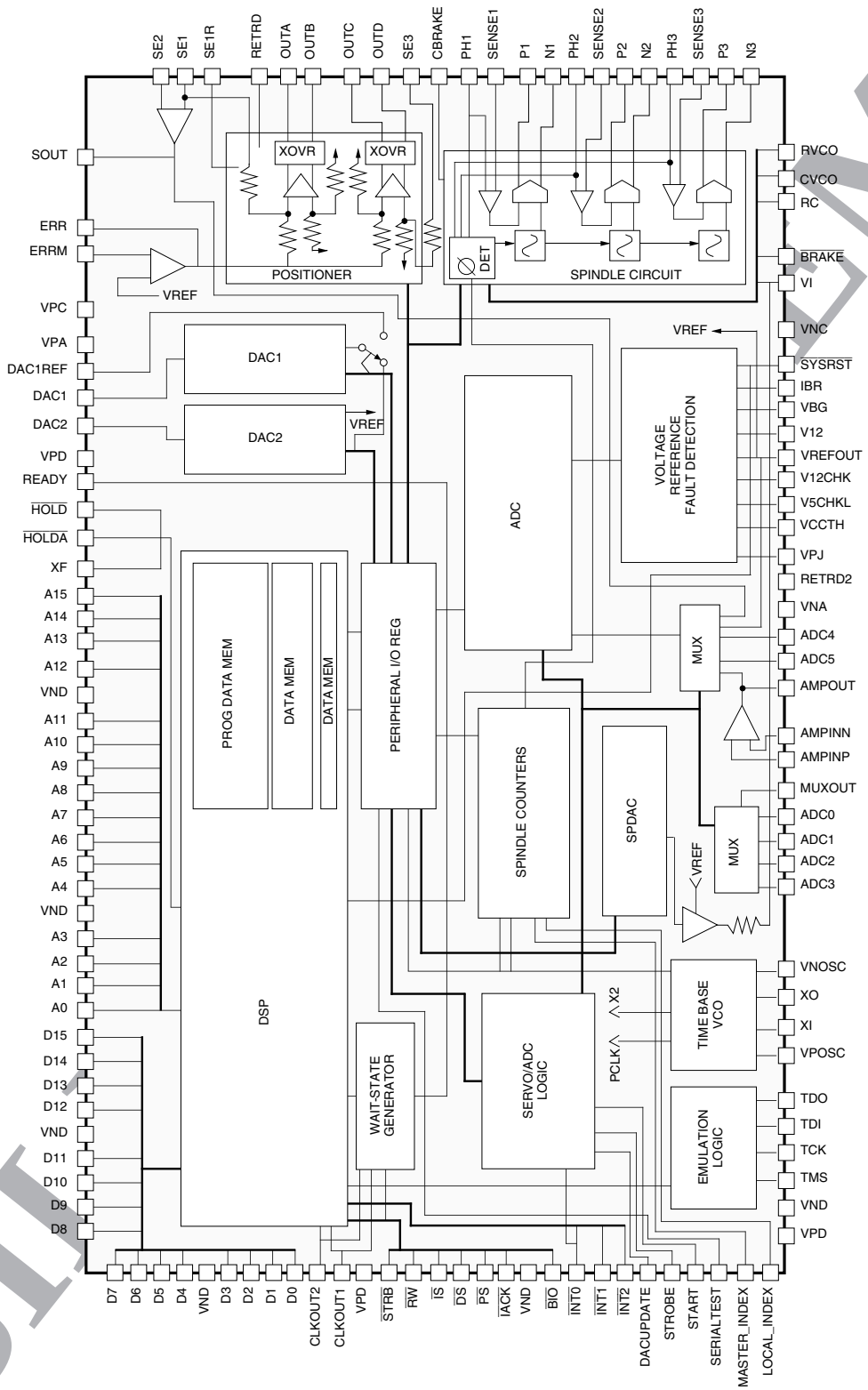


TABLE 1: Interrupt Sources

SOURCE	LEVEL	DESCRIPTION
RSB	1	External Reset Signal
INT0	2	External User Interrupt #0
INT1	3	External User Interrupt #1
INT2	4	External User Interrupt #2
TINT	5	Interval Timer Interrupt
TRAP	N/A	Software Interrupt

FUNCTIONAL DESCRIPTION

The SSI 32H6840 functional block diagram contains five major sections. These sections are Logic Functions (DSP core, DSP memory, wait-state generator, Peripheral I/O, servo logic, spindle timers, time base, emulation logic, and spindle DAC), ADC and DACs, Actuator Predriver, Spindle Predriver, Voltage Reference and Power Fault Detection.

DSP CORE

The DSP core is code compatible with the industry standard TMS32C025™. This high-speed, 15 MIPS core internally includes 1568 words of configurable program and data RAM. An internal wait state generator simplifies attachment of external peripherals. The on-chip peripheral page address is programmable and may be overlaid with internal data RAM for maximum algorithm performance.

EXTERNAL CONNECTIONS

An on-chip frequency synthesizer generates a 60 MHz system clock from an external 10 MHz crystal or clock source. This system clock operates a 4 stage instruction pipeline thereby determining the maximum instruction rate of 15 MIPS. The full address, data, and control bus is accessible so that external peripherals including program memory, data memory, and IO devices may be attached. Internal wait state generation is configurable for external bus transfers by type, address range, and duration. Hardware interrupt sources include three external pins and one internal timer interval interrupt as shown in Table 1.

DEVELOPMENT TOOLS

Development support for the 32H6840 includes JTAG Emulation Port, (compatible with IEEE 1149.1 standard), and a C source level debugger. Source code may be written in assembly or C languages. The 32H6840 debugger is compatible with many third party software tools as well.

PERIPHERAL IO PAGE

The DSP communicates with on-chip peripherals through the peripheral IO registers. These registers are accessible as data memory space. The page in data memory of these registers is programmed by the DSP by writing to the peripheral IO page bits 8..0 in memory mapped register PPWSC. The peripheral IO addresses always occupy the highest 16 words in their programmed data page. The peripheral IO page can be placed anywhere including the pages of internal RAM blocks B0 and B1. By programming the peripheral IO page to share the same data page as the most frequently used data memory, the peripheral IO registers may be accessed without the need to reload the data page pointer thereby significantly reducing instruction overhead.

WAIT STATE GENERATION

An on-chip programmable wait state generator simplifies the attachment of external program and data memory. The memory wait state generator register MEMWSG defined in Table 2 partitions the two memory spaces into four address segments each. Each memory segment can be assigned a different number of automatically inserted wait states as determined by the two-bit code. A two-bit code is further translated by values in the wait state control register PPWSC, (bits 14 and 15), into one of four values corresponding from zero to seven wait states.

TABLE 2: MEMWSG Definition

2-BIT WAIT STATE CODE	MEMORY SPACE	ADDRESS SEGMENT
0..1	program	0000H..3FFFH
2..3	program	4000H..7FFFH
4..5	program	8000H..BFFFH
6..7	program	C000H..FFFFH
8..9	data	0000H..3FFFH
10..11	data	4000H..7FFFH
12..13	data	8000H..BFFFH
14..15	data	C000H..FFFFH

TABLE 3: PPWSC Definition

BIT	DESCRIPTION
0..8	Peripheral IO Page Pointer
9..10	Not Used
11	Program wait state control
12	Data wait state control
13	IO wait state control
14..15	IO wait state code

TABLE 4: Memory Mapped Registers

NAME	ADDRESS	DESCRIPTION
MEMWSG	0	Memory Wait State
PPWSC	1	PIOREG page pointer (8-0) and Wait State Control
TIM	2	Timer
PRD	3	Period
IMR	4	Interrupt mask (5-0)
GREG	5	Global memory (7-0)

TABLE 5: IMR Definition

BIT	NAME	DESCRIPTION
0	INT0	External Interrupt 0
1	INT1	External Interrupt 1
2	INT2	External Interrupt 2
3	TINT	Timer Interrupt
4		Unused
5		Unused
15..6		Unused

TABLE 6: Interrupt Vectors

SOURCE	LOCATION	DESCRIPTION
RSB	0000H	Reset
INT0B	0002H	External Interrupt 0
INT1B	0004H	External Interrupt 1
INT2B	0006H	External Interrupt 2
TINT	0018H	Timer
TRAP	001EH	Software

WAIT STATE GENERATION (continued)

Table 4 describes the memory mapped special function registers located in data memory page zero. Register MEMWSG is located in the first word of page 0 while PPWSC is located in the second word.

Wait states may be automatically inserted for IO space accesses as well. IO wait states are programmed in the wait state control register PPWSC. The definition of the PPWSC register is found in Table 3. Program, data, and IO spaces each have a control bit which when "0" translates the two-bit wait state code into zero, one, two, or three wait states. When the wait control bit is a "1", then the translation of the two-bit wait state code is zero, one, three, or seven. When the device is reset, the default wait state timing for all spaces is preset for seven.

INTERRUPTS

Interrupts can be selectively enabled by writing a "1" or disabled by writing a "0" to the corresponding IMR register bit. Enabled interrupts are serviced by jumping to interrupt vectors in program memory. Table 5 shows the definition of the IMR register and Table 6 identifies the interrupt service vectors.

PERIPHERAL IO

The peripheral IO block consists of peripheral IO functions and registers. The registers are accessible by the DSP core in data memory with zero wait states. The data page of the peripheral IO registers is programmable in the peripheral IO page bits in the PPWSC register. The peripheral page may be programmed to overlay internal or external data memory. When overlaying internal data memory, the peripheral registers are accessible without intermediate data pointer loads and internal memory will not be affected by PIOREG writes. When overlaying external data memory, a write to PIOREG will overwrite both the PIOREG and the external memory. Internal data RAM, undisturbed by register accesses, may be recovered by programming the peripheral page to another location.

Each PIOREG register is 16 bits wide and the DSP communicates through the peripheral IO registers with the programmable digital functions such as A/D, D/As, spindle speed and phase counters, pulse density PWM-type DAC, and mode or control bits. See Figure 1 for PIOREG MAP definitions.

Data Acquisition

The A/D can be programmed to operate in different conversion modes which differ in the method of starting the A/D conversion, the number of conversions performed, and the input source. Table 7 lists these A/D conversion modes and the timing diagrams of Figure 13 and Figure 14 show two typical modes of operation. The method of starting the conversions is programmable and includes both external and DSP triggering. In a typical application, five conversions are performed corresponding to four position bursts from a quadrature servo demodulator and a fifth representing VCM motor current. Conversion status is indicated by use of the ADCBUSY and ADC(3:0) DONE status bits which are polled to monitor conversion progress and which registers have been updated. The result registers hold the left justified 10-bit result of 2's complement A/D conversions.

Data Conversion

Two 1 µs, 2's complement, 10-bit D/As identified as DAC1 and DAC2 are written left justified in the PIOREG register. Depending on the mode of operation selected, the DACs can be configured for independent writes, cascaded 16-bit DAC or FIFO pipelining of input data words. When configured as 16-bit cascaded DAC, the conversion of PIOREG 6 is as follows: bit 15 is the sign bit for both DACs, bits 14..6 are sent to DAC1, bits 5..0 are sent to DAC2 (corresponding to bits 8..3 of DAC2), and bits 2..0 of DAC2 are set to "100".

For spindle motor current control, a 12-bit pulse density DAC provides a PWM-type output through a 50 kΩ resistor to the VI pin of the spindle control circuit. A single capacitor to ground from the VI pin will provide adequate filtering. The SPDAC output is pulse density because it utilizes a technique illustrated in the timing diagram of Figure 2. Pulse density modulation redistributes the output signal's energy spectrum upward in frequency when compared to traditional PWM methods. With this technique, modulation ripple is significantly reduced.

Spindle Speed and Phase Counters

Spindle speed and phase control is implemented using three dedicated counters. Three counters provide sufficient resources to robustly implement synchronized spindle applications in both MASTER and SLAVE modes. Figure 3 shows these speed and phase counters. Counter 1 is dedicated to measuring the period of the local spindle. The spindle mode bits can be programmed so that the measurement periodcan be based on the commutation of the spindle motor itself or from an external source through the

TABLE 7: A/D Conversion Modes

MODE	ADC MODE CONTROL BIT VALUES			OPERATION
Normal	0	0	0	The START signal is asserted and each STROBE will convert ADC0-3 in sequence. After START is de-asserted, SOUT will be converted. There may be up to four STROBE signals during the START interval depending upon the number of bursts utilized. SOUT is converted on the fall of START after any active conversion is complete.
Normal-auto	0	0	1	After the assertion of START, a single STROBE signal will initiate the sequential conversion of ADC0-3 and SOUT. The conversions will complete at the rate of PCLK/13 in accordance with the PCLK clock being used. SOUT is converted after the de-assertion of start and any active conversion is complete.
Direct ADC0	0	1	0	This mode allows direct external control of the servo ADC to convert input ADC0 for use with external sample and hold and MUX circuits. The input is converted upon assertion of the STROBE signal.
Direct ADC4	0	1	1	This mode allows direct external control of the servo ADC to convert input ADC4 via the STROBE signal. For use with external level conditioning and sampling circuits.
External Calibration	1	0	0	The inputs ADC4, ADC5, SOUT, and VREF are converted when DSP sets the ADC START bit.
Manual Conversion	1	0	1	The inputs ADC0-3, and SOUT are converted under DSP control by asserting the ADC START bit.
SOUT Conversion	1	1	0	The DSP can initiate a conversion of SOUT by asserting ADC START bit.
Internal Calibration	1	1	1	The DSP initiates a sequence of conversions by setting ADC START. The outputs of DAC1, DAC2, VREF, and SOUT are converted and loaded into PIOREG.

Address-NAME	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 2	BIT 0
0 SERVO CONTROL	FIFO MODE	DAC WRITE MODE	ADC3 DONE	ADC2 DONE	ADC1 DONE	ADC0 DONE	ADC MODE 3	ADC MODE 2	ADC MODE 1	MARGIN	DAC1 VREF	RE-TRACT	SAT	VCM ENABLE	ADC START	ADC BUSY
1 ADCO/4 (READ)	BIT 9	ADC0/ADC4/DAC1								BIT 0						
1 SP PARAM (WRITE)					VHYST3	VHYST2	VHYST1	VHYST0	ISLEW3	ISLEW2	ISLEW1	ISLEW0	IPH3	IPH2	IPH1	IPH0
2 ADC1/5	BIT 9	ADC1/ADC5/DAC2								BIT 0						
3 ADC2/ VREF	BIT 9	ADC2/VREF								BIT 0						
4 ADC3	BIT 9	ADC3								BIT 0						
5 SOUT	BIT 9	SOUT								BIT 0						
6 DAC1	BIT 9 SIGN	DAC1								BIT 0	Refer to bit definitions in data conversion section					
7 DAC2	BIT 9 SIGN	DAC2								BIT 0						
8 CLOCK CONTROL								SLEEP 1	SLEEP 0	PCLK DIV 3	PCLK DIV 2	PCLK DIV 1	PCLK DIV 0	CNTR3 FLAG	CNTR2 FLAG	CNTR2 FLAG
9 TEST	BIT 15	TEST WORD (READ BACK IS ALWAYS 0)														
A SPIN. CONTROL	SPMUX MODE1	SPMUX MODE0	SPCNTR MODE1	SPCNTR MODE0	SPDIV MODE3	SPDIV MODE2	SPDIV MODE1	SPDIV MODE0	SPCLK SEL3	SPCLK SEL2	SPCLK SEL1	SP RESET	ENABLE	DIS PWR	GAIN	AD-VANCE
B SPDAC	0	BIT 11 MSB	SPINDLE DAC										BIT 0 LSB			
C SPIN. COUNT1	0	BIT 14	SPINDLE COUNTER 1													BIT 0
D SPIN. COUNT2	0	BIT 14	SPINDLE COUNTER 2													BIT 0
E SPIN. COUNT3	BIT 15 SIGN	SPINDLE COUNTER 3														BIT 0
F SPCNT3 PRESET	BIT 15 SIGN	SPINDLE COUNTER 3 PRE-LOAD														BIT 0

FIGURE 1: Peripheral I/O Register Map - PIOREG

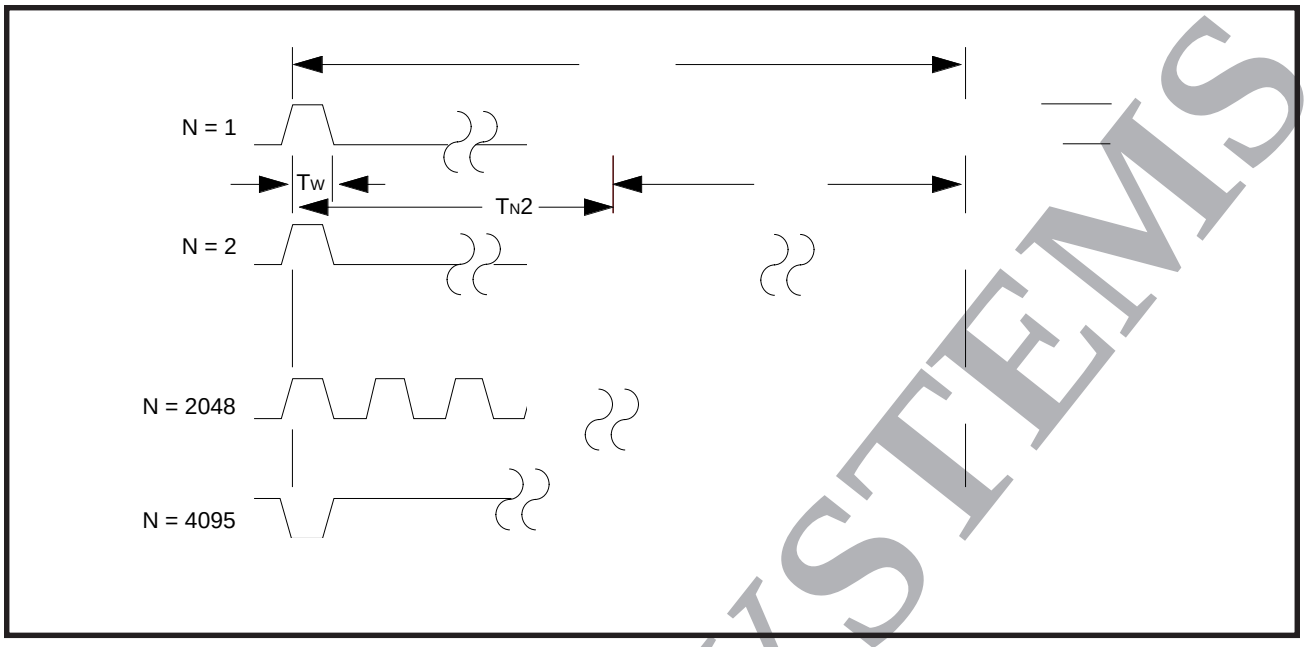


FIGURE 2: Spindle Pulse-Density PWM Timing Diagram (Internal signal, for reference only)

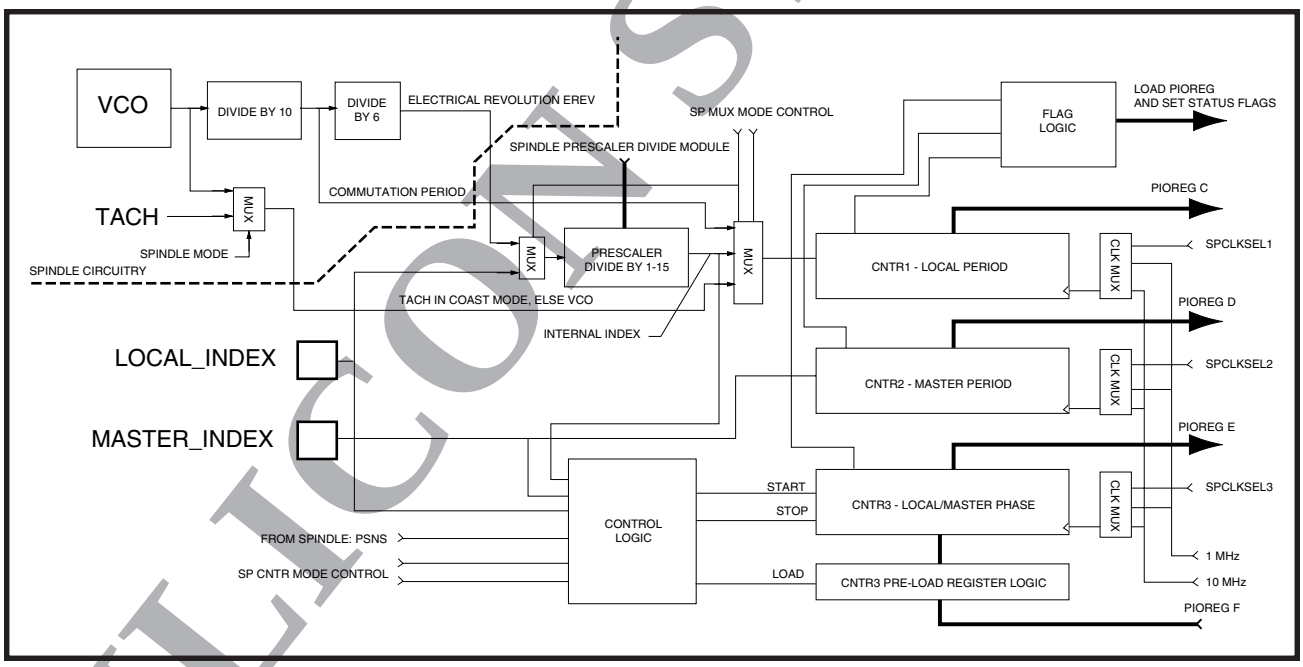


FIGURE 3: Spindle Counter Functional Blocks

Spindle Speed and Phase Counters (continued)

LOCAL pin. Programmable counters are included which can divide the measurement source down in frequency. Typically, the counters are programmed to account for the number of motor poles so that the period measurement is exactly one revolution. When the period measurement is complete, the count will be saved in the PIOREG and signal the DSP by setting the associated flag bit.

Synchronized spindle operation is supported with counters 2 and 3. Counter 2 is intended to measure the period of the master spindle through the MASTER pin. Counter 3 is a relative phase counter which is started by the master and stopped by the local spindle. Phase can be determined by reading counter 3. To assist measuring phase for all angles, counter 3 may be preloaded with a number such that a 2's complement value centered at zero corresponds to the desired phase.

Each spindle counter can be configured to count at a rate of 1 MHz or 10 MHz depending on the resolution required and the expected period to be measured. Counters 1 and 2 are up-counters which start at zero and count to 7FFFH where they saturate. Counter 3 is a presetable down counter (2's complement) ranging from 7FFFH to 8000H where it saturates.

Spindle Startup

Spindle motor startup is readily implemented by the DSP. The DSP asserts the ADVANCE bit in the spindle control register which in turn advances the commutation counter 1/10th of a commutation. The role of the DSP during startup is to provide an increasing frequency of ADVANCE pulses which will accelerate the motor. Once the motor has reached sufficient speed, the DSP enables normal mode. Once in normal mode, all further commutation is handled entirely by the spindle predriver block.

Capability for closed-loop, position sense and go, starting is provided in the spindle drivers and spindle timers. Refer to applications notes for details.

Time Base Prescaler

A Time Base prescaler is provided for the generation of internal clock signals. The signal X2 is generated by a PLL and is 6 times the frequency of the crystal or external clock referenced at X1, and is used to generate the DSP core clocks. A DSP cycle uses four X2 cycles. Outputs CLK1 and CLK2 are derived from X2 and are used for DSP interface timing. The clock for the peripheral circuits is referred to as PCLK and is generated from X2 divided by the value of bits PCLK (3-0) in the PIOREG register. In general, the peripherals require a clock rate of 10 MHz to 12.5 MHz (maximum), which is set by dividing X2 by the appropriate value. The PCLK register is preset to divide X2 by 6 on reset. The timing signals for the spindle counters are X2 divided by 6, or X2 divided by 60.

ACTUATOR PREDRIVER

Figure 4 details the actuator predriver, spindle predriver, and voltage reference and power fault blocks. The actuator block consists of amplifiers A1 through A4, saturation detector, and cross-over protection. The actuator predriver serves as a transconductance amplifier by driving four external MOSFETs in an H-bridge configuration. It has two modes of operation which are linear and retract. The retract mode is activated by a power supply failure or assertion of the RETRACT pin. Otherwise, the actuator operates in linear or normal mode.

Loop Compensation Amplifier

During linear operation, the acceleration signal is applied through amplifier A1 with three connections all available externally. RC components may be used to provide loop compensation at this stage. The saturation detector monitors amplifier A1 for saturation. Whenever amplifier A1 is in saturation, the current flowing through the summing node at ERRM will be detected and the SAT bit in the peripheral IO status register will be asserted.

MOSFET Drivers

ERR is the output signal of A1 and it drives two precision amplifiers each with a gain of 8.5. The first of these two amplifiers is inverting and it is formed from opamp A3, an on-chip resistor divider, and an off-chip complementary MOSFET pair. The second amplifier is non-inverting and it is formed in a similar manner as opamp A4. Feedback from the MOSFET drains on sense inputs SE1 and SE3 allow the amplifier gains to be established precisely. The voice coil motor and a current sense resistor is connected in series between SE1 and SE3.

ACTUATOR PREDRIVER (continued)

Crossover Protection Blocks

Crossover protection circuitry between the outputs of A3 and A4 and the external MOSFETs ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also apply a constant voltage across the motor to retract the heads at a constant velocity.

Current Sense Amplifier

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 is fixed gain with internal resistors) through inputs SE1 and SE2. SOUT is referenced to VREF.

Retract Function

The 6840 incorporates a dual level retract scheme. When retract is initiated, a fixed voltage (level 1) is applied across the actuator to force a constant retract velocity. After an externally adjustable amount of time, a higher voltage (level 2) is briefly applied to the actuator. At the end of level 2, the actuator is floated (i.e., zero current).

The timing and amplitude of the level 2 phase can be adjusted with external components. R_{RTR}, C_{RTR}, and an internal discharge resistor which is activated during level 2 control the retract timing. When $\overline{\text{RETRACT}}$ is first lowered, R_{RTR} discharges C_{RTR} until the RETRD pin reaches the level 2 trigger threshold (nominally 0.85V). At this time, the level 2 tract amplitude is applied to the actuator and the internal discharge resistor (nominally 32 kΩ) quickly discharges C_{RTR}. When C_{RTR} has been discharged to half of the trigger voltage, all retract current is turned off and the actuator is floated. The level 1 retract amplitude is internally fixed (0.85V nominal). During level 2, SE1R is fed back to the retract amplifier instead of SE1. Thus the level 2 amplitude will be increased by the factor $(1 + R_{R1}/R_{R2})$.

A second external RC delay is used between $\overline{\text{RETRACT}}$ and $\overline{\text{BRAKE}}$ to program the brake delay and ensure the actuator has enough time to retract before the spindle is braked.

SPINDLE PREDRIVER

Figure 4 provides a detailed block diagram of the spindle predriver block. The spindle block includes spindle motor current shaping, a phase error circuit and phase locked loop, MOSFET predrivers, and a delayed spindle brake circuit. The current shaping circuit employs Silicon Systems' SilentSpin™ technology which shapes the spindle motor current to minimize acoustic noise.

SilentSpin™ Waveform Generator

The SilentSpin™ wave generator drives the spindle motor windings with properly phased current waveforms. In run mode, the generator is clocked by the VCO output. During start mode, the generator is clocked by the ADVANCE bit in the spindle control register.

The analog signal at pin VI controls the peak amplitude of the current waveform. With the spindle control register bit GAIN programmed as "0", the peak current occurring when the voltage at VI is equal to VREFOUT corresponds to 294 mV dropped across each sense resistor. Programming GAIN to "1" configures the peak current to correspond to 79 mV across each sense resistor.

Phase Error Circuit and PLL

The phase error circuit determines the phase error between the current and voltage in each winding. Depending on the result of the comparison and the phase of the commutator, a positive or negative pump current is applied to the RC pin.

The magnitude of the pump current at RC is the sum of a constant current (IPH) and a current proportional to the VCO frequency. The constant current value for IPH is set by the value of the bits IPH(3:0) in the PIOREG word 1. (see PIOREG definition.) The default value is 8h (10 μA), otherwise IPH = 1.25 μA • N, for N = 0 to 15. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on VCO is nominally 2.0 volts. When the VCO is reset, the VCO output is forced low. The first VCO clock will occur immediately after the VCO exits reset.

MOSFET Predrivers

The N and P outputs drive the gates of the external N and P channel power MOSFETs. Except during brake, both the N and P drivers are switched with PWM. During brake, the N channel MOSFETs are turned on and the P channel MOSFETs are turned off. To minimize electrical switching noise, the charge and discharge currents at N and P can be adjusted with the ISLEW DAC. The output current is 100 times the value of ISLEW (ISLEW = 6.8 μA • (N+1)).

Delayed Spindle Brake

Brake mode is invoked whenever the $\overline{\text{BRAKE}}$ pin or the BRAKE bit in the spindle mode register is asserted. A delayed spindle brake resulting from power failure is implemented with and external resistor and capacitor. The brake resistor tied between $\overline{\text{BRAKE}}$ and $\overline{\text{SYSRST}}$. The brake delay capacitor is connected from $\overline{\text{BRAKE}}$ to ground. The time constant of the two discrete components determines the delay from system reset assertion to dynamic braking.

A second capacitor is required to provide the voltage necessary to assert the brake condition during power failure. This capacitor is connected at the CBRAKE pin to ground.

Voltage Reference and Fault

The voltage reference circuit generates VRETRACT, VIDLE, and several other internal voltage and current references. It also generates an precise 1.200 volt reference at pin VBG for use with the fault detection comparators. VBG is internally multiplied by 1.875 and output as VREFOUT.

The voltage fault detector contains sensing for under-voltage on the twelve volt supply through the V12CHK pin and on the five volt supply with the VCCHKL pin. An internal resistor divider monitoring the five volt supply is available at the VCCTH pin. If VCCTH is the correct voltage and tolerance, it can be connected directly to VCCHKL; otherwise, an external resistor divider can be used with VCCHKL.

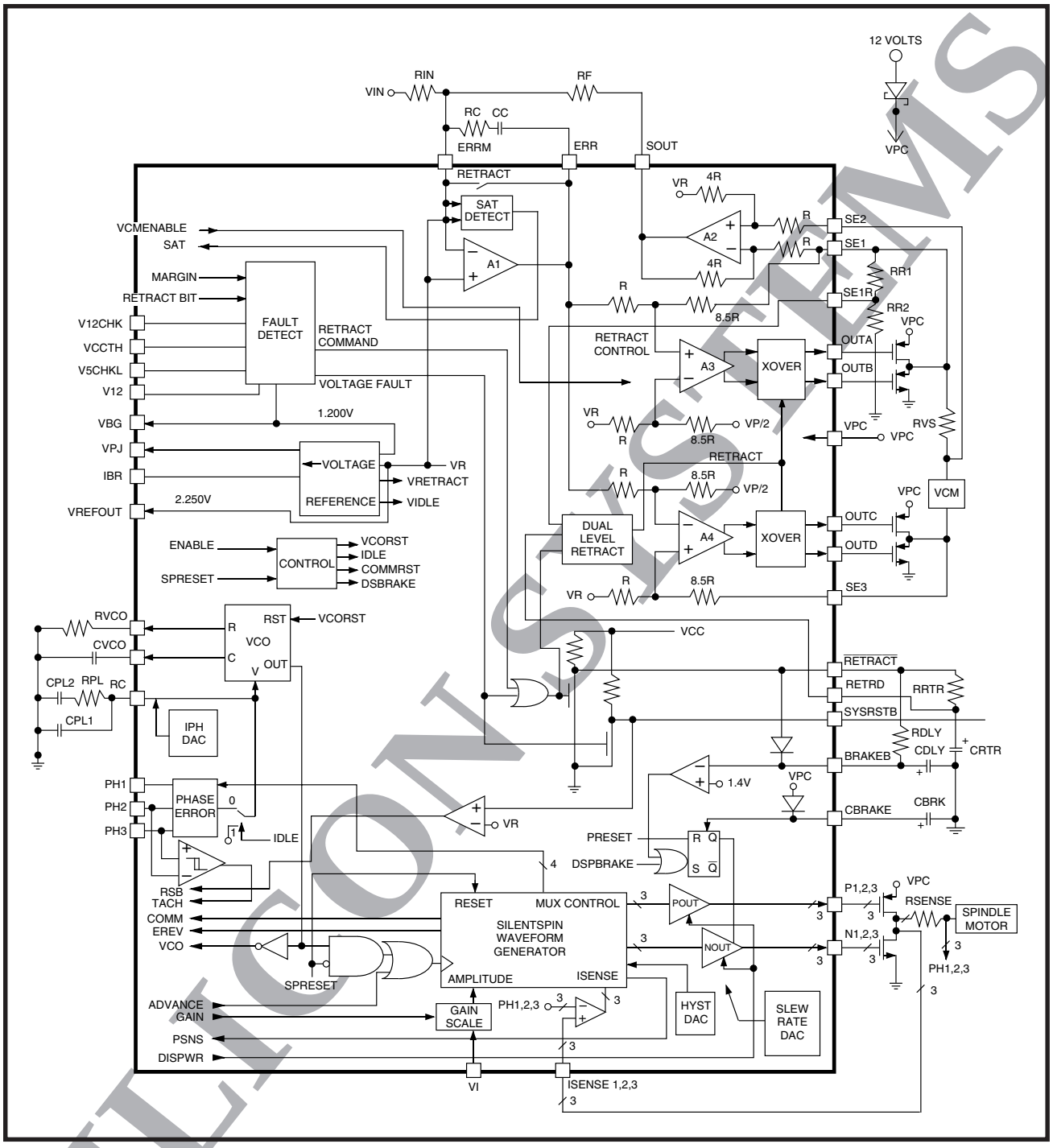


FIGURE 4: Spindle and Positioner Circuitry

PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, I = Digital Input, AO = Analog Output, O = Digital Output, Z = Tri-State Output, OC = Open Collector Output.

SUPPLIES

NAME	TYPE	DESCRIPTION
VNA, VND	GROUND	Analog and Digital grounds. These pins are internally connected.
VDD	POWER	Digital +5V supply
VPO	POWER	+5V supply for internal crystal oscillator
VNO	GROUND	Internal crystal oscillator ground
VPC	POWER	The +12V supply. Diode protected from system +12V. This is also the bridge supply for the spindle and actuator FETs.

DSP CORE

D(15:0)	I/O/Z	Data input/output pins. Pin is high impedance state in hold mode.
READY	I	Data ready input, allows cycle extension for external devices if the internal wait-state generator is not utilized. Ready is sampled when $\overline{DS}$, $\overline{IS}$, or $\overline{PS}$ go low, if READY is high, the internal wait-state is used, if low, the external wait-state generator is used.
$\overline{HOLD}$	I	When this input is asserted, the DSP core places all its control lines and buses in a high impedance state.
$\overline{BIO}$	I	Branch control input. If low, the DSP core will branch on a BIOZ instruction.
$\overline{INT}$(2:0)	I	Three external user interrupts. $\overline{INT}$0 must be used as servo interrupt when DAC FIFO mode is being used.
A(15:0)	O/Z	Address bus outputs. Pin is high impedance state in hold mode.
$\overline{DS}$	O/Z	Data memory select signal. Pin is in high impedance state in hold mode.
$\overline{PS}$	O/Z	Program memory select signal. Pin is in high impedance state in hold mode.
$\overline{IS}$	O/Z	Input/Output select signal.Pin is in high impedance state in hold mode.
R/$\overline{W}$	O/Z	Read/Write signal for communication with external devices. Pin is high impedance state in hold mode.
$\overline{STRB}$	O/Z	Strobe signal for external bus cycles. Pin is in high impedance state in hold mode.
$\overline{HOLDA}$	O	Hold Acknowledge signal, asserted when in hold mode
$\overline{IACK}$	O	Interrupt acknowledge signal. Asserted when CLKOUT1 is low, and the program is branching to address on A(15:0).
XF	O	External flag
CLKOUT1	O	Instruction cycle phase indicator. Rises at start of Q3, falls at start of Q1.
CLKOUT2	O	Instruction cycle phase indicator. Rises at start of Q2, falls at start of Q4.
XO	AO	Output pin of the internal crystal oscillator. Leave unconnected if oscillator function is not used.

DSP CORE (continued)

NAME	TYPE	DESCRIPTION
XI	AI	Input pin for externally supplied clock, or connection to crystal for internal oscillator
SERIALTEST	O	Serial test port. DSP writes to special PIOREG location will result in contents shifted out on this pin.
DACUPDATE	I	Outputs data from DACFIFO to the DACs when DAC FIFO mode is selected
TDI	I	Emulator serial input port
TDO	O	Emulator serial output port
TCK	I	Emulator serial port clock
TMS	I	Emulator serial port mode select
LOCALINDEX	I	Signal from local spindle indicating rate of revolution
MASTERINDEX	I	Signal from (remote) master spindle in synchronized spindle applications

DATA CONVERSION

DAC1	AO	Output of DAC1
DAC2	AO	Output of DAC2
DAC1VREF	AI	Provides reference voltage to DAC1 if appropriate mode is selected.
ADC(5:0)	AI	Inputs to ADC multiplexer
MUXOUT	AO	Output of the first level multiplexer which selects ADC(3:0)
AMPINN	AI	Level and gain conditioning amplifier negative input
AMPINP	AI	Level and gain conditioning amplifier positive input
AMPOUT	AO	Level and gain conditioning amplifier output signal
START	I	This pin causes a sequence of A/D conversions in conjunction with STROBE
STROBE	I	Initiates a conversion by the ADC per the defined operating mode

ACTUATOR

NAME	TYPE	DESCRIPTION
ERR	AO	POSITION ERROR - The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3 - SE1 = 17 • (ERR - VREFOUT)
ERRM	AI	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier
SOUT	AO	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external sense resistor, as follows: SOUT - VREFOUT = 4 • (SE2 - SE1)
SAT	O	SATURATION DETECT - Monitors the error amplifier and is high when the amplifier has saturated (ERR is no longer proportional to the VCM voltage).
SE2	AI	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	AI	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point from ERR is: SE1 - VREFOUT = -8.5 • (ERR - VERFOUT)
SE3	AI	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3 - VREFOUT = 8.5 • (ERR - VREFOUT)
SE1R	AI	Alternate SE1 connection to the retract amplifier. This input is selected during the “pulse” phase of retract. An external resistor divider connected to this pin programs the retract amplitude during the “pulse” phase.
$\overline{\text{RETRACT}}$	OC	A retract command from the DSP or a voltage fault will cause this pin to go low, initiating a retract. This pin is open drain with internal pull-up resistor and may be activated internally.
RETRD	AI	A resistor from pin $\overline{\text{RETRACT}}$ and a capacitor to GND will set the timing for the dual-level retract operation. When the voltage on this pin falls below the trigger level, the “pulse” phase of the retract occurs (an internal pull-down resistor is activated also). When the voltage falls to 50% of the trigger value, the “pulse” phase is terminated.
OUTA OUTC	AO	P-FET DRIVE - Drive signal for a P-channel MOSFET connected between one side of the motor and VPC
OUTB OUTD	AO	N-FET DRIVE - Drive signal for an N-channel MOSFET connected between one side of the motor and GND. Crossover protection circuitry ensures that the P and N channel devices connected to the same side of the motor are never enabled simultaneously.

PIN DESCRIPTION (continued)

SPINDLE

NAME	TYPE	DESCRIPTION
P1, P2, P3	AO	P-CHANNEL SPINDLE DRIVERS - These pins are connected to the gates of three P channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	AO	N-CHANNEL SPINDLE DRIVERS - These pins are connected to the gates of three N channel power MOSFETs in the spindle motor power bridge.
VI	AO, C	SPINDLE CURRENT CONTROL VOLTAGE - Determines the peak amplitude of the spindle motor drive currents. External capacitor at this pin forms low-pass filter.
ISENSE1 ISENSE2 ISENSE3	AI	SPINDLE CURRENT SENSE - Connects to the spindle current sense resistors. The motor current in each winding is calculated by subtracting that winding's PH from its ISENSE.
RVCO	C	VCO RESISTOR - Sets the speed range of the VCO. The voltage at RVCO is forced to track RC.
CVCO	C	VCO CAPACITOR - Sets the speed range of VCO.
RC	C	PLL LOOP FILTER - Sets the time constant for the PLL in run mode. In all other modes, it is connected to a DC voltage, VIDLE. VIDLE determines the VCO frequency at which crossover from startup to run should occur (by setting the ENABLE bit).
PH1 PH2 PH3	AI	SPINDLE MOTOR TERMINALS - These pins are used to calculate the phase error in the PLL. They are also used, in conjunction with ISENSE1,2,3 to calculate winding current.

VOLTAGE REFERENCE AND FAULT DETECT

NAME	TYPE	DESCRIPTION
V12	AI	The 12V supply reference to the 12V fault detector.
V12CHK	AI	12V RESET COMPARATOR INPUT - The input to the 12V reset comparator and the connection to an optional external bypass capacitor. V12 is divided down at this pin by an on-chip resistor divider and then compared to VBG. If V12CHK falls below VBG, a forced retract occurs.
V5CHKL	AI	The 5V low voltage detect pin. May be connected to a bypass capacitor. When this pin falls below VBG, $\overline{\text{SYSRST}}$ is active and retract is initiated.
VCCTH	AI	The 5V divider output. Normally left open. The VCC low voltage check level can be modified by biasing this pin with an external resistor divider.
IBR	C	BIAS RESISTOR - This resistor sets the internal bias currents of the analog circuitry.
$\overline{\text{SYSRST}}$	OC	SYSTEM RESET - Active low, this open-collector output is asserted when a low condition is detected on either 5V or 12V. Provides reset signal to internal logic, including $\overline{\text{RS}}$ signal in DSP.
$\overline{\text{BRAKE}}$	AI	BRAKE - Active low, this input is pulled low by an external RC to perform a delayed brake. Note that when $\overline{\text{BRAKE}}$ is asserted, it sets a latch that is cleared in the Preset mode.
CBRAKE	C	BRAKE CAPACITOR - A storage capacitor is connected to CBRAKE to supply the charge necessary to turn on the NMOS device during brake.
VREFOUT	AO	VREFOUT is equal to 1.875 • VBG and represents the reference potential for the actuator, data converters, and spindle analog circuits.
VBG	AO	Output voltage of the band-gap voltage reference generator.
VPJ	AO, C	Internally generated 5V power supply for spindle and positioner logic and analog circuits. VPJ will hold its value as long as VPC maintains due to back-EMF from the spindle motor. Attach bypass capacitor as required.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
V12, VPC	0 to 14V
VPA, VCC	0 to 7V
SE1, SE2, SE3, N1, N2, N3, $\overline{\text{BRAKE}}$, CBRAKE	0 to 15V
PH1, PH2, PH3, ISENSE1, ISENSE2, ISENSE3	-2 to 15V
$\overline{\text{SYSRST}}$, RETRD, $\overline{\text{RETRACT}}$	0 to VCC
All other pins	0 to VCC
Storage Temperature	-45 to 165°C
Soldering Temperature, 10 seconds duration	260°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, the following conditions are valid through this document.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V12	Normal Mode	9	12	13.2	V
	Retract Mode	3.5		14.0	V
VPC	Normal Mode	9	$V12-V_D$	14	V
	Retract Mode (back-emf)	3.5		14	V
VPA, VCC		4.5	5.0	5.5	V
VBG bypass capacitor			0.1		µF
VPJ bypass capacitor			0.1		µF
VREFOUT bypass capacitor			0.1		µF
IBR Resistor		11.8	12.0	12.2	kΩ
RVCO Resistor		24	25	26	kΩ
Operating Temperature		0		70	°C

DC CHARACTERISTICS

VPC Current	Normal Operation			35	mA
VCC Current	Normal Operation			100	mA
VPA Current	Normal Mode			15	mA

A1, LOOP COMPENSATION AMPLIFIER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Bias Current	Pin ERRM	-100		100	nA
Input Offset Voltage	w.r.t. VREFOUT	-10		10	mV
Voltage Swing V_{OL} V_{OH}, wrt VREFOUT	R_L = 10 kΩ to VREFOUT	 1		 -1	 V V
Load Capacitance	Maximum Load			100	pF
Gain		60			dB
Unity Gain Bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB
Retract Switch Resistance	Retract Mode, VPC > 9V			1	kΩ
SAT threshold (|ERR-VREFOUT|)		0.8	0.9	1.0	V
Hysteresis			40		mV

A2, CURRENT SENSE AMPLIFIER

Input Impedance, Resistive	SE2 = VREFOUT	2.6	4.3	100	kΩ
	SE1 = VREFOUT	3.2	5.4		kΩ
Input Offset Voltage	SE1 = SE2 = VREFOUT			20	mV
Output Voltage Swing V_{OL}	R_L = 20 kΩ to VREFOUT			 -1	 V
V_{OH}	wrt VREFOUT	1			V
Common Mode Range V_{OL}		 -0.2			 V
V_{OH}				V12+0.2	V
Load Capacitance	Maximum Load			100	pF
Load Resistance	to VREFOUT	20			kΩ
Output Impedance				20	Ω
Gain (SOUT-VREFOUT)/(SE1-SE2)		3.9	4.0	4.1	V/V
Unity Gain Bandwidth		0.5			MHz
CMRR		52			dB
PSRR		60			dB

ELECTRICAL SPECIFICATIONS (continued)

ACTUATOR MOSFET DRIVERS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SE3 Input Impedance	to VREFOUT	10	25		kΩ
OUTA, OUTC voltage swing	|IOUT|<1 mA	1.5		VP-1	V
OUTB, OUTD voltage swing	|IOUT|<1 mA	1		VP-1.5	V
VTH, crossover separation threshold				1.6	V
Slew Rate, OUTA...D	CL ≤ 1000 pF	0.5			V/µs
Crossover Time	±300 mV step at ERR CL ≤ 1000 pF			4	µs
Output impedance, OUTA...D			20		kΩ
Transconductance I(OUTA...D)/(ERR-VREFOUT)			8		mA/V
Gain - (SE1-VREFOUT)/(ERR-VREFOUT) or (SE3-VREFOUT)/(ERR-VREFOUT)		8	8.5	9	V/V
Retract Motor Voltage	VP.5V	0.7	0.82	1.0	V

VCO

Unless otherwise specified, C_{VCO} = 1.0 µF, R_{VCO} = 25 kΩ

Typical Frequency		$F_{VCO} = V_{RC}/(4 \cdot R_{VCO}C_{VCO})$			Hz
Run Frequency	RC = 2.0V	17.5	19.75	22.0	kHz
Idle Frequency	Mode = Reset	700	1100	1500	Hz
Reset Phase Error	RC = V_{IDLE}			18	°

RETRACT CIRCUITS

Retract Voltage	VP>5V, level 1	0.7	0.82	1.0	V
RETRD Discharge Resistor	VP>5V, level 2	22	32	42	kΩ
RETRD Trigger Voltages VT1: level 1 to level 2 VT2: level 2 to float (% of VT1)	 VP>5V, level 1 VP>5V, level 2	 0.75 45	 0.85 50	 0.95 55	 V %
$\overline{\text{RETRACT}}$ Output Level V_{OL}	I_{SINK} = 8 mA			0.4	V
$\overline{\text{RETRACT}}$ Output Voltage V_{OH}	I_{SOURCE} = 0.1 mA	VCC-2.0			V
$\overline{\text{RETRACT}}$ Input Threshold V_{IL}		0.8			V
$\overline{\text{RETRACT}}$ Input Threshold V_{IH}				2.0	V
RETRD Input Bias Current	level 1			100	nA
SE1R Input Bias Current				100	nA

PHASE ERROR AMPLIFIER

Unless otherwise specified, RVCO = 25 kΩ, IPH = 0

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V_{RC} (V_{IDLE})	Mode = Reset		100		mV
Pump Current at RC					
Start Mode	$V_{RC} = V_{IDLE}$		7		µA
Run Mode, at speed	V_{RC} = 2V		82		µA
Source/Sink Current Mismatch	V_{RC} = 2V			5	%
PH1 Input Offset, State B	PH2 = V12, PH3 = 0	-60		60	mV
PH1 Input Offset, State E	PH2 = 0, PH3 = V12	-60		60	mV
PH2 Input Offset, State A	PH1 = V12, PH3 = 0	-60		60	mV
PH2 Input Offset, State D	PH1 = 0, PH3 = V12	-60		60	mV
PH1 Input Offset, State B	PH1 = V12, PH2 = 0	-60		60	mV
PH1 Input Offset, State E	PH1 = 0, PH2 = V12	-60		60	mV

BRAKING CIRCUITS

CBRAKE Input Current - RUN	Run mode, VC_{BRAKE} = VP			2	µA
CBRAKE Input Current - BRAKE	Brake mode, VC_{BRAKE} = 10V			0.2	µA
$\overline{\text{BRAKE}}$ Threshold	T_A = 25°C, VP = 4V	1.1	1.25	1.4	V
$\overline{\text{BRAKE}}$ VP Threshold	$\overline{\text{BRAKE}}$ = 1.5V			3.8	V
$\overline{\text{BRAKE}}$ Bias Current				0.1	mA

VOLTAGE FAULT CIRCUIT

VCC Low Trip Point	VCC falling, MARGIN = 0 VCCTH = open	4.26	4.35	4.44	V
VCC Low Hysteresis		30	40	50	mV
VCC Low Trip Point	VCC falling, MARGIN = 0 VCCTH = 0	4.635	4.74	4.843	V
VCC Low Trip Point	VCC falling, MARGIN = 0 VCCTH = VCC	3.49	3.57	3.65	V
VCC Low Trip Change	MARGIN = 0 MARGIN = 1	-10	-14	-16	%
VCCTH Input Range	normal operation	0		2.9	V
VCCTH Input Resistance		90	140	250	kΩ
VREFOUT Fail Threshold	VREFOUT falling	1.4	1.55	1.7	V
VREFOUT Check Hysteresis			85		mV
V12 Low Trip Point	V12 falling	9.2	9.5	9.8	V
V12 Low Hysteresis		60	80	100	mV
V12CHK Impedance			14K		Ω
V5CHKL Bias Current				0.1	µA

ELECTRICAL SPECIFICATIONS (continued)

NMOS MOTOR DRIVER OUTPUTS (N1, N2, N3)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Source Current	V_{OUT} = 4V, ISLEW = 8h		5.8		mA
Sink Current	V_{OUT} = 4V, ISLEW = 8h		5.8		mA
Output High On Resistance				TBD	Ω
Output Low On Resistance				TBD	Ω

PMOS MOTOR DRIVER OUTPUTS (P1, P2, P3)

Source Current	V_{OUT} = VP-4, ISLEW = 8h		5.8		mA
Sink Current	V_{OUT} = VP-4, ISLEW = 8h		5.8		mA
Output High On Resistance				TBD	Ω
Output Low On Resistance				TBD	Ω
V_{OL}	I_{IN} =1 mA		0.4		V
V_{OH}	I_{OUT} =1 mA	VCC-0.4			V

TACH COMPARATOR

SENSOR Rising Edge Threshold	PH3-PH2	60	140	200	mV
SENSOR Falling Edge Threshold	PH2-PH3	60	140	200	mV

ISENSE1,2,3 (WITH RESPECT TO PH1,2,3)

OffsetVP (ISENSE-PH)	PH = VP, HYST = TBD, VI = 0	3	5.2	7.5	mV
Offset0 (ISENSE-PH)	PH = 0, HYST = TBD, VI = 0	-7.5	-5.2	-3	mV
Offset (OffsetVP - Offset0)	HYST = TBD, VI = 0	-2		2	mV
Hysteresis (OffsetVP-Offset0)	HYST = TBD, VI = 0	9		12	mV
V57Degrees (Average of PH=VP and PH=0 measurements)	VI = 2.4V, HIGHI = 1, HYST = TBD	113		138	mV

VBG OUTPUT

Output Voltage	No DC Load		1.20		V
Load Capacitance				0.1	µF

VREFOUT

Output Voltage	No DC Load	2.14	2.25	2.36	V
Output Impedance	$I_{SOURCE} \leq 1.0$ mA $I_{SINK} \leq 1.0$ mA			20	Ω

VPJ

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Voltage	VPC ≥ 6V	4.5	5.0	5.5	V
Bypass Capacitor Value			1		µF

SYSRST

Output Level	V_{OL}	I_{SINK} ≤ 8 mA			0.4	V
Output Voltage	V_{OH}	I_{SOURCE} ≤ 0.1 mA	VCC-2.0			V
Input Threshold	V_{IL}	Input rising	2.10		2.37	V
Input Hysteresis			120			mV

CLOCK TIMING

$\overline{\text{SYNC}}$ Hold Time	THS					ns
$\overline{\text{SYNC}}$ Setup Time	TSUS					ns
CLKOUT1/CLKOUT2 Cycle Time	TCC		67			ns
CLKOUT1/CLKOUT2 Low Pulse Duration	TWCL		26		36	ns
CLKOUT1/CLKOUT2 High Pulse Duration	TWCH		30		40	ns
CLKOUT1 Edge to CLKOUT2 Edge	TDC1C2		11.66		21.66	ns

ELECTRICAL SPECIFICATIONS (continued)

MEMORY AND I/O READ AND WRITE TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{\text{STRB}}$ from CLKOUT1	TDC1S		15		19	ns
CLKOUT2 to $\overline{\text{STRB}}$	TDC2S		0		5	ns
$\overline{\text{STRB}}$ Low Pulse Duration	TWSL		32		35	ns
$\overline{\text{STRB}}$ High Pulse Duration	TWSH		32		35	ns
Address Setup Time before $\overline{\text{STRB}}$ Low	TSUA		8			ns
Address Hold Time after $\overline{\text{STRB}}$ High	THA		15			ns
Read Data Access Time from Address	TAA				19	ns
Data Read Setup Time before $\overline{\text{STRB}}$ High	TSUDR		15			ns
Data Read Hold Time after $\overline{\text{STRB}}$ High	THDR		0			ns
Data Bus Starts Being Driven after $\overline{\text{STRB}}$ Low	TEND		0			ns
Data Write Setup Time before $\overline{\text{STRB}}$ High	TSUDW		22			ns
Data Write Hold Time from $\overline{\text{STRB}}$ High	THDW		12			ns
Data Bus Tri-state after $\overline{\text{STRB}}$ High	TDISD		30			ns
READY Hold Time after $\overline{\text{STRB}}$ Low	THSLR		16			ns
READY Valid after $\overline{\text{STRB}}$ Low	TDSLR				-5	ns

EXTERNAL WAIT-STATE MEMORY AND I/O READ AND WRITE TIMING

READY Hold after CLKOUT2 High	THC2HR		16.66			ns
RREADY Valid after CLKOUT2 High	TDC2HR				-4.34	ns

$\overline{\text{SYSRST}}$ TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{\text{SYSRST}}$ Setup before CLKOUT1 High		TSUIN		TBD		ns
$\overline{\text{SYSRST}}$ Hold after CLKOUT1 High		THIN		TBD		ns
CLKOUT1 Low to Reset State Entered		TDRS		TBD		ns
$\overline{\text{SYSRST}}$ Low Pulse Duration	TWRS			TBD		ns

INTERRUPT, $\overline{\text{BIO}}$ AND XF TIMING

$\overline{\text{INT}}$/$\overline{\text{BIO}}$ Low Pulse Duration	TWIN		66			ns
CLKOUT1 to $\overline{\text{IACK}}$ Valid	TDIACK		-2			ns
XF Valid before Falling Edge of $\overline{\text{STRB}}$	TDXF		9			
$\overline{\text{INT}}$/$\overline{\text{BIO}}$ Setup before CLKOUT1 High	TSUIN		15			
$\overline{\text{INT}}$/$\overline{\text{BIO}}$ Hold after CLKOUT1 High	THIN		0			

HOLD CONDITION ENTRY TIMING

$\overline{\text{HOLD}}$ valid after CLKOUT2 High	TDC2HH				-2	ns
Address tri-state after CLKOUT1 Low	TDISC1LA				14	ns
$\overline{\text{HOLDA}}$ low to address tri-state	TDISALA				8	ns
$\overline{\text{HOLDA}}$ Low after CLKOUT1 Low	TDC1LAL				6	ns

HOLD CONDITION EXIT TIMING

Address Driven before CLKOUT1 Low	TENAC1L				15	ns
$\overline{\text{HOLD}}$ Valid after CLKOUT2 High	TDC2HH				-2	ns
$\overline{\text{HOLD}}$ High to $\overline{\text{HOLDA}}$ High	TDHHAH				15	

ELECTRICAL SPECIFICATIONS (continued)

ADC CONTROL TIMING

Tpclk is multiples of TCCL and is configured by the value of bits PCLK(3:0)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
STROBE Cycle Time TSTRBCL		14 • Tpclk			ns
STROBE High Pulse Duration TSTRBW		2 • Tpclk			ns
START Setup Time before STROBE High TSTRTSU		0			ns
STROBE High to Valid SOUT TSTRTSO	Normal mode, Figure 13		13 • Tpclk		ns
START Hold Time after SOUT Strobe TSTRTH		4 • Tpclk		8 • Tpclk	ns
START Low Pulse Duration TSTSRTL		16 • Tpclk			ns
ADC Signal Setup Time before STROBE High TADCSU		0			ns
SOUT Hold Time after SOUT Valid TSOUTH		4 • Tpclk			ns
ADC Signal Hold Time after STROBE High TADCH		4 • Tpclk			ns
SOUT Hold Time TSOUTSU		Tpclk			ns
ADC Valid Signal Cycle Time (auto mode) TSTRCL		13 • Tpclk			ns
SOUT Setup Time (auto mode) TSOSU		Tpclk			ns
SOUT Hold Time (auto mode) TSOH		4 • Tpclk			ns

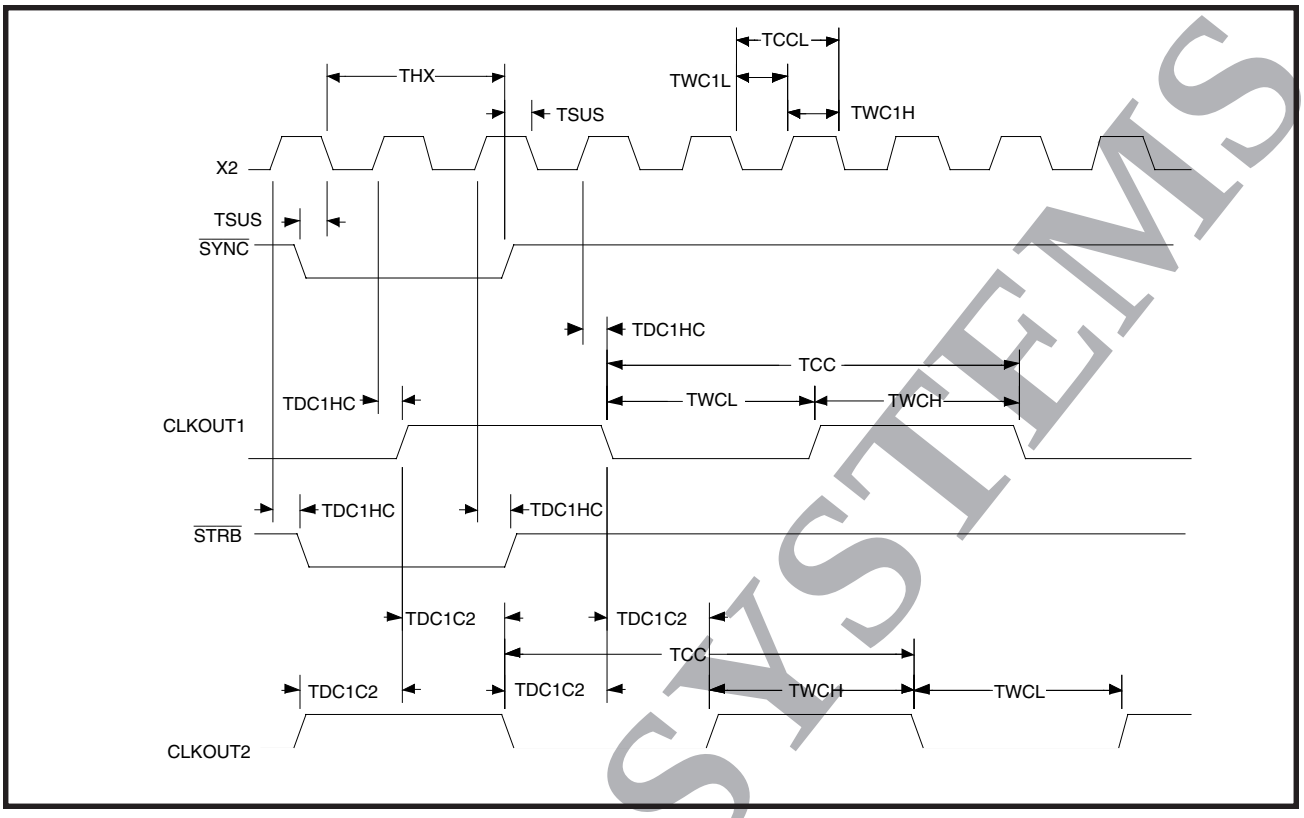


FIGURE 5: Clock Timing Diagram

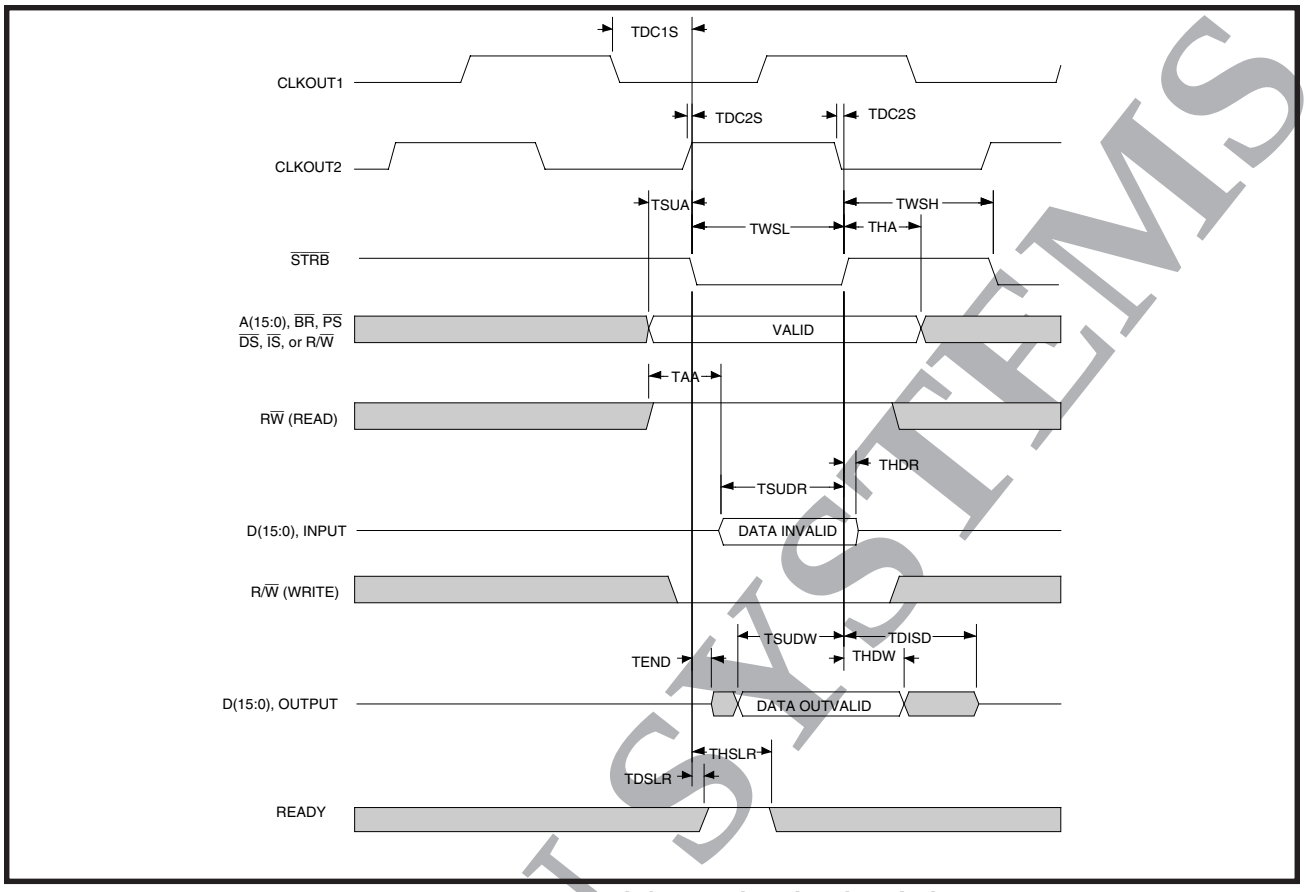


FIGURE 6: Memory and I/O Read and Write Timing

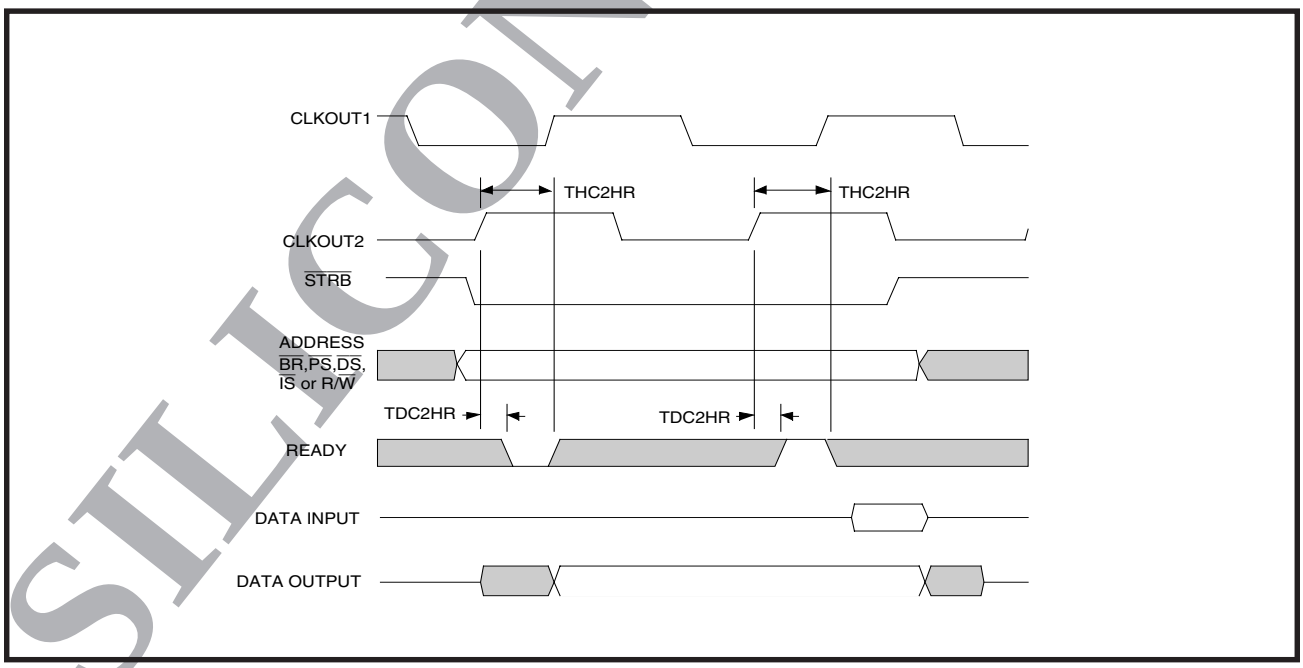


FIGURE 7: One External Wait-State Memory Access Timing

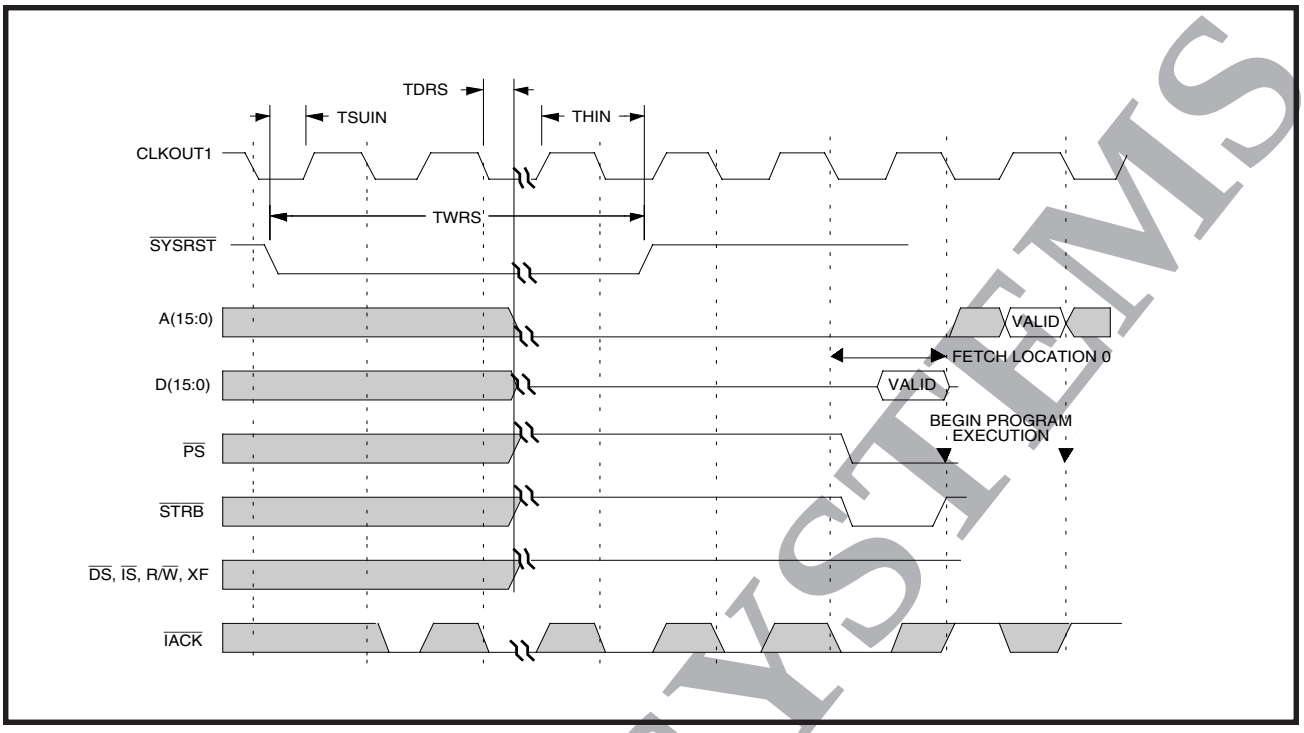


FIGURE 8: Reset Timing

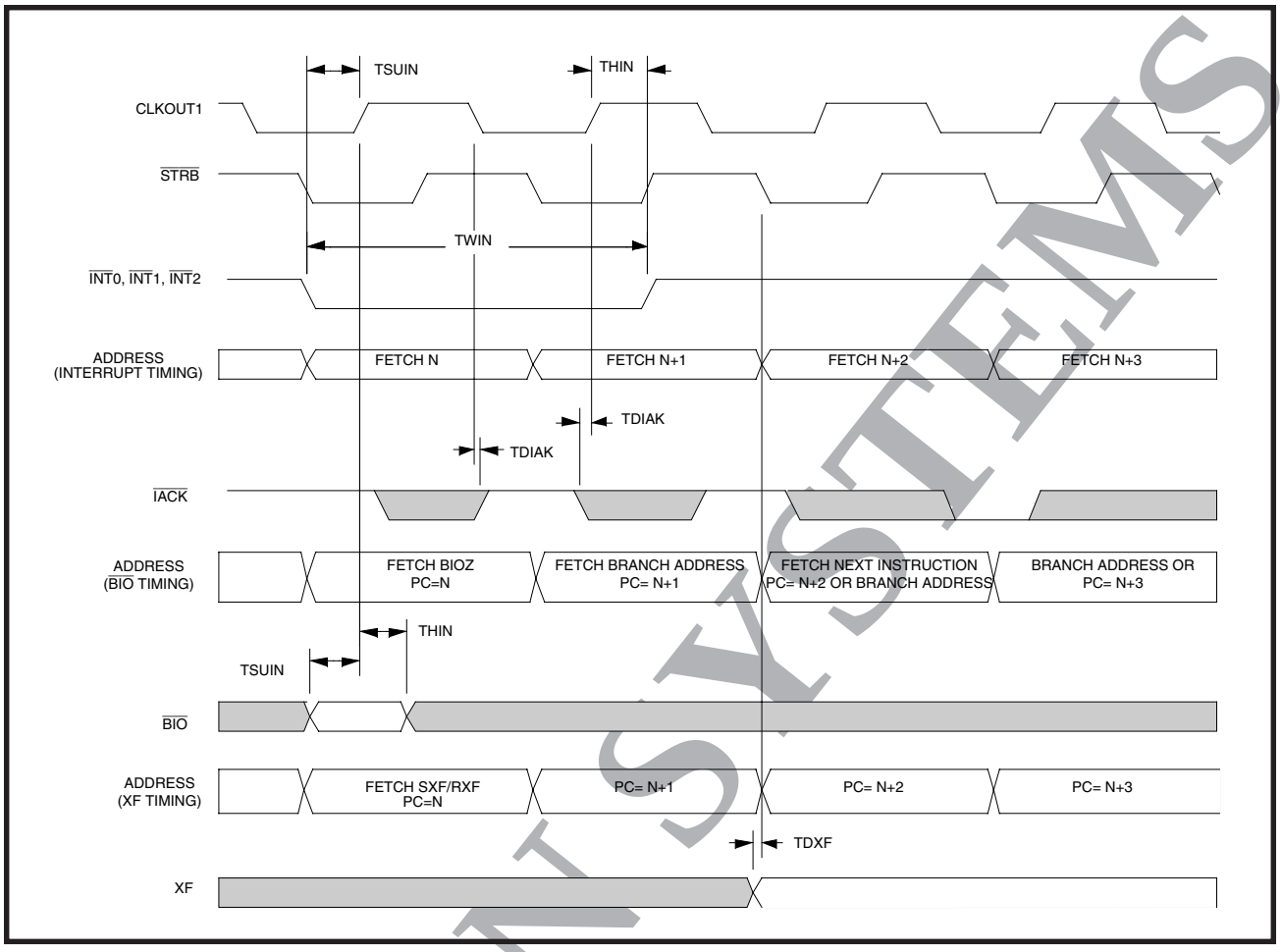


FIGURE 9: Interrupt, BIO, and XF Timing

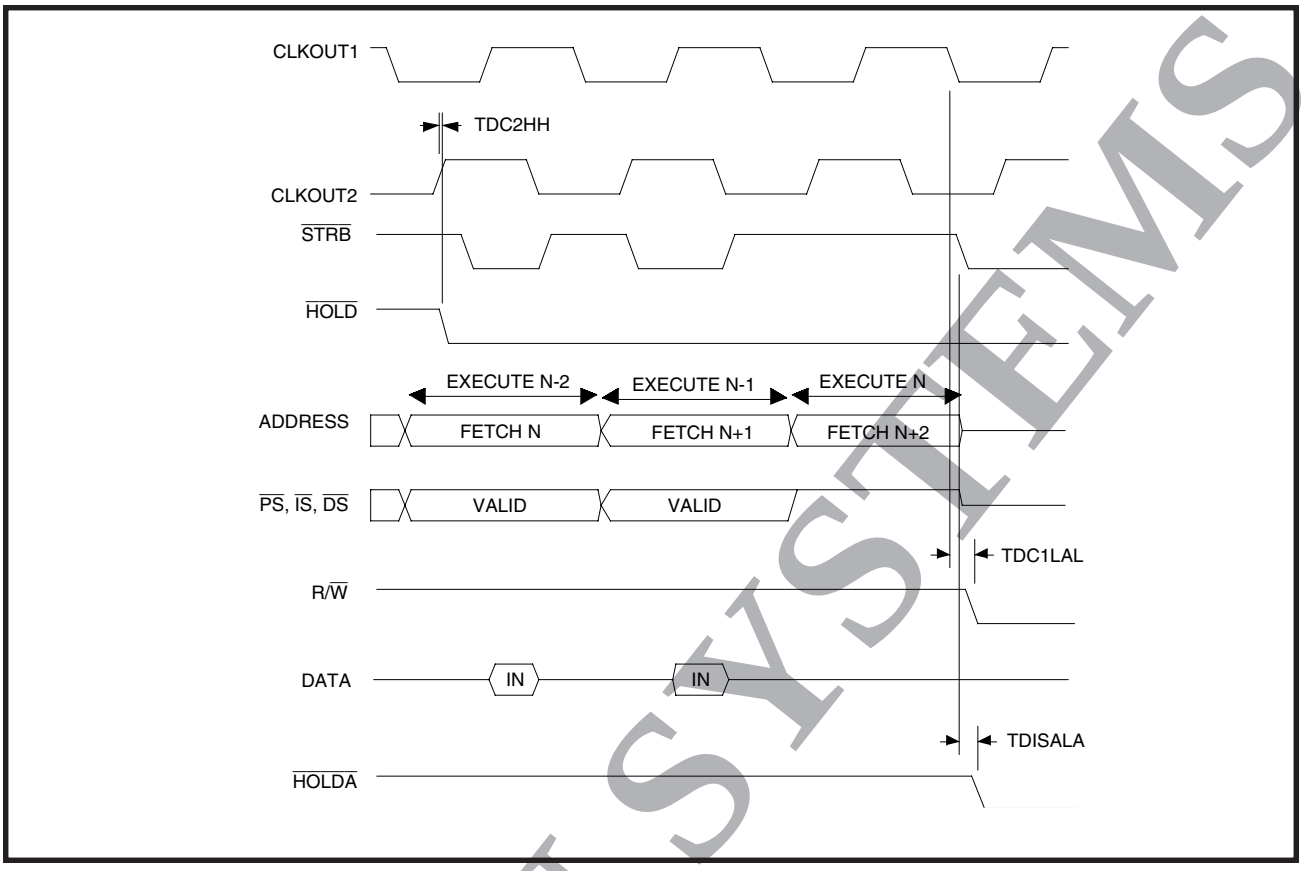


FIGURE 10: Hold Condition Entry Timing

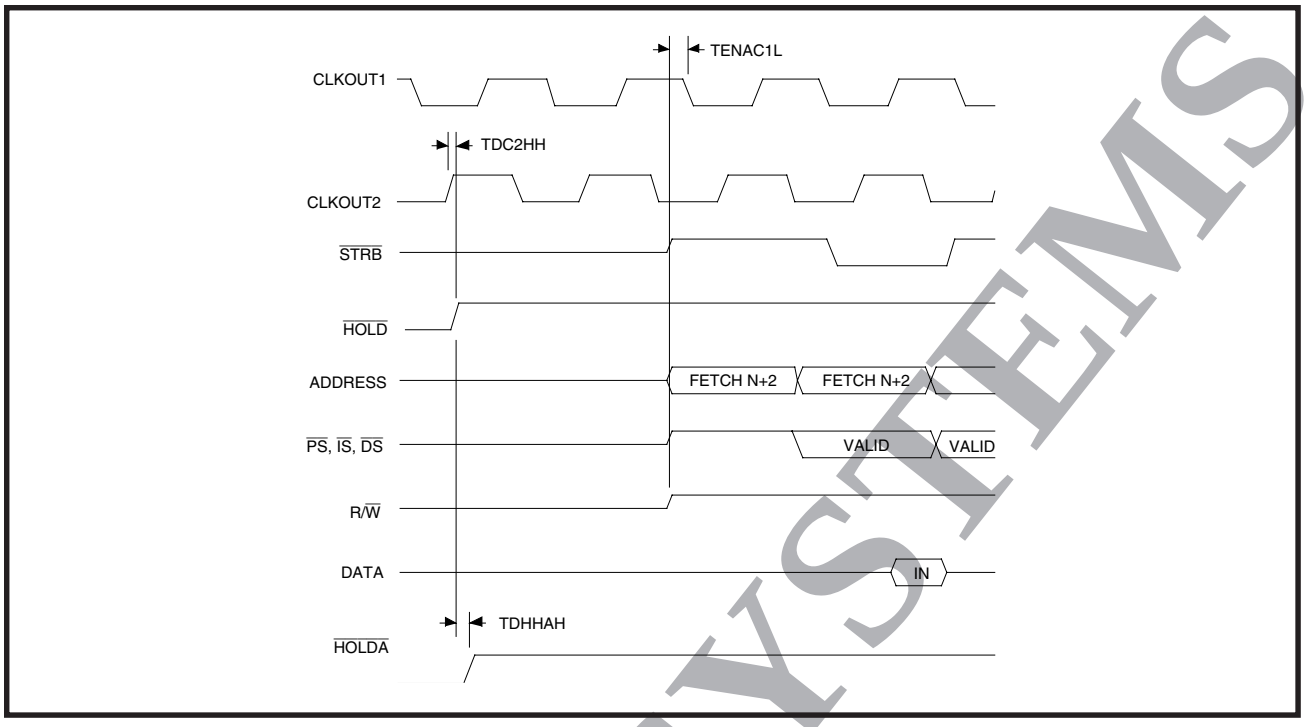


FIGURE 11: Hold Condition Exit Timing

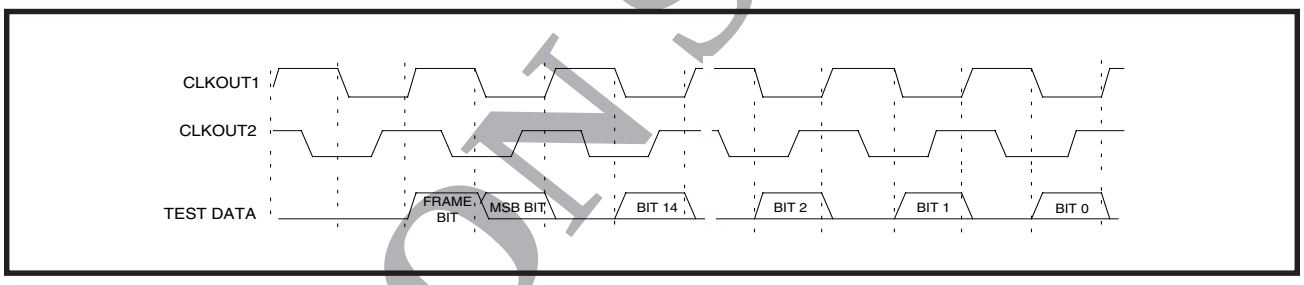


FIGURE 12: Serial Test Pin Timing

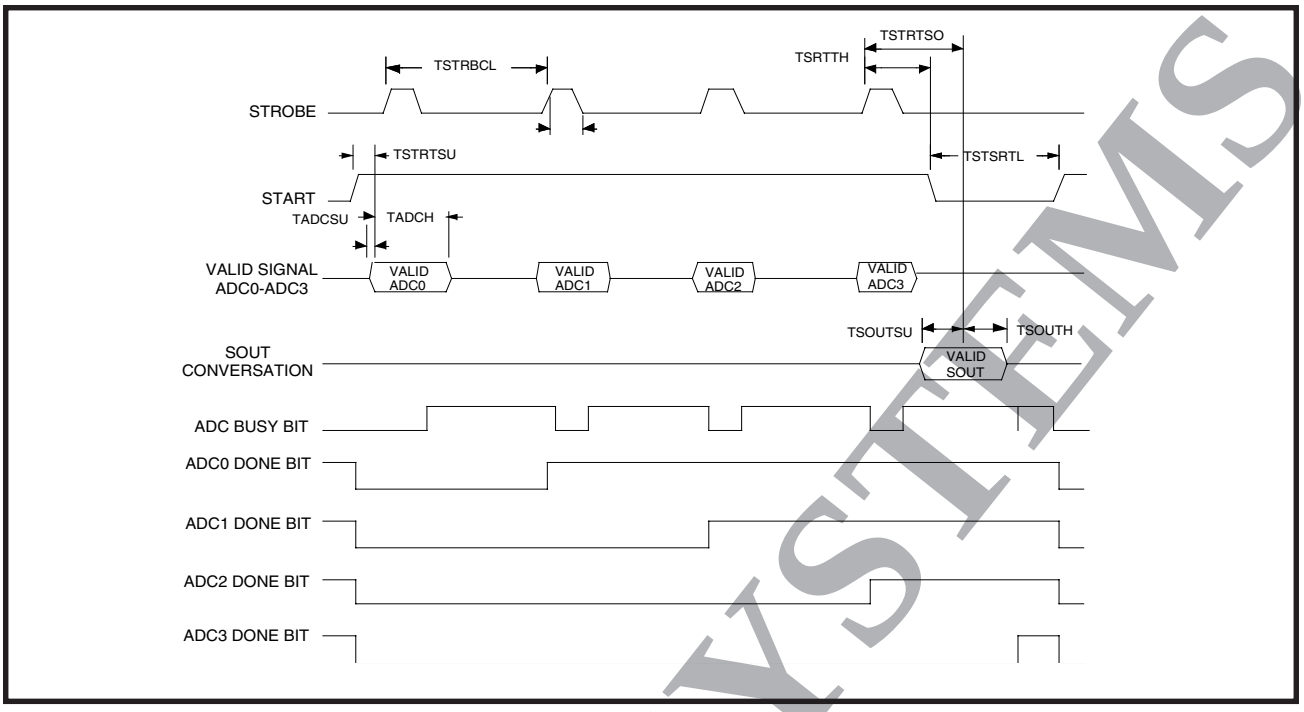


FIGURE 13: ADC Normal Mode Timing

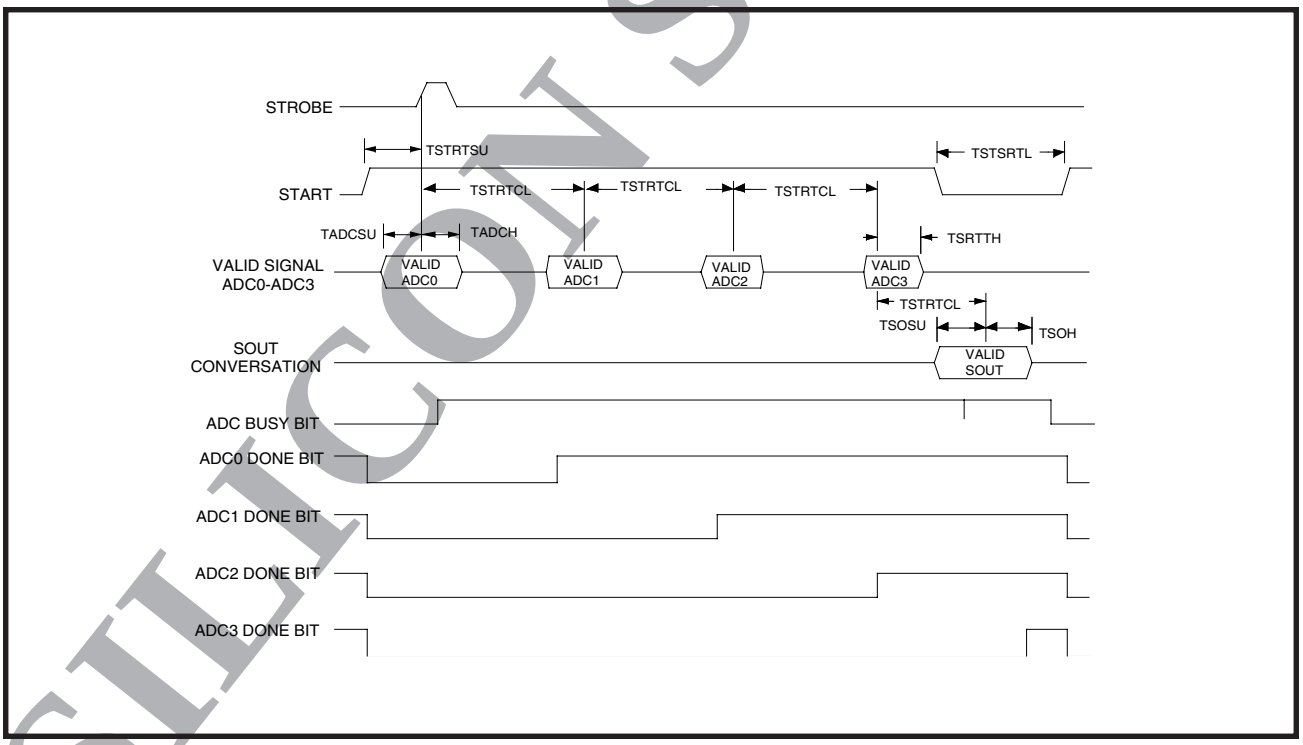
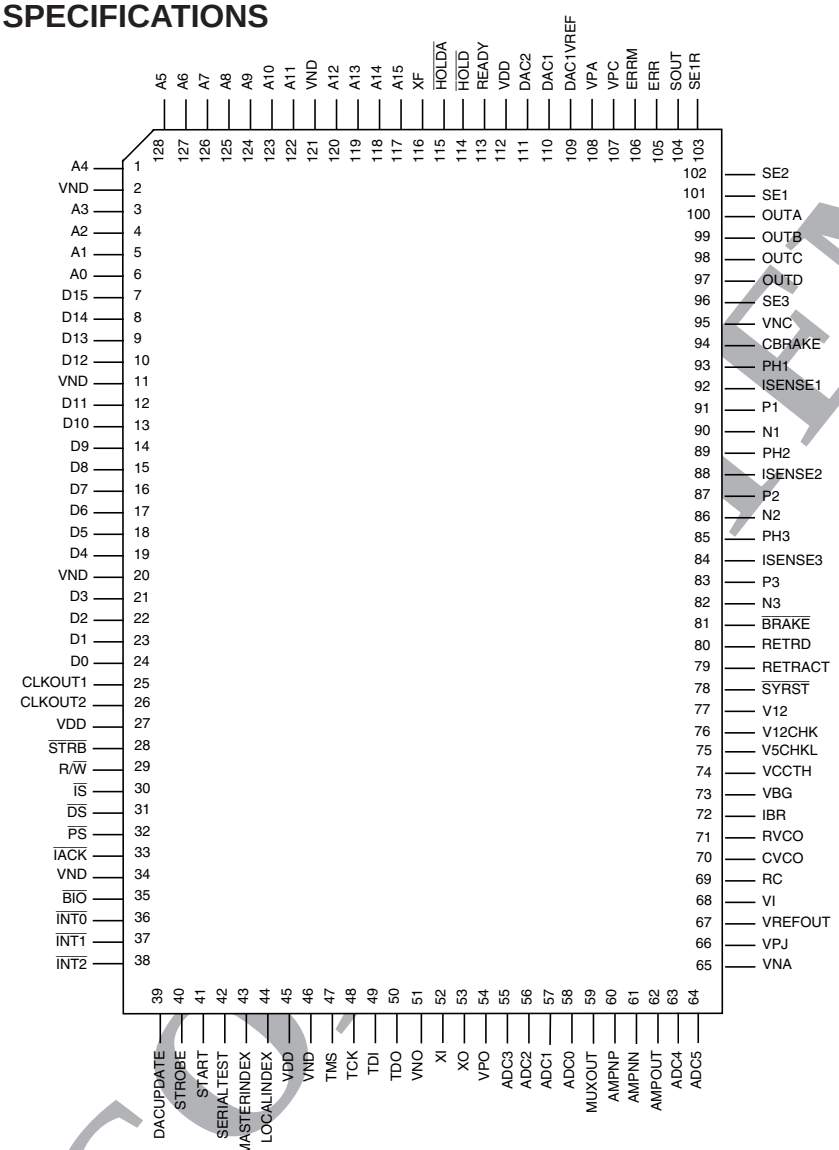


FIGURE 14: ADC Normal-Auto Mode Timing

PACKAGE PIN SPECIFICATIONS

(Top View)



128-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SSI 32H6900
Servo/Spindle Driver

Prototype

December 1996

DESCRIPTION

The SSI 32H6900 servo and spindle driver, a BiCMOS monolithic integrated circuit housed in a 64-Lead TQFP package, operates from +5 V and +12 V supplies. It is designed to drive a voice coil actuator and a 3-phase hall-sensorless motor. Integrated in the device are power MOSFETs. The device is intended for use in 12 V disk drive applications.

FEATURES

VCM DRIVER

- **0.5 A 12 V class AB VCM driver**
- **1.75 Ω max on resistance ($R_{ON\text{-}UP}$ + $R_{ON\text{-}DOWN}$)**

SPINDLE DRIVER

- **1.2 A, 12 V 3-phase motor driver**
- **Internal flyback protection**
- **PWM during run and start**
- **PLL for high jitter immunity**
- **2 Ω max on resistance ($R_{ON\text{-}UP}$ + $R_{ON\text{-}DOWN}$)**
- **Precision internal current sense**

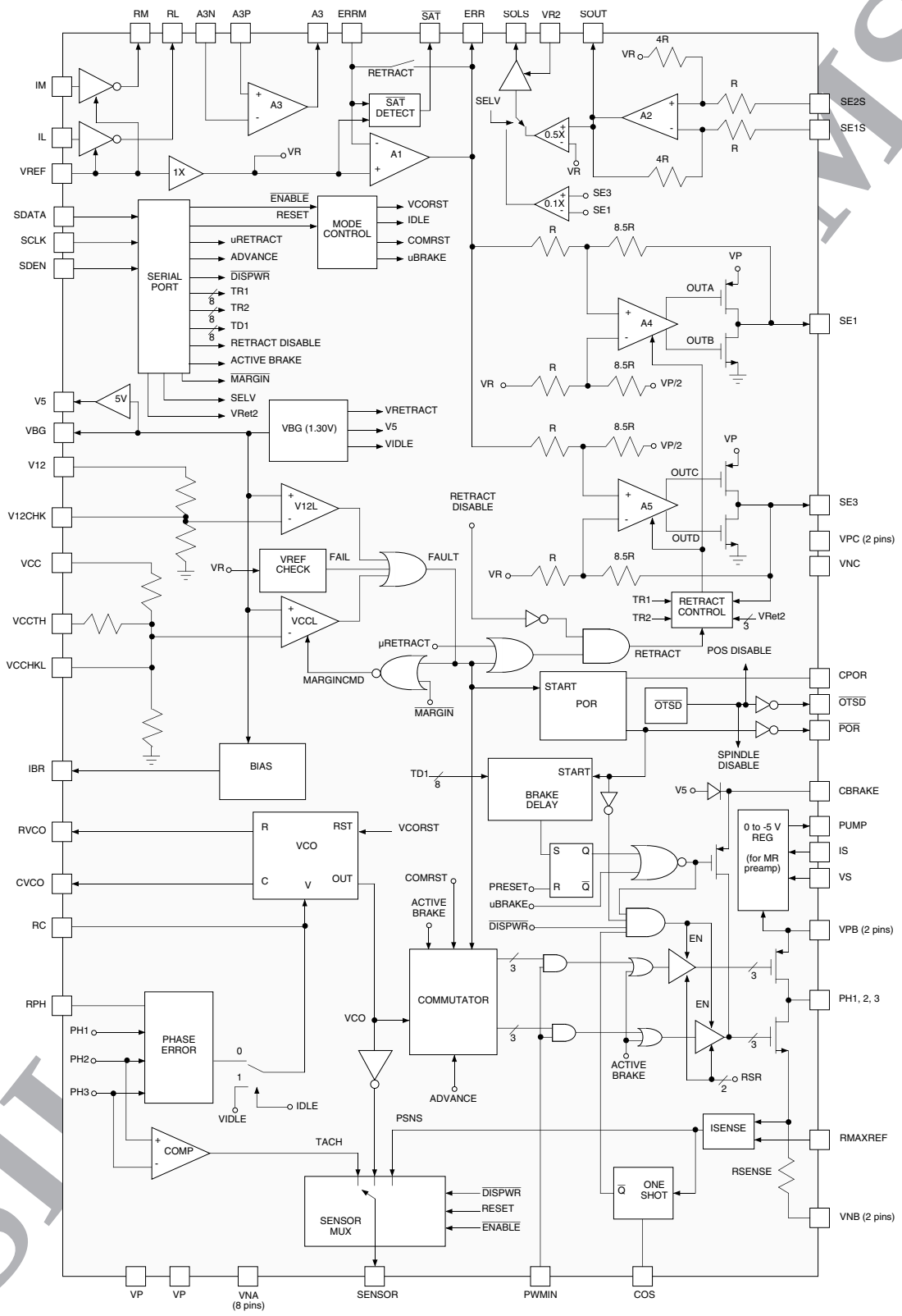
FAULT DETECTION/RETRACT

- **Power-on-reset**
- **5 V and 12 V fault detection**
- **Internal active BEMF rectifiers**
- **Retract amplifier sources and sinks current**
- **Digitally programmable dual level retract voltage**
- **Digitally programmable retract and brake delay timing**

GENERAL

- **64-Lead thermally enhanced TQFP**
- **Bi-directional serial port**
- **OTSD, over temperature protection**
- **Negative power supply for MR preamps**
- **Analog output proportional to junction temperature**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The arrangement of the major blocks contained in the SSI 32H6900 is shown in the block diagram. It is similar to the SSI 32H6829 except all power devices and the spindle current sense devices are internal. The SSI 32H6900 contains an actuator driver with analog or PWM interface, a spindle driver with PLL commutator, and a low voltage monitor with power-on-reset.

ACTUATOR DRIVER

The actuator driver is a class AB design. It has two modes of operation, normal (linear) and retract. The retract mode is activated when a voltage fault is detected or by the uRETRACT bit in the serial interface. Otherwise, the device operates in linear mode. It consists of a 5 V reference, A1 through A6, and a saturation detector. It is functionally similar to the SSI 32H6829.

Loop Compensation Amplifier

During linear operation, the acceleration signal is applied through amplifier A1. RC components may be used to provide loop compensation at this stage. The saturation detector monitors amplifier A1 and indicates when saturation is detected.

MOSFET Power Amplifiers

ERR, the output signal of A1, drives two precision amplifiers, each with a gain of 8.5. The first of these two amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an on-chip complementary MOSFET pair. The second is non-inverting, and is formed similarly from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifier gains to be established precisely. The current sense resistor is connected to SE1 in series with the voice-coil motor which is then connected to SE3.

Retract Function

The SSI 32H6900 incorporates a dual level retract scheme. When retract is initiated, a fixed voltage (level 1) is applied across the actuator to force a constant retract velocity. After an adjustable amount of time, TR1 ms, a higher voltage (level 2) is applied to the actuator for TR2 ms. At the end of level 2, the actuator is floated (i.e., zero current). The timing of the two phases and the increased amplitude during level 2 is set by registers in the serial interface. A third delay, TD1, is the brake delay and ensures the actuator has enough time to retract before the spindle is braked. The retract amplifier of the 32H6900 both sinks and sources current to cause the head to quickly acquire retract velocity regardless of the initial direction of travel. Power for the retract circuit is derived from spindle BEMF by internal active rectifiers which have less voltage overhead than passive diodes and therefore permit higher retract voltages.

Current Sense Amplifier

Actuator current is sensed by a small external series resistor. The voltage drop across this resistor is amplified by A2, a differential amplifier with a gain of 4, whose inputs are SE1S and SE2S. The resulting voltage, SOUT, is proportional to motor current. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired current and the actual motor current. SOUT, referenced to VREF, is also connected to a level-shifter to generate SOLS, which is referenced to VR2.

PWM Inverters

Two PWM inverters powered from VREF are provided to generate power supply insensitive square waves from two pulse width modulation digital data streams. The two outputs may be weighted and summed into a low pass filter constructed with A3.

SPINDLE DRIVER

The spindle driver section monitors spindle back emf and drives a 3-phase spindle motor. It includes current limit, commutator, a phase locked loop to properly phase the commutation times, and a delayed spindle brake circuit. The PWM output drivers include circuitry to minimize inductive flyback spikes and at the same time preserve high switching efficiency.

SPINDLE DRIVER (continued)

Commutator

The commutator drives the spindle motor windings in a proper sequence to operate a 3-phase spindle motor. In "run" mode, the commutator is clocked by the VCO output. In "start" mode, the commutator is clocked by external pulses applied at the ADVANCE bit. Table 1 shows the commutator sequence and identifies which power FETs are on.

TABLE 1: Commutator Sequence

STATE	PH1	PH2	PH3
Com Reset	VPB	VNB	VPB
A	VPB	float	VNB
B	float	VPB	VNB
C	VNB	VPB	float
D	VNB	float	VPB
E	float	VNB	VPB
F	VPB	VNB	float

Phase Error Amplifier

The phase error circuit compares the undriven winding voltage with the average of the other two winding voltages. Depending on the result of the comparison and the state of the commutator, a positive or negative current is applied to the RC pin. Table 2 shows which winding is undriven and the polarity of the output current when that winding is positive with respect to the average of the other two.

TABLE 2: Undriven Winding and Polarity

COMMUTATOR	UNDRIVEN WINDING	POLARITY
A	PH2	Source
B	PH1	Sink
C	PH3	Source
D	PH2	Sink
E	PH1	Source
F	PH3	Sink

The phase error circuit is only used during "run" mode. In all other modes, RC is forced to V_{IDLE}, an internally generated voltage that will cause the VCO to idle at approximately 1/20 of the run rate. The magnitude of the current at RC is the sum of a constant current and a current proportional to the VCO frequency. The constant current value is set by RPH which is biased to 2.4 V nominally. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on CVCO is nominally 2 V. The frequency formula is:

$$F_{VCO} = \frac{V_{RC}}{4\ R_{VCO}\ C_{VCO}}$$

The VCO will be reset whenever $\overline{\text{ENABLE}}$ = high and RESET = low. During VCO reset, the VCO output is forced low. The first VCO clock will occur immediately after the VCO exits reset. This timing relationship is shown in Figure 1.

OUTPUT DRIVERS

The spindle drivers are always in PWM mode, Table 3 illustrates the behavior of the spindle drivers to their inputs. The current to the spindle motor is normally controlled by PWMIN and the current sense one-shot. Voltage is applied to the driven phases (which are selected by the commutator) when PWMIN is high and the one-shot is timed out (low). When PWMIN is low the selected phases are shorted to unless ACTIVE BRAKE is set, in which case all motor windings float. When the one-shot is active (high), all motor windings are floated.

A common way of using the one-shot and PWMIN in is to set the one-shot to trip at the maximum starting current desired, and then to modulate the duty cycle of PWMIN during run. The one-shot is triggered whenever the spindle bridge current exceeds 3400x of RMAXREF current. When the one-shot times out, its output will remain high if the bridge current is still too high. During the time the one-shot output is high, all FETs are turned off. This behavior implements PWM over-current limit, where the peak current is $I_{RMAXREF}$ • 3400 in amps.

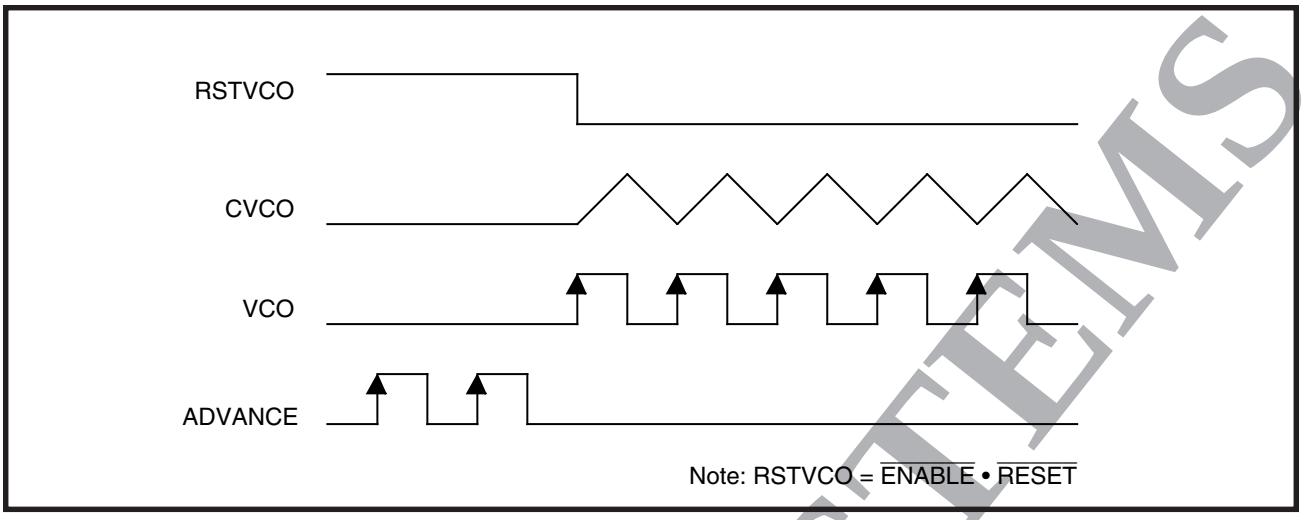


FIGURE 1: VCO Timing Diagram

TABLE 3: Output Driver Behavior

DRIVER INPUT						SPINDLE VOLTAGES (COMMUTATOR IN STATE A)		
PWMIN	ACTIVE BRAKE	ONE-SHOT	$\overline{\text{DISPWR}}$	$\overline{\text{OTSD}}$	BRAKE	PH1	PH2	PH3
1	0	0	1	1	0	VPB	float	VNB
0	0	0	1	1	0	VPB	float	VPB
1	1	0	1	1	0	VNB	float	VPB
0	1	0	1	1	0	float	float	float
X	X	1	1	1	0	float	float	float
X	X	X	0	1	0	float	float	float
X	X	X	X	0	0	float	float	float
X	X	X	X	X	1	VNB	VNB	VNB

TABLE 4: Spindle Modes of Operation

RESET	$\overline{\text{ENABLE}}$	$\overline{\text{DISPWR}}$	MODE	SENSOR	RC	VCO	COMMUTATOR
1	1	X	Preset	$\overline{\text{VCO}}$	V_{IDLE}	Idle	Reset
0	1	X	Start	PSNS	V_{IDLE}	Reset	Run
0	0	1	Run	$\overline{\text{VCO}}$	Run	Run	Run
0	0	0	Coast	TACH	Run	Run	Run
1	0	X	Brake	$\overline{\text{VCO}}$	V_{IDLE}	Idle	Reset

OUTPUT DRIVERS (continued)

$\overline{\text{DISPWR}}$ and $\overline{\text{OTSD}}$ also control the output drivers, when active these inputs cause all three phases to float. On-chip active rectifiers limit the phase voltage to within approximately 300 mV beyond VPB and 300 mV below VNB. In brake mode all three phases are shorted to VNB and $\overline{\text{DISPWR}}$, $\overline{\text{OTSD}}$, PWMIN, and the one-shot are all ignored.

SPINDLE MODES OF OPERATION

The spindle driver modes of operation are governed by the RESET, $\overline{\text{ENABLE}}$, $\overline{\text{DISPWR}}$ and inputs according to Table 4. Spindle braking is activated by power fault or by assertion of the uBrake mode. Spindle braking, if initiated by power fault, is latched until the preset mode is asserted. While spindle braking is activated, $\overline{\text{DISPWR}}$ is ignored. To ensure a known state during system power failure, the serial bits $\overline{\text{DISPWR}}$, ADVANCE, RESET, $\overline{\text{ENABLE}}$, uRETRACT, and MARGIN are initialized to zero. PWMIN is pulled to ground by a 20 kΩ (minimum) resistor.

FAULT DETECTION

Voltage Fault

Precision low voltage monitor circuitry is included to monitor VREF and both supplies, +5 V and +12 V. The circuitry includes a precision voltage reference generator, VCC reset comparator, +12 V reset comparator, and associated logic.

The voltage reference circuit generates a precision voltage reference VBG at 1.3 V. From VBG, it also generates: $V_{RETRACT}$ (nominally 0.82 V), V_{IDLE} (nominally 0.1 V), V_{LIMIT} (nominally 0.1 V), and several other internal voltage and current references.

Both supplies are individually divided down by on-chip resistor dividers and then compared to VBG. The VCC monitor includes a resistor attenuator connected to VCCTH which permits the exact trip point to be externally adjusted if necessary. The threshold voltage of the VCC reset comparator will be pulled to a lower value if $\overline{\text{MARGIN}}$ is asserted while $\overline{\text{POR}}$ is high. This allows the VCC reset comparator to be effectively disabled during power supply margin testing.

POR

When a voltage fault is detected, $\overline{\text{POR}}$ is activated immediately. The retract and braking sequence is then started. If the fault is removed, the $\overline{\text{POR}}$ timer will delay the falling edge of POR for 256 cycles of the POR oscillator. When POR falls, all bits on the serial port will revert to their default values.

Thermal Fault

An $\overline{\text{OTSD}}$ (over-temperature shutdown) circuit is included to help protect the chip from damage during momentary shorts that might occur during prototyping and troubleshooting. The trip temperature is set very high to prevent thermal faults in normal operation. A thermal fault causes all spindle and positioner FETs to be turned off and the $\overline{\text{OTSD}}$ output to be pulled low. A voltage fault overrides a thermal fault and always causes the retract and braking sequence to occur.

SERIAL PORT

The various modes of the SSI 32H6900 are controlled through a synchronous 3-pin bi-directional serial port. The serial port conforms to the Silicon Systems standard convention and is compatible with commonly used microprocessors. The direction is determined by the state of the R/$\overline{\text{W}}$ bit during the transmission preamble and all bits can be read back except ADVANCE which will always read as a float. The serial port includes a counter which inhibits write if less than 16 rising edges are enabled by SDEN. This counter is reset when SDEN is low. The serial port is disabled for both read and write operation during $\overline{\text{POR}}$, the default values for the registers are loaded at power-up and during the interval between the end of $\overline{\text{POR}}$ and the first serial port write.

The serial port is used to input digital data to control registers as defined in Table 6 using the transfer protocol shown in Figure 2 and Table 5, note that timing durations for TR1, TR2 and TD1 assume the $\overline{\text{POR}}$ oscillator frequency is 1/T Hz.

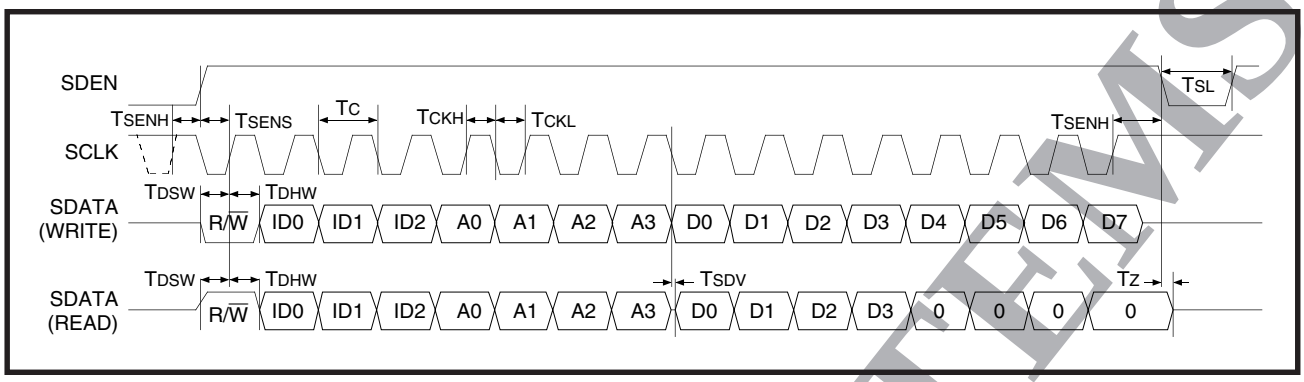


FIGURE 2: Serial Port Timing Diagram

TABLE 5: Data Transfer Preamble

BIT	FUNCTION	DESCRIPTION
0	R/W	Read/Write, 1 = read, 0 = write
1	ID0	Device ID, these three bits define Silicon Systems device for which the serial communication is to be established, '111' is designated for this device.
2	ID1	
3	ID2	
4	ADDR0	Register address, these four bits define the internal register to which the data is transferred.
5	ADDR1	
6	ADDR2	
7	ADDR3	

TABLE 6: Serial Port Bit Assignments

BIT	WORD 0	WORD 1	WORD 2	WORD 3	WORD 4
0	$\overline{\text{ENABLE}}$	TR1-0	TR2-0	TD1-0	VRet2-0
1	RESET	TR1-1	TR2-1	TD1-1	VRet2-1
2	uRETRACT	TR1-2	TR2-2	TD1-2	VRet2-2
3	ADV/FLOAT	TR1-3	TR2-3	TD1-3	MARGIN
4	$\overline{\text{DISPWR}}$	TR1-4	TR2-4	TD1-4	THERM
5	ACTIVE BRAKE	TR1-5	TR2-5	TD1-5	RETRACT DISABLE
6	THERMAL	TR1-6	TR2-6	TD1-6	RSR-0
7	SELV	TR1-7	TR2-7	TD1-7	RSR-1

FUNCTIONAL DESCRIPTION (continued)

NEGATIVE REGULATOR

A block diagram of the negative regulator is shown in Figure 3. This is a constant frequency, self oscillating switching regulator. The negative voltage is adjusted with RN2 and RN1 using the V5 pin as a 5 V reference. The inductor current is sensed by RS, which is typically 1 W. The diode is an inexpensive silicon diode (Schottky is not necessary). A precision 80 mV hysteresis in each comparator, in conjunction with the inductor value, establishes the frequency of the switcher. The VMAX comparator limits the peak inductor current to VMAX/RS. VMAX is nominally 250 mV.

The equations of operation for the regulator are:

$$\text{Period} = L\frac{\text{Vhyst}}{\text{RS}}\left(\frac{1}{|\text{Vout}| + \theta} + \frac{1}{\text{VP}}\right)$$

$$\text{Ipeak} = \text{Iload}\left(1 + \frac{|\text{Vout}| + \theta}{\text{VP}}\right) + \frac{1}{2}\frac{\text{Vhyst}}{\text{RS}}$$

$$\frac{\text{RN2}}{\text{RN1}} = \frac{\text{V5} - \text{IpeakRS}}{|\text{Vout}| + \text{IpeakRS}}$$

$$\text{Rout} = \text{RS}\left(1 + \frac{|\text{Vout}| + \theta}{\text{VP}}\right)\frac{\text{RN1} + \text{RN2}}{\text{RN2}}$$

where:

Period	-	Period of one switching cycle
Vhyst	-	The hysteresis voltage (nominally 80 mV)
RS	-	The sense resistor
|Vout|	-	The desired output voltage of the regulator
q	-	The forward voltage drop of the diode
VP	-	Positive power supply (same as the MSC bridge supply)
Ipeak	-	Peak inductor current
Iload	-	The average current supplied by the negative regulator
IR	-	The peak voltage drop across RS
V5	-	The 5 V reference output (see Pin Description)
Rout	-	The regulator's DC output impedance

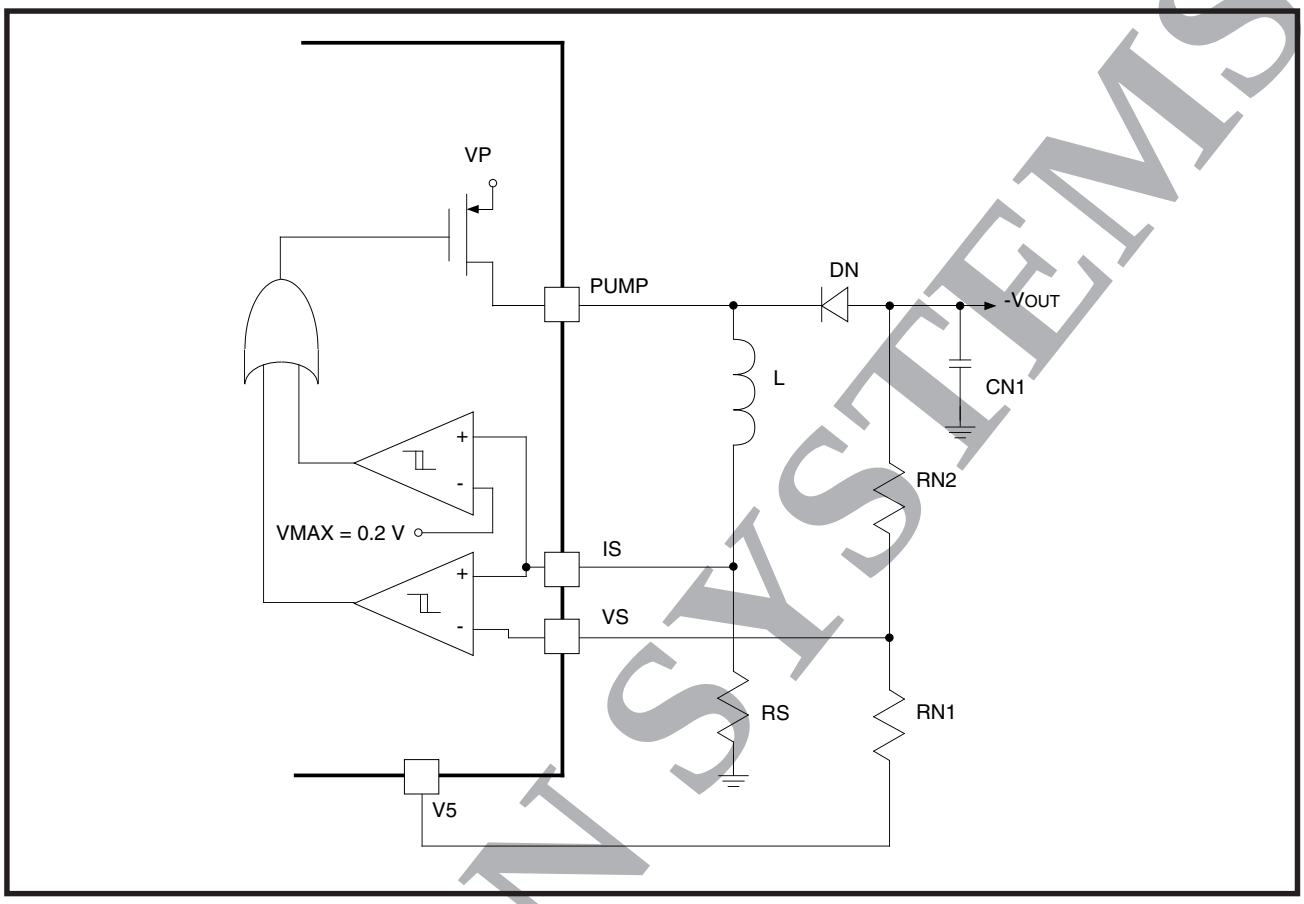


FIGURE 3: Negative Regulator

REGISTER DESCRIPTION

ADDRESS 0

BIT	NAME	DESCRIPTION
0	$\overline{\text{ENABLE}}$	MODE CONTROL: Default is 0 (see Table 3)
1	RESET	MODE CONTROL: Default is 0 (see Table 3)
2	uRETRACT	INITIATES RETRACT: Default is 0
3	ADV/FLOAT	This bit serves dual functions when written, controlling commutator advance and actuator float: 1. If in start mode, the commutation will advance one state whenever a one is written. Advance is reset when SDEN falls. 2. If not in start mode, a one written to this bit will float the actuator by turning the power FETs off. If uRETRACT and float are both asserted, the float condition will be asserted. The default value for this bit is one. When read this register will always report the condition of float.
4	$\overline{\text{DISPWR}}$	Enables the spindle drivers. Brake mode overrides $\overline{\text{DISPWR}}$. Default is 0 (see Table 3).
5	ACTIVE BRAKE	Causes spindle current to be reversed in preset, run, and start modes. This bit is useful in rapidly slowing the spindle motor and is ignored during POR. Default is 0.
6	THERMAL	Connects the input of the THERM buffer to VBG. This permits the offset of the buffer to be calibrated.
7	SELV	SELECT VOLTAGE: When high this bit selects that VCM voltage be selected by the SOLS amplifier. When low, SOUT is selected. Default is 0.

ADDRESS 1

0-7	TR1-0 - TR1-7	LEVEL 1 RETRACT DURATION: 2T • (TR1 + 0.5) - T/4, T is the period of the POR oscillator in seconds. TR1-0 is LSB. Default is TR1 = 100_{10}.

ADDRESS 2

0-7	TR2-0 - TR2-7	LEVEL 2 RETRACT DURATION: T • (TR2 + 0.5), T is the period of the POR oscillator in seconds. TR2-0 is LSB. Default is TR2 = 20_{10}.

ADDRESS 3

0-7	TD1-0 - TD1-7	BRAKE DELAY DURATION: 32T • (TD1 + 0.5) - T/4, T is the period of the POR oscillator in seconds. TD1-0 is LSB. Default is TD1 = 28_{10}.

ADDRESS 4

BIT	NAME	DESCRIPTION
0-2	VRet2-0 - VRet2-2	Amplification factor for level 2 retract, amplitude is level 1 amplitude multiplied by (1 + VRet2 • 0.375). VRet2-0 is LSB. Default is 00.
3	MARGIN	Reduces the VCC fault threshold while $\overline{\text{POR}}$ if off. Default is 0.
4	THERM	Allows VCCTH to output a voltage proportional to junction temperature. Nominally, 2.6 V corresponds to 150° C. Default is 0.
5	RETRACT DISABLE	Inhibits retraction caused by fault, $\overline{\text{OTSD}}$, or uRETRACT.
6-7	RSR-0 - RSR-1	Determines the slew rate at PH1,2,3. The default setting is 00 which corresponds to the slowest slew rate. 11 corresponds to 4X the slowest slew rate and is the recommended value for most applications. RSR-0 is LSB.

PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VNA (8 pins)	Ground	DIGITAL AND ANALOG GROUNDS: The 8 VNA pins are shorted together internally and provide a low thermal path to the chip. Junction temperature can be reduced by connecting them to large metal areas on the PC board.
VNB (2 pins)	Ground	SPINDLE BRIDGE GROUNDS: Must be externally connected to VNA.
VNC	Ground	POSITIONER BRIDGE GROUND: Must be externally connected to VNA.
VPB (2 pins)	Supply	SPINDLE BRIDGE SUPPLIES: Must be externally connected to VP.
VPC (2 pins)	Supply	POSITIONER BRIDGE SUPPLY: Must be externally connected to VP.
VCC	Supply	SYSTEM 5 V POWER SUPPLY: Used by digital I/O circuits.
VP	Supply	The 12 V supply, diode protected from system 12 V. This is must be connected to the bridge supply for the spindle and actuator.

SERIAL PORT

SDATA	DI	BI-DIRECTIONAL SERIAL DATA INPUT
SCLK	DI	SERIAL PORT CLOCK: SDATA is clocked on the rising edge. On-chip parameters are updated after the 16th clock.
SDEN	DI	DATA ENABLE: The SCLK counter is reset while SDEN is low.

NEGATIVE REGULATOR

PUMP	AO	Pulled to VP by the internal switching MOSFET.
IS	AI	CURRENT SENSE INPUT
VS	AI	VOLTAGE SENSE INPUT

ACTUATOR

VREF	AI	ACTUATOR VOLTAGE REFERENCE: All actuator analog signals are referenced to this voltage.
ERRM	AI	POSITION ERROR INVERTING INPUT: Inverting input to the loop compensation amplifier.
ERR	AO	POSITION ERROR: The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor as follows: SE3-SE1 = 17(ERR-VREF)
SOUT	AO	MOTOR CURRENT OUTPUT: This output provides a voltage proportional to the voltage drop across the external sense resistor. SOUT-VREF = 4(SE2S-SE1S)
SOLS	AO	MOTOR CURRENT SENSE OUTPUT: This output provides a voltage proportional to I_{MOTOR} that is level shifted to VR2 as follows: SOLS-VR2 = (SOUT-VREF)/2

ACTUATOR (continued)

NAME	TYPE	DESCRIPTION
VR2	AI	VOLTAGE REFERENCE: The output reference for SOLS.
$\overline{SAT}$	AO	SATURATION DETECT OUTPUT: Active low, with an on-chip 10 kΩ pull-up resistor. It is asserted when the current flowing through the summing node at ERRM exceeds the saturation detector limits.
SE1	AO	SENSE RESISTOR CONNECTION: The gain to this point from ERR is: SE1-VREF = -8.5(ERR-VREF)
SE1S	AI	Current sense input
SE2S	AI	Motor connection and non-inverting input to the current sense differential amplifier.
SE3	AO	MOTOR CONNECTION: This input provides feedback to the non-inverting MOSFET driver amplifier.
V5	AO	The 5 V output to which VREF is to be connected.
RM, RL	AO	PWM INVERTER OUTPUTS: These pins are connected to an external low pass filter network to generate the analog positioner input.
IM, IL	DI	PWM INVERTER INPUTS: These pins are driven by PWM digital waveforms. IL and IM are pulled down with an internal 100 k resistor.
A3P	AI	NON-INVERTING A3 INPUT: Positive input to A3, the uncommitted opamp.
A3N	AI	INVERTING A3 INPUT: Negative input to A3, the uncommitted opamp.
A3	AO	A3 OUTPUT: The output of A3, the uncommitted opamp.

SPINDLE

PH1, 2, 3	AO	The three motor connections.
RMAXREF	AI	SPINDLE CURRENT SENSE: This pin is biased at 1.3 V such that the maximum spindle current is $I_{RMAXREF}$ • 3400 amps.
COS	C	ONE-SHOT CAPACITOR: Sets the time delay in the one-shot. The one-shot is clocked whenever the current in the spindle exceeds a limit controlled by R_{MS}.
PWMIN	DI	PULSE WIDTH MODULATION INPUT: Modulates the N-channel power MOSFETs to control spindle motor current.
SENSOR	DO	DIGITAL MUX OUTPUT: A totem pole output, which is multiplexed from the VCO output, the TACH comparator output and the sense comparator output according to Table 3.
RVCO	C	VCO RESISTOR: Sets the speed range of the VCO. The voltage at RVCO is forced to track RC.
CVCO	C	VCO CAPACITOR: Sets the speed range of the VCO.
RC	C	PLL LOOP FILTER: Sets the time constant for the PLL in “run” mode. In all other modes, it is connected to a DC voltage, V_{IDLE}. V_{IDLE} determines the VCO frequency at which crossover from start to run should occur (by lowering $\overline{ENABLE}$).
RPH	C	PHASE ERROR CURRENT SET: The pump current in the phase error amplifier is the sum of the VCO current (through RVCO) and the current through RPH.

PIN DESCRIPTION (continued)

LOW VOLTAGE MONITOR, OTSD, AND RETRACT

NAME	TYPE	DESCRIPTION
VBG	AO	BANDGAP VOLTAGE OUTPUT: A voltage reference output at 1.3 V. It is used internally as a reference voltage in the low voltage monitor circuitry.
IBR	C	BIAS CURRENT RESISTOR: Biased at VBG, this pin connects to an external current setting resistor.
V12	AI	SYSTEM +12 V SUPPLY: The upper side connection of the resistor divider for +12 V reset comparator.
V12CHK	AI	+12 V RESET COMPARATOR INPUT: The input to the +12 V reset comparator and the connection to a bypass capacitor. V12 is divided down at this pin by an on-chip resistor divider and then compared to VBG. If V12CHK falls below VBG, $\overline{POR}$ is asserted.
VCCTH	C	VCC RESISTOR DIVIDER OUTPUT: The VCCHKL trip point can be adjusted by connecting an external VCC resistor divider to this pin.
VCCHKL	AI	VCC RESET COMPARATOR INPUT: The input to the VCC reset comparator and the connection to a bypass capacitor. If VCCHKL falls below VBG, $\overline{POR}$ is asserted.
CPOR	C	$\overline{POR}$ TIMEBASE CAPACITOR: Determines the frequency of the $\overline{POR}$ timebase which is controls the two retract phase timings, the brake delay, and the POR duration.
$\overline{POR}$	DO	POWER FAULT: Active low, with an on-chip 10 kΩ pull-up resistor. It is asserted when a low voltage condition is detected on either VREF, +5 V, or +12 V supply. After the fault condition is cleared, $\overline{POR}$ will remain low for 256 counts of the POR oscillator.
CBRAKE	C	BRAKE CAPACITOR: A capacitor is connected to CBRAKE to provide pull-up to the N-channel spindle MOSFETs during brake.
$\overline{OTSD}$	DO	OVER TEMPERATURE SHUTDOWN: Active low, with an on-chip 10 kΩ pull-up resistor. It is asserted when the chip temperature exceeds the specified limit. $\overline{OTSD}$ also disables the positioner outputs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability. If multiple ratings are listed for the same parameter they all apply simultaneously.

PARAMETER	RATING
VP	0 to 14 V
|VPC-VP|, |VPB-VP|	0.2 V
|VNC-VNA|, |VNB-VNA|	0.2 V
VCC, IM, IL, RM, RL, VR2, V12CHK, VCCHKL, VCCTH, PWMIN	0 to 7 V
SDATA, SDEN, SCLK, $\overline{POR}$, SENSOR, $\overline{SAT}$, $\overline{OTSD}$	0 to VCC
Current in SE1,SE3	0.5 A
Current in PH1, PH2, PH3	1.2 A
CPOR, RC, RVCO, RPH, CVCO, COS, V5, RMAXREF, VREF	0 to 6 V
VBG, IBR	0 to VP
V12	0 to 15 V
PUMP	-6 to VP
SE1S, SE2S	-2 to VP +2
VS, IS, SOLS, SOUT, ERR, ERRM, A3, A3N, A3P	0 to VP
Storage temperature	-45 to 165° C
Solder temperature - 10 sec duration	260° C

RECOMMENDED OPERATING CONDITIONS

Performance specifications do not apply when the device is operated outside the below recommended conditions.

VP supply voltage	VP	9 V to 13.2 V, 12 V nominal
VCC supply voltage	VCC	4.5 V to 5.5 V, 5 V nominal
Actuator reference voltage	VREF	4.75 to 5.25, 5 V nominal
Bias resistor	IBR	12.7 kΩ to 13.3 kΩ, 13 kΩ nominal
VCO resistor	RVCO	24 kΩ to 26 kΩ, 25 kW nominal
Ambient temperature	Ta	0 to 70° C
V_{RC} voltage range		0 V to 3 V, 2 V nominal
VR2 voltage range		1.8 V to 5.5 V
Pump frequency	f_{PUMP}	300 kHz, maximum

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VP current	$I_{ACTUATOR} = I_{SPINDLE} = 0$			50	mA
VCC current				3.5	mA
V12 current				2	mA
VR2 current	VR2 = 2.493 V SOUT = 2.5 V wrt VREF			0.5	mA
VREF current	SE1 = SE2S = VREF			0.1	mA

ACTUATOR PERFORMANCE SPECIFICATIONS

A1, Loop Compensation Amplifier

Input bias current				100	nA
Input offset voltage				±10	mV
Voltage swing	wrt VREF	±1			V
Load resistance	wrt VREF	10			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB
Retract switch resistance	retract mode, VP ≥ 9 V			1	kΩ

A2, Current Sense Amplifier

Input Impedance	$\overline{SE1S}$	SE2S = VREF	1.5	2.4		kΩ
	$\overline{SE2S}$	SE1S = VREF	3.2	4.2		kΩ
Input offset voltage		SE1S = SE2S = VREF			±3	mV
Output voltage swing		wrt VREF				
	V_{OL}				-3	V
	V_{OH}	VP > 10.3 V	3			V
Common mode range	V_{IL}				-0.2	V
	V_{IH}		VP+0.2			V
Load resistance		wrt VREF	20			kΩ
Load capacitance					100	pF
Output impedance					25	Ω
Gain (SOUT - VREF)/(SE2S - SE1S)		no load	3.9	4	4.1	V/V
Unity gain bandwidth			1			MHz
CMRR			60			dB
PSRR			60			dB

ACTUATOR PERFOMANCE SPECIFICATIONS (continued)

A3 Amplifier

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input bias current					100	nA
Input offset voltage					±10	mV
Output voltage swing	V_{OL}				1	V
	V_{OH}	wrt VP	-2			V
Common mode range	V_{IL}				1	V
	V_{IH}	wrt VP	-3			V
Load resistance		wrt VREF	20			kΩ
Load capacitance					100	pF
Gain			60			dB
Unity gain bandwidth			500			kHz
CMRR			60			dB
PSRR			60			dB

SOLS Output

Output voltage swing	V_{OL}	wrt VR2			-1.5	V
	V_{OH}	wrt VR2	1.5			V
Input offset voltage	SELV = 0				±7	mV
	SELV = 1				±20	mV
CMRR		SELV = 1	50			dB
Common mode input range	Vil	SELV = 1			-0.2	V
	Vih		VP + 0.2			V
Load resistance		wrt VR2	20			kΩ
Load capacitance					100	pF
Output impedance					200	Ω
Gain (SOLS - VR2)/(SOUT - VREF)		SELV = 0	0.4875	0.5	0.5125	V/V
(SOLS - VR2)/(SE3 - SE1)		SELV = 1	0.097	0.1	0.103	V/V

V5 Voltage Reference

Output impedance	I_{OUT} = 0 to 6 mA			20	Ω
Open circuit voltage	I_{OUT} = 0	4.9	5.07	5.25	V
Load capacitance				no limit	F

ACTUATOR PERFORMANCE SPECIFICATIONS (continued)

Saturation Detector

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
$\overline{SAT}$ threshold	|ERR - VREF|	0.8	0.9	1	V
Hysteresis			40		mV

Actuator Drive

Output Voltage Drop VPC - |SE1 - SE3|	I_{LOAD} = ±0.5 A			0.875	V
Slew rate, |SE1 - SE3|	RL = 20 Ω	4			V/µs
Gain (SE3 - SE1)/(ERR - VREF)	RL = 20 Ω	16	17	18	V/V

Actuator Performance
(RIN = 20 kΩ, RL = 20 Ω, LL = 0.6 mH, RC = 180 kΩ, CC = 160 pF)

Distortion THD	100 Hz, 0.1 A peak			2	%

VREF Monitor

VREF fail threshold	VREF falling	2.7	3	3.3	V
Hysteresis			200		mV

PWM Buffers

ROUT--Pch				15	Ω
ROUT--Nch				15	Ω
IL, IM pull-down resistor			100		kΩ

SPINDLE

VCO
(Unless otherwise specified, C_{VCO} = 0.01 µF, R_{VCO} = 25 kΩ)

Typical frequency		$\frac{V_{RC}}{4\,R_{VCO}\,C_{VCO}}$			Hz
Run frequency	V_{RC} = 2 V	1750	1950	2200	Hz
Idle frequency	mode = preset	70		150	Hz
Reset phase error	$V_{RC} = V_{IDLE}$			18	°

SPINDLE (continued)

Phase Error Amplifier
(Unless otherwise specified, Rvco = 25 kΩ, R_{RPH} = ∞)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{RC} (V_{IDLE})		mode = reset		100		mV
Pump current at RC						
Run mode, at start		V_{RC} = V_{IDLE}, R_{RPH} = ∞		4		µA
Run mode, at speed		V_{RC} = 2 V		80		µA
Source/sink current mismatch		V_{RC} = 2 V			5	%
PH1 input offset	State B	PH2 = VP, PH3 = 0	-100		100	mV
	State E	PH2 = 0, PH3 = VP	-100		100	mV
PH2 input offset	State A	PH1 = VP, PH3 = 0 D	-100		100	mV
	State D	PH1 = 0, PH3 = VP D	-100		100	mV
PH3 input offset	State F	PH1 = VP, PH2 = 0	-100		100	mV
	State C	PH1 = 0, PH2 = VP	-100		100	mV
RPH voltage		R_{RPH} = 120 kΩ		2.4		V

Motor Current Control

RMAXREF voltage	RMAXREF = 4.42 kΩ	1.2	1.3	1.4	V
I_{MAX}	RMAXREF = 4.42 kΩ	0.9	1	1.1	A
One-shot off time	C_{OS} = 0.002 µF	10	25	40	µs

Spindle Drive Outputs (PH1, PH2, PH3)

Total voltage drop VP - (PHup - PHdn)	I_{PH} = 1 A			2	V

TACH Comparator

Sensor rising edge threshold	PH2 - PH3	30	100	170	mV
Sensor falling edge threshold	PH3 - PH2	30	100	170	mV

Negative Regulator

Pump on resistance	I = 0.1 A			15	Ω
Comparator offset	VS = 0 V, IS = rising	-10		10	mV
Comparator hysteresis	VS = 0	70		90	mV
VMAX	VS = 0.5 V, IS = rising	230		270	mV
VMAX hysteresis	VS = 0.5 V	70		90	mV
PUMP leakage	PUMP = -6 V			TBD	µA

ELECTRICAL SPECIFICATIONS (continued)

VOLTAGE FAULT MONITOR, POR, RETRACT, BRAKE

VBG Output

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output voltage	No DC load	1.265	1.30	1.335	V
Load capacitance			0.1		µF

Bias

IBR bias voltage		1.25	1.30	1.35	V

VCC Reset Comparator

Trip voltage, regular mode (VCC falling, MARGIN = off)	VCCTH = VCCHKL	4.26	4.35	4.44	V
	VCCTH = 0	4.65	4.76	4.86	V
	VCCTH = VCC	3.54	3.62	3.70	V
Trip voltage reduction	VCC falling, MARGIN = on	10	14	16	%
Hysteresis		28	37	46	mV
Input resistance at VCCTH		120	190	340	kΩ

+12 V Reset Comparator (MARGIN = Off)

Trip voltage	V12 falling	9.20	9.50	9.80	V
Hysteresis		60	80	100	mV
V12CHK input resistance			20		kΩ

POR, Retract, Brake (CPOR = 1200 pF)

Timebase frequency		0.8	1	1.2	kHz
Timebase frequency, test mode		50	100	150	kHz
$\overline{\text{POR}}$ pulse extension past fault		255		256	counts
$\overline{\text{POR}}$ delay from power failure	VP > 9 V			1	µs
Retract voltage, V_{RETR}	level 1, R_L = 20 Ω	0.7	0.82	1	V
CBRAKE current	brake mode, VP = 0, CBRAKE = 5 V			0.2	µA

OTSD (Over Temperature Shutdown)

Trip temperature			150		°C
Hysteresis			5		°C

DIGITAL I/O

Digital Input (PWMIN)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input voltage	V_{IL}		0.8			V
	V_{IH}				2	V
Input bias current	I_{IH}	V_{IN} = 4 V			200	µA
Open circuit voltage					0.4	V

Digital Input (SDATA, SCLK, SDEN)

Input voltage	V_{IL}		VCC/3			V
	V_{IH}				2 • VCC/3	V
Input bias current	I_{IH}	V_{IN} = 4 V			1	µA

Digital Output (SENSOR, SDATA)

Output voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 1 mA	-1			V

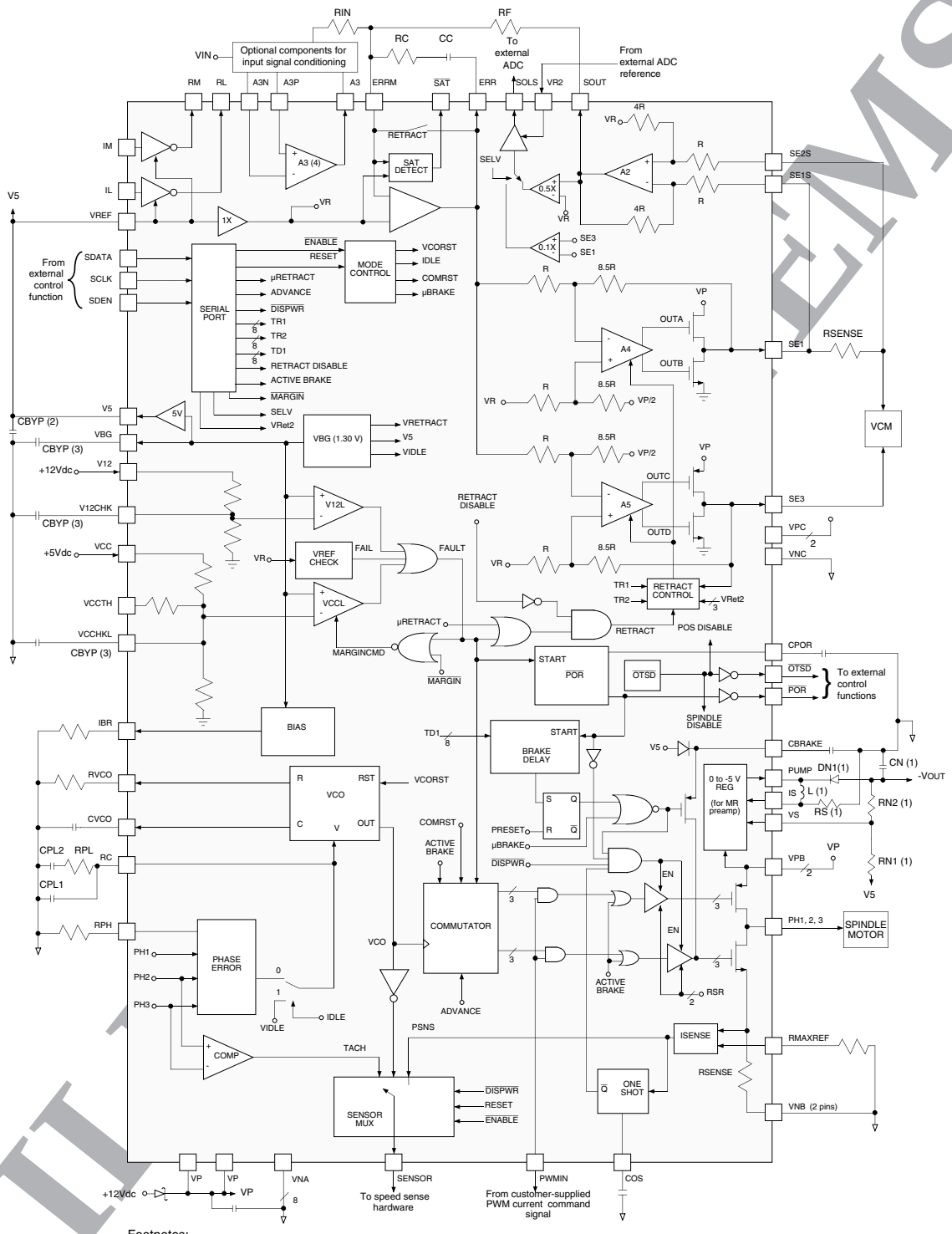
Digital Output ($\overline{SAT}$, $\overline{OTSD}$, $\overline{POR}$)

Output voltage	V_{OL}	I_{SINK} = 8 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-2	-1		V

Serial Port Timing

SDEN set-up time prior to SCLK rise	Tsens		10			ns
SDEN hold time after SCLK rise	Tsenh		10			ns
SDEN low time	Tsl		30			ns
SDATA input set-up time prior to SCLK rise	Tds		10			ns
SDATA input hold time after SCLK rise	Tdh		10			ns
SDATA output delay after SCLK fall, C_L = 20 pF	Tsdv				15	ns
SDATA High-Z delay after SDEN fall	Tz				15	ns
SCLK period	Tc		50			ns
SCLK high pulse width	Tckh		20			ns
SCLK low pulse width	Tckl		20			ns

APPLICATION BLOCK DIAGRAM



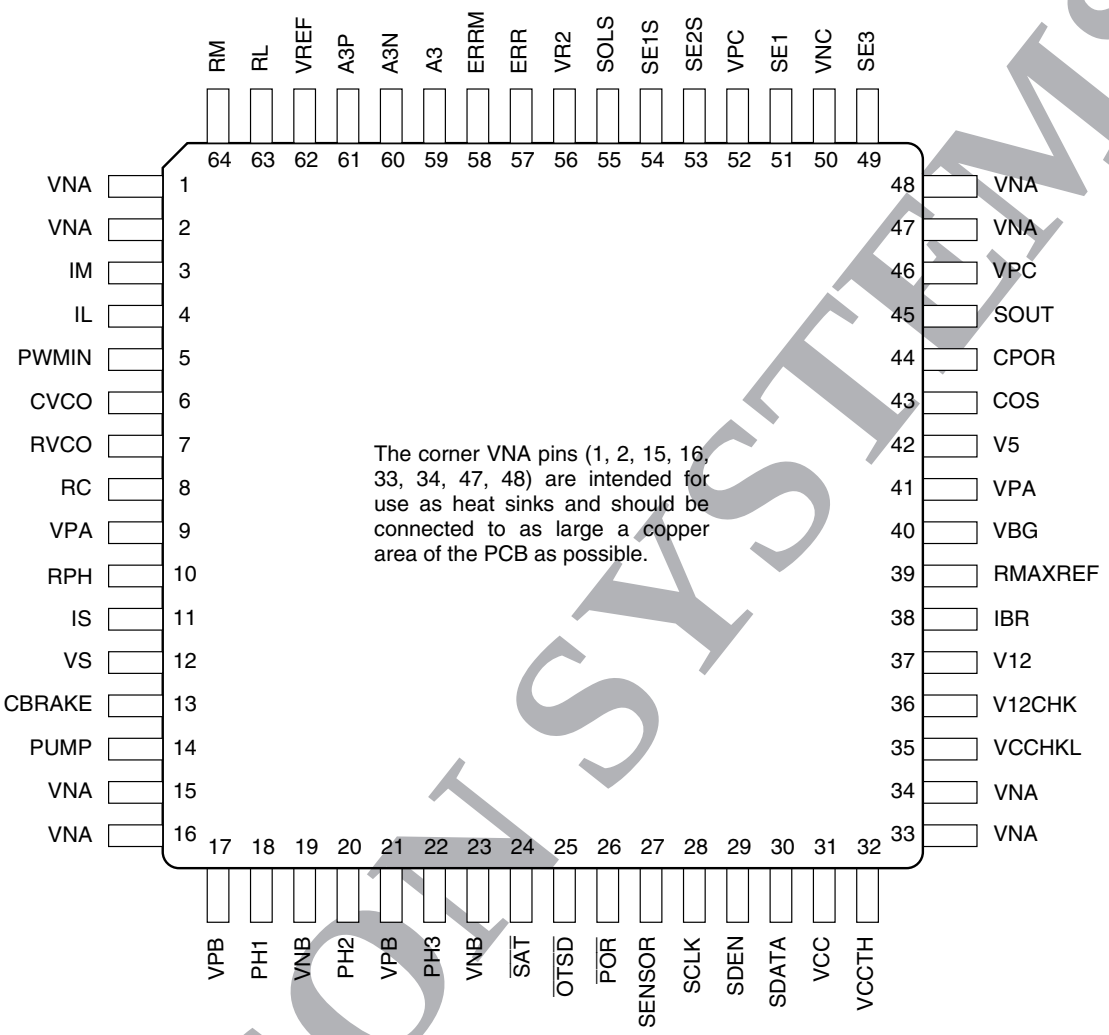
Footnotes:

(1) - denotes an optional component for negative voltage regulator. If not used, connect PUMP pin to +12V and VS and IS pins to VNC

(2) - denotes filter capacitor mounted as close as possible to VREF pin

(3) - denotes optional filter capacitor to improve system noise immunity

PACKAGE PIN DESIGNATIONS



SSI 32H6900
64-Lead Thermally Enhanced TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32H6910
12 V VCM/Spindle Driver

Prototype

April 1999

DESCRIPTION

The SSI 32H6910 is a VCM and spindle motor driver intended for cost-conscious desktop applications up to 4 disks. It is housed in a 64-Pin TQFP deep down-set package that, when installed using recommended mounting techniques, offers <20°C/W thermal resistance to keep the IC cool during motor start.

The VCM section includes a high performance, 14-bit on-chip DAC programmable through the serial port. This provides the user with a complete positioning transconductance amplifier that requires only three external resistors and one external capacitor. By having the entire positioner chain on-chip, sources of offset error are minimized.

A band-gap derived 2.5 V voltage reference is provided for ADC and level shifted current sense amplifier output reference for current monitoring. The VM/2 positioner reference allows the use of the full available power supply in both directions during seek conditions without introducing a CMRR-induced sense amplifier offset at quiescent conditions.

The spindle section allows selectable six-state or SilentSpin™ PWM commutation with synchronous rectification at all times. SilentSpin™ commutation reduces the audible pure tone harmonics of the commutation frequency that are difficult to filter with mechanical means. Synchronous rectification reduces self-heating of the power FETs and eliminates the need for external rectifying diodes. An on-chip 8-bit linear DAC is provided for current control via the serial port.

A bi-directional serial port provides control of all chip functions. Full read-back capability gives the user instant feedback during the debugging process.

FEATURES

VOICE COIL MOTOR DRIVER
- **1.25 Ω total Rdson, Tj = 125°C**
- **1.5 A DC current capability**
- **VM/2 positioner reference**
- **Current sense amplifier output level translator for off-chip ADC support**
- **Serial port programmable retract and VCM float modes**

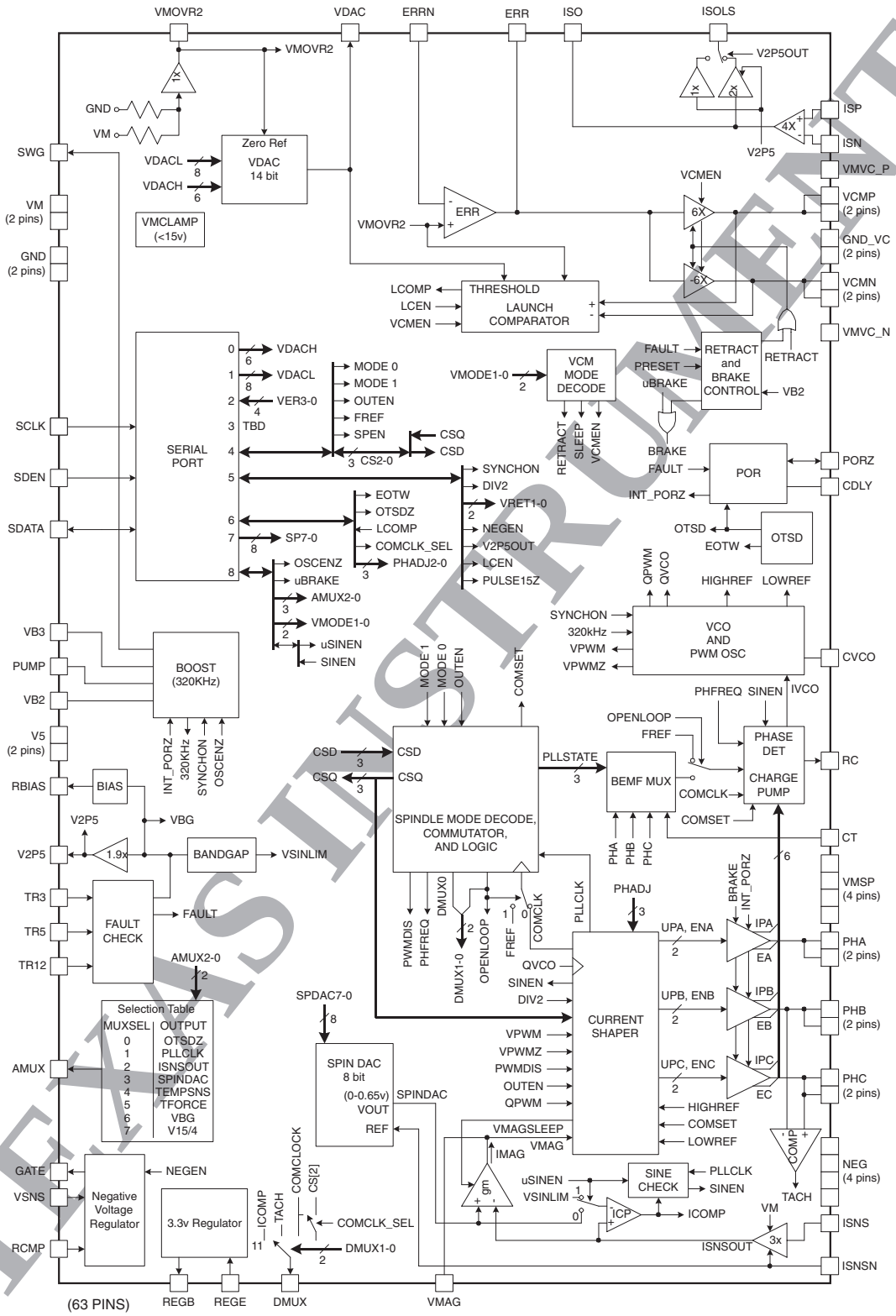
SPINDLE MOTOR DRIVER
- **1.0 Ω total Rdson, Tj = 125°C**
- **2.5 A DC current capability**
- **Current sense comparator for position sense-and-go starting**
- **Serial port readable and writeable spindle motor commutation state**
- **On-chip 8-bit speed control DAC**
- **Six-state PWM start and selectable SilentSpin™ or six-state PWM run**
- **Full time synchronous rectification**

SERIAL PORT INTERFACE
- **25 MHz bi-directional serial port**
- **All mode selection and control functions serial port-programmable**

UTILITY FUNCTIONS
- **Negative voltage regulator for differential MR preamps**
- **+3.3 V voltage regulator**
- **+2.5 V reference for external ADC**

FAULT DETECTION
- **External set-point adjustable 12 V, 5 V, and 3.3 V under voltage detection**
- **Over-temperature warning through serial port bit and shutdown**
- **Power-on reset duration selectable via external capacitor**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The arrangement of the major blocks contained in the SSI 32H6910 is shown in the Block Diagram. The SSI 32H6910 contains an actuator driver, a spindle driver with PLL commutator, a low voltage monitor with power-on reset pulse stretching, and a serial port for interface to common micro-controllers or digital signal processors for all control functions.

ACTUATOR DRIVER

The actuator driver implements a class AB transconductance amplifier using four internal power MOSFETs arranged in an H-bridge configuration. The reference voltage for the amplifier chain is VM/2 to allow full symmetrical use of the available power supply during high velocity seeks. It consists of the VM/2 reference voltage, an error amplifier, an H-bridge power amplifier, and a current sense feedback amplifier. Current command input to the actuator is a voltage centered around VM/2 that swings ±1 V. A launch comparator is available for use in determining VCM velocity by coasting the VCM and measuring back electromotive force (bemf) during head launching. The launch comparator is also useful in calibrating the loop offset and determining the offset shift due to quesient common mode voltage.

There are five modes of operation: sleep, normal (linear), VCM brake, retract, and float. Float mode disables the output while leaving the sense and error amplifier active for calibration purposes. The retract mode is asserted via the serial port by the VMODE bits or in response to a voltage or over-temperature fault. VCM brake mode shorts the VCM through the lower DMOS FETs in order to ensure zero velocity of the VCM by pulling the bemf to zero volts. Linear operation exists whenever the part is not in sleep, retract, or float modes and is used to provide positioning control of the VCM. Table 1 shows the operating mode of the VCM section in response to the digital command bits in the serial port register. Table 2 shows which blocks of the VCM chain are enabled and disabled for each mode of operation.

Loop Compensation Amplifier, ERR

During linear operation, the acceleration signal is applied through amplifier ERR. RC components may be used to provide loop compensation at this stage. Feedback from the current sense amplifier from the ISO output corrects the VCM current to the desired current by the high DC gain of the loop compensation amplifier. The non-inverting input to this amplifier is internally connected to VM/2. Except in sleep mode,

TABLE 1: VCM Digital Input Commands

VMODE0	VMODE1	LCEN	OPERATING MODE	DESCRIPTION
0	0	x	Sleep Mode	Amplifiers are de-biased
0	1	x	Normal Mode	Normal operation
1	0	0	Retract Mode	Retract or VCM brake
1	0	1	VCM Brake	VCM voltage is forced to zero.
1	1	X	Float Mode	Disables output power drivers.

TABLE 2: VCM Modes by Block

MODE	VCMDAC	ERROR, CURRENT SENSE AMPLIFIER, AND VMOVR2 AMPLIFIERS	POWER AMPLIFIER	RETRACT
SLEEP	Disabled	Disabled	Disabled	Disabled
RETRACT	Disabled	Enabled, FBK switch = ON	Disabled	Enabled
VCM Brake	Disabled	Enabled, FBK switch = ON	Disabled	VCM Brake
NORMAL	Enabled	Enabled	Enabled	Disabled
FLOAT	Enabled	Enabled, FBK switch = ON	Disabled	Disabled

Loop Compensation Amplifier, ERR (continued)

whenever the power amplifier is disabled, a feedback switch is turned on, connecting ERRN with ERR and maintaining ERR near VMOVR2.

MOSFET power amplifiers

ERR, the output signal of the error amplifier, drives two precision amplifiers, each with a gain of 6. The first of these two amplifiers is inverting, and is formed from an op-amp, an on-chip resistor divider and an on-chip complementary MOSFET pair, the second is non-inverting, and is formed similarly. Feedback from the MOSFET drains, on sense inputs VCMP and VCMN, allows the amplifier gains to be established precisely. The current sense resistor is connected to VCMP (two pins) in series with the voice-coil motor which is then connected to VCMN (two pins).

Current Sense Amplifier

Actuator current is sensed by a small external series resistor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4, whose inputs are ISP and ISN. ISP is connected at the sense resistor to the side of the sense resistor that connects to the VCMP pins while the ISN pin is connected at the sense resistor to the side that connects to the VCM load. The resulting voltage, ISO, is proportional to motor current. This signal is externally fed back to ERRN, so that the signal ERR represents the difference between the desired current and the actual motor current. ISO, referenced to VM/2, is also connected to a level-shifter to generate ISOLS, which is referenced to V2P5 (2.5 V) for use by an external ADC.

Retract Function

The SSI 32H6910 incorporates a single retract voltage that lasts as long as there is VM voltage available. The voltage level is programmable via the serial port. When retract is initiated, a selected voltage is applied across the actuator to force a constant retract velocity. There are two methods for initiating retract; automatically by power fault detection and via the serial port. When an automatic retraction is signaled by the power fault detection logic a brake delay is applied while retract is occurring that ensures the actuator has enough time to retract before the spindle is braked.

Two bits in the serial port select one of 4 retract voltages: 0.5 V, 0.75 V, 1.0 V, or 1.25 V. The two bits go to a transparent latch powered from the VM supply. These two bits become latched whenever a power fault event has occurred. The transparent latch is how the retract voltage is remembered even if the serial port has reset due to a power fault. When retract is initiated, the selected voltage is applied across the actuator to force a constant retract velocity.

Figure 1 shows the arrangement of the retract section. During retract, amplifiers A1, A2 and A3 are enabled and devices M4 and Q2 are turned on. Also, devices M1 and M2 are turned off. If the voltage across the VCM is less than Vretract, the active loop is Q1 and A1. This attempts to pull the regulated node up to linearly regulate at Vretract. In this case, A2 and M3 are inactive. If the voltage across the VCM is less than Ground, the loop A3 and M3 becomes active also. This attempts to pull up the node to GND by supplying

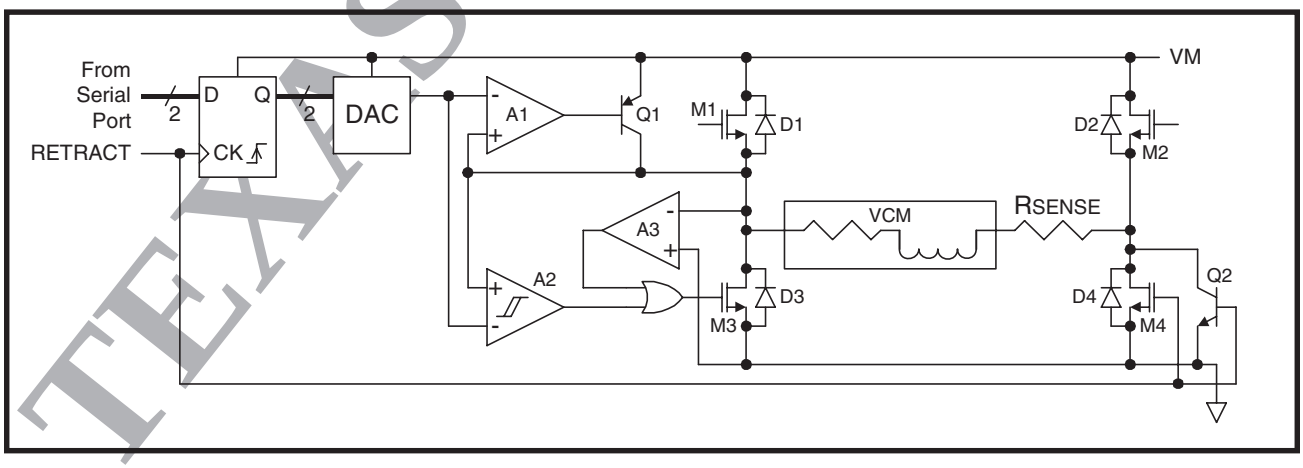


FIGURE 1: Retract Section

current through M3. If the voltage across the VCM is too great the loop A2 and M3 becomes active. If the voltage exceeds Vretract by more than the comparator's hysteresis, it turns on M3. Once the VCM voltage has pulled below the threshold, this turns off. This makes the average voltage at the VCM equal to Vretract, and the coil smooths out the current fluctuations. A1/Q1/A3 are all inactive at this time (except as discussed in Figure 1).

Because of the switching nature of the above circuit, the VCM can pull the drain of M3 below ground. The amplifier A3 causes M3 to become a dynamic rectifier, clamping the VCM flyback at ground. Not shown in the block diagram is a separate low-voltage reference in the retract circuit which provides the 0.5 to 1.25 V retract voltage down to VM = 2 V. The bandgap reference is not used, and does not need to be functional down to VM = 2 V. The A2/M3 loop only functions down to about VM = 4 V. It is thought that by this time, the VCM arm is at least traveling in the right direction if not already done with the Retract operation. The A1/Q1 loop is supposed to remain functional down to VM = 2 V. Additionally, Q2 is supposed to remain on down to VM = 2 V.

14-BIT DAC

A 14-bit, 2's complement linear DAC referenced to VM/2 is provided to allow programming of the desired VCM current through the serial port. The DAC is programmed by writing the most significant 6 bits to the VDACH register (right justified) first. The lower 8 bits of the 14-bit word are then written to the VDACL register as the least significant byte. The DAC will update to the new command word when the VDACL register write is complete.

Launch Comparator

Figure 2 below shows the Launch Comparator subsystem. When the VCM driver is in 'FLOAT' mode, the launch comparator can indicate to the firmware whether the VCM bemf exceeds the value set on the VDAC. When the VCM driver is in 'NORMAL' mode, the launch comparator monitors the VCM voltage and provides information that allows the firmware to find which VDAC command nulls the VCM voltage. The resulting VCM current will depend on the LCOMP offset and the resistance of the VCM. The launch comparator is controlled via the serial port by the VCM MODE[1:0] bits and the LCEN bit and the output is via the LCOMP bit.

VCM Brake

In VCM Brake mode, the two lower VCM DMOS devices are turned on to apply zero volts across the VCM. In this mode, the power amplifiers are disabled and the ERR feedback switch is turned on.

SPINDLE DRIVERS

The spindle driver section monitors spindle bemf and drives a 3-phase spindle motor. It includes current limit, commutator, a phase locked loop to properly phase the commutation times, and a delayed spindle brake circuit. The output drivers include circuitry to minimize inductive fly-back spikes and at the same time preserve high switching efficiency. The PWM frequency is internally generated and can be selected to be synchronous with commutation during run. The PWM duty cycle is based on the error between desired average current, the actual average current and an instantaneous current set-point forming a transconductance amplifier.

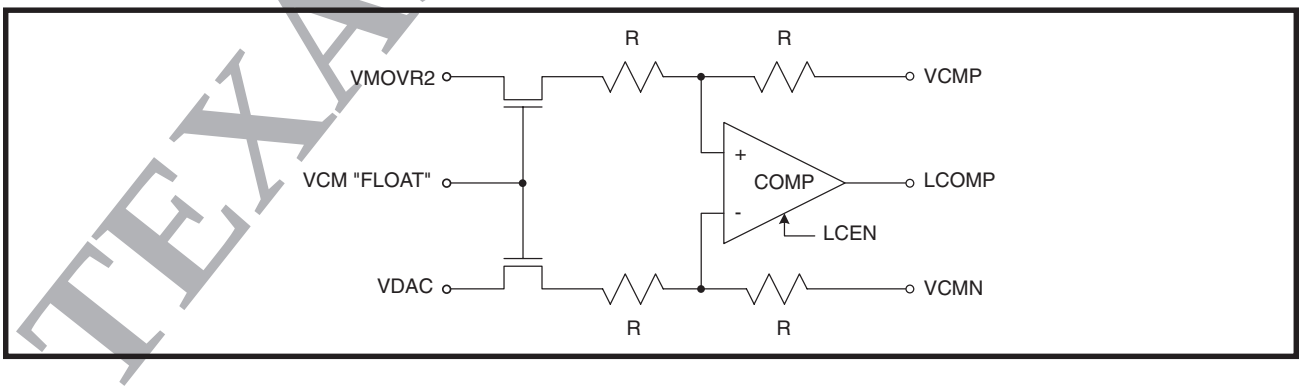


FIGURE 2: Launch Comparator

SPINDLE DRIVERS (continued)

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by CVCO. The voltage swing on CVCO is nominally 2 V. The nominal Vrc voltage at speed in RUN mode is 2.7 V to maximize the dynamic range of the PLL. The frequency formula is:

$$F_{VCO} = \frac{V_{RC} - 0.7}{100k\ C_{VCO}}$$

Commutator

The commutator drives the spindle motor windings in proper sequence to operate a 3-phase spindle motor. In RUN mode, the commutator is clocked by COMCLOCK which is VCO/10 when DIV2 is set to a "0" and VCO/5 when DIV2 is set to a "1." The VCO is phase-locked by the PLL to the bemf of the motor. In START mode, the commutator is clocked by the user toggling the FREF bit in the serial port at some low frequency which the PLL will lock COMCLOCK to and the motor can follow. Table 3 shows the commutator sequence in six-state operation.

TABLE 3: Six-State Commutation Sequence

STATE	PH1	PH2	PH3
A	VMSP	float	NEG
B	float	VMSP	NEG
C	NEG	VMSP	float
D	NEG	float	VMSP
E	float	NEG	VMSP
F	VMSP	NEG	float

TABLE 4: Undriven Winding and Polarity

COMMUTATOR	UNDRIVEN WINDING	POLARITY
A	PH2	Source
B	PH1	Sink
C	PH3	Source
D	PH2	Sink
E	PH1	Source
F	PH3	Sink

SilentSpin™ Commutation

SilentSpin™ works such that at each VCO cycle the desired current set-point is advanced to form a sinusoidal current waveform rather than the well-known sharp-edged six-state pattern of +1, 0, and -1 advanced every COMCLOCK cycle.

Phase Error Amplifier

The phase error circuit compares the undriven winding voltage with the center tap of the spindle motor. Depending on the result of the comparison and the state of the commutator, a positive or negative current is applied to an RC network connected to the RC pin. Component selection criteria and loop stability information can be found in the SSI 32H6910 Applications Note (currently in production). Table 4 shows which winding is undriven and the polarity of the output current when that winding is positive with respect to the center tap.

Depending on the mode of spindle operation, the phase detector operates as a phase-only phase detector which is the best for jitter-free performance during run or as a phase-frequency detector which allows an infinite lock range during motor recovery conditions. The use of the phase-frequency detector requires a clean signal free of false transitions. This condition exists during motor start when FREF is the PLL VCO frequency and when reacquiring phase-lock on a still-spinning motor after a short duration power fault condition. This makes the phase-frequency mode ideal for catching the slowly spinning motor before it stops, shortening the time it takes to recover from the power fault condition. At all other times the phase-only detector must be used to prevent a noisy bemf signal from adversely affecting the PLL.

Output Drivers

The output drivers consist of the on-chip power FETs and the input pre-driver amplifiers necessary to implement PWM six-state or sinusoidal waveshaping and synchronous rectification.

VMAG Loop Operation

An on-chip 8-bit DAC is used to control the average power supply current through the spindle motor. The VMAG loop uses the output of the DAC as a command for the actual current. The current is sensed by a differential amplifier placed across a small value sense resistor that is placed in series with the ground return of the motor. The gain of the differential amplifier is internally fixed at 3X.

A Gm amplifier compares the sensed current to the output of the DAC and outputs a current whose sign and magnitude are proportional to the mismatch between commanded and actual current. This pin is connected to the GND pin via an RC network. Selection of the filter components and other issues related to the operation of an average power supply current command spindle section are covered in the SSI 32H6910 Applications Note (currently in production).

The function of this filter is to convert the current into a analog voltage that forms the PWM duty cycle command to the current shaper block. Thus, the PWM duty cycle adjusts to maintain the commanded current level. This creates a transconductance amplifier that reduces the effect of power supply variations on the spindle system by maintaining a constant Gm over operating conditions.

When the spindle section is in either ISENSE and IMAX modes, the PWM duty cycle is fixed at 100% independent to the magnitude of VMAG. To prevent the accumulation of large VMAG errors during these modes the output of the VMAG Gm amplifier is tri-stated and the magnitude of VMAG will be held constant.

Spindle Modes of Operation

The SSI 32H6910 spindle driver operates in one of eight modes. The modes are selected by MODE1, MODE0 and OUTEN. Table 5 summarizes the internal mode decodes. Table 6 summarizes the behavior of each mode. The spindle driver's eight modes are:

ISENSE — Spindle position sense

In this mode, the user programs the spindle commutation state directly with CS[2:0] and sets the ICOMP threshold with SPDAC[7:0]. The VMAG Gm amplifier is tri-stated to prevent saturation of the loop due to the accumulation errors while the loop is open and the PWM duty cycle is fixed at 100%.

The spindle motor position can be deduced by measuring the current rise times of all six commutation states. This is accomplished by using the ICOMP comparator to setup OUTEN-to-ICOMP toggle delay measurements. ICOMP is monitored at the DMUX output and while voltage drop across the spindle supply current sense resistor is below the threshold set by the SPDAC voltage, the DMUX output will be a logic "0."

During this mode, when ICOMP rises, the FET outputs are immediately disabled and ICOMP is latched. To reset ICOMP and restore operation of the FETs it is necessary to wait until the current falls below the threshold level and assert ICOAST mode by setting OUTEN to a logic zero.

IMAX — Spindle position sense, with current limit disabled

This mode is identical to ISENSE except the power FETs do not turn off automatically when ICOMP rises and ICOMP is not latched. OUTEN must be lowered through the serial port to turn off the power FETs. This mode is used to blank the turn-on transients from the position sense and to free a stuck disk that is not responding to the normal starting ramp.

Spindle Modes of Operation (continued)

ICOAST — Coast mode for IMAX and ISENSE modes

This is the companion COAST mode for ISENSE and IMAX modes and is used to re-enable the ICOMP comparator and restore the operation of the FETs after an ICOMP rise in ISENSE mode.

START — Open-loop ramp up

Before entering START mode from ISENSE, IMAX, or ICOAST, the user should program his desired initial spindle state. In START mode, the commutator will be advanced on rising edges of FREF. The user programs a maximum supply current with SPDAC[7:0] and ramps the frequency of FREF at a rate the motor can follow. In this mode, the PLL will lock the falling edge of COMCLK with the falling edge of FREF, thus preparing the PLL for transition to closed loop RUN mode. COMCLK can be monitored through DMUX to determine if the PLL has locked.

OLCOAST — Open-loop coast

During START, if OUTEN is lowered, the part will enter OLCOAST mode. During this mode, the PH outputs are tri-stated, the PLL continues to lock COMCLK to FREF, and the commutator continues to advance on FREF rising edges. Spindle velocity can be detected by monitoring TACH at DMUX.

RUN — Internal Commutation

In this mode, the commutator ignores FREF and clocks on the rising edge of COMCLK. The phase detector will monitor the polarity of bemf voltage in 6-state operation (SINEN = 0) or motor current in sinusoidal operation (SINEN = 1). If the COMCLKSEL bit is 0, DMUX will output the state of the CS[2] bit which should be in phase with TACH and toggles every third COMCLOCK pulse. Otherwise, it will output COMCLK.

COAST and FCOAST — Coast modes

These two modes are used to determine if the motor is spinning, and to reacquire its commutation phase. The TACH signal at DMUX is measured to determine if the motor is spinning. The PLL acquires commutation phase by monitoring bemf polarity. It uses either the phase-only detector (COAST mode) or the phase-frequency detector (FCOAST mode). The phase-frequency detector has the advantage of infinite capture range and is the preferred mode for reacquiring commutation. The phase-only detector, because of its finite capture range, should only be used in systems where the bemf is too noisy for proper operation of the phase-frequency detector. COAST mode is the default mode of the spindle section at power-up.

Table 6 describes the state of the various functional blocks of the spindle section in each of the spindle section operating modes. The columns of the table and their state during each mode is defined here.

TABLE 5: Spindle Motor Operating Mode Selection

OUTEN	MODE1	MODE0	MODE NAME
1	1	0	IMAX
1	1	1	ISENSE
0	1	1	ICOAST
1	0	1	START
0	0	1	OLCOAST
1	0	0	RUN
0	0	0	COAST
0	1	0	FCOAST

MODE – this column is the selected spindle section operating mode, selected by the OUTEN, MODE0, and MODE1 bits.

COMMUTATOR – this column defines the input or control of the commutator state for each mode. CS[2:0] indicates that the serial port bits directly program the commutation state as defined by Table 8. FREF↑ indicates that the FREF serial port bit advances the commutation state on a rising edge, a logic "0" to logic "1" transition. COMCLK↑ indicates that the commutation state is advanced when the PLL clocks on a rising edge.

PHASE DETECTOR – these three columns, TYPE, REF, INPUT, define the operation of the phase detector of the PLL. An "x" in the first three modes in each column indicates that the PLL is disabled.

TYPE – refers to either the phase-frequency (ph-f) or phase-only (ph) modes of PLL operation.

REF – refers to the reference input of the PLL to which the PLL will align to. In phase-only operation the V(PH) or I(PH) zero crossing is centered in between the input edges. In phase-frequency operation the zero crossing will be aligned with the input edge. In RUN mode when six state operation is enabled the V(PH) is selected as the input to the PLL while in SilentSpin™ operation, I(PH) is used for the PLL input.

INPUT – refers to the comparison input to the PLL. The PLL adjusts the phase and frequency of INPUT to align to REF as described above. COMCLK↑ indicates commutation clock rising edges and define the window in which the PLL will attempt to center the reference edge. COMCLK↓ indicates commutation clock falling edges which are aligned with REF.

RC PUMP – refers to the current pump used to drive the RC pin at the output of the phase detector and input to the VCO. "reset" indicates that the pumps are turned off and the pin is pulled down approximately to DC. "on" indicates that the RC pin is free to be pumped up or down by the output current sources of the phase detector.

DMUX OUTPUT – this column indicates which logic level signal is available at the DMUX output pin. ICOMP is the output of the current sense resistor comparator used for inductive position sense starting algorithms. COMCLK is the commutation advance clock. TACH is the tachometer comparator connected across the PHB and PHC pins. CSQ[2] is the state of the CS[2] serial port bit when read.

POWER AMP – the power amplifier FETs. "on" indicates that the FETs are on and current is available at the spindle phase outputs of the part. "hiZ" indicates the spindle output FETs are tri-stated.

SPDAC CURRENT CONTROL – this column refers to the control of the duty cycle. 100% indicates that the Gm amplifier is tri-stated, the SPDAC level sets the comparison level for the ICOMP comparator, and the duty cycle is internally fixed at 100%. "x" indicates a coast mode is asserted which tri-states the spindle power amplifier outputs and the Gm amplifier. VMAG indicates that the VMAG loop is closed and the Gm amplifier is controlling duty cycle by comparison of the average spindle supply current to the SPDAC command.

TABLE 6: Spindle Mode Details

MODE	COM-MUTATOR	PHASE DETECTOR			RC PUMP	DMUX OUTPUT	POWER AMP	SPDAC CURRENT CONTROL
		TYPE	REF	INPUT				
IMAX	CS[2:0]	x	x	x	reset	ICOMP	on	100%
ISENSE	CS[2:0]	x	x	x	reset	ICOMP	on	100%
ICOAST	CS[2:0]	x	x	x	reset	ICOMP	hiZ	x
START	FREF↑	ph-f	FREF↓	COMCLK↓	on	COMCLK	on	VMAG
OLCOAST	FREF↑	ph-f	FREF↓	COMCLK↓	on	TACH	hiZ	x
RUN	COMCLK↑	ph	V(PH) or I(PH)	COMCLK↑	on	CSQ[2] or COMCLK	on	VMAG
COAST	COMCLK↑	ph	V(PH)	COMCLK↑	on	TACH	hiZ	x
FCOAST	COMCLK↑	ph-f	V(PH)	COMCLK↓	on	TACH	hiZ	x

SPINDLE DRIVERS (continued)

Other Spindle Control Serial Port Bits

The serial port bits µBRAKE, µSINEN, SPEN, SYNCHON, DIV2, PULSE15Z, PHADJ[2:0], CS[2:0], and PHSLOW affect spindle section operation and need to be used properly for optimal performance of the spindle driver.

µBRAKE – setting this bit turns on the dynamic brake of the spindle section. This brake will be held until the bit is cleared or the part is reset.

µSINEN – setting this bit enables SilentSpin™ operation. This is done during RUN mode to reduce the acoustic output of the spindle motor. In IMAX, ISENSE, and COAST modes, the mSINEN bit should be kept at a logic 0, the default state. During SilentSpin™ operation, the PLL monitors phase current and if the peak voltage across the spindle current sense resistor drops below 7 mV the commutator reverts back to six-state operation. SilentSpin™ operation will resume when the supply current again exceeds 7 mV. When this bit is read it reflects the state of the SINEN bit which is an AND of the µSINEN bit and the output of the 7 mV comparator after the first valid COMCLOCK edge. When power is first applied the state of the bit is indeterminate until the the first COMCLOCK edge can clock a flip-flop that stores the legal state of the bit.

COMCLKSEL – during RUN mode, this bit controls whether DMUX ouputs COMCLK or CSQ[2]. When COMCLKSEL is one, COMCLK is output.

SPEN – this bit controls the spindle sleep capability of the SSI 32H6910 and should be set to a "1" to allow normal spindle operation, the motor should already be stopped prior to asserting spindle sleep mode.

SYNCHON – this bit synchronizes the PWM frequency with the spindle commutation and is the preferred method of operating during RUN mode. Synchronization is accomplished by using the VCO output as the PWM modulation reference. SYNCHON should be set to a "1" when approaching final speed and be a "0" for all other conditions.

DIV2 and PULSE15Z – these bits select the PWM-to-Commutation frequency ratio – selecting between 5:1, 10:1, and 15:1. The selection of this ratio depends on the motor speed and the number of motor poles and should be set to the proper value while initializing the part for operation. The correct setting for these bits for several popular motor and speed combinations is shown in Table 7.

The following information is useful in determining the correct setting for the DIV2 bit in applications not shown in Table 6. Given the desired RPM and number of motor poles calculate the commutation rate for COMCLOCK as:

$$Fcomclock = \frac{RPM(Poles \bullet 3)}{60}$$

TABLE 7: Recommended Settings for DIV2 and PULSE15Z

RPM	POLES	PULSE15Z	DIV2	RESULTANT PWM PULSES PER COMSTATE	RESULTANT PWM FREQUENCY
5000	8	0	X	15	30.0 kHz
5400	6	0	X	15	24.3 kHz
	8	0 or 1	X or 0	15 or 10	32.4 kHz or 21.6 kHz
	12	1	0	10	32.4 kHz
7200	6	0 or 1	X or 0	15 or 10	32.4 kHz or 21.6 kHz
	8	1	0	10	28.8 kHz
	12	1	1	5	21.6 kHz
10000	6	1	0	10	30 kHz
	8	1	1	5	20 kHz
	12	1	1	5	30 kHz

To balance motor efficiency while maintaining a PWM frequency above the audio range of the human ear, keep the PWM frequency between 20 to 40 kHz. PWM frequency equals the VCO frequency and is 10X the commutation frequency with DIV2 set to a “0.” Setting DIV2 to a “1” divides PWM rate by 2 if PULSE15Z is a "1" otherwise it is ignored. The user should use the DIV2 setting that gives a PWM frequency within the selection criteria. The phase adjust bits are affected by the selection of DIV2.

PHADJ[2:0] – these bits adjust phase lead during SilentSpin™ operation. In order to properly align motor current with bemf, the motor’s excitation must lead the bemf. The actual phase lead achieved relative to the selection of the PHADJ[2:0] and DIV2 bits are shown in Table 8 below. It is imperative that illegal PHADJ values not be used as they will cause non-operation of the spindle motor.

CS[2:0] – These bits program the state of the commutator when written and when read give the current state of the commutator. The Table 9 shows the states and their representative CS[2:0] word.

PHSLOW – setting this bit reduces the slew rate of PHA, PHB, and PHC outputs by one-half. The default value is a “0” and results in the best efficiency possible. Reducing the slew rate will reduce the efficiency but may allow the user to improve read channel performance if spindle PWM noise is coupling into the read channel.

Typical Spindle Section Operation Sequence

Spindle Section Preparation:

Prior to starting the motor, the serial port bits that govern spindle operation should be set to their values when different from the default states at power-up. Typically this is the time to set DIV2, SPEN, PHADJ[2:0], PULSE15Z, and PHSLOW.

Alignment:

There are two methods of aligning the disk and the commutation state; one which forces the disk to line up with the current commutation state which may include reverse rotation and another which measures the current position of the disk and sets the commutation state to the next one that will prevent reverse rotation. The name applied to the first alignment method is called “Align-and-Go” while the second is called “Sense-and-Go.”

TABLE 8: Phase Adjust Values

PHADJ 2	PHADJ 1	PHADJ 0	PULSE15Z = "1" DIV2 = “0”	PULSE15Z = "1" DIV2 = “1”	PULSE15Z = "0" DIV2 = X
0	0	0	3°	ILLEGAL	2°
0	0	1	6°	ILLEGAL	6°
0	1	0	9°	6°	8°
0	1	1	12°	12°	12°
1	0	0	15°	ILLEGAL	14°
1	0	1	18°	ILLEGAL	18°
1	1	0	21°	18°	20°
1	1	1	24°	24°	24°

TABLE 9: Commutation State Decode

COMMUTATION STATE	CS0	CS1	CS2
A	0	0	0
B	1	0	0
C	1	1	0
D	1	1	1
E	0	1	1
F	0	0	1

Typical Spindle Section Operation Sequence
(continued)

Align-and-Go is the simplest method to apply and has traditionally been used for HDD applications. The part is put into START mode, OUTEN = 1 and the current command is set for the desired start current. The first three states are held longer than the ramp to allow the motor time to break the head-to-disk surface stiction and align with the commutation state. The FREF bit is used to advance the state with the advance occurring on each rising edge of the FREF bit.

Sense-and-Go is used to keep the motor from rotating in the reverse direction to eliminate compressive forces applied to the gimbal while the head is stuck to the disk surface. The current rise time of each state is measured to determine the motor position. The correct first state for rotation in the proper direction is two states beyond the state that exhibited the shortest measured rise time. This technique is patented by Seagate Technology, patent no. 5,569,900.

Begin by preparing the timing measurement and setting the SPDAC to the desired current trip point. Set the spindle mode to IMAX initially to keep turn-on transients from turning off the FETs as they would in ISENSE mode. Note that these same transients will cause ICOMP to toggle prematurely and so the timing measurement should ignore these while in IMAX mode. After the turn-on transients die away, switch from IMAX mode to ISENSE mode. The timing starts from the moment the part is placed in IMAX mode and continues through ISENSE mode until the ICOMP rise is observed. After ICOMP rises the FETs are shut off automatically and operation will resume when OUTEN is lowered and then raised again. The next commutation state is then programmed and the measurement repeated for the next state and all other states for a total of six measured rise times.

Ramping:

Once the commutator is initialized, the motor is started by asserting START mode and ramping the FREF frequency. The motor will begin to spin up open-loop. As long as the frequency ramp of FREF does not exceed the ability of the motor to accelerate, the motor's velocity will follow FREF. During the open loop ramp phase, the OLCOAST mode can be asserted to disable the spindle drivers and monitor the actual frequency of the motor via the TACH output available at the DMUX pin. While FREF ramps up in frequency, the PLL acquires and locks to FREF. To maintain this lock, FREF must continue to be applied when the OLCOAST mode is commanded.

Run:

When the motor has accelerated to the point at which the bemf voltage is sufficient to support internal commutation, the RUN mode is asserted. Commutation will now be controlled by the PLL. The cross-over point is about 1/40th of the run rate.

Braking:

Braking is applied in two ways, automatically in response to a power fault and by setting the µBRAKE bit in the serial port. When a power fault occurs a brake delay is provided based on the discharge of the capacitor attached to the voltage doubler pin, VB2, with respect to the VM supply so that retraction can be completed before braking is applied. Selection criteria for the brake delay capacitor can be found in the SSI 32H6910 Applications Note (currently in production).

Spin Recovery:

When a power fault occurs during run conditions and clears prior to the brake delay elapsing, it is possible to recover PLL lock without performing a complete startup sequence. This is done to decrease the recovery time and requires that the µC or DSP that controls the part be out of reset condition and active to control the recovery. The first thing that must be done is to initialize the serial port spindle configuration bits that have been reset due to the power fault.

Since the part comes up in COAST mode, it is possible that the PLL can be already locked onto the spindle bemf but this is unlikely due to the capture range limitations of the phase-only comparator. It is therefore preferable to put the part in FCOAST mode to use the phase-frequency mode of the PLL to lock to the spindle bemf. Since the bemf waveforms are clean of the switching noise that prevents their use during run, the phase-frequency mode of the PLL is useful for this activity.

PLL lock can be confirmed by polling the commutation state of the part and comparing that with the commutation state just prior to and after a TACH transition which is available at the DMUX output. Alternatively it is possible to calculate the step response of the system and calculate a worst case time to wait until the PLL will be locked.

Spindle BODE Characterization

To support the Bode analysis of the spindle section by use of an analog dynamic signal analyzer, the attenuation between the AMUX pin when selected as SPINDAC and the SPDAC output is designed to be 10 nominal when the VCM is in FLOAT mode. The user then programs the VDAC output with the “clean” compensator output word as the input to the source channel analyzer while the signal source (swept frequency, noise, et. al.) is input to the AMUX pin and the output of the DAC at VMAG is used as the response signal for the analyzer.

Fault Detection

Voltage fault

Precision low voltage monitor circuitry is included to monitor +3.3 V, +5 V, and +12 V supplies. The circuitry includes a precision voltage reference generator, three reset comparators, and associated logic. The voltage reference circuit generates a precision voltage reference VBG at 1.30 V. From VBG, it also generates several other internal voltage and current references. The three system supplies are individually divided down by off-chip resistor dividers and then compared to VBG to determine the set-point of a low voltage condition.

Power-on Reset, POR

When a voltage fault is detected, PORZ is lowered immediately. The retract and braking sequence is then started. If the fault is removed, the POR timer will delay the rising edge of POR based on the charging of the CDLY capacitor. The PORZ pin is pulled low by the internal fault monitoring circuitry to reset the part and external devices connected to the output. The PORZ pin is an open-drain output and can be driven low by external devices to reset the part.

When PORZ falls, all bits on the serial port will revert to their default values except the VRET bits which are kept locally and will be maintained as long as the VM voltage lasts. The latch that holds the VRET values is transparent such that when PORZ is high, the serial port bits reflect the values stored in the serial port register. When PORZ falls, the retract values are latched into the local register and are held. When PORZ goes back high the latch is set to the values of the serial port register which are reset to a “0” by the POR.

Thermal Fault

An OTSD (over-temperature shutdown) circuit is included to help protect the chip from damage during momentary shorts that might occur during prototyping and troubleshooting. The trip temperature is set to 150°C. A thermal fault causes a retract/brake sequence to be applied to the VCM and spindle while the $\overline{\text{OTSD}}$ output will be set low. The status of OTSD is observable on AMUX or at the OTSDZ bit in the serial port.

An Early Over-Temperature Warning (EOTW) is signaled by the EOTW bit in the serial port reading a “1” and its set-point is 25°C less than that of the OTSD to give the user warning prior to the shutdown occurring. The hysteresis of OTSD is such that EOTW will be asserted the entire time that the OTSD shutdown is occurring and will only clear when the over-temperature condition is gone. The status of the EOTW is observable on the EOTW bit in the serial port.

NEGATIVE REGULATOR

A negative regulator is included to provide a negative voltage source for use in MR head pre-amplifiers that require such a voltage. The negative regulator is enabled by writing the NEGEN serial port bit to a “1.” Component selection for this function are described in the SSI 32H6910 Applications Note (currently in production).

3.3 V REGULATOR

A simple external pass element and two resistors allow the generation of a regulated +3.3 V supply suitable for powering external digital logic operating at the reduced voltage. Component selection for this function are described in the SSI 32H6910 Applications Note (currently in production).

VBOOST DOUBLER AND TRIPLER

To allow the use of a stacked NFET power bridge arrangement a tripled and doubled voltage supply is required by the SSI 32H6910. The external diodes do not require any special characteristics and any commonly available switching diodes such as the 1N4148 can be used.

FUNCTIONAL DESCRIPTION (continued)

V2P5 VOLTAGE REFERENCE

The V2P5 output pin is meant to provide a precision voltage reference for use by external circuitry.

VM CLAMP

A clamping circuit is provided which clamps the VM supply voltage at 15 V nominal to eliminate the need for large value, polarized capacitors used to snub voltage transients caused by VCM and spindle motor inductive fly-backs. The operation of the clamp is completely internal to the part and is transparent to the user.

BLOCKING FET CONTROL

To eliminate the need for an expensive external Schotky diode used to isolate the spindle and VCM bridge power supplies from the system +12 V supply to allow the spindle bemf to power VCM retraction, a control output for an external pass FET is provided. This turns on the FET during normal operation and allows the +12 V power supply to provide power to the VCM and spindle bridge. During power fault conditions the pass FET is turned off to prevent the system load from drawing down the spindle bemf.

ANALOG MULTIPLEXER

To provide test visibility into internal analog signals, the AMUX pin is used to multiplex various internal analog signals. Table 9 defines the output signals for each state. In normal operation, AMUX must be set to 000 (OTSDZ) or 001 (PLLCLK). Other positions are for production test and chip evaluation only. Performance specifications do not apply when other positions are selected.

SERIAL PORT

The various functions of the SSI 32H6910 are controlled through a synchronous 3 pin bi-directional serial port. The serial port conforms to the Silicon Systems standard architecture and is compatible with commonly used DSPs and microprocessors. The direction is determined by the state of the R/$\overline{W}$ bit during the transmission preamble. All addresses can be read back except CS[2:0] which programs the commutation state when written. During read back, CS[2:0] is the current commutation state. Data is written or read 8 bits at a time with 8 bits of preamble forming a 16 bit wide transaction for each serial port transaction.

The serial port is disabled for write operation during POR however the serial port may be read at anytime. The default values for the registers are loaded whenever PORZ falls. Note that all default register settings are a “0” except the VRET bits which are maintained locally and will last as long as the VM voltage remains high if written to other than the default value.

The 14-bit VCM DAC command is written in two independent write activities due to the length of the register being limited to 8-bits. Therefore the command is only updated after a complete write of the VDACL register (address 1) which represents the Least Significant Byte of the 14-bit DAC word. After a valid write to the VDACL register the contents of both the VDACL and VDACH registers will be sent to the DAC even if the value of the VDACH register has not changed.

The serial port is used to input digital data to control registers as defined in register map shown in Table 11 using the transfer protocol shown in Figure 3 and Table 10. The device ID for the SSI 32H6910 is “111.” The function of each register bit is described in the REGISTER DESCRIPTION section which follows.

TABLE 9: Analog MUX output selection

SERIAL PORT BITS			
AMUX2	AMUX1	AMUX0	AMUX
0	0	0	OTSDZ
0	0	1	PLLCLK
0	1	0	ISNSOUT
0	1	1	SPINDAC
1	0	0	TEMPSNS
1	0	1	TFORCE
1	1	0	VBG
1	1	1	V15/4

TABLE 10: Data Transfer Preamble

BIT	FUNCTION	DESCRIPTION
0	R/W	Read/Write, 1 = Read, 0 = Write
1	ID0	Device ID, these three bits define SSI device for which the serial communication is to be established, '111' is designated for this device.
2	ID1	
3	ID2	
4	ADDR0	Register Address, these four bits define the internal register to which the data is transferred.
5	ADDR1	
6	ADDR2	
7	ADDR3	

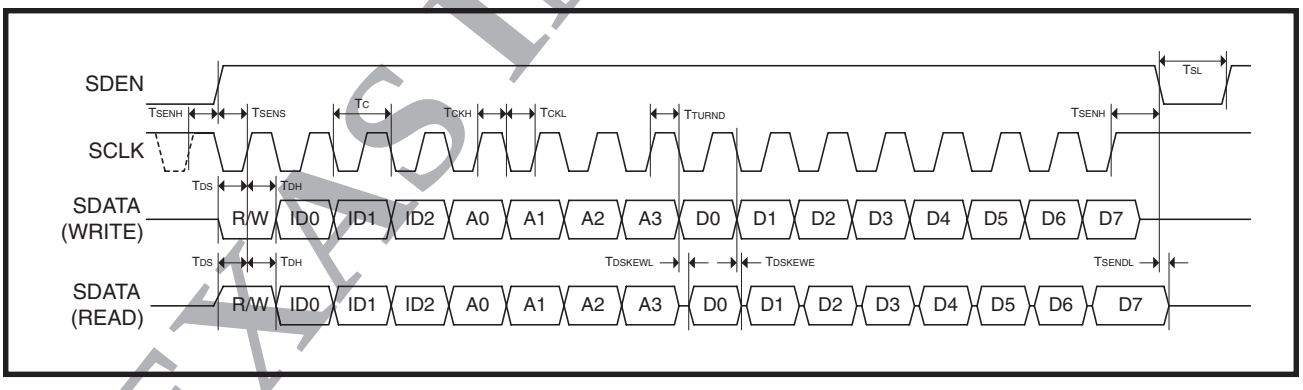


FIGURE 3: Serial Port Timing Diagram

TABLE 11: Serial Port Bit Assignments

BIT	ADDR0	ADDR1	ADDR2	ADDR3	ADDR4	ADDR5	ADDR6	ADDR7	ADDR8
0	VDACH0 (D8)	VDACL0 (D0)	Not Used	Not Used	MODE0	SYNCH ON	EOTW	SPDAC 0	OSCENZ
1	VDACH1 (D9)	VDACL1 (D1)	Not Used	Not Used	MODE1	DIV2	OTSDZ	SPDAC 1	µBRAKE
2	VDACH2 (D10)	VDACL2 (D2)	Not Used	Not Used	OUTEN	VRET0	LCOMP	SPDAC 2	AMUX0
3	VDACH3 (D11)	VDACL3 (D3)	Not Used	Not Used	FREF	VRET1	COMCL K_SEL	SPDAC 3	AMUX1
4	VDACH4 (D12)	VDACL4 (D4)	VER0	Not Used	SPEN	NEGEN	PHSLOW	SPDAC 4	AMUX2
5	VDACH5 (D13)	VDACL5 (D5)	VER1	Not Used	CS0	V2P5 OUT	PHADJ0	SPDAC 5	VMODE0
6	Not Used	VDACL6 (D6)	VER2	Not Used	CS1	LCEN	PHADJ1	SPDAC 6	VMODE1
7	Not Used	VDACL7 (D7)	VER3	Not Used	CS2	PULSE15Z	PHADJ2	SPDAC 7	µSINEN

REGISTER DESCRIPTION

ADDRESS 0 - VCM DAC MOST SIGNIFICANT BYTE

BIT	NAME	DESCRIPTION
0	VDACH0	VDAC D8
1	VDACH1	VDAC D9
2	VDACH2	VDAC D10
3	VDACH3	VDAC D11
4	VDACH4	VDAC D12, Most Significant Bit
5	VDACH5	VDAC D13, Sign Bit
6	Not Used	
7	Not Used	

ADDRESS 1 - VCM DAC LEAST SIGNIFICANT BYTE

0	VDACL0	VDAC D0, Least Significant Bit
1	VDACL1	VDAC D1
2	VDACL2	VDAC D2
3	VDACL3	VDAC D3
4	VDACL4	VDAC D4
5	VDACL5	VDAC D5
6	VDACL6	VDAC D6
7	VDACL7	VDAC D7

DAC updates when LSB register write is complete.

ADDRESS 2 - VERSION

0	Not Used	
1	Not Used	
2	Not Used	
3	Not Used	
4	VER0	Version Information - gives version when read, current SSI 32H6910 version is 1110
5	VER1	
6	VER2	
7	VER3	

ADDRESS 3 - NOT USED

REGISTER DESCRIPTION (continued)

ADDRESS 4 - SPINDLE MODE CONTROL AND COMMUTATION SELECT

BIT	NAME	DESCRIPTION
0	MODE0	Spindle Commutator Mode, selects spindle commutator mode, see selection decode and mode detail information above
1	MODE1	
2	OUTEN	Spindle FET Enable - when asserted spindle power FET amplifiers are enabled, else they are tri-stated
3	FREF	Frequency Reference - the input to the PLL and the commutator clock during START mode
4	SPEN	Spindle Enable - when asserted the spindle section is enabled for operation, else the section is in low current “sleep” mode
5	CS0	Commutation State - when read provides current commutation state (CSQ). When written, asserts desired commutation state (CSD). Note that writing CS bits has no effect when not in IMAX, ISENSE, or ICOAST modes. (See Table 6)
6	CS1	
7	CS2	

ADDRESS 5 -VRETRACT SETTING AND SPINDLE PWM SELECTIONS

0	SYNCHON	Synchronous PWM on - turns on synchronous PWM spindle mode when written to a “1.” See Other Spindle Control Serial Bits section above for detailed description.
1	DIV2	Divide-by-2 - selects 10 PWM cycles per commutation state when written to a “1” or 5 when written to a “0.” See Other Spindle Control Serial Bits section above for detailed description.
2	VRET0	Retract Voltage - sets desired retract voltage level. 00 = 0.50 V, 0.1 = 0.75 V, 10 = 1.00 V, 11 = 1.25 V
3	VRET1	
4	NEGEN	Enable Negative Voltage Regulator - when written to a “1” enables the negative voltage regulator
5	V2P5OUT	Substitutes V2P5 voltage reference for sense amplifier output at ISOLS output when written to a “1” for ADC offset calibration.
6	LCEN	Launch comparator enable. In RETRACT mode, causes VCM Brake.
7	PULSE15Z	In conjunction with DIV2, selects 5, 10, or 15 PWM pulses per comstate when SYNCHON = 1.

ADDRESS 6 - SPINRD: OVER-TEMP INDICATION AND SPINDLE PHASE ADJUST

BIT	NAME	DESCRIPTION
0	EOTW	Early Over-Temperature Warning, indicates maximum junction temperature is approaching
1	OTSDZ	Over-Temperature Shutdown, indicates maximum junction temperature has occurred and the part is in shutdown
2	LCOMP	Read state of launch comparator output
3	COMCLK_SEL	Selects COMCLOCK output from DMUX output during spindle run mode when asserted, else the state of the CS[2] serial port bit
4	PHSLOW	Reduces PHA, PHB, PHC slew rate by 2x
5	PHADJ0	Spindle Motor Phase Adjust - selects the commutation phase adjustment, see Other Spindle Control Serial Port Bits section above for detailed description.
6	PHADJ1	
7	PHADJ2	

ADDRESS 7 - SPDAC: SPINDLE DAC

0	SPDAC0	D0, Spindle DAC LSB
1	SPDAC1	D1
2	SPDAC2	D2
3	SPDAC3	D3
4	SPDAC4	D4
5	SPDAC5	D5
6	SPDAC6	D6
7	SPDAC7	D7, Spindle DAC MSB

ADDRESS 8 - COMND: ANALOG MULTIPLEXOR AND VCM MODE

0	OSCENZ	Oscillator Enable - turns off the boost oscillator when asserted
1	µBRAKE	Processor Brake - places spindle motor in BRAKE mode when asserted
2	AMUX0	Analog MUX Select - selects outputs for analog multiplexor, see table in description above.
3	AMUX1	
4	AMUX2	
5	VMODE0	VCM Mode - Controls operating mode of VCM section, see detailed description above for decode definitions and mode details.
6	VMODE1	
7	µSINEN	Sinusoidal Current Selection - when asserted selects sinusoidal spindle current shaping for acoustic noise reduction otherwise traditional six-state commutation is selected. When read this bit reflects the status of the SINEN bit which is an AND of µSINEN and the output of the 7 mV current sense comparator.

PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output, DIO = Digital Bi-directional Input/Output

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
V5	Supply	System 5 V, 2 pins
VM (2 pins) VMVC_P VMVC_N VMSP (4 pins)	Supply	The +12 V motor supply connections from FET protected system 12 V
GND (2 pins) GND_VC (2 pins)	Ground	Digital, analog, and VCM power supply current returns

SERIAL PORT

SDATA	DIO	Bi-directional serial data input.
SCLK	DI	Serial port clock. SDATA is clocked on the rising edge. On-chip parameters are updated after the 16th clock.
SDEN	DI	Data enable. The SCLK counter is reset while SDEN is low.

ACTUATOR

VDAC	AO	Output from VCM current command DAC
ERRN	AI	Summing junction for ERR amplifier
ERR	AO	Output from ERR amplifier
ISO	AO	Output from current sense amplifier
ISOLS	AO	V2P5 referenced level shifted output from current sense amplifier. Outputs V2P5 (2.5 V) reference when V2P5OUT bit set in serial port and current sense amplifier when bit is cleared
ISN	AI	Inverting Kelvin sense input to current sense amplifier
ISP	AI	Non-inverting Kelvin sense input to current sense amplifier
VCMN	AO	VCM load current connections to VCM load, 2 pins
VCMP	AO	VCM load current connection to sense resistor, 2 pins

SPINDLE

NAME	TYPE	DESCRIPTION
CVCO	C	VCO capacitor connection
RC	C	PLL filter connection
CT	AI	Connection for spindle motor center tap
PHA, PHB, PHC	AO	Spindle motor current connections, 2 pins each phase, 6 pins total.
NEG	AO	Spindle motor bridge negative supply connections, 4 pins, should be connected together and to top of spindle motor current sense resistor
ISNS	AI	Spindle motor current sense resistor connection, should be connected directly to sense resistor
ISNSN	AI	ISENSE resistor Kelvin junction connection directly to bottom (ground) side of spindle motor current sense resistor independent of spindle motor current
VMAG	C	Voltage that represents current error from spindle transconductance loop, a RC filter is connected to this pin to compensate the error correction loop
DMUX	DO	Output from digital MUX for ICOMP, TACH, COMCLOCK, and CS[2] signals.

NEGATIVE REGULATOR

GATE	DO	Controls gating of the switching transistor
VSNS	AI	Voltage sense input of negative regulator
RCMP	C	Compensation component connection

3.3V REGULATOR

REGB	AO	Connection to base of series pass element
REGE	AI	Voltage sense input for 3.3 V regulator

LOW VOLTAGE MONITOR AND POWER-ON RESET

TR3	AI	3.3 V trip comparison voltage, should be connected to a resistor divider from 3.3 V supply such that 1.3 V will be generated at the desired 3.3 V low voltage trip point.
TR5	AI	5 V trip comparison voltage, should be connected to a resistor divider from 5V supply such that 1.3 V will be generated at the desired 5 V low voltage trip point.
TR12	AI	12 V trip comparison voltage, should be connected to a resistor divider from 12 V supply such that 1.3 V will be generated at the desired 12 V low voltage trip point.
PORZ	DO	Power-on Reset, low during voltage fault and for a fixed time afterward. Desired minimum low time is set by selection of CDLY capacitor
CDLY	C	Power-on Reset Capacitor

PIN DESCRIPTION (continued)

CHARGE PUMP AND BIAS

NAME	TYPE	DESCRIPTION
SWG	AO	The control output to the blocking FET used to isolate VM from V12 (system +12 V)
RBIAS	C	Bias Resistor, sets internal bias currents
VB3	C	Tripled boost voltage from charge pump
VB2	C	Doubled boost voltage from charge pump
PUMP	C	Pump node for charge pump

REFERENCE VOLTAGES

V2P5	AO	A band-gap generated 2.5 V reference voltage for external ADC. A bypass capacitor should be connected to this point for best performance
VMOVR2	AO	VM divided by 2, reference voltage for VCM section. A bypass capacitor should be connected to this point for best performance.

ANALOG MULTIPLEXER

AMUX	AO	Analog multiplexor outputs for various internal signals used to test the device and an input for spindle Bode response testing.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability. If multiple ratings are listed for the same parameter they all apply simultaneously.

PARAMETER	RATING
VM (2 pins)	-1 to 15 V
VCMP (2 pins), VMVC_P/N (2 pins), VCMN (2 pins), PHA (2 pins), PHB (2 pins), PHC (2 pins), VMSP (4 pins), NEG (4 pins), ISN, VCMPS, CT	-1 V to VM +1 V
SCLK, SDEN, SDATA, DMUX, CVCO, RC, VMAG	0 to 7 V
ISNS	-0.3 V to VM
ISNSN	-0.3 V to 0.3 V
Total current in PHA (2 pins), PHB (2 pins), PHC (2 pins)	TBD A
Total current in VCMP (2 pins), VCMN (2 pins)	TBD A
VB2, VB3	0 to 30 V
All others	0 to VM
Thermal resistance, junction to case	TBD°C/W
Operating virtual junction temperature	TBD°C
Storage temperature	-45 to 165°C
Solder temperature - 10 sec duration	260°C

RECOMMENDED OPERATING CONDITIONS

Performance specifications do not apply when the device is operated outside the below recommended conditions.

VM supply voltage	VM	9 V to 13.2 V, 12.0 V nominal
V5 supply voltage	V5	4.5 V to 5.5 V, 5.0 V nominal
Total current in PHA, PHB, PHC	Ispm	2.5 A maximum
Total current in VCMP, VCMN	Ivcm	1.5 A maximum
CVCO deviaiton from nominal CVCO (nom) = 20 µ/Fvco	CVCO(nom)	±20%
Bias resistor	IBR	12.7 k to 13.3 k, 13.0 k nominal
Charge pump capacitors	C1 C2 C3 C4	1 µF ±50% 0.1 µF ±50% 0.47 µF ±50% 0.1 µF ±50%

RECOMMENDED OPERATING CONDITIONS (continued)

PARAMETER		RATING
VMOVR2 Output series components Capacitor Resistor		 0.01 µF ± 10% 10 Ω ± 1%
VMAG voltage range	Vvmag	0 V to 3 V, 2 V nominal
Ambient temperature	Ta	0 to 70°C
Vrc voltage range	Vvrc	0 V to 4 V, 2 V nominal

DC CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VM current	$I_{ACTUATOR} = I_{SPINDLE} = 0$			50	mA
V5 current				TBD	mA
VM clamp voltage			15		V

PERFORMANCE SPECIFICATIONS

ACTUATOR

Loop Compensation Amplifier

Open loop gain	DC	60	75		dB
Input offset voltage		-3	0	3	mV
Low side output voltage clamp	No load ± 1 mA	0.30 • VM		0.35 • VM 0.40 • VM	V
High side output voltage clamp	No load ± 1 mA	0.64 • VM 0.60 • VM		0.71 • VM	V
Feedback Switch Resistance	|V(ERR) - VMOVR2| < 0.5V			15	kΩ
Power supply rejection	DC over VM range		TBD		mV
Input common mode range		2		VM-2	V
Unity gain bandwidth	A_{VOL} > 2 @ 1 MHz	2			MHz
Slew rate			±6		V/µS

A2, Current Sense Amplifier

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Closed Loop Gain		3.92	4	4.08	V/V
Output Offset Voltage		-16	0	16	mV
Input Common Mode Range		-1		VM + 1	V
Output Voltage Range	|±1.0 mA| < Io, wrt VMOVR2	-2.5		+2.5	V
Common Mode Rejection	V_{CM} from 0 to VM	-18		+18	mV
Power Supply Rejection	DC		13.2	TBD	mV
Unity Gain Bandwidth		TBD	2		MHz

ISOLS OutpuT (V2P5OUT = “0” unless stated otherwise)

Closed Loop Gain		1.96	2.0	2.04	V/V
Offset (voltage change when V2P5OUT bit is set)	|Iload| = 0, ISO = VMOVR2	-10		10	mV
Output Swing Vol Voh	|Iload| < 1 mA Min() = Minimum of VM-2 or 6 V	 Min()		1	 V V
Output Impedance	|Iload| < 1 mA			10	Ω

14-Bit DAC

Resolution			14		bits
Differential Non-linearity		-0.9		0.9	LSB
Integral Linearity		9			bits
Local Gain Error	Over any 20 codes	-5		5	%
Midscale Offset	Referenced to VMOVR2	-10		10	mV
Conversion Time				5	ms
Full Scale Error		-4		4	%
Output Voltage Swing	wrt VMOVR2	-1		1	V
Maximum Source/Sink Current	wrt VMOVR2	-1		1	mA

VM/2 Voltage Reference

Accuracy	wrt VMOVR2	-50		50	mV
Output Drive		-2		2	mA

ACTUATOR (continued)

Actuator Power amplifiers

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Closed Loop Gain		TBD	6.00	TBD	V/V
Output Offset Voltage		TBD	0	TBD	mV
Unity Gain-Bandwidth			1		MH
Power Supply Rejection		TBD	TBD	TBD	dB
Slew Rate			0.5 to 2		V/µs
Total Voltage Drop	I_{VCMP} = 1.5 A			1.875	V

Launch Comparator

Input Offset Voltage	FLOAT mode	-20		20	mV
	NORMAL mode	-10		10	mV
Hysteresis			0		V
Maximum Bemf Detected	FLOAT mode	0.95		1.05	V
Minimum Bemf Detected	FLOAT mode	-1.05		-0.95	V

VCM Retract

Retract Levels	VRET = 11* VRET = 10* VRET = 01* VRET = 00*	1.06 0.85 0.64 0.42	1.25 1.00 0.75 0.50	1.44 1.15 0.86 0.58	V V V V
Minimum VM to maintain bipolar retract.		5			V
Minimum VM to maintain unipolar retract.		2			V

* - IVCM = current sourced from VCMP to VCMN. For this test IVCM = ± 100 mA. Retract voltage is measured at VCMP with respect to VCMN.

SPINDLE

VCO (Unless otherwise specified, Cvco = 670 pF)

Typical Frequency (Fvco)		$\frac{V_{RC} - 0.7}{100k\ C_{VCO}}$			Hz
Run Frequency	V_{RC} = 2.7 V, T_A = 25°C		30		kHz
Gain		10	15	20	kHz/V
Charge/Discharge Current Mismatch		-10		+10	%

Phase Error Amplifier (Unless otherwise specified, Cvco = 670 pF)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Pump Current at RC		3u + (4Cvco Fvco)			A
Pump Current Deviation from Formula	Fvco = 0 Fvco = 30 kHz			2 8	µA µA
Source/Sink Current Mismatch	Vrc = 2.7 V	-5		5	%
PH Input Offset PHA	RUN or COAST mode	-10		10	mV
PHB		-10		10	mV
PHC		-10		10	mV
PHA, PHB, PHC Matching Offset		-7		7	mV
PH Input Hysteresis PHA	FCOAST mode		50		mV
PHB			50		mV
PHC			50		mV
PH Current Offset. PHA, high side	RUN mode, SINEN = 1	-25		25	mA
PHA, low side		-25		25	mA
PHB, high side		-25		25	mA
PHB, low side		-25		25	mA
PHC, high side		-25		25	mA
PHC, low side		-25		25	mA

Motor Current Control

Zero Current Code	Extrapolated from: SPDAC = 07FH to SPDAC = 01FH	0		20	LSB
Voltage Gain: $\frac{\Delta(ISNS - ISNSN)}{\Delta SPDAC}$	Extrapolated from: SPDAC = 07FH to SPDAC = 01FH	800		900	µV/ LSB
Full Scale Accuracy	SPDAC = 0FFH	201	214	227	mV
VMAG PWM Range: 0% duty cycle 100% duty cycle	SINEN = 0, Extrapolated from measurements at VMAG = 2.4 V and 3.4 V	1.8 3.7		2.0 4.1	V V
VMAG Gm: $\frac{\Delta I(VMG)}{\Delta(ISNS - ISNSN)}$	SPDAC = 03FH, I(VMAG) = 10 µA, -10 µA	105	150	195	µA/V

SPINDLE (continued)

Spindle DAC

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SPDAC Resolution			8		bits
SPDAC DNL Step from 080H to 07FH All other steps		 -2 -1		 2 1	 LSB LSB
SPDAC INL			TBD		LSB
Full Scale Output Voltage		630	650	670	mV

Spindle Drive Outputs (PHA, PHB, PHC)

Total Voltage Drop	I_{PH} = 2.5 A			2.5	V
Slew Rate	I_{PH} = 2.5 A PHSLOW = 0 PHSLOW = 1	 TBD TBD	 10 5	 TBD TBD	 V/µS V/µS
Leakage	OUTEN = 0			1	mA

TACH Comparator

Rising Offset	PHB-PHC,PHB rising	30		50	mV
Falling Offset	PHB-PHC,PHB falling	-30		-50	mV

UTILITY FUNCTIONS

V2P5 Voltage Reference

Voltage Accuracy	Iload = 0 mA, V referenced to 2.50 V	-3		+3	%
Output Impedance	|Iload| = <1 mA			10	Ω

Boost Regulator

VBOOST voltage	wrt VM	14		16	V
Switch Frequency		272	320	368	kHz
Current				5	mA
Regulation	Over specified VM range	TBD		TBD	%

Analog Multiplexer

Attenuation from AMUX pin to SPDAC output	AMUX = {111}	9	10	11	V/V

Negative Regulator

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gate Driver Switching Frequency			320		KHz
Maximum Duty Cycle			50		%
Gate Driver Output Voltage	Iout = 20 mA (sinking)	0.5		VM-0.3	V
Gate Driver Output Transition Time	Cl = 200 pF		150		ns

3.3 V Regulator (V5 - REGB $\geq$ 0.35 V, R1 $||$ R2 $\leq$ 500 Ω)

REGE voltage	I(REGB) = 10 mA	1.235	1.3	1.365	V
Transimpedance = $\frac{\Delta VREGE}{\Delta I\ (REGB)}$	I(REGB) = 0 to 20 mA, V(REGB) < V5 - 0.35, V(REGB) > 3.6	TBD		TBD	Ω
REGB short circuit current	REGB = 0 V			TBD	mA
REGB bias current		-1		1	µA

BIAS

RBIAS bias voltage		1.26	1.30	1.34	V

+3.3 V Reset Comparator

Trip voltage, regular mode (TR12 falling)		1.25	1.30	1.35	V
Hysteresis current		4	5	6	µA
Propagation delay from TR3 to PORZ	TR3 pulse to 100 mV below VBG			300	ns

+5V Reset Comparator

Trip voltage, regular mode (TR5 falling)		1.274	1.30	1.326	V
Hysteresis current		4	5	6	µA
Propagation delay from TR5 to PORZ	TR5 pulse to 100 mV below VBG			300	ns

+12V Reset Comparator

Trip voltage, regular mode (TR12 falling)		1.25	1.30	1.35	V
Hysteresis current		4	5	6	µA
Propagation delay from TR12 to PORZ	TR12 pulse to 100 mV below VBG			300	ns

UTILITY FUNCTIONS (continued)

POR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
CDLY charge current	CDLY = 1.4 V TR3, TR5, and TR12 > 1.3 V	5.7	6	6.3	µA
CDLY discharge impedance	CDLY = 0.2 V, TR5 < 1.3 V, TR3 and TR12 > 1.3 V, Measure I and calculate R			400	Ω

SWG

VOH, wrt VB2	ILOAD = TBD	-1			V
VOL	ILOAD = TBD			1	V

Bandgap

VBG		1.268	1.3	1.333	V

OTSD (Over temperature shutdown)

Trip temperature—OTSD	Temperature rising		150		°C
Hysteresis			45		°C
Trip temperature—EOTW	wrt OTSD trip temp		-25		°C

DIGITAL I/O

Digital Input (SDATA, SCLK, SDEN)

Input voltage V_{IL}				0.6	V
V_{IH}		2.4			V
Input bias current, I_{IH}	V_{IN} = 4 V			1	µA

Digital Output (DMUX, SDATA)

Output voltage V_{OL}	I_{SINK} = 1 mA			0.4	V
V_{OH}, wrt V5	I_{SOURCE} = 1 mA	-1			V

Digital Output (PORZ)

Output voltage V_{OL}	I_{SINK} = TBD mA			0.4	V
V_{OH}, wrt V5	I_{SOURCE} = TBD mA	-2	-1.0		V

UTILITY FUNCTIONS (continued)

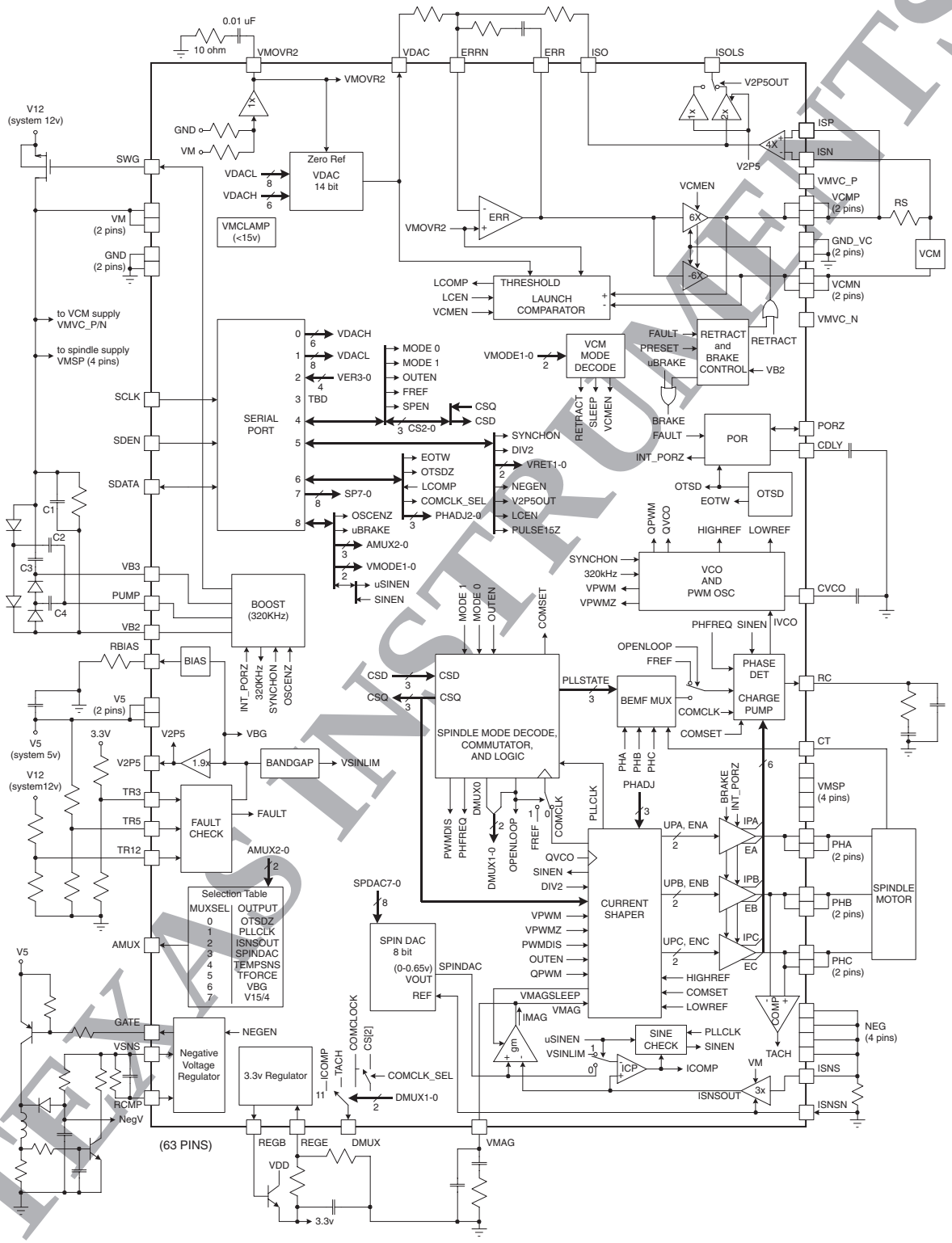
Serial Port Read Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SDEN setup time prior to SCLK rise	Tsens		10			ns
SDEN hold time after SCLK rise	Tsenh		10			ns
SDATA input setup time prior to SCLK rise	Tds		10			ns
SDATA input hold time after SCLK rise	Tdh		10			ns
SCLK to valid SDATA delay	Tdskewl				15	ns
End of valid data to SCLK	Tdskewe				TBD	ns
SDEN fall to SDATA tri-state	Tsendl				15	ns
SDATA turn around from SCLK	Tturnd		20			ns
SCLK period	Tc		40			ns
SCLK high pulse width	Tckh		20			ns
SCLK low pulse width	Tckl		20			ns
SDEN low time	Tsl		30			ns

Serial Port Write Timing

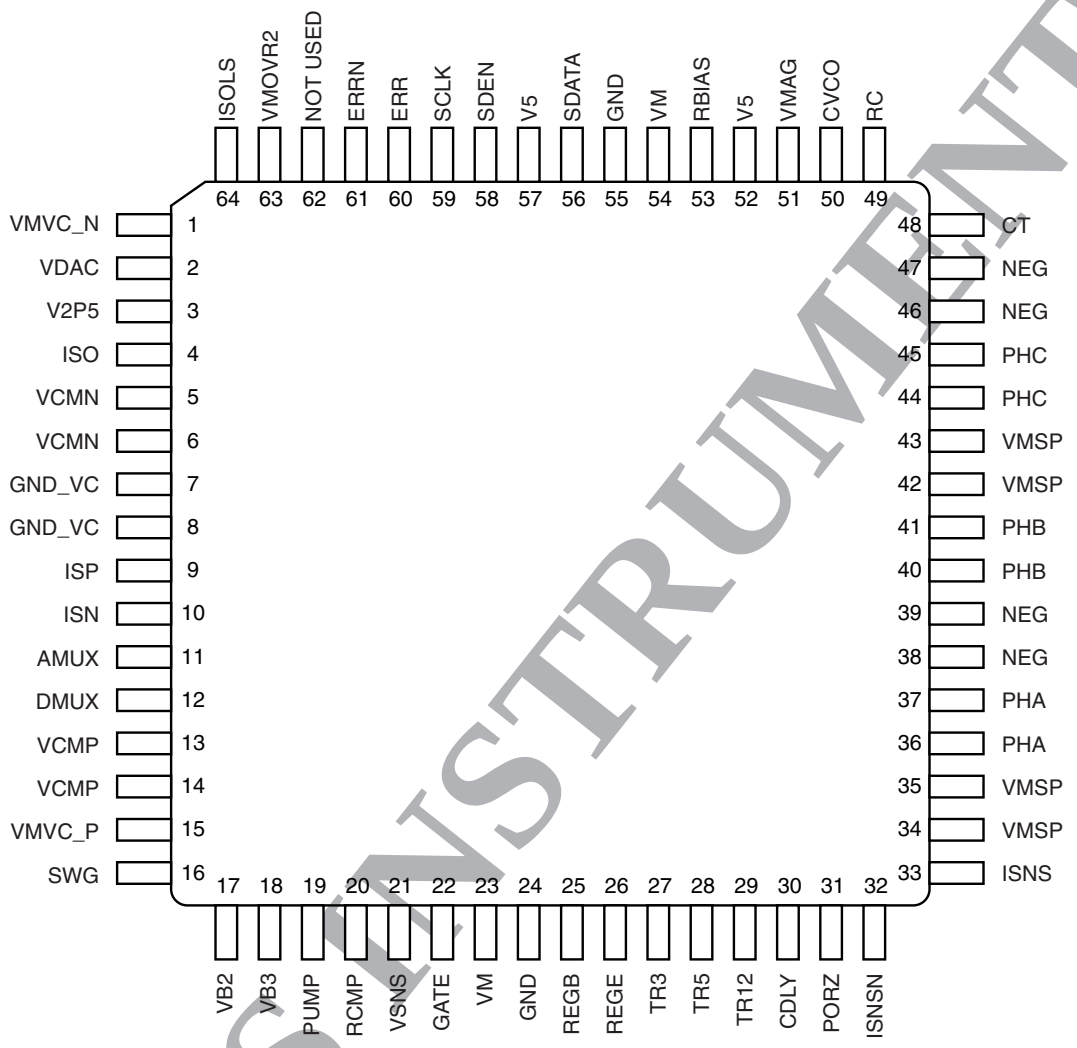
SCLK data clock period	Tc		40			ns
SCLK low time	Tckl		20			ns
SCLK high time	Tckh		20			ns
SDEN rise to SCLK setup time	Tsens		10			ns
SDEN fall to SCLK hold time	Tsenh		10			ns
SDATA to SCLK setup time	Tds		10			ns
SDATA to SCLK hold time	Tdh		10			ns
SDEN minimum low time	Tsl		30			ns

APPLICATION BLOCK DIAGRAM



PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

TLS2231
Servo-Combination Predriver

May 1998

DESCRIPTION

The TLS2231 is a servo-combination predriver designed for use in hard-disk-drive applications. The predriver, when used in combination with the TPIC150x, can drive a voice-coil motor (VCM) and a spindle motor. Figure 1–1 is a functional block diagram of the servo-combination predriver.

FEATURES

VOICE-COIL MOTOR PREDRIVER

- **Linear input control**
- **Transconductance amplifier with class AB output (when used with TPIC150x drivers)**
- **Saturation detection of VCM drivers**
- **Summing amplifier**
- **Current-sense amplifier**
- **Retract function on power loss or on software command**
- **External set for retract voltage**

SPINDLE MOTOR PREDRIVER

- **Pulse width modulated (PWM) start and PWM current limit**
- **Advance terminal signals commutation timing to on-chip sequencer during start mode**
- **Current-sense comparator**
- **Low noise phase-locked loop performs commutation timing during run mode**
- **PWM or linear run**
- **Low-side driver transconductance amplifier for linear run mode**
- **Dynamic brake**
- **Power-down brake after delay**
- **Soft switching or limited dV/dT reduces acoustic noise in linear current control mode**
- **KELVIN_SENSE input to reduce current-sense errors induced by ground level variances**

SUPPORT FUNCTIONS

- **Voltage monitor (based on 5 V and 12 V supplies)**
- **Charge pump (24 V) for driving N-channel DMOS H-bridge drivers**

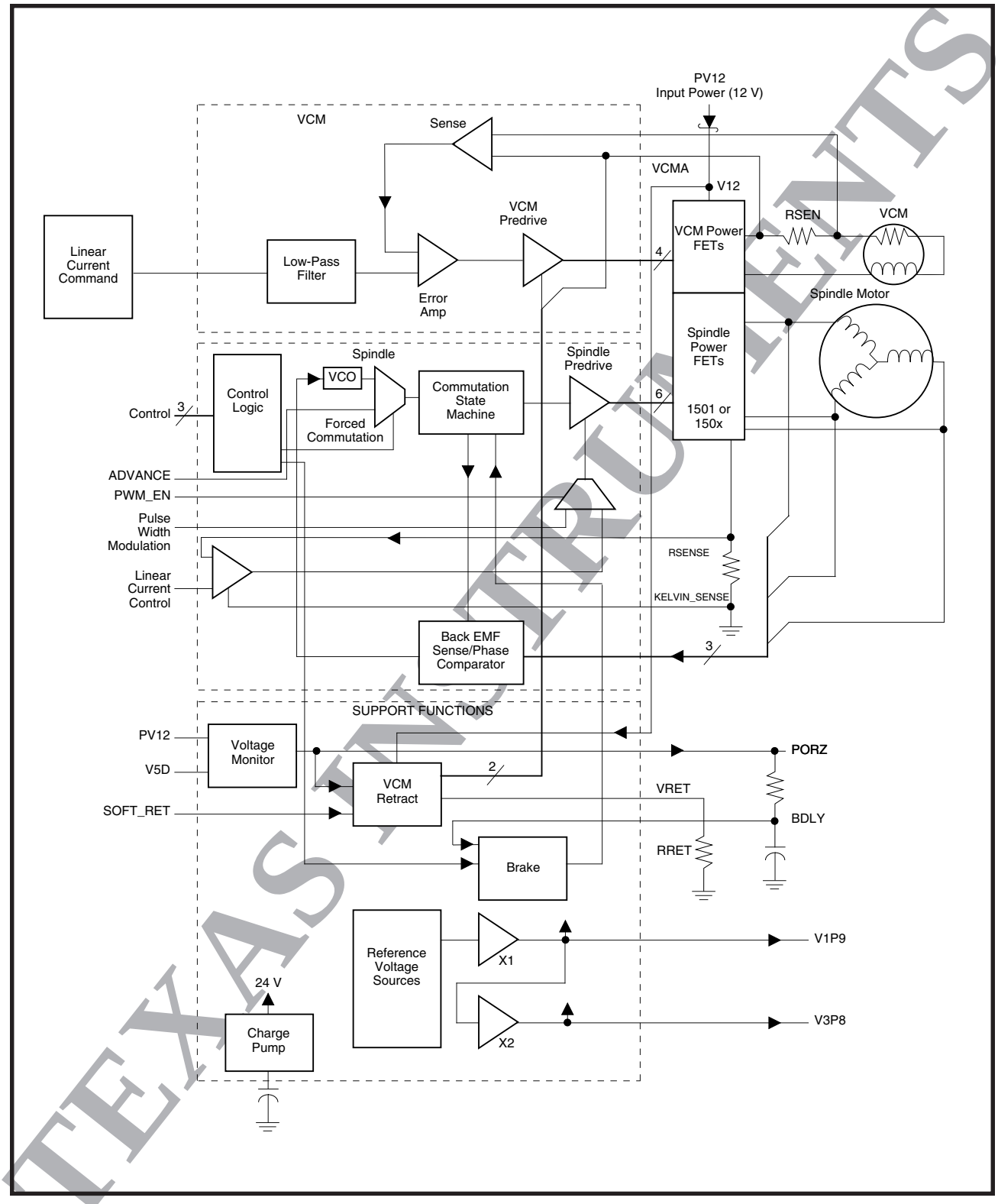


FIGURE 1-1: Functional Block Diagram

FUNCTIONAL DESCRIPTION

VOICE-COIL MOTOR DRIVE

The TLS2231 uses a linear voltage to control the current applied to the VCM. An input amplifier is provided for convenient filtering of the input voltage command. The bandwidth of the low-pass filter is determined by external components. The error amplifier compensates for a transconductance loop. The error amplifier output represents the difference between the command current and the actual current. The actual current is measured across the RSEN resistor by the sense amplifier. The compensated output of the error amplifier is applied to the VCM predrive circuit that biases the VCM power field-effect transistors (FETs) of the TPIC150x.

SPINDLE MOTOR DRIVE

The spindle motor is started under PWM control using an external signal for forced commutation. As the motor approaches operational speed, the commutation state machine is driven by the output of the voltage-controlled oscillator (VCO). The VCO utilizes the back electromotive force (EMF) of the motor to close a phase-locked loop that matches the commutation frequency to the motor. Once in the run mode, the motor speed can be controlled using either a PWM signal to modulate the current applied to the motor or by a linear current command that acts as the input to the spindle transconductance loop.

SUPPORT FUNCTIONS

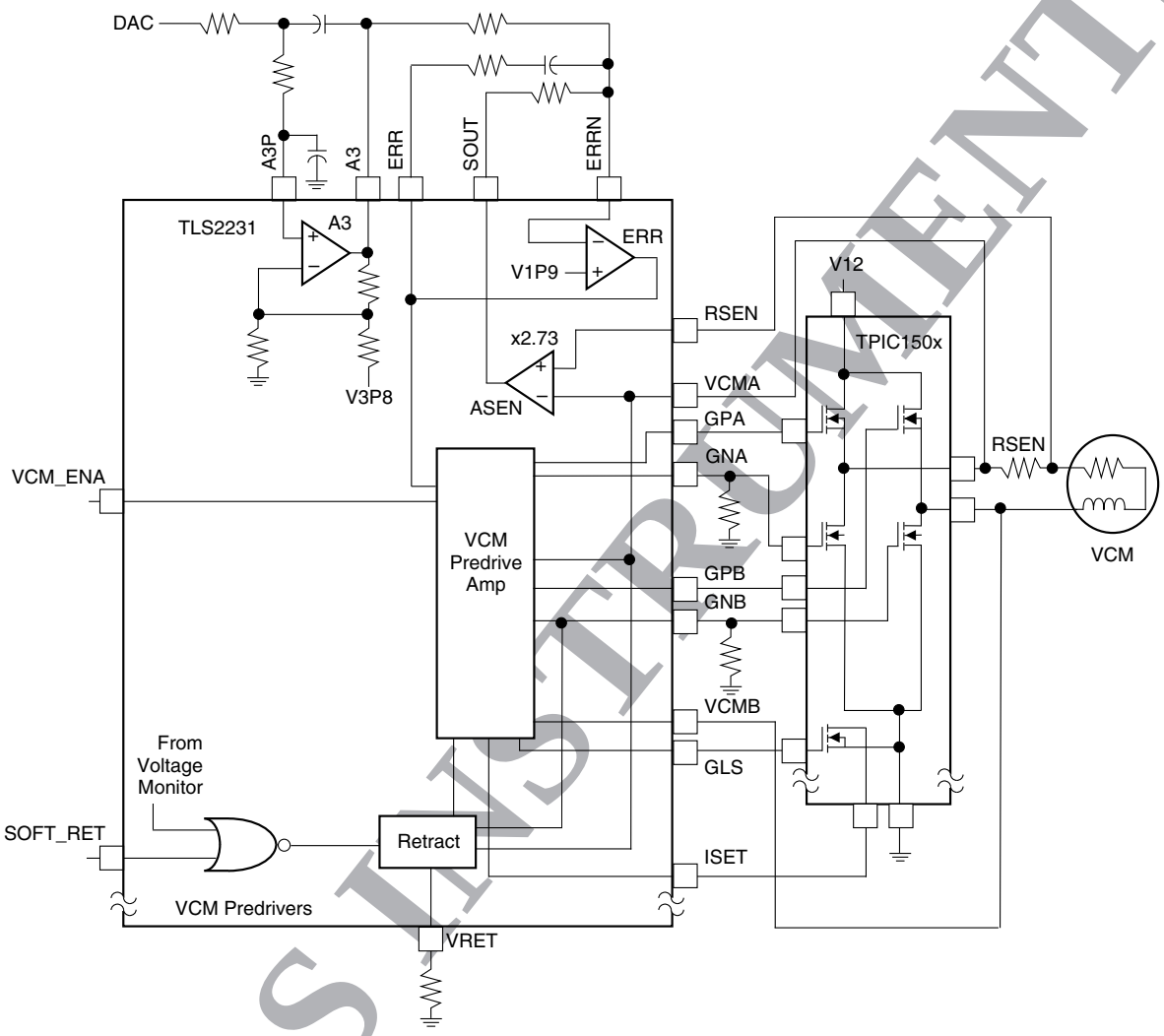
The TLS2231 support functions include a voltage monitor that indicates a fault when power supply voltages drop below a specified threshold. When triggered, the fault signal initiates a VCM retract and can also initiate delayed braking of the spindle motor. The VCM retract voltage is set by the selection of an external resistor. Other support functions include the on-chip reference voltage and the charge pump. The reference voltages are used internally and are also available for external use. The charge pump generates 24 V for driving the N-channel DMOS H-bridge drivers of the TPIC150x.

DETAILED DESCRIPTION

VOICE-COIL MOTOR PREDRIVER

The TLS2231, when combined with a power driver such as the TPIC150x, provides current drive capability for a VCM. Figure 2–1 shows the functional block diagram of a typical application. A signal applied to the input filter amplifier, A3, as shown indicates the level of current to be delivered to the VCM. This signal is low-pass filtered by amplifier A3 and applied to the error amplifier ERR.

The error amplifier implements a transconductance loop. Its output is the difference between the commanded current and the actual current as measured across RSEN by the differential amplifier ASEN. This error signal is applied to the predriver amplifier that biases the power FETs of the TPIC150x for class AB operation.



NOTE:
The GNA and GNB terminals can be connected to external 10-MΩ to 20-MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2231.

FIGURE 2-1: Voice-Coil Motor Predriver Functional Block Diagram

INPUT FILTER AMPLIFIER (A3)

The input filter amplifier (A3) filters the applied input. This amplifier can be used to implement a Sallen and Key filter as shown in Figure 2–2.

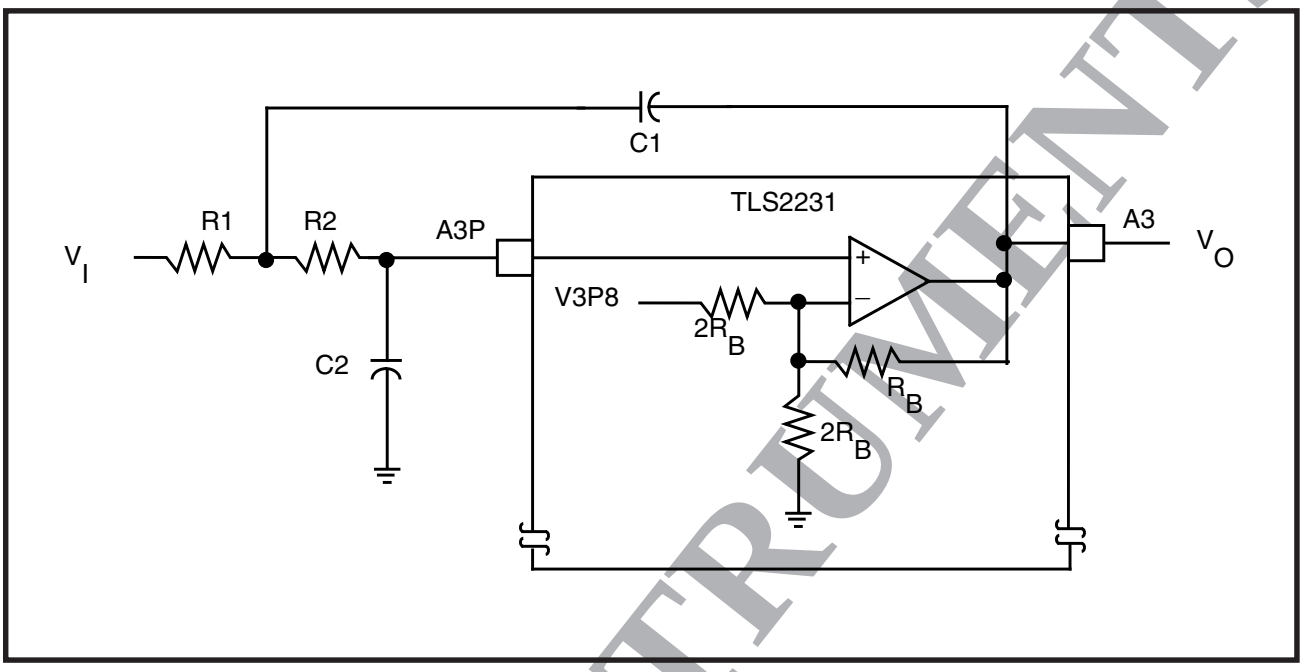


FIGURE 2-2: Sallen and Key Low-pass Filter Implementation

Equations 1, 2, 3, and 4 show the transfer function of this circuit.

$$H(S) = \frac{K\omega^2}{S^2 + \frac{\omega}{Q}S + \omega^2} \quad (1)$$

$$K = 1 + \frac{R_B}{2R_B \| 2R_B} = 2; \; R_B \text{ matched internal components} \quad (2)$$

$$Q = \frac{1}{3 - K} = 1 \quad (3)$$

$$\omega = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \quad (4)$$

R1, R2, C1, and C2 are choosen to match ω to the applied input signal.

DETAILED DESCRIPTION (continued)

SUMMING AMPLIFIER (ERR)

The summing amplifier (ERR) generates an error signal that is proportional to the difference between the command current and the actual current. Selection of the external components provides compensation for the transconductance loop (see Figure 2–3).

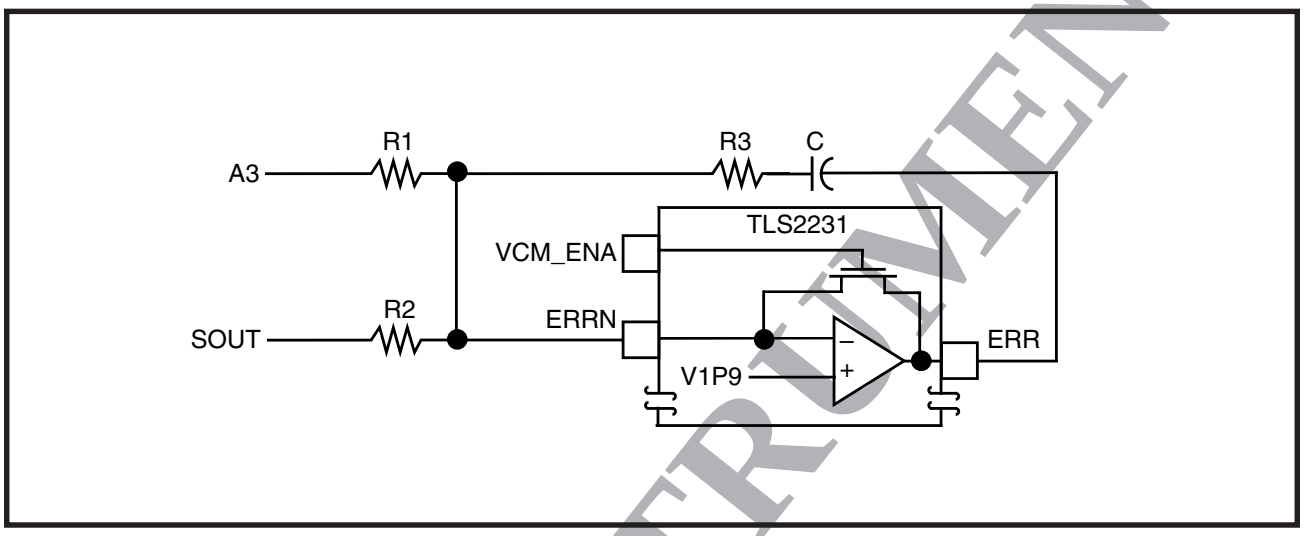


FIGURE 2-3: Summing Amplifier Implementation

Equation 5 shows the transfer function of this circuit.

$$H(S) = \frac{(R_3C)S + 1}{(R_2C)S} \quad (5)$$

Selecting values for R1, R2, and RSEN sets the VCM transconductance gain (Gm) (see equation 6).

$$Gm = \frac{IVCM}{VCMD} = \frac{R_2}{2.73 \bullet R_1 \bullet RSEN} \quad (6)$$

NOTE: If the error amplifier is near saturation, which is detected by either VCMA < (1/12) V12 and VCMB >(11/12) V12 or by VCMA > (11/12) V12 and VCMB < (1/12) V12, then the SAT_DET signal is set high.

CURRENT-SENSE AMPLIFIER (ASEN)

The current-sense amplifier (ASEN) (see Figure 2–4) provides a measure of the current that is being delivered to the motor by measuring the voltage across the sense resistor. The gain of this amplifier is fixed at 2.73. The offset can be calibrated by setting VCM_ENA low, along with SOFT_RET, to ensure that the VCM outputs are turned off and no current is being delivered to the VCM. In this state SOUT should be equal to V1P9.

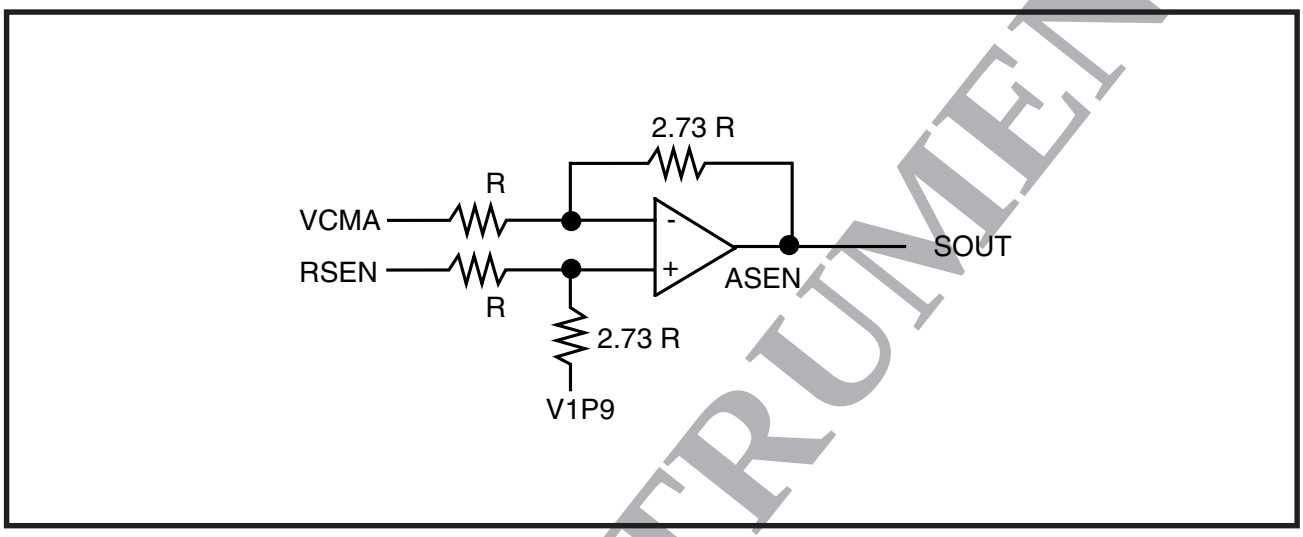
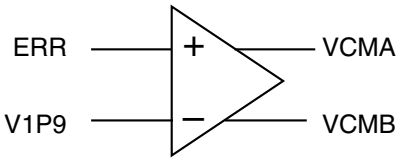


FIGURE 2-4: Current-Sense Amplifier Implementation

VCM PREDRIVER AMPLIFIER

The VCM predriver amplifier biases and operates the power FETs of the TPIC150x as a class AB amplifier with a gain of 12. Equation 7 shows this relationship.

$$\frac{VCMA - VCMB}{ERR - V1P9} = 12 \qquad (7)$$



NOTE: Setting VCM_ENA to logic low when SOFT_RET is equal to logic low disables the VCM output. Setting SOFT_RET to high disables the VCM and causes a retract.

DETAILED DESCRIPTION (continued)

BIASING THE TPIC150X POWER FETS

The VCM predriver amplifier uses signals GLS and ISET to determine the bias point for the TPIC150x power FETs (see Figure 2–5). A constant current source is applied to the ISET pin. The gate voltage for the TPIC150x sense FET is varied until the voltage on ISET matches a known reference of V12/2. The voltage at GLS is then scaled and used to set the bias point of the TPIC150x power FETs.

$$I_{quiescent} \approx (150) \bullet I_{source} \quad (8)$$

Where: Iquiescence is the bias current in the VCM H-bridge, and Isource ≈ 40 µA.

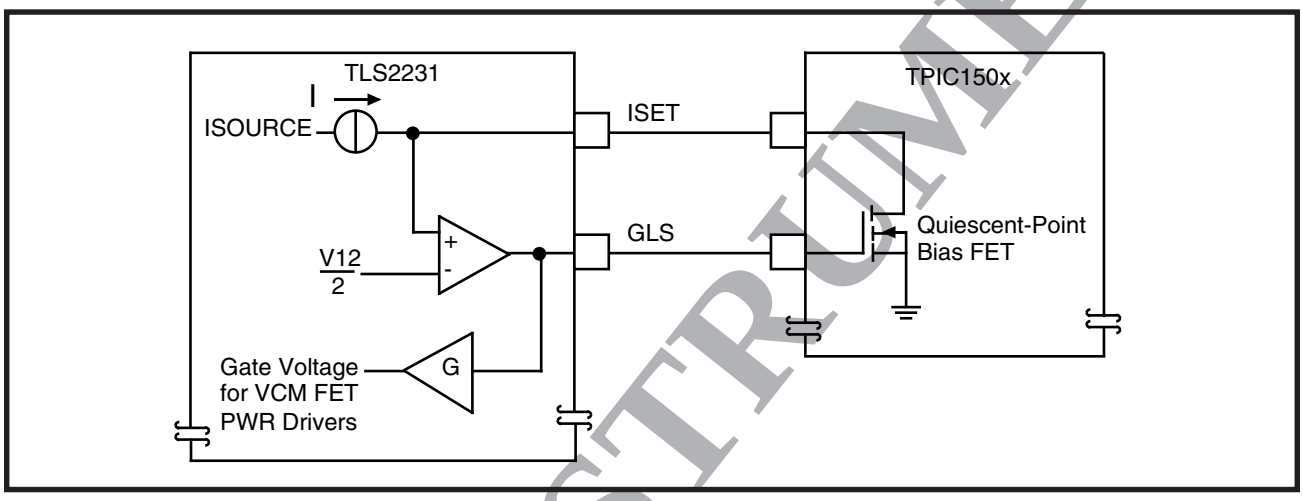


FIGURE 2-5: GLS and ISET Biasing the TPIC150x

SPINDLE MOTOR PREDRIVER

Spindle Motor Predriver Functional Overview

Figure 2–6 shows the TLS2231 spindle motor predriver section. The RESET, ENABLEZ and DISPWRZ signals command one of eight different operational modes:

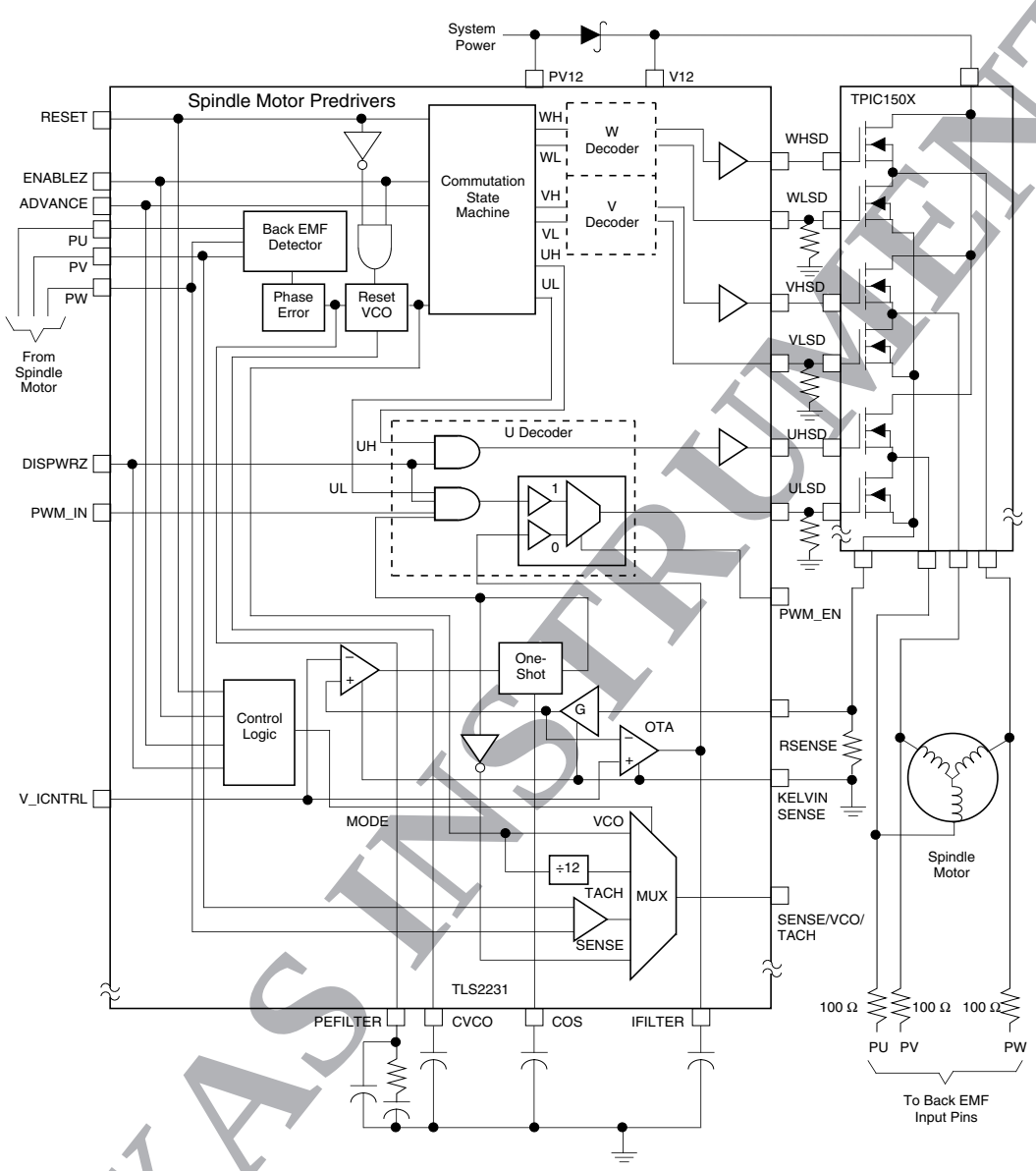
- Preset
- Start/SENSE and Start/TACH
- Run
- Coast
- Brake
- I_CAL
- Test1†
- Test2†

†Modes Test1 and Test2 are for factory test purposes and are shown for reference only.

The preset and start/SENSE and start/TACH modes are used to start the spindle motor. The commutation state machine controls motor commutation by enabling the appropriate high- and low-side drivers of the TPIC150x.

During start-up, the commutation state machine is advanced by pulses applied on ADVANCE. As the spindle motor approaches idle frequency, the run mode is selected. At this time, the commutation state machine is advanced by the output of the VCO. The BEMF detector and phase error amplifier generate an error signal that is applied to the input of the VCO. The commutation frequency is adjusted by the VCO using this error signal.

In run mode, the current applied to the motor can be controlled by either pulse width modulation (PWM) or by the application of a linear signal. The type of control is determined by setting PWM_EN (pin 49). A logic high selects PWM control, while a logic low selects linear control.



NOTE:
The ULSD, VLSD, and WLSD terminals can be connected to external 10-MΩ to 20-MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2231.

FIGURE 2-6: Spindle Predrivers Functional Block Diagram

Spindle Motor Predriver Functional Overview(continued)

The MUX shown in Figure 2–6 implements the logic illustrated in Figure 2–7. The TACH, SENSE, and VCO output signals are combined with the mode signals indicated (these signals represent the various states determined by selection of RESET, ENABLEZ, and DISPWRZ as defined in Table 2–1) to provide a real-time status signal at the SENSE/VCO/TACH output.

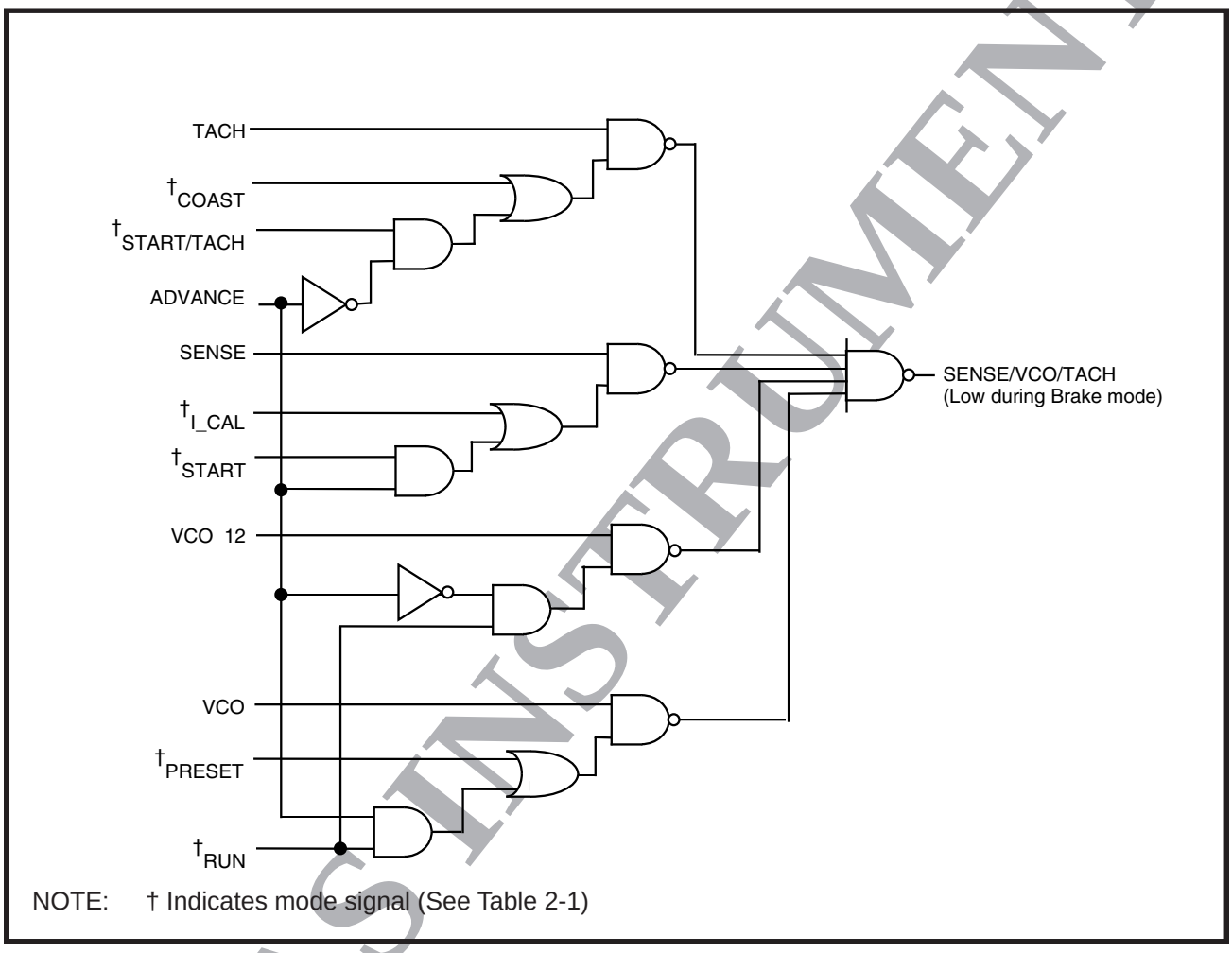


FIGURE 2-7: Sense/VCO/TACH MUX Logic

Spindle Motor Predriver Modes of Operation

The TLS2231 spindle motor predriver circuitry operates in one of eight modes as selected by RESET, ENABLEZ, and DISPWRZ. Table 2–1 defines the combinations of these signals that are used to select either the preset, start/SENSE and start/TACH, run, coast, brake, I_CAL, Test1, or Test2 mode.

TABLE 2–1: Modes of Operation

MODE	RESET	ENABLEZ	DISPWRZ	ADVANCE	SENSE/ VCO/TACH	PE FILTER	VCO	STATE MACHINE	V19P OUT
Preset	1	1	1	X	VCO	0.1 V	Idle	Reset	1.9 V
Start	0	1	1	1	SENSE	0.1 V	Reset	†	1.9 V
Run	0	0	1	1	VCO	Run	Run	Run	1.9 V
Run	0	0	1	0	VCO/12	Run	Run	Run	1.9 V
Coast	0	0	0	X	TACH	Run	Run	Run	1.9 V
Brake	1	0	0	X	GND	0.1 V	Idle	Reset	1.9 V
I_CAL	1	1	0	X	SENSE	0.1 V	Idle	Reset	1.9 V
Test1 ‡	0	1	0	X	X	X	X	X	Vbg
Test2 ‡	1	0	1	X	X	X	X	X	Thermal Shutdown

† During start mode, the state machine is advanced on the rising edge of the ADVANCE pin.
‡ Modes Test1 and Test2 are for factory test purposes and are shown here for reference only.

The transitions between the various modes should be done according to the diagram shown in Figure 2–8 to prevent logic race conditions.

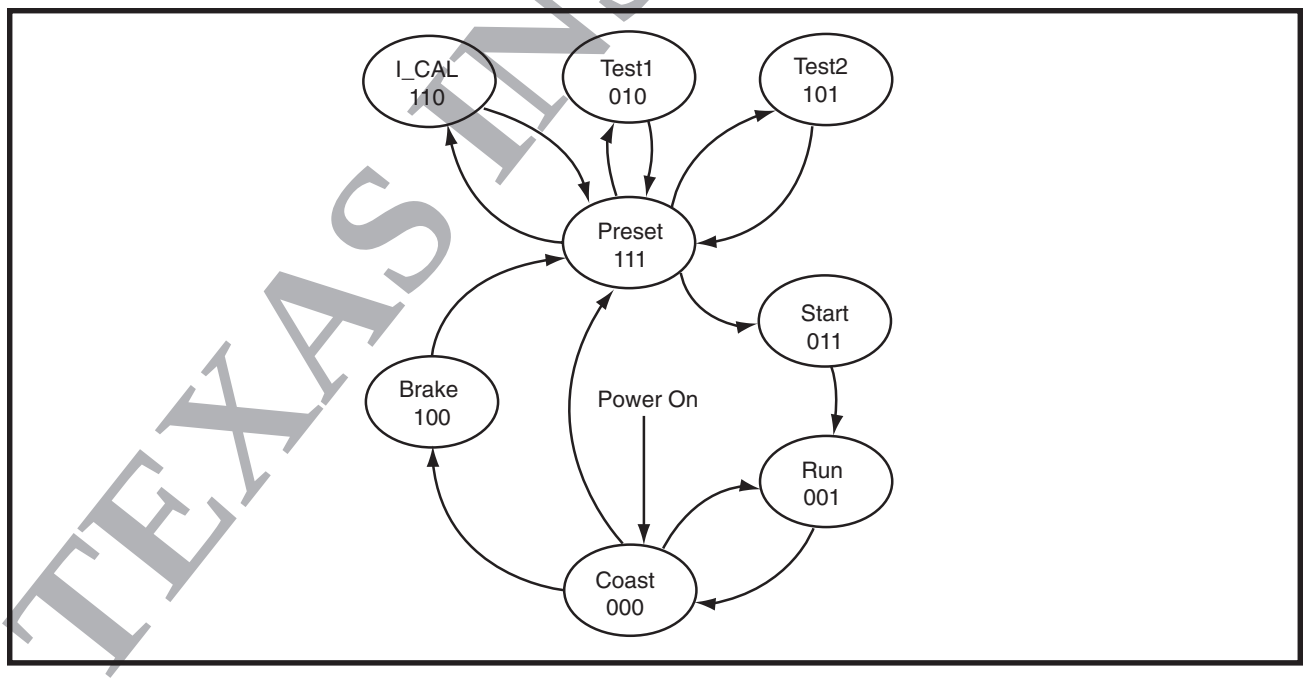


FIGURE 2-8: Mode Transition State Diagram

Spindle Motor Predriver Modes of Operation
(continued)

Preset

In the preset mode, a fixed voltage of 100 mV is applied at the input to the VCO causing it to operate at its idle frequency. The VCO idle frequency, which is available at the SENSE/VCO/TACH output, is measured so that switching over (handing off) from forced commutation to closed-loop commutation can be accomplished at a frequency within the lock range of the PLL. This should be done at a frequency which is at least 10 percent higher than the idle frequency.

NOTE: To allow the filter network to settle, the VCO idle frequency measurement should not be made until after the preset mode has been commanded for at least 200 ms.

Start/SENSE

The start/SENSE mode can be used to determine the approximate position of the spindle motor's rotor so that the commutation state machine can be initialized. The output of the SENSE comparator is available at the SENSE/VCO/TACH output. The SENSE comparator will switch from low to high when the voltage across the RSENSE resistor exceeds the voltage applied at V_ICNTRL.

Start/TACH

The start/TACH mode is used to start the spindle motor. The PWM_EN pin is held high to select PWM control. In order to get maximum spindle motor acceleration, PWM_IN is held high also. This allows maximum current to be applied to the spindle motor. When the current, as measured across RSENSE, exceeds the threshold as set by the voltage applied at V_ICNTRL, the one-shot disables the low-side spindle motor drive creating a constant off time which is set by the external capacitor COS. Choose this capacitor to optimize spin-up time and to provide sufficient over-current protection. Use equations 9 and 10 to select COS.

$$COS = \frac{I}{\Delta V} \bullet \Delta t \qquad (9)$$

where $I = \frac{Vbg}{RSLEW}$,
$Vbg = 1.21$, and $\Delta V = 2$

$$COS = \left(\frac{0.605}{RSLEW}\right) \bullet \Delta t \qquad (10)$$

Where: COS is in farads.

RSLEW is in Ω and its value is chosen using equations 11 through 18. Δt is off time in seconds.

NOTE: Adjusting RSLEW also affects spindle driver slew rates as described in the Slew Rate Control subsection.

Since the back EMF from the spindle motor is small during start-up, the commutation state machine must be advanced manually with the ADVANCE pin. This is done open-loop, using a timing algorithm that is matched to the dynamics of the motor/spindle.

During open-loop acceleration, the VCO is held at reset. When the frequency of the signal being applied to the ADVANCE pin exceeds the VCO idle frequency measured in the preset mode, select the run mode. This releases reset of the VCO enabling it to advance the commutation state machine.

NOTE: Although the TACH output is available during this mode, it will contain noise induced by current limit switching. Therefore, TI recommends that the coast mode be used for making TACH measurements.

Run

In the run mode, the commutation state machine is advanced by the output of the VCO. The voltage of each phase (PU, PV, and PW) is monitored to determine if commutation occurs late or early. This is done by generating a signal that is the undriven phase minus the average of the two driven phases. This signal is inverted every other cycle to obtain positive pulses. If commutation occurs too early, an increasing positive signal is generated to increase the VCO frequency to align the commutation with the motor winding. The VCO or VCO/12 output at the SENSE/VCO/TACH pin can be used as feedback for closed-loop speed regulation.

NOTE: Servo data can also be used for higher regulation.

The spindle speed is regulated by adjusting the current that is applied to the spindle motor. This is done in one of three ways.

Setting PWM_EN high selects PWM control which can be implemented in one of two ways. In the first method (voltage mode) a variable duty cycle signal is applied at PWM_IN (pin 4). This duty cycle variability is used to change the voltage that is supplied to the motor. This leads to changes in speed of the motor. Current limiting is determined by the selection of RSENSE and by the application of a threshold voltage at V_ICNTRL. When the current through the sense resistor becomes large enough that the sense amplifier output exceeds the voltage at V_ICNTRL, the one-shot is triggered pulling the low-side driver gates to ground which turns them off. This current limiting is needed only during a fault condition since the current in RSENSE is not sufficient during normal operation.

NOTE: KELVIN_SENSE is used to sense the ground side of RSENSE to eliminate offset caused by ground potential differences.

In the second PWM control method (current mode) V_ICNTRL is used to control the maximum threshold at the sense resistor while PWM_IN is held at constant high level. The voltage applied at V_ICNTRL is proportional to the desired motor current. When the current through the sense resistor becomes large enough that the sense amplifier output exceeds the voltage at V_ICNTRL, the one shot is triggered which turns off the low-side drivers. The duty cycle at which the drivers turn on and off is proportional to the signal applied at V_ICNTRL. This controls the effective current applied to the spindle motor.

The linear mode is implemented by setting PWM_EN low and applying a voltage at V_ICNTRL that is proportional to the desired motor current. The transconductance amplifier (OTA) drives the gate of the appropriate low-side driver until the desired current (as sensed through RSENSE) is attained.

Coast

During coast mode, the spindle motor drivers are disabled and the spindle spins freely. The TACH output is available at the SENSE/VCO/TACH pin. An example of the signal appearing at the TACH output is shown in Figure 2–9.

Brake

During brake mode, the spindle motor high-side drivers are all turned on. This causes the motor to brake dynamically.

Calibration Mode

Figure 2–10 shows the calibration mode used to measure the voltage at V_ICNTRL that corresponds to 0.3 V across the sense resistor. When the calibration mode is selected, the output of MUXA is an internal 0.3 V reference. By applying a ramp from maximum to minimum at the input of V_ICNTRL and monitoring the output at SENSE/VCO/TACH, the point at which the sense comparator switches states can be determined.

Test Modes 1 and 2

These modes are for factory testing of the TLS2231. In test mode 1, the band-gap voltage (Vbg) is available at V1P9 (pin 43). Test mode 2 is used to test over temperature or thermal shutdown through V1P9.

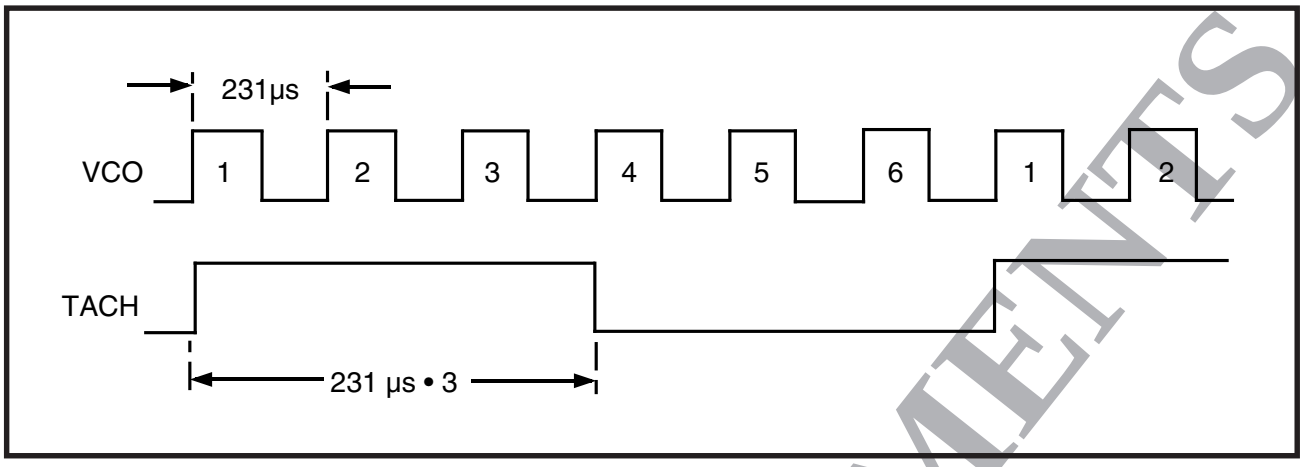


FIGURE 2-9: TACH Output for a 12-Pole 7200-RPM Motor

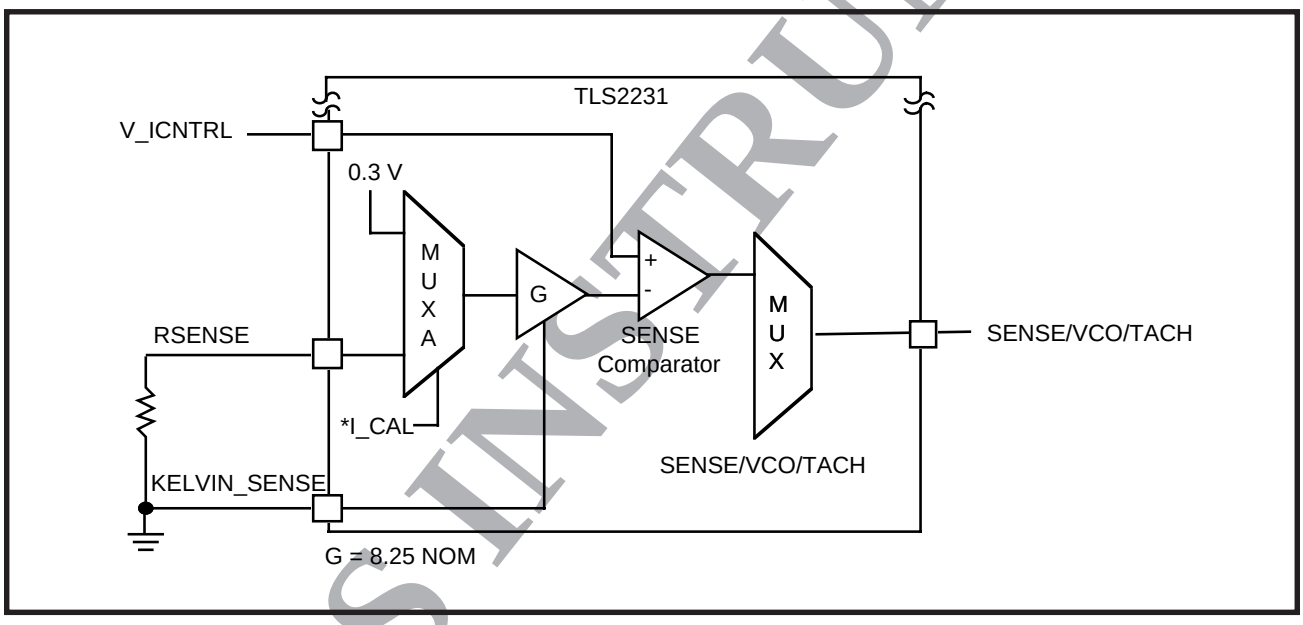


FIGURE 2-10: Calibration Mode Logic Diagram

SPINDLE MOTOR PREDRIVER (continued)

Commutation Control

The commutation process involves sequentially turning the spindle motor high- and low-side drivers on and off as illustrated in Figure 2–11 and listed in Table 2–2.

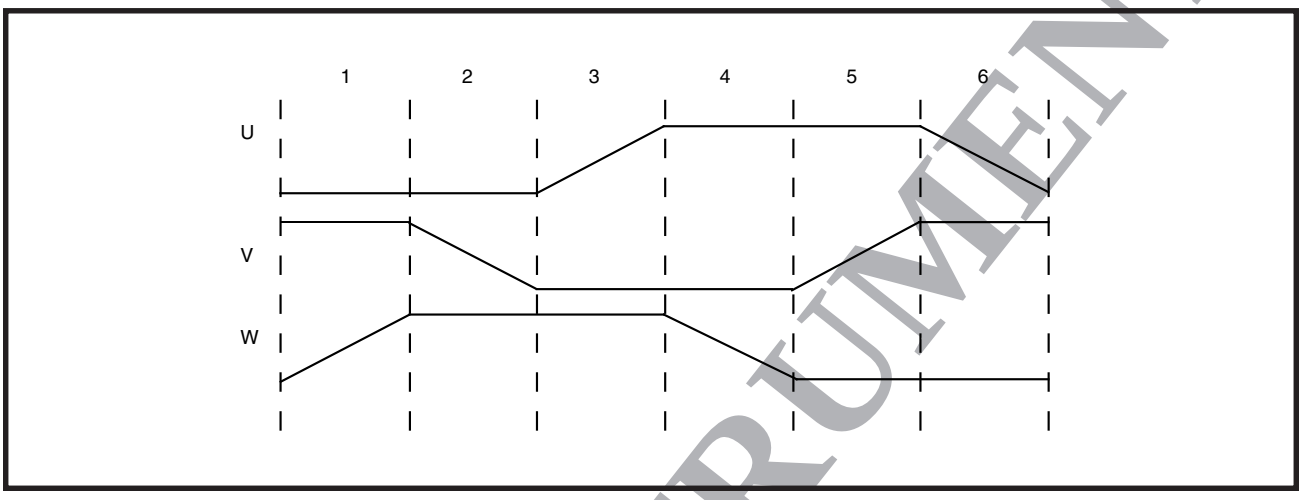


FIGURE 2-11: Commutation Graphical Form

TABLE 2-2: Commutation State Table

STATE	0 (PRESET)	1	2	3	4	5	6
UL	0	1	1	0	0	0	0
VL	0	0	0	1	1	0	0
WL	0	0	0	0	0	1	1
UH	0	0	0	0	1	1	0
VH	0	1	0	0	0	0	1
WH	0	0	1	1	0	0	0

SPINDLE MOTOR PREDRIVER (continued)

Slew Rate Control

A resistor attached to the RSLEW pin controls the slew rate of the spindle motor driver power FETs by adjusting the amount of current that is applied to the gate. The RSLEW resistor establishes a reference current, ISLEW as shown in Figure 2–12. This current is used by the high- and low-side driver circuits to determine the amount of current that is applied to the power FETs gate.

The high-side driver circuitry (Figure 2–13) provides two different levels of current for charging and discharging the power FETs gate (Figure 2–14). During the charging interval, switch S1 is closed until the voltage at the power FETs gate, V_{GHS}, exceeds ~20 V. At that point, switch S1 opens.

Equation 11 is used to calculate the current applied to the gate when S1 is closed. Equation 12 is used to calculate the current applied to the gate when S1 is open.

$$I_{CHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 26.4 \quad (11)$$

$$I_{CHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 2.4 \quad (12)$$

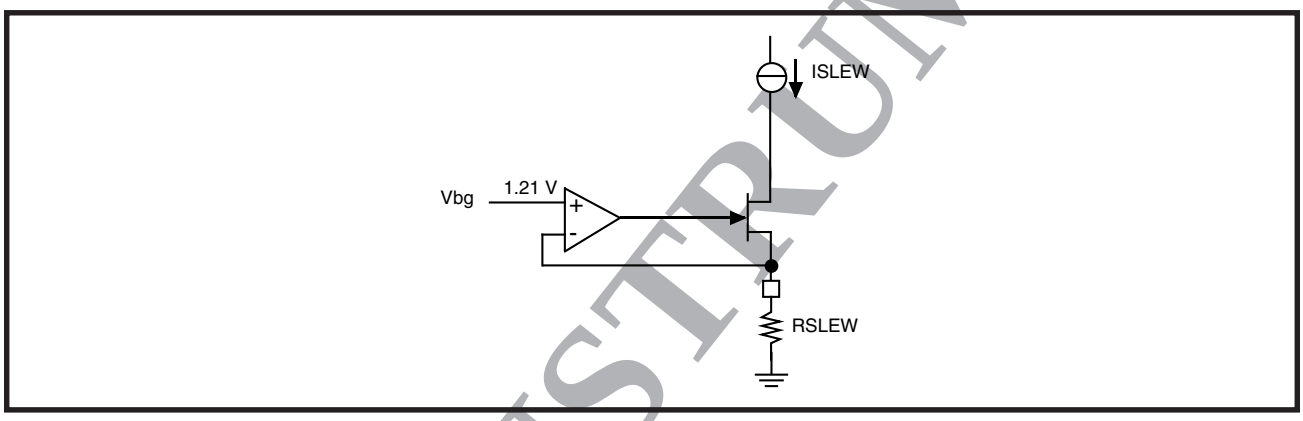


FIGURE 2-12: ISLEW Biasing Circuit

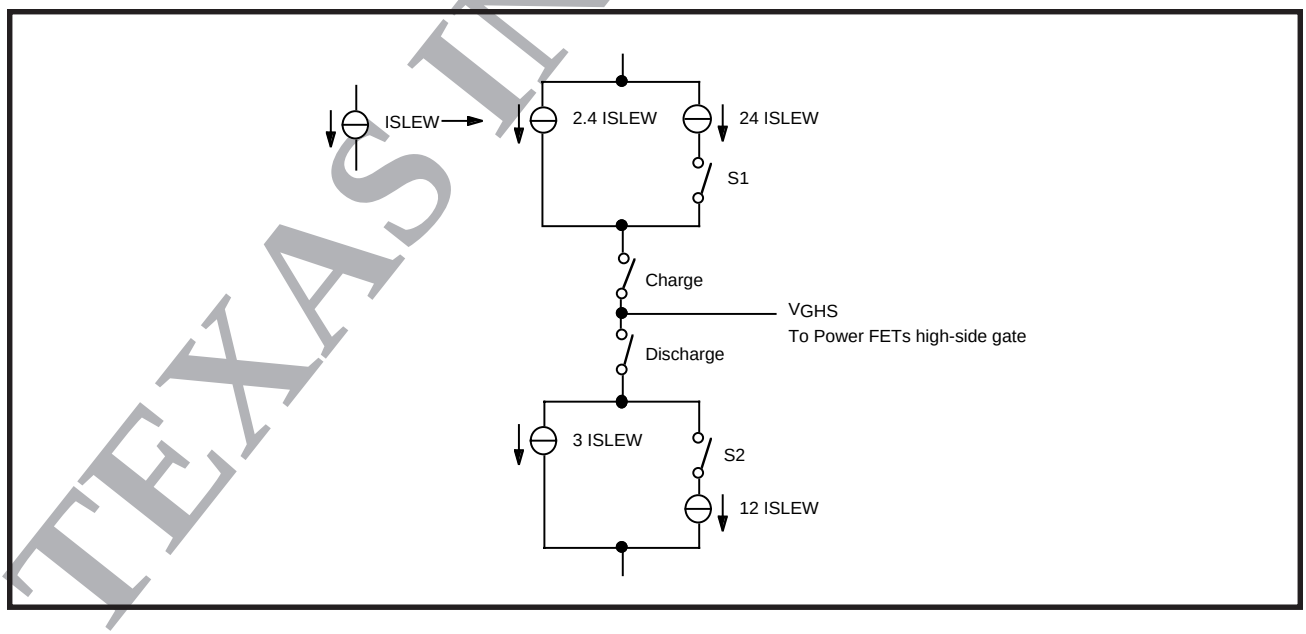


FIGURE 2-13: High-Side Driver Circuitry

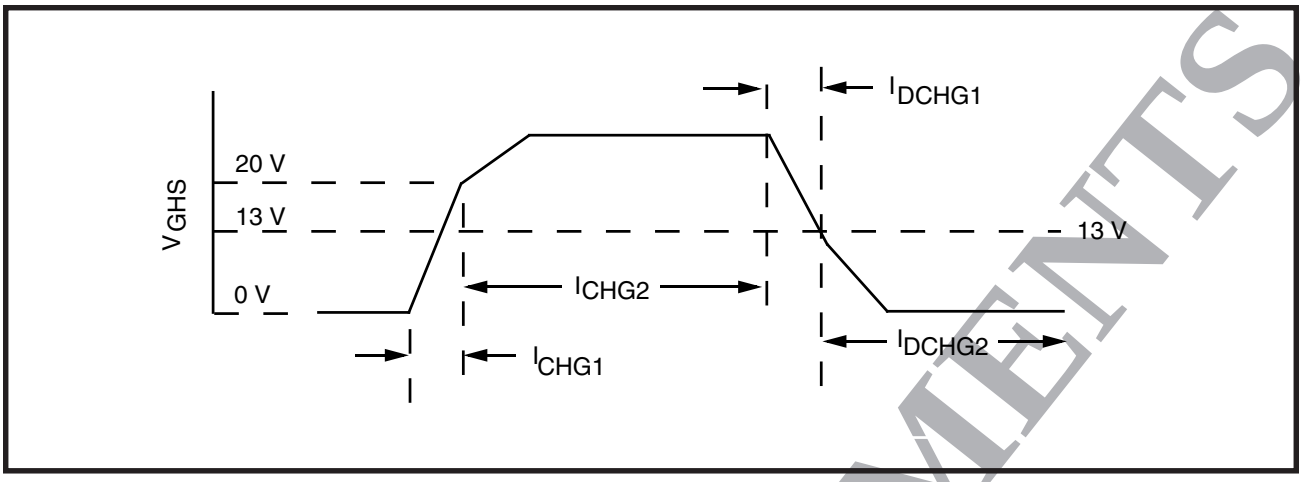


FIGURE 2-14: V_{GHS} During Charging and Discharging

During the discharging interval, switch S2 remains closed until V_{GHS} drops to below ~ 13 V. At this point, S2 opens. Equation 13 is used to calculate the current applied to the gate when S2 is closed. Equation 14 is used to calculate the current applied to the gate when S2 is open.

Figure 2–15 shows the low-side driver circuitry. Equation 15 is used to calculate the charge current, I_{CHG3} . During PWM switching of the low-side drivers, S3 and S4 are open and S5 is closed. Equation 16 is used to calculate the discharge current. Switches S3, S4, and S5 are used to control the discharge current during commutation switching of the low-side drivers. When V_{GLS} is greater than ~ 6 V, both S3 and S4 are closed, S5 is open, and equation 17 is used to determine the current drawn from the gate. As V_{GLS} drops below 6 V, switch S4 opens and equation 18 is used to determine the discharge current.

$$I_{DCHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 15 \quad (13)$$

$$I_{DCHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 3 \quad (14)$$

$$I_{CHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 20 \quad (15)$$

$$I_{DCHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 20 \quad (16)$$

$$I_{DCHG4} = \left(\frac{1.21}{RSLEW}\right) \bullet 22.5 \quad (17)$$

$$I_{DCHG5} = \left(\frac{1.21}{RSLEW}\right) \bullet 7.5 \quad (18)$$

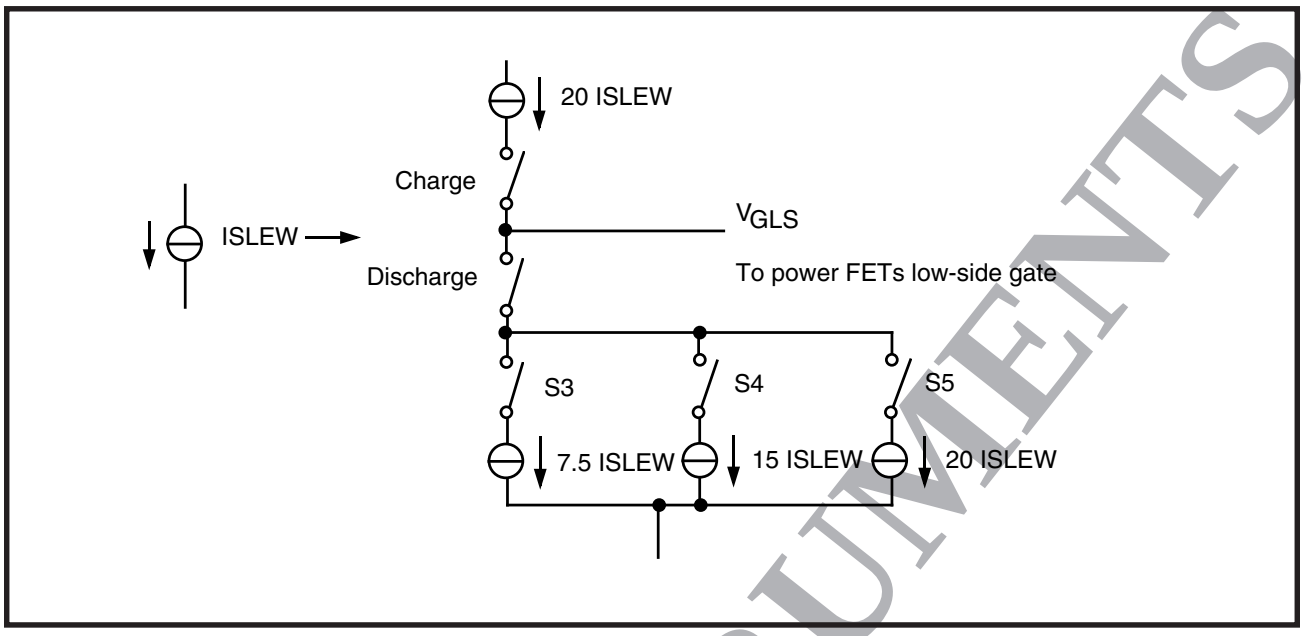


FIGURE 2-15: Low-Side Driver Circuitry

The application of these low-side currents for a single commutation interval is illustrated in Figure 2-16.

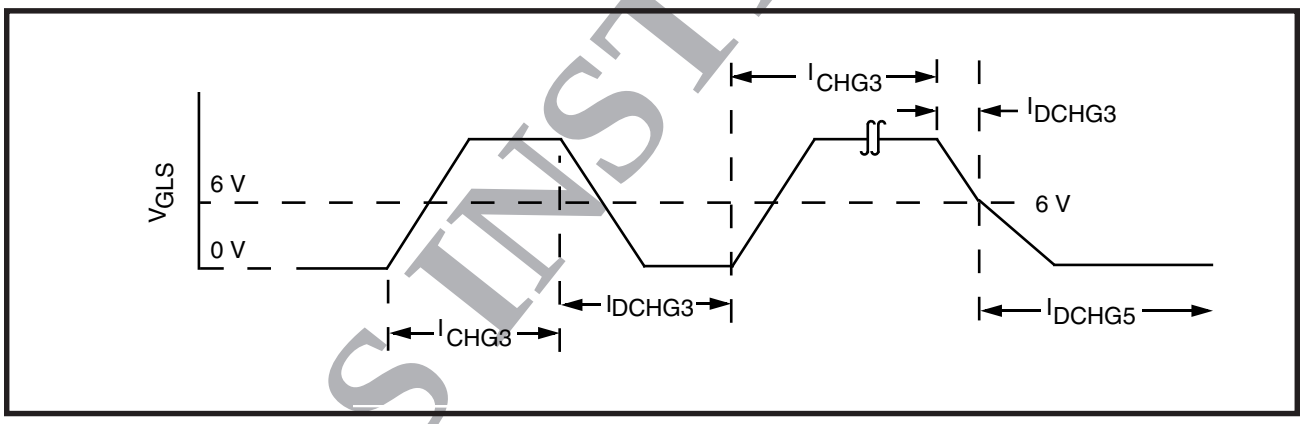


FIGURE 2-16: V_{GLS} for a Single Commutation Interval

NOTE: Adjusting RSLEW also affects the one-shot timing as described in the Start/TACH subsection.

DETAILED DESCRIPTION (continued)

SUPPORT FUNCTIONS

The TLS2231 support functions include:

- Voltage regulator
- Voltage monitor
- Actuator retract control
- Spindle motor brake control
- Voltage reference
- Charge pump

Voltage Regulator

A 5 V on-chip regulator is powered from the voltage at V12, and keeps selected functions such as retract, brake, and spindle commutation powered up and functioning during power brownouts. In case of a complete 5 V and 12 V power fault, the on-chip 5 V regulator supplies power (V5R) by way of the spindle's BEMF to complete actuator retract and spindle braking. To ensure that chip logic is functional during a 12 V fault with no BEMF, a forward biased diode supplies 5 V (minus a V_f diode drop) from V5A to the V5R power bus (see Figure 2–17).

Voltage Monitor

The TLS2231 monitors 5 V and 12 V power and indicates a low condition on PORZ. The voltage monitor is shown in Figure 2–18. Off-chip capacitors are recommended at pins 47 (VCK5)and 48 (VCK12). These capacitors filter the supply voltage to ensure momentary system spikes do not interrupt system operation. The internal resistor dividers set the voltage trip levels, and external resistors can be added if adjustments in trip level are desired.

Figure 2–19 shows the PORZ response to low 5 V or 12 V voltage levels.

The PORZ signal typically is used as a processor reset. Selection of C_{POR} sets the delay (tdly) of PORZ rising after power becomes valid. Equations 19 and 20 define this relationship.

$$t_{dly} = CPOR \bullet \frac{\Delta V}{I} \qquad \Delta V = V1\,P9 \tag{19}$$

$$\text{Note: Again, } \Delta t = \frac{C}{I}\Delta V \qquad I = 5\ \mu A \tag{20}$$

Where: CPOR is in farads.

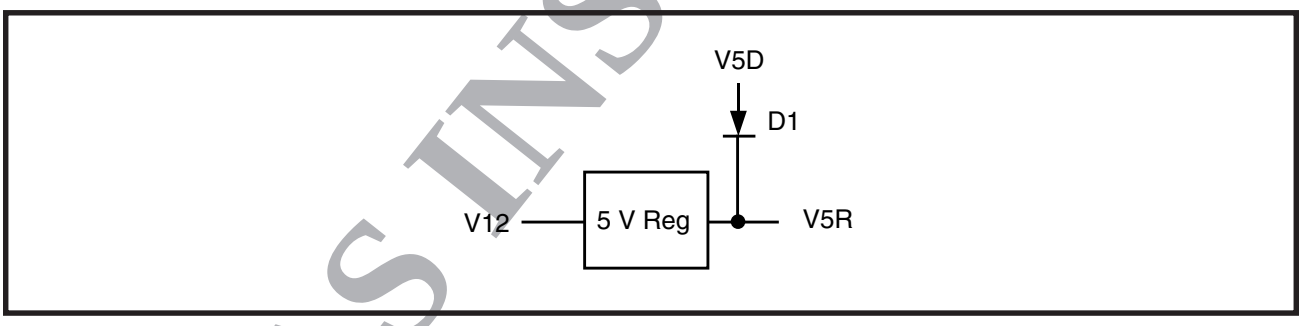


FIGURE 2-17: V5R Power Bus

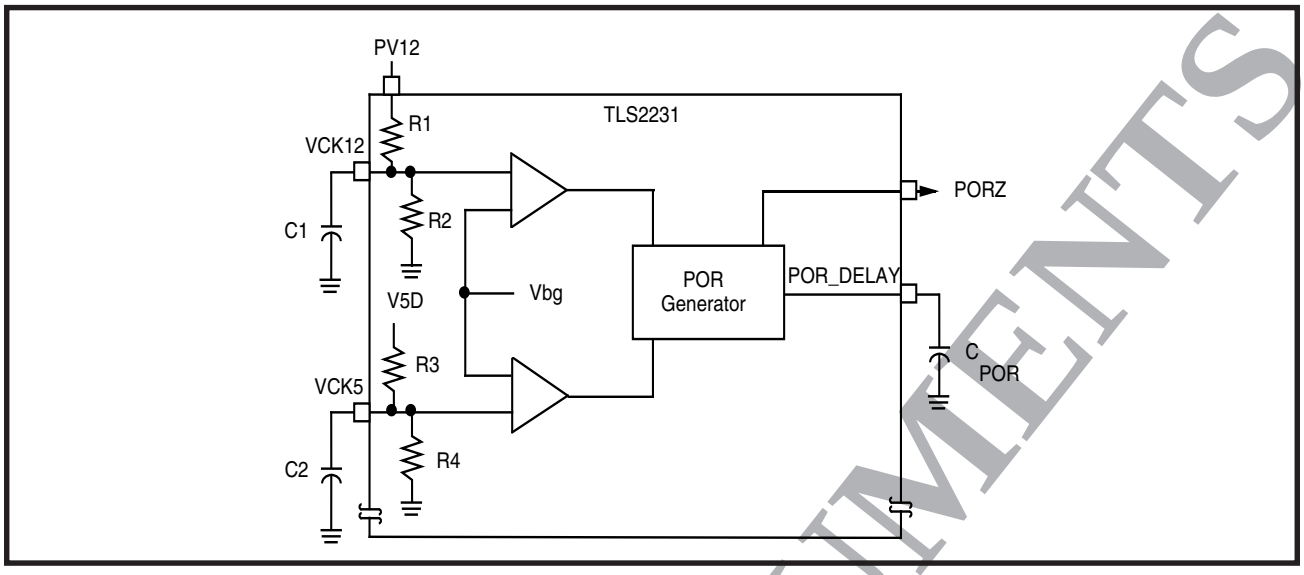


FIGURE 2-18: Voltage Monitor Schematic Diagram

NOTE: R1 = 26 270 Ω nominal
R2 = 3 650 Ω nominal
R3 = 26 270 Ω nominal
R4 = 9 429 Ω nominal
Vbg = 1.21 V nominal

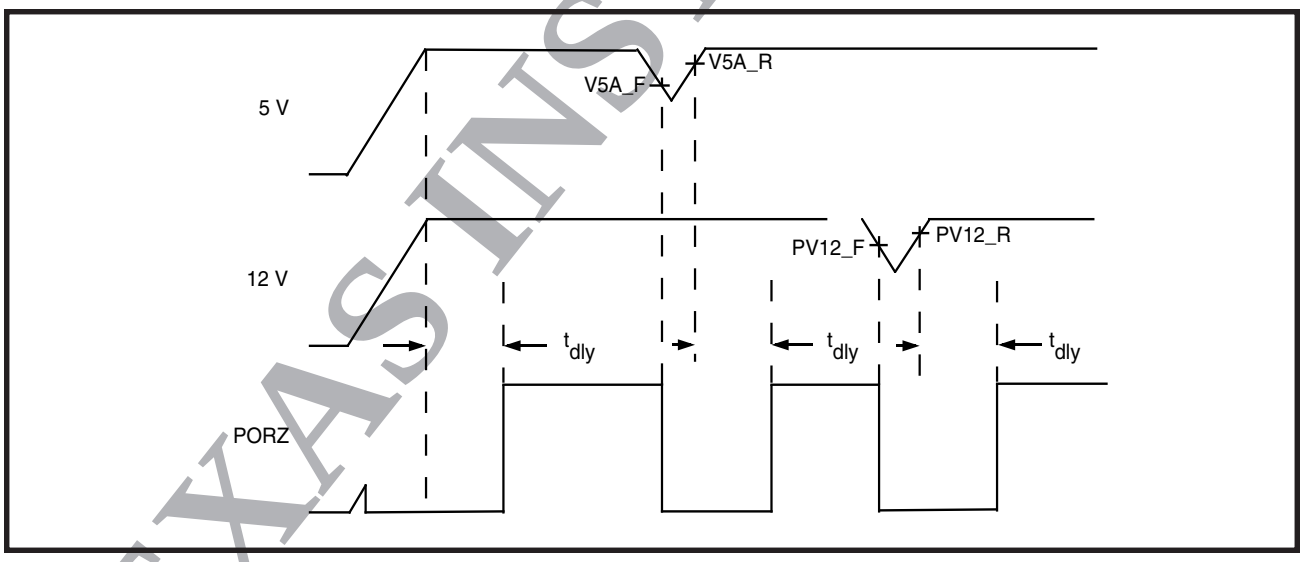


FIGURE 2-19: Voltage Monitor Response to Supply Voltages

SUPPORT FUNCTIONS (continued)

Retract

Figure 2–20 shows the retract control logic. The actuator is immediately retracted on detection of a power fault. The PORZ signal going low causes the retract latch to be set. This causes the signal at RETP to be high, ensuring that Q1 is off and Q2, Q3 and Q4 are all on. This signal also acts as an enable to the voltage control block which outputs the retract voltage on VCMA and 12 V on GNB. The retract voltage is set by the selection of RRET as follows:

$$\text{Retract voltage} = 0.5\ \text{V}\left(1 + \frac{25\ \text{k}\Omega}{5\ \text{k}\Omega + \text{RRET}}\right) \qquad (21)$$

Where: RRET is in ohms.

NOTE: Retract voltage = 0.5 V when RRET = ∞.

During a power-down event, energy from the spindle provides the VCM retract voltage.

The retract voltage to the VCM continues until either a delayed BRAKE occurs (this is indicated by DBRK going high in response to BDLY dropping below 1.2 V as illustrated in Figure 2-21) or until PORZ returns high and then DISPWRZ is set high. If delayed brake is not used and BDLY is held high, then RETP remains set and the retract voltage continues to be applied until power is restored. Then DISPWRZ is set high.

The retract function can also be initiated by applying a logic high at SOFT_RET.

If VCM_ENA is taken low when RETP is not set, then Q1, Q2, Q3, and Q4 are on, ensuring that the VCM is disabled.

NOTE: The TLS2231 provides thermal protection for the retract circuitry. At approximately 150°C, the retract current is disabled. When the temperature drops below 140°C, the retract current is enabled.

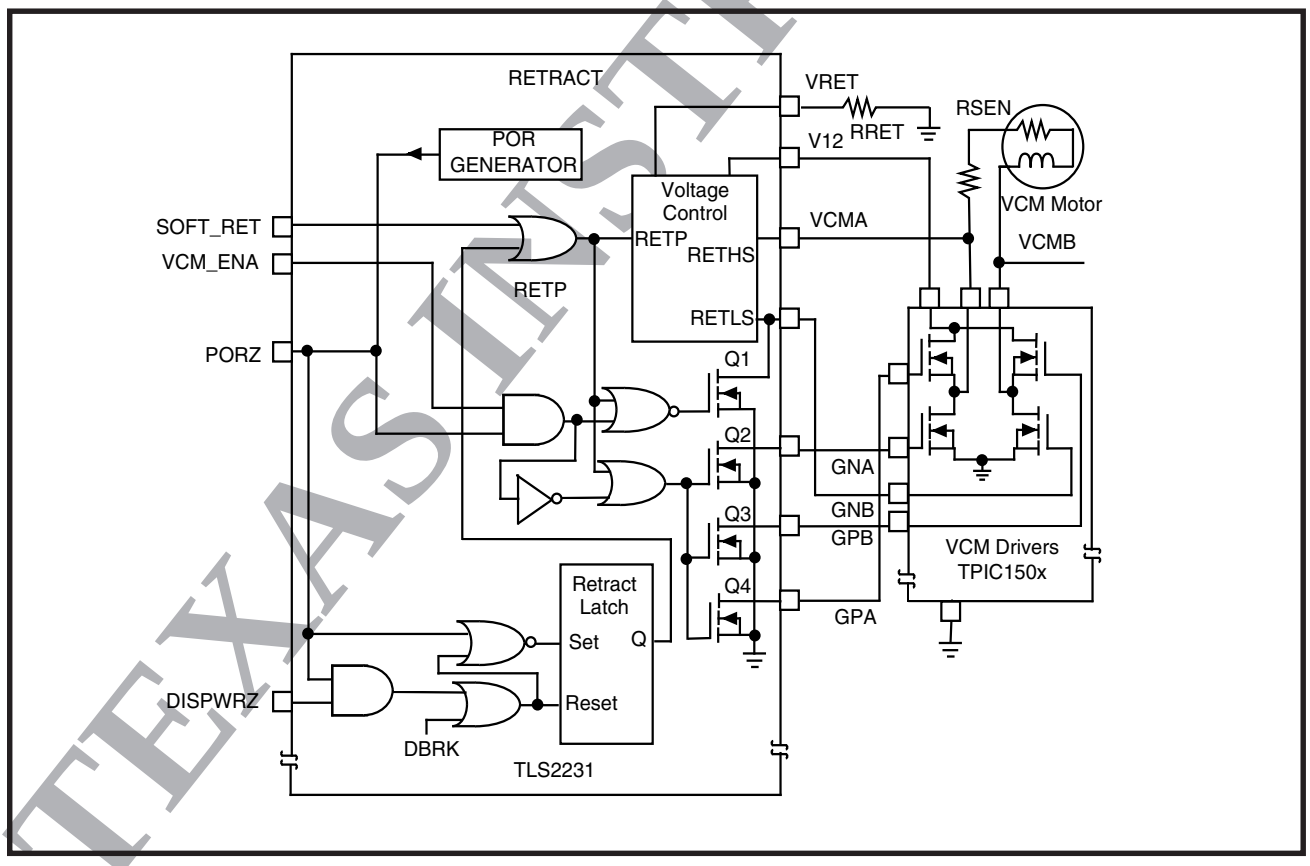


FIGURE 2-20: Retract Function Schematic

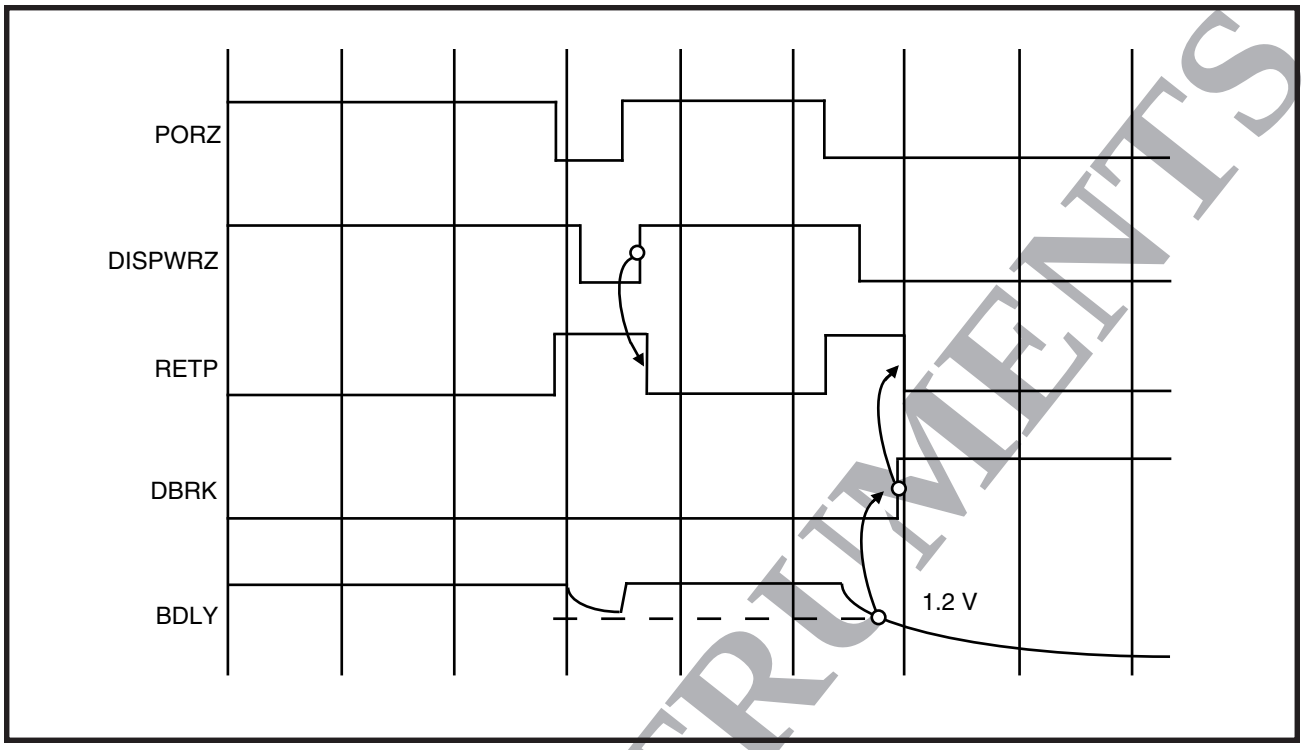


FIGURE 2-21: DISPWRZ, RETP, and SBRK Responses to PORZ and BDLY

SUPPORT FUNCTIONS (continued)

Spindle Brake

Figure 2-22 shows the TLS2231 spindle brake logic.

The brake function turns on all spindle high-side drivers (UHSD, VHSD, and WHSD). The brake function is initiated when SBRK goes high, which sets the brake latch. This is done using software or generating a delayed brake.

Software Brake (SFT_BRK)

A software brake can be commanded by setting RESET to a logic high and both ENABLEZ and DISPWRZ to a logic low.

Delayed Brake (DBRK)

A delayed brake is set after PORZ has been low for a time determined by the selection of Rext and Cext as follows:

$$\text{Brake delay time} = Rext \bullet Cext \bullet \ln\left(\frac{V5D}{Vbg}\right) \quad (22)$$

Where:

Rext is in Ω
Cext is in farads
Ln is natural log
V5D is in volts
V5D = 5 V and Vbg = 1.21 V

NOTE: If the DBRK function is not used it is recommended that the BDLY pin be pulled up to V12 through a 100 kΩ resistor.

Voltage Reference

The TLS2231 generates accurate and stable voltages of 1.9 V and 3.8 V for use both internally and externally.

Charge Pump

The charge pump generates 24 V to drive the TPIC150x high side N-channel FETs. The charge pump requires only one external component, a storage capacitor. The recommended value for the storage capacitor is 1 µF.

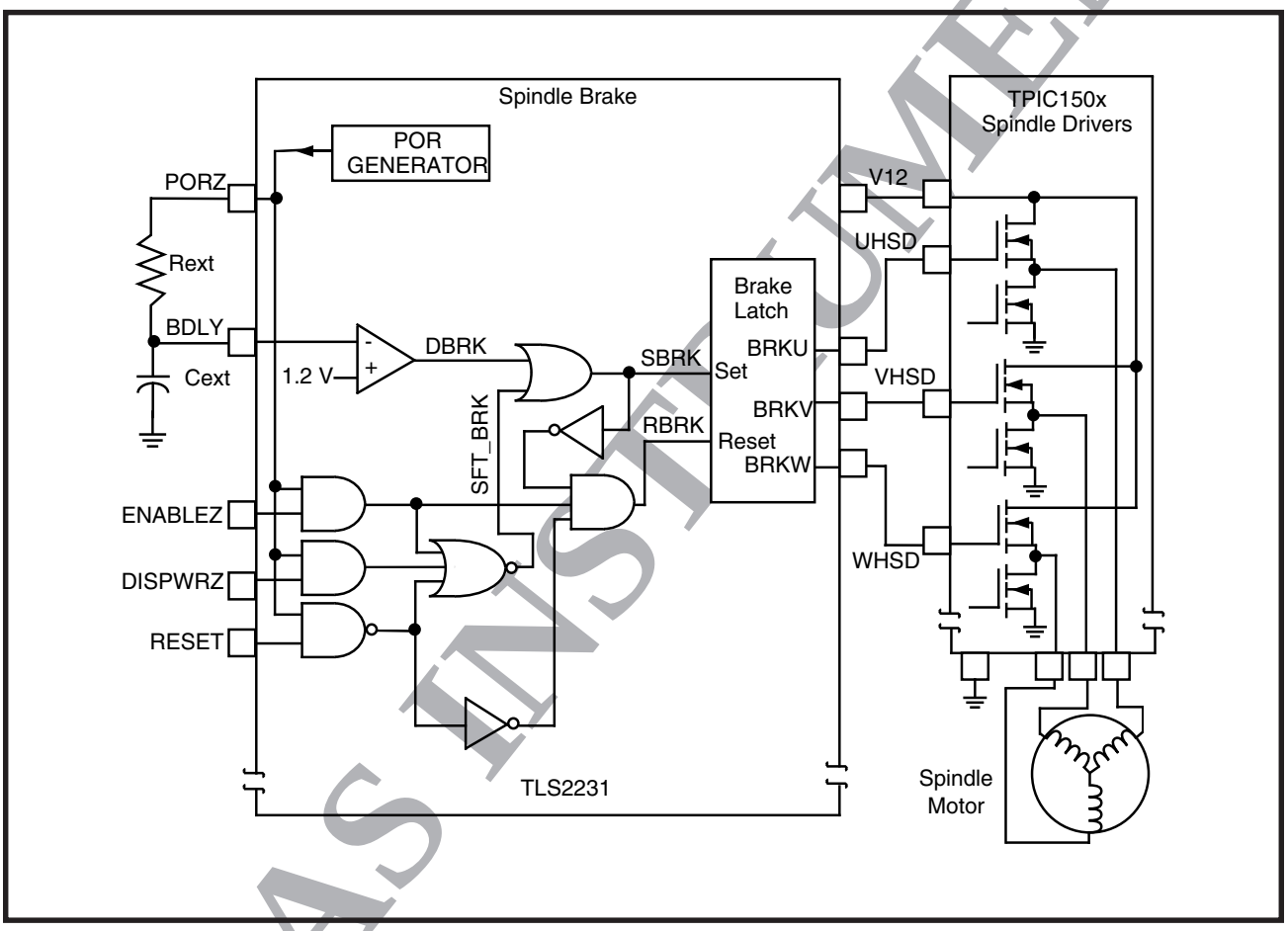


FIGURE 2-22: Spindle Brake Function Schematic

PIN DESCRIPTION

TLS2231Terminal Functions

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
SUPPLIES				
AGND	14		Ground	Analog ground
CP	41	O	Analog	Charge pump storage capacitor connection
DGND	52		Ground	Digital ground
PV12	50	I	Analog	12 V power supply monitor (sensed by voltage monitor to generate PORZ)
V1P9	43	O	Analog	1.9 V reference output
V5A	15		Power	5 V power supply (analog)
V5D	51		Power	5 V power supply (digital)
V3P8	42	O	Analog	Reference output (2 • V1P9)
V12	36		Power	12 V power supply (with blocking diode)
VCM				
A3	33	O	Analog	Filter amplifier output
A3P	34	I	Analog	Filter amplifier noninverting input
ERR	32	O	Analog	VCM current loop error amplifier output
ERRN	35	I	Analog	VCM current loop error amplifier inverting input
GLS	24	O	Analog	Driver sense gate
GNA	29	O	Analog	A low-side driver gate output
GNB	26	O	Analog	B low-side driver gate output
GPA	30	O	Analog	A high-side driver gate output
GPB	28	O	Analog	B high-side driver gate output
ISET	25	O	Analog	Driver sense drain (bias current for class AB operation)
RSEN	23	I	Analog	VCM current-sense feedback. Connects internally to the inverting input of the current-sense differential amplifier
SAT_DET	37	O	Digital	High level indicates VCM drivers are in saturation
SOFT_RET	38	I	Digital	Initiates retract (high level indicates retract)
SOUT	22	O	Analog	VCM current-sense amplifier feedback
VCMA	31	I	Analog	VCM current-sense resistor. Connects internally to the noninverting input of the current-sense differential amplifier and externally to the driver side of the sense resistor
		O	Analog	Retract voltage output
VCMB	27	I	Analog	VCM in. Connects externally between the drivers and the VCM

TLS2231 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
VCM (continued)				
VCM_ENA	39	I	Digital	High level enables the VCM, low level disables the VCM. This signal is ignored during retract.
VRET	45	I	Analog	VCM retract voltage control (voltage controlled by selection of resistor connected externally to this pin)
SPINDLE MOTOR				
ADVANCE	13	I	Digital	Commutation state machine advance (used for spindle start)
COS	6	O	Analog	Capacitor for one-shot timing
CVCO	21	O	Analog	Capacitor to set VCO speed range for motor commutation
DISPWRZ	10	I	Digital	Mode control (low level disables spindle power)
ENABLEZ	12	I	Digital	Mode control (active low)
IFILTER	3	O	Analog	Linear current control filter
KELVIN_SENSE	5	I	Analog	RSENSE ground
PEFILTER	20	O	Analog	Phase error filter for commutation PLL
PU	18	I	Analog	Phase U back EMF sense
PV	17	I	Analog	Phase V back EMF sense
PW	16	I	Analog	Phase W back EMF sense
PWM_IN	4	I	Digital	PWM input for low-side driver (used during PWM start and PWM run modes)
PWM_EN	49	I	Digital	High level selects PWM run, low level selects linear run
RESET	11	I	Digital	Mode control (active high) (resets VCO and state machine)
RSENSE	8	I	Analog	Spindle current-sense voltage feedback (high side of RSENSE)
RSLEW	9	O	Analog	Current setting control for spindle driver, slew rates, and one-shot timing used in the constant off-time spindle motor current regulator
SENSE/VCO/TACH	19	O	Digital	MUX output: Current threshold SENSE during start mode. VCO during preset mode or run mode. TACH during coast mode.
UHSD	55	O	Analog	U high-side driver gate output
ULSD	2	O	Analog	U low-side driver gate output
VHSD	54	O	Analog	V high-side driver gate output

TLS2231 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
SPINDLE MOTOR (continued)				
VLSD	1	O	Analog	V low-side driver gate output
WHSD	53	O	Analog	W high-side driver gate output
WLSD	56	O	Analog	W low-side driver gate output
V_ICNTRL	7	I	Analog	Motor current control
VOLTAGE MONITOR (VM)				
BDLY	44	I	Analog	Brake delay, retract time-out
PORZ	46	O	Digital	Power on reset (active low)
POR_DELAY	40	O	Analog	Capacitor to set PORZ delay
VCK5	47	O	Analog	Low V5D voltage monitor filter/threshold set
VCK12	48	O	Analog	Low PV12 voltage monitor filter/threshold set

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted) †

PARAMETER		RATING
Supply voltage	V12, PV12 (see Note 1)	15 V
Supply voltage	V5D, V5A (see Note 1)	7 V
Negative voltage applied to any pin	(see Note 2)	–0.5 V
Power dissipation	T_A = 70°C	1 W
Charge pump output voltage		26 V
Operating free-air temperature range		0°C to 70°C
Operating virtual junction temperature	T_J	≤ 150°C
Thermal resistance: Junction-to-case	$R_{\theta JC}$	27.3°C/W
Storage temperature range	T_{stg}	–55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground.
NOTE 2: The maximum negative voltage can be affected by either temperature or current.

RECOMMENDED OPERATING CONDITIONS OVER RECOMMENDED SUPPLY VOLTAGE, T_A = 25°C (see Note 3)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply voltage V5A, V5D	VCK5 = 5 V	4.75	5	5.25	V
Supply voltage PV12	VCK12 = 5 V	10.8	12	13.2	V
Supply voltage V12	VCK12 = 5 V	10.3	11.5	12.7	V
Digital high-level input voltage V_{IH}		3.5		V5D+0.3	V
Low-level input voltage V_{IL}		–0.4		0.5	V
Voltage applied to any pin		–0.4			V

NOTE 3: These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

Total Device Over Recommended Supply Voltage

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply Current	I_{DD}	I_{PV12}			600	µA
		I_{V12}			25	mA
		I_{V5}			10	mA
High-level logic input current (see Note 4)	I_{IH}	At ENABLEZ, DISPWRZ, or RESET V_{IH} = 5 V			70	µA
		At PWM_IN,PWM_EN, SOFT_RET, or VCM_ENA V_{IH} = 5 V			1	µA
Low-level logic input current	I_{IL}				–1	µA
Low-level output voltage	V_{OL}	I_O = –20 µA			0.1	V
High-level output voltage	V_{OH}	I_O = 20 µA	V5D – 0.1 V			V

NOTE 4: There are internal 120 kΩ pulldown resistors on ENABLEZ, DISPWRZ, and RESET.

Voltage Monitor (see Note 5)

Falling 12-V voltage, PORZ	PV12_F		9.5	9.8		V
Rising 12-V voltage, PORZ	PV12_R			10	10.4	V
Hysteresis 12 V, PORZ			50	250	500	mV
Falling 5 V voltage, PORZ	V5A_F		4.4	4.5		V
Rising 5 V voltage, PORZ	V5A_R			4.6	4.7	V
Hysteresis 5 V, PORZ			50	100		mV
Short-circuit output current, PORZ	I_{OS}	V_{OL} = 0.5 V	375		650	µA
Low-level output current, PORZ	I_{OL}				–5	mA
High-level output voltage, PORZ	V_{OH}	V5D = 5 V, I_{OH} = 100 µA	3.5	4		V
Low-level output voltage, PORZ	V_{OL}	V5D = 5 V, I_{OL} = –5 mA		0.3	0.5	V

NOTE 5: As the power goes up and/or down, comparators and band gap voltage are available at 1.5 V for 5 V supply and 2.5 V for 12 V supply, which allows proper driver disabling through the power-up process.

PORZ Minimum Supply Threshold, PORZ I_{OL} = –5 mA (see Note 6)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V5A (rising from 0)	PV12 = 0 V		0.92	1.5	V
PV12 (rising from 0 to 3.0 V)	V5A = V5D = 0 V		2.52	3.0	V

NOTE 6: Typical and maximum values indicated for valid PORZ.

Retract (see Note 7)

Mimimum retract voltage range at VCMA†	VCMA I_O = 50 mA, VRET = OPEN	0.4		0.6	V
Maximum retract voltage range at VCMA†	VCMA I_O = 50 mA, VRET = GND	2.4	3	3.6	V
Retract current limit	VCMA = GND, VRET = OPEN	100	135	170	mA
Retract voltage accuracy†	VCMA IO = 50 mA VRET tied 7.5 kΩ to GND	1	1.5	2	V
Voltage on GPA, GPB, GNA				0.7	V
Voltage GNB		V12–1			V

NOTE 7: Retract is disabled when temperature exceeds 150°C. This parameter is tested in terms of voltage using the factory mode Test2.

† These parameters are not tested. They are determined by design characterization.

Braking Circuit

VLSD OFF	Software brake			0.7	V
VHSD HIGH	Software brake	20			V
Leakage current, C_{BDLY}	V_{BDLY} = 5 V			200	nA
Brake threshold voltage, BDLY		0.8	1.2	1.4	V

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

Charge Pump (see Notes 8 and 9)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Charge pump output voltage	V12 = 12 V, V5D = 5 V	22	25	26	V
Charge pump output voltage load regulation†	See Note 10		0.015	0.025	V/µA
Oscillator frequency†			4		MHz
Charge time †			0.5		s
Charge pump leakage current	V12 = 0, V5D = 0, V_{cp} = 16 V			250	nA

NOTE 8: External storage capacitor is typically 1 µF.
NOTE 9: Minimum voltage, that should be maintained on the charge pump to ensure successful delayed brake, is typically 18 V for any TPIC150x device. However, this voltage is a function of the current that the power driver sinks and the power dissipated in the device.
NOTE 10: The output can drive external N-channel DMOS switches; the effective dc loading should be less than 1 µA.

† These parameters are not tested. They are determined by design characterization.

Voltage Reference (see Note 11)

V1P9 output	Load 3 mA, –80 µA	1.824	1.9	1.978	V
V3P8 output	Load 3 mA, –80 µA	3.648	3.8	3.952	V
Ratio of V3P8 to V1P9		1.96	2	2.04	V/V
V1P9 source current (see Note 12)				3	mA
V3P8 source current (see Note 13)				3	mA
V1P9 sink current (see Note 12)		–80			µA
V3P8 sink current (see Note 13)		–80			µA

NOTE 11: Maximum external capacitive load = 10 µF. TI recommends a load of 1 µF with a 1 mA dc load.
NOTE 12: Verified from V1P9 output test.
NOTE 13: Verified from V3P8 output test.

VCM Input-Filter Amplifier (A3)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input bias current	I_{IB}		–1		1	µA
Input offset voltage	V_{IO}		–10		+10	mV
Average temperature coefficient of input offset voltage†	VIO			15		µV/C
Slew rate†	SR	R_L = 10 kΩ ,C_L = 60 pF		1		V/µs
Gain (see Note 14)	G		1.9	2	2.1	V/V
Gain bandwidth product†	GBN			1		MHz
Open-loop voltage gain†		f = 1 kHz, R_L = 10 kΩ		60		dB
Supply voltage rejection ratio†	PSRR		60	70		dB
Common mode rejection ratio†	CMRR			60		dB
Input voltage range, with respect to V1P9†	V_{IC}			±1.9		V
Output swing, with respect to V1P9	V_{OPP}	R_L = 10 kΩ (tied to V1P9 level)	–1.5		+ 1.5	V

NOTE 14: Filter gain set internal to device
† These parameters are not tested. They are determined by design characterization.

VCM Current-Loop-Error Amplifier (ERR)

Input bias current	I_{IB}		–1		1	µA
Input offset voltage	V_{IO}		–10		10	mV
Average temperature coefficient of input offset voltage†	VIO			15		µV/C
Slew rate†	SR	R_L = 10 kΩ C_L = 60 pF to V1P9		1		V/µs
Gain bandwidth product†	GBW			1		MHz
Open-loop voltage gain†		f = 1 kHz, R_L = 10 kΩ		70		dB
Supply voltage rejection ratio†	PSRR		60	70		dB
Common mode rejection ratio†	CMRR			60		dB
Input voltage range, with respect to V1P9†	V_{IC}			±1.9		V
Output swing, with respect to V1P9	V_{OPP}	R_L = 10 kΩ (tied to V1P9 level)	–1.5		+ 1.5	V

† These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

VCM Current-Sense Amplifier (ASEN)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input offset voltage	V_{IO}	Measured at SOUT with respect to V1P9 (RSEN tied to VCMA)	–5	0	+5	mV
Gain	G		2.67	2.73	2.79	V/V
Slew rate†	SR	R_L = 10 kΩ, C_L = 60 pF		1		V/µs
Gain bandwidth product†	GBW			1		MHz
Open-loop voltage gain†		f = 1 kHz, R_L = 10 kΩ		66		dB
Supply voltage rejection ratio†	PSRR		60			dB
Common mode rejection ratio	CMRR	V_{CMRR} 0.5 V to 11.5 V	55			dB
Common mode input voltage†	V_{IC}		0		12	V
Output swing, with respect to V1P9	V_{OPP}	R_L = 5 kΩ (tied to V1P9 level)	–1.5		+ 1.5	V

† These parameters are not tested. They are determined by design characterization.

VCM Predriver Amplifier

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage GPA, GPB	V_{OH}	R_L = 6 MΩ	20			V
High level output voltage GNA, GNB	V_{OH}	R_L = 6 MΩ	V12–2			V
Low-level output voltage GPA, GPB	V_{OL}				0.7	V
Low level output voltage GNA, GNB	V_{OL}				0.7	V
Slew rate, positive† GPA, GPB	SR+	C_L = 50 pF, see Note 15		0.5		V/µs
Slew rate, positive† GNA, GNB	SR+	C_L = 50 pF, see Note 16		0.5		V/µs
Slew rate, negative† GPA, GPB	SR–	C_L = 50 pF, see Note 17		2		V/µs
Slew rate, negative† GNA, GNB	SR–	C_L = 50 pF, see Note 17		2		V/µs
Quiescent current†				8		mA
Gain†	G	VCMA to VCMB		12		V/V
Unity gain bandwidth†				1		MHz
Common-mode rejection ratio†	CMRR		60			dB
Power supply rejection ratio†	PSRR		60			dB

NOTE 15: Slew rate measured as average positive slew rate from 1 V to 18 V
NOTE 16: Slew rate measured as average positive slew rate from 1 V to 10 V
NOTE 17: Slew rate measured as average negative slew rate from 18 V to 1 V

† These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

VCO (unless otherwise specified, CVCO = 0.0042 μF)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Typical frequency† f	$\left(\frac{VPE}{2 \cdot 30.48\ k\Omega \cdot V1P9 \cdot CVCO}\right)$				Hz
	$V_{0(PEFILTER)}$ = 2.1 V	3456	4320	5184	Hz
Idle frequency†	Mode = Reset	160	200	240	Hz
High-side CVCO voltage trip level	Ramp CVCO from 2.5 V to 3.2 V	2.6	2.85	3.1	V
Low-side CVCO voltage trip level	Ramp CVCO from 1.1 V to 0.8 V	0.85	0.95	1.05	V
Source/Sink Current (CVCO)	PEFILTER = 3 V	75	100	125	μA
Low-level output voltage V_{OL} (–100 μA), SENSE/VCO/TACH				0.5	V
High-level output voltage V_{OH} (100 μA),SENSE/VCO/TACH		3.5			V
Rise/fall time (SENSE/VCO/TACH) †	C_L = 10 pF		100		ns

† These parameters are not tested. They are determined by design characterization.

Phase-Error Amplifier

Output voltage V_O $V_{PEFILTER}$, (V_{idle})	Mode = Preset	75	100	125	mV
Output current at PEFILTER, run mode I_O	$V_{0(PEFILTER)}$ = 2.1 V	115	150	175	μA
Source/sink current mismatch	$V_{0(PEFILTER)}$ = 2.1 V	–7%		+7%	
Input offset voltage † V_{IO} PU, PV, or PW See Note 18	PU, PV, or PW	–180		+180	mV
Maximum voltage † PU, PV, and PW				15	V

NOTE 18: Add 100 Ω resistor in series with PU, PV, and PW inputs to prevent high reverse (below ground) current during start.

† These parameters are not tested. They are determined by design characterization.

Spindle-Predriver Amplifier

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage UHSD, VHSD, WHSD	V_{OH}	R_L = 6 MΩ	20			V
Low-level output voltage UHSD, VHSD, WHSD	V_{OL}				0.7	V
High-level output voltage ULSD, VLSD, WLSD	V_{OH}	R_L = 6 MΩ	V12–2			V
Low-level output voltage ULSD, VLSD, WLSD	V_{OL}				0.7	V

Spindle Current-Sense Amplifier

Input voltage range†			0		0.5	V
Closed-loop gain	G	I_{CAL}	6.75	7.5	8.25	V/V
Output swing†	V_{OPP}		0.1		4.5	V
Input offset voltage†	V_{IO}			8		mV

†These parameters are not tested. They are determined by design characterization.

Current-Sense Comparator

Input offset voltage†	V_{IO}			10		mV
Common mode†			0		4	V

†These parameters are not tested. They are determined by design characterization.

TACH Comparator

Input offset voltage	V_{IO}		–10		+10	mV
Hysteresis	V_{hys}		75	100	125	mV
Common mode†			0		4	V

†These parameters are not tested. They are determined by design characterization.

Motor Current Control

I_COS_CHG		80	100	120	µA
I_COS_DCHG		3			mA
One-shot off time (see Note 19)	C_{OS} = 0.001 µF, R_{SLEW} = 12.1 kΩ	15	25	35	µs
V_ICNTRL deadband†		80	95	110	mV

NOTE 19: Minimum one-shot off time regardless of COS and RSLEW values is typically 5 µs.
†These parameters are not tested. They are determined by design characterization.

MECHANICAL DATA

Figure 4-1 shows mechanical outline dimensions.

DL (R-PDSO-G56) **PLASTIC SMALL OUTLINE PACKAGE**

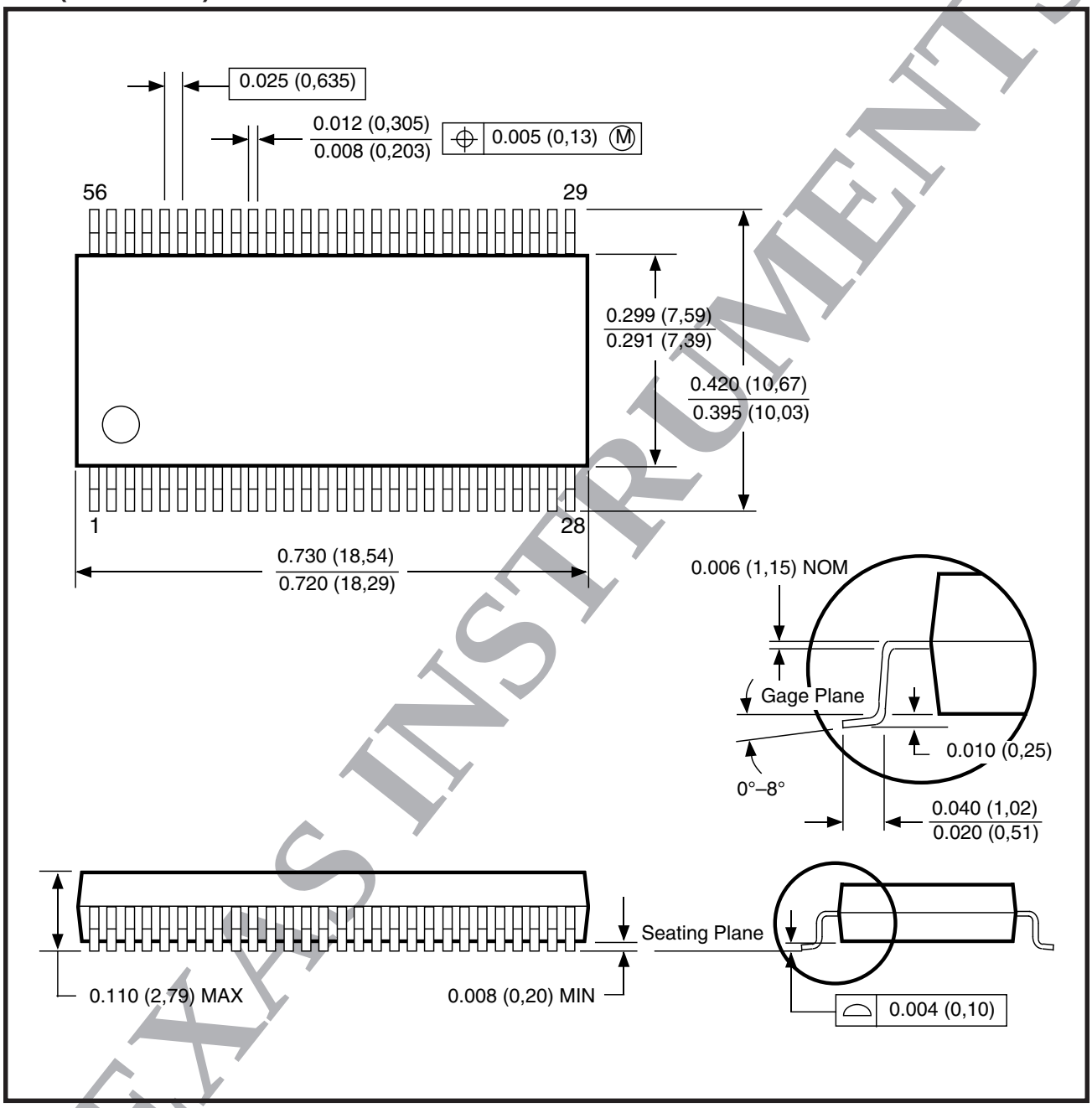


FIGURE 4-1: Mechanical Data

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

TABLE A-1: System Level Responses to Various Inputs

POR	DBRK	V12	SBRK	VCM_ENA	SFT_RES	RESET	ENABLEZ	DISPWRZ	SOFTWARE MODE (as selected by RESET, ENABLEZ, and DISPWRZ)	SPIN MOTOR	GPA, GPB, GNA	GNB	VCM_RET	VCM_BRK	VCM	RETRACT
1	0	>10.4 V	0	1	0	0	0	1	RUN	RUN	ON	ON	0	0	ON	OFF
1	0	>10.4 V	0	X	1	0	0	1	RUN	RUN	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	0	0	0	0	0	1	RUN	RUN	LOW	LOW	1	1	OFF	OFF
1	0	>10.4 V	1	1	0	1	0	0	BRAKE	BRAKE	ON	ON	0	0	ON	OFF
1	0	>10.4 V	1	X	1	1	0	0	BRAKE	BRAKE	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	1	0	0	1	0	0	BRAKE	BRAKE	LOW	LOW	1	1	OFF	OFF
1	0	>10.4 V	0	1	0	0	0	0	COAST	COAST	ON	ON	0	0	ON	OFF
1	0	>10.4 V	0	X	1	0	0	0	COAST	COAST	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	0	0	0	0	0	0	COAST	COAST	LOW	LOW	1	1	OFF	OFF
0	0	>2 V	X	X	X	X	X	X	XXX	COAST	LOW	HI	1	0	OFF	ON
0	1	>2 V	X	X	X	X	X	X	XXX	BRAKE	LOW	LOW	1	1	OFF	OFF

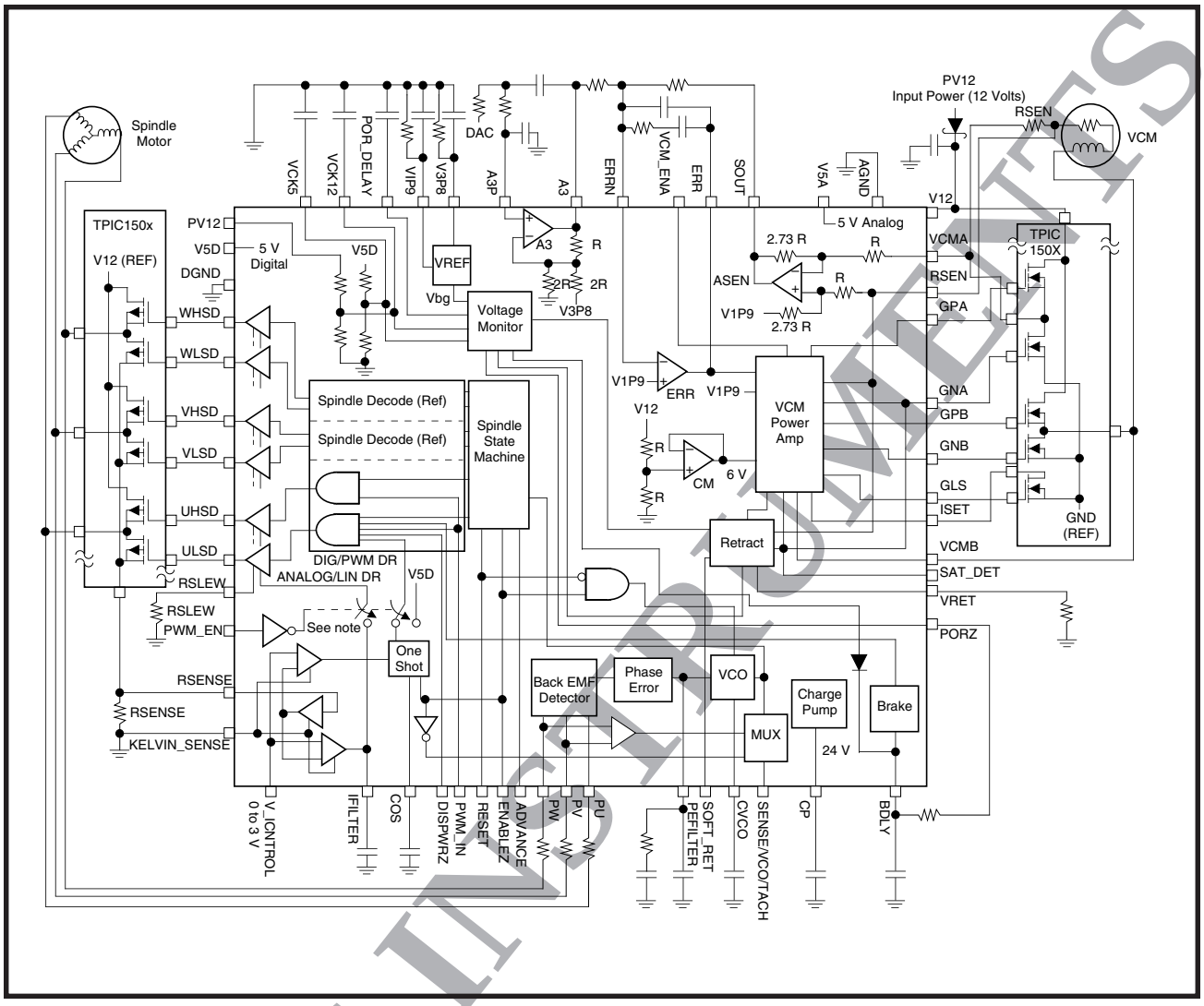


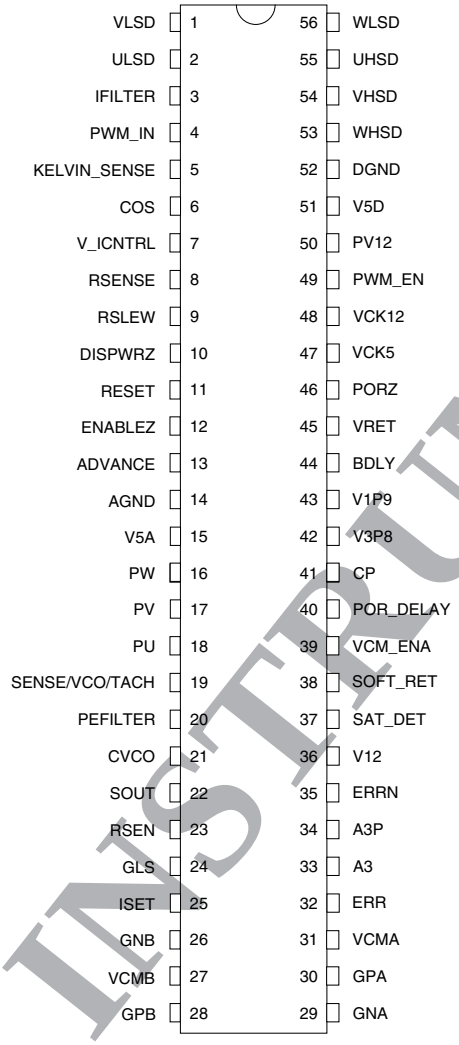
FIGURE 4-1: Typical Application

NOTES: A. All external FETs are located in TPIC150x drive array.
B. During linear drive, the digital/PWM drive is disconnected from the one-shot and tied to supply rail. Also the IFILTER or the output of the OTA is tied to linear drive.
C. During PWM mode, output of the OTA or IFLITER is disconnected from the analog/linear drive, and digital drive is connected to the one-shot output.

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



TLS2231
DL Package

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TI TLS2231 56-Pin Servo-Combination Predriver	**TLS2231CDLR**	**T2231CB**

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

TLS2232
Servo-Combination Predriver

July 1998

DESCRIPTION

The TLS2232 (Figure 1–1) is a servo-combination predriver designed for use in hard disk drive applications. The predriver, when used in combination with the TPIC150x, can drive a voice-coil motor (VCM) and a spindle motor.

FEATURES

VOICE-COIL MOTOR PREDRIVER

- **Linear input control**
- **Transconductance amplifier with class AB output (when used with TPIC150x drivers)**
- **Saturation detection of VCM drivers**
- **Summing amplifier**
- **Current-sense amplifier**
- **Retract function on power loss or on software command**
- **External set for retract voltage**

SPINDLE MOTOR PREDRIVER

- **Pulse width modulated (PWM) start and PWM current limit**
- **Advance terminal signals commutation timing to on-chip sequencer during start mode**
- **Current-sense comparator**
- **Low noise phase-locked loop performs commutation timing during run mode**
- **PWM run**
- **Dynamic brake**
- **Power-down brake after delay**
- **KELVIN_SENSE input to reduce current-sense errors induced by ground level variances**

SUPPORT FUNCTIONS

- **Voltage monitor (based on 5 V and 12 V supplies)**
- **Low-voltage brake**
- **Charge pump (24 V) for driving N-channel DMOS H-bridge drivers**
- **Gated charge pump output for driving external power supply isolation FET.**

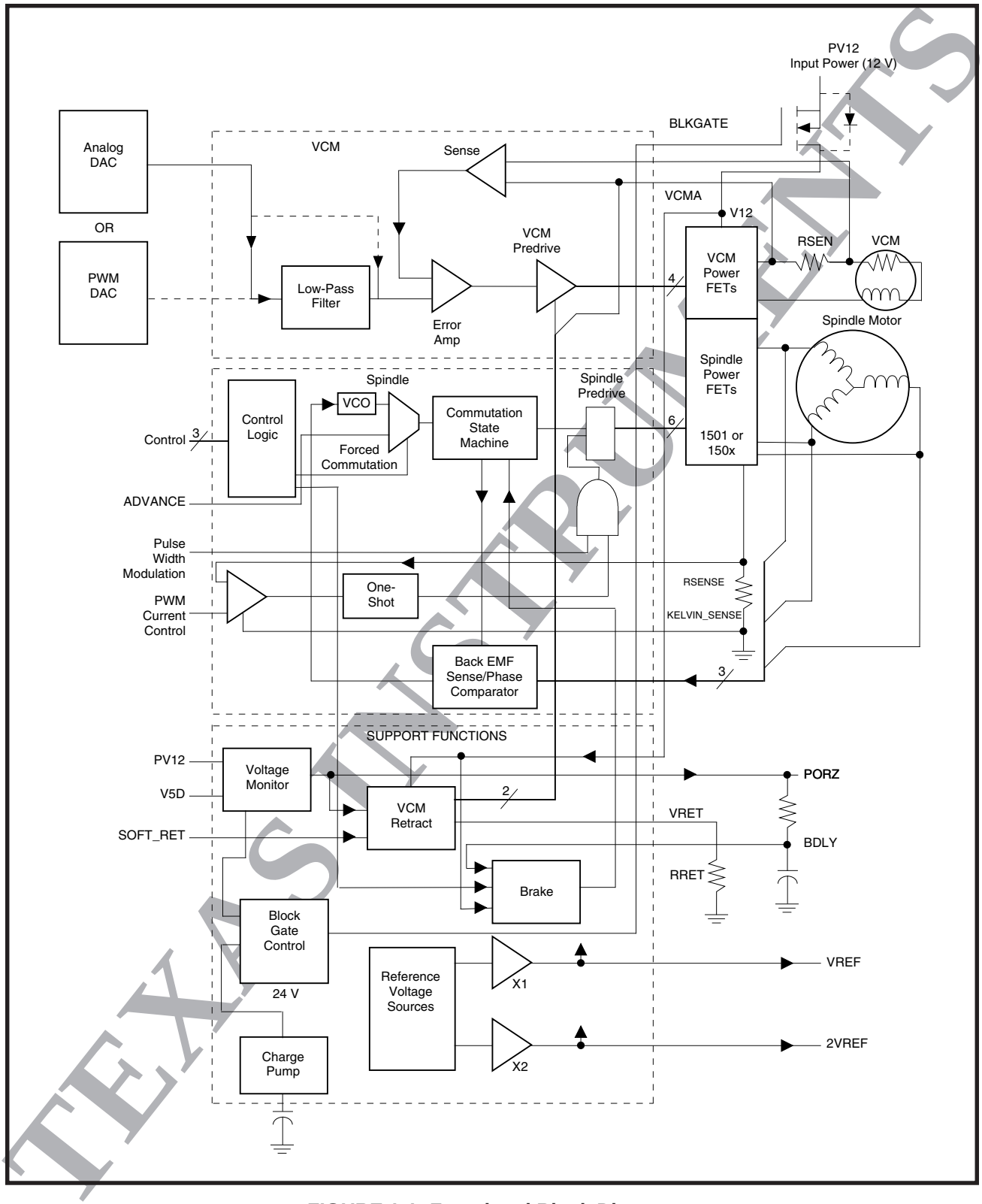


FIGURE 1-1: Functional Block Diagram

FUNCTIONAL DESCRIPTION

VOICE-COIL MOTOR DRIVE

The TLS2232 uses a linear voltage to control the current applied to the VCM. An input amplifier is provided for convenient filtering of the input voltage command. This amplifier may also be used to filter the output of a PWM DAC. Its bandwidth is determined by the selection of external components. The error amplifier implements a transconductance loop. The error amplifier output represents the difference between the command current and the actual current. The actual current is measured across the RSEN resistor by the sense amplifier. The compensated output of the error amplifier is applied to the VCM predrive circuit that biases the VCM power field-effect transistors (FETs) of the TPIC150x.

SPINDLE MOTOR DRIVE

The spindle motor is started under PWM control using an external signal for forced commutation. As the motor approaches operational speed, the commutation state machine is driven by the output of the voltage-controlled oscillator (VCO). The VCO utilizes the back EMF (BEMF) of the motor to close a phase-locked loop that matches the commutation frequency to the motor. Once in the run mode, the motor speed can be controlled using a PWM signal to modulate the current applied to the motor.

SUPPORT FUNCTIONS

The TLS2232 support functions include a voltage monitor that indicates a fault when power supply voltages drop below a specified threshold. When triggered, the fault signal initiates a VCM retract and can also initiate delayed braking of the spindle motor. It also switches the gate drive signal which is applied to an external blocking FET. This isolates the system's power from the rectified power that appears across the spindle motor. The VCM retract voltage is set by the selection of an external resistor. Other support functions include the on-chip reference voltage and the charge pump. The reference voltages are used internally and are also available for external use. The charge pump generates 24 V for driving the N-channel DMOS H-bridge drivers of the TPIC150x.

DETAILED DESCRIPTION

VOICE-COIL MOTOR PREDRIVER

The TLS2232, when combined with a power driver such as the TPIC150x, provides current drive capability for a VCM. Figure 2–1 shows the functional block diagram of a typical application. A signal applied to the input filter amplifier, A3, as shown indicates the level of current to be delivered to the VCM. This signal is low-pass filtered by amplifier A3 and applied to the error amplifier ERR.

NOTE: The input signal may be applied directly to the error amplifier, bypassing A3, if low pass filtering is not required.

The error amplifier implements a transconductance loop. Its output is the difference between the commanded current and the actual current as measured across RSEN by the differential amplifier ASEN. This error signal is applied to the predriver amplifier that biases the power FETs of the TPIC150x for class AB operation.

NOTE: The GNA and GNB terminals can be connected to external 10 MΩ to 20 MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2232.

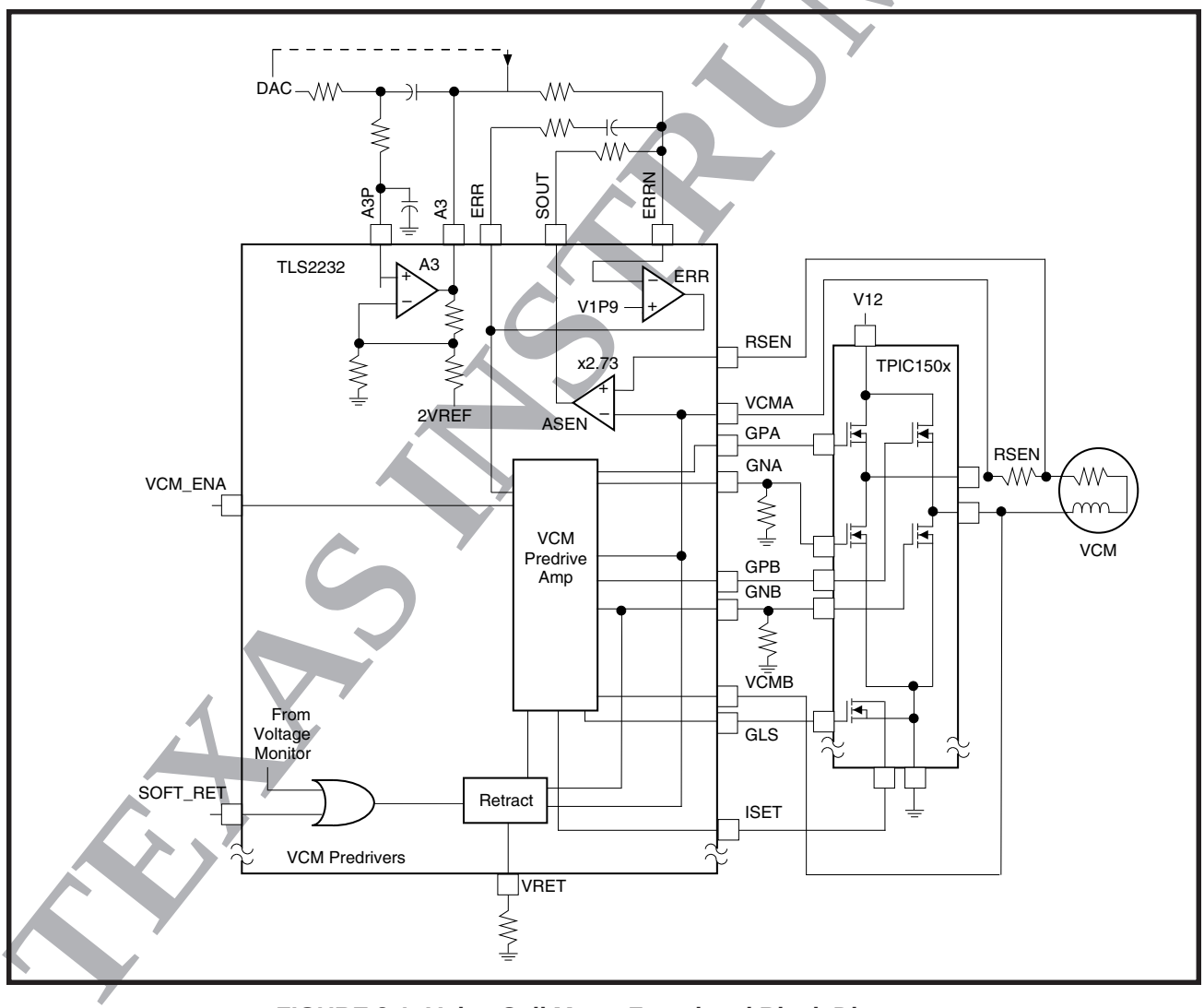


FIGURE 2-1: Voice-Coil Motor Functional Block Diagram

Input Filter Amplifier (A3)

The input filter amplifier (A3) filters the applied input. This amplifier can be used to implement a Sallen and Key filter as shown in Figure 2–2.

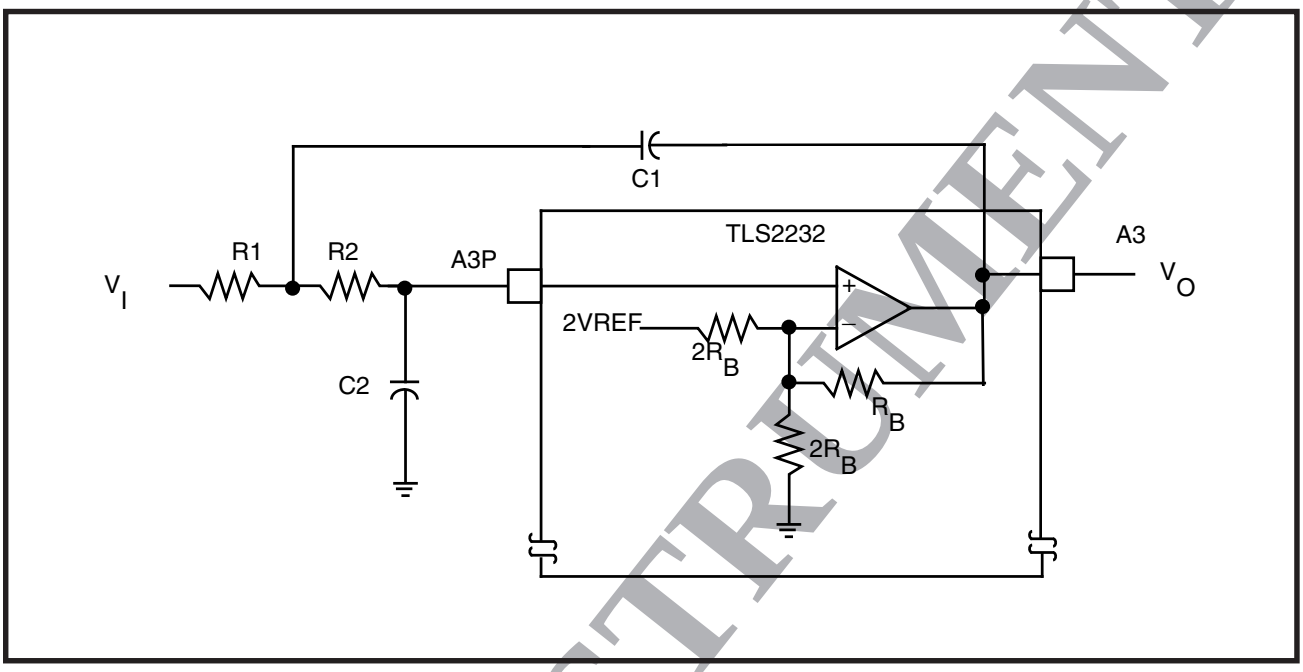


FIGURE 2-2: Sallen and Key Low-Pass Filter Implementation

Equations 1, 2, 3, and 4 show the transfer function of this circuit.

$$H(S) = \frac{K\omega^2}{S^2 + \frac{\omega}{Q}S + \omega^2} \quad (1)$$

$$K = 1 + \frac{R_B}{2R_B \| 2R_B} = 2;\ R_B \text{ matched internal components} \quad (2)$$

$$Q = \frac{1}{3 - K} = 1 \quad (3)$$

$$\omega = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \quad (4)$$

R1, R2, C1, and C2 are chosen to match ω to the applied input signal.

VOICE-COIL MOTOR PREDRIVER (continued)

Summing Amplifier (ERR)

The summing amplifier (ERR) generates an error signal that is proportional to the difference between the command current and the actual current. Selection of the external components provides compensation for the transconductance loop (see Figure 2–3).

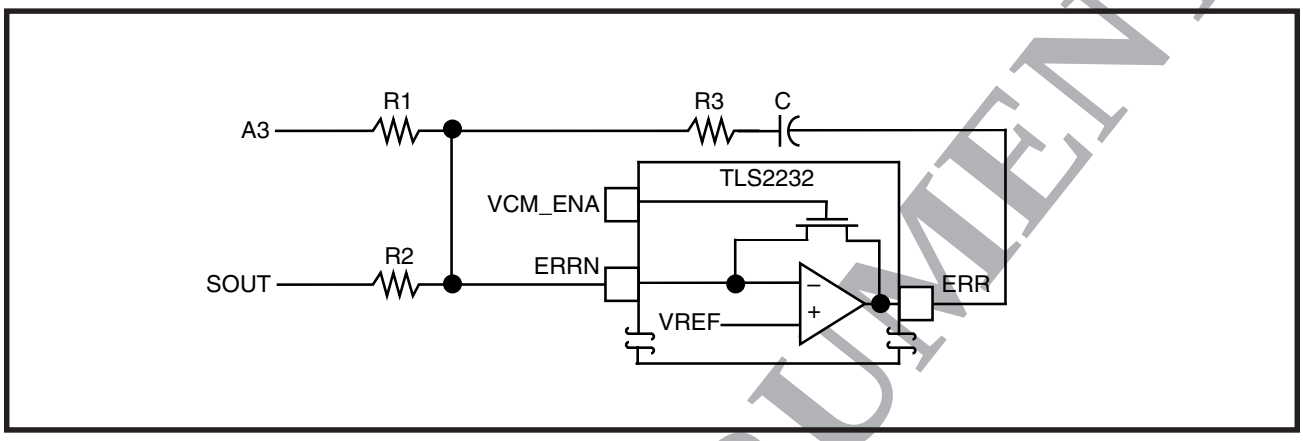


FIGURE 2-3: Summing Amplifier Implementation

Equation 5 shows the transfer function of this circuit.

$$H(S) = \frac{(R3\ C)S + 1}{(R\ C)S} \quad (5)$$

Where: R = R1 = R2

Selecting values for R1, R2, and RSEN sets the VCM transconductance gain (Gm) (see equation 6).

$$Gm = \frac{IVCM}{VCMD} = \frac{R2}{2.73 \bullet R1 \bullet RSEN} \quad (6)$$

NOTE: If the error amplifier is near saturation, which is detected by either VCMA < (1/12) V12 and VCMB > (11/12) V12 or by VCMA > (11/12) V12 and VCMB < (1/12) V12, then the SAT_DET signal is set high.

NOTE: When the VCM is disabled by setting VCM_ENA low, ERR and ERRN are shorted internally. This prevents the error amp output voltage from saturating.

Current-Sense Amplifier (ASEN)

The current-sense amplifier (ASEN) (see Figure 2–4) provides a measure of the current being delivered to the motor by measuring the voltage across the sense resistor. The gain of this amplifier is fixed at 2.73. The offset can be calibrated by setting VCM_ENA low, along with SOFT_RET, to ensure that the VCM outputs are turned off and no current is being delivered to the VCM. In this state SOUT should be equal to VREF.

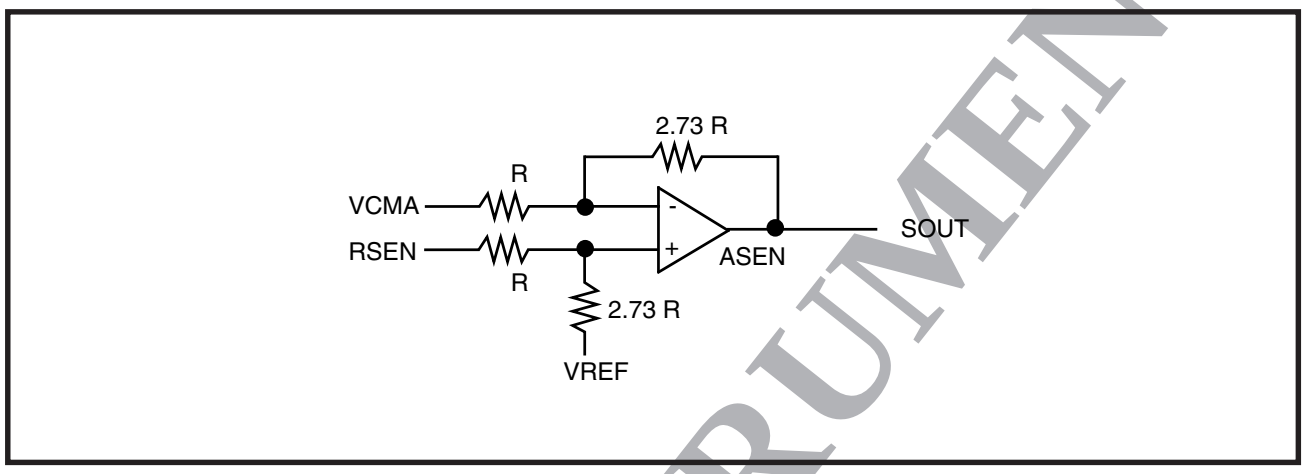
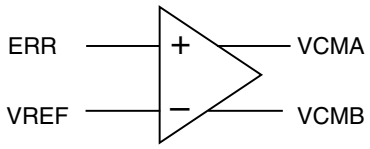


FIGURE 2-4: Current-Sense Amplifier Implementation

VCM Predriver Amplifier

The VCM predriver amplifier biases and operates the power FETs of the TPIC150x as a class AB amplifier with a gain of 12. Equation 7 shows this relationship.

$$\frac{VCMA - VCMB}{ERR - VREF} = 12 \qquad (7)$$



NOTE: Setting VCM_ENA to logic low when SOFT_RET is equal to logic low disables the VCM output. Setting SOFT_RET to high disables the VCM and causes a retract.

VOICE-COIL MOTOR PREDRIVER (continued)

Biasing the TPIC150x Power FETs

The VCM predriver amplifier uses signals GLS and ISET to determine the bias point for the TPIC150x power FETs (see Figure 2–5). A constant current source is applied to the ISET pin. The gate voltage for the TPIC150x sense FET is varied until the voltage on ISET matches a known reference of V12/2. The voltage at GLS is then scaled and used to set the bias point of the TPIC150x power FETs.

$$I_{quiescent} \approx (150) \bullet I_{source} \quad (8)$$

Where:
Iquiescent is the bias current in the VCM H-bridge, and Isource ≈ 40 μA.

SPINDLE MOTOR PREDRIVER

Spindle Motor Predriver Functional Overview

Figure 2–6 shows the TLS2232 spindle motor predriver section. The RESET, ENABLEZ and DISPWRZ signals command one of eight different operational modes:

- Preset
- Start/SENSE and Start/TACH
- Run
- Coast
- Brake
- I_CAL
- Test1†
- Test2†

†Modes Test1 and Test2 are for factory test purposes and are shown for reference only.

The preset and start/SENSE and start/TACH modes are used to start the spindle motor. The commutation state machine controls motor commutation by enabling the appropriate high- and low-side drivers of the TPIC150x.

During start-up, the commutation state machine is advanced by pulses applied on ADVANCE. As the spindle motor approaches idle frequency, the run mode is selected. At this time, the commutation state machine is advanced by the output of the VCO. The BEMF detector and phase error amplifier generate an error signal that is applied to the input of the VCO. The commutation frequency is adjusted by the VCO using this error signal.

In run mode, the current applied to the motor can be controlled by using one of two modes of pulse width modulation for either voltage or current control. The methods are discussed in the Run section.

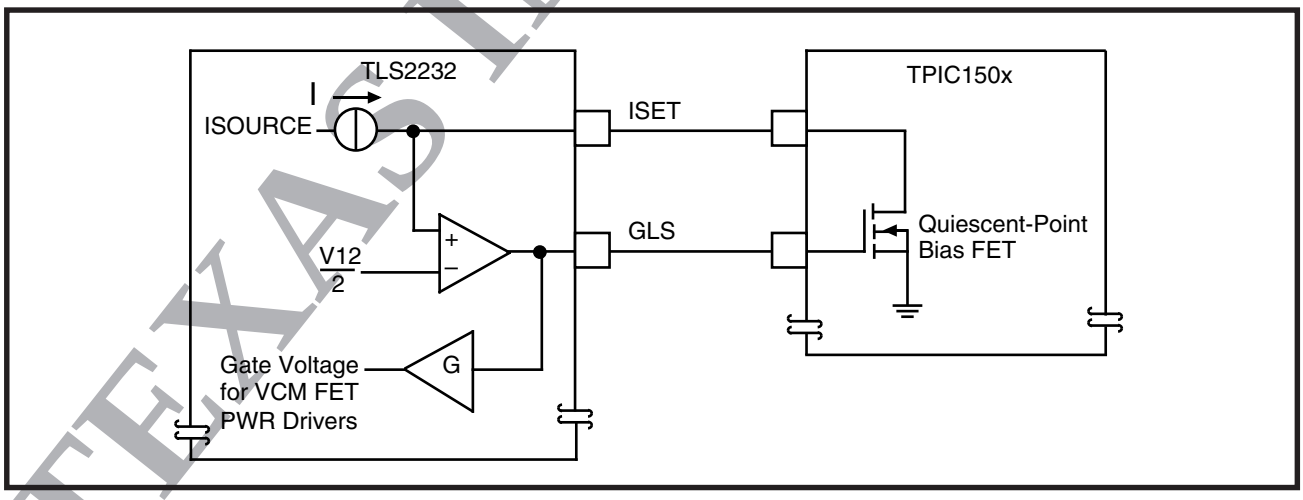
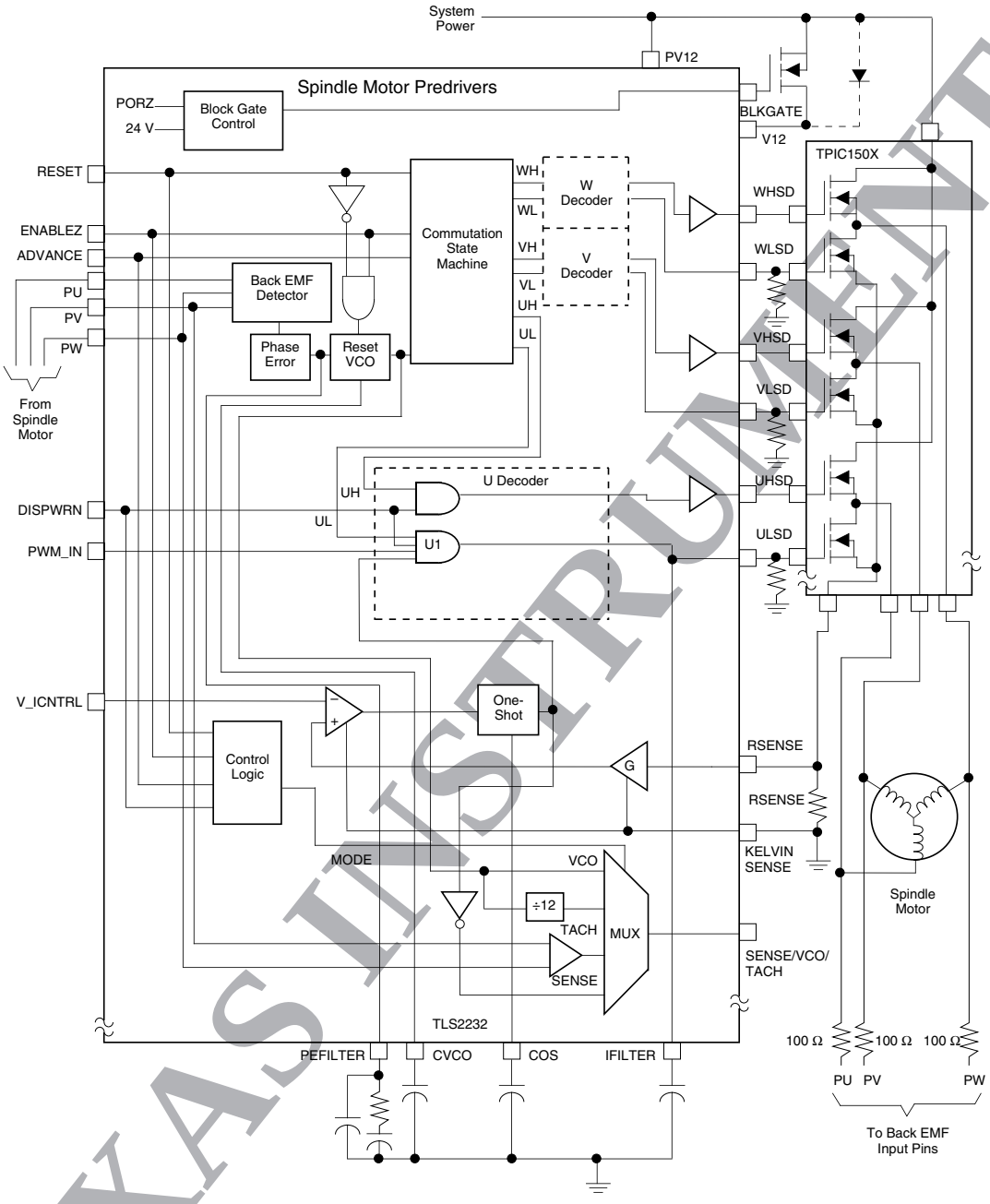


FIGURE 2-5: GLS and ISET Biasing the TPIC150x



NOTE:
The ULSD, VLSD, and WLSD terminals can be connected to external 10-MΩ to 20-MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2232.

FIGURE 2-6: Spindle Predrivers Functional Block Diagram

Spindle Motor Predriver Functional Overview (continued)

The MUX shown in Figure 2–6 implements the logic illustrated in Figure 2–7. The TACH, SENSE, and VCO outputs are combined with the mode signals indicated (these signals represent the various states determined by selection of RESET, ENABLEZ, and DISPWRZ as defined in Table 2–1) to provide a real-time status signal at the SENSE/VCO/TACH output.

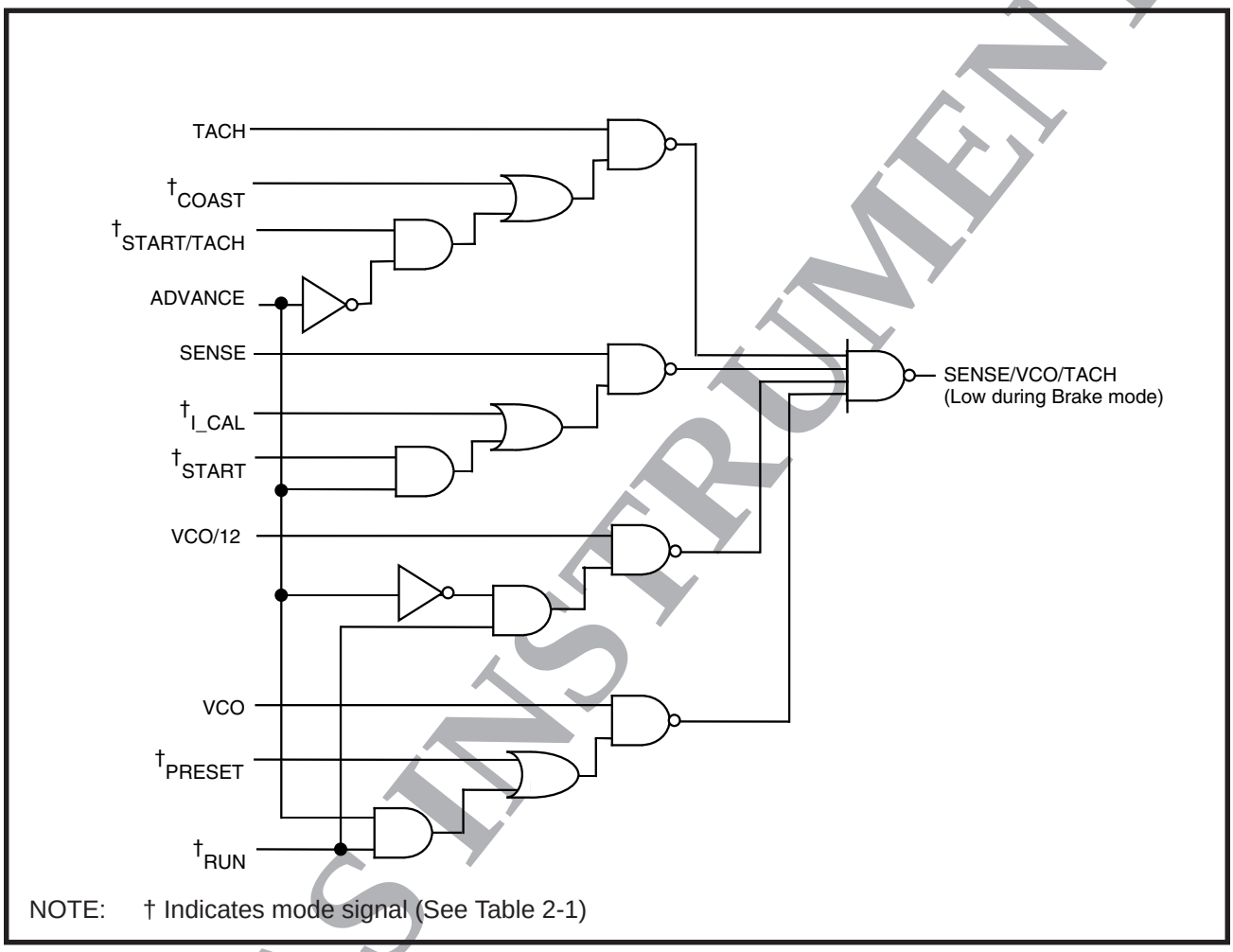


FIGURE 2-7: Sense/VCO/TACH MUX Logic

Spindle Motor Predriver Modes of Operation

The TLS2232 spindle motor predriver circuitry operates in one of eight modes as selected by RESET, ENABLEZ, and DISPWRZ. Table 2–1 defines the combinations of these signals that are used to select either the preset, start/SENSE and start/TACH, run, coast, brake, I_CAL, test1, or test2 mode.

TABLE 2–1: Modes of Operation

MODE	RESET	ENABLEZ	DISPWRZ	ADVANCE	SENSE/ VCO/TACH	PE FILTER	VCO	STATE MACHINE	VREF OUT
Preset	1	1	1	X	VCO	0.1 V	Idle	Reset	2.2 V
Start	0	1	1	1	SENSE	0.1 V	Reset	†	2.2 V
Run	0	0	1	1	VCO	Run	Run	Run	2.2 V
Run	0	0	1	0	VCO/12	Run	Run	Run	2.2 V
Coast	0	0	0	X	TACH	Run	Run	Run	2.2 V
Brake	1	0	0	X	GND	0.1 V	Idle	Reset	2.2 V
I_CAL	1	1	0	X	SENSE	0.1 V	Idle	Reset	2.2 V
Test1 ‡	0	1	0	X	X	X	X	X	Vbg
Test2 ‡	1	0	1	X	X	X	X	X	Thermal Shutdown

† During start mode, the state machine is advanced on the rising edge of the ADVANCE pin.
‡ Modes Test1 and Test2 are for factory test purposes and are shown here for reference only.

The transitions between the various modes should be done according to the diagram shown in Figure 2–8 to prevent logic race conditions.

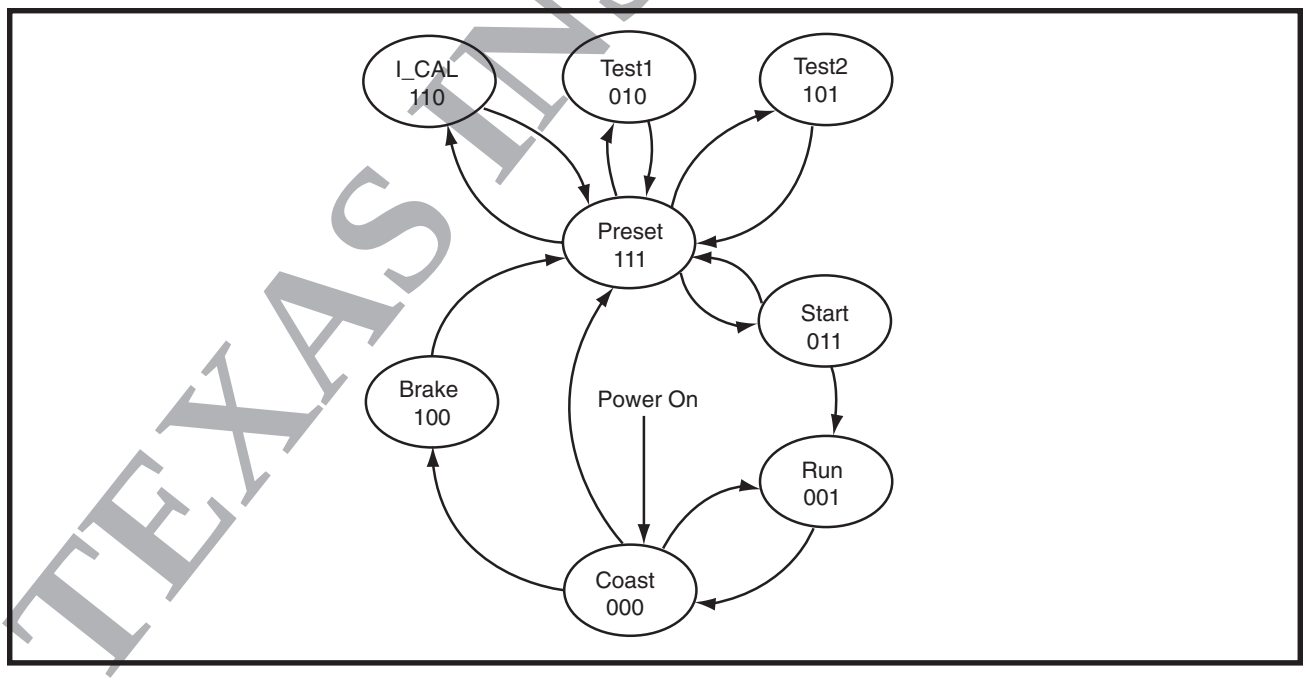


FIGURE 2-8: Mode Transition State Diagram

Spindle Motor Predriver Modes of Operation
(continued)

Preset

In the preset mode, a fixed voltage of 100 mV is applied at the input to the VCO, causing it to operate at its idle frequency. The VCO idle frequency, which is available at the SENSE/VCO/TACH output, is measured so that switching over (handing off) from forced commutation to closed-loop commutation can be accomplished at a frequency within the lock range of the PLL. This should be done at a frequency which is at least 10 percent higher than the idle frequency.

NOTE: To allow the filter network to settle, the VCO idle frequency measurement should not be made until after the preset mode has been commanded for at least 200 ms.

Start/SENSE

The start/SENSE mode can be used to determine the approximate position of the spindle motor's rotor so that the commutation state machine can be initialized. The output of the SENSE comparator is available at the SENSE/VCO/TACH output. The SENSE comparator switches from low to high when the voltage across the RSENSE resistor exceeds the voltage applied at V_ICNTRL.

Start/TACH

The start/TACH mode is used to start the spindle motor. In order to get maximum spindle motor acceleration, PWM_IN is held high. This allows maximum current to be applied to the spindle motor. When the current as measured across RSENSE exceeds the threshold as set by the voltage applied at V_ICNTRL, the one shot disables the low-side spindle motor drive creating a constant off time which is set by the external capacitor COS. Choose this capacitor to optimize spin-up time and to provide sufficient over-current protection. Use equations 9 and 10 to select COS.

$$COS = \frac{I}{\Delta V} \bullet \Delta t \qquad (9)$$

where $I = \frac{Vbg}{RSLEW}$,

$Vbg = 1.21$, and $\Delta V = 2$

$$COS = \left(\frac{0.605}{RSLEW}\right) \bullet \Delta t \qquad (10)$$

Where: COS is in farads.
RSLEW is in ohms and its value is chosen using equations 11 through 14.
Δt is off time in seconds

NOTE: Adjusting RSLEW also affects spindle driver slew rates as described in the Slew Rate Control subsection.

Since the back EMF from the spindle motor is small during start-up, the commutation state machine must be advanced manually with the ADVANCE pin. This is done open-loop, using a timing algorithm that is matched to the dynamics of the motor/spindle.

During open-loop acceleration, the VCO is held at reset. When the frequency of the signal being applied to the ADVANCE pin exceeds the VCO idle frequency measured in the preset mode, select the run mode. This releases the VCO from reset enabling it to advance the commutation state machine.

Run

In the run mode, the commutation state machine is advanced by the output of the VCO. The voltage of each phase (PU, PV, and PW) is monitored to determine if commutation occurs late or early. This is done by generating a signal that is the undriven phase minus the average of the two driven phases. This signal is inverted every other cycle to obtain positive pulses. If commutation occurs too early, an increasing positive signal is generated to increase the VCO frequency to align the commutation with the motor winding. The VCO or VCO/12 output at the SENSE/VCO/TACH pin can be used as feedback for closed-loop speed regulation.

NOTE: Servo data can also be used when more precise regulation is required.

The spindle speed is regulated by adjusting the current that is applied to the spindle motor. This is done in one of two ways.

PWM is used to control the applied current in one of two ways. In the first method (voltage mode) a variable duty cycle signal is applied at PWM_IN (pin 4). This duty cycle variability is used to change the voltage that is supplied to the motor. This leads to changes in speed of the motor. Current limiting is determined by the selection of RSENSE and by the application of a threshold voltage at V_ICNTRL. When the current through the sense resistor becomes large enough that the sense amplifier output exceeds the voltage at V_ICNTRL, the one-shot is triggered pulling the low-side driver gates to ground which turns them off.

NOTE: KELVIN_SENSE is used to sense the ground side of RSENSE to eliminate offset caused by ground potential differences.

In the second PWM control method (current mode) V_ICNTRL is used to control the maximum threshold at the sense resistor while PWM_IN is held at constant high level. The voltage applied at V_ICNTRL is proportional to the desired motor current. When the current through the sense resistor becomes large enough that the sense amplifier output exceeds the voltage at V_ICNTRL the one shot is triggered which turns off the low-side drivers. The duty cycle at which the drivers turn on and off is proportional to the signal applied at V_ICNTRL. This controls the effective current applied to the spindle motor.

Coast

During coast mode, the spindle motor drivers are disabled and the spindle spins freely. The TACH output is available at the SENSE/VCO/TACH pin. An example of the signal appearing at the TACH output is shown in Figure 2–9.

Brake

During brake mode, the spindle motor high-side drivers are all turned on. This causes the motor to brake dynamically.

Calibration Mode

Figure 2–10 shows the calibration mode used to measure the voltage at V_ICNTRL that corresponds to 0.3 V across the sense resistor. When the calibration mode is selected, the output of MUXA is an internal 0.3 V reference. By applying a ramp from maximum to minimum at the input of V_ICNTRL and monitoring the output at SENSE/VCO/TACH, the point at which the sense comparator switches states can be determined.

Test Modes 1 and 2

These modes are for factory testing of the TLS2232. In test mode 1, the band-gap voltage (Vbg) is available at VREF (pin 43). Test mode 2 is used to test over temperature or thermal shutdown through VREF.

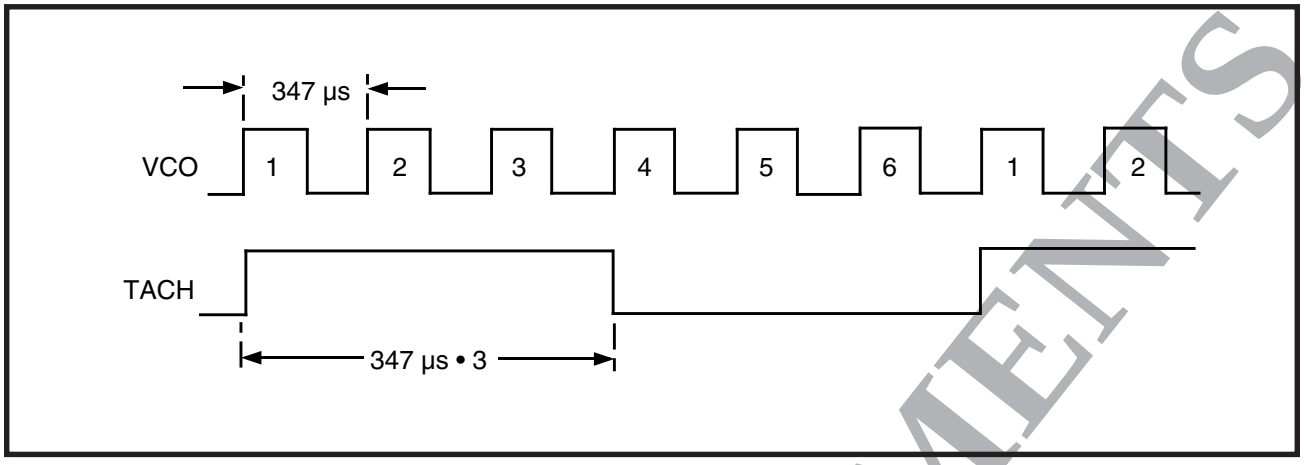


FIGURE 2-9: TACH Output for an 8-Pole 7200-RPM Motor

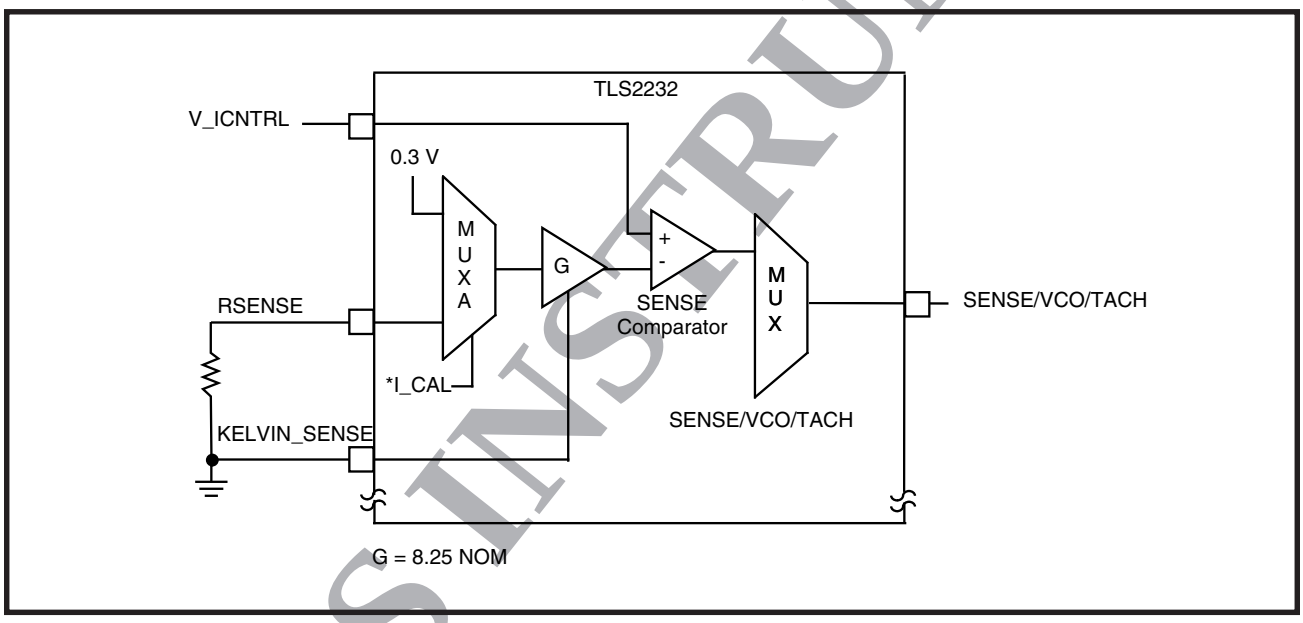


FIGURE 2-10: Calibration Mode Logic Diagram

SPINDLE MOTOR PREDRIVER (continued)

Commutation Control

The commutation process involves sequentially turning the spindle motor high- and low-side drivers on and off as illustrated in Figure 2–11 and listed in Table 2–2.

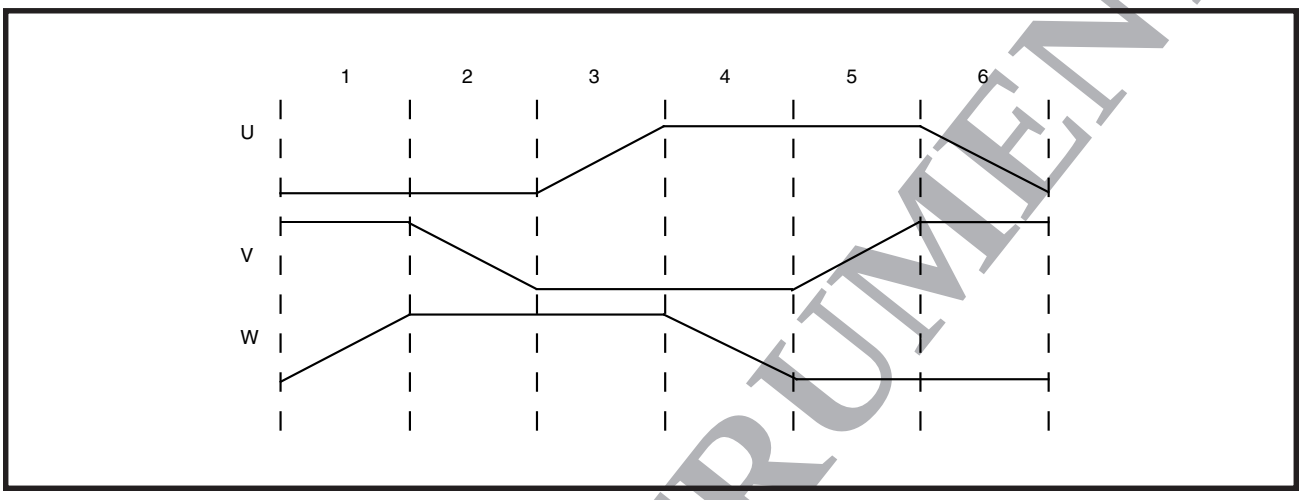


FIGURE 2-11: Commutation Graphical Form

TABLE 2-2: Commutation State Table

STATE	0 (PRESET)	1	2	3	4	5	6
UL	0	1	1	0	0	0	0
VL	0	0	0	1	1	0	0
WL	0	0	0	0	0	1	1
UH	0	0	0	0	1	1	0
VH	0	1	0	0	0	0	1
WH	0	0	1	1	0	0	0

SPINDLE MOTOR PREDRIVER (continued)

Slew Rate Control

A resistor attached to the RSLEW pin controls the slew rate of the spindle motor driver power FETs by adjusting the amount of current that is applied to the gate. The RSLEW resistor establishes a reference current, I_{SLEW}, as shown in Figure 2–12. This current is used by the high- and low-side driver circuits to determine the amount of current that is applied to the power FETs gate.

The high-side driver circuitry (Figure 2–13) provides two different levels of current for charging and discharging the power FETs gate (see Figure 2–14). During the charging interval, switch S1 is closed until the voltage at the power FETs gate, V_{GHS}, exceeds ~ 20 V. At that point, switch S1 opens.

Equation 11 is used to calculate the current applied to the gate when S1 is closed. Equation 12 is used to calculate the current applied to the gate when S1 is open.

$$I_{CHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 26.4 \quad (11)$$

$$I_{CHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 2.4 \quad (12)$$

NOTE: Maximum charge current for high side drive = 1 mA.

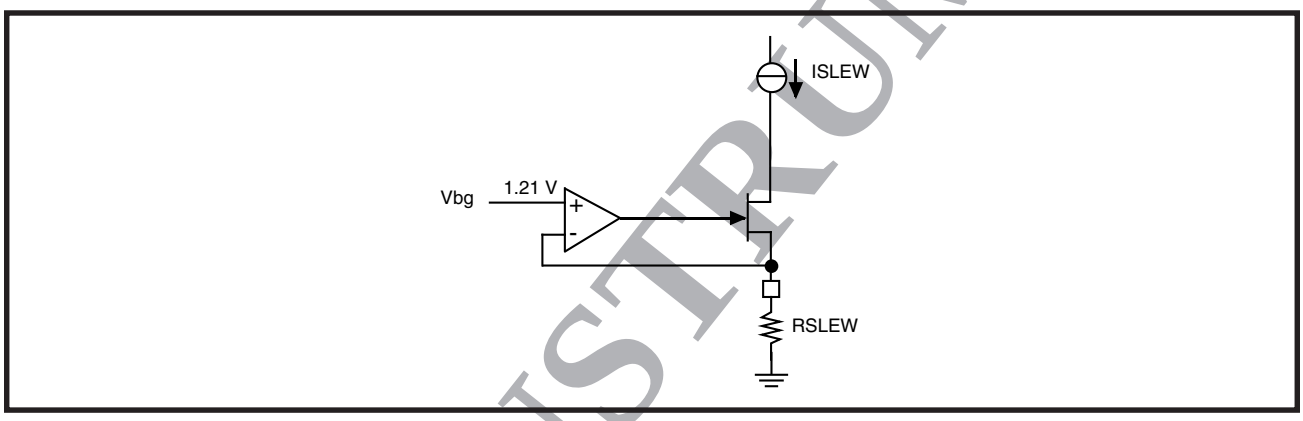


FIGURE 2-12: ISLEW Biasing Circuit

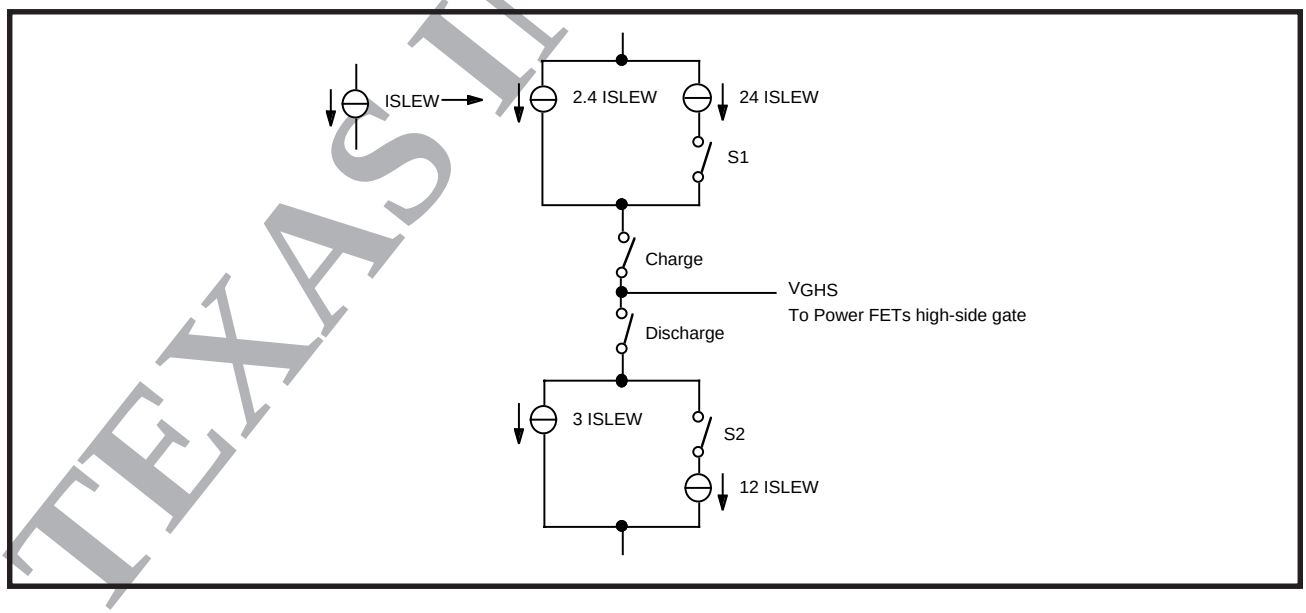


FIGURE 2-13: High-Side Driver Circuitry

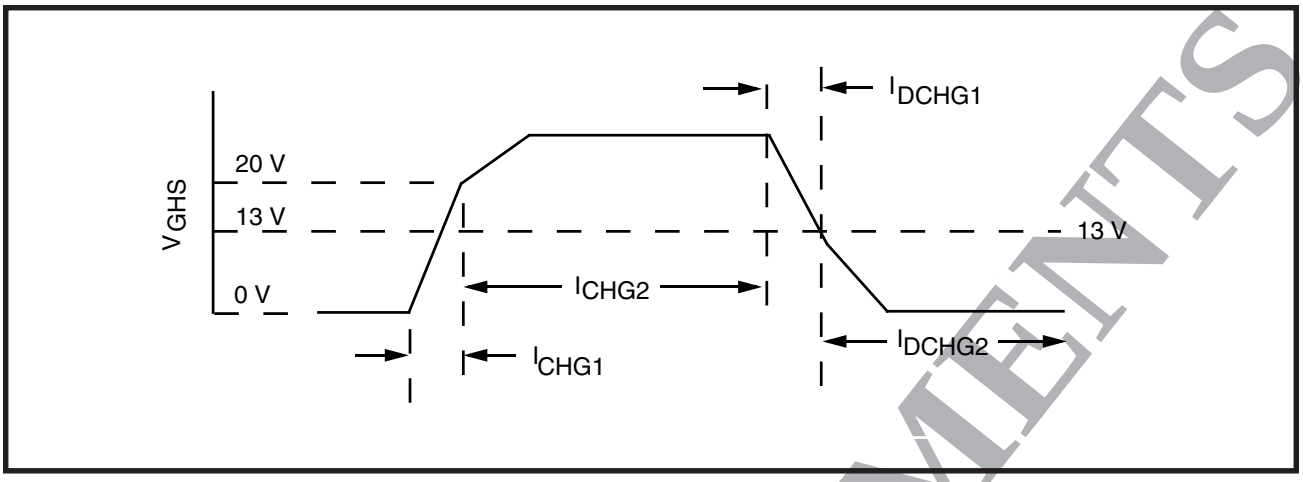


FIGURE 2-14: V_{GHS} During Charging and Discharging

Slew Rate Control (continued)

During the discharging interval, switch S2 remains closed until V_{GHS} drops to below ~ 13 V. At this point, S2 opens. Equation 13 is used to calculate the current applied to the gate when S2 is closed. Equation 14 is used to calculate the current applied to the gate when S2 is open.

Figure 2–15 shows the low-side driver circuitry. Equation 15 is used to calculate the charge current, I_{CHG3}. During PWM switching of the low-side drivers, S3 and S4 are open and S5 is closed. Equation 16 is used to calculate the discharge current. Switches S3, S4, and S5 are used to control the discharge current during commutation switching of the low-side drivers. When V_{GLS} is greater than ~ 6 V, both S3 and S4 are closed, S5 is open, and equation 17 is used to determine the current drawn from the gate. As V_{GLS} drops below 6 V, switch S4 opens and equation 18 is used to determine the discharge current.

$$I_{DCHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 15 \quad (13)$$

$$I_{DCHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 3 \quad (14)$$

$$I_{CHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 160 \quad (15)$$

$$I_{DCHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 40 \quad (16)$$

$$I_{DCHG4} = \left(\frac{1.21}{RSLEW}\right) \bullet 22.5 \quad (17)$$

$$I_{DCHG5} = \left(\frac{1.21}{RSLEW}\right) \bullet 7.5 \quad (18)$$

NOTE: The slew-rate circuitry saturates when current is set >2 mA.

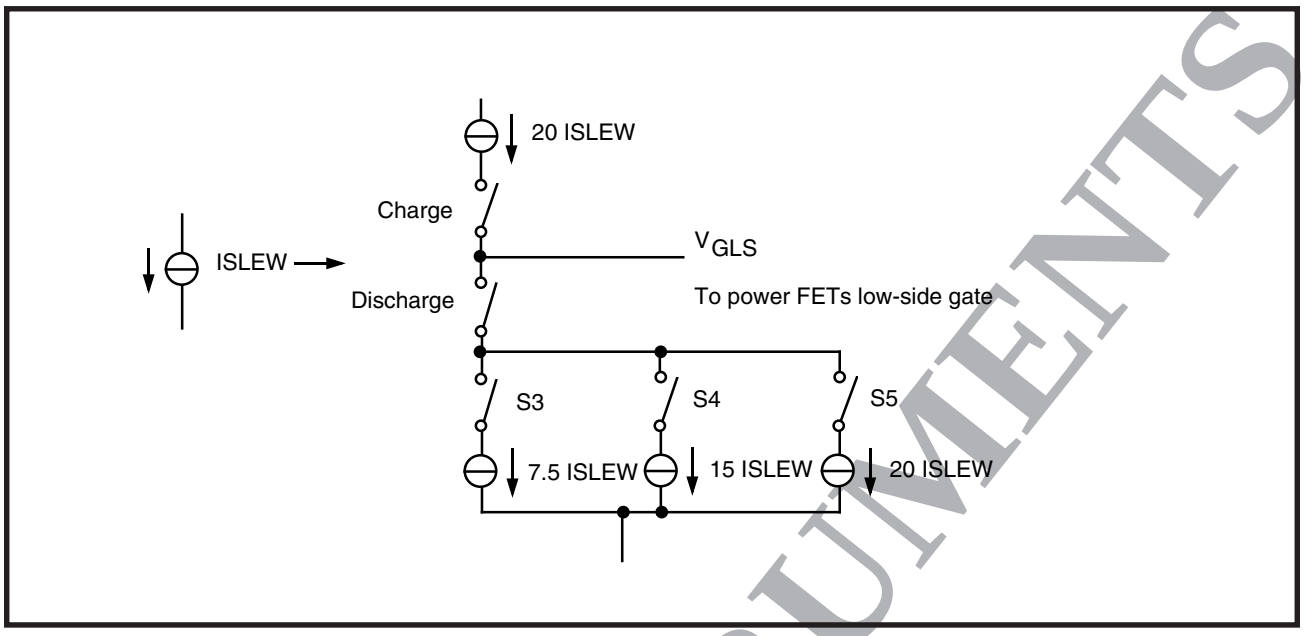


FIGURE 2-15: Low-Side Driver Circuitry

The application of these low-side currents for a single commutation interval is illustrated in Figure 2-16.

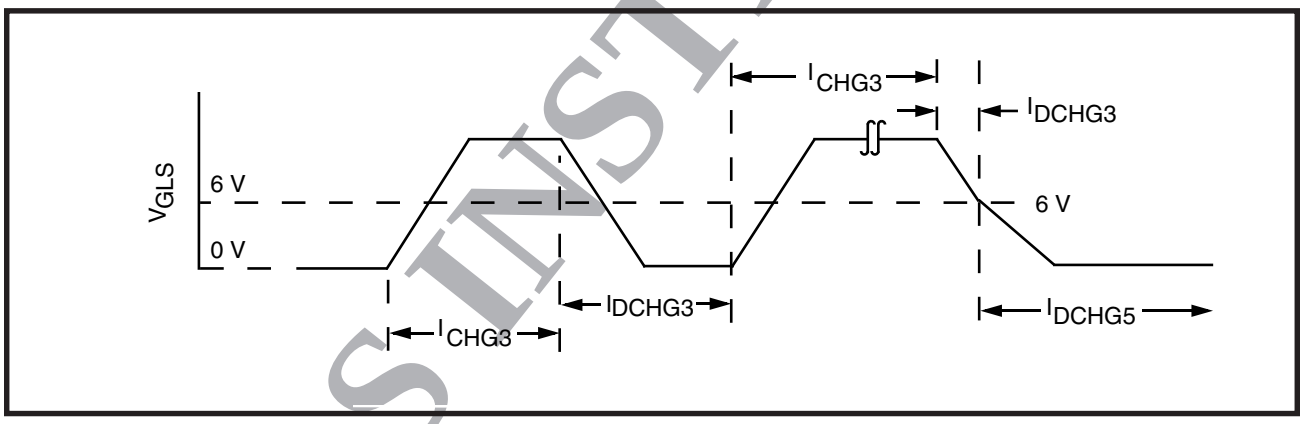


FIGURE 2-16: V_{GLS} for a Single Commutation Interval

NOTE: Adjusting RSLEW also affects the one-shot timing as described in the Start/TACH subsection.

DETAILED DESCRIPTION (continued)

SUPPORT FUNCTIONS

The TLS2232 support functions include:

- Voltage regulator
- Voltage monitor
- Actuator retract control
- Spindle motor brake control
- Voltage reference
- Charge pump

Voltage Regulator

A 5 V on-chip regulator is powered from the voltage at V12, and keeps selected functions such as retract, brake, and spindle commutation powered up and functioning during power brownouts. In case of a complete 5 V and 12 V power fault, the on-chip 5 V regulator supplies power (V5R) by way of the spindle's BEMF to complete actuator retract and spindle braking. To ensure that chip logic is functional during a 12 V fault with no BEMF, a forward biased diode supplies 5 V (minus a V_f diode drop) from V5A to the V5R power bus (see Figure 2–17).

Voltage Monitor

The TLS2232 monitors 5 V and 12 V power and indicates a low condition on PORZ. The voltage monitor is shown in Figure 2–18. Off-chip capacitors are recommended at pins 47 (VCK5)and 48 (VCK12). These capacitors filter the supply voltage to ensure momentary system spikes do not interrupt system operation. The internal resistor dividers set the voltage trip levels, and external resistors can be added if adjustments in trip level are desired.

The PORZ signal typically is used as a processor reset. Selection of C_{POR} sets the delay (tdly) of PORZ rising after power becomes valid. Equations 19 and 20 define this relationship.

$$t_{dly} = CPOR \bullet \frac{\Delta V}{I} \qquad \Delta V = VREF \tag{19}$$

$$\text{Note: Again, } \Delta t = \frac{C}{I}\Delta V \qquad I = 5\ \mu A \tag{20}$$

Where: CPOR is in farads.

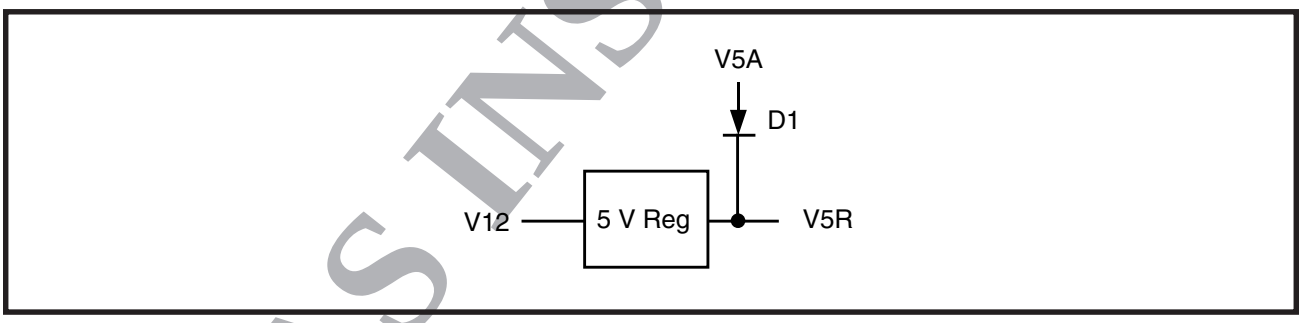


FIGURE 2-17: V5R Power Bus

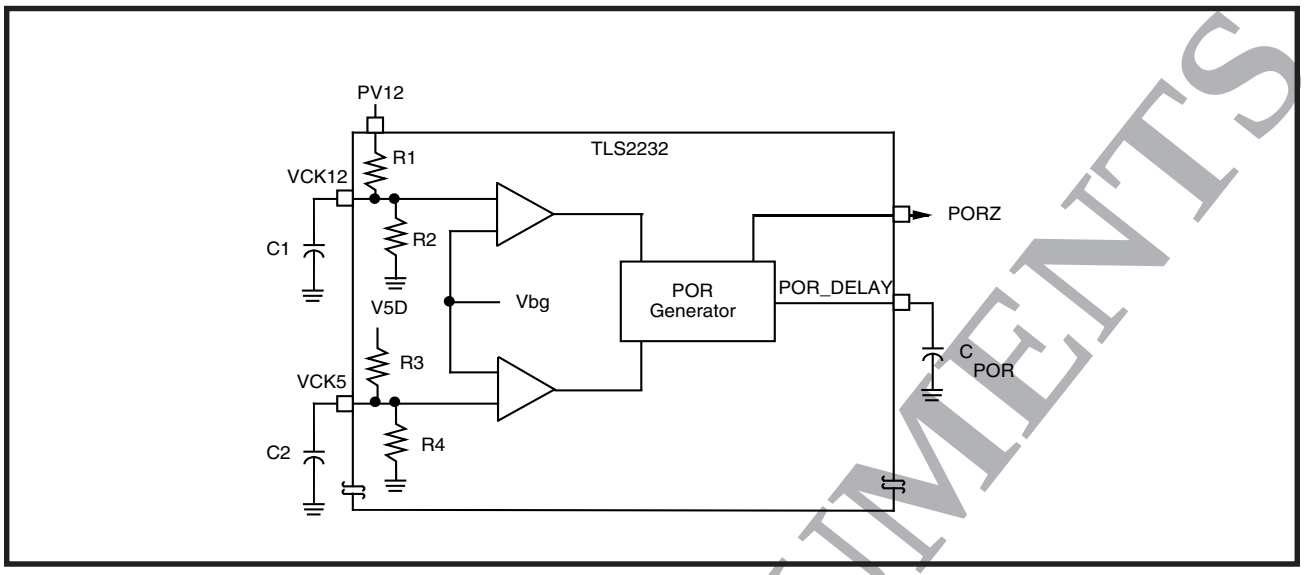


FIGURE 2-18: Voltage Monitor Schematic Diagram

NOTE: R1 = 26 270 Ω nominal
R2 = 3 650 Ω nominal
R3 = 26 270 Ω nominal
R4 = 9 429 Ω nominal
Vbg = 1.21 V nominal

Figure 2-19 shows the PORZ response to low 5 V or 12 V voltage levels

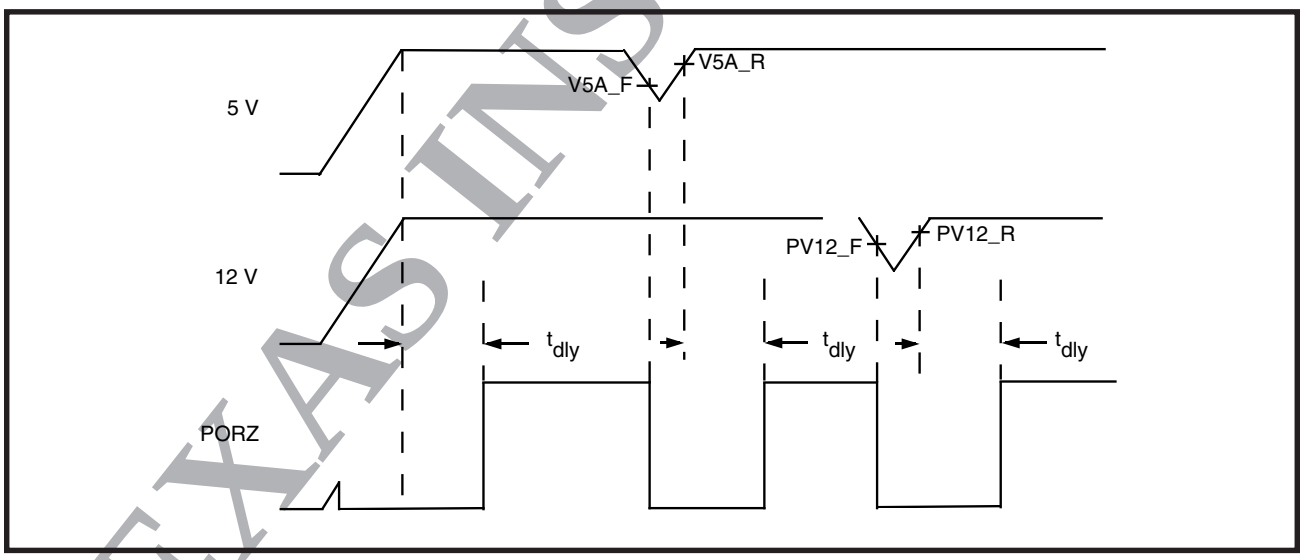


FIGURE 2-19: Voltage Monitor Response to Supply Voltages

SUPPORT FUNCTIONS (continued)

Retract

Figure 2–20 shows the retract control logic. The actuator is immediately retracted on detection of a power fault. The PORZ signal going low causes the retract latch to be set. This causes the signal at RETP to be high ensuring that Q1 is off and Q2, Q3 and Q4 are all on. This signal also acts as an enable to the voltage control block which outputs the retract voltage on VCMA and 12 V on GNB. The retract voltage is set by the selection of RRET as follows:

$$\text{Retract voltage} = 0.5\,\text{V}\left(1 + \frac{25\ \text{k}\Omega}{5\ \text{k}\Omega + \text{RRET}}\right) \quad (21)$$

Where: RRET is in ohms.

NOTE: Retract voltage = 0.5 V when RRET = ∞.

During a power-down event, energy from the spindle provides the VCM retract voltage.

The retract voltage to the VCM continues until either a delayed BRAKE occurs (this is indicated by DBRK going high in response to BDLY dropping below 1.2 V as illustrated in Figure 2–21) or until PORZ returns high and then DISPWRZ is set high. If delayed brake is not used and BDLY is held high, then RETP remains set and the retract voltage continues to be applied until power is restored. Then DISPWRZ is set high.

The retract function can also be initiated by applying a logic high at SOFT_RET.

If VCM_ENA is taken low when RETP is not set, then Q1, Q2, Q3, and Q4 are on, ensuring that the VCM is disabled.

NOTE: The TLS2232 provides thermal protection for the retract circuitry. At approximately 150°C, the retract current is disabled. When the temperature drops below 140°C, the retract current is enabled.

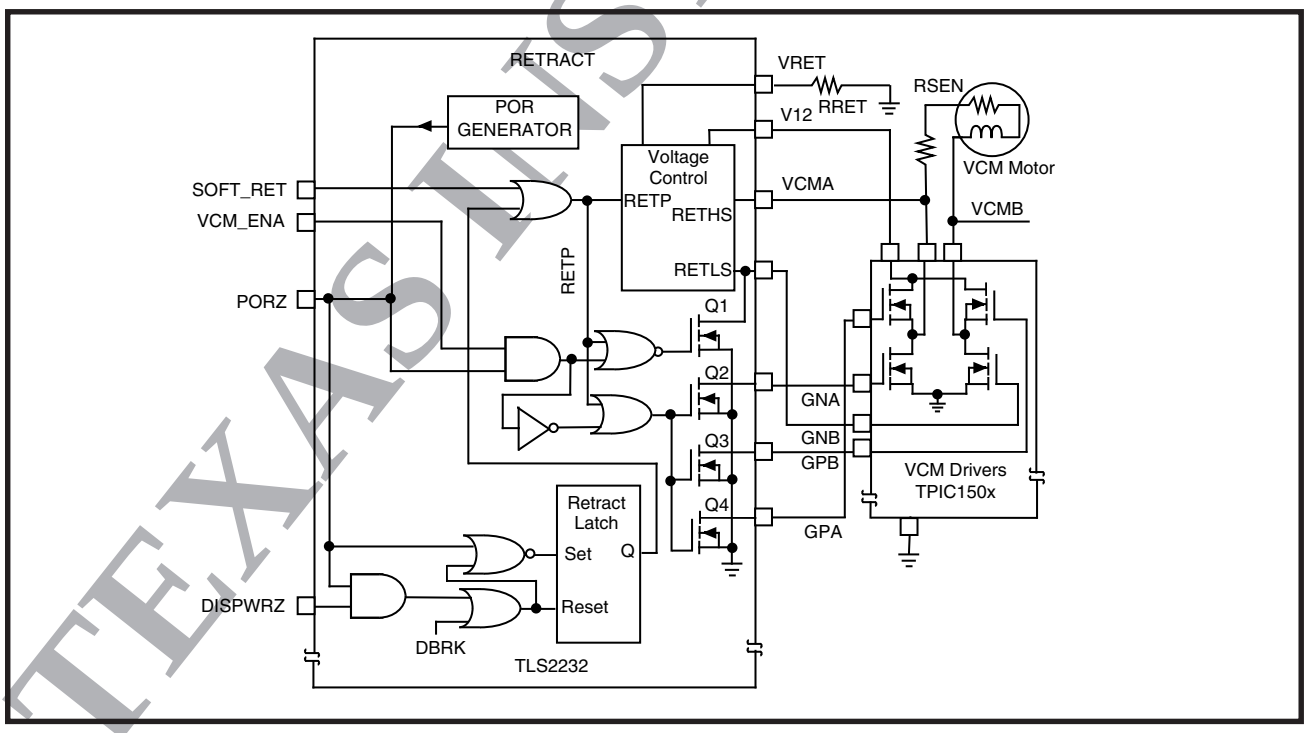


FIGURE 2-20: Retract Function Schematic

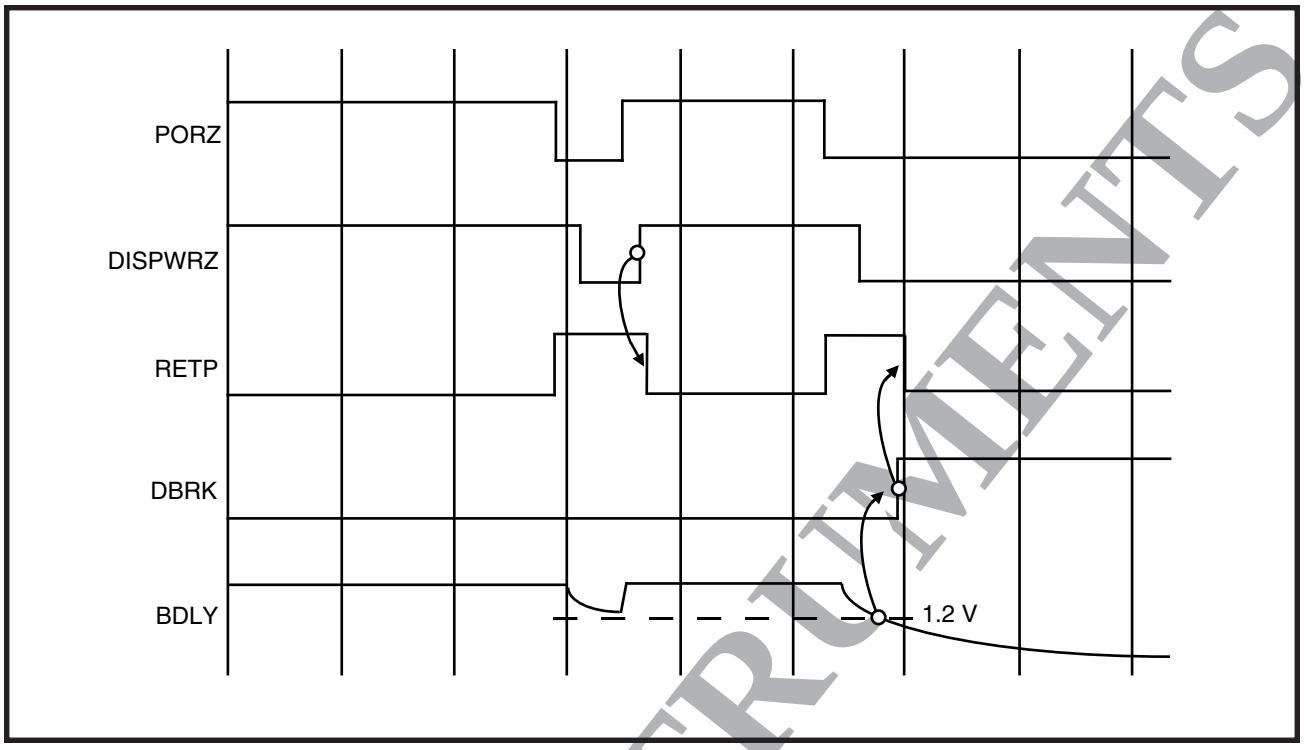


FIGURE 2-21: DISPWRZ, RETP, and SBRK Responses to PORZ and BDLY

SUPPORT FUNCTIONS (continued)

Spindle Brake

The brake function turns on all spindle high-side drivers (UHSD, VHSD, and WHSD). The brake function is initiated when SBRK goes high, which sets the brake latch. This is done using software, generating a delayed brake, or generating an automatic brake.

Software Brake (SFT_BRK)

A software brake can be commanded by setting RESET to a logic high and both ENABLEZ and DISPWRZ to a logic low.

Delayed Brake (DBRK)

A delayed brake is set after PORZ has been low for a time determined by the selection of Rext and Cext as follows:

$$\text{Brake delay time} = Rext \bullet Cext \bullet \ln\left(\frac{V5D}{Vbg}\right) \quad (22)$$

Where: Rext is in ohms
Cext is in farads
Ln is natural log
V5D is in volts
V5D = 5 V and Vbg = 1.21 V

NOTE: If the DBRK function is not used it is recommended that the BDLY pin be pulled up to V12 through a 100 kΩ resistor.

Automatic Brake (ABRK)

The automatic brake is set when the voltage at V12 (the voltage generated from the spindle's BEMF during a power loss situation) drops below 2 V.

Voltage Reference

The TLS2232 generates accurate and stable voltages of 2.2 V and 4.4 V for use both internally and externally.

Charge Pump

The charge pump generates 24 V used to drive the TPIC150x high side N-channel FETs. The charge pump requires only one external component, a storage capacitor. The recommended value for the storage capacitor is 1 µF.

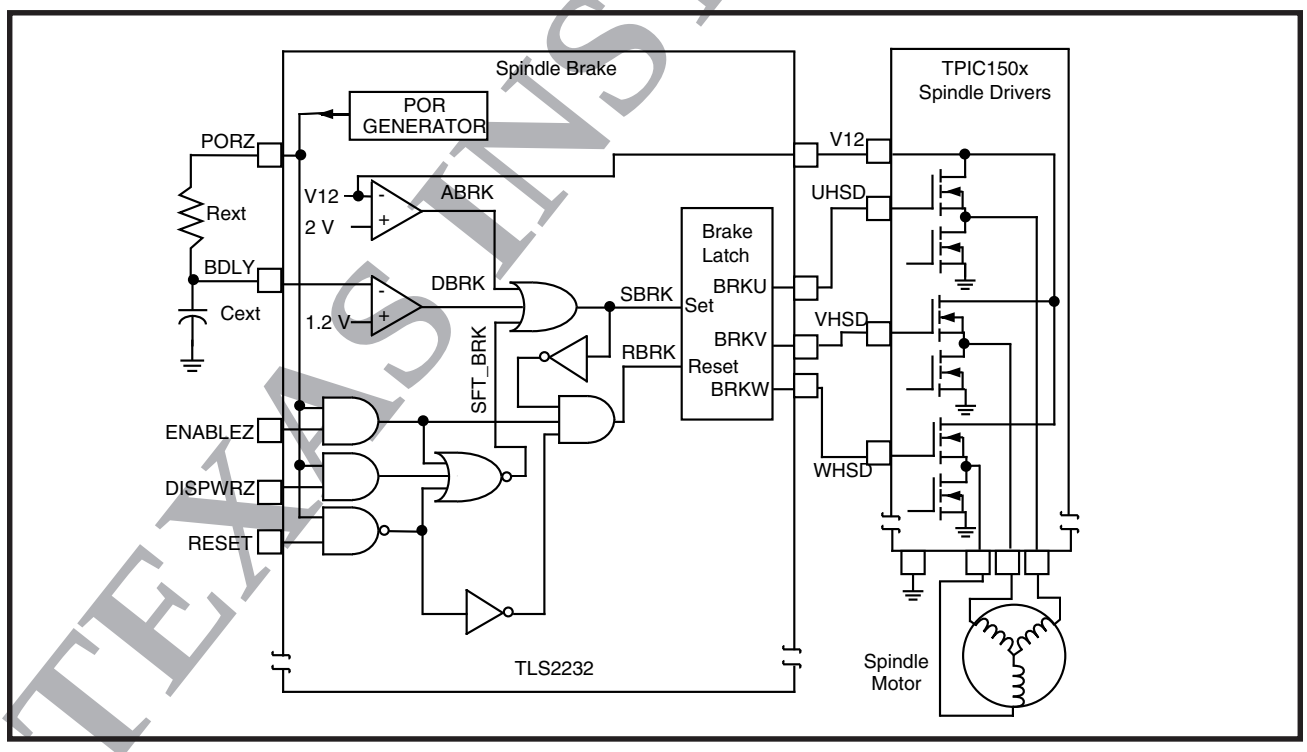


FIGURE 2-22: Spindle Brake Function Schematic

PIN DESCRIPTION

TLS2232 Terminal Functions

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
SUPPLIES				
AGND	14		Ground	Analog ground
CP	41	O	Analog	Charge pump storage capacitor connection
DGND	52		Ground	Digital ground
PV12	50	I	Analog	12 V power supply monitor (sensed by voltage monitor to generate PORZ)
VREF	43	O	Analog	2.2 V reference output
V5A	15		Power	5 V power supply (analog)
V5D	51		Power	5 V power supply (digital)
2VREF	42	O	Analog	Reference output (2 • 2.2 V)
V12	36		Power	12 V power supply (with blocking diode)
VCM				
A3	33	O	Analog	Filter amplifier output
A3P	34	I	Analog	Filter amplifier noninverting input
ERR	32	O	Analog	VCM current loop error amplifier output
ERRN	35	I	Analog	VCM current loop error amplifier inverting input
GLS	24	O	Analog	Driver sense gate
GNA	29	O	Analog	A low-side driver gate output
GNB	26	O	Analog	B low-side driver gate output
GPA	30	O	Analog	A high-side driver gate output
GPB	28	O	Analog	B high-side driver gate output
ISET	25	O	Analog	Driver sense drain (bias current for class AB operation)
RSEN	23	I	Analog	VCM current-sense feedback. Connects internally to the noninverting input of the current-sense differential amplifier
SAT_DET	37	O	Digital	High level indicates VCM drivers are in saturation
SOFT_RET	38	I	Digital	Initiates retract (high level indicates retract)
SOUT	22	O	Analog	VCM current-sense amplifier feedback
VCMA	31	I	Analog	VCM current-sense resistor. Connects internally to the inverting input of the current-sense differential amplifier and externally to the driver side of the sense resistor
		O	Analog	Retract voltage output
VCMB	27	I	Analog	VCM in. Connects externally between the drivers and the VCM

PIN DESCRIPTION (continued)

TLS2232 Terminal Functions

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
VCM (continued)				
VCM_ENA	39	I	Digital	High level enables the VCM, low level disables the VCM. This signal is ignored during retract.
VRET	45	I	Analog	VCM retract voltage control (voltage controlled by selection of resistor connected externally to this pin)
SPINDLE MOTOR				
ADVANCE	13	I	Digital	Commutation state machine advance (used for spindle start)
COS	6	O	Analog	Capacitor for one-shot timing
CVCO	21	O	Analog	Capacitor to set VCO speed range for motor commutation
DISPWRZ	10	I	Digital	Mode control (low level disables spindle power)
ENABLEZ	12	I	Digital	Mode control (active low)
IFILTER	3	O	Analog	Linear current control filter
KELVIN_SENSE	5	I	Analog	RSENSE ground
PEFILTER	20	O	Analog	Phase error filter for commutation PLL
PU	18	I	Analog	Phase U back EMF sense
PV	17	I	Analog	Phase V back EMF sense
PW	16	I	Analog	Phase W back EMF sense
PWM_IN	4	I	Digital	PWM input for low-side driver (used during PWM start and PWM run modes)
BLKGATE	49	I	Analog	Drives external FET for blocking of V12 supply during power fault
RESET	11	I	Digital	Mode control (active high) (resets VCO and state machine)
RSENSE	8	I	Analog	Spindle current-sense voltage feedback (high side of RSENSE)
RSLEW	9	O	Analog	Current setting control for spindle driver, slew rates, and timing of the one-shot used in the constant off-time spindle motor current regulator
SENSE/VCO/TACH	19	O	Digital	MUX output: Current threshold SENSE during start mode. VCO during preset mode or run mode. TACH during coast mode.
UHSD	55	O	Analog	U high-side driver gate output
ULSD	2	O	Analog	U low-side driver gate output
VHSD	54	O	Analog	V high-side driver gate output

TLS2232 Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
SPINDLE MOTOR (continued)				
VLSD	1	O	Analog	V low-side driver gate output
WHSD	53	O	Analog	W high-side driver gate output
WLSD	56	O	Analog	W low-side driver gate output
V_ICNTRL	7	I	Analog	Motor current control
VOLTAGE MONITOR (VM)				
BDLY	44	I	Analog	Brake delay, retract time-out
PORZ	46	O	Digital	Power on reset (active low)
POR_DELAY	40	O	Analog	Capacitor to set PORZ delay
VCK5	47	O	Analog	Low V5D voltage monitor filter/threshold set
VCK12	48	O	Analog	Low PV12 voltage monitor filter/threshold set

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED) †

PARAMETER	RATING
Supply voltage, V12, PV12 (see Note 1)	15 V
Supply voltage, V5D, V5A (see Note 1)	7 V
Negative voltage applied to any pin (see Notes 2 and 3)	–0.5 V
Power dissipation, T_A = 70°C	1 W
Charge pump output voltage	26 V
Operating free-air temperature range	0°C to 70°C
Operating virtual junction temperature, T J	≤150°C
Thermal resistance: Junction-to-case, $R_{\theta JC}$	27.3°C/W
Storage temperature range, T_{stg}	–55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to ground.
2. The maximum negative voltage can be affected by either temperature or current.
3. This rating applies for dc conditions. See Table C-1, Latch-Up Test† Parameters for detailed transient parameters.

RECOMMENDED OPERATING CONDITIONS OVER RECOMMENDED SUPPLY VOLTAGE, T_A = 25°C (SEE NOTE 4)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply voltage V5A, V5D (see Note 5)	VCK5 = 5 V	4.75	5	5.25	V
Supply voltage PV12	VCK12 = 5 V	10.8	12	13.2	V
Supply voltage V12	VCK12 = 5 V	10.3	11.5	12.7	V
Digital high-level input voltage V_{IH}		3.5		V5D+0.3	V
Low-level input voltage V_{IL}		–0.4		0.5	V
Voltage applied to any pin		–0.4			V

NOTES: 4. These parameters are not tested. They are determined by design characterization.
5. V5A and V5D must be tied together. TI recommends that the +5 V (system) be routed first to V5A (pin 15) and then to V5D (pin 51). The width of the traces should be ≥ 0.010 inch and the length of the trace between the two pins should be ≤ 1.5 inches. The trace from V5A to V5D should not be routed to other +5 V requirements.

ELECTRICAL SPECIFICATIONS (continued)

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

Total Device Over Recommended Supply Voltage (see Note 6)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply current	I_{DD}	I_{PV12}			600	µA
		I_{V12}			25	mA
		I_{V5}			10	mA
High-level logic input current	I_{IH}	At ENABLEZ, DISPWRZ, or RESET, V_{IH} = 5 V			70	µA
		At ADVANCE, PWM_IN, SOFT_RET, or VCM_ENA, V_{IH} = 5 V			1	µA
Low-level logic input current	I_{IL}				–1	µA
Low-level output voltage	V_{OL}	I_O = –20 µA			0.1	V
High-level output voltage	V_{OH}	I_O = 20 µA	V5D – 0.1 V			V

NOTE: 6. There are internal 120 kΩ pulldown resistors on ENABLEZ, DISPWRZ, and RESET.

Voltage Monitor (see Note 7)

Falling 12 V voltage PORZ	PV12_F		9.5	9.8		V
Rising 12 V voltage PORZ	PV12_R			10	10.4	V
Hysteresis 12 V, PORZ			50	250	500	mV
Falling 5 V voltage PORZ	V5A_F		4.4	4.5		V
Rising 5 V voltage PORZ	V5A_R			4.6	4.7	V
Hysteresis 5 V, PORZ			50	100		mV
Short-circuit output current PORZ	I_{OS}	V_{OL} = 0.5 V	375		650	µA
Low-level output current, PORZ	I_{OL}				–5	mA
High-level output voltage, PORZ	V_{OH}	V5D = 5 V, I_{OH} = 100 µA	3.5	4		V
Low-level output voltage, PORZ	V_{OL}	V5D = 5 V, I_{OL} = –5 mA		0.3	0.5	V

NOTE: 7. As the power goes up and/or down, comparators and band gap voltage are available at 1.8 V for 5 V supply and 2.5 V for 12 V supply, which allows proper driver disabling through the power-up process.

PORZ Minimum Supply Threshold, PORZ I_{OL} = –5 mA (see Note 8)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V5A (rising from 0)	PV12 = 0 V		0.92	1.5	V
V5A (rising from 0 to 1.5 V)	PV12 = 12 V		0.0	0.5	V
PV12 (rising from 0 to 3.0 V)	V5A = V5D = 5 V		0.0	0.5	V

NOTE: 8. Typical and maximum values indicated are for valid PORZ.

Retract (see Note 9)

Retract voltage range at VCMA	Minimum, VCMA I_O = 40 mA, VRET = OPEN	0.4	0.5	0.6	V
	Maximum†, VCMA I_O = 40 mA, VRET = GND	2.4	3	3.6	V
Retract current limit	VCMA = GND, VRET = OPEN	100	135	170	mA
Retract voltage accuracy†	VCMA IO = 40 mA VRET tied 7.5 kΩ to GND	1	1.5	2	V
Voltage on GPA, GPB, GNA				0.7	V
Voltage GNB		V12–1			V

NOTE: 9. Retract is disabled when temperature exceeds 150°C. This parameter is not tested.
†These parameters are not tested. They are determined by design characterization.

Braking Circuit

VLSD OFF	Software brake			0.7	V
VHSD HIGH	Software brake	20			V
Leakage current, C_{BDLY}	V_{BDLY} = 5 V			200	nA
Brake threshold voltage, BDLY		0.8	1.2	1.4	V
V12-BEMF voltage automatic low voltage brake threshold†	V5A = V5D = 0 PV12 = 0		2.1		V

†These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

Charge Pump (see Notes 10 and 11)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Charge pump output voltage	V12 = 12 V, V5D = 5 V	22	25	26	V
Charge pump output voltage load regulation†	See Note 12		0.015	0.025	V/μA
Oscillator frequency†			4		MHz
Charge time†			0.5		s
Voltage drop in retract	V12 = 12 V, R_L = 6 V5A = V5D = 0, C_p = 0.1 μ			2	V
Voltage after brake	V12 = 12 V, V5A = V5D = 0 BDLY = 0.5 V, TD = 50 ms C_p = 0.1 μ, R_L = 6 MΩ	18			V
Leakage current	V12 = V5A = V5D = 0 V_{CP} = 16 V			250	nA

NOTES: 10. External storage capacitor is typically 1 μF.
11. Minimum voltage that should be maintained on the charge pump to ensure successful delayed brake is typically 18 volts for any TPIC150x device. However, this voltage is a function of the current that the power driver sinks and the power dissipated in the device.
12. The output can drive external N-channel DMOS switches; the effective dc loading should be less than 1 μA.

† These parameters are not tested. They are determined by design characterization.

Voltage Reference (see Note 13)

VREF output	Load 3 mA and –80 μA	2.112	2.2	2.288	V
2VREF output	Load 3 mA and –80 μA	4.224	4.4	4.576	V
Ratio of 2VREF to VREF		1.96	2	2.04	V/V
VREF source current (see Note 14)				3	mA
2VREF source current (see Note 15)				3	mA
VREF sink current (see Note 14)		–80			μA
2VREF sink current (see Note 15)		–80			μA

NOTES: 13. Maximum external capacitive load = 10 μF. TI recommends a load of 1 μF with a 1 mA dc load.
14. Verified from VREF output test.
15. Verified from 2VREF output test.

VCM Input Filter Amplifier (A3)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input bias current	I_{IB}		–1		1	µA
Input offset voltage	V_{IO}		–10		+10	mV
Average temperature coefficient of input offset voltage†	V_{IO}			15		µV/C
Slew rate†	SR	R_L = 10 kΩ, C_L = 60 pF		1		V/µs
Gain (see Note 16)	G		1.9	2	2.1	V/V
Gain bandwidth product†	GBN			1		MHz
Open-loop voltage gain†		f = 1 kHz, R_L = 10 kΩ		60		dB
Supply voltage rejection ratio	PSRR		60	70		dB
Common mode rejection ratio†	CMRR			60		dB
Input voltage range, with respect to VREF†	V_{IC}			±2.2		V
Output swing, with respect to VREF	V_{OPP}	R_L = 10 kΩ (tied to VREF level)	–1.8		+1.8	V

NOTE: 16. Filter gain set internal to device

† These parameters are not tested. They are determined by design characterization.

VCM Current-Loop-Error Amplifier (ERR)

Input bias current	I_{IB}		–1		1	µA
Input offset voltage	V_{IO}		–10		10	mV
Average temperature coefficient of input offset voltage†	V_{IO}			15		µV/C
Slew rate†	SR	R_L = 10 kΩ ,C_L = 60 pF to VREF		1		V/µs
Gain bandwidth product †	GBW			1		MHz
Open-loop voltage gain†		f = 1 kHz, R_L = 10 kΩ		70		dB
Supply voltage rejection ratio	PSRR		60	70		dB
Common mode rejection ratio†	CMRR			60		dB
Input voltage range, with respect to VREF†	V_{IC}			±2.2		V
Output swing, with respect to VREF	V_{OPP}	R_L = 10 kΩ (tied to VREF level)	–1.8		+1.8	V

† These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

VCM Current-Sense Amplifier (ASEN)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input offset voltage	V_{IO}	Measured at SOUT with respect to VREF (RSEN tied to VCMA)	–5	0	+5	mV
Gain	G		2.67	2.73	2.79	V/V
Slew rate†	SR	R_L = 10 kΩ, C_L = 60 pF		1		V/µs
Gain bandwidth product†	GBW			1		MHz
Open-loop voltage gain†		R_L = 10 kΩ		66		dB
Supply voltage rejection ratio	PSRR		60			dB
Common mode rejection ratio	CMRR		55			dB
Common mode input voltage†	V_{IC}		0		12	V
Output swing	V_{OPP}	R_L = 5 kΩ (tied to VREF level)	–1.8		+ 1.8	V

† These parameters are not tested. They are determined by design characterization.

VCM PREDRIVER AMPLIFIER

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage GPA, GPB	V_{OH}	R_L = 6 MΩ	20			V
High level output voltage GNA, GNB	V_{OH}	R_L = 6 MΩ	V12–2			V
Low-level output voltage GPA, GPB	V_{OL}				0.7	V
Low level output voltage GNA, GNB	V_{OL}				0.7	V
Slew rate, positive† GPA, GPB	SR+	C_L = 50 pF, see Note 15		0.5		V/µs
Slew rate, positive† GNA, GNB	SR+	C_L = 50 pF, see Note 16		0.5		V/µs
Slew rate, negative† GPA, GPB	SR–	C_L = 50 pF, see Note 17		2		V/µs
Slew rate, negative† GNA, GNB	SR–	C_L = 50 pF, see Note 17		2		V/µs
Quiescent current†				8		mA
Gain†	G	VCMA to VCMB		12		V/V
Unity gain bandwidth†				1		MHz
Common-mode rejection ratio†	CMRR		60			dB
Power supply rejection ratio†	PSRR		60			dB

NOTES: 17. Slew rate calculated as average positive slew rate from 1 V to 18 V
18. Slew rate calculated as average positive slew rate from 1 V to 10 V
19. Slew rate calculated as average negative slew rate from 18 V to 1 V

† These parameters are not tested. They are determined by design characterization.

Block Gate Driver

High-level output voltage	V_{OH}		20			V
Low-level output voltage	V_{OL}				0.7	V

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

VCO (unless otherwise specified, CVCO = 0.0056 μF)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Typical frequency† f	$\left(\frac{VPE}{2 \cdot 30.48\ k\Omega \cdot VREF \cdot CVCO}\right)$				Hz
	$V_{0(PEFILTER)}$ = 2.16 V	2304	2880	3456	Hz
Idle frequency†	Mode = Reset	106	133	160	Hz
High side CVCO voltage trip level	Ramp CVCO from 3 V to 3.5 V	3	3.3	3.6	V
Low side CVCO voltage trip level	Ramp CVCO from 1.2 V to 0.9 V	1	1.1	1.2	V
Source/Sink Current (CVCO)	PEFILTER = 3 V	75	100	125	μA
Low-level output voltage V_{OL} (–100 μA) SENSE/VCO/TACH				0.5	V
High-level output voltage, V_{OH} (100 μA) SENSE/VCO/TACH		3.5			V
Rise/Fall Time (SENSE/VCO/TACH)†	C_L = 10 pF		100		ns

† These parameters are not tested. They are determined by design characterization.

Phase Error Amplifier

Output voltage V_O $V_{PEFILTER}$, (V_{idle})	Mode = Preset	75	100	125	mV
Output current at PEFILTER, I_O run mode	$V_{0(PEFILTER)}$ = 2.1 V	115	150	175	μA
Source/sink current mismatch	$V_{0(PEFILTER)}$ = 2.1 V	–7%		+7%	
Input offset voltage† V_{IO} PU, PV, or PW See Note 20	PU, PV, or PW	–180		+180	mV
Maximum voltage† PU, PV, and PW				15	V

NOTE: 20. Add 100 Ω resistance in series with PU, PV, and PW inputs to prevent high reverse (below ground) current during start.

† These parameters are not tested. They are determined by design characterization.

Spindle Predriver Amplifier

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage UHSD, VHSD, WHSD	V_{OH}	R_L = 6 MΩ	22			V
Low-level output voltage UHSD, VHSD, WHSD	V_{OL}				0.7	V
High-level output voltage ULSD, VLSD, WLSD	V_{OH}	R_L = 6 MΩ	V12–2			V
Low-level output voltage ULSD, VLSD, WLSD	V_{OL}				0.7	V

Spindle Current-Sense Amplifier

Input voltage range†			0		0.5	V
Closed-loop gain	G	I_{CAL}	6.75	7.5	8.25	V/V
Output swing†	V_{OPP}		0.1		4.5	V
Input offset voltage†	V_{IO}			8		mV

†These parameters are not tested. They are determined by design characterization.

Current-Sense Comparator

Input offset voltage†	V_{IO}			10		mV
Common mode†			0		4	V

†These parameters are not tested. They are determined by design characterization.

TACH Comparator

Input offset voltage	V_{IO}		–10		+10	mV
Hysteresis	V_{hys}		75	100	125	mV
Common mode†			0		4	V

† These parameters are not tested. They are determined by design characterization.

Motor Current Control

I_COS_CHG		80	100	120	µA
I_COS_DCHG		3.0			mA
One shot off time† (see Note 21)	C_{OS} = 0.001 µF, R_{SLEW} = 12.1 kΩ	15	25	35	µs
V_ICNTRL deadband†		80	95	110	mV

NOTE: 21. Minimum one-shot off time regardless of COS and RSLEW values is typically 5 µs.

†These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

POR Delay **PARAMETER**	**CONDITION**	**MIN**	**NOM**	**MAX**	**UNIT**
I_{CHG}	V POR_DELAY = 1 V	3		7	µA
I_{DCHG}	V5A = V5D = 0	2			mA
Threshold voltage V_{TH}		2	2.2	2.4	V

†These parameters are not tested. They are determined by design characterization.

MECHANICAL DATA

Figure 4-1 shows mechanical outline dimensions.

DL (R-PDSO-G56) **PLASTIC SMALL OUTLINE PACKAGE**

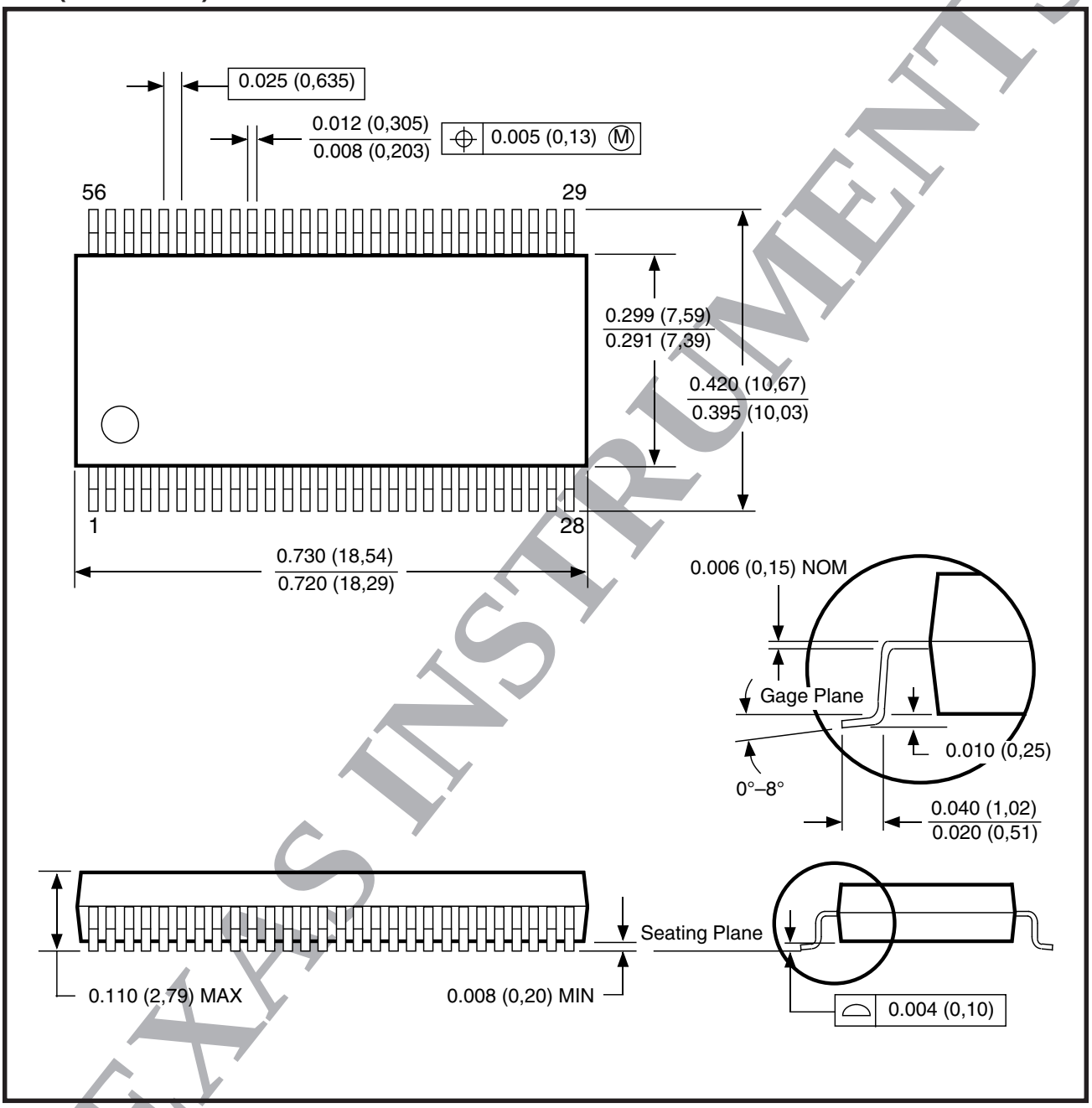


FIGURE 4-1: Mechanical Data

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

TABLE A-1: System Level Responses to Various Inputs

POR	DBRK	V12	ABRK	SBRK	VCM_ENA	SFT_RET	RESET	ENABLEZ	DISPWRZ	SOFTWARE MODE (as selected by RESET, ENABLEZ, and DISPWRZ)	SPIN MOTOR	GPA, GPB, GNA	GNB	VCM_RET	VCM_BRK	VCM	RETRACT
1	0	>10.4 V	0	0	1	0	0	0	1	RUN	RUN	ON	ON	0	0	ON	OFF
1	0	>10.4 V	0	0	X	1	0	0	1	RUN	RUN	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	0	0	0	0	0	0	1	RUN	RUN	LOW	LOW	1	1	OFF	OFF
1	0	>10.4 V	0	1	1	0	1	0	0	BRAKE	BRAKE	ON	ON	0	0	ON	OFF
1	0	>10.4 V	0	1	X	1	1	0	0	BRAKE	BRAKE	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	0	1	0	0	1	0	0	BRAKE	BRAKE	LOW	LOW	1	1	OFF	OFF
1	0	>10.4 V	0	0	1	0	0	0	0	COAST	COAST	ON	ON	0	0	ON	OFF
1	0	>10.4 V	0	0	X	1	0	0	0	COAST	COAST	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	0	0	0	0	0	0	0	COAST	COAST	LOW	LOW	1	1	OFF	OFF
0	0	>2 V	0	X	X	X	X	X	X	XXX	COAST	LOW	HI	1	0	OFF	ON
0	1	>2 V	0	X	X	X	X	X	X	XXX	BRAKE	LOW	LOW	1	1	OFF	OFF
0	X	<2 V	1	X	X	X	X	X	X	XXX	BRAKE	LOW	HI	1	0	OFF	ON

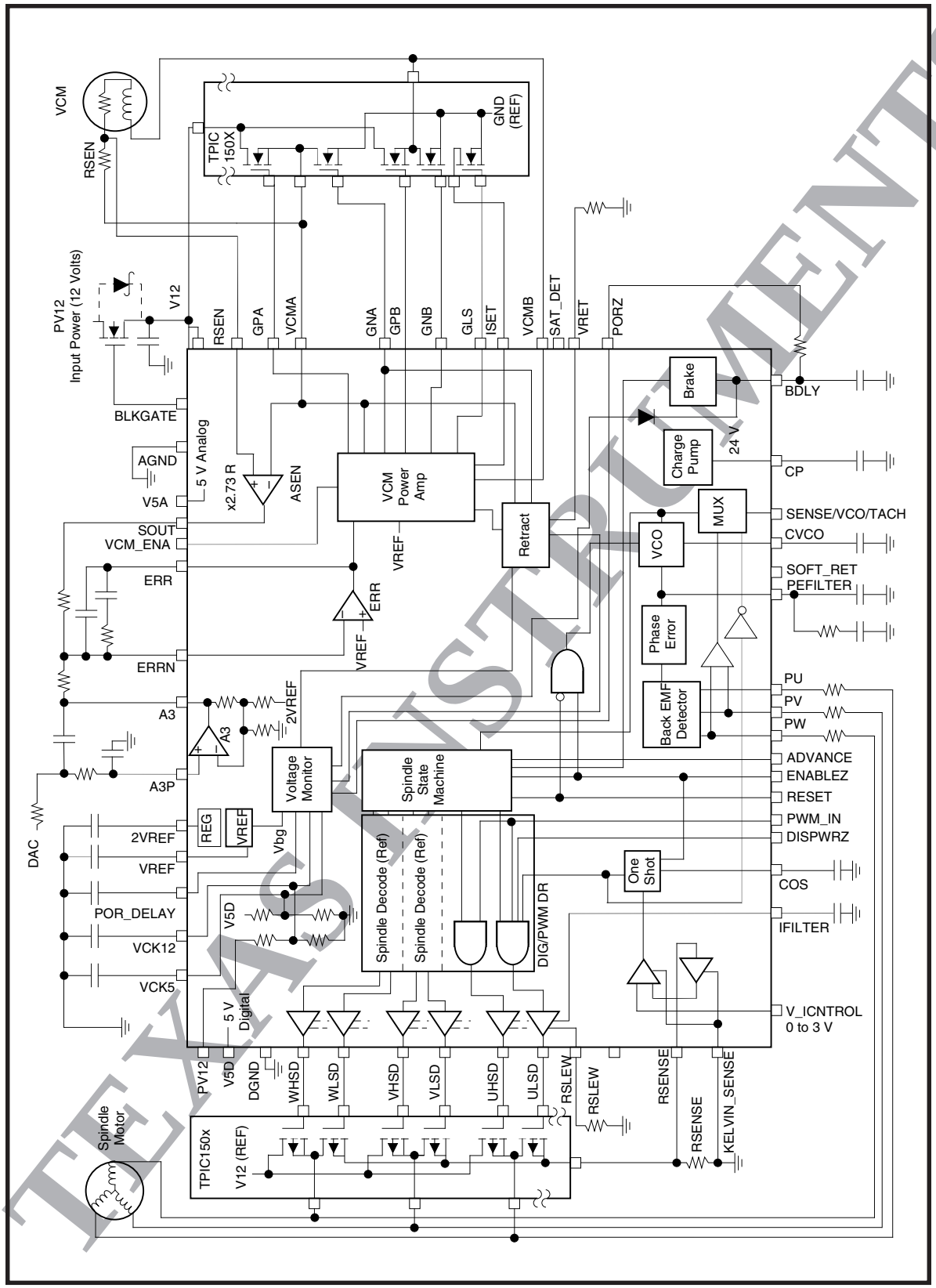


FIGURE B-1: Typical Application

NOTES: All external FETs are located in TPIC150x drive array except for PV12 blocking FET.

LATCH-UP TEST PARAMETERS

TABLE: C-1. Latch-Up Test† Parameters

TERMINAL NO.	TERMINAL NAME	MAXIMUM NEGATIVE CURRENT (mA)‡	TYPICAL VF, TA = 25°C, (V)§	MAXIMUM POSITIVE CURRENT (mA)
1	VLSD	-800	-1.8	+250
2	ULSD	-800	-1.8	+250
3	IFILTER	-250	-0.5	+250
4	PWM_IN	-250	-0.5	+250
5	KELVIN_SENSE	-250	-0.5	+250
6	COS	-250	-0.5	+250
7	V_ICNTRL	-250	-0.5	+250
8	RSENSE	-250	-0.5	+250
9	RSLEW	-250	-0.5	+250
10	DISPWRZ	-250	-0.5	+250
11	RESET	-250	-0.5	+250
12	ENABLEZ	-250	-0.5	+250
13	ADVANCE	-250	-0.5	+250
14	AGND			
15	V5A			
16	PW	-800	-1.8	+250
17	PV	-800	-1.8	+250
18	PU	-800	-1.8	+250
19	SENSE/VCO/TACH	-250	-0.5	+250
20	PEFILTER	-250	-0.5	+250
21	CVCO	-250	-0.5	+250
22	SOUT	-250	-0.5	+250
23	RSEN	-450	-1.3	+250
24	GLS	-250	-0.5	+250
25	ISET	-250	-0.5	+250
26	GNB	-400	-1.2	+250
27	VCMB	-400	-1.2	+250
28	GPB	-350	-1.1	+250

† For design qualification purposes latch-up testing has been done on sample units to ensure that no latch up occurs when the currents specified are applied to any pin.

‡ Current specified is for a pulse with a maximum duration of 10 ms.

§ Voltage is specified with respect to ground.

TABLE: C-1. Latch-Up Test† Parameters (continued)

TERMINAL NO.	TERMINAL NAME	MAXIMUM NEGATIVE CURRENT (mA)‡	TYPICAL VF, TA = 25°C, (V)§	MAXIMUM POSITIVE CURRENT (mA)
29	GNA	-400	-1.2	+250
30	GPA	-350	-1.1	+250
31	VCMA	-400	-1.2	+250
32	ERR	-250	-0.5	+250
33	A3	-250	-0.5	+250
34	A3P	-250	-0.5	+250
35	ERRN	-250	-0.5	+250
36	V12			
37	SAT_DET	-250	-0.5	+250
38	SOFT_RET	-250	-0.5	+250
39	VCM_ENA	-250	-0.5	+250
40	POR_DELAY	-250	-0.5	+250
41	CP	-250	-0.5	+250
42	2VREF			
43	VREF			
44	BDLY	-250	-0.5	+250
45	VRET	-250	-0.5	+250
46	PORZ	-250	-0.5	+250
47	VCK5	-250	-0.5	+250
48	VCK12	-250	-0.5	+250
49	BLKGATE	-800	-1.8	+250
50	PV12			
51	V5D			
52	DGND			
53	WHSD	-800	-1.8	+250
54	VHSD	-800	-1.8	+250
55	UHSD	-800	-1.8	+250
56	WLSD	-800	-1.8	+250

† For design qualification purposes latch-up testing has been done on sample units to ensure that no latch up occurs when the currents specified are applied to any pin.

‡ Current specified is for a pulse with a maximum duration of 10 ms.

§ Voltage is specified with respect to ground.

TEST PLAN ADDENDUM

TABLE: D-1. VCM Functional Test a

PARAMETER	TEST CONDITIONS	TEST DESCRIPTION	VOLTAGE	MIN	MAX	UNIT	PIN
A) Source current of the gate drivers GPA and GNB	VCM_ENA is high, ERRN is high (5 V)	Measure source current at GPA	16 V	30	70	µA	V_GPA
			9 V	30	70	µA	
			7.5 V	60	120	µA	
			6 V	120	215	µA	
A) Source current of the gate drivers GPA and GNB	VCM_ENA is high, ERRN is high (5 V)	Measure source current at GNB	11 V	30	70	µA	V_GPB
			3 V	30	70	µA	
			1 V	60	135	µA	

PARAMETER	TEST CONDITIONS	TEST DESCRIPTION	MIN	NOM	MAX	UNIT	PIN
B) Resistance of the gate driver GPA	VCM_ENA is high, ERRN is high (5 V)	1. Apply 5 V to GPA & measure the voltage V_1 and current I_1 2. Apply 3 V to GPA and measure the voltage V_2 and current I_2 3. Compute the resistance: R = (V2 - V1)/(I2 - I1)	7	10	13	kΩ	
C) Relative change in the current of gate drivers GPA and GNB	VCM_ENA is high, ERRN is high (5 V)	GPA ratio: (IGPA(16 V) - IGPA (9 V) / IGPA (9 V)			20%		
	VCM_ENA is high, ERRN is high (5 V)	GNB ratio: (IGNB(11 V) - IGNB (3 V) / IGNB (3 V)			20%		

TABLE: D-1. VCM Functional Test b

PARAMETER	TEST CONDITION	TEST DESCRIPTION	VOLTAGE	MIN	MAX	UNIT	PIN
A) Source current of the gate drivers GPB and GNA	VCM_ENA is high, ERRN is low (0 V)	Measure source current at GPB	16 V	30	70	µA	V_GPB
			9 V	30	70	µA	
			7.5 V	60	120	µA	
			6 V	120	215	µA	
A) Source current of the gate drivers GPB and GNA	VCM_ENA is high, ERRN is low (0 V)	Measure source current at GNA	11 V	30	70	µA	V_GNA
			3 V	30	70	µA	
			1 V	60	135	µA	

PARAMETER	TEST CONDITION	TEST DESCRIPTION	MIN	NOM	MAX	UNIT	PIN
B) Resistance of the gatedriver GPB	VCM_ENA is high, ERRN is low (0 V)	1. Apply 5 V to GPB & measure the voltage V_1 and current I_1 2. Apply 3 V to GPB and measure the voltage V_2 and current I_2 3. Compute the resistance: R = (V2 - V1)/(I2 - I1)	7	10	13	kΩ	
C) Relative change in the current of the gate drivers GPB and GNA	VCM_ENA is high, ERRN is low (0 V)	GPB ratio: (IGPB(16 V) - IGPB (9 V) / IGPB (9 V)		20%			
	VCM_ENA is high, ERRN is low (0 V)	GNA ratio: (IGNA(11 V) - IGNA (3 V) / IGNA (3 V)			20%		

TABLE D-3: Spindle Drive Current Test (Start Mode)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
High Side Gate Driver Slew Current (See Figure 2-14)	MODE = START: (RESET = 0, ENABLEZ = 1, DISPWRZ = 1), IRSLEW = 100 µA ADVANCE used to switch between comm. states. Cp = 0.1 µF (These conditions apply to entire table.)				
I_{CHG1}	V_{GHS} = 0 V	0.5	1		mA
I_{DCHG1} (See Note and Figure 2-14)	V_{GHS} = 15 V	300		750	µA
I_{DCHG2} (See Note and Figure 2-14)	V_{GHS} = 3 V	200		450	µA
$I_{DISCHARGE}$ (nonslewing gate)	V_{GHS} = 1.5 V	0.5		4.5	mA
Low side Gate Driver Slew Current (See Figure 2-16)					
I_{CHG3}	PWMIN = High, V_{GLS} = 6 V	1		3.1	mA
I_{DCHG3} (See Figure 2-15 and Equation 16)	PWMIN = Low, V_{GLS} = 1.5 V	0.3		2	mA
I_{DCHG4} (See Figure 2-15 and Equation 17)	PWMIN = Low, V_{GLS} = 12 V	0.75		1.5	mA
I_{DCHG5} (See Figure 2-15 and Equation 18)	PWMIN = Low, V_{GLS} = 2 V	0.35		1	mA
$I_{DISCHARGE}$ (Nonslewing gate)	PWMIN = Low, V_{GLS} = 1.5 V	1		3	mA

NOTE: I_{DC1} is at high voltage region.

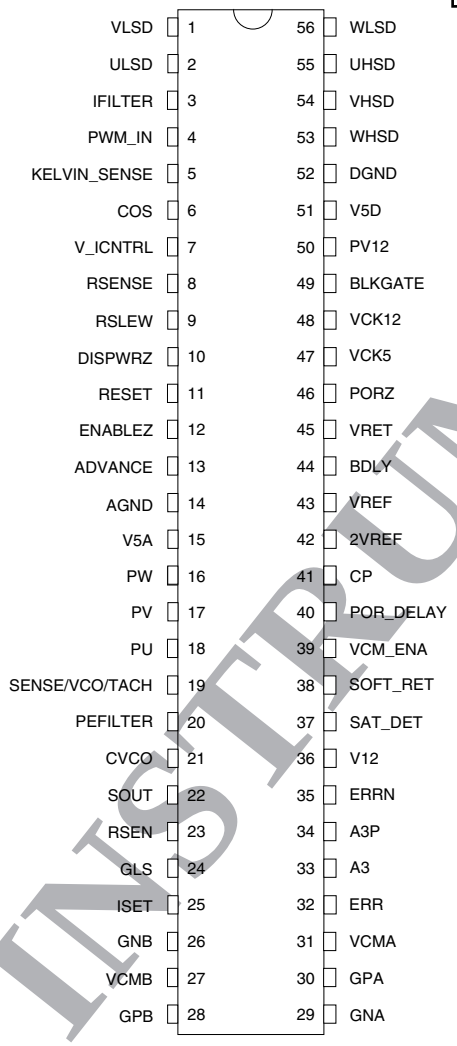
TABLE D-4: Spindle Current Test (Preset, Coast, Brake Modes)

PROCEDURE	TEST CONDITIONS	TEST DESCRIPTION	PARAMETER	VOLTAGE	MIN	NOM	MAX	UNIT
A) Spindle sink current test in preset mode	MODE = PRESET: (RESET = 1 ENABLEZ = 1 DISPWRZ = 1) RSLEW = 12.1 kΩ or 100 µA	During PRESET, all of the gate drivers are held low by pulling them down internally.	HSD Sink Current	2 V	150			µA
			LSD Sink Current	2 V	300			µA
B) Spindle sink current test in coast mode	MODE = COAST: (RESET = 0 ENABLEZ = 0 DISPWRZ = 0) RSLEW = 12.1 kΩ or 100 µA	During COAST, all the gate drivers are held low by pulling them down internally.	HSD Sink Current	2 V	1			mA
			LSD Sink Current	2 V	1.3	1.8	2.5	mA
C) Spindle sink current test in brake mode	MODE = BRAKE: (RESET = 1 ENABLEZ = 0 DISPWRZ = 0) RSLEW = 12.1 kΩ or 100 µA	During BRAKE, all low side drivers are held low by pulling them down internally. The high side drivers are turned high to execute a brake, hence source current is measured for them.	HSD Source Current	10 V	300			µA
			LSD Sink Current	2 V	3			mA

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



TLS2232
DL Package

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TI TLS2232 56-Pin Servo-Combination Predriver	TLS2232CDLR	T2232CB

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

TLS2233
Servo-Combination Predriver

September 1998

DESCRIPTION

The TLS2233 is a servo-combination predriver designed for use in hard-disk-drive applications. When combined with a power driver such as the TPIC150x, the TLS2233 can drive a voice-coil motor (VCM) and a spindle motor. Figure 1–1 is a functional block diagram of the servo-combination predriver.

FEATURES

VOICE-COIL MOTOR (VCM) PREDRIVER

- **Pulse-width modulated (PWM) input control**
- **Transconductance amplifier with class AB output (when used with TPIC150x drivers)**
- **Summing amplifier**
- **Current-sense amplifier**
- **Retract function on power loss or command**
- **Error amplifier clamp during retract**

SPINDLE MOTOR PREDRIVER

- **PWM start and PWM current limit**
- **Advance terminal signals commutation timing to on-chip sequencer during start mode**
- **Current-sense comparator**
- **Low-noise phase-locked loop performs commutation timing during run mode**
- **PWM run mode**
- **Power-down brake after delay**

SUPPORT FUNCTIONS

- **Voltage monitor (based on 5 V and 12 V supplies)**
- **Low-voltage brake**
- **Charge pump (25 V) for driving N-channel DMOS H-bridge drivers**

DETAILED DESCRIPTION

VOICE-COIL MOTOR DRIVE

The TLS2233 uses either a pulse-width-modulated (PWM) or linear input voltage to control the current applied to the VCM. A set of precision buffers provides input scaling for two separate PWM inputs that, when used together, can provide increased resolution. The bandwidth of the low-pass filter is determined by external components and is matched to the PWM digital-to-analog converter (DAC) being used. If linear voltage control is desired, the PWM buffers and the low-pass filter function are bypassed and the control signal is applied directly to the error amplifier. The error amplifier compensates for the transconductance loop. Its output represents the difference between the command current and the actual current. The actual current is measured across the RSEN resistor by the sense amplifier. The compensated output of the error amplifier is applied to the VCM predrive circuit that biases the VCM power field-effect transistors (FETs) of the TPIC150x for class AB operation.

SPINDLE MOTOR DRIVE

The spindle motor is started under PWM control using an external signal for forced commutation. As the motor approaches operational speed, the commutation state machine is driven by the output of the voltage-controlled oscillator (VCO). The VCO utilizes the back electromotive force (BEMF) of the motor to close a phase-locked loop, matching the commutation frequency to the motor. Once in the run mode, the motor speed can be controlled using a PWM signal to modulate the voltage applied to the motor.

SUPPORT FUNCTIONS

The TLS2233 support functions include a voltage monitor that indicates a fault when power supply voltages are out of tolerance. When triggered, this fault signal initiates a VCM retract and delayed braking of the spindle motor. Other support functions include the reference-voltage buffers and the charge pump. The reference voltages are supplied to several on-chip requirements and provide an external 2 • VREF output. The charge pump generates 25 V for driving the TPIC150x N-channel DMOS H-bridge drivers.

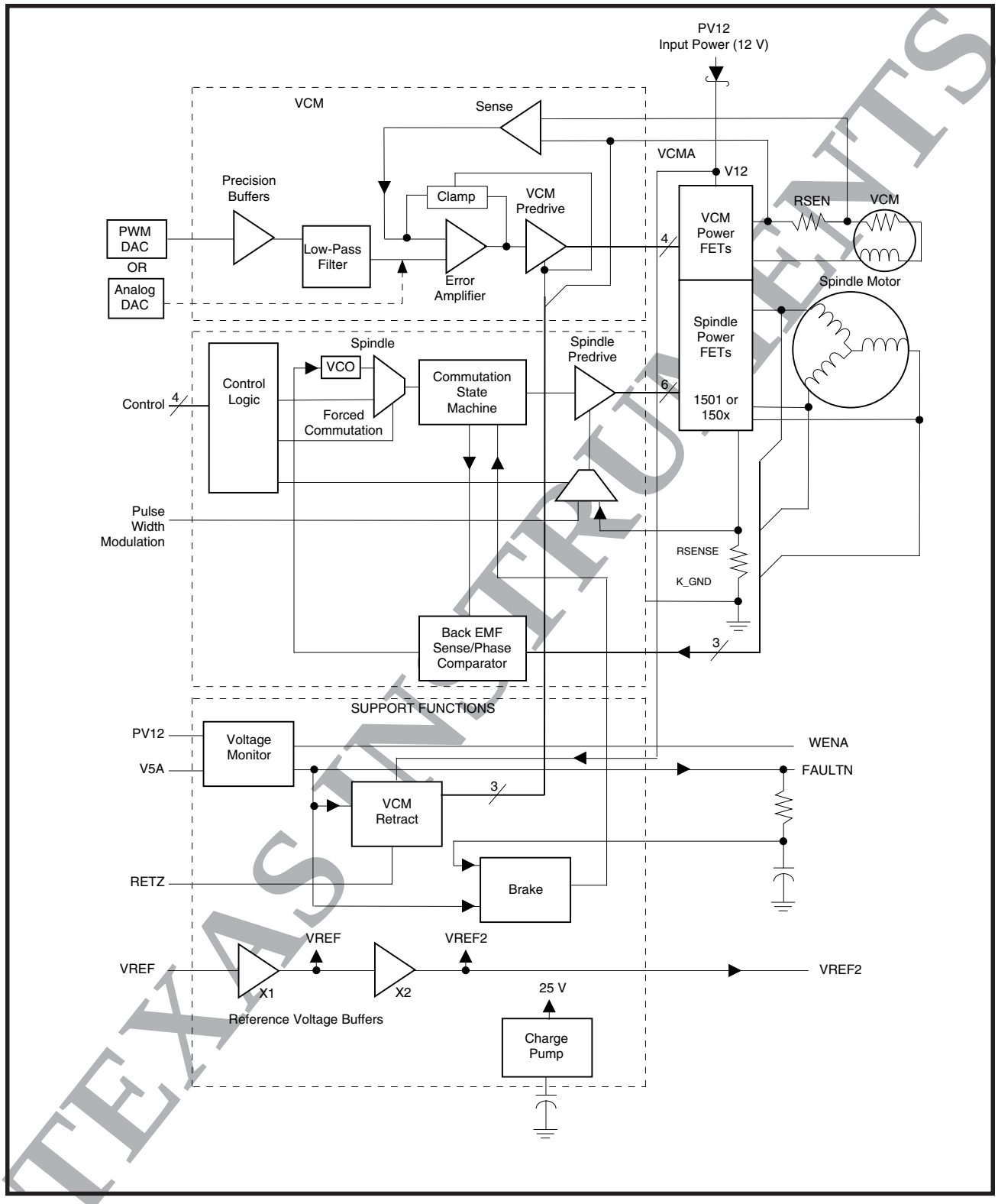


FIGURE 1-1: Functional Block Diagram

DETAILED DESCRIPTION (continued)

VOICE-COIL MOTOR PREDRIVER

The TLS2233, when combined with a power driver such as the TPIC150x, provides current-drive capability for the VCM. Figure 2–1 shows a typical application; PWM signals applied to SPWMAI and SPWMBI indicate the level of current delivered to the VCM. External resistors on the SPWMAO and SPWMBO outputs scale the PWM signals to increase the effective resolution of the PWM input. Amplifier A3 filters these signals so that the information contained in their respective duty cycles is represented by a linear voltage. This voltage, which represents the current command, is applied to the transconductance loop. The output of the summing amplifier (ERR) is the difference between the commanded current and the actual current as measured across RSEN by the differential amplifier (ASEN). This error signal is applied to the predriver that biases the power FETs of the TPIC150x for class AB operation.

NOTE: The GNA and GNB terminals can be connected to external 10-MΩ to 20-MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2233.

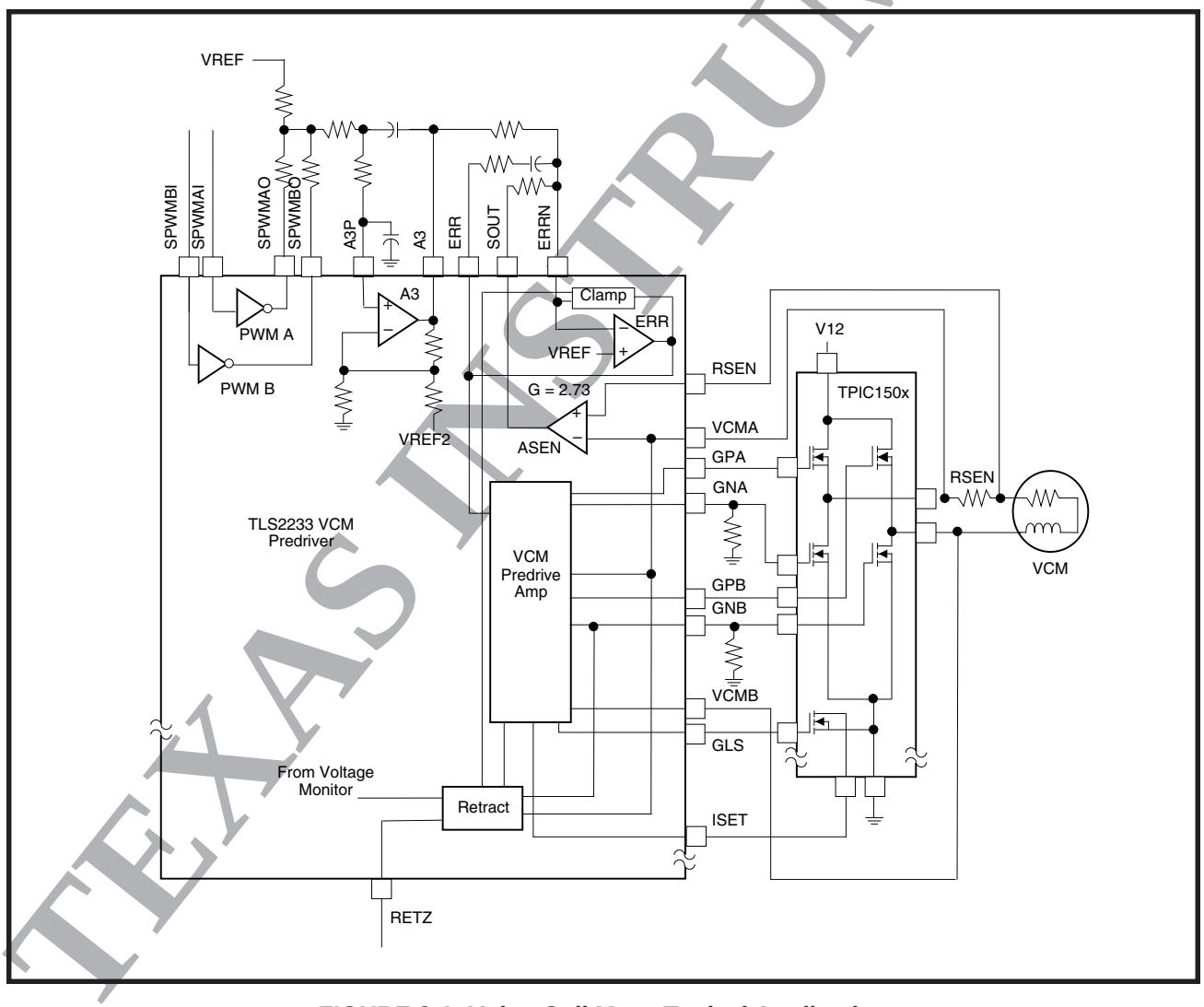


FIGURE 2-1: Voice-Coil MotorTypical Application

Pulse-Width Modulation Sampling Inverters

The sampling inverters act as buffers for the PWM inputs at SPWMAI and SPWMBI. The output of these inverters provides a precision controlled 0-to-VREF2 peak-to-peak waveform.

Input-Filter Amplifier (A3)

The input-filter amplifier (A3) filters the PWM inputs. This amplifier can be used to implement a Sallen and Key low-pass filter, as shown in Figure 2–2.

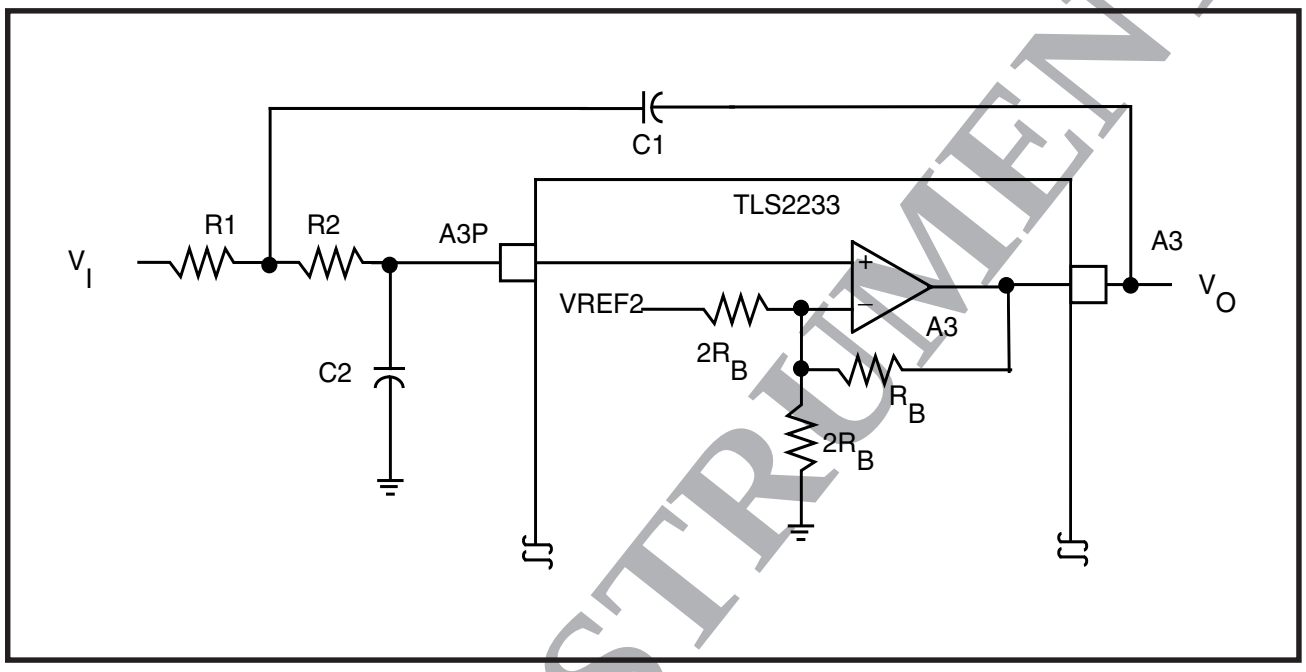


FIGURE 2-2: Sallen and Key Low-Pass Filter Implementation

The transfer function of this circuit is shown in equations 1, 2, 3, and 4.

$$H(S) = \frac{K\omega^2}{S^2 + \frac{\omega}{Q}S + \omega^2} \quad (1)$$

$$K = 1 + \frac{R_B}{2R_B \| 2R_B} = 2;\ R_B \text{ matched internal components} \quad (2)$$

$$Q = \frac{1}{3 - K} = 1 \quad (3)$$

$$\omega = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \quad (4)$$

R1, R2, C1, and C2 are chosen to match ω to the PWM DAC being used.

VOICE-COIL MOTOR PREDRIVER (continued)

Summing Amplifier (ERR)

Summing amplifier (ERR) is used to generate an error between the command current and the actual current, and to apply compensation for the transconductance loop (see Figure 2–3).

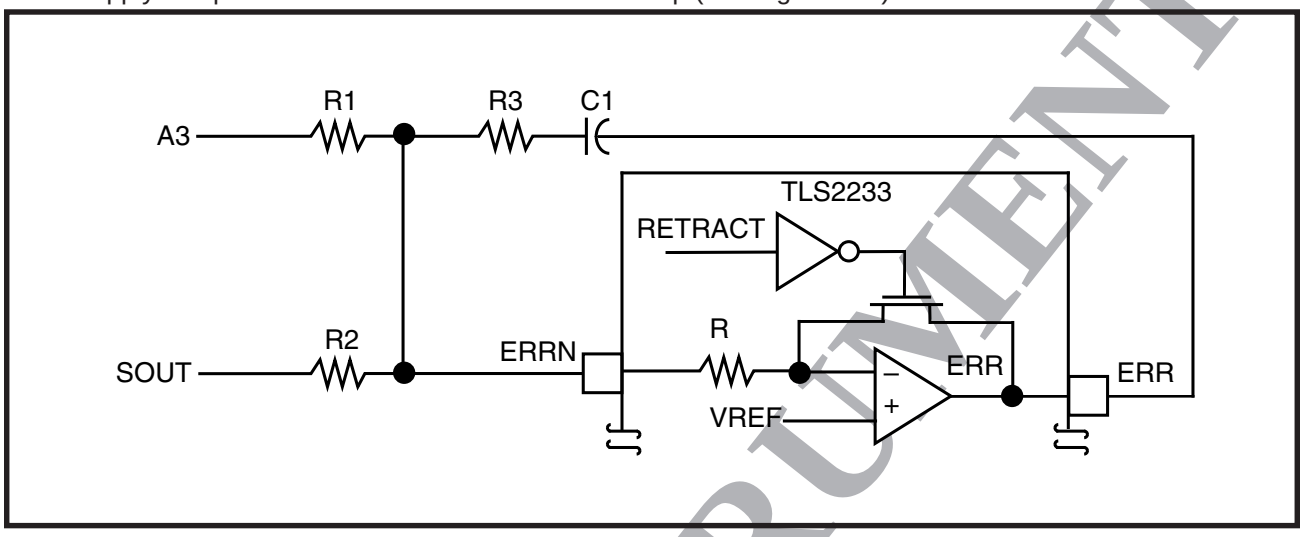


FIGURE 2-3: Summing Amplifier (ERR) Implementation

The transfer function of this circuit is shown in equation 5.

$$H(S) = \frac{(R3\ C1)s + 1}{(RC1)s} \quad (5)$$

Where: R = R1 = R2

Selecting R_1, R_2, and RSEN sets the VCM transconductance gain (Gm) (see equation 6).

$$Gm = \frac{I_{VCM}}{VCMB} = \frac{R2}{2.73 \bullet R1 \bullet RSEN} \quad (6)$$

A clamp transistor across ERR and ERRN turns on when a retract is commanded by RETZ or when the voltage monitor senses a voltage fault.

Current-Sense Amplifier (ASEN)

The current-sense amplifier (ASEN) provides a measure of the current delivered to the motor by measuring the voltage across the sense resistor. The gain of this amplifier is fixed at 2.73. The ASEN offset can be calibrated by commanding a software brake (see the Brake subsection , and the Support Functions Brake subsection) to ensure that the VCM driver transistors are turned off and that no current is delivered to the VCM. In this state, SOUT should be equal to V_{REF}.

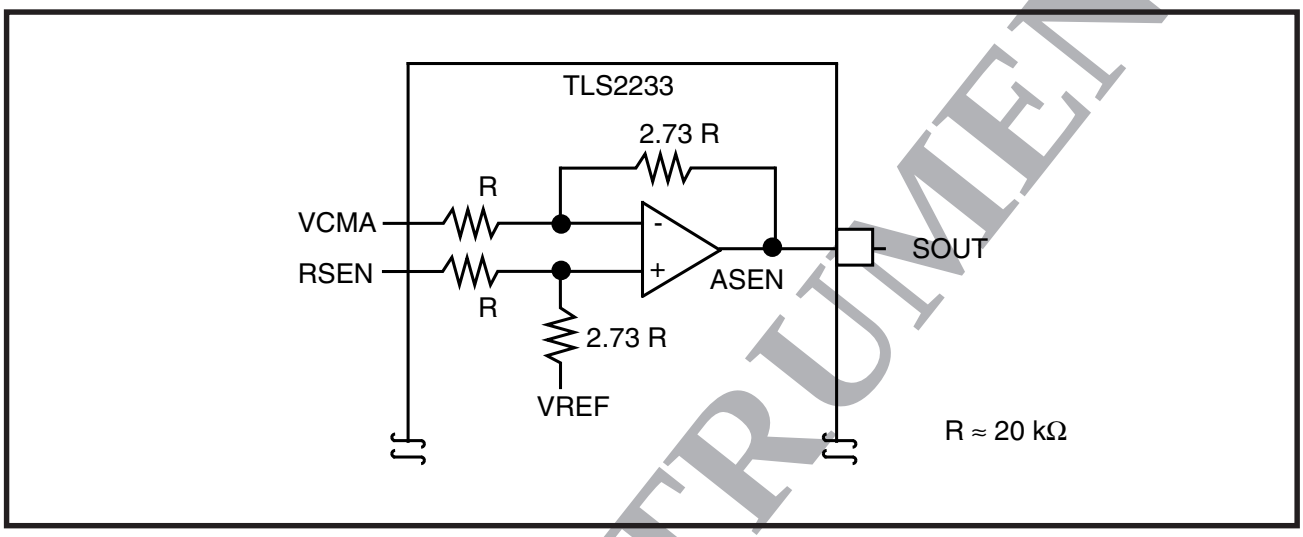
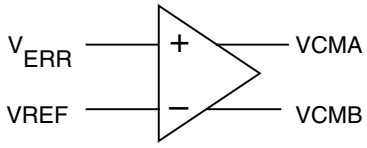


FIGURE 2-4: Current-Sense Amplifier (ASEN) Implementation

VCM Predriver Amplifier

The VCM predriver amplifier biases and operates the power FETs of the TPIC150x as a class AB amplifier with a gain of 12. The relationship is shown in equation 7.

$$\frac{VCMA - VCMB}{V_{ERR} - VREF} = 12 \qquad (7)$$



VCM Predriver Amplifier (continued)

The VCM predriver amplifier uses signals GLS and ISET to determine the bias point for the TPIC150x power FETs (see Figure 2–5). A constant current source is applied to ISET, and the voltage at GLS, the gate voltage for the TPIC150x sense FET, is varied until the voltage on ISET matches a known reference (1/2) V12. The voltage at GLS is then scaled and used to set the bias point of the TPIC150x power FETs, as shown in equation 8.

$$I_{quiescent} \approx (150) \bullet I_{source} \quad (8)$$

Where: $I_{quiescent}$ is the bias current in the VCM H-bridge and $I_{source} \approx 40\ \mu A$.

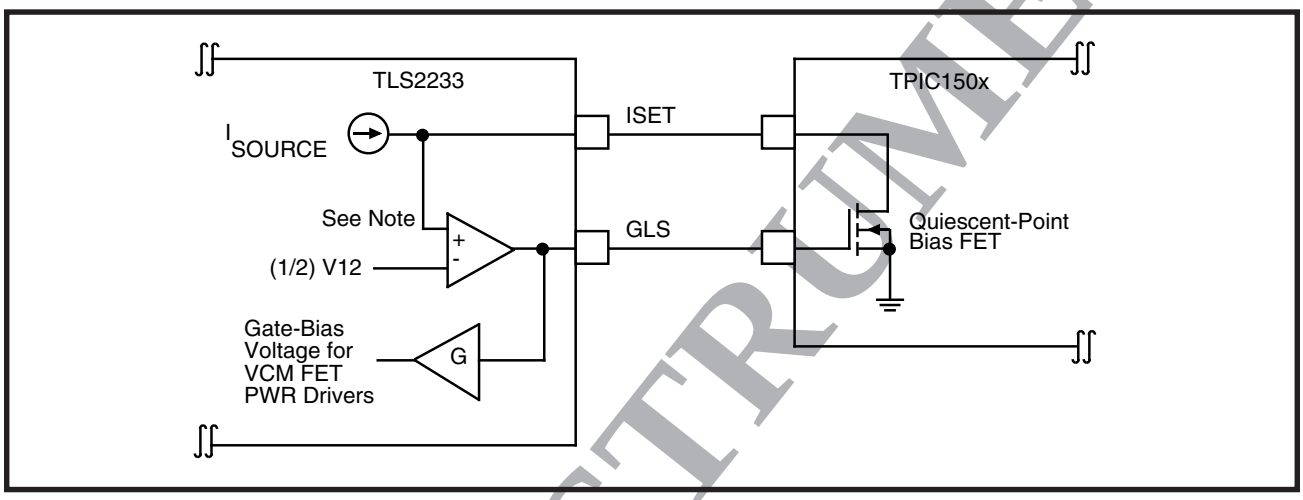
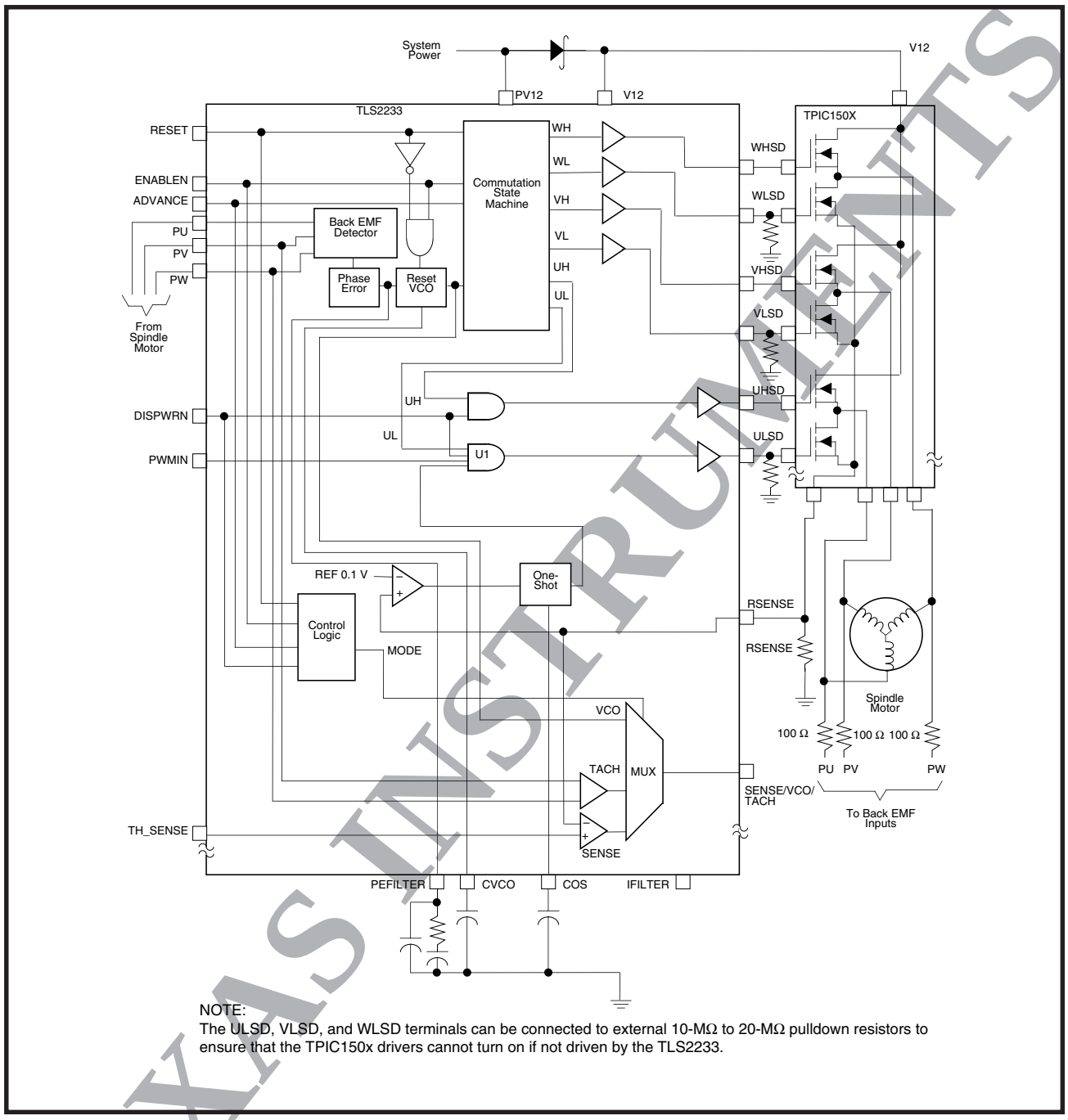


FIGURE 2-5: GLS and ISET Biasing the TPIC150x Power FETs

NOTE: This input is effectively the negative input when the entire system is considered.



NOTE:
The ULSD, VLSD, and WLSD terminals can be connected to external 10-MΩ to 20-MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2233.

FIGURE 2-6: Spindle Motor Predriver Functional Block Diagram

SPINDLE MOTOR PREDRIVER

Spindle Motor Predriver Functional Overview

Figure 2–6 shows the spindle motor predriver section of the TLS2233. The RESET, ENABLEN, ADVANCE, and DISPWRN signals command one of six different operational modes:

- Preset
- Start/SENSE
- Start/TACH
- Run
- Coast
- Brake

The preset, start/SENSE, and start/TACH modes are used to start the spindle motor. The commutation state machine controls motor commutation by enabling the appropriate TPIC150x high- and low-side drivers.

During start-up, the commutation state machine is advanced by pulses applied on ADVANCE. As the spindle motor approaches idle frequency, the run mode is selected. At this time, the commutation state machine is advanced by the output of the VCO. The BEMF detector and phase-error amplifier generate an error signal that is applied to the input of the VCO. The use of this error signal adjusts the commutation frequency to the spindle motor.

In the run mode, the voltage applied to the motor is adjusted by PWM control.

For PWM control, the output of gate U1 is applied to the low-side driver of the spindle motor. The PWMIN signal to gate U1 modulates the voltage applied to the spindle motor. If the maximum current that is adjustable by the selection of RSENSE is exceeded, the one-shot timing forces the output of U1 low to turn off the low-side driver.

The MUX shown in Figure 2–6 implements the logic illustrated in Figure 2–7. The TACH, SENSE, and VCO outputs are combined with the indicated mode signals to provide a real-time status signal at SENSE/VCO/TACH. This status signal provides information for monitoring the current status of the predriver controls and can be used to implement other control circuitry. Table 2–1 lists the multiplexed signal that is present at SENSE/VCO/TACH for each mode of operation.

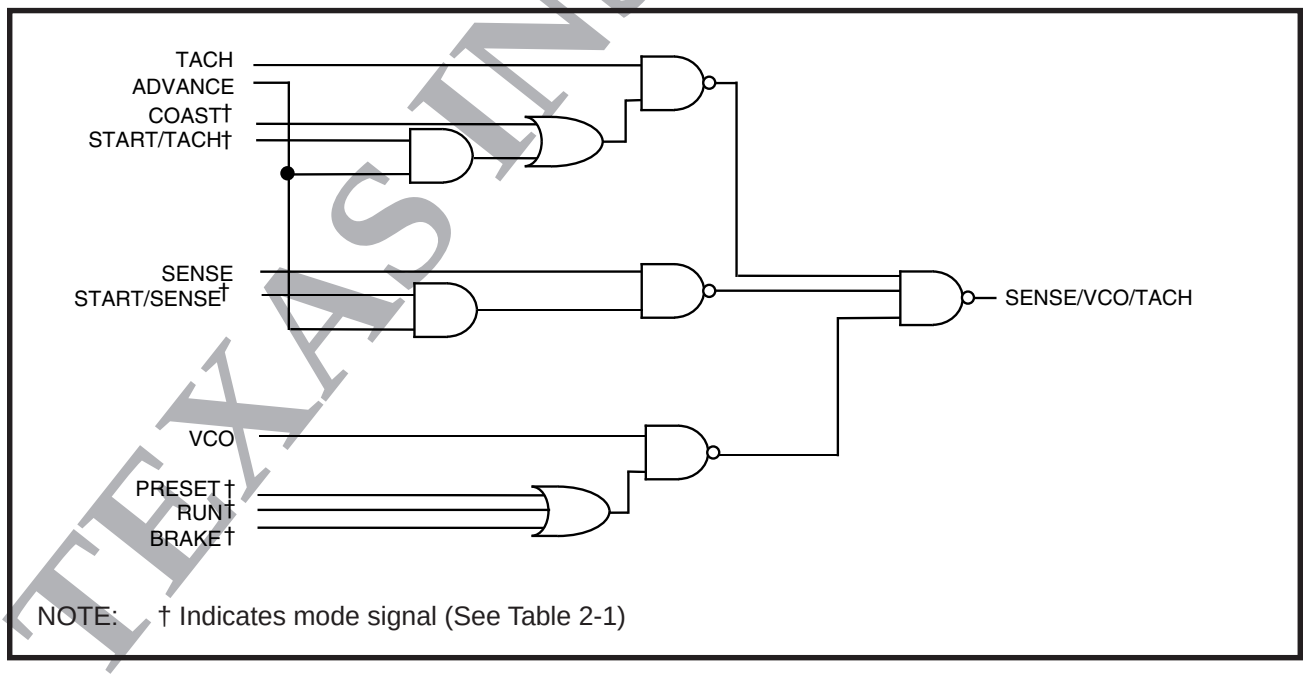


FIGURE 2-7: SENSE/VCO/TACH Multiplexer Logic

SPINDLE MOTOR PREDRIVER (continued)

Spindle Motor Predriver Modes of Operation

The TLS2233 spindle motor predriver circuitry operates in one of six modes as selected by RESET, ENABLEN, ADVANCE, and DISPWRN. Table 2–1 lists the combinations of these signal states, which are used to select either the preset, start/SENSE, start/TACH, run, coast, or brake mode.

TABLE 2–1: Modes of Operation

MODE	DISPWRN	RESET	ENABLEN	ADVANCE	SENSE/ VCO/TACH	VCO	STATE MACHINE
Preset	1	1	1	X	VCO	Idle	Reset
Start/SENSE	1	0	1	1 †	SENSE	Reset	Run
Start/TACH	1	0	1	0 ‡	TACH	Reset	Run
Run	1	0	0	X	VCO	Run	Run
Coast	0	0	0	X	TACH	Run	Run
Brake	0	1	0	X	VCO	Idle	Reset

† Forces SENSE on the SENSE/VCO/TACH output. To advance the state machine, this signal is switched to 0 and then back to 1.

‡ Forces TACH on the SENSE/VCO/TACH output. For forced commutation, this signal is switched to 1 and then back to 0.

The transitions between the various modes should be done according to the diagram shown in Figure 2–8 to prevent logic race conditions.

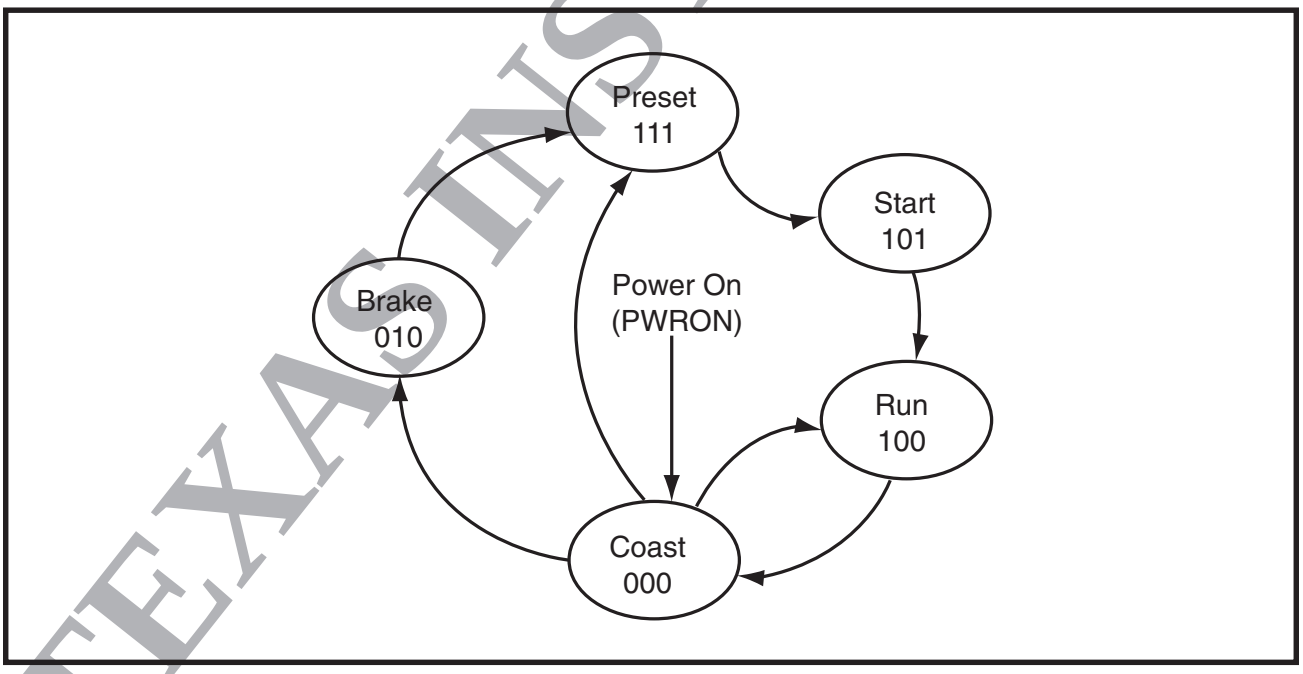


FIGURE 2-8: Mode Transition State Diagram

Spindle Motor Predriver Modes of Operation
(continued)

Preset

In the preset mode, a fixed voltage of 100 mV is applied at the input to the VCO, causing it to operate at its idle frequency. The VCO idle frequency, which is available at the SENSE/VCO/TACH output, can be measured so that switching over (handing off) from forced commutation to closed-loop commutation is accomplished at a frequency within the lock range of the phase-locked loop.

NOTE: To allow the filter network to settle, the VCO idle frequency measurement should be made after the preset mode has been commanded for at least 200 ms.

Start/SENSE

The start/SENSE mode can be used to determine the approximate position of the spindle motor rotor to initialize the commutation state machine. The output of the SENSE comparator is available at the SENSE/VCO/TACH output. The SENSE comparator switches from low to high when the voltage across the RSENSE resistor exceeds the voltage applied at TH_SENSE.

Start/TACH

The start/TACH mode is used to start the spindle motor. PWMIN is held high during motor startup so that the maximum current, which is determined by the selection of RSENSE, is applied to the spindle motor. This results in maximum spindle motor acceleration. When the current reaches the maximum current threshold, the one shot disables the low-side spindle motor drive creating a constant off time that is set by the external capacitor (COS). This capacitor should be selected to optimize the spin-up time and provide sufficient overcurrent protection.

Equations 9 and 10 define the selection of COS.

$$COS = \frac{I}{\Delta V} \bullet \Delta t \quad (9)$$

$$COS = \left(\frac{0.55}{RSLEW}\right) \bullet \Delta t \quad (10)$$

Where: COS is in farads
RSLEW is in ohms
Δ t is of f time in seconds
RSLEW is chosen according to equations 11-18.

NOTE: Adjusting RSLEW also affects the spindle driver slew rates as described in the Run subsection.

Since the BEMF from the spindle motor is low during startup, the commutation state machine must be advanced manually using ADVANCE. This is done open loop, using a timing algorithm matched to the dynamics of the spindle motor.

During open-loop acceleration, the VCO is held at reset. When the frequency of the signal being applied to ADVANCE exceeds the VCO idle frequency measured in the PRESET mode, select the run mode. This action releases the VCO, enabling it to advance the commutation state machine.

NOTE: Although the TACH output is available during the start/TACH mode, the TACH output contains noise induced by current-limit switching. TI recommends that coast mode be used for making TACH measurements.

Run

In the run mode, the commutation state machine is advanced by the output of the VCO. The voltage of each phase (PU, PV, and PW) is monitored to determine if commutation occurs late or early.

NOTE: A 100 Ω series resistor should be used between the PU, PV, and PW inputs and the spindle motor to prevent high reverse current during start.

This is accomplished by generating a signal that is the undriven phase minus the average of the two driven phases. This generated signal is inverted every other cycle to obtain positive pulses. If commutation occurs too early, an increasing positive signal is generated that increases the VCO frequency aligning the commutation with the spindle motor winding.

The spindle motor speed is regulated by adjusting the voltage applied to the spindle motor. This is accomplished by adjusting the PWMIN duty cycle.

Coast

During coast mode, the spindle motor drivers are disabled and the spindle spins freely. During this mode, the TACH signal is available at SENSE/VCO/TACH.

Brake

During brake mode, all of the spindle motor high-side drivers are turned on. This causes the motor to brake dynamically. When the VCM retract function is activated during a power-loss condition, a brake command is ignored.

Commutation Control

The commutation process involves sequentially turning the spindle motor high- and low-side drivers on and off as illustrated in Figure 2–9 and listed in Table 2–2.

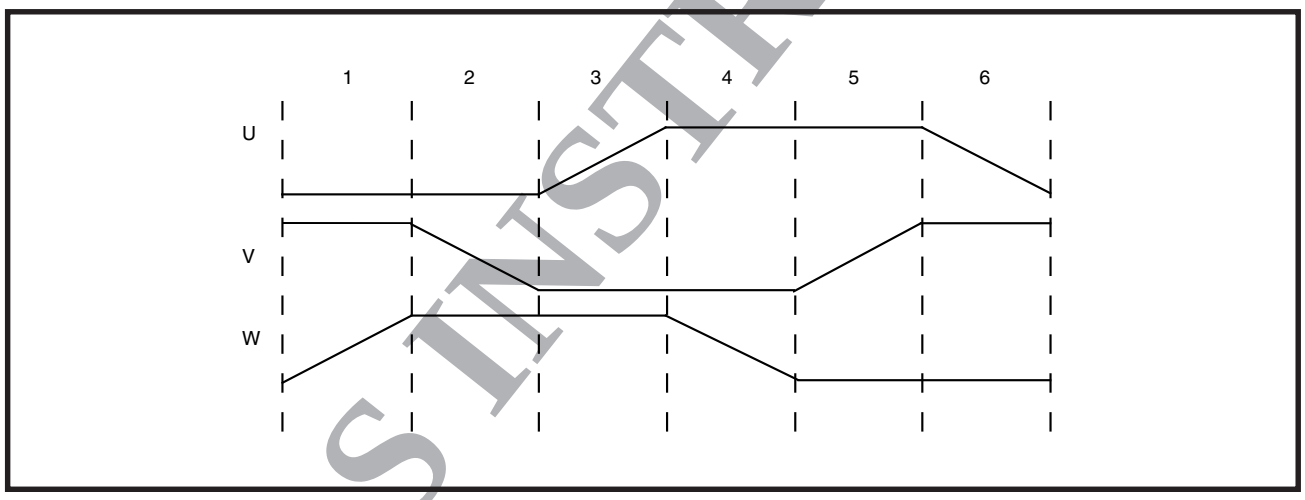


FIGURE 2-9: Commutation Graphical Form

TABLE 2–2: Commutation State Table

STATE	0 (PRESET)	1	2	3	4	5	6
UL	0	1	1	0	0	0	0
VL	0	0	0	1	1	0	0
WL	0	0	0	0	0	1	1
UH	0	0	0	0	1	1	0
VH	0	1	0	0	0	0	1
WH	0	0	1	1	0	0	0

SPINDLE MOTOR PREDRIVER (continued)

Slew-Rate Control

A resistor, attached to the RSLEW pin, controls the slew rate of the spindle motor driver power FETs by adjusting the amount of current which is applied to the gate. The RSLEW resistor establishes a reference current, I SLEW , as shown in Figure 2–10. This current is used by the high- and low-side driver circuits to determine the amount of current that will be applied to the power FETs gate.

The high-side driver circuitry, which is shown in Figure 2–11, provides two different levels of current for both charging and discharging the power FETs gate as illustrated in Figure 2–12. During the charging interval, switch S1 will be closed until the voltage at the power FETs gate, V_{GHS} , exceeds about 13 V, at which point it opens. During the interval when S1 is closed, the current applied to the gate can be calculated using equation 11. When S1 is open, the current applied to the gate is given by equation 12.

$$I_{CHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 31.5 \quad (11)$$

$$I_{CHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 2.6 \quad (12)$$

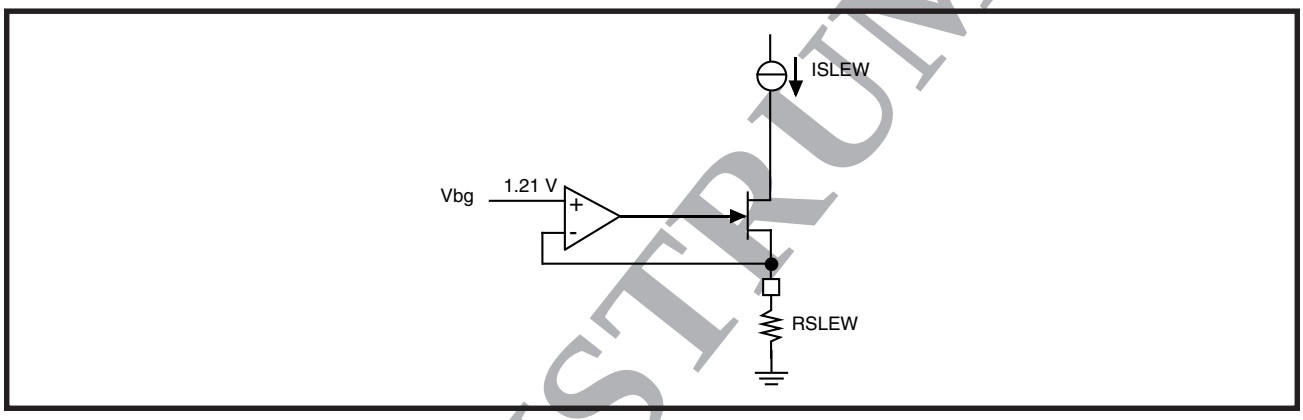


FIGURE 2-10: ISLEW Biasing Circuit

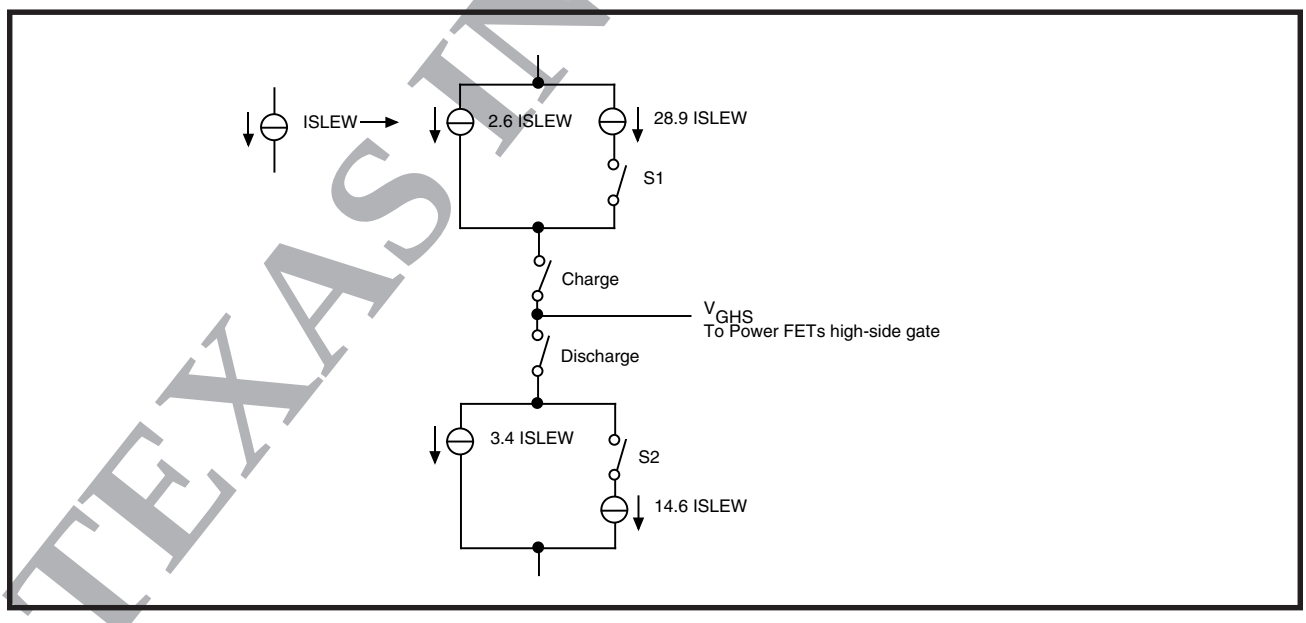


FIGURE 2-11: High-Side Driver Circuitry

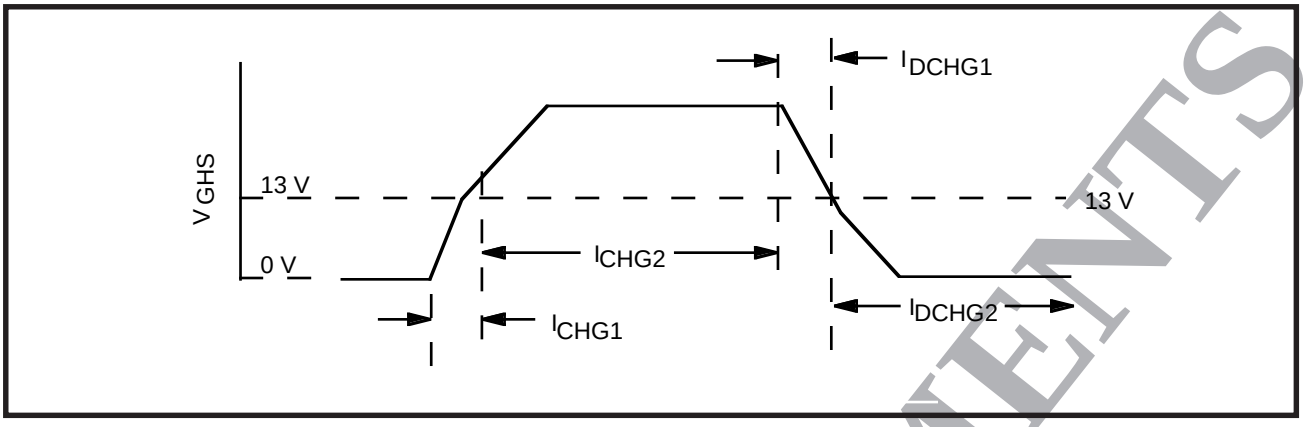


FIGURE 2-12: V_{GHS} During Charging and Discharging

Slew-Rate Control (continued)

During the discharging interval, switch S2 will be closed until V_{GHS} drops to below about 13 V at which point it will open. With S2 closed, the current applied to the gate is given by equation 13, and when S2 is open, the gate current is given by equation 14.

$$I_{DCHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 18 \quad (13)$$

$$I_{DCHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 3.4 \quad (14)$$

The low-side driver circuitry is shown in Figure 2–13. The charge current, I chg3 , is given by equation 15. During PWM switching of the low-side drivers, both S3 and S4 are open and the discharge current is given by equation 16. Switches S3 and S4 are used to control the discharge current during commutation switching of the low-side drivers. When V_{GLS} is greater than about 6 V, both S3 and S4 will be closed, and the current which is drawn from the gate is given by equation 17. As V_{GLS} drops below 6 V, switch S4 will open and the discharge current is given by equation 18.

$$I_{CHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 22.7 \quad (15)$$

$$I_{DCHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 24.3 \quad (16)$$

$$I_{DCHG4} = \left(\frac{1.21}{RSLEW}\right) \bullet 25 \quad (17)$$

$$I_{DCHG5} = \left(\frac{1.21}{RSLEW}\right) \bullet 8.5 \quad (18)$$

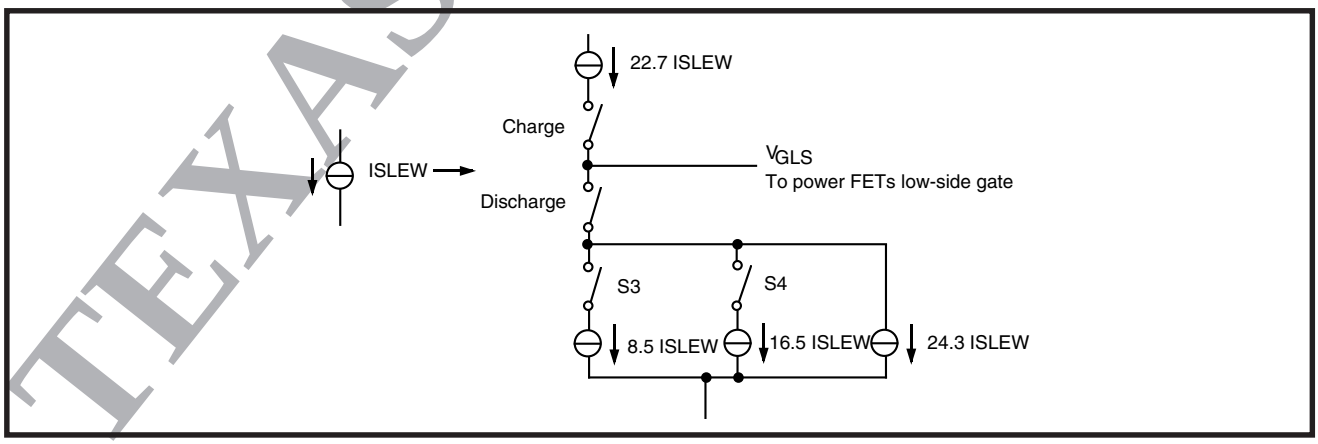


FIGURE 2-13: Low-Side Driver Circuitry

The application of these low-side currents for a single commutation interval is illustrated in Figure 2-14.

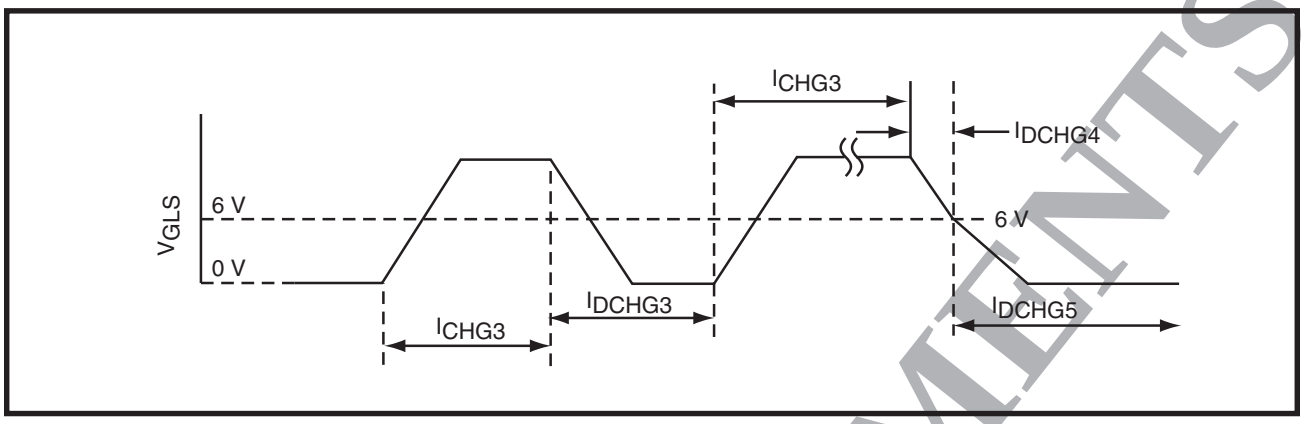


FIGURE 2-14: V_{GLS} for a Single Commutation Interval

NOTE: Adjusting RSLEW also affects the one-shot timing as described in the subsection Start/TACH.

DETAILED DESCRIPTION (continued)

SUPPORT FUNCTIONS

Miscellaneous support functions include:

- Voltage monitor
- Actuator-retract control
- Spindle motor brake control
- Voltage-reference buffer
- Charge pump

Voltage Monitor

When the 5 V supply is low or high or when the 12 V supply is low, the TLS2233 monitors supply-voltage status and generates fault indicators. Off-chip capacitors filter the supply voltages to ensure that momentary system spikes do not interrupt system operation. Internal resistor dividers set voltage levels, while off-chip resistors allow for adjustments in trip level. Responses to these voltage levels include retract, WENA, and FAULTN.

FAULTN and WENA indicate fault conditions on the 12 V (PV12) and 5 V (V5A) power lines (see Figure 2–15). Overvoltage on the 5 V line causes the output on FAULTN and WENA to rise until the overvoltage threshold is reached. At this time, WENA goes low. If either the 5 V or 12 V lines fall below their respective undervoltage threshold, both FAULTN and WENA go low. The retract function (see the Retract subsection) and subsequent delayed brake function (see the Brake subsection) are initiated by FAULTN going low.

A 5 V on-chip regulator powered from the voltage at V12 keeps selected functions such as retract, brake, and spindle commutation powered up and functioning during power brownouts. In case of a complete 5 V and 12 V power fault, the on-chip 5 V regulator supplies power (V5R) via the spindle's BEMF to complete actuator retract and spindle braking. To ensure that chip logic is functional during a 12 V fault with no BEMF, a forward-biased diode supplies 5 V (minus a V_f diode drop) from V5A to the V5R power bus as shown in Figure 2–16.

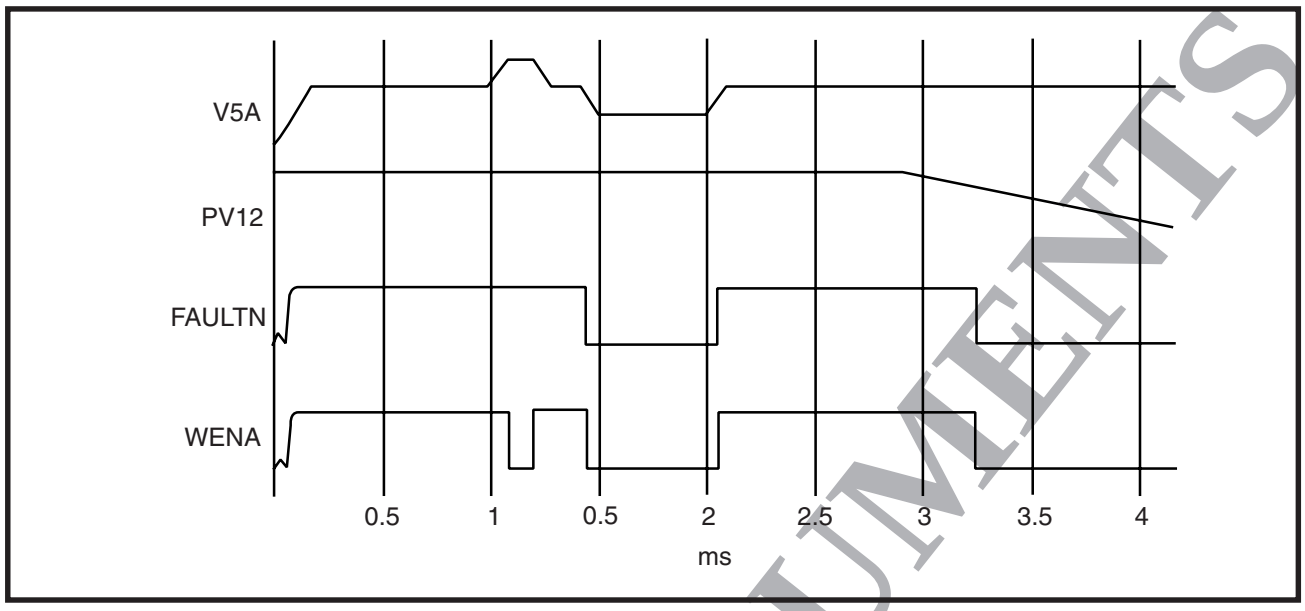


FIGURE 2-15: FAULTN and WENA Responses to Over 5 V, and 12 V Signal Decay

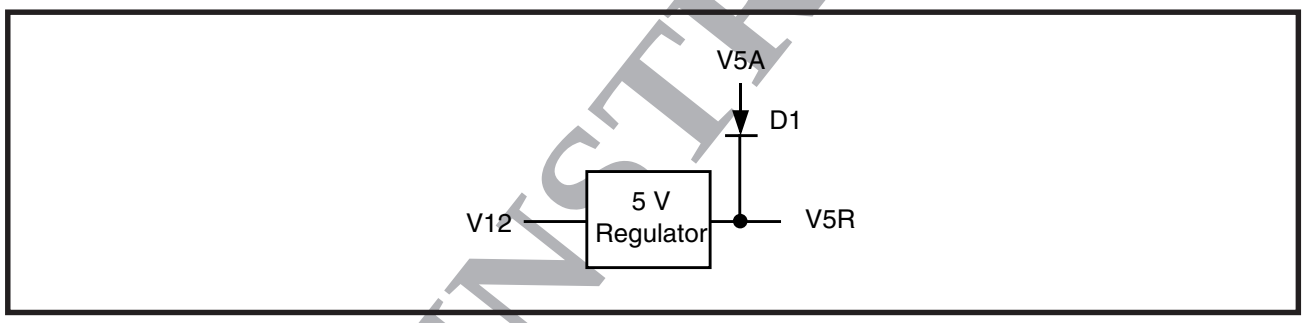
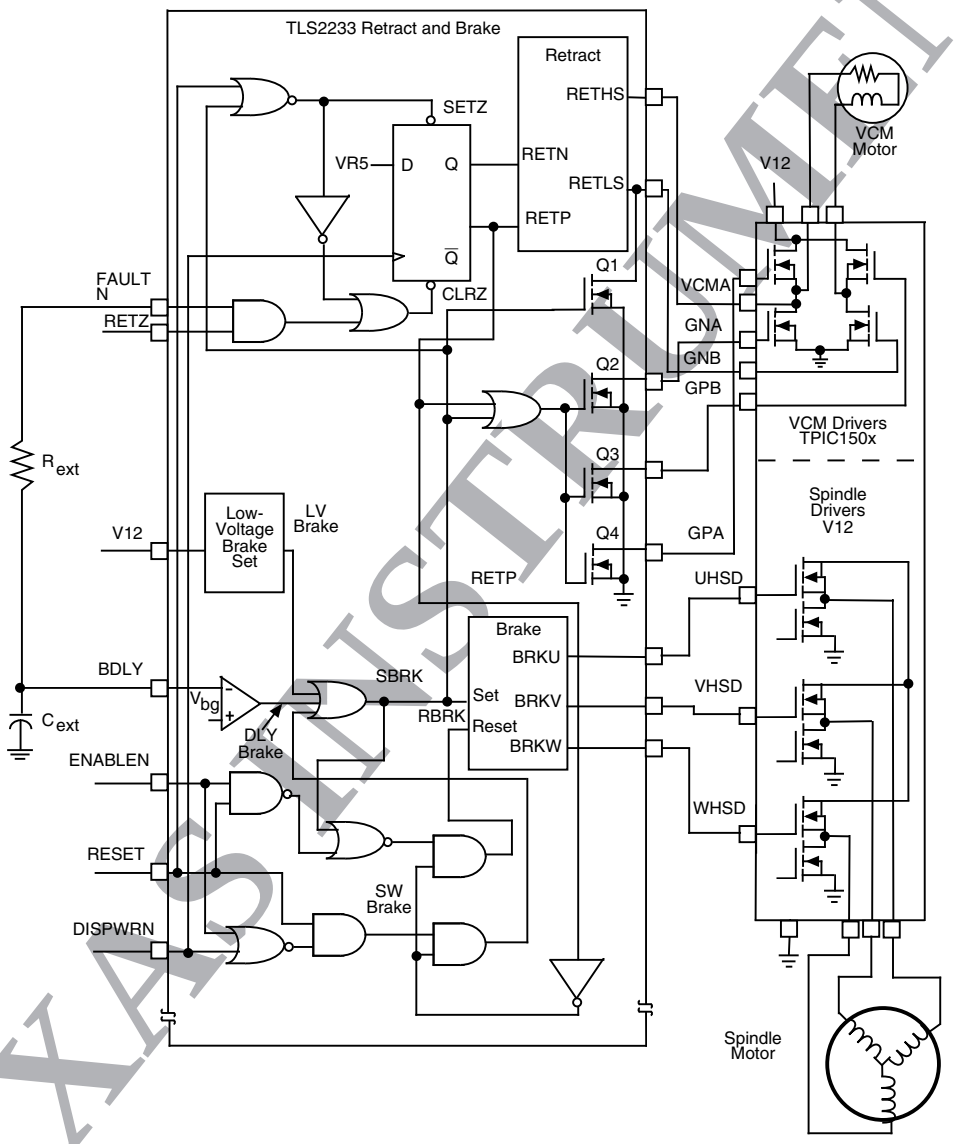


FIGURE 2-16: V5R Power Bus

SUPPORT FUNCTIONS (continued)

Retract

Figure 2–17 shows the retract- and brake-control logic. The actuator is immediately retracted on detection of a power fault. The retract voltage applied to the VCM continues until the delayed brake occurs. After a brownout condition where a power fault ends before a delayed brake occurs, a logical 1 must be applied to DISPWRN to reset or turn off the retract voltage (see Figure 2–18). A software brake is ignored during a retract.



NOTE: The GNA, GNB, ULSD, VLSD, and WLSD terminals can be connected to external 10 MΩ to 20 MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2233.

FIGURE 2-17: Retract- and Brake-Control Function Schematic Diagram

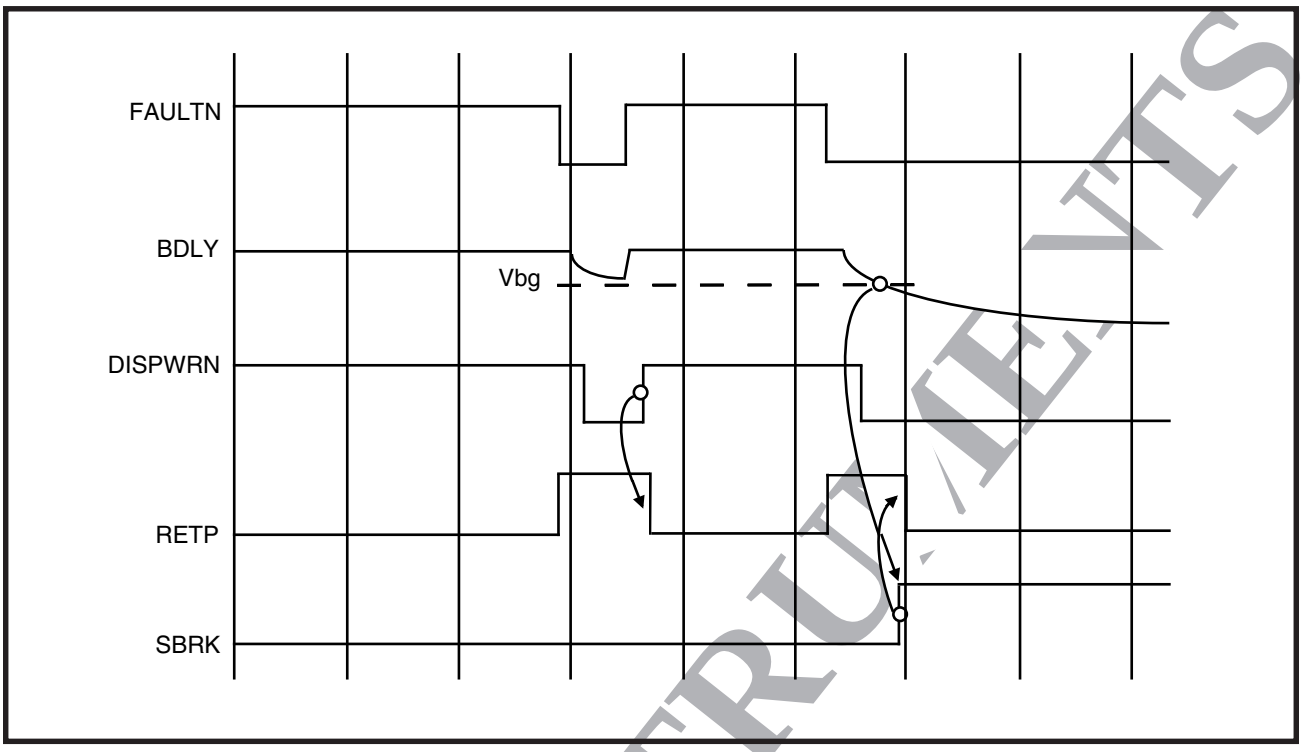


FIGURE 2-18: DISPWRZ, RETP, and SBRK Responses to FAULTN and BDLY

A power-fault retract causes the outputs to the VCM driver gates (GPA, GPB, and GNA), shown in Figure 2–17), to be pulled to ground. This ensures that the three driver transistors are powered off. The single low-side driver, tied to GNB, is turned on to return the actuator node to ground. Regulated retract voltage (1 V) is applied across the VCM at VCMA.

The retract function can also be initiated by applying a logic high at RETZ.

NOTE: The TLS2233 provides thermal protection for the retract circuitry. At approximately 150°C, the retract current is disabled. When the temperature drops below 140°C, the retract current is enabled.

Brake

The brake function turns on all spindle high-side drivers (UHSD, VHSD, and WHSD) and turns off all low-side drivers (see Figure 2–17).

Any braking function (delayed or software) causes all four actuator outputs (GPA, GPB, GNA, and GNB) to go low, ensuring that all VCM driver transistors are turned off. The current sources driving the outputs also are disabled. A software (SW) brake can be used to set the VCM current to zero for optional servo calibration.

Delay (DLY) brake time is set by an external resistor (R_{ext}) and capacitor (C_{ext}), as shown in Figure 2–17.

This value is calculated using equation 19.

$$\text{Brake delay time} = R_{ext} \bullet C_{ext} \bullet \text{Ln}\left(\frac{V5D}{V_{bg}}\right) \quad (19)$$

Where: V5D = 5 V
V_{bg} = 1.21 V
R_{ext} is in ohms
C_{ext} is in farads
Ln is natural log

Then: Brake delay time = $1.419 \bullet R_{ext} \bullet C_{ext}$

If a brake delay does not time out before the BEMF voltage (V12) reaches a low of about 2 V during a power fault, the low-voltage (LV) brake is automatic.

Brake (continued)

During a power-down event, energy from the spindle provides power to the VCM and retracts the heads to the landing zone. This operation employs both a current limit and a regulated voltage to ensure controlled motion. This current and voltage control is accomplished internally and is not adjustable.

NOTE: Preset-mode logic should be avoided when the spindle is running. If automatic braking (low V12 brake) occurs during a 12 V power fault and preset logic is applied, it is possible to lose charge-pump voltage and be unable to complete braking.

Voltage-Reference Buffer

An external 2 V reference (VREF) is buffered for on-chip use. A 4 V (VREF2) reference is generated from the 2 V buffer and is available as an output.

Charge Pump

The charge pump generates 25 volts to drive the TPIC150x high-side N-channel FETs. The charge pump requires only one external component, a storage capacitor. The recommended value for the storage capacitor is 1 μF.

PIN DESCRIPTION

TLS2233 TERMINAL FUNCTIONS

NAME	NO.	TYPE	I/O	DESCRIPTION
SUPPLIES				
AGND	14		Ground	Analog ground
CP	41	O	Analog	Charge-pump storage-capacitor connection
DGND	52		Ground	Digital ground
PV12	50	I	Analog	12-V power-supply monitor (sensed by voltage monitor to generate FAULTN)
VREF	43	I	Analog	Input reference voltage
VREF2	42	O	Analog	Output reference voltage (2 • VREF)
V5A	15		Power	5-V power supply (analog)
V5D	51		Power	5-V power supply (digital)
V12	36		Power	12-V power supply (isolated from PV12 with blocking diode)
VCM				
A3	33	O	Analog	Filter amplifier
A3P	34	I	Analog	Filter amplifier (noninverting)
ERR	32	O	Analog	VCM current-loop error amplifier
ERRN	35	I	Analog	VCM current-loop error amplifier (inverting)
GLS	24	O	Analog	Driver-sense gate
GNA	29	O	Analog	A low-side driver gate
GNB	26	O	Analog	B low-side driver gate
GPA	30	O	Analog	A high-side driver gate
GPB	28	O	Analog	B high-side driver gate
ISET	25	O	Analog	Driver-sense drain (bias current for class AB operation)
RSEN	23	I	Analog	VCM current-sense feedback. Connects internally to the inverting input of the current-sense differential amplifier.
RETZ	5	I	Digital	Commands VCM retract (active low)
SOUT	22	O	Analog	VCM current-sense amplifier feedback
SPWMAI	39	I	Digital	PWM input
SPWMAO	38	O	Digital	Inverted PWM output from SPWMAI
SPWMBI	40	I	Digital	PWM input
SPWMBO	37	O	Digital	Inverted PWM output from SWPWMBI
VCMA	31	I/O	Analog	VCM current-sense resistor. Connects internally to the noninverting input of the current-sense differential amplifier and externally to the driver side of the sense resistor. Retract voltage output.
VCMB	27	I	Analog	VCM input. Connects externally between the drivers and the VCM.

TLS2233 TERMINAL FUNCTIONS (continued)

NAME	NO.	TYPE	I/O	DESCRIPTION
SPINDLE MOTOR				
ADVANCE	13	I	Digital	Commutation-state-machine advance (used for spindle start)
COS	6	O	Analog	Capacitor for one-shot timing
CVCO	21	O	Analog	Capacitor to set VCO speed range for motor commutation
DISPWRN	10	I	Digital	Disable-power (active low) mode control (low level disables spindle power)
ENABLEN	12	I	Digital	Mode control (active low)
K_GND	3	O	Analog	Kelvin ground sense for RSENSE resistor
PEFILTER	20	O	Analog	Phase-error filter for commutation PLL
PU	18	I	Analog	Phase U back EMF sense
PV	17	I	Analog	Phase V back EMF sense
PW	16	I	Analog	Phase W back EMF sense
PWMIN	4	I	Digital	PWM input for low-side driver (used during PWM-start and PWM-run modes)
RESET	11	I	Digital	Mode control (active high). Resets VCO and state machine.
RSENSE	8	I	Analog	Spindle current-sense voltage feedback (high side of RSENSE)
RSLEW	9	O	Analog	Current-setting control for spindle-motor drive slew rates and one-shot timing used in the constant off-time spindle-motor-current regulator
SENSE/VCO/ TACH	19	O	Digital	MUX out: Current threshold SENSE during start mode. VCO during preset TACH mode or run mode. TACH during coast mode.
TH_SENSE	7	I	Analog	Current-sense comparator
UHSD	55	O	Analog	U high-side driver gate
ULSD	2	O	Analog	U low-side driver gate
VHSD	54	O	Analog	V high-side driver gate
VLSD	1	O	Analog	V low-side driver gate
WHSD	53	O	Analog	W high-side driver gate
WLSD	56	O	Analog	W low-side driver gate
VOLTAGE MONITOR (VM)				
BDLY	44	I	Analog	Brake delay
FAULTN	46	O	Digital	Fault (active low)
VCKWI	49	O	Analog	High 5-V voltage-monitor filter/threshold set
VCK5	47	O	Analog	Low 5-V voltage-monitor filter/threshold set
VCK12	48	O	Analog	Low 12-V voltage-monitor filter/threshold set
WENA	45	O	Digital	Write enable (active high). Low on overvoltage or fault.

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE
(unless otherwise noted) †

PARAMETER	RATING
Supply voltage, V12, PV12 (see Note 1)	15 V
Supply voltage, V5D, V5A (see Note 1)	7 V
Charge-pump output voltage	30 V
Power dissipation, T A = 70°C	1 W
Operating virtual junction temperature, T J	≤ 150°C
Storage temperature range, T stg	–55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS OVER RECOMMENDED SUPPLY VOLTAGE, T_A = 25°C

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply voltage V5A, V5D		VCK5 = 5 V	4.5	5	5.5	V
Supply voltage PV12			10.8	12	13.8	V
Supply voltage V12			10.1	11.7	13.8	V
High-level input voltage	V_{IH}		3.5		V5D+0.3	V
Low-level input voltage	V_{IL}		–0.3		0.5	V

ELECTRICAL CHARACTERISTICS

TOTAL DEVICE OVER RECOMMENDED SUPPLY VOLTAGE, T_A = 25°C (See NOTE 2)

High-level output voltage	V_{OH}	I_O = 20 µA	V5D – 0.1 V			V
Low-level output voltage	V_{OL}	I_O = – 20 µA			0.1	V
Supply current	I_{DD}					
	I_{PV12}				520	µA
	I_{V12}				16	mA
	I_{V5A}				6.8	mA
	I_{V5D}				3	mA
High-level input current	I_{IH}				50	µA
Low-level input current	I_{IL}				–1	µA

NOTE 2: There are internal 120 kΩ pulldown resistors for RESET, ENABLEN, DISPWRN, and ADVANCE.

VOLTAGE MONITOR, V5D = 5 V ±10%, T_A = 25°C (SEE NOTE 3)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage FAULTN,WENA	V_{OH}	V5D = 5 V, I_{OH} = 50 µA	3.5	4		V
Low-level output voltage FAULTN	V_{OL}	V5D = 5 V, I_{OL} = 6 mA		0.3	0.5	V
Low-level output voltage WENA	V_{OL}	V5D = 5 V, I_{OL} = 100 µA		0.3	0.5	V
Falling 12-V voltage FAULTN	PV12_F		9.3	9.83	10.36	V
Rising 12-V voltage FAULTN	PV12_R		9.36	9.95	10.42	V
Falling 5-V voltage FAULTN	V5A_F		4.42	4.52	4.6	V
Falling 5-V voltage WENA	V5A_F		5.58	5.88	6.25	V
Rising 5-V voltage FAULTN	V5A_R		4.47	4.56	4.65	V
Rising 5-V voltage WENA	V5A_R		5.64	5.97	6.28	V
Hysteresis 5-V voltage FAULTN	V_{hys}		30	48	70	mV
Hysteresis 5-V voltage WENA	V_{hys}		30	81	130	mV
Hysteresis 12-V voltage FAULTN	V_{hys}		60	109	150	mV
Short-circuit output current WENA, FAULTN	I_{OS}				0.4	mA
Low-level output current BDLY, FAULTN	I_{OL}				6	mA
Low level output current WENA	I_{OL}				500	µA

NOTE 3: As the power goes up and/or down, comparators and band-gap voltage are available at 3 V (goal 2.5 V), which allows proper driver disabling through the power-up process.

ELECTRICAL CHARACTERISTICS (continued)

FAULTN AND WRITE MINIMUM SUPPLY THRESHOLD (SEE NOTE 4)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V5 (rising from 0)	FAULTN	Loads (FAULTN = 640 Ω WENA = 15 kΩ)		0.92	1.5	V
	WENA	Loads (FAULTN = 640 Ω WENA = 15 kΩ)		1	1.5	V
V12 (set at 0)	FAULTN	Loads (FAULTN = 640 Ω, WENA = 15 kΩ)		0	0	V
	WENA	Loads (FAULTN = 640 Ω, WENA = 15 kΩ)		0	0	V
V5 (set at 0)	FAULTN	Loads (FAULTN 1 6 kΩ WENA = 40 kΩ)		0	0	V
	WENA	Loads (FAULTN 1 6 kΩ WENA = 40 kΩ)		0	0	V
V12 (rising from 0)	FAULTN	Loads (FAULTN 1 6 kΩ WENA = 40 kΩ)		2.52	3	V
	WENA	Loads (FAULTN 1 6 kΩ WENA = 40 kΩ)		2.9	3.5	V
V5 (set at 5 V)	FAULTN	Loads (FAULTN 640 Ω WENA = 15 kΩ)		5	5	V
	WENA	Loads (FAULTN 640 Ω WENA = 15 kΩ)		5	5	V
V12 (rising from 0)	FAULTN	Loads (FAULTN = 640 Ω WENA = 15 kΩ)		0	0	V
	WENA	Loads (FAULTN 640 Ω WENA = 15 kΩ)		0	0	V
V5 (rising from 0)	FAULTN	Loads (FAULTN = 640 Ω WENA = 15 kΩ)		0	0	V
	WENA	Loads (FAULTN 640 Ω WENA = 15 kΩ)		0	0	V
V12 (set at 12 V)	FAULTN	Loads (FAULTN = 640 Ω WENA = 15 kΩ)		12	12	V
	WENA	Loads (FAULTN 640 Ω WENA = 15 kΩ)		12	12	V

NOTE 4: Typical and maximum values indicate where a valid FAULTN/WENA occurs.

ELECTRICAL CHARACTERISTICS (continued)

RETRACT (SEE NOTE 5)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Voltage at VCMA	Sourcing 40 mA	0.8	1	1.2	V
Voltage on GPA, GPB, GNA				0.7	V
Voltage on GNB		10			V
Retract current limit	VCMA to GND	0.15		0.25	A

NOTE 5: Retract = 0.5 V if temperature exceeds 150°C

BRAKING CIRCUIT

Voltage on VLSD off	Functional test			0.7	V
Voltage on VHSD high	Functional test	20			V
Brake-threshold voltage, BDLY	T_A = 25°C	1	1.4	1.6	V
Back EMF voltage to regulate brake	V5A = V5D = 0		4		V
Low-voltage brake	V5A = V5D = 0		2		V
Leakage current, BDLY I_{lkg}	$V_{I(BDLY)}$ = 5 V			200	nA

CHARGE PUMP (see NOTE 6)

Charge-pump output voltage	V12 = 12 V, V5D = 5 V	20	25	26.7	V
Charge-pump output-voltage load regulation	See Note 7		0.015	0.025	V/µA
VCO frequency			4		MHz
Charge time			0.5		s

NOTES 6. External storage capacitor is typically 1 µF.
7. The output can drive external N-channel DMOS switches; the external dc leakage should be less than 1 µA.

VOLTAGE REFERENCE

Reference voltage (input at VREF pin) V_{ref}		2		2.4	V
VREF2 gain (see Note 8) G		1.9	2	2.1	V/ V
VREF2 source/sink current I_O			±100		µA

NOTE 8: Gain includes offsets

PWM PULSE-SAMPLING INVERTERS

High-level output voltage V_{OH}	10 kΩ to VREF2	3.9	4	4.1	V
Low-level output voltage V_{OL}	10 kΩ to VREF2	0	0	0.3	V

VCM INPUT-FILTER AMPLIFIER

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Common-mode input voltage with respect to VREF	V_{IC}			±2		V
Input offset voltage	V_{IO}		–10		10	mV
Average temperature coefficient of input offset voltage	V_{IO}			15		µV/C
Output swing with respect to VREF	$V_{O(PP)}$	R_L = 10 kΩ (tied to V_{ref} level)	1.5		– 1.5	V
Open-loop voltage gain		f = 1 kHz, R_L = 10 kΩ		60		dB
Common-mode rejection ratio	CMRR	V_{CMRR} = ± 1.5 V		60		dB
Gain (see Note 9)	G			2		V/V
Gain bandwidth product	GBW			1		MHz
Input bias current	I_{IB}				1	µA
Supply voltage rejection ratio †	k_{SVR}	f = 100 kHz, R_L = 10 kΩ C_L < 60 pF		70		dB
Slew rate	SR	R_L = 10 kΩ,C_L = 60 pF		1		V/µs

NOTE 9: Filter gain set internal to device
† These parameters are not tested. They are determined by design characterization.

VCM CURRENT-LOOP-ERROR AMPLIFIER

Common-mode input voltage, REF	V_{IC}			±2		V
Input offset voltage	V_{IO}		–10		10	mV
Average temperature coefficient of input offset voltage	V_{IO}			15		µV/C
Output swing with respect to VREF	$V_{O(PP)}$	R_L = 10 kΩ (tied to VREF level)	1.5		–1.5	V
Open-loop voltage gain †		f = 1 kHz, R_L = 10 kΩ	50	70		dB
Gain bandwidth product	GBW			1		MHz
Input bias current	I_{IB}			0	1	µA
Supply voltage rejection ratio	k_{SVR}	f = 100 kHz, R_L = 10 kΩ C_L < 60 pF		70		dB
Slew rate	SR	R_L = 10 kΩ C_L = 60 pF to VREF		1		V/µs

† These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS (continued)

VCM CURRENT-SENSE AMPLIFIER

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Common-mode input voltage	V_{IC}		0		12	V
Input offset voltage	V_{IO}	Measured at SOUT with respect to V_{REF} (RSEN tied to VCMA)	–4	0	4	mV
Output swing	$V_{O(PP)}$	R_L = 10 kΩ (tied to V_{ref} level)	1.5		–1.5	V
Open-loop voltage gain		f = 1 kHz, R_L = 10 kΩ		66		dB
Common-mode rejection ratio	CMRR	V_{CMRR} = 0.5 V to 11.5 V	54	70		dB
Gain	G		2.67	2.73	2.79	V/V
Gain bandwidth product †	GBW		0.5	1		MHz
Slew rate	SR	R_L = 10 kΩ,C_L = 60 pF		1		V/µs
Supply voltage rejection ratio †	k_{SVR}	f = 100 kHz, R_L = 10 kΩ C_L < 60 pF		70		dB

† These parameters are not tested. They are determined by design characterization.

VCM PREDRIVER AMPLIFIER

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage GPA, GPB	V_{OH}	R_L = 6 MΩ	20			V
High-level output voltage GNA, GNB	V_{OH}	R_L = 6 MΩ	V12–2			V
Low-level output voltage GPA, GPB	V_{OL}				1.2	V
Low-level output voltage GNA, GNB	V_{OL}				1.2	V
Quiescent current		See Note 10		2		mA
Unity-gain bandwidth				1		MHz
Common-mode rejection ratio †	CMRR		60			dB
Gain	G	VCMA to VCMB		12		V/V
Slew rate positive, GPA, GPB	SR+	C_L = 50 pF, See Note 11		0.5		V/µs
Slew rate positive GNA, GNB	SR+	C_L = 50 pF, See Note 12		0.5		V/µs
Slew rate negative, GPA, GPB	SR–	C_L = 50 pF, See Note 13		2		V/µs
Slew rate negative GNA, GNB	SR–	C_L = 50 pF, See Note 13		2		V/µs
Power-supply rejection ratio †	PSRR		60			dB
ISET output current	I_o		–25		–65	µA
GLS voltage	V_{opp-}		60		100	mV
GLS voltage	V_{opp+}		3.5			V

NOTES: 10. This provides less than 0.5% current harmonic distortion at 1 kHz with V_I = 20 mVp-p. Maximum and minimum are not specified until the device is characterized.
11. Slew rate measured as average positive slew rate from 1 V to 19 V
12. Slew rate measured as average positive slew rate from 1 V to 10 V
13. Slew rate measured as average negative slew rate from 18 V to 1 V

† These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS (continued)

VCO (CVCO = 0.0068 MF) *(unless otherwise specified)*

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage (100 μA) SENSE/VCO/TACH	V_{OH}		V5D – 0.1			V
Low-level output voltage (-100 μA) SENSE/VCO/TACH	V_{OL}				0.1	V
Frequency, idle	f	Mode = Preset	80	100	120	Hz
Frequency, run	f	$V_{O(PEFILTER)}$ = 2.16 V	1728	2160	2592	Hz
Frequency, typical	f		$\frac{V_{O(PEFILTER)}}{122,000 \bullet CVCO}$			Hz
Reset phase error		$V_{O(PEFILTER)}$ = Vidle = 0.1 V			36	degrees C

PHASE-ERROR AMPLIFIER

Output voltage (V_{idle})	V_O	Mode = Preset		100		mV
Maximum voltage PU, PV, and PW					15	V
Input offset voltage, state F PU (see Note 14)	V_{IO}	PW = Vsupply, PV = 0	–180		180	mV
Input offset voltage, state C PU (see Note 14)	V_{IO}	PV = Vsupply, PW = 0	–180		180	mV
Input offset voltage, state A PV (see Note 14)	V_{IO}	PW = Vsupply, PU = 0	–180		180	mV
Input offset voltage, state D PV (see Note 14)	V_{IO}	PU = Vsupply, PW = 0	–180		180	mV
Input offset voltage, state B PW (see Note 14)	V_{IO}	PV = Vsupply, PU = 0	–180		180	mV
Input offset voltage, state E PW (see Note 14)	V_{IO}	PU = Vsupply, PV = 0	–180		180	mV
Output current at PEFILTER, reset mode	I_O	$V_{O(PEFILTER)}$ = V_{idle} = 0.1 V		150		μA
Output current at PEFILTER, run/idle mode	I_O	$V_{O(PEFILTER)}$ = 2 V		120		μA
Source/sink current mismatch		$V_{O(PEFILTER)}$ = 2 V	–7		7	%

NOTE: 14. Add 100 Ω resistance in series with PU, PV, and PW to prevent high reverse (below ground) current during start.

SPINDLE-PREDRIVER AMPLIFIER

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage UHSD, VHSD, WHSD	V_{OH}	R_L =6 MΩ	22			V
Low-level output voltage UHSD, VHSD, WHSD	V_{OL}				0.7	V
High-level output voltage ULSD, VLSD, WLSD	V_{OH}	R_L =6 MΩ	V12–2			V
Low-level output voltage ULSD, VLSD, WLSD	V_{OL}				0.7	V

CURRENT-SENSE COMPARATOR (TH_SENSE)

Common-mode input voltage	V_{IC}		0		2	V
Input offset voltage	V_{IO}		–10		10	mV

TACH COMPARATOR

Hysteresis	V_{hys}			280		mV
Input offset voltage †	V_{IO}		–42		42	mV

† Measured at PV and PW terminals.

MOTOR CURRENT CONTROL

I_COS_CHG			100		µA
I_COS_DCHG			3.7		mA
One shot	Ramp RSENSE up from 50 mV	95		115	mV
One-shot off time	C_{OS} = 0.001 µF R_{SLEW} = 12.1 kΩ	15	25	35	µs

MECHANICAL DATA

Figure 4-1 shows mechanical outline dimensions.

DL (R-PDSO-G56) **PLASTIC SMALL OUTLINE PACKAGE**

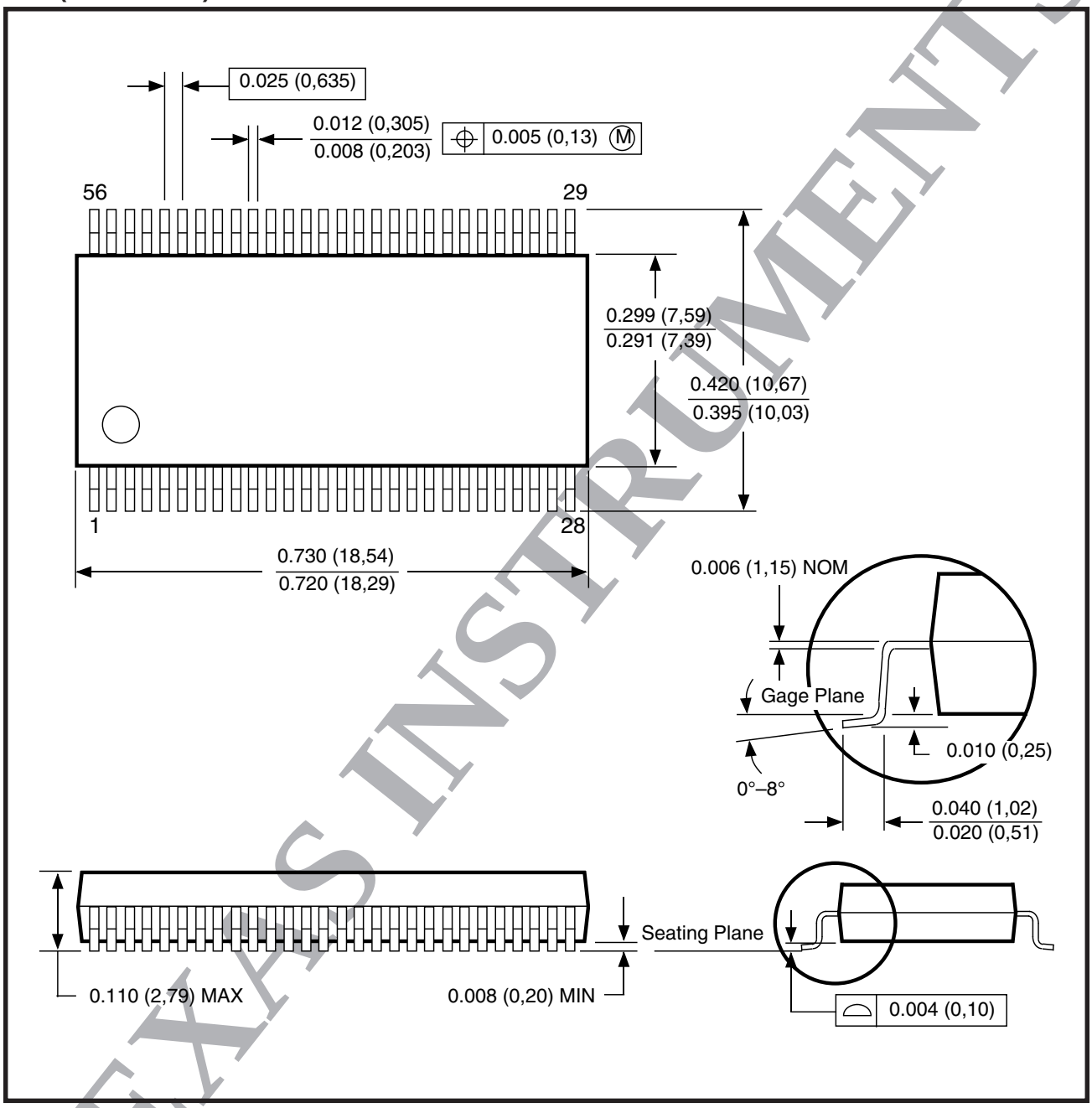


FIGURE 4-1: Mechanical Data

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

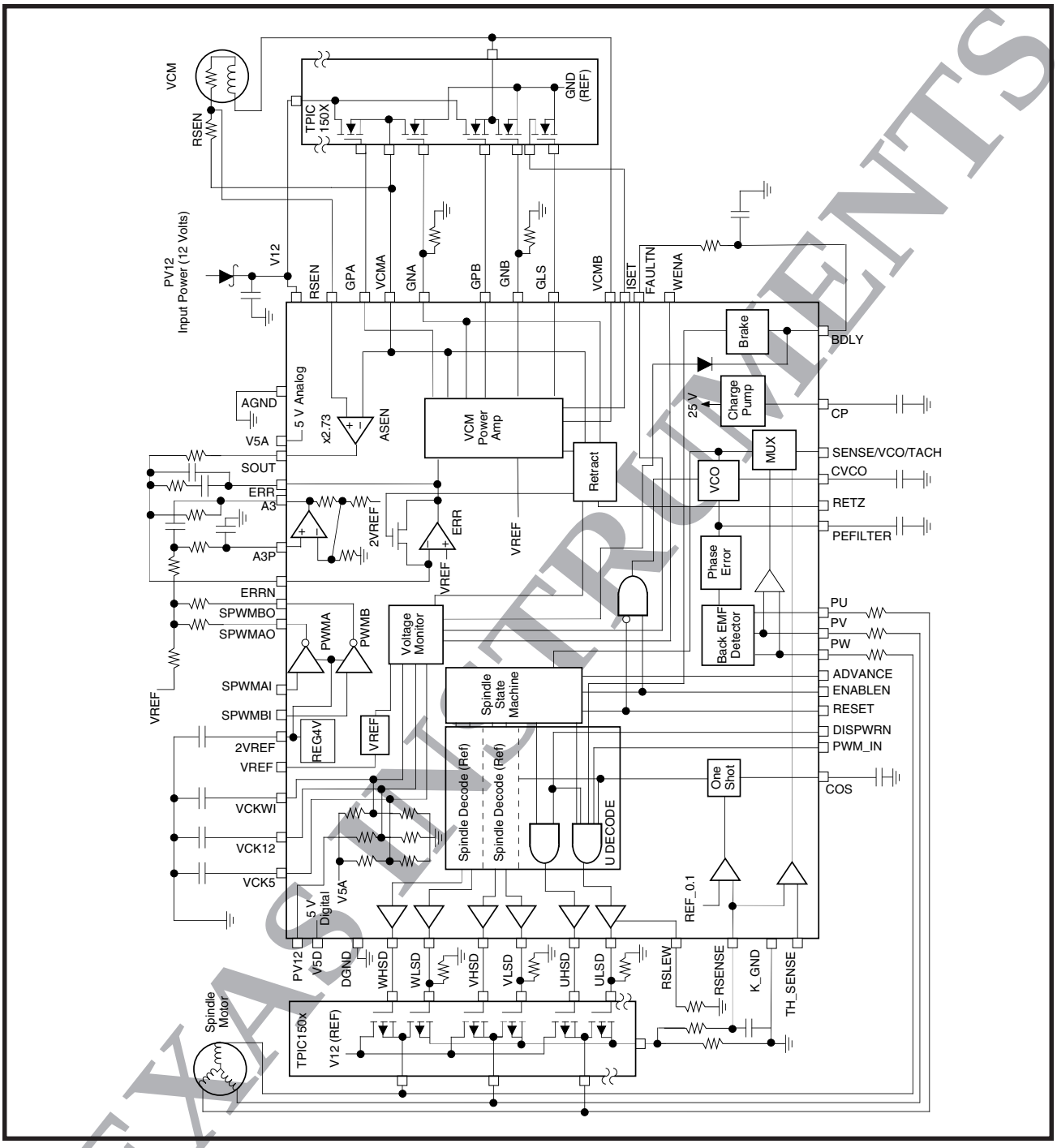
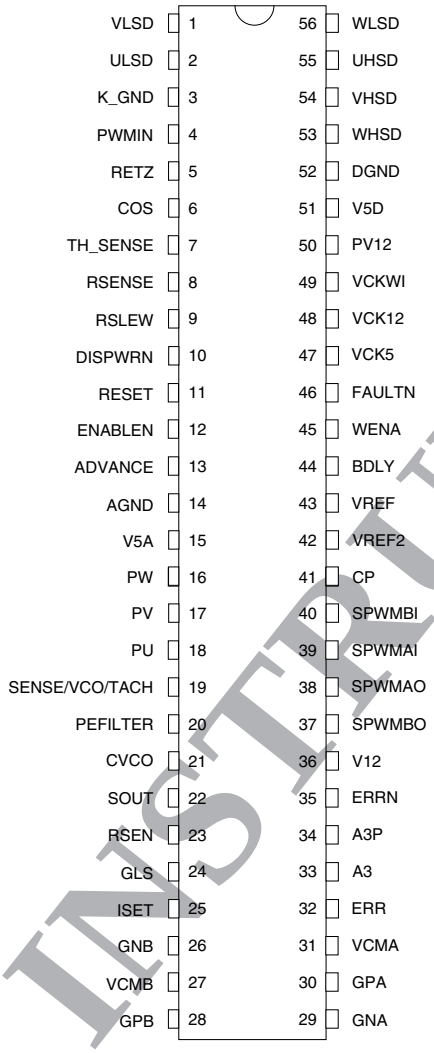


FIGURE 4-1: Typical Application

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



TLS2233
DL Package

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TI TLS2233 56-Pin Servo-Combination Predriver	**TLS2233CDLR**	**T2233CB**

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

TLS2234
Servo-Combination Predriver

August 1998

DESCRIPTION

The TLS2234 (Figure 1-1) is a servo-combination predriver designed for use in hard disk drive applications. The predriver, when used in combination with the TPIC150x, can drive a voice-coil motor (VCM) and a spindle motor.

FEATURES

VOICE-COIL MOTOR (VCM) PREDRIVER

- **Linear input control**
- **Transconductance amplifier with class AB output (when used with TPIC150x drivers)**
- **Summing amplifier**
- **Current-sense amplifier**
- **Retract function on power loss or on software command**
- **External set for retract voltage**

SPINDLE MOTOR PREDRIVER

- **Pulse-width modulated (PWM) start and PWM current limit**
- **Advance terminal signals commutation timing to on-chip sequencer during start mode**
- **Current-sense comparator**
- **Low-noise phase-locked loop performs commutation timing during run mode**
- **PWM or linear run**
- **Low-side driver transconductance amplifier for linear run mode**
- **Dynamic brake**
- **Power-down brake after delay**
- **Soft switching or limited dV/dT reduces acoustic noise in linear current control mode**
- **KELVIN_SENSE input to reduce current-sense errors induced by ground level variances**

SUPPORT FUNCTIONS

- **Voltage monitor (based on 5 V and 12 V supplies)**
- **Charge pump (24 V) for driving N-channel DMOS H-bridge drivers**

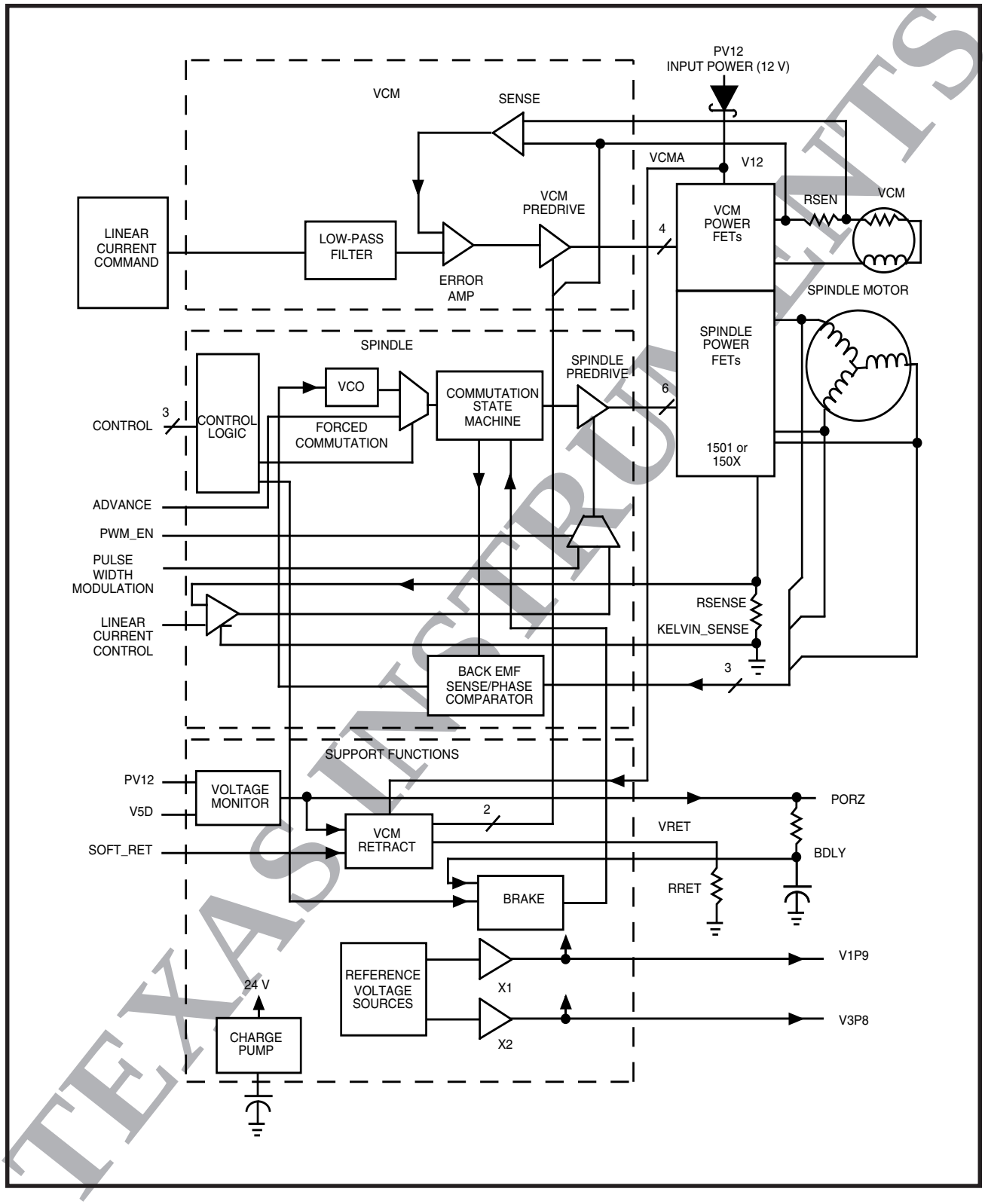


FIGURE 1-1: Functional Block Diagram

FUNCTIONAL DESCRIPTION

VCM DRIVE

The TLS2234 uses a linear voltage to control the current applied to the VCM. An input amplifier is provided for convenient filtering of the input voltage command. The bandwidth of the low-pass filter is determined by external components. The error amplifier implements a transconductance loop. The error amplifier output represents the difference between the command current and the actual current. The actual current is measured across the RSEN resistor by the sense amplifier. The compensated output of the error amplifier is applied to the VCM predrive circuit that biases the VCM power field-effect transistors (FETs) of the TPIC150x.

SPINDLE MOTOR DRIVE

The spindle motor is started under PWM control using an external signal for forced commutation. As the motor approaches operational speed, the commutation state machine is driven by the output of the voltage-controlled oscillator (VCO). The VCO utilizes the back EMF (BEMF) of the motor to close a phase-locked loop that matches the commutation frequency to the motor. Once in the run mode, the motor speed can be controlled using either a PWM signal to modulate the current applied to the motor or by a linear current command that acts as the input to the spindle transconductance loop.

SUPPORT FUNCTIONS

The TLS2234 support functions include a voltage monitor that indicates a fault when power supply voltages drop below a specified threshold. When triggered, the fault signal initiates a VCM retract and can also initiate delayed braking of the spindle motor. The VCM retract voltage is set by the selection of an external resistor. Other support functions include the on-chip reference voltage and the charge pump. The reference voltages are used internally and are also available for external use. The charge pump generates 24 V for driving the N-channel DMOS H-bridge drivers of the TPIC150x.

DETAILED DESCRIPTION

VOICE-COIL MOTOR PREDRIVER

The TLS2234, when combined with a power driver such as the TPIC150x, provides current drive capability for a VCM. Figure 2-1 shows the functional block diagram of a typical application. A signal applied to the input filter amplifier, A3, as shown indicates the level of current to be delivered to the VCM. This signal is low-pass filtered by amplifier A3 and applied to the error amplifier ERR.

The error amplifier implements a transconductance loop. Its output is the difference between the commanded current and the actual current as measured across RSEN by the differential amplifier ASEN. This error signal is applied to the predriver amplifier that biases the power FETs of the TPIC150x for class AB operation.

NOTE: The GNA and GNB terminals can be connected to external 10 MΩ to 20 MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2234.

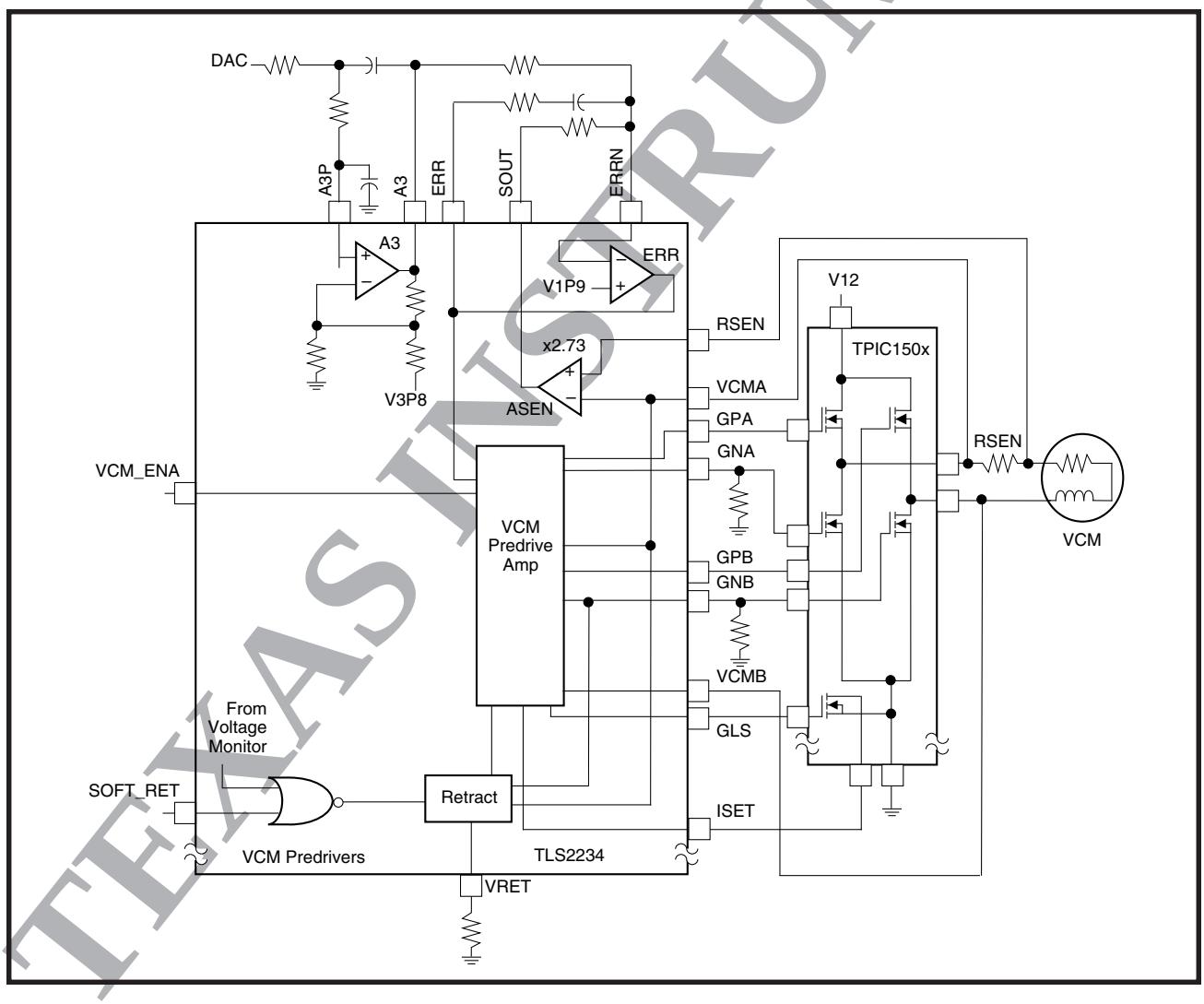


FIGURE 2-1: Voice-Coil Motor Functional Block Diagram

Input Filter Amplifier (A3)

The input filter amplifier (A3) filters the applied input. This amplifier can be used to implement a Sallen and Key filter as shown in Figure 2-2.

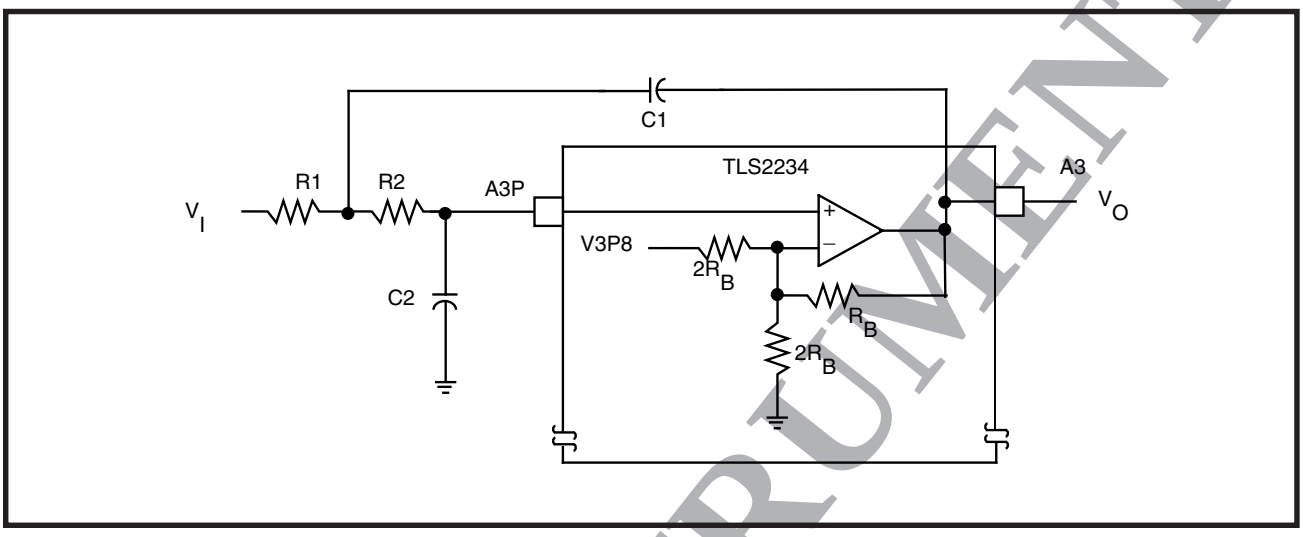


FIGURE 2-2: Sallen and Key Low-Pass Filter Implementation

Equations 1, 2, 3, and 4 show the transfer function of this circuit.

$$H(S) = \frac{K\omega^2}{S^2 + \frac{\omega}{Q}S + \omega^2} \quad (1)$$

$$K = 1 + \frac{R_B}{2R_B \| 2R_B} = 2;\ R_B \text{ matched internal components} \quad (2)$$

$$Q = \frac{1}{3 - K} = 1 \quad (3)$$

$$\omega = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \quad (4)$$

R1, R2, C1, and C2 are chosen to match ω to the applied input signal.

VOICE-COIL MOTOR PREDRIVER (continued)

Summing Amplifier (ERR)

The summing amplifier (ERR) generates an error signal that is proportional to the difference between the command current and the actual current. The selection of the external components provides compensation for the transconductance loop (see Figure 2-3).

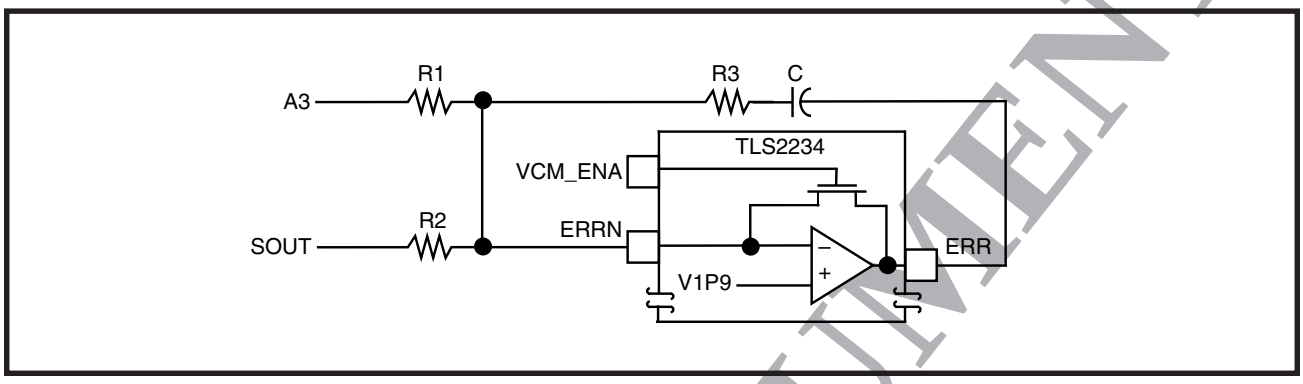


FIGURE 2-3: Summing Amplifier Implementation

Equation 5 shows the transfer function of this circuit.

$$H(S) = \frac{(R3\ C)S + 1}{(R2\ C)S} \quad (5)$$

Selecting values for R1, R2, and RSEN sets the VCM transconductance gain (Gm) (see equation 6).

$$Gm = \frac{IVCM}{VCMD} = \frac{R2}{2.73 \bullet R1 \bullet RSEN} \quad (6)$$

Current-Sense Amplifier (ASEN)

The current-sense amplifier (ASEN) (see Figure 2-4) provides a measure of the current being delivered to the motor by measuring the voltage across the sense resistor. The gain of this amplifier is fixed at 2.73. The offset can be calibrated by setting VCM_ENA low, along with SOFT_RET, to ensure that the VCM outputs are turned off and no current is being delivered to the VCM. In this state SOUT should be equal to V1P9.

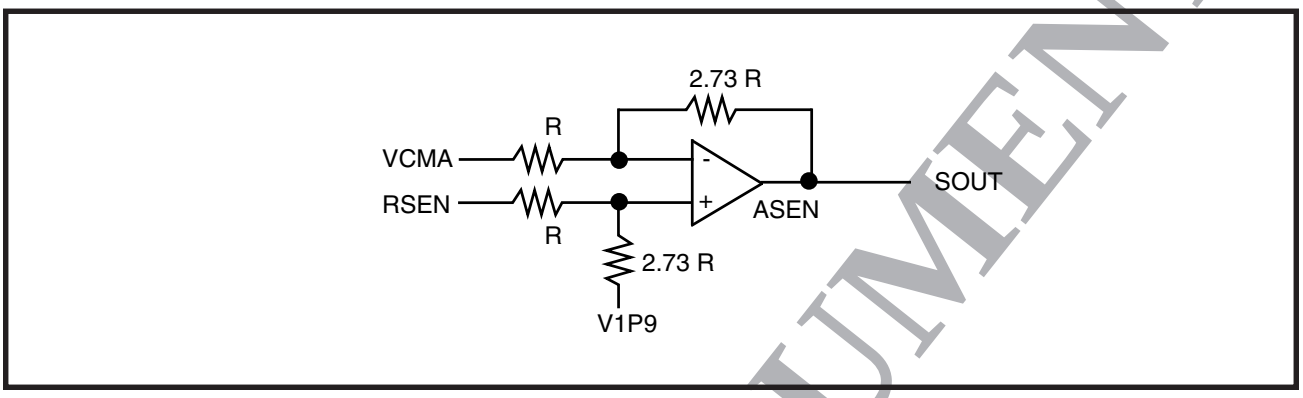
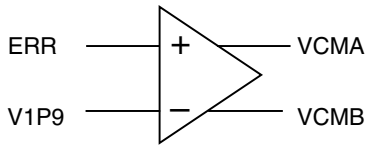


FIGURE 2-4: Current-Sense Amplifier Implementation

VCM Predriver Amplifier

The VCM predriver amplifier biases and operates the power FETs of the TPIC150x as a class AB amplifier with a gain of 12. Equation 7 shows this relationship.

$$\frac{VCMA - VCMB}{ERR - V1P9} = 12 \qquad (7)$$



NOTE: Setting VCM_ENA to logic low when SOFT_RET is equal to logic low disables the VCM output. Setting SOFT_RET to high disables the VCM and causes a retract.

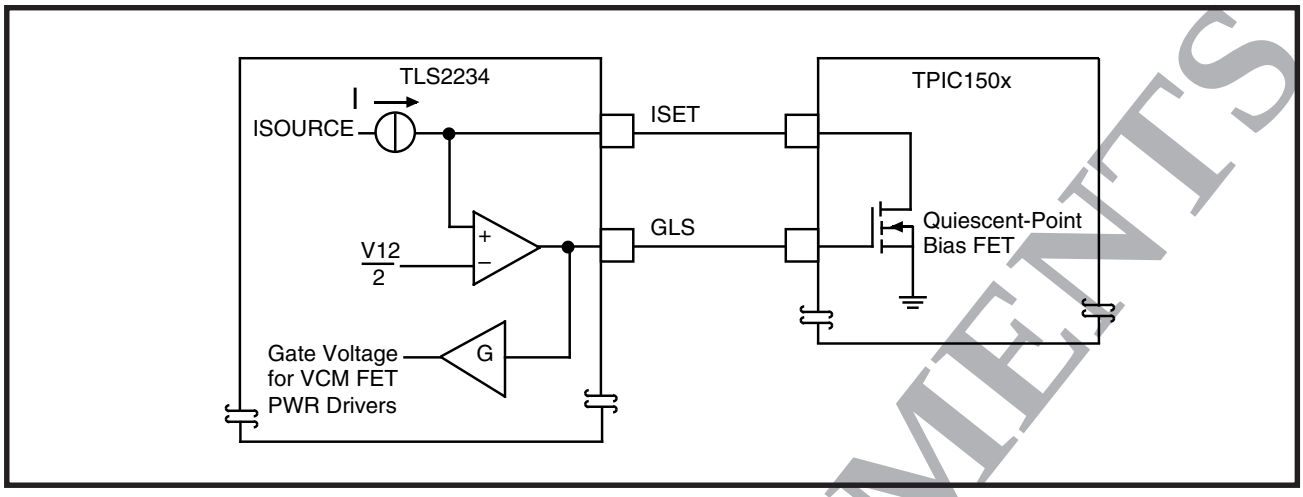


FIGURE 2-5: GLS and ISET Biasing the TPIC150x

VOICE-COIL MOTOR PREDRIVER (continued)

Biasing the TPIC150x Power FETs

The VCM predriver amplifier uses signals GLS and ISET to determine the bias point for the TPIC150x power FETs (see Figure 2-5). A constant current source is applied to the ISET pin. The gate voltage for the TPIC150x sense FET is varied until the voltage on ISET matches a known reference of V12/2. The voltage at GLS is then scaled and used to set the bias point of the TPIC150x power FETs.

$$I_{quiescent} \approx (150) \bullet I_{source}$$

Where: $I_{quiescent}$ is the bias current in the VCM H-bridge, and $I_{source} \approx 40\ \mu A$.

SPINDLE MOTOR PREDRIVER

Spindle Motor Predriver Functional Overview

Figure 2-6 shows the TLS2234 spindle motor predriver section. The RESET, ENABLEZ, and DISPWRZ signals command one of eight different operational modes:

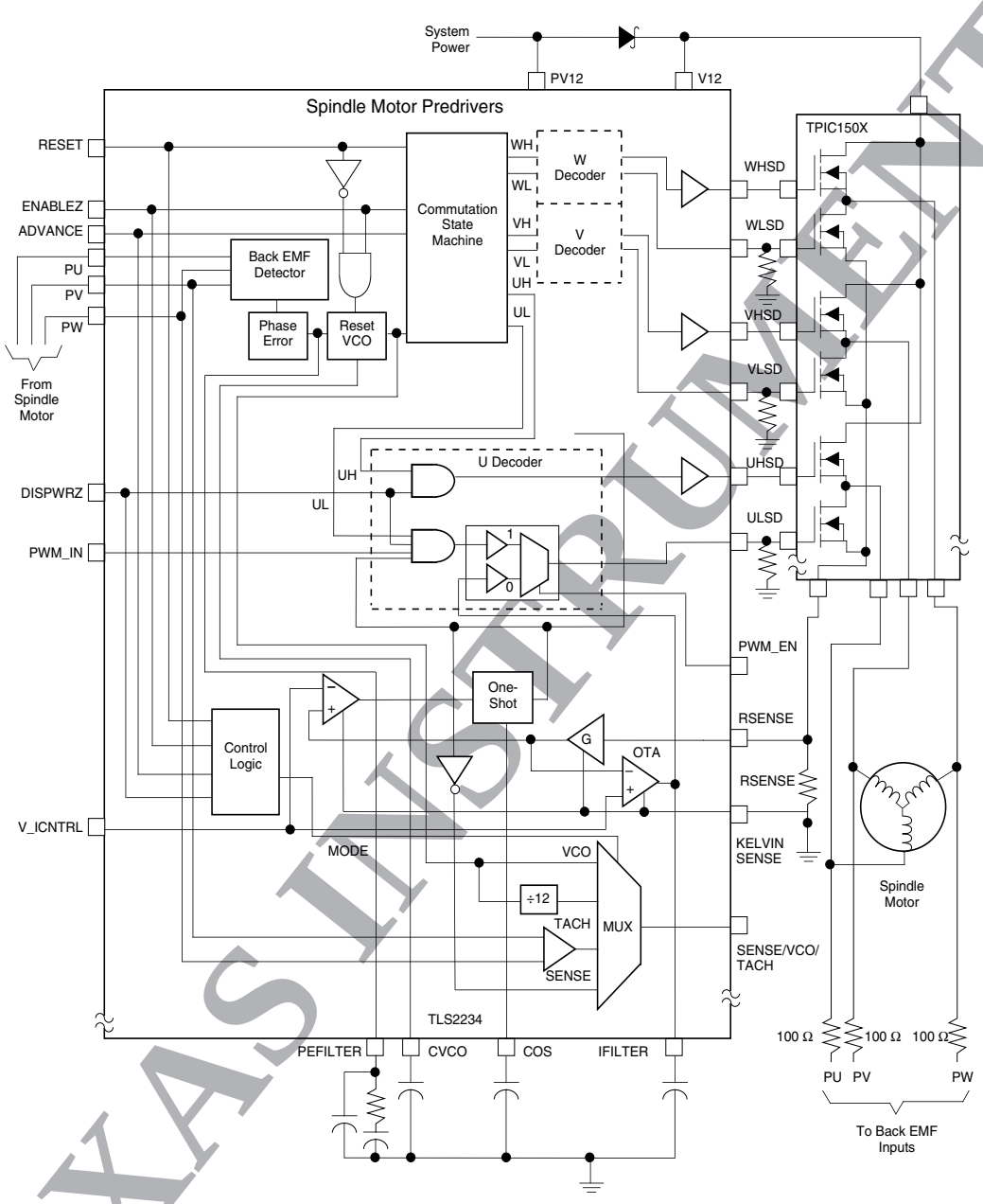
- Preset
- Start/SENSE and Start/TACH
- Run
- Coast
- Brake
- I_CAL
- Test1 †
- Test2 †

† Modes test1 and test2 are for factory test purposes and are shown for reference only.

The preset and start/SENSE and start/TACH modes are used to start the spindle motor. The commutation state machine controls motor commutation by enabling the appropriate high- and low-side drivers of the TPIC150x.

During start-up, the commutation state machine is advanced by pulses applied on ADVANCE. As the spindle motor approaches idle frequency, the run mode is selected. At this time, the commutation state machine is advanced by the output of the VCO. The BEMF detector and phase error amplifier generate an error signal that is applied to the input of the VCO. The commutation frequency is adjusted by the VCO using this error signal.

In run mode, the current applied to the motor can be controlled by either pulse width modulation (PWM) or by the application of a linear signal. The type of control is determined by setting PWM_EN (pin 49). A logic high selects PWM control, while a logic low selects linear control.

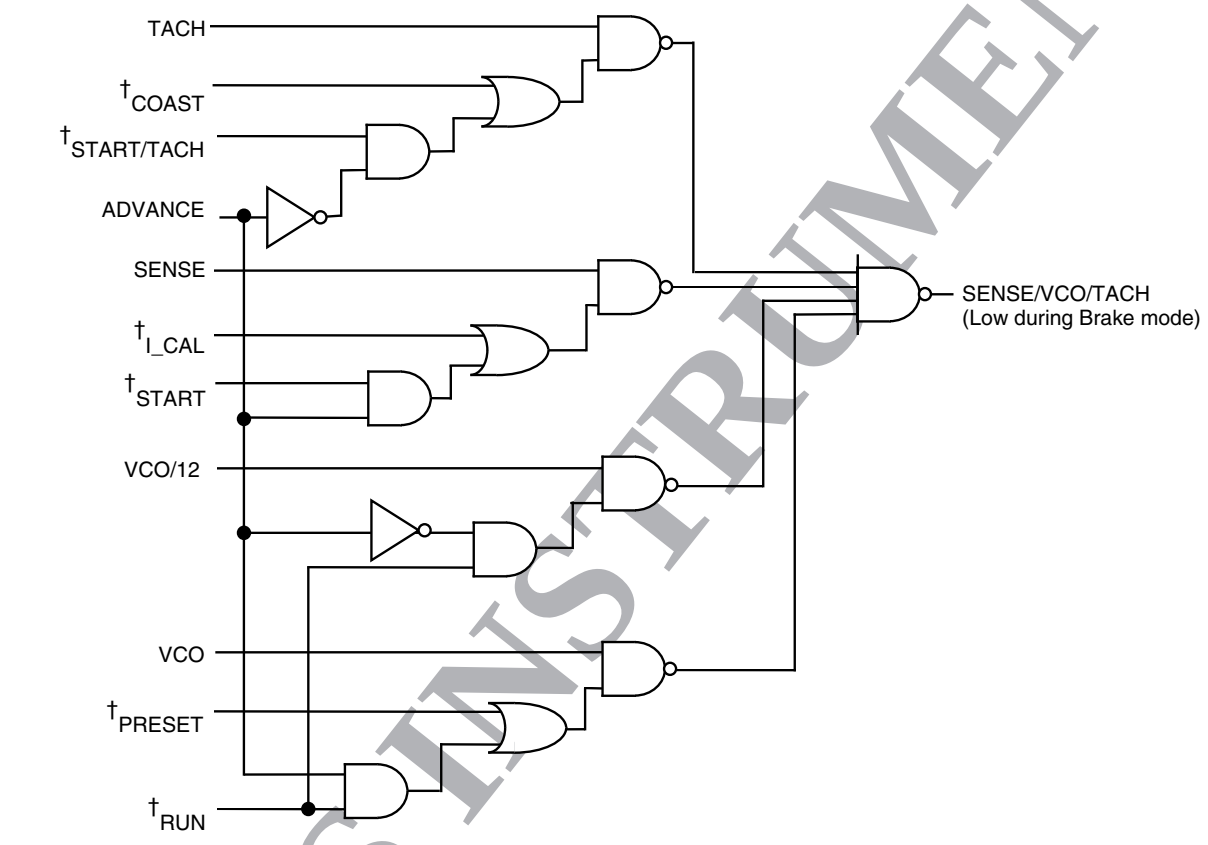


NOTE:
The ULSD, VLSD, and WLSD terminals can be connected to external 10-MΩ to 20-MΩ pulldown resistors to ensure that the TPIC150x drivers cannot turn on if not driven by the TLS2234.

FIGURE 2-6: Spindle Predrivers Functional Block Diagram

Spindle Motor Predriver Functional Overview (continued)

The MUX shown in Figure 2-6 implements the logic illustrated in Figure 2-7. The TACH, SENSE, and VCO outputs are combined with the mode signals indicated (these signals represent the various states determined by selection of RESET, ENABLEZ, and DISPWRZ as defined in Table 2-1) to provide a real-time status signal at the SENSE/VCO/TACH output.



NOTE: † Indicates mode signal (See Table 2-1)

FIGURE 2-7: Sense/VCO/TACH MUX Logic

Spindle Motor Predriver Modes of Operation

The TLS2234 spindle motor predriver circuitry operates in one of eight modes as selected by RESET, ENABLEZ, and DISPWRZ. Table 2-1 defines the combinations of these signals that are used to select either the preset, start/SENSE and start/TACH, run, coast, brake, I_CAL, test1, or test2 mode.

TABLE 2–1: Modes of Operation

MODE	DISPWRZ	RESET	ENABLEZ	ADVANCE	SENSE/ VCO/TACH	PE FILTER	VCO	STATE MACHINE	V1P9 OUT
Preset	1	1	1	X	VCO	0.1 V	Idle	Reset	1.9 V
Start	1	0	1	1	SENSE	0.1 V	Reset	†	1.9 V
Run	0	0	1	1	VCO	Run	Run	Run	1.9 V
Run	0	0	1	0	VCO/12	Run	Run	Run	1.9 V
Coast	0	0	0	X	TACH	Run	Run	Run	1.9 V
Brake	0	1	0	X	GND	0.1 V	Idle	Reset	1.9 V
I_CAL	0	1	1	X	SENSE	0.1 V	Idle	Reset	1.9 V
TEST1‡	0	0	1	X	X	X	X	X	Vbg
TEST2‡	1	1	0	X	X	X	X	X	Thermal Shutdown

† During start mode, the state machine is advanced on the rising edge of the ADVANCE pin.

‡ Modes test1 and test2 are for factory test purposes and are shown here for reference only.

The transitions between the various modes should be done according to the diagram shown in Figure 2-8 to prevent logic race conditions.

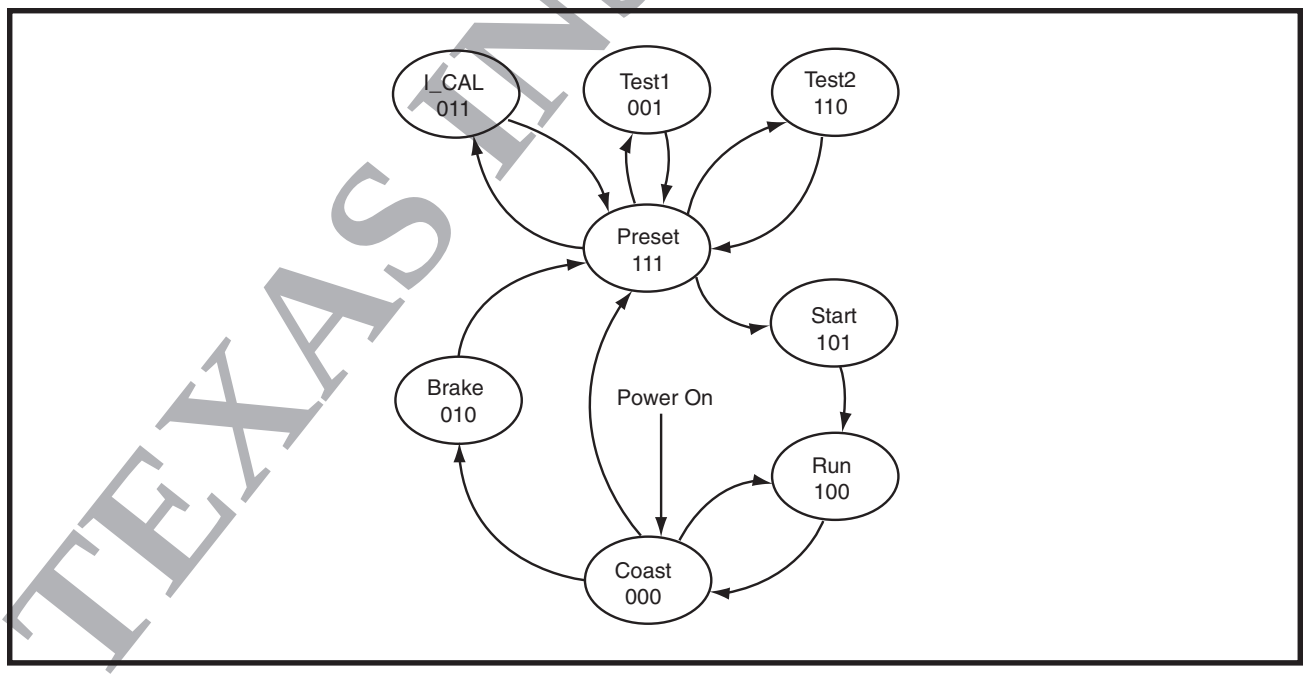


FIGURE 2-8: Mode Transition State Diagram

Spindle Motor Predriver Modes of Operation
(continued)

Preset

In the preset mode a fixed voltage of 100 mV is applied at the input to the VCO causing it to operate at its idle frequency. The VCO idle frequency, which is available at the SENSE/VCO/TACH output, is measured so that switching over (handing off) from forced commutation to closed-loop commutation can be accomplished at a frequency within the lock range of the PLL. This should be done at a frequency which is at least 10 percent higher than the idle frequency.

NOTE: To allow the filter network to settle, the VCO idle frequency measurement should not be made until after the preset mode has been commanded for at least 200 ms.

Start/SENSE

The start/SENSE mode can be used to determine the approximate position of the spindle motor's rotor so that the commutation state machine can be initialized. The output of the SENSE comparator is available at the SENSE/VCO/TACH output. The SENSE comparator will switch from low to high when the voltage across the RSENSE resistor exceeds the voltage applied at V_ICNTRL.

Start/TACH

The start/TACH mode is used to start the spindle motor. The PWM_EN pin is held high to select PWM control. In order to get maximum spindle motor acceleration, PWM_IN is held high also. This allows maximum current to be applied to the spindle motor. When the current as measured across RSENSE exceeds the threshold as set by the voltage applied at V_ICNTRL, the one shot disables the low-side spindle motor drive creating a constant off time which is set by the external capacitor COS. Choose this capacitor to optimize spin-up time and to provide sufficient over-current protection. Use equations 9 and 10 to select COS.

$$COS = \frac{I}{\Delta V} \bullet \Delta t \qquad (9)$$

where $I = \frac{Vbg}{RSLEW}$,

$Vbg = 1.21$, and $\Delta V = 2$

$$COS = \left(\frac{0.605}{RSLEW}\right) \bullet \Delta t \qquad (10)$$

Where: COS is in farads.

RSLEW is in ohms and its value is chosen using equations 11 through 14.

Δt is off time in seconds.

NOTE: Adjusting RSLEW also affects spindle driver slew rates as described in the Slew Rate Control subsection .

Since the back EMF from the spindle motor is small during start-up, the commutation state machine must be advanced manually with the ADVANCE pin. This is done open loop, using a timing algorithm that is matched to the dynamics of the motor/spindle.

During open-loop acceleration, the VCO is held at reset. When the frequency of the signal being applied to the ADVANCE pin exceeds the VCO idle frequency measured in the preset mode, select the run mode. This releases reset of the VCO enabling it to advance the commutation state machine.

Run

In the run mode, the commutation state machine is advanced by the output of the VCO. The voltage of each phase (PU, PV, and PW) is monitored to determine if commutation occurs late or early. This is done by generating a signal that is the undriven phase minus the average of the two driven phases. This signal is inverted every other cycle to obtain positive pulses. If commutation occurs too early, an increasing positive signal is generated to increase the VCO frequency to align the commutation with the motor winding. The VCO or VCO/12 output at the SENSE/VCO/TACH pin can be used as feedback for closed-loop speed regulation.

NOTE: Servo data can also be used for higher regulation.

The spindle speed is regulated by adjusting the current that is applied to the spindle motor. This is done in one of three ways.

Setting PWM_EN high selects PWM control which can be implemented in one of two ways. In the first method (voltage mode) a variable duty cycle signal is applied at PWM_IN (pin 4). This duty cycle variability is used to change the voltage that is supplied to the motor. This leads to changes in speed of the motor. Current limiting is determined by the selection of RSENSE and by the application of a threshold voltage at V_ICNTRL. When the current through the sense resistor becomes large enough that the sense amplifier output exceeds the voltage at V_ICNTRL, the one shot is triggered pulling the low-side driver gates to ground which turns them off. This current limiting is needed only during a fault condition since the current in RSENSE is not sufficient during normal operation.

NOTE: KELVIN_SENSE is used to sense the ground side of RSENSE to eliminate offset caused by ground potential differences.

In the second PWM control method (current mode) V_ICNTRL is used to control the maximum threshold at the sense resistor while PWM_IN is held at constant high level. The voltage applied at V_ICNTRL is proportional to the desired motor current. When the current through the sense resistor becomes large enough that the sense amplifier output exceeds the voltage at V_ICNTRL, the one shot is triggered which turns off the low-side drivers. The duty cycle at which the drivers turn on and off is proportional to the signal applied at V_ICNTRL. This controls the effective current applied to the spindle motor.

The linear mode is implemented by setting PWM_EN low and applying a voltage at V_ICNTRL that is proportional to the desired motor current. The transconductance amplifier (OTA) drives the gate of the appropriate low-side driver until the desired current (as sensed through RSENSE) is attained.

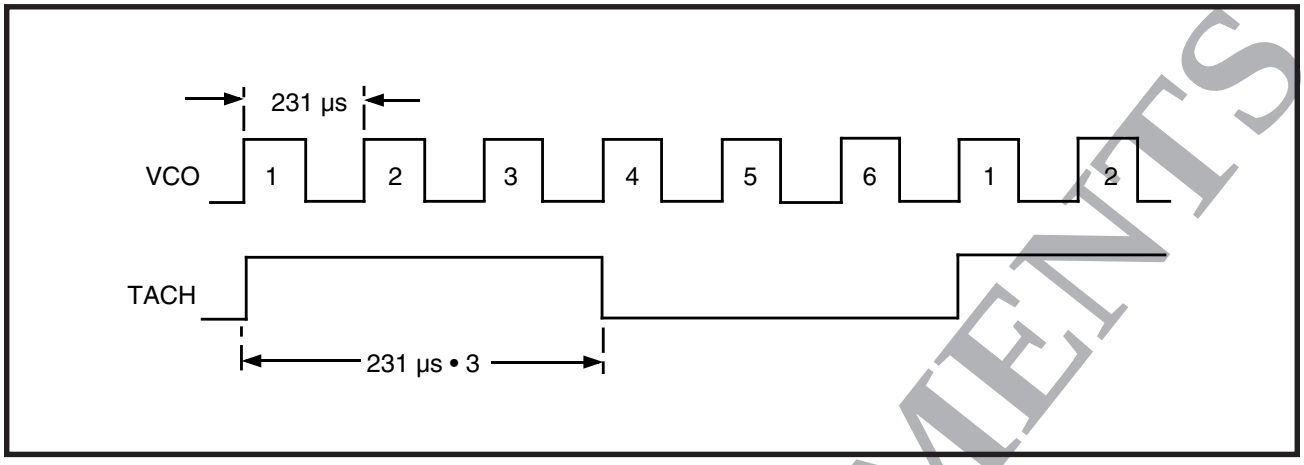


FIGURE 2-9: TACH Output for an 12-Pole 7200-RPM Motor

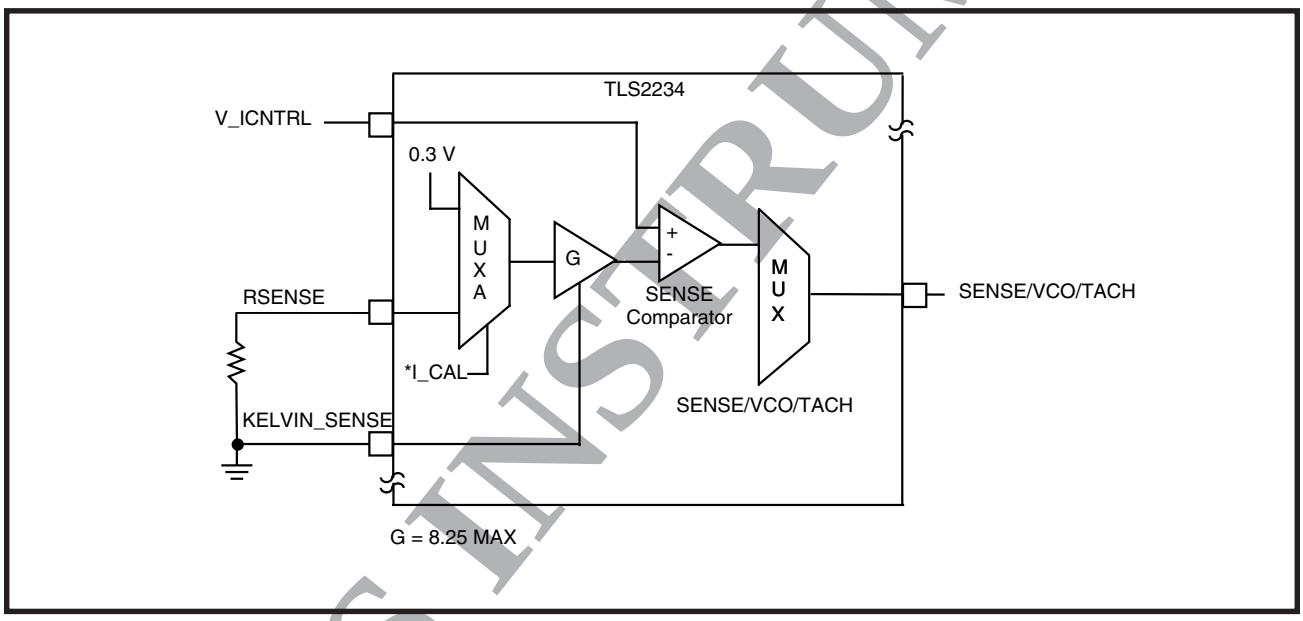


FIGURE 2-10: Calibration Mode Logic Diagram

Spindle Motor Predriver Modes of Operation

(continued)

Coast

During coast mode, the spindle motor drivers are disabled and the spindle spins freely. The TACH output is available at the SENSE/VCO/TACH pin. An example of the signal appearing at the TACH output is shown in Figure 2-9.

Brake

During brake mode, the spindle motor high-side drivers are all turned on. This causes the motor to brake dynamically.

Calibration Mode

Figure 2-10 shows the calibration mode used to measure the voltage at V_ICNTRL that corresponds to 0.3 V across the sense resistor. When the calibration mode is selected, the output of MUXA is an internal 0.3 V reference. By applying a ramp from maximum to minimum at the input of V_ICNTRL and monitoring the output at SENSE/VCO/TACH, the point at which the sense comparator switches states can be determined.

Test Modes 1 and 2

These modes are for factory testing of the TLS2234. In test mode 1, the band-gap voltage (Vbg) is available at V1P9 (pin 43). Test mode 2 is used to test over temperature or thermal shutdown through V1P9.

Commutation Control

The commutation process involves sequentially turning the spindle motor high- and low-side drivers on and off as illustrated in Figure 2-11 and listed in Table 2-2.

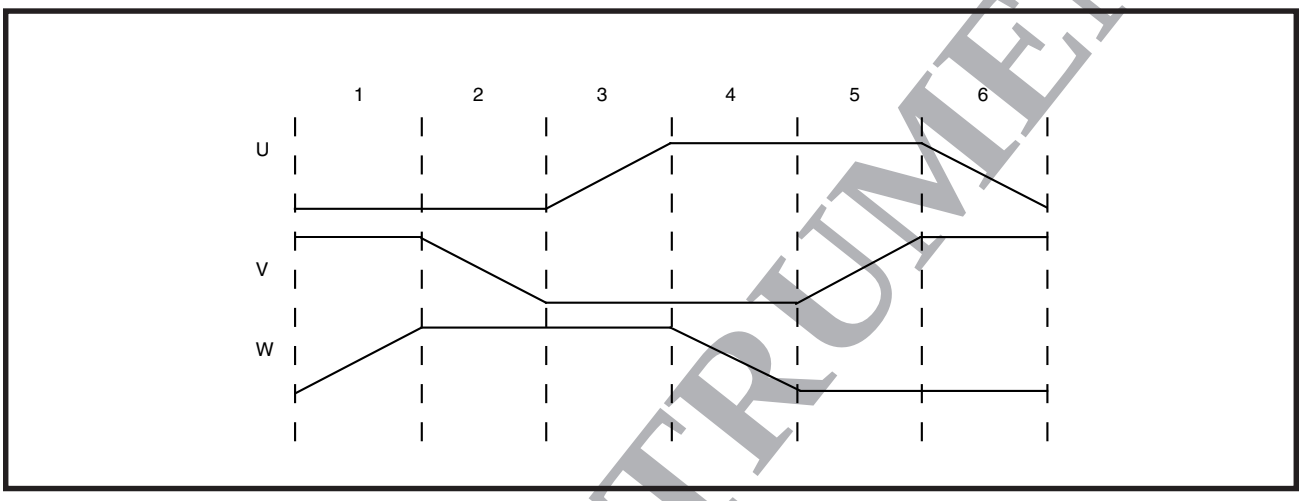


FIGURE 2-11: Commutation Graphical Form

TABLE 2-2: Commutation State Table

STATE	0 (PRESET)	1	2	3	4	5	6
UL	0	1	1	0	0	0	0
VL	0	0	0	1	1	0	0
WL	0	0	0	0	0	1	1
UH	0	0	0	0	1	1	0
VH	0	1	0	0	0	0	1
WH	0	0	1	1	0	0	0

SPINDLE MOTOR PREDRIVER (continued)

Slew Rate Control

A resistor attached to the RSLEW pin controls the slew rate of the spindle motor driver power FETs by adjusting the amount of current that is applied to the gate. The RSLEW resistor establishes a reference current, I_{SLEW}, as shown in Figure 2-12. This current is used by the high- and low-side driver circuits to determine the amount of current that is applied to the power FETs gate.

The high-side driver circuitry (Figure 2-13), provides two different levels of current for charging and discharging the power FETs gate (see Figure 2-14). During the charging interval, switch S1 is closed until the voltage at the power FETs gate, V_{GHS} , exceeds ~ 20 V. At that point, switch S1 opens.

Equation 11 is used to calculate the current applied to the gate when S1 is closed. Equation 12 is used to calculate the current applied to the gate when S1 is open.

$$I_{CHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 26.4 \quad (11)$$

$$I_{CHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 2.4 \quad (12)$$

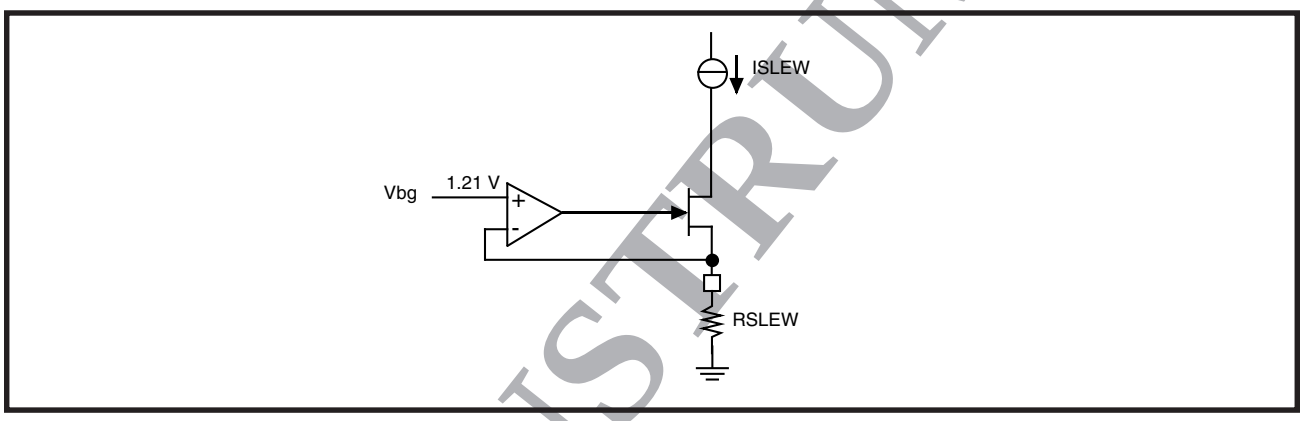


FIGURE 2-12: ISLEW Biasing Circuit

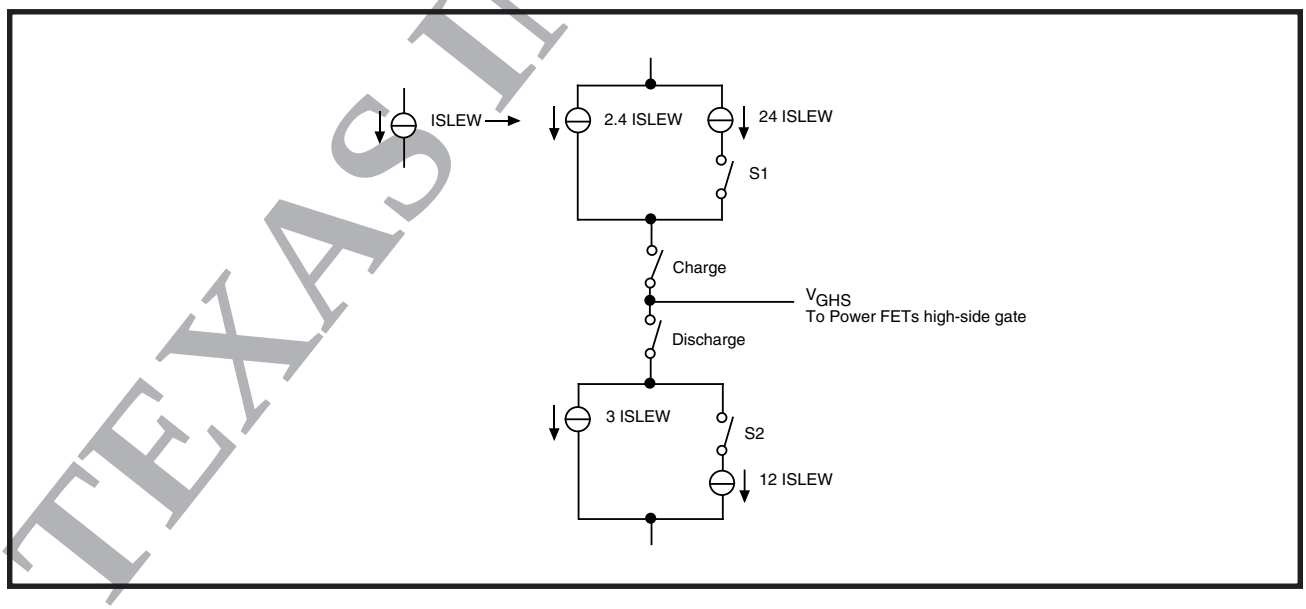


FIGURE 2-13: High-Side Driver Circuitry

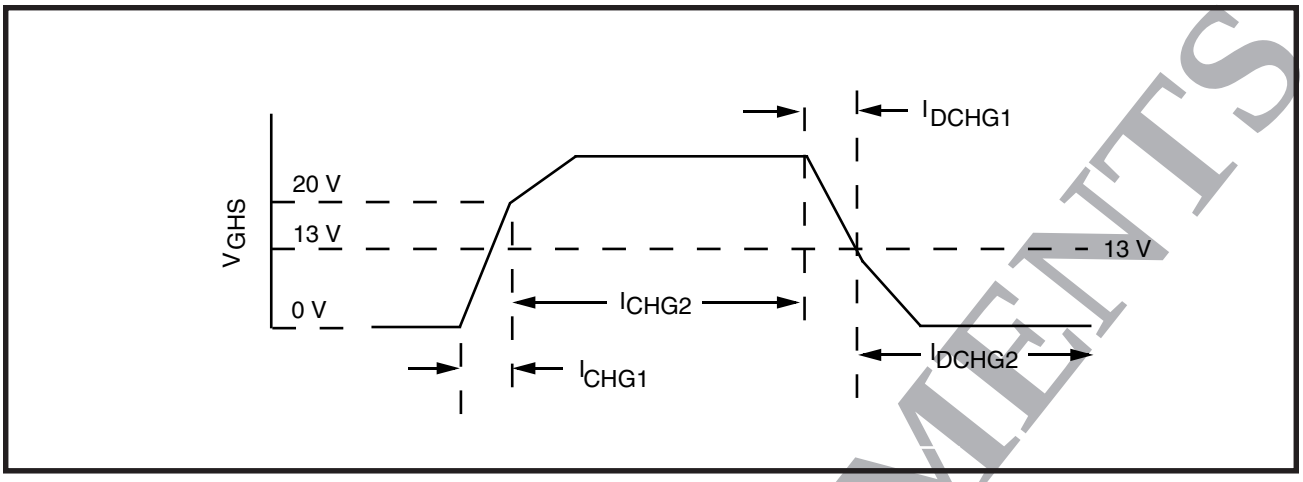


FIGURE 2-14: V_{GHS} During Charging and Discharging

During the discharging interval, switch S2 remains closed until V_{GHS} drops to below ~13 V. At this point S2 opens. Equation 13 is used to calculate the current applied to the gate when S2 is closed. Equation 14 is used to calculate the current applied to the gate when S2 is open.

Figure 2-15 shows the low-side driver circuitry. Equation 15 is used to calculate the charge current, I_{chg3} . During PWM switching of the low-side drivers, S3 and S4 are open and S5 is closed. Equation 16 is used to calculate the discharge current. Switches S3, S4, and S5 are used to control the discharge current during commutation switching of the low-side drivers. When V_{GLS} is greater than ~6 V, both S3 and S4 are closed, S5 is open, and equation 17 is used to determine the current drawn from the gate. As V_{GLS} drops below 6 V, switch S4 opens and equation 18 is used to determine the discharge current.

$$I_{DCHG1} = \left(\frac{1.21}{RSLEW}\right) \bullet 15 \quad (13)$$

$$I_{DCHG2} = \left(\frac{1.21}{RSLEW}\right) \bullet 3 \quad (14)$$

$$I_{CHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 20 \quad (15)$$

$$I_{DCHG3} = \left(\frac{1.21}{RSLEW}\right) \bullet 20 \quad (16)$$

$$I_{DCHG4} = \left(\frac{1.21}{RSLEW}\right) \bullet 22.5 \quad (17)$$

$$I_{DCHG5} = \left(\frac{1.21}{RSLEW}\right) \bullet 7.5 \quad (18)$$

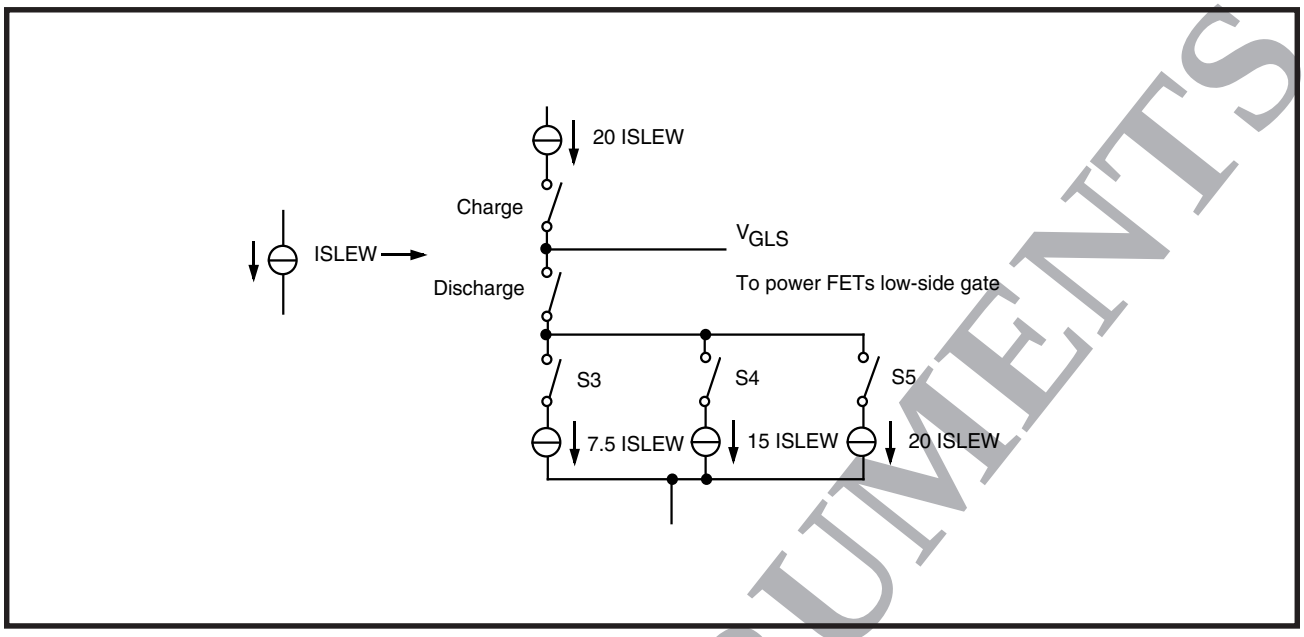


FIGURE 2-15: Low-Side Driver Circuitry

The application of these low-side currents for a single commutation interval is illustrated in Figure 2-16.

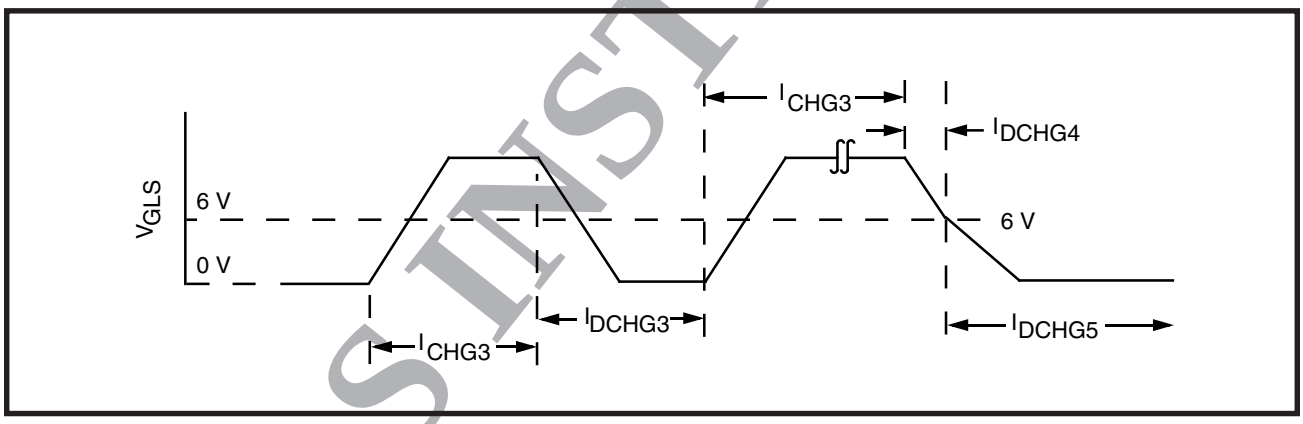


FIGURE 2-16: V_{GLS} for a Single Commutation Interval

NOTE: Adjusting RSLEW also affects the one-shot timing as described in the Start/TACH subsection.

SUPPORT FUNCTIONS

The TLS 2234 support functions include:

- Voltage regulator
- Voltage monitor
- Actuator retract control
- Spindle motor brake control
- Voltage reference
- Charge pump

Voltage Regulator

A 5 V on-chip regulator is powered from the voltage at V12, and keeps selected functions such as retract, brake, and spindle commutation powered up and functioning during power brownouts. In case of a complete 5 V and 12 V power fault, the on-chip 5 V regulator supplies power (V5R) by way of the spindle's BEMF to complete actuator retract and spindle braking. To ensure that chip logic is functional during a 12 V fault with no BEMF, a forward biased diode supplies 5 V (minus a V_f diode drop) from V5A to the V5R power bus (see Figure 2-17).

Voltage Monitor

The TLS2234 monitors 5 V and 12 V power and indicates a low condition on PORZ. The voltage monitor is shown in Figure 2-18. Off-chip capacitors are recommended at pins 47 (VCK5)and 48 (VCK12). These capacitors filter the supply voltage to ensure momentary system spikes do not interrupt system operation. The internal resistor dividers set the voltage trip levels, and external resistors can be added if adjustments in trip level are desired.

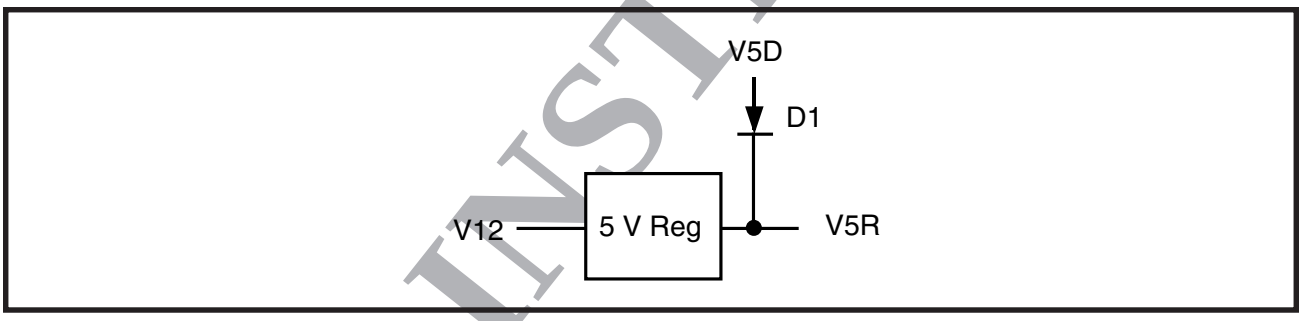


FIGURE 2-17: V5R Power Bus

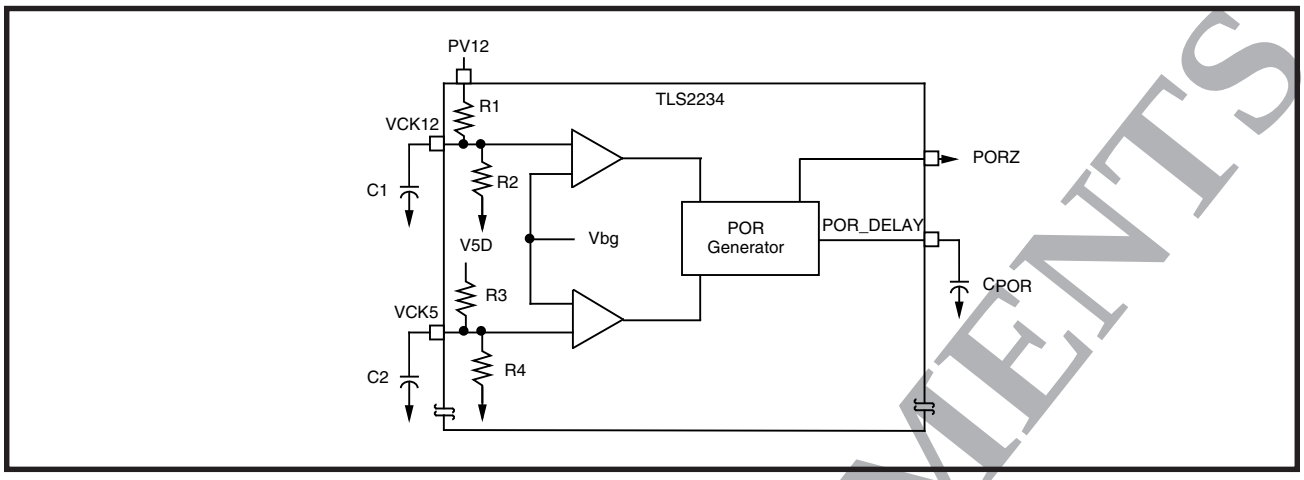


FIGURE 2-18: Voltage Monitor Schematic Diagram

NOTE: R1 = 26 270 Ω nominal
R2 = 3 650 Ω nominal
R3 = 26 270 Ω nominal
R4 = 9 429 Ω nominal
Vbg = 1.21 V nominal

Figure 2-19 shows the PORZ response to low 5 V or 12 V voltage levels

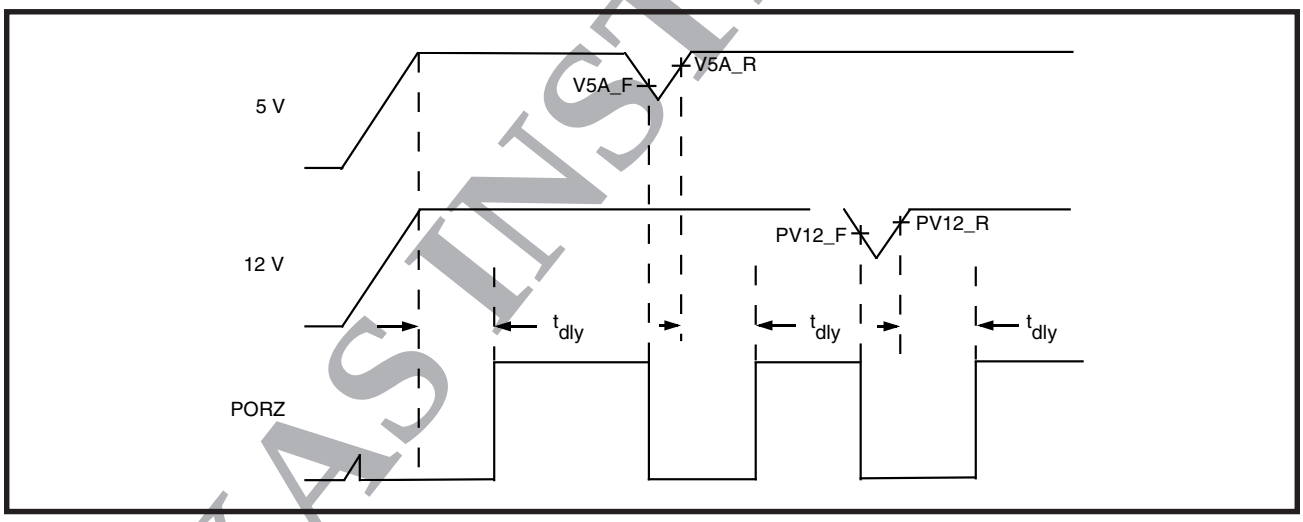


FIGURE 2-19: Voltage Monitor Response to Supply Voltages

The PORZ signal typically is used as a processor reset. Selection of C_{POR} sets the delay (tdly) of PORZ rising after power becomes valid. Equations 19 and 20 define this relationship.

$$t_{dly} = CPOR \bullet \frac{\Delta V}{I} \qquad \Delta V = VIP9 \tag{19}$$

$$\text{Note: Again, } \Delta t = \frac{C}{I}\Delta V \qquad I = 5\ \mu A \tag{20}$$

Where: CPOR is in farads.

Retract

Figure 2-20 shows the retract control logic. The actuator is immediately retracted on detection of a power fault. The PORZ signal going low causes the retract latch to be set. This causes the signal at RETP to be high ensuring that Q1 is off and Q2, Q3 and Q4 are all on. This signal also acts as an enable to the voltage control block which outputs the retract voltage on VCMA and 12 V on GNB. The retract voltage is set by the selection of RRET as follows:

$$\text{Retract voltage} = 0.5\ \text{V}\left(1 + \frac{25\ \text{k}\Omega}{5\ \text{k}\Omega + \text{RRET}}\right) \quad (21)$$

(See Note)

Where: RRET is in ohms.

NOTE: Retract voltage = 0.5 V when RRET = ∞.

During a power-down event, energy from the spindle is used to provide the VCM retract voltage.

The retract voltage to the VCM continues until either a delayed BRAKE occurs (this is indicated by DBRK going high in response to BDLY dropping below 1.2 V as illustrated in Figure 2-21) or until PORZ returns high and then DISPWRZ is set high. If delayed brake is not used and BDLY is held high, then RETP remains set and the retract voltage continues to be applied until power is restored. Then DISPWRZ is set high.

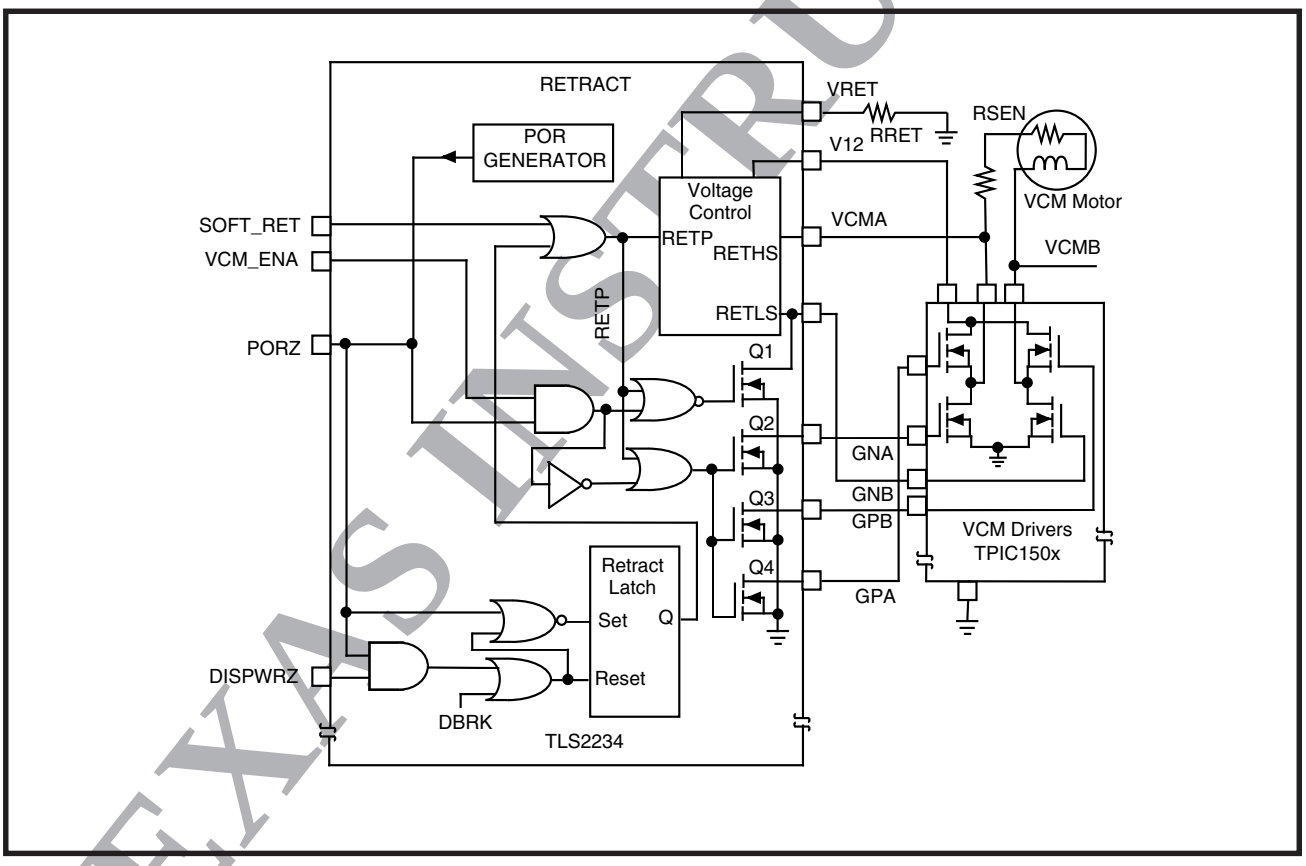


FIGURE 2-20: Retract Function Schematic

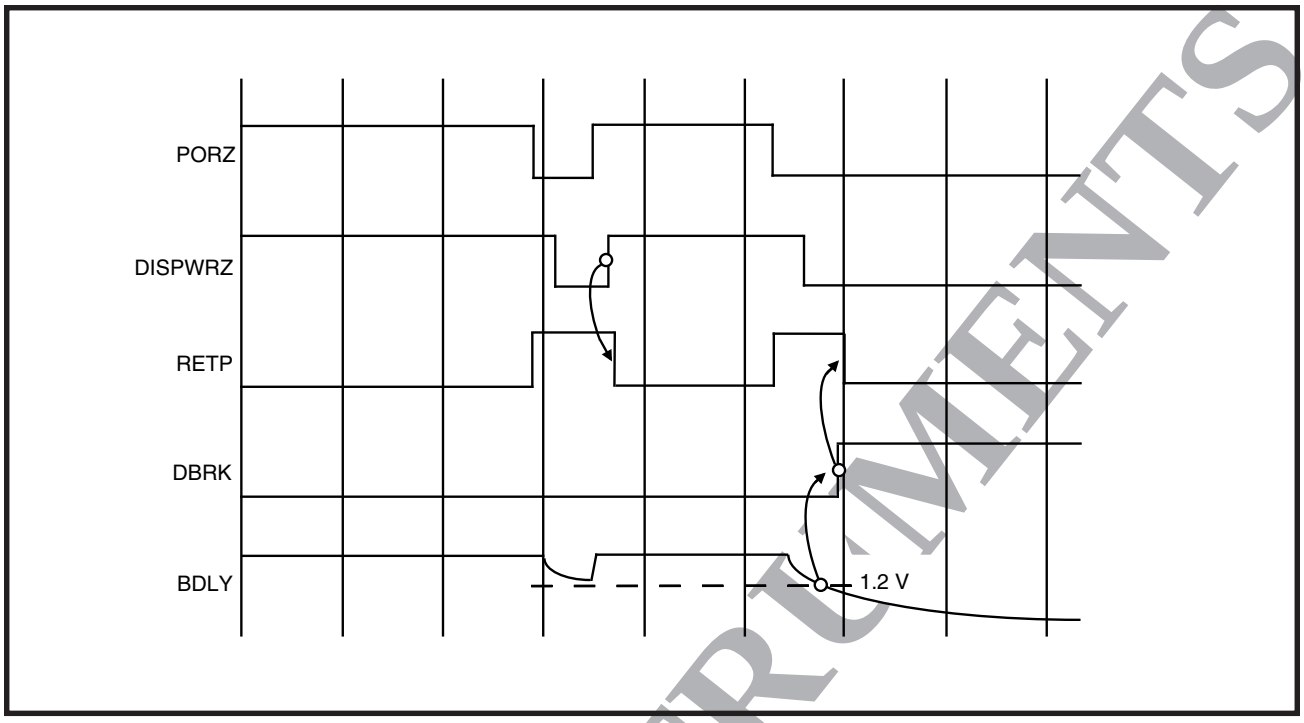


FIGURE 2-21: DISPWRZ, RETP, and SBRK Responses to PORZ and BDLY

Retract (continued)

The retract function can also be initiated by applying a logic high at SOFT_RET.

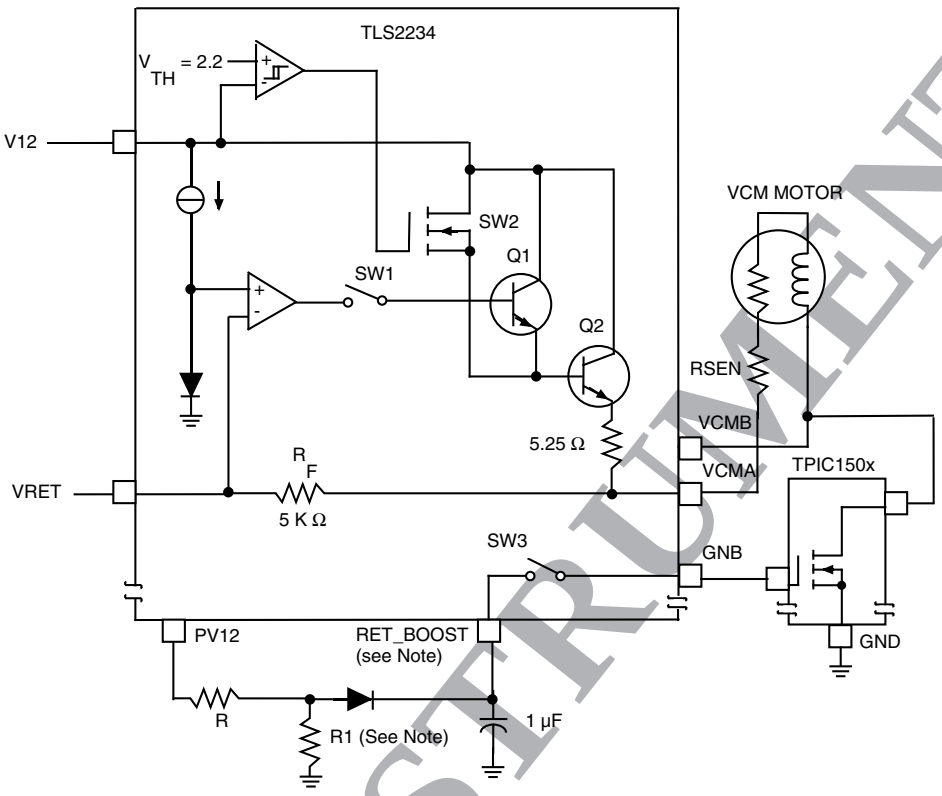
If VCM_ENA is taken low when RETP is not set, then Q1, Q2, Q3, and Q4 are on, ensuring that the VCM is disabled.

Figure 2-22 shows the retract boost circuit that ensures that the retract voltage applied to the voice coil actuator will continue even when the rectified BEMF voltage level at V12 falls during the event of a power failure. SW1 closes whenever a power fault is detected. This provides a voltage to the VCM actuator. Once the V12 voltage falls below V_{TH} , SW2 closes. This extends the range for which retract voltage is valid by increasing the gate voltage at Q2. The 2.2 V V_{TH} threshold has approximately 550 mV hysteresis to prevent unwanted switching of the boost circuit.

The RET_BOOST pin is provided to ensure that the power FET at GNB remains turned on as the V12 voltage falls. In the event of a power fault, SW3 closes, allowing the charge stored on the external capacitor to drive the gate of the power FET. This ensures that the power FET will remain on for the duration of the retract.

TI recommends that the value of the reservoir capacitor be 1µF or greater.

NOTE: The TLS2234 provides thermal protection for the retract circuitry. At approximately 150°C, the retract current is disabled. When the temperature drops below 140°C, the retract current is enabled.



NOTE: R/R1 ≃ 0.8 maximum. Maximum voltage at pin 37 (RET_BOOST) will be 10 volts.

FIGURE 2-22: RET_BOOST Scematic Diagram

The retract circuitry switches operate as follows:

Switch 1 (SW1) closes in the event of a power failure or a software retract.

Switch 2 (SW2) closes when BEMF falls below V_{TH} after a power failure.

Switch 3 (SW3) is closed during 12 V power failures.

SUPPORT FUNCITONS (continued)

Spindle Brake

The brake function turns on all spindle high-side drivers (UHSD, VHSD, and WHSD). The brake function is initiated when SBRK goes high setting the brake latch. This is done using software or generating a delayed brake. Figure 2-23 shows the TLS2234 spindle brake logic.

Software Brake (SFT_BRK)

A software brake can be commanded by setting RESET to a logic high and both ENABLEZ and DISPWRZ to a logic low.

Delayed Brake (DBRK)

A delayed brake is set after PORZ has been low for a time determined by the selection of Rext and Cext as follows:

$$\text{Brake delay time} = \text{Rext} \bullet \text{Cext} \bullet \text{Ln}\left(\frac{V5D}{Vbg}\right) \quad (22)$$

Where: Rext is in ohms
Cext is in farads
Ln is natural log
V5D is in volts
V5D = 5 V and Vbg = 1.21 V

NOTE: If the DBRK function is not used it is recommended that the BDLY pin be pulled up to V12 through a 100 kΩ resistor.

Voltage Reference

The TLS2234 generates accurate and stable voltages of 1.9 V and 3.8 V for use both internally and externally.

Charge Pump

The charge pump generates 24 V used to drive the TPIC150x high-side N-channel FETs. The charge pump requires only one external component, a storage capacitor. The recommended value for the storage capacitor is 1 μF.

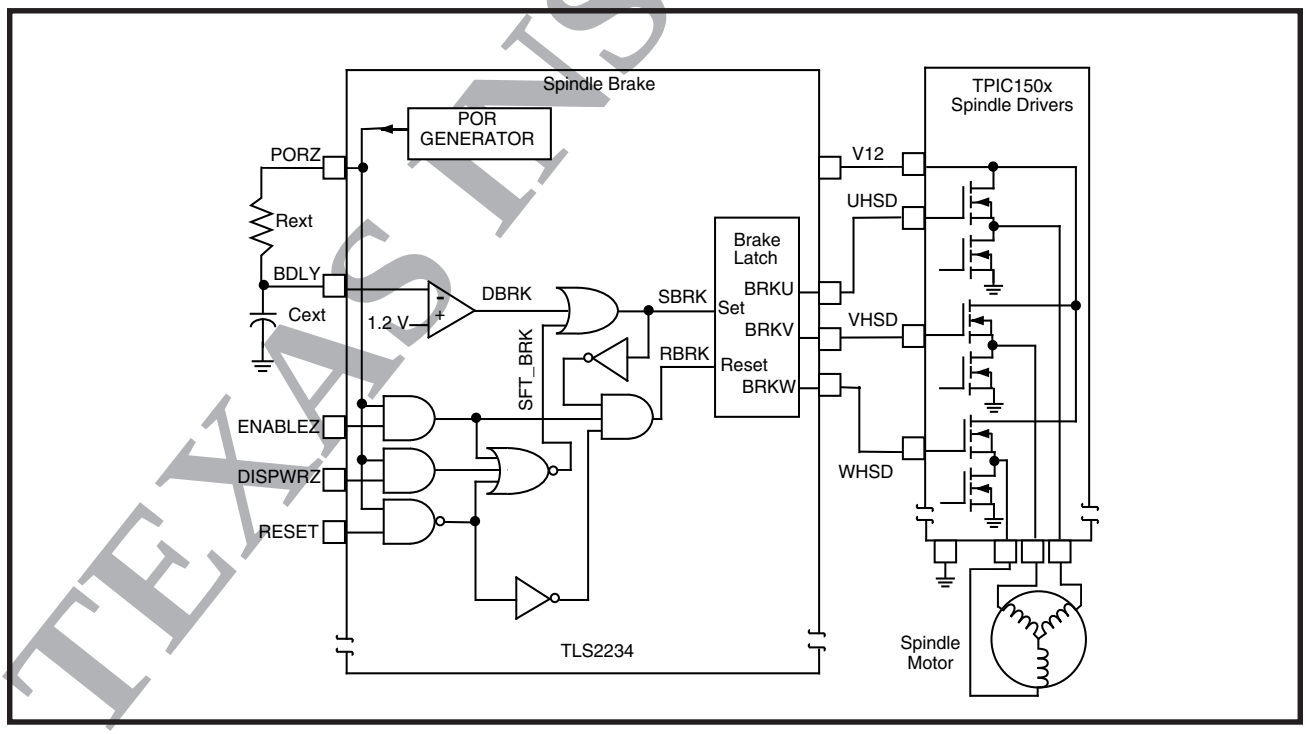


FIGURE 2-23: Spindle Brake Function Schematic

PIN DESCRIPTION

TERMINAL FUNCTIONS

Lists the TLS2234 terminal functions.

TERMINAL NAME	I/O	TYPE	DESCRIPTION
SUPPLIES			
AGND		Ground	Analog ground
CP	O	Analog	Charge pump storage capacitor connection
DGND		Ground	Digital ground
PV12	I	Analog	12 V power supply monitor (sensed by voltage monitor to generate PORZ)
V1P9	O	Analog	1.9 V reference output
V5A		Power	5 V power supply (analog)
V5D		Power	5 V power supply (digital)
V3P8	O	Analog	Reference output (2 • V1P9)
V12		Power	12 V power supply (with blocking diode)
VCM			
A3	O	Analog	Filter amplifier output
A3P	I	Analog	Filter amplifier noninverting input
ERR	O	Analog	VCM current loop error amplifier output
ERRN	I	Analog	VCM current loop error amplifier inverting input
GLS	O	Analog	Driver sense gate
GNA	O	Analog	A low-side driver gate output
GNB	O	Analog	B low-side driver gate output
GPA	O	Analog	A high-side driver gate output
GPB	O	Analog	B high-side driver gate output
ISET	O	Analog	Driver sense drain (bias current for class AB operation)
RSEN	I	Analog	VCM current-sense feedback. Connects internally to the inverting input of the current-sense differential amplifier
RET_BOOST	I	Analog	VCM low-side driver gate bias boost
SOFT_RET	I	Digital	Initiates retract (high level indicates retract)
SOUT	O	Analog	VCM current-sense amplifier feedback
VCMA	I	Analog	VCM current-sense resistor. Connects internally to the noninverting input of the current-sense differential amplifier and externally to the driver side of the sense resistor
	O	Analog	Retract voltage output

TABLE 1-1: Terminal Functions (continued)

TERMINAL NAME	I/O	TYPE	DESCRIPTION
VCM (continued)			
VCMB	I	Analog	VCM in. Connects externally between the drivers and the VCM
VCM_ENA	I	Digital	High level enables the VCM, low level disables the VCM. This signal is ignored during retract.
VRET	I	Analog	VCM retract voltage control (voltage controlled by selection of resistor connected externally to this pin)
SPINDLE MOTOR			
ADVANCE	I	Digital	Commutation state machine advance (used for spindle start)
COS	O	Analog	Capacitor for one-shot timing
CVCO	O	Analog	Capacitor to set VCO speed range for motor commutation
DISPWRZ	I	Digital	Mode control (low level disables spindle power)
ENABLEZ	I	Digital	Mode control (active low)
IFILTER	O	Analog	Linear current control filter
KELVIN_SENSE	I	Analog	RSENSE ground
PEFILTER	O	Analog	Phase error filter for commutation PLL
PU	I	Analog	Phase U back EMF sense
PV	I	Analog	Phase V back EMF sense
PW	I	Analog	Phase W back EMF sense
PWM_IN	I	Digital	PWM input for low-side driver (used during PWM start and PWM run modes)
PWM_EN	I	Digital	High level selects PWM run, low level selects linear run
RESET	I	Digital	Mode control (active high) (resets VCO and state machine)
RSENSE	I	Analog	Spindle current-sense voltage feedback (high side of RSENSE)
RSLEW	O	Analog	Current setting control for spindle driver, slew rates, and one-shot timing used in the constant off-time spindle motor current regulator
SENSE/VCO/ TACH	O	Digital	MUX out: Current threshold SENSE during start mode. VCO during prestart mode or run mode. TACH during coast mode.
UHSD	O	Analog	U high-side driver gate output
ULSD	O	Analog	U low-side driver gate output
VHSD	O	Analog	V high-side driver gate output
VLSD	O	Analog	V low-side driver gate output
WHSD	O	Analog	W high-side driver gate output
WLSD	O	Analog	W low-side driver gate output
V_ICNTRL	I	Analog	Motor current control

TABLE 1-1: Terminal Functions (continued)

TERMINAL NAME	I/O	TYPE	DESCRIPTION
VOLTAGE MONITOR (VM)			
BDLY	I	Analog	Brake delay, retract time-out
PORZ	O	Digital	Power on reset (active low)
POR_DELAY	O	Analog	Capacitor to set PORZ delay
VCK5	O	Analog	Low V5D voltage monitor filter/threshold set
VCK12	O	Analog	Low PV12 voltage monitor filter/threshold set

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE
(unless otherwise noted)†

PARAMETER	RATING
Supply voltage, V12, PV12 (see Note 1)	15 V
Supply voltage, V5D, V5A (see Note 1)	7 V
Negative voltage applied to any pin (see Note 2)	-0.5 V
Power dissipation, T_A = 70°C	1 W
Charge pump output voltage	26 V
Operating free-air temperature range	0°C to 70°C
Operating virtual junction temperature, T_J	≤ 150°C
Thermal resistance Junction-to-case, $R_{\theta JC}$	27.3°C/W
Storage temperature range, T_{stg}	-55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to ground.
2. The maximum negative voltage can be affected by either temperature or current.

RECOMMENDED OPERATING CONDITIONS OVER RECOMMENDED SUPPLY
Voltage, T_A = 25°C (see Note 3)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply voltage V5A, V5D	VCK5 = 5 V	4.75	5	5.25	V
Supply voltage PV12	VCK12 = 5 V	10.8	12	13.2	V
Supply voltage V12	VCK12 = 5 V	10.3	11.5	12.7	V
Digital high-level input voltage V_{IH}		3.5		V5D+0.3	V
Low-level input voltage V_{IL}		-0.4		0.5	V
Voltage applied to any pin		-0.4			V

NOTE 3: These parameters are not tested. They are determined by design characterization.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

Total Device Over Recommended Supply Voltage (see Note 4)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply current I_{DD}	I_{PV12}				600	µA
	I_{V12}				25	mA
	I_{V5}				10	mA
High-level logic input current (see Note 4) At ENABLEZ, DISPWRZ, or RESET	I_{IH}	V_{IN} = 5 V			70	µA
High-level logic input current (see Note 4) At ADVANCE, PWM_EN, PWM_IN, SOFT_RET, or VCM_ENA	I_{IH}	V_{IN} = 5 V			1	µA
Low-level logic input current	I_{IL}				-1	µA
Low-level output voltage	V_{OL}	I_O = -20 µA			0.1	V
High-level output voltage	V_{OH}	I_O = 20 µA	V5D - 0.1 V			V

NOTE 4: There are internal 120 kΩ pulldown resistors for DISPWRZ, ENABLEZ, and RESET.

Voltage Monitor (see Note 5)

Falling 12-V voltage, PORZ	PV12_F		9.5	9.8		V
Rising 12-V voltage, PORZ	PV12_R			10	10.4	V
Hysteresis 12 V, PORZ			50	250	500	mV
Falling 5-V voltage, PORZ	V5A_F		4.4	4.5		V
Rising 5-V voltage, PORZ	V5A_R			4.6	4.7	V
Hysteresis 5 V, PORZ			50	100		mV
Short-circuit output current, PORZ	I_{OS}	V_{OL} = 0.5 V	375		650	µA
Low-level output current, PORZ	I_{OL}		-5			mA
High-level output voltage, PORZ	V_{OH}	V5D = 5 V, I_{OH} = 100 µA	3.5	4		V
Low-level output voltage, PORZ	V_{OL}	V5D = 5 V, I_{OL} = -5 mA		0.3	0.5	V

NOTE 5: As the power goes up and/or down, comparators and band gap voltage are available at 1.5 V for 5 V supply and 2.5 V for 12 V supply, which allows proper driver disabling through the power-up process.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

PORZ Minimum Supply Threshold, PORZ I_{OL} = –5 mA (see Note 6)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V5A (rising from 0)	PV12 = 0 V		0.92	1.5	V
PV12 (rising from 0 to 3.0 V)	V5A = V5D = 0 V		2.52	3.0	V

NOTE 6: Typical and maximum values indicated for valid PORZ.

Retract (See Note 7)

Minimum retract voltage (see Note 8)	I_{VCMA} = 50 mA, V_{RET} = OPEN	0.4	V_{MED}	0.6	V
Maximum retract voltage†	I_{VCMA} = 50 mA, V_{RET} = GND	2.4	3	3.6	V
Retract voltage program accuracy †	I_{VCMA} = 50 mA, V_{RET} = 20 kΩ to GND	0.75	1	1.25	V
Retract voltage regulation	I_{VCMA} = 25 mA, V_{RET} = OPEN V12 = 1.9 V	250			mV
Retract boost threshold	I_{VCMA} = 40 mA, V_{RET} = GND (see Note 9)	V12 = 1.9			V
Retract boost threshold	I_{VCMA} = 40 mA, V_{RET} = GND (see Note 10)			V12 = 2.9	V
Retract current limit	VCMA to GND	100	135	170	mA
Voltage on GPA, GPB, GNA				0.7	V
Voltage on GNB		V12-1			V

NOTES: 7. Retract is disabled when temperature exceeds 150°C. This parameter is not tested.
8. $V_{MED} \cong 0.5$ V which is the forward bias voltage of the Schottky diode. This voltage will vary with temperature.
9. V12 falling until VCMA > 600 mV.
10. V12 rising until VCMA < V_{MED} .

Braking Circuit

VLSD OFF	Software brake			0.7	V
VHSD HIGH	Software brake	20			V
Leakage current, C_{BDLY}	V_{BDLY} = 5 V			200	nA
Brake threshold voltage, BDLY		0.8	1.2	1.4	V

Charge Pump (see Notes 11 and 12)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Charge pump output voltage	V12 = 12 V, V5D = 5 V	22	25	26	V
Charge pump output voltage load regulation †	See Note 13		0.015	0.025	V/µA
Oscillator frequency †			4		MHz
Charge time †			0.5		s
Charge pump leakage current				1	µA

NOTES: 11. External storage capacitor is typically 1 µF.
12. Minimum voltage, that should be maintained on the charge pump to ensure successful delayed brake, is typically 18 V for any TPIC150x device. However, this voltage is a function of the current that the power driver sinks and the power dissipated in the device.
13. The output can drive external N-channel DMOS switches; the effective dc loading should be less than 1 µA.

† These parameters are not tested. They are determined by design characterization.

Voltage Reference (see Note 14)

V1P9 output	Load 3 mA and -80 µA	1.824	1.9	1.978	V
V3P8 output	Load 3 mA and -80 µA	3.648	3.8	3.952	V
Ratio of V3P8 to V1P9		1.96	2	2.04	V/V
V1P9 source current (see Note 15)				3	mA
V3P8 source current (see Note 16)				3	mA
V1P9 sink current (see Note 15)		-80			µA
V3P8 sink current (see Note 16)		-80			µA

NOTES: 14. Maximum external capacitive load = 1 µF.
15. Verified from V1P9 test.
16. Verified from V3P8 test.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

VCM Input Filter Amplifier (A3)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input bias current	I_{IB}		-1		1	µA
Input offset voltage	V_{IO}		-10		+10	mV
Average temperature coefficient of input offset voltage†	VIO			15		µV/C
Slew rate †	SR	R_L = 10 kΩ, C_L = 60 pF		1		V/µs
Gain (see Note 17)	G		1.9	2	2.1	V/V
Gain bandwidth product †	GBN			1		MHz
Open-loop voltage gain †		f = 1 kHz, R_L = 10 kΩ		60		dB
Supply voltage rejection ratio	PSRR		60	70		dB
Common mode rejection ratio†	CMRR			60		dB
Input voltage range, with respect to V1P9 †	V_{IC}			±1.9		V
Output swing, with Respect to V1P9	V_{OPP}	R_L = 10 kΩ (tied to V1P9 level)	-1.5		+ 1.5	V

NOTE 17: Filter gain set internal to device
† These parameters are not tested. They are determined by design characterization.

VCM Current-Loop-Error Amplifier (ERR)

Input bias current	I_{IB}		-1		1	µA
Input offset voltage	V_{IO}		-10		10	mV
Average temperature coefficient of input offset voltage†	VIO			15		µV/C
Slew rate†	SR	R_L = 10 kΩ, C_L = 60 pF to V1P9		1		V/µs
Gain bandwidth product†	GBW			1		MHz
Open-loop voltage gain†		R_L = 10 kΩ, f = 1 kHz		70		dB
Supply voltage rejection ratio	PSRR		60			dB
Common mode rejection ratio†	CMRR			60		dB
Input voltage range, with respect to V1P9†	V_{IC}			±1.9		V
Output swing, with respect to V1P9	V_{OPP}	R_L = 10 kΩ (tied to V1P9 level)	-1.5		+ 1.5	V

† These parameters are not tested. They are determined by design characterization.

VCM Current-Sense Amplifier (ASEN)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input offset voltage	V_{IO}	Measured at SOUT with respect to V1P9 (RSEN tied to VCMA)	-5	0	+5	mV
Gain	G		2.67	2.73	2.79	V/V
Slew rate †	SR	R_L = 10 kΩ,C_L = 60 pF		1		V/µs
Gain bandwidth product†	GBW			1		MHz
Open-loop voltage gain†		f = 1 kHz, R_L = 10 kΩ		66		dB
Supply voltage rejection ratio	PSRR		60			dB
Common mode rejection ratio	CMRR	VCMRR = 0.5 V to 4.5 V	55			dB
Common mode input voltage†	V_{IC}		0		12	V
Output swing, with respect to V1P9	V_{OPP}	R_L = 5 kΩ (tied to V1P9 level)	-1.5		+ 1.5	V

† These parameters are not tested. They are determined by design characterization.

VCM Transconductance Loop System Offset

Output offset current	I_{IO}	Figure C-1	-20		+20	mA

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

VCM Predriver Amplifier

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage GPA, GPB	V_{OH}	R_L = 6 MΩ	20			V
High-level output voltage GNA, GNB	V_{OH}	R_L = 6 MΩ	V12-2			V
Low-level output voltage GPA, GPB	V_{OL}				0.7	V
Low-level output voltage GNA, GNB	V_{OL}				0.7	V
Slew rate positive† GPA, GPB	SR+	C_L = 50 pF, see Note 18		0.5		V/µs
Slew rate positive† GNA, GNB	SR+	C_L = 50 pF, see Note 19		0.5		V/µs
Slew rate negative† GPA, GPB	SR-	C_L = 50 pF, see Note 20		2		V/µs
Slew rate negative† GNA, GNB	SR-	C_L = 50 pF, see Note 20		2		V/µs
Quiescent current†				8		mA
Gain†	G	VCMA to VCMB		12		V/V
Unity gain bandwidth †				1		MHz
Common-mode rejection ratio†	CMRR		60			dB
Power supply rejection ratio†	PSRR		60			dB

NOTES: 18. Slew rate calculated as average positive slew rate from 1 V to 18 V
19. Slew rate calculated as average positive slew rate from 1 V to 10 V
20. Slew rate calculated as average negative slew rate from 18 V to 1 V

† These parameters are not tested. They are determined by design characterization.

VCO (unless otherwise specified, CVCO = 0.0042 μF)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Typical frequency† f	$\left(\frac{VPE}{2 \cdot 30.48\ k\Omega \cdot V1P9 \cdot CVCO}\right)$				Hz
	$V_{0(PEFILTER)}$ = 2.1 V	3456	4320	5184	Hz
Idle frequency†	Mode = Reset	160	200	240	Hz
High-side CVCO voltage trip level	Ramp CVCO from 2.5 V to 3.2 V	2.6	2.85	3.1	V
Low-side CVCO voltage trip level	Ramp CVCO from 1.1 V to 0.8 V	0.85	0.95	1.05	V
Source/Sink Current (CVCO)	PEFILTER = 3 V	75	100	125	μA
Low-level output voltage, V_{OL} (-100 μA) SENSE/VCO/TACH				0.5	V
High-level output voltage, V_{OH} (100 μA) SENSE/VCO/TACH		3.5			V
Rise/Fall Time (SENSE/VCO/TACH)†	C_L = 10 pF		100		ns

† These parameters are not tested. They are determined by design characterization.

Phase Error Amplifier

Output voltage V_O $V_{PEFILTER}$, (V_{idle})	Mode = Preset	75	100	125	mV
Output current at PEFILTER, I_O run mode	$V_{0(PEFILTER)}$ = 2.1 V	115	150	175	μA
Source/sink current mismatch	$V_{0(PEFILTER)}$ = 2.1 V	-7%		+7%	
Input offset voltage† V_{IO} PU, PV, or PW See Note 21	PU, PV, or PW = V12, PW = 0	-180		+180	mV
Maximum voltage† PU, PV, and PW				15	V

NOTE 21: Add 100 Ω resistance in series with PU, PV, and PW inputs to prevent high reverse (below ground) current during start.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C (continued)

Spindle Predriver Amplifier

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
High-level output voltage UHSD, VHSD, WHSD	V_{OH}	R_L = 6 MΩ	20			V
Low-level output voltage UHSD, VHSD, WHSD	V_{OL}				0.7	V
High-level output voltage ULSD, VLSD, WLSD	V_{OH}	R_L = 6 MΩ	V12-2			V
Low-level output voltage ULSD, VLSD, WLSD	V_{OL}				0.7	V

Spindle Current-Sense Amplifier

Input voltage range†			0		0.5	V
Closed-loop gain	G	I_{CAL}	6.75	7.5	8.25	V/V
Output swing†	V_{OPP}		0.1		4.5	V
Input offset voltage†	V_{IO}			8		mV

† These parameters are not tested. They are determined by design characterization.

Current-Sense Comparator

Input offset voltage†	V_{IO}			10		mV
Common mode†			0		4	V

† These parameters are not tested. They are determined by design characterization.

TACH Comparator

Input offset voltage	V_{IO}		-10		+10	mV
Hysteresis	V_{hys}		60	100	125	mV
Common mode†			0		4	V

† These parameters are not tested. They are determined by design characterization.

Motor Current Control

I_COS_CHG		80	100	120	µA
I_COS_DCHG		3	3.7		mA
One-shot off time† (see Note 22)	C_{OS} = 0.001 µF, R_{SLEW} = 12.1 kΩ	15	25	35	µs
V_ICNTRL deadband†		80	95	110	mV

NOTE 22: Minimum one-shot off time regardless of COS and RSLEW values is typically 5 µs.
† These parameters are not tested. They are determined by design characterization.

MECHANICAL DATA

Figure 4-1 shows mechanical outline dimensions.

DL (R-PDSO-G56) **PLASTIC SMALL OUTLINE PACKAGE**

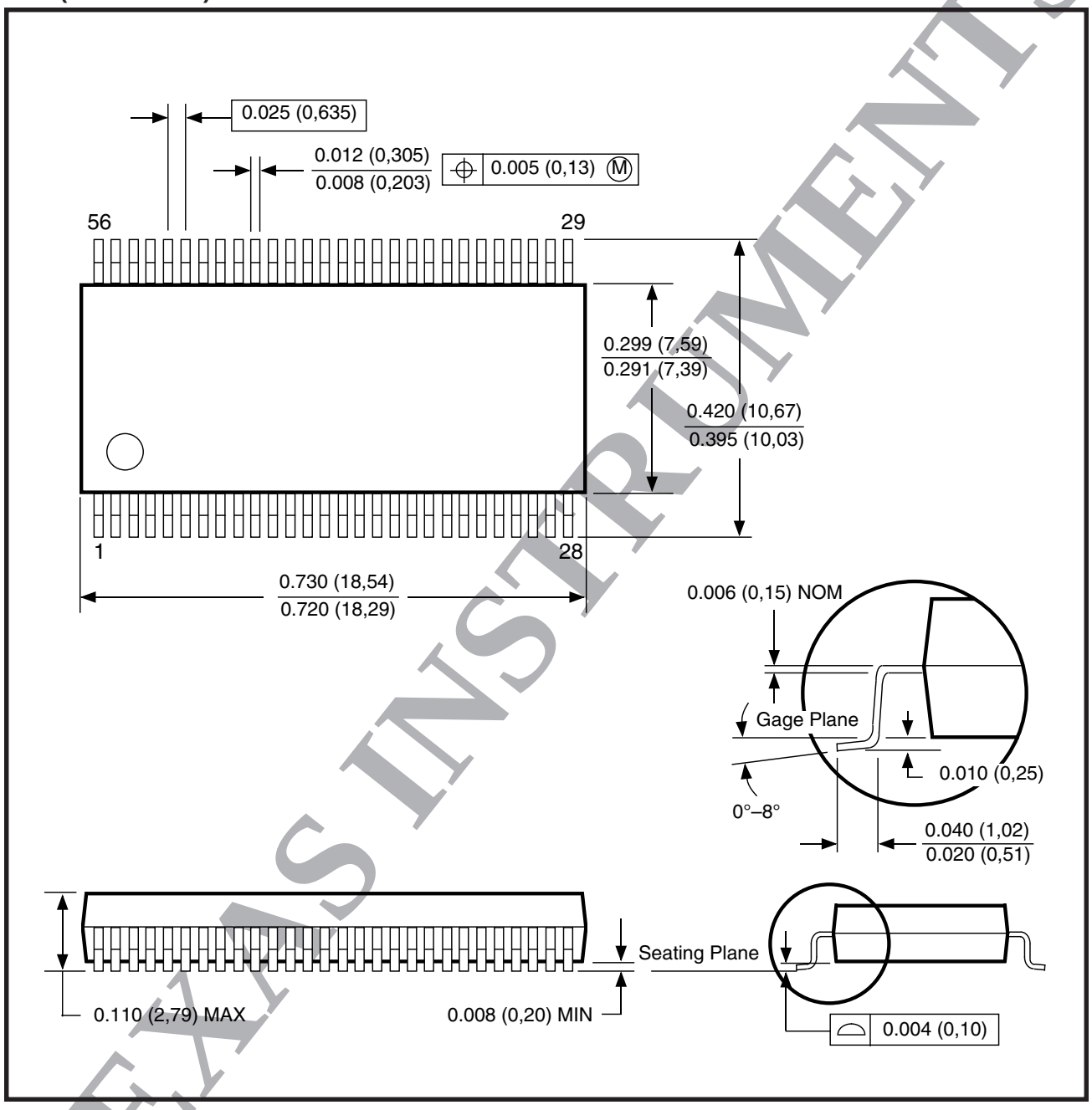
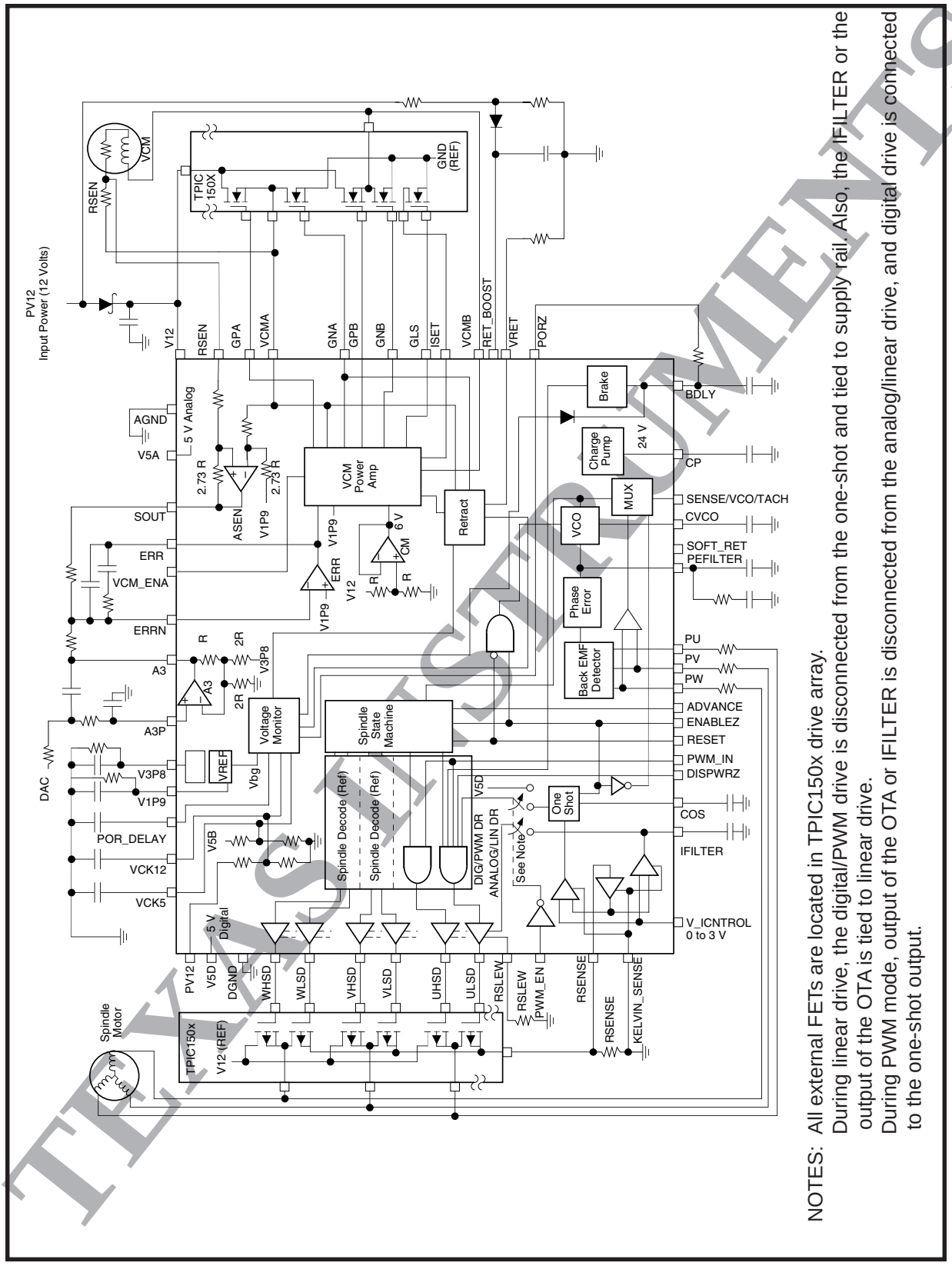


FIGURE 4-1: Mechanical Data

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

TABLE A-1: System Level Responses to Various Inputs

POR	DBRK	V12	SBRK	VCMENA	SFTRST	RESETB	ENABLEZ	DISPWRZ	SOFTWARE MODE (as selected by RESET, ENABLEZ, and DISPWRZ)	SPIN MOTOR	GPA, GPB, GNA	GNB	VCMRET	VCMBRK	VCM	RETRACT
1	0	>10.4 V	0	1	0	0	0	1	RUN	RUN	ON	ON	0	0	ON	OFF
1	0	>10.4 V	0	X	1	0	0	1	RUN	RUN	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	0	0	0	0	0	1	RUN	RUN	LOW	LOW	1	1	OFF	OFF
1	0	>10.4 V	1	1	0	1	0	0	BRAKE	BRAKE	ON	ON	0	0	ON	OFF
1	0	>10.4 V	1	X	1	1	0	0	BRAKE	BRAKE	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	1	0	0	1	0	0	BRAKE	BRAKE	LOW	LOW	1	1	OFF	OFF
1	0	>10.4 V	0	1	0	0	0	0	COAST	COAST	ON	ON	0	0	ON	OFF
1	0	>10.4 V	0	X	1	0	0	0	COAST	COAST	LOW	HI	1	0	OFF	ON
1	0	>10.4 V	0	0	0	0	0	0	COAST	COAST	LOW	LOW	1	1	OFF	OFF
0	0	>2 V	X	X	X	X	X	X	XXX	COAST	LOW	HI	1	0	OFF	ON
0	1	>2 V	X	X	X	X	X	X	XXX	BRAKE	LOW	LOW	1	1	OFF	OFF



NOTES: All external FETs are located in TPIC150x drive array.
During linear drive, the digital/PWM drive is disconnected from the one-shot and tied to supply rail. Also, the IFILTER or the output of the OTA is tied to linear drive.
During PWM mode, output of the OTA or IFILTER is disconnected from the analog/linear drive, and digital drive is connected to the one-shot output.

FIGURE B-1: Typical Application

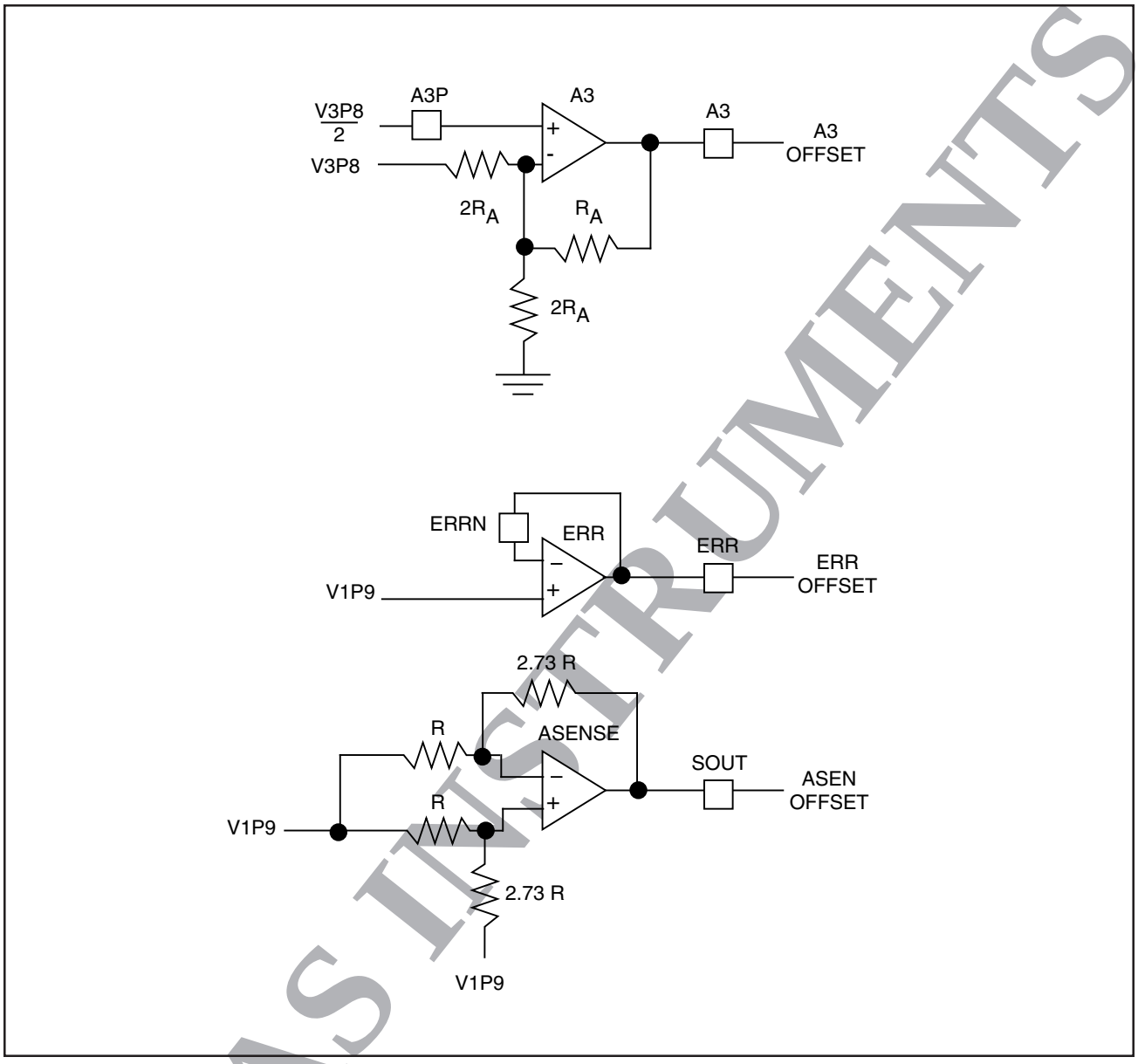


FIGURE C-1: TEST SETUP FOR SYSTEM OFFSET MEASUREMENT

TOTAL OFFSET CURRENT:

$$I_{IO} = \frac{\left((A3\ \ Offset)\left(\frac{R_F}{R_I}\right)\right) + (ASEN\ Offset) - (ERR\ Offset)}{2.73\ RSEN} \quad (1)$$

Where:

R_F = 13 kΩ

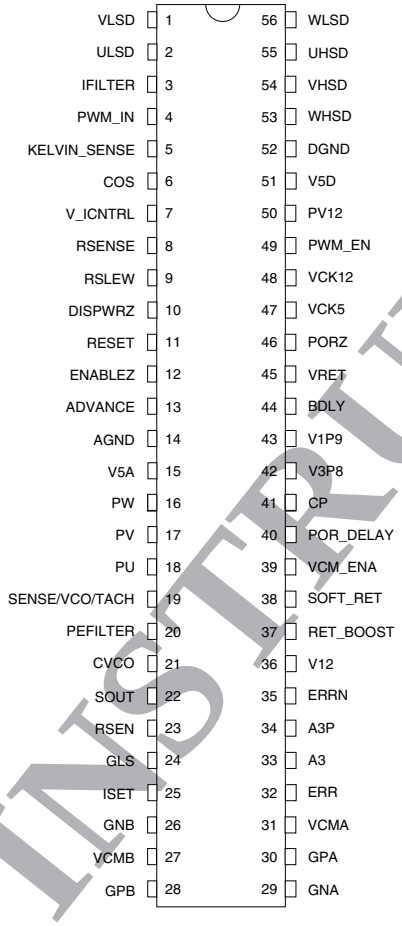
R_I = 15.4 kΩ

RSEN = 0.332 Ω

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



TLS2234

DL Package- Terminal Assignments

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
TLS2234	**56-Pin Servo-Combination Predriver**	**TLS2234CDLR**	**T2234CB**

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

TLS2271
SERVO AND SPINDLE PREDRIVER

June, 2000

DESCRIPTION

The SSI TLS2271 is a 56-pin TSSOP voice-coil actuator and spindle motor predriver. It is designed to drive a 3-phase sensorless motor and voice coil actuator with external NMOS power devices. The TLS2271 can interface with commonly-used micro-devices including digital signal processors (DSPs) via a 3-wire serial interface. An A/D converter provides 10-bit signal conversion. The device is intended for 12 V disk drive applications.

FEATURES

SERIAL PORT

- **20 MHz Register Read/Write**
- **6 MHz 10-bit Successive Approximation A/D converter**

VCM CONTROL

- **Full H-bridge Transconductance Loop**
- **Dual range, 10-bit current control D/A converter**
- **Class A-B Operation with External Discrete Power MOSFETs without a Sense FET**
- **Programmable Retract Voltage with Source/Sink Capability**

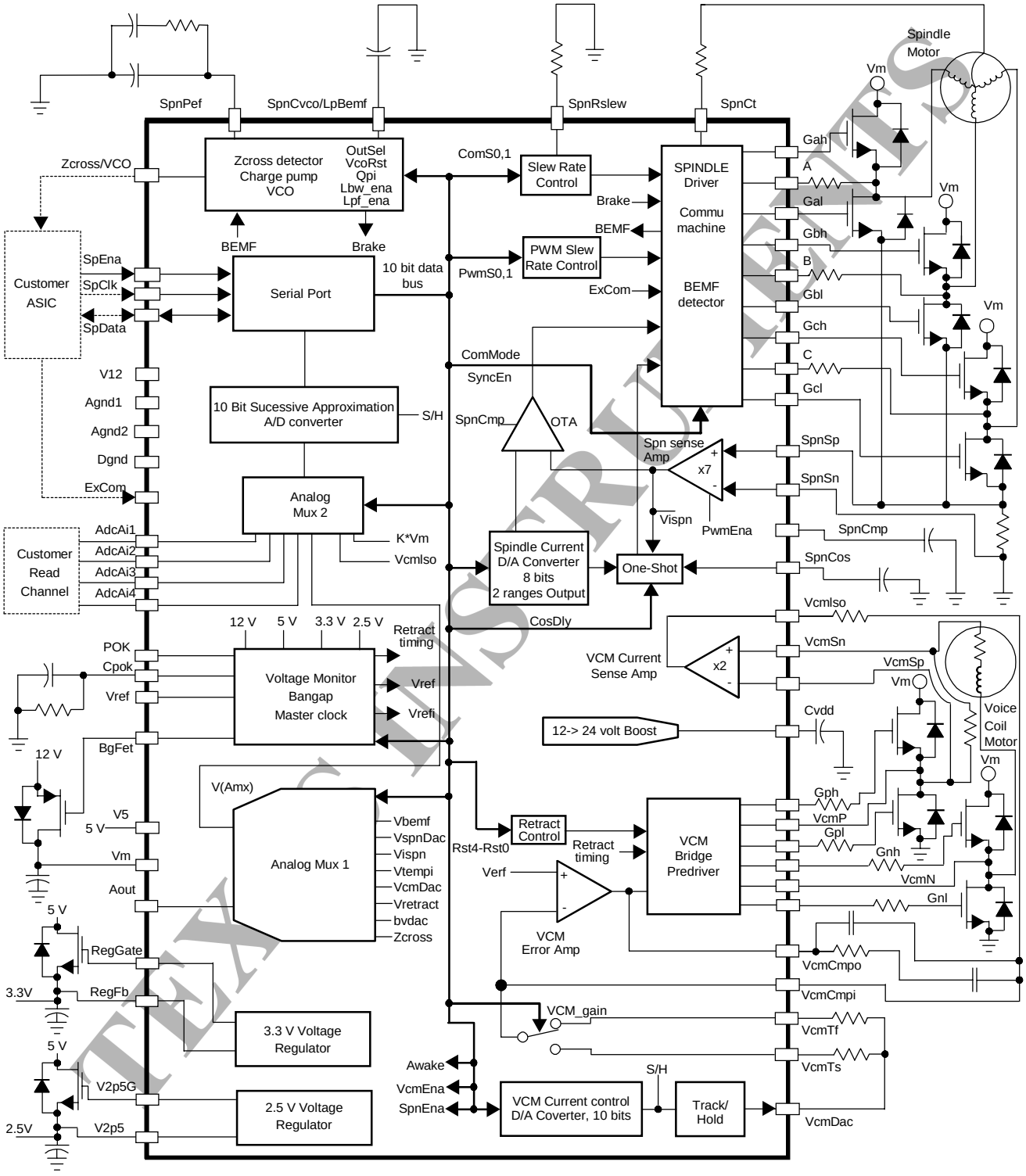
SPINDLE MOTOR PREDRIVER

- **Six-State Linear/PWM Transconductance Control Using External Power MOSFETs**
- **Programmable Constant-Off-Time PWM Current Control**
- **Dual Range, 8-bit Current Control D/A Converter**
- **Programmable commutation and PWM Slew Rates**
- **Internal VCO or External Commutation**
- **High Efficiency Synchronous Rectification**
- **Programmable Initial VCO Frequency setup**
- **BEMF or VCO Output**
- **Spindle Brake After Retract**

SUPPORT FUNCTIONS

- **3.3 V Linear Voltage Regulator**
- **2.5 V Linear Voltage Regulator**
- **Charge Pump (24 V) for driving NMOS FETs**
- **Voltage Monitor (2.5 V, 3.3 V, 5 V, and 12 V)**
- **Vm Shunt Regulator for Transient Protection**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI TLS2271 contains a serial port, a voice coil motor (VCM) predriver, a spindle predriver with Phase Lock Loop (PLL), a 2.5V regulator, a 3.3-V regulator, and other supporting functions including spindle brake, VCM retract control and voltage monitoring circuit. The chip has two modes: awake and asleep. The default power-up state is the sleep mode.

SERIAL PORT

The serial port is a bi-directional communication port used for reading and writing to internal digital registers of the TLS2271. The port has a three-wire external connection, consisting of: serial port enable (SpEna), data transfer clock (SpClk), and data (SpData). Each read or write operation consists of 6 bits of address (with one read/write bit) and 10 bits of data. The order of transfer is the 6-bit address with the LSB as the first bit followed by the 10-bit data word. The address bits contain a one-bit R/W indicator. Depending on whether the indicator is high or low, the data word has two orders of bit sequence. When reading (R/W bit high), the MSB of data goes first; when writing (R/W low), the LSB goes first. All SpData bits are recognized on the positive edge of each clock; except when reading, the data bits are latched out on the negative edge of the clock. At the end of each transfer SpEna should be deasserted. The serial port clock can operate up to a maximum of 20 MHz for register reads and writes, and 6 MHz for analog-to-digital conversions (A/D).

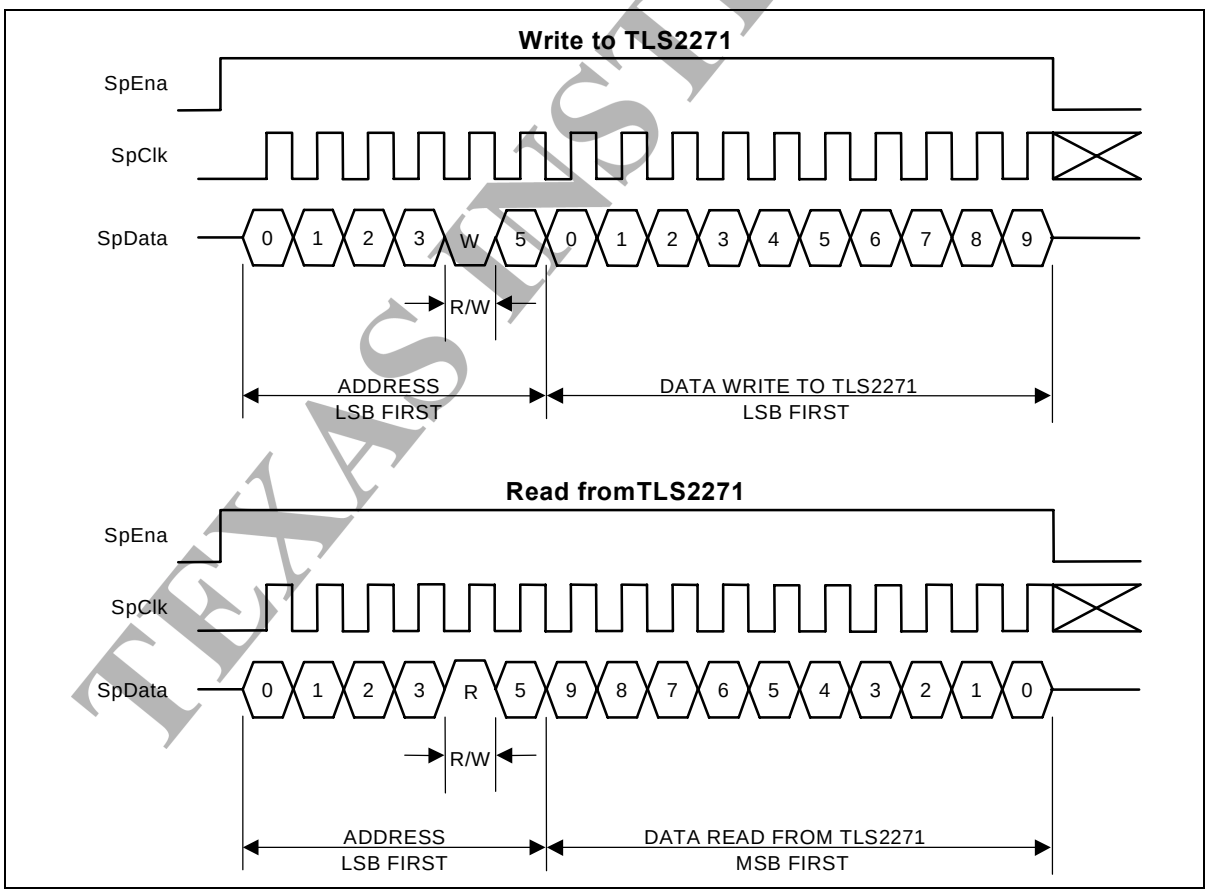
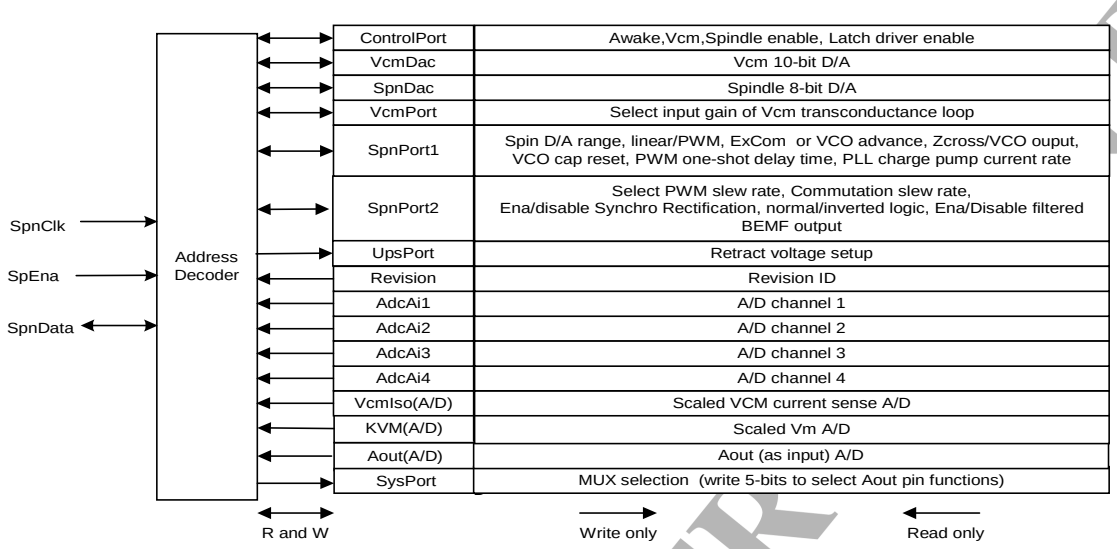


FIGURE 1: Read and Write Timing Sequence

TABLE 1: Digital Registers



The TLS2271 chip has 17 digital registers which can be accessed by the serial port (see Table 1). Two of the registers are “write only,” nine are “read only,” and six are bi-directional.

VCM PREDRIVER

The TLS2271 provides the gate drive signals to control external power FETs. It uses a transconductance loop driven by a 10-bit D/A converter to control the VCM current. A current sense amplifier is used to provide a gain for the feedback. A two-range VCM D/A-gain is selected through a serial port by a bit, fitting the different needs of VCM seeks and track-follow operations.

The VCM predriver has two modes of operation, normal (linear) and retract. The retract mode is activated by the falling edge of signal POK. The retract time-duration is determined by the voltage time constant at pin Cpok.

VCM ERROR AMPLIFIER

During linear operation, the VCM current command is applied through the VCM error amplifier. Resistor/capacitor components may be used to provide loop compensation. The error amplifier has an internal clamp to make the voltage across the compensation zero when the VCM loop is disabled.

VCM BRIDGE PREDRIVER

The VCM bridge predriver amplifies the output of the VCM error amplifier. The bridge predriver output, with a gain of 8, is applied across pins VcmP and VcmN, accompanied by four power-driving gate-signals. The gate signals drive the external MOS FETs of an H-bridge that operates in the Class B mode. The TLS2271 has an internal H-bridge that operates in the Class AB mode. This reduces quiescent energy consumption and improves the crossover linearity of VCM current. When the current of VCM is small, the internal H bridge is used to drive the motor. Otherwise, the external H bridge is turned on. The predriver does not require any external sense FET.

RETRACT FUNCTION

The retract is started when signal POK goes low. Once started, the TLS2271 stays in the retract mode for a selected time period (Tretract) and then goes into the brake mode with retract disabled. The TLS2271 continues braking until the Cvdd capacitor is discharged or until the power supply returns. The retract voltage is selected through the serial port. The TLS2271 actively controls the voltage on pin VcmP, relative to ground, during the retract. An external diode or FET is used to isolate 12-V power supply. The TLS2271 provides a pin (BgFet) for the gate control of the external blocking FET.

CURRENT SENSE AMPLIFIER

VCM current is sensed by a small series resistor across inputs VcmSn and VcmSp . The voltage drop across the resistor is amplified by the VCM current sense differential amplifier with a gain of two. The amplifier output voltage VcmIso is proportional to the VCM current. The VcmIso signal is externally fed back to the VCM error amplifier.

SPINDLE MOTOR PREDRIVER

The TLS2271 provides gate drive signals for the spindle motor that control external power FETs. Based on the BEMF zero crossing of the undriven phase, the TLS2271 controls the commutation sequence of the motor, by either an external digital signal applied to ExCom pin, or an internal signal from Voltage Controlled Oscillator (VCO). A transconductance loop is used to maintain the desired spindle motor current specified by the spindle motor D/A converter.

COMMUTATION STATES

The commutation states are defined in Table 2. When the TLS2271 spindle driver is enabled (SpnEna = 1), it comes up in the brake mode (commutation state 0).

LINEAR AND PWM MODE

TLS2271 spindle motor operates in one of two modes, a linear mode or a "constant off-time" PWM mode. The two modes are selected by a register (SpnPort1) through the serial port. In both modes, the external "high side drivers" are operated as on/off switches based on the commutation state. The “low side drivers” are linear or PWM controlled, depending on the state of the PwmEna bit in SpnPort1.

The TLS2271 has an 8-bit D/A converter (SpinDac) to command the spindle transconductance loop. In both spindle motor operating modes, a spindle current error signal is created by comparing the output of the spindle D/A converter with the current feedback signal from the spindle current sense amplifier. The SpinDac register has two ranges of output that are selected through the serial port.

In the linear mode, the error signal is amplified and is used to control the gates of the low side driver of the external three-phase bridge.

In the PWM mode, the error signal goes to a one-shot function block to create a PWM switching signal. When the current feedback signal is greater than the SpinDac output voltage, the low side driver is turned off for a constant off-time. The constant off-time is selected by an external capacitor at pin SpnCos and the CosDly bit in digital register SpnPort1.

PHASE DETECTOR

The TLS2271 has a spindle BEMF phase detector. The detector outputs source or sink current pulses to an external compensation network at pin SpnPef.

TABLE 2: Commutation States/Sequence

OMMUTATION STATE	PHASE A	PHASE B	PHASE C	COMMENTS
0	H	H	H	Brake Mode (Default)
1	L	H	Z	
2	L	Z	H	
3	Z	L	H	
4	H	L	Z	
5	H	Z	L	
6	Z	H	L	
7	Z	Z	Z	SpnEna=0

The voltage at this pin, V(SpnPef) is used to control the frequency of the Voltage Controlled Oscillator (VCO). Initial value of V(SpnPef) can be set using UpsPort register when VcoRst bit of SpnPort1 is 1. The phase detector and VCO form a Phase Lock Loop (PLL) that controls the commutation of the spindle motor when the VCO commutation is used.

COMMUTATION SLEW RATE AND PWM SLEW RATE

The commutation slew rate and PWM slew rate both depend on the selection of the external slew rate resistor (Rslew) at pin SpnRslew. Once the resistor value is fixed, individual slew rates can be selected through the serial port. There are four options for both PWM and commutation slew rates. The setup for PWM slew rate is not independent. When the spindle motor is in the PWM mode, the fastest commutation slew rate has to be selected.

INTERNAL AND EXTERNAL COMMUTATION

The TLS2271 can control spindle commutation by an external or internal signal. When the ComMode bit in the SpnPort1 register is set to 0, the ExCom pin is used to input an external triggering signal for commutation. Otherwise, the internal VCO is used for commutation. The commutation triggering is edge sensitive, depending on the state of the ComSel bit in the SpnPort1 register. If the ComSel bit is set to 0, only the rising edge of the signal causes a commutation; otherwise, every edge (rising or falling) triggers a commutation. The polarity of the triggering signal can be inverted by setting the ComPh bit in the SpnPort2 register to 1. If the Lpf_Ena bit in the SpnPort2 register is set to 1, the TLS2271 can output a low-pass filtered BEMF signal on pin SpnCvco/LpfBemf and the VCO function of the TLS2271 is automatically disabled. The commutation can then be triggered from pin ExCom by setting the ComMode bit to 0. The low-pass filter consists of an external capacitor at pin SpnCvco/LpBemf and a 5 kΩ internal resistor.

The VCO or BEMF Zero Cross (Zcross) signal is output on pin Zcross/VCO when the OutSel bit in the SpnPort1 register is 1 or 0. The Zcross signal can also be multiplexed out at pin Aout.

SUPPORT FUNCTIONS

The TLS2271 support functions include a 10-bit successive approximation A/D converter, a 2.5-V voltage-regulator, a 3.3-V voltage regulator, and a voltage monitor. A built-in shunt regulator connected to pin Vm safeguards the chip against a high voltage surge.

A/D CONVERTER

The 10-bit successive approximation A/D converter is used to perform up to 6 MHz of analog-to-digital conversion. It has internal sample/hold circuitry since it uses the 10-bit VCM D/A converter. The converter can be multiplexed to five external and 11 internal analog signals through Analog Mux 1 and Analog Mux 2. This A/D converter can be used to interface with the read channel device for servo demodulation. Channel selection and conversion occur in one serial port I/O cycle.

VOLTAGE MONITORING CIRCUIT

The TLS2271 uses the Power OK (POK) signal as the voltage monitoring output. The 5-V and 12-V supplies, and the 2.5-V and 3.3-V voltage-regulator outputs are monitored by internally dividing them to appropriate values and comparing these values with their corresponding threshold levels. POK being high indicates that the voltages have all risen above their respective thresholds and have remained above the thresholds for a selected period of time. The selected time period is determined by the capacitor and resistor on pin CPOK. Once POK is high and any voltage goes below its corresponding threshold, the POK signal will go to its low state, which will reset the TLS2271 chip. The POK signal is an open drain with a 10 kΩ internal pull-up resistor. Commanding TLS2271 into the sleep state does not affect the contents of registers.

THERMAL SENSE CIRCUIT

An internal temperature sensor (diode) can be used to monitor the junction temperature of the TLS2271. The internal temperature diode is connected to the Aout multiplexer and can be measured on the Aout pin or digitally converted through the A/D. The signal name is Vtempi.

2.5 AND 3.3 VOLT REGULATORS

The 2.5-V and 3.3-V regulators convert the 5 V power supply voltage to 2.5 V and 3.3 V respectively, and maintains these voltages throughout the operation period of the TLS2271.

AOUT PIN

The Aout pin allows the external measurement of several TLS2271 internal multiplexed analog signals. The Aout pin can also be configured to be used as a spare external input to the TLS2271 A/D converter. The Aout pin signal is selected by the SysPort register through the serial port.

PIN DESCRIPTION

POWER SUPPLIES

PIN	NAME	TYPE	DESCRIPTION
15	V12	Analog In	+12 Volt Power Supply (for internal voltage monitor)
34	Vm	Power In	Motor Supply Voltage through the Block FET (or Block Diode)
49	V5	Power In	+5 Volt Power Supply
33	Agnd1	Ground	Analog Signal Return
12	Agnd2	Ground	Analog Signal Return
46	Dgnd	Ground	Digital Signal Return

SERIAL PORT

43	SpEna	Logic In	Serial I/O Port Select on High
44	SpClk	Logic In	Serial I/O Clock
45	SpData	Logic I/O	Serial Port I/O Data

VCM DRIVER

40	Vref	Analog Out	DC Voltage Reference Output, Typical Value 2 V
21	VcmP	Power Out	VCM Positive Output
22	VcmN	Power Out	VCM Negative Output
23	VcmSp	Analog In	VCM Current Sense Positive Input
24	VcmSn	Analog In	VCM Current Sense Negative Input
29	VcmTs	Analog In	VCM Seek Input
30	VcmTf	Analog In	VCM Track-Following Input
31	VcmCmpi	Analog In	VCM Compensation Input
28	VcmCmpo	Analog Out	VCM Compensation Output
32	VcmDac	Analog Out	VCM D/A Converter Output
26	VcmIso	Analog Out	VCM Current Sense Amplifier Output
17	Gnh	Analog Out	VCM High side driver Gate, Negative Side
18	Gnl	Analog Out	VCM Low side driver Gate, Negative Side
19	Gpl	Analog Out	VCM Low side driver Gate, Positive Side
20	Gph	Analog Out	VCM High side driver Gate, Positive Side

SPINDLE MOTOR DRIVER

PIN	NAME	TYPE	DESCRIPTION
1	Gah	Analog Out	Spindle Phase A Connection, High Side Gate
56	Gbh	Analog Out	Spindle Phase B Connection, High Side Gate
55	Gch	Analog Out	Spindle Phase C Connection, High Side Gate
4	Gal	Analog Out	Spindle Phase A Connection, Low Side Gate
3	Gbl	Analog Out	Spindle Phase B Connection, Low Side Gate
2	Gcl	Analog Out	Spindle Phase C Connection, Low Side Gate
5	SpnSp	Analog In	Spindle current sense Positive Input
6	SpnSn	Analog In	Spindle current sense Negative Input, Kelvin Ground
7	SpnCmp	Analog In	Spindle transconductance loop compensation in Linear Mode
8	SpnCos	Analog In	Spindle Timing Cap for Constant Off-Time PWM
9	SpnCvco/LpBemf	Analog In	Spindle VCO Timing Cap/Low Pass Filtered BEMF Output
10	SpnPef	Analog I/O	Spindle Phase Lock Loop Compensation
11	SpnRslew	Analog In	Spindle Slew Rates Control Resistance
47	Zcross/VCO	Logic Out	Spindle Back EMF Detect Output/VCO Output
48	ExCom	Analog In	External Input for Spindle Commutation
51	SpnCt	Analog In	Spindle Motor Center-tap
54	A	Analog In	Spindle Phase A Connection, BEMF Sense
53	B	Analog In	Spindle Phase B Connection, BEMF Sense
52	C	Analog In	Spindle Phase C Connection, BEMF Sense

SUPPORT FUNCTIONS

14	Cvdd	Analog I/O	Charge Pump Storage Cap
41	POK	Logic I/O	Power OK Output/Retract Trigger Input
42	Cpok	Analog In	Retract Delay Capacitor
35	AdcAi1	Analog In	External analog Input to A/D
36	AdcAi2	Analog In	External analog Input to A/D
37	AdcAi3	Analog In	External analog Input to A/D
38	AdcAi4	Analog In	External analog Input to A/D
25	RegGate	Analog Out	Gate Control of 3.3 V Regulator
27	RegFB	Analog Out	Feed Back from 3.3 V Regulator
39	V2P5G	Analog Out	Gate Control of 2.5 V Regulator
50	V2P5	Analog Out	Feed Back from 2.5 V Regulator
13	BgFet	Logic Out	Block FET Gate
16	Aout	Analog Out	Analog Test Output/ Extra AD Input

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING	UNIT
V5	6	V
V12	13.8	V
Max Voltage on VcmP, VcmN, A, B, C, Vm	15	V
Storage Temperature	– 45 to 150	°C
Solder Temperature (10 Second Duration)	245	°C
ESD Discharge (all pins, Charge Device Model)	1000	V

RECOMMENDED OPERATION CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended ranges.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
V5		4.5	5	5.5	V
V12		10.8	12	13.2	V
Ambient Temperature		0		70	°C

DC CHARACTERISTICS

Sleep current (5V)	Awake = 0		0.5	0.85	mA
Sleep current (12V)	Awake = 0		1.5		mA
Operating supply current (5V)	Awake=1, SpnEna=0, VcmEna=0		6	15	mA
Operating supply current (12V)	Awake=1, SpnEna=0, VcmEna=0		6	15	mA
Charge pump voltage	Cvdd = 0.1µF, Awake=1, SpnEna=0, VcmEna=0	18.9	22.0	24.7	V
Power dissipation			0.25	1	W

REFERENCE VOLTAGE

Vref	0 to 100 µA load	1.88	2	2.12	V
Vref capacitive load				15	pF
Vrefi	No Load	2.24	2.36	2.48	V

NOTE: Vrefi is an internal reference voltage of TLS2271 for various functions.

SERIAL PORT (Digital Input Table)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SpClk frequency	Excluding A/D conversion			20	MHz
SpClk duty cycle		40	50	60	%
SpData setup time, Data stable before positive edge of SpClk		10			ns
SpData hold time, Data stable after positive edge of SpClk		10			ns
High level input voltage, SpEna, SpClk, SpData		2.2			V
Low level input voltage, SpEna, SpClk, SpData				0.8	V
High level input current, SpEna, SpClk, SpData				2	µA
Low level input current, SpEna, SpClk, SpData				2	µA
Input capacitance	Specified By Design (SBD)			13	pF

SERIAL PORT (Digital Output Table)

Access time, Data stable after negative edge of SpClk	Data field read from TLS2271			38	ns
High level output voltage, SpData	Io = 100 µA	V5-0.8			V
Low level output voltage, SpData	Io = 100 µA			0.4	V
Capacitance load, SpData	SBD			50	pF

DIGITAL REGISTERS

R/W addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
20/30h	0	0	0	0	0/1	1	**Control Port**		Chip control register
							D5-D4		D4 is a spare bit. D5 is TI reserved for Cvdd internal cap test.
							D3	Spare	
							D2	SpnEna	0=Spindle driver disabled, 1=Spindle driver enabled
							D1	VcmEna	0=VCM driver disabled, 1=VCM driver enabled
							D0	Awake	0=Chip asleep, 1=Chip awake

R/W addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
28/38h	0	0	0	1	0/1	1	**VcmDac**		Vcm loop input register
							D9-D0	Vvd9-Vvd0	

R/W addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
24/34h	0	0	1	0	0/1	1	**SpnDac**		Spindle motor loop input register
							D7-D0	Vsd7-Vsd0	

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
3Eh	0	1	1	1	1	1	**Revision**		Revision identification register
							D2	Rev2	Revision ID 2
							D1	Rev1	Revision ID 1
							D0	Rev0	Revision ID 0

Notes: 1. D2D1D0= 101 for TLS2271.

W addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
2Eh	0	1	1	1	0	1	**UpsPort**		Retract voltage register
							D4-D0	Rst4-Rst0	

DIGITAL REGISTERS (continued)

R/W addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
2C/3Ch	0	0	1	1	0/1	1	**VcmPort**		Gain control register for Vcm loop
							D1	Spare	
							D0	Vcm Gain	Gain Control, 0=TF, 1=Ts

R/W addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Description	Details
22/32h	0	1	0	0	0/1	1	**SpnPort1**			Spindle control register 1
							D7	Qpi	PLL charge Pump Current	0=7 μA, 1=14 μA
							D6	CosDly	PWM constant off delay	0=normal, 1=1/3 normal time
							D5	VcoRst	VCO input reset	0=not reset, 1=reset V(SpnPef) to equal retract voltage specified by the UpsPort register
							D4	OutSel	Zcross/VCO output	0=Zcross, 1=VCO
							D3	ComSel	Commutation Logic	0=One edge trigger commutation, 1=Two edges trigger commutation
							D2	Com Mode	Commutation Control	0=Ext Adv, 1=Vco adv.
							D1	Pwm Ena	Spindle Current Control	0=linear, 1=PWM
							D0	Spn Range	Spindle Dac Range	0=low, 1=high

DIGITAL REGISTERS (continued)

(Data Part comes from Aout Register)																	
							Port Name										
Whex Ad A0 drA1 Pa A2 RtA3 A4 A5							**Syst Port**	Data Part (Aout Selection) hex	D4				D0	Aout pin state (input, output, or to be in tri-state)	internal A/D input	Description
26	0	1	1	0	0	1		00	0	0	0	0	0	Tri_State	Vbemf	Detected BEMF voltage
26	0	1	1	0	0	1		01	0	0	0	0	1	Tri_State	VspnDac	Spin DAC output
26	0	1	1	0	0	1		02	0	0	0	1	0	Tri_State	Vispn	Scaled spin current sense
26	0	1	1	0	0	1		03	0	0	0	1	1	Tri_State	Vtempi	Internal temperature diode voltage
26	0	1	1	0	0	1		04	0	0	1	0	0	Tri_State	Vretract	Retract voltage reference
26	0	1	1	0	0	1		05	0	0	1	0	1	Tri_State	VcmDac	VCM DAC from VcmDac sample/hold
26	0	1	1	0	0	1		06	0	0	1	1	0	Tri_State	bvdac	Buffered high speed DAC output
26	0	1	1	0	0	1		07	0	0	1	1	1	Tri_State	Zcross	ZCROSS signal
26	0	1	1	0	0	1		08	0	1	0	0	0	Tri_State		
26	0	1	1	0	0	1		10	1	0	0	0	0	Vbemf (output)	Vbemf	Detected BEMF Voltage
26	0	1	1	0	0	1		11	1	0	0	0	1	VspnDac (output)	VspnDac	Spin Dac Output
26	0	1	1	0	0	1		12	1	0	0	1	0	Vispn (output)	Vispn	Scaled Spin Current Sense
26	0	1	1	0	0	1		13	1	0	0	1	1	Vtempi (output)	Vtempi	Internal Temperature Diode voltage
26	0	1	1	0	0	1		14	1	0	1	0	0	Vretract (output)	Vretract	Retract Voltage Reference
26	0	1	1	0	0	1		15	1	0	1	0	1	VcmDac (output)	VcmDac	VCM DAC from VcmDac sample/hold
26	0	1	1	0	0	1		16	1	0	1	1	0	bvdac (output)	bvdac	Buffered high speed DAC output
26	0	1	1	0	0	1		17	1	0	1	1	1	Zcross (output)	Zcross	ZCROSS signal
26	0	1	1	0	0	1		18	1	1	0	0	0	input	Aout Pin	Extra external ADC Input

DIGITAL REGISTERS (continued)

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
31h	1	0	0	0	1	1	**AdcAi1(A/D)**		A/D register 1
							D9-D0	A1i9-A1i0	

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
39h	1	0	0	1	1	1	**AdcAi2(A/D)**		A/D register 2
							D9-D0	A2i9-A2i0	

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
35h	1	0	1	0	1	1	**AdcAi3(A/D)**		A/D register 3
							D9-D0	A3i9-A3i0	

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
3Dh	1	0	1	1	1	1	**AdcAi4(A/D)**		A/D register 4
							D9-D0	A4i9-A4i0	

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
33h	1	1	0	0	1	1	**VcmIso(A/D)**		Vcm current sense A/D register
							D9-D0	VIso9-VIso0	

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
37h	1	1	1	0	1	1	**KVm(A/D)**		Scaled Vm voltage A/D register
							D9-D0	KVm9-KVm0	

R addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Details
3Fh	1	1	1	1	1	1	**Aout(A/D)**		Aout (as input) A/D register
							D9-D0	Aout9-Aout0	

DIGITAL REGISTERS (continued)

R/W addr	A0	A1	A2	A3	A4	A5	Port Name	Bit Name	Description	Details
2A/3Ah	0	1	0	1	0/1	1	**SpnPort2**			Spindle control register 2
							D7	Lpf_Ena	BEMF low-pass filter enable	0= pin 9 as SpnCvco pin, 1= pin 9 as filtered Bemf output
							D6		TI Reserved	Always set to 0
							D5	ComPh	Invert the commutation logic	0= normal, 1= inverted logic
							D4	SyncEn	Synchronous Rectification	0= disable, 1= enable
							D3	ComS1	MSB for Commutation Slew rate	See *Commutation Slew Rate Selection* table on page 20
							D2	ComS0	LSB for Commutation Slew rate	
							D1	PwmS1	MSB for PWM Slew rate	See *PWM Slew Rate Selection* table on page 20
							D0	PwmS0	LSB for PWM Slew rate	

10-BIT VCM D/A CONVERTER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Zero Scale Voltage	Code = 00 hex	0	0	0.1	V
Full scale Output Voltage	Code = 3FFhex	1.97	2	2.04	x Vref
Integral Nonlinearity Error (INL)		-4		4	LSB
Differential Nonlinearity Error (DNL)	1FD to 200hex	-4		17	mV
	1FF to 200hex			8	mV
S/H drift	During ADC conversion			140	V/s
Settling Time	1/4 LSB, SBD		35		ns

NOTES: 1. DNL is defined as the product of step size in number of LSBs and the ideal single step voltage of (4V/1024) .

2. INL is defined as the deviation from the ideal steps between the real (measured) voltage end points.

VCM RETRACT

VCM retract voltage is selected by UpsPort register through the serial port.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Retract voltage range	VcmP to Ground, at Vm=5V	0.693		2.596	V
	UpsPort	9		32	LSB
Retract voltage accuracy		–10		+10	%
Minimum Vm for retract		5			V
Tretract coefficient (Kr)	Note 1	0.935	1.1	1.265	
Cvdd Pin Leakage (Note 2)	12V power supply low, retract cycle complete, Cvdd = 0.1µF, SBD			50	nA

NOTES: 1. Tretract = Kr * Rpok * Cpok, Rpok and Cpok are external components on pin Cpok.

2. Drain determines how long the brake is on after retract.

VCM LOOP CURRENT CONTROL SPECIFICATION (NOTE)

Full scale (FS) accuracy, digital DAC input to current output	0% external components. Uncalibrated offset current subtracted out	–9	0	9	%
Current sense amp gain		1.98	2	2.02	
Offset Current (uncalibrated)	DAC = 200 hex, Rsen = 10 Ω, Rf = 22.1K, Ri=22.1K, Rvcm=500 Ohm			1.6	mA
Rdson, VcmGain switch			850		Ω

NOTE: The VCM offset current is defined as the current in the VCM when 200h is written to the VCM DAC. The Ri and Rf are resistors from VcmDac pin and VcmIso pin to VcmCmpi pin, respectively (see the Block Diagram on page 2).

VCM BRIDGE PREDRIVER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Voltage Gain	(VcmP-VcmN)/VcmCmpo, SBD		8		
Unity Gain Bandwidth	SBD	2			MHz
Internal Class AB quiescent current	SBD		2		mA
Maximum Output at VcmP, VcmN			15		mA
High Side Gate, Voltage	VcmCmpi = 0 V or 3V	18.1		24.7	V
Low Side Gate, Voltage	VcmCmpi = 0 V or 3V	9.8		13.5	V
High Side Gate, Current			50		µA
Low Side Gate, Current			50		µA

VCM ERROR AMPLIFIER

Gain-Bandwidth Product	SBD	0.75	2		MHz
Power Supply Rejection Ratio (PSRR)		60			dB
Capacitive Load				50	pF
Resistive Load		5			kΩ

VCM CURRENT SENSE AMPLIFIER

Current sense amp gain		1.98	2	2.02	
Gain-Bandwidth Product	SBD	0.75	2		MHz
Common Mode Gain	DC test only	-0.7		0.7	%
Power Supply Rejection Ratio (PSRR)	DC test only	60			dB
Input Common Mode Range		-0.3		Vm+0.8	V
Capacitive Load				50	pF
Resistive Load		5			kΩ

EXTERNAL COMMUTATION (EXCOM)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
High level input voltage, ExCom		2.2			V
Low level input voltage, ExCom				0.8	V
High level input current, ExCom	ExCom = 5 V			2	µA
Low level input current, ExCom	ExCom = 0 V			2	µA

VOLTAGE CONTROLLED OSCILLATOR (VCO)

Offset Frequency	Lpf_Ena=0, Vin=0V, Cvco=10nF	4	25	46	Hz
VCO Average Gain (Note)	Lpf_Ena=0, Cvco=10nF	700	980	1300	Hz/V
Cvco Charge/Discharge Current	Lpf_Ena=0, Vin=0 V	155	500	905	nA
Input Control Range	Lpf_Ena=0	0		V5	V

NOTE: Kvco =[f(5V)-f(0V)]/5V

BEMF ZERO CROSS (ZCROSS/VCO PIN)

High level Output		Vcc5-0.8			V
Low level output				0.4	V
BEMF Detection Offset		-50		50	mV
BEMF Sense Gain		0.61	0.643	0.668	

SPINDLE CURRENT SENSE AMPLIFIER

Deadband Voltage at Output	SpnSn=0, SpnSp=0	40	54	75	mV
Sense Amplifier Gain		6.7		7.0	V/V

LINEAR CONTROL

OTA Gain	SpinDac=80H	1.15	1.50	1.9	mA/V
OTA Current Range		–1.1		1.1	mA

COMMUTATION SLEW RATE SELECTION

ComS1	ComS0	Modifying effect	Comments
0	0	Commutation baseline slew current setting	Fastest commutation slew rate
0	1	Commutation baseline slew current multiplied by 1/2	
1	0	Commutation baseline slew current multiplied by 1/4	
1	1	Commutation baseline slew current multiplied by 1/8	Slowest commutation slew rate

NOTE: Commutation baseline slew current is defined to be (8*Vrefi)/(5*Rslew).

PWM SLEW RATE SELECTION

PwmS1	PwmS0	Modifying effect	Comments
0	0	PWM baseline slew current setting	Slowest PWM slew rate
0	1	PWM baseline slew current multiplied by 2	
1	0	PWM baseline slew current multiplied by 4	
1	1	PWM baseline slew current multiplied by 8	Fastest PWM slew rate

NOTES: 1. PWM baseline slew current is defined to be (6*Vrefi)/Rslew.
2. In PWM mode, the Commutation Slew Rate must be set to be the fastest (ComS1=0, ComS0=0).

SLEW RESISTOR SELECTION (RSLEW)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Rslew range		23		240	kΩ

NOTE: The Rslew range provides the maximum and minimum values. The actual value of Rslew should be chosen within this range, according to the power FETs used, in order to have proper linear and PWM operations. In general, the bigger the power FET, the smaller the Rslew should be.

SPINDLE DRIVER GATE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
High Side Gate Output Voltage	HSD off			0.7	V
	HSD on	Vcvdd-0.8		24.7	V
Low Side Gate Output Voltage	LSD off			0.7	V
	LSD on	9.8		13.5	V
High Side Gate Output Current	Islew=10 µA				
	HSD on, V(ghx)=8V		-1.4		mA
	HSD off, V(ghx)=16V		3.0		mA
	HSD off, V(ghx)=8V				
	ComS0 = 0, ComS1 = 0		16		µA
	ComS0 = 1, ComS1 = 0		8		µA
	ComS0 = 0, ComS1 = 1		4		µA
	ComS0 = 1, ComS1 = 1		2		µA
	Islew=100 µA				
	HSD on, V(ghx)=8V		-1.7		mA
	HSD off, V(ghx)=16V		3.0		mA
	HSD off, V(ghx)=8V				
	ComS0 = 0, ComS1 = 0		160		µA
	ComS0 = 1, ComS1 = 0		80		µA
	ComS0 = 0, ComS1 = 1		40		µA
	ComS0 = 1, ComS1 = 1		20		µA
	HSD off, locked, V(ghx)=8V		5.1		mA
Low Side Gate Output Current	Islew=10 µA				
	LSD on		-550		µA
	LSD off, off state				
	V(glx)=5V, V(ph)=0V		2.7		mA
	V(glx)=5V, V(ph)=V12				
	ComS0 = 0, ComS 1 = 0		16		µA
	ComS0 = 1, ComS 1 = 0		8		µA
	ComS0 = 0, ComS 1 = 1		4		µA
	ComS0 = 1, ComS 1 = 1		2		µA
	Locked, V(glx)=5V, V(ph)=12V		3		mA
	Locked, V(glx)=5V, V(ph)=0V		4.6		mA
	LSD off, PWM mode, V(glx)=5V				
	PwmS0 = 0, PwmS1 = 0		65		µA
	PwmS0 = 1, PwmS1 = 0		130		µA
	PwmS0 = 0, PwmS1 = 1		260		µA
	PwmS0 = 1, PwmS1 = 1		530		µA

SPINDLE DRIVER GATE (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Low Side Gate Output Current	Islew=100 µA				
	LSD on		-4.8		mA
	LSD off, off state				
	V(glx)=5V, V(ph)=0V		2.7		mA
	V(glx)=5V, V(ph)=V12				
	ComS0 = 0, ComS 1 = 0		160		µA
	ComS0 = 1, ComS 1 = 0		80		µA
	ComS0 = 0, ComS 1 = 1		40		µA
	ComS0 = 1, ComS 1 = 1		20		µA
	Locked, V(glx)=5V, V(ph)=12V		3.0		mA
	Locked, V(glx)=5V, V(ph)=0V		4.6		mA
	LSD off, PWM mode, V(glx)=5V				
	PwmS0 = 0, PwmS1 = 0		0.62		mA
	PwmS0 = 1, PwmS1 = 0		1.24		mA
	PwmS0 = 0, PwmS1 = 1		2.4		mA
	PwmS0 = 1, PwmS1 = 1		4.9		mA

SPINDLE DRIVER PHASE (A, B, C)

Phase Input Current	V(ph)=12 V, SpnEna=0	200		470	µA
	V(ph)=12, SpnEna=1, Phase is High Z	400		730	µA
Center Tap Input Current	V(ct)=12 V, SpnEna=0, Phases disabled	200		470	µA

8-BIT SPINDLE D/A CONVERTER

Integral Nonlinearity Error (INL)		–1		1	LSB
Differential Nonlinearity Error (DNL)		-0.75		1	LSB
Zero Scale Voltage	Code=00 hex	0	0	0.04	V
Full scale Output Voltage	Code = FFhex	3.255		3.745	V
Low/High range ratio	SpnRange=0/1	38	40	42	%FS

NOTES: 1. DNL is defined as the deviation from an ideal 1 LSB step (1 LSB +/- DNL).

2. INL is defined as the deviation from the ideal steps between the real (measured) voltage end points.

PWM ONE-SHOT

Charge Current to SpnCos (Icos)	SpnEna = 1:				
	CosDly = 0	20	42	70	µA
	CosDly = 1	82	126	192	µA

NOTE: Offtime Tcos=Ccos*Vrefi/Icos. Ccos is the external capacitor on SpnCos pin.

PHASE DETECTOR (SPNPEF)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Voltage	ComMode = 0, VcoRst = 0			400	mV
	ComMode = 1, VcoRst = 1, UpsPort=1Fh	2.24		2.48	V
	VSpnpef = 1.0, 2.5, and V5-1.0 volts:				
Output Source/Sink Current	Qpi = 0	4.0	7	10.0	µA
	Qpi = 1	9.0	14	20.0	µA
Source/Sink Matching	Icharge/discharge	0.90	1	1.10	

SPINDLE LOOP CURRENT ACCURACY

Full Scale (FS) Current Accuracy (digital DAC input to current output)	0% Sense Resistor and High Gain Range of DAC	–9	0	9	%

VOLTAGE MONITOR

2.5 V POK threshold		1.8		2.1	V
2.5 V POK hysteresis			30		mV
3.3 V POK threshold		2.6	2.75	2.9	V
3.3 V POK hysteresis			10		mV
5V POK threshold		3.9	4.15	4.4	V
5V POK hysteresis			40		mV
12V POK threshold		8	8.5	9	V
12V POK hysteresis			40		mV
POK internal pull-up resistor			10		kΩ
Cpok charging current		3.6		6.1	µA
Tpok coefficient (Kpok)		1.125	1.5	1.875	
POK output low voltage	Ipok = 1mA			0.4	V
POK output high voltage	Ipok = 1µA	4.4			V
POK rise time (10% to 90%)	cpok=40Pf, SBD			1	µs

NOTE: Retract time Tpok=Kpok*Cpok/Ipok. Cpok is the external capacitor on Cpok pin.

10-BIT A/D CONVERTER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Serial clock frequency	During conversion			6	MHz
Input leakage current			0.01	2	µA
Input resistance	SBD	10	100		MΩ
Input capacitance	SBD		10	13	pF
Integral Nonlinearity error (INL)					LSB
Differential Nonlinearity error (DNL)					LSB
Zero scale voltage	Code = 00 hex	–0.1	0	0.1	V
Full scale voltage	Code = 3FF hex	3.72	4.00	4.28	V

EXTERNAL BLOCK FET

BGfet		18.9	21.8	24.7	V

2.5 V VOLTAGE REGULATOR

Regulated Output Voltage	Over full current range	2.25	2.5	2.75	V
Regulated Current Range	External FET, Ref only	0	150	650	mA
Load Capacitance		0	0.1	15	µF

3.3 V VOLTAGE REGULATOR

Regulated Output Voltage	Over full current range	3	3.3	3.6	V
Regulated Current Range	External FET, Ref only	0	150	650	mA
Load Capacitance		0	0.1	15	µF

AOUT AS OUTPUT PIN

Capacitive load				50	pF
Resistive load		1			MΩ

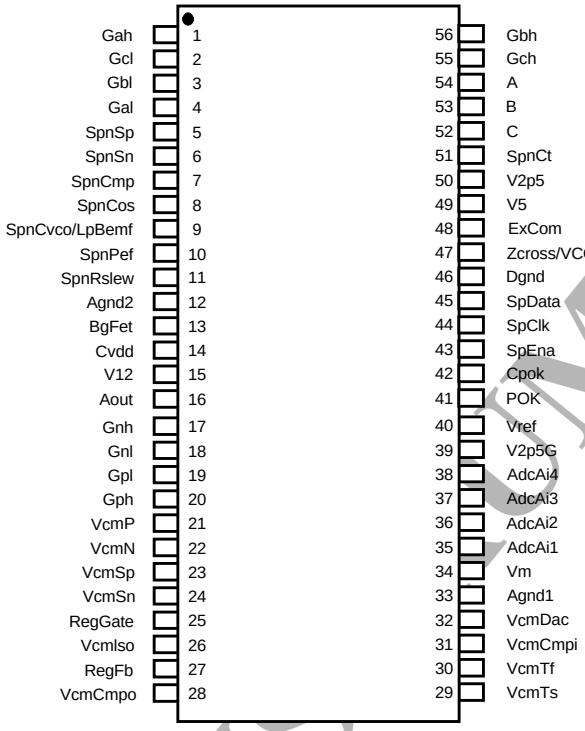
AOUT AS INPUT PIN

Input leakage current				2	µA
Input resistance	Pin-to-ground	10			MΩ
Input capacitance	Pin-to-ground			13	pF

VM SHUNT REGULATOR

Voltage	I=50 mA	14		17.5	V
Turn-On Delay (by simulation)	I=50 mA at 14.5 V		1.2		µs
Rdson	I=2A		1		Ω

PACKAGE PIN DESIGNATIONS



ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TLS2271 56-Lead TSSOP		

Texas Instruments Storage Products, 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

2000

DSP CORES

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Texas Instruments

- **T320C2700B0 Core Includes:**
  - **Central Processing Unit (CPU)**
  - **Memory Interface**
  - **Clock Interface**
  - **Test and Emulation Logic**
- **Divide-by-One Clock Input**
- **7.7-ns Instruction Cycle Time**
- **130 Million Instructions Per Second (MIPS) at 1.8-V Operation**
- **Power-Down (IDLE) Mode**
- **Low-Power Dissipation**
- **22-Bit Linear Address Reach, Program, and Data Space, Total Address Space Equal to 4M of 16-Bit Words**
- **16-Bit or 32-Bit Instruction Size**
- **Byte-Packing/Unpacking Operations With Byte-Indexing Into 16-Bit Words**
- **Register-to-Register Operations**
- **Code-Efficient Addressing Modes**
- **Fast Interrupt Response**
- **Single-Cycle Execution for Virtually All Instructions**
- **Eight-Stage Fully Protected Pipeline**
- **32-Bit Single-Cycle Read/Write Operations**
- **Modified Harvard Architecture**
- **Real-Time Emulation**
- **Memory Options**
  - **Single-Access RAM (SARAM)**
  - **Read-Only Memory (ROM)**
- **Peripheral Options**
  - **Complete Library of Logic and Analog Peripherals**
  - **Customer-Designed Application-Specific Integrated Circuit (ASIC) Logic**
- **The T320C2700B0 Core Is Designed Using Static Logic**
- **All Logic and Buses Are Latched Each Cycle**
- **Logic Can Be Run at Any Clock Frequency**
- **Clock Frequency Can Be Slowed or Even Stopped to Lower the Power Requirements During Off-Peak Task Management**
  - **Suitable for Battery-Operated Applications**
- **Designed Specifically for the Texas Instruments (TI™) ASIC Library**
  - **Fully Process-Compatible With the TSC6000 Standard-Cell ASIC Libraries**
  - **Simulation Models Are Available**

PRODUCT PREVIEW

description

The T320C2700B0 core is a low-cost, 130-MIPS (0.18 μm), 16-bit fixed-point digital-signal processor (DSP) optimized for mass-storage mechanical and interface control applications. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets. The DSP features include Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture (usable in Von Neumann mode). The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and improved bit manipulation.

The T320C2700B0 core is a member of the TI line of customizable digital signal processors (cDSPs). The cDSP provides a simple and effective method for reducing a system by merging TI DSPs with TI application-specific integrated circuit (ASIC) gate-array or standard cell products. The TI ASIC design environment enables logic designers to combine custom logic with cDSP cores, other digital hardware macros, and linear hardware macros. This enables the designer to reduce part or all of a system design to a single device to improve performance and reliability while reducing system cost, hardware size, and power consumption.

Table of Contents

description (continued)

Because the instructions are bundled to allow one instruction in the place of several instructions in older devices, the code size for the T320C2700B0 is smaller. Smaller code size reduces system memory costs and improves performance.

The core consists of a central processing unit (CPU), emulation logic, and signals for interfacing with memory and peripherals. Figure 1 shows an example of a system using the core. The core also includes six interface buses: three 22-bit address buses and three 32-bit data buses. The T320C2700B0 is implemented in a modified Harvard architecture, which uses multiple memory spaces to enable instruction and data fetches to be performed in parallel, allowing single-cycle instructions. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over the six separate address/data buses. Figure 2 shows the interface buses, indicated by shading. The unshaded buses are internal to the core. The core does not contain memory, a clock generator, or peripheral devices.

The core is designed for use in an embedded cDSP environment. A typical cDSP device contains various kinds of memories (ROM or SARAM), peripherals, and user logic in addition to the core. For the purpose of testing the core and the other components in an embedded cDSP environment, different test modes have been defined. The core can be put into any of the test modes only through the test-access port. SLAVE mode is an exception and also has an additional dedicated input signal that can be used to put the device in SLAVE mode.

The test modes of the core are as follow:

- Core functional test mode – a test mode in which the core is completely isolated from the logic connected to it. B0 and B1 are the only memories that the core can access in this mode. All interrupts, reset, NMIn, READY signals from other memories are isolated from the core.
- Memory interface functional test mode – In this test mode, all the components connected to the memory interface can be accessed by the core. Interrupts, NMIn reset, and others are still isolated from the core.
- SLAVE mode – In this test mode, the core is completely inactive and does not respond to any of the normal input signals. The outputs are in an unknown state. Only the test mode status signals contain valid output values, as shown in Table 1.
- Core automatic test-pattern generation (ATPG) – This mode is defined for ATPG of the core.
- Peripheral ATPG – This mode is defined for ATPG of components connected to the core.

description (continued)

Table 1. Modes of Operation

OPERATING MODE	XLOGOFF OUTPUT	COREATPG OUTPUT	PERIATPG OUTPUT	MEMXFTEST OUTPUT	COREFTEST OUTPUT
Normal	0	0	0	0	0
Slave	1	0	0	0	0
Core Function	0	0	0	0	1
MEMX Function	0	0	0	1	0
Core ATPG	1	1	0	0	0
Peripheral ATPG	0	0	1	0	0

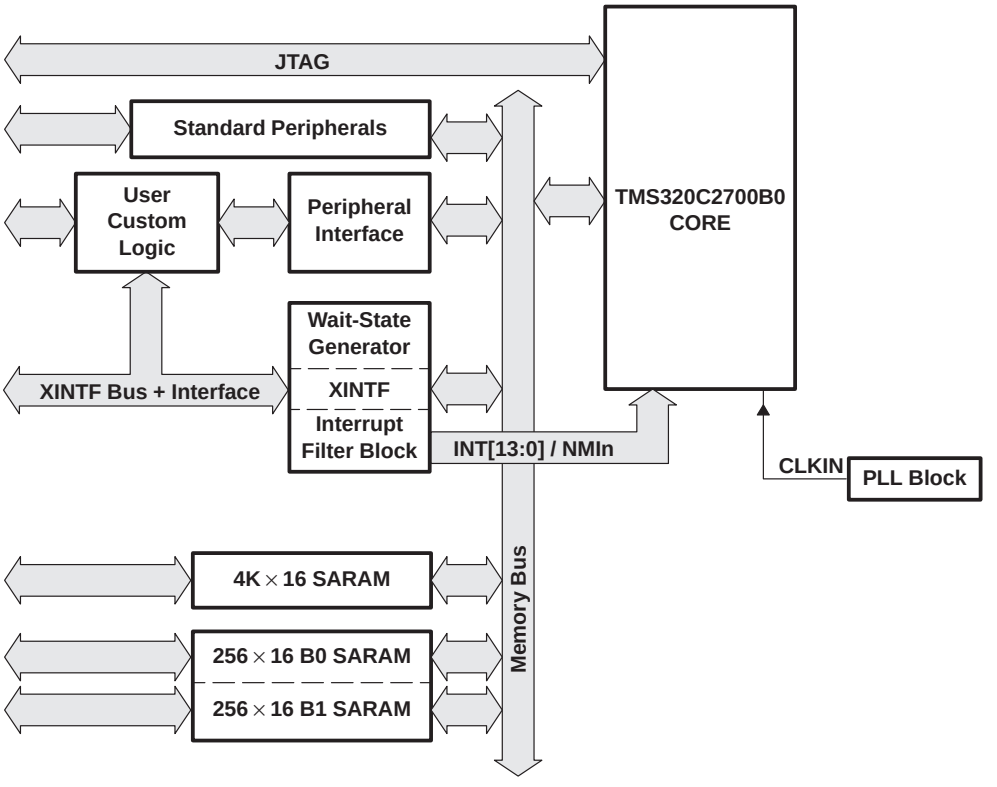

Figure 1. Example of a System Using the T320C2700B0 Core

PRODUCT PREVIEW

description (continued)

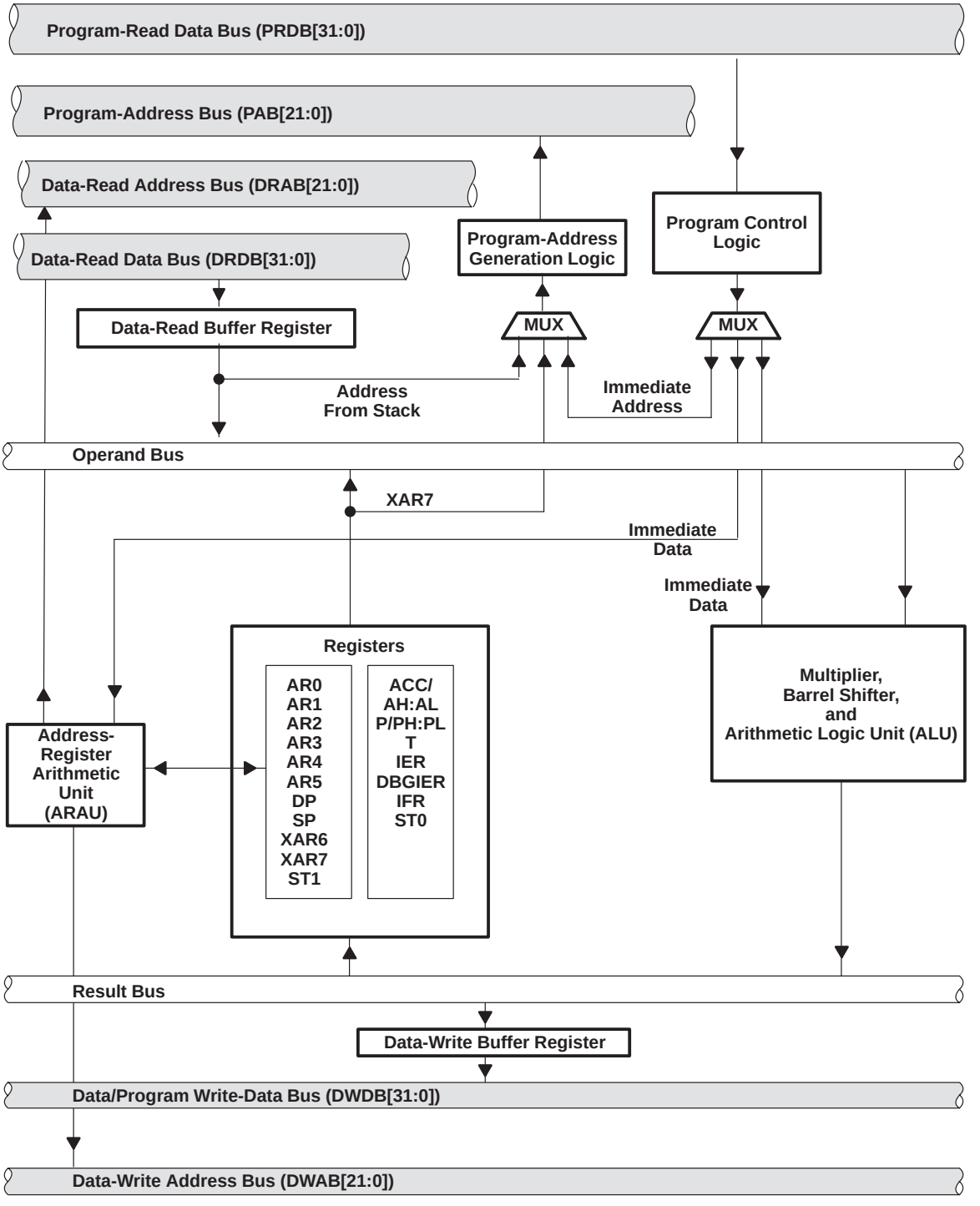

Figure 2. Conceptual Block Diagram of the CPU

signal descriptions

The core includes the following groups of signals:

- Memory-interface signals (see Table 2)
- Control and status signals (see Table 3)
- Write/read protection mode signals (see Table 4)
- Reset and interrupt signals (see Table 5)
- Emulation signals (see Table 6)
- Visibility port signals (see Table 7)

Figure 3 shows an overview of the signals for the memory interface, Figure 4 shows the control and status signals, and Figure 5 shows the emulation signals.

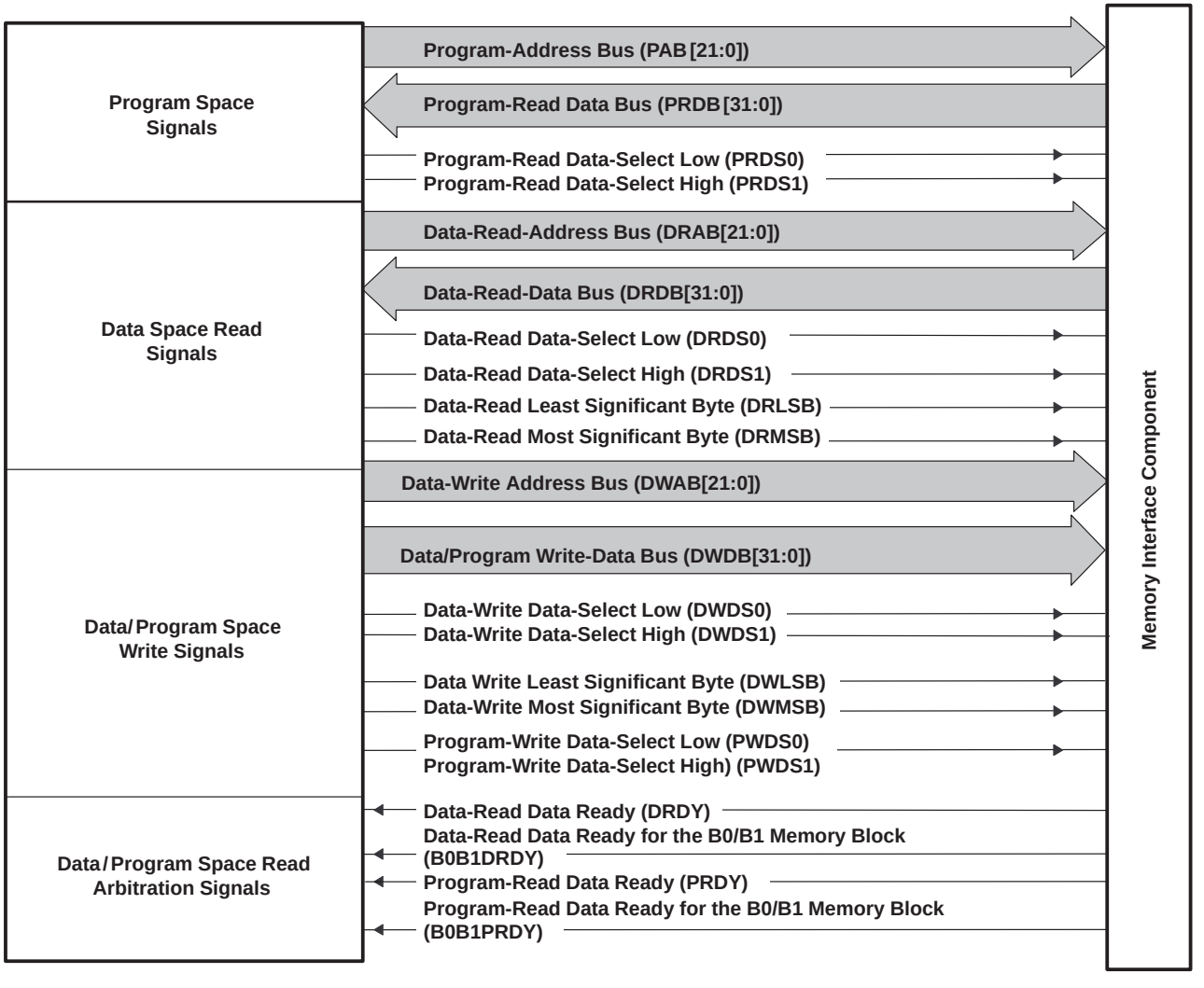

Figure 3. Memory-Interface Signal Diagram

signal descriptions (continued)

Table 2. Memory-Interface Signals

SIGNAL NAME	TYPE†	DESCRIPTION
PROGRAM-SPACE SIGNALS		
PAB[21:0]	O	Program address bus. PAB is a 22-bit bus that provides the address for both reads and writes to program space. PAB[0] is the LSB. PAB[21:0] go active on the rising edge of SYSCLKOUT and remains active until the next memory cycle starts.
PRDB[31:0]‡	I	Program-read data bus. PRDB[31:0] is a 32-bit program-space bus, defined for operations assuming banked memory (i.e., memories with one 16-bit bank for odd addresses and another 16-bit bank for even addresses). The odd bank always drives the higher half of the bus, while the even bank always drives the lower half of the bus. Both banks are enabled by 32-bit accesses. Data is always latched on the rising edge of SYSCLKOUT at the end of a program read cycle.
PRDS0 PRDS1‡	O	Program-read data-select low and program-read data-select high. PRDS0, when active (high), indicates that the CPU is requesting a 16-bit read from an even-address program-space location. PRDS1, when active (high), indicates that the CPU is requesting a 16-bit read from an odd-address program-space location. PRDS0 and PRDS1 go active on the rising edge of SYSCLKOUT and remain active until the next memory cycle starts. PRDS0 and PRDS1 are used to decode the following bus transactions: Transaction Type / PRDS1 / PRDB[31:16] / PRDS0 / PRDB[15:0] 32-bit read, even aligned / high / data(16) / high / data(16) 16-bit read, even address / low / undefined / high / data(16) 16-bit read, odd address / high / data(16) / low / undefined no transaction / low / undefined / low / undefined
DATA-SPACE READ SIGNALS		
DRAB[21:0]	O	Data-read address bus. DRAB is a 22-bit bus that outputs the data-read addresses from the CPU. DRAB[0] is the least significant bit (LSB). DRAB goes active on the rising edge of SYSCLKOUT and remains active until the next memory cycle starts.
DRDB[31:0]	I	Data-read data bus. DRDB[31:0] is a 32-bit bus that inputs 16- or 32-bit data-read data. The data is latched into the core on the rising edge of SYSCLKOUT at the end of the data-read cycle.
DRDS0 DRDS1	O	Data-read data select low and data-read data-select high. DRDS0, when active (high), indicates that the CPU is requesting a 16-bit read from an even-address data-space location. DRDS1, when active (high), indicates that the CPU is requesting a 16-bit read from an odd-address data-space location. DRDS0 and DRDS1 go active at the rising edge of SYSCLKOUT and remain active until the next memory cycle starts. DRDS0 and DRDS1 are used to decode the following bus transactions: Transaction Type / DRDS1 / DRDB[31:16] / DRDS0 / DRDB[15:0] 32-bit read, even aligned / high / data(16) / high / data(16) 16-bit read, even address / low / undefined / high / data(16) 16-bit read, odd address / high / data(16) / low / undefined no transaction / low / undefined / low / undefined

† I = Input, O = Output

‡ Instructions are normally fetched as 32-bit program read operations, except at the start of a discontinuity. If the address starts at an odd location, only PRDS1 is driven high and the instruction is fetched on PRDB[31:16]. The core ignores any data present on PRDB[15:0]

signal descriptions (continued)

Table 2. Memory-Interface Signals (Continued)

SIGNAL NAME	TYPE†	DESCRIPTION
DATA-SPACE READ SIGNALS (CONTINUED)		
DRLSB DRMSB	O	Data-read least significant byte (LSByte) and data-read most significant byte (MSByte). DRLSB, when active (high), indicates that the CPU is performing a 16-bit read operation with the LSByte of the word being the active data element. DRMSB, when active (high), indicates that the CPU is performing a 16-bit read operation with the MSByte of the word as the active data element. DRLSB and DRMSB go active at the rising edge of SYSCLKOUT and remain active until the next memory cycle starts. The DRLSB and DRMSB signals can be used in conjunction with the DRSD0 and DRSD1 signals to perform byte-only accesses from byte-wide peripherals or memory. This usage can improve cycle performance on accesses to such peripherals. The decode of the signals is as follows: Transaction Type — DRDS1 — DRDS0 — DRMSB — DRLSB 32-bit read — high — high — high — high 16-bit read, even address — low — high — high — high Read, LSByte — low — high — low — high Read, MSByte — low — high — high — low 16-bit read, odd address — high — low — high — high Read, LSByte — high — low — low — high Read, MSByte — high — low — high — low No transaction — low — low — low — low
DATA-SPACE WRITE SIGNALS		
DWAB[21:0]	O	Data-write address bus. DWAB is a 22-signal bus that outputs the data-write addresses from the CPU. DWAB[0] is the LSB. DWAB goes active on the rising edge of SYSCLKOUT and remains active until the next memory cycle starts.
DWDB[31:0]	O	Data-/program-write data bus. DWDB is a 32-bit bus that outputs 16-bit or 32-bit data to data or program space. This data is written out on the rising edge of SYSCLKOUT and remains active until the end of the data-write cycle.
DWDS0 DWDS1	O	Data-write data-select low and data-write data-select high. DWDS0, when active (high), indicates that the CPU is requesting a 16-bit write to an even-address data-space location. DWDS1, when active (high), indicates that the CPU is requesting a 16-bit write to an odd-address data-space location. DWDS0 and DWDS1 go active at the rising edge of SYSCLKOUT and remain active until the next memory cycle starts. DWDS0 and DWDS1 are used to decode the following bus transactions: Transaction Type — DWDS1 — DWDB[31:16] — DWDS0 — DWDB[15:0] 32-bit write, even aligned — high — data(16) — high — data(16) 16-bit write, even address — low — undefined — high — data(16) 16-bit write, odd address — high — data(16) — low — undefined no transaction — low — undefined — low — undefined

† I = Input, O = Output

‡ Instructions are normally fetched as 32-bit program read operations, except at the start of a discontinuity. If the address starts at an odd location, only PRDS1 is driven high and the instruction is fetched on PRDB[31:16]. The core ignores any data present on PRDB[15:0]

PRODUCT PREVIEW

signal descriptions (continued)

Table 2. Memory-Interface Signals (Continued)

SIGNAL NAME	TYPE†	DESCRIPTION
DATA-SPACE WRITE SIGNALS (CONTINUED)		
DWLSB DWMSB	O	Data-write LSByte, data-write MSByte. DWLSB, when active (high), indicates that the CPU is performing a 16-bit write operation with the LSByte of the word being the active data element. DWMSB, when active (high), indicates that the CPU is performing a 16-bit write operation with the MSByte of the word being the active data element. DWLSB and DWMSB go active at the rising edge of SYSCLKOUT and remain active until the next memory cycle starts. The DWLSB and DWMSB signals can be used with the DWDS0 and DWDS1 signals to perform byte-only accesses from byte-wide peripherals or memory to improve cycle performance on accesses to such peripherals. The decode of the signals is as follows: Transaction Type / DWDS1 / DWDS0 / DWMSB / DWLSB 32-bit write, even aligned: high / high / high / high 16-bit write, even address: low / high / high / high write, LSByte: low / high / low / high write, MSByte: low / high / high / low 16-bit write, odd address: high / low / high / high write, LSByte: high / low / low / high write, MSByte: high / low / high / low no transaction: low / low / low / low
PWDS0 PWDS1	O	Program-write data-select low and program-write data-select high. PWDS0, when active (high), indicates that the CPU is requesting a 16-bit write to an even-address program-space location. PWDS1, when active (high), indicates that the CPU is requesting a 16-bit write to an odd-address program-space location. PWDS0 and PWDS1 go active at the rising edge of SYSCLKOUT and remain active until the next memory cycle starts (determined by POREADY signals to the core). PWDS0 and PWDS1 are used to decode the following bus transactions: Transaction Type / PWDS1 / DWDB(31:16) / PWDS0 / PWDB(15:0) 32-bit write, even aligned: high / data(16) / high / data(16) 16-bit write, even address: low / undefined / high / data(16) 16-bit write, odd address: high / data(16) / low / undefined no transaction: low / undefined / low / undefined
PROGRAM/DATA SPACE READ ARBITRATION SIGNALS		
B0B1DRDY	I	Data-read data ready for the B0 memory block. B0B1DRDY is the same as the DRDY, except that the signal is connected only to the B0/B1 memory blocks. B0B1DRDY is asserted by the B0/B1 block to indicate to the CPU that the DRDB is being driven with read data in response to a data-read request.

† I = Input, O = Output

‡ Instructions are normally fetched as 32-bit program read operations, except at the start of a discontinuity. If the address starts at an odd location, only PRDS1 is driven high and the instruction is fetched on PRDB[31:16]. The core ignores any data present on PRDB[15:0]

signal descriptions (continued)

Table 2. Memory-Interface Signals (Continued)

SIGNAL NAME	TYPE†	DESCRIPTION
PROGRAM/DATA SPACE READ ARBITRATION SIGNALS (CONTINUED)		
B0B1PRDY	I	B0B1PRDY is similar to the PRDY but is connected to the B0/B1 block and cannot be connected to anything else. B0B1PRDY is asserted by the B0/B1 block to indicate to the CPU that the PRDB is being driven with read data in response to a program-read request.
DRDY	I	Data-read data ready. DRDY, when active (high), indicates that the data on the DRDB [31:0] bus is available to the core. DRDY is daisy-chained through memory blocks. The input to the first block of DRDY must be tied low. If the application includes no data space blocks, DRDY must be tied low at the input to the port. Blocks B0 and B1 must be daisy-chained through the B0B1DRDY signal and not daisy-chained through the DRDY signal (to which all other memory blocks or peripherals are connected). This is required for isolation during core functional tests.
PRDY	I	Program-read data ready. PRDY, when active (high), indicates that the data on the PRDB [31:0] bus is available to the core. This signal is daisy-chained through memory blocks or peripherals. The input to the first block of PRDY must be tied low. If the application contains no program space blocks, PRDY must be tied low at the input to the port. Blocks B0 and B1 must be daisy-chained through the B0B1PRDY signal and not daisy-chained through the PRDY signal (to which all other memory blocks are connected). This is required for isolation during core functional tests.

† I = Input, O = Output

‡ Instructions are normally fetched as 32-bit program read operations, except at the start of a discontinuity. If the address starts at an odd location, only PRDS1 is driven high and the instruction is fetched on PRDB[31:16]. The core ignores any data present on PRDB[15:0]

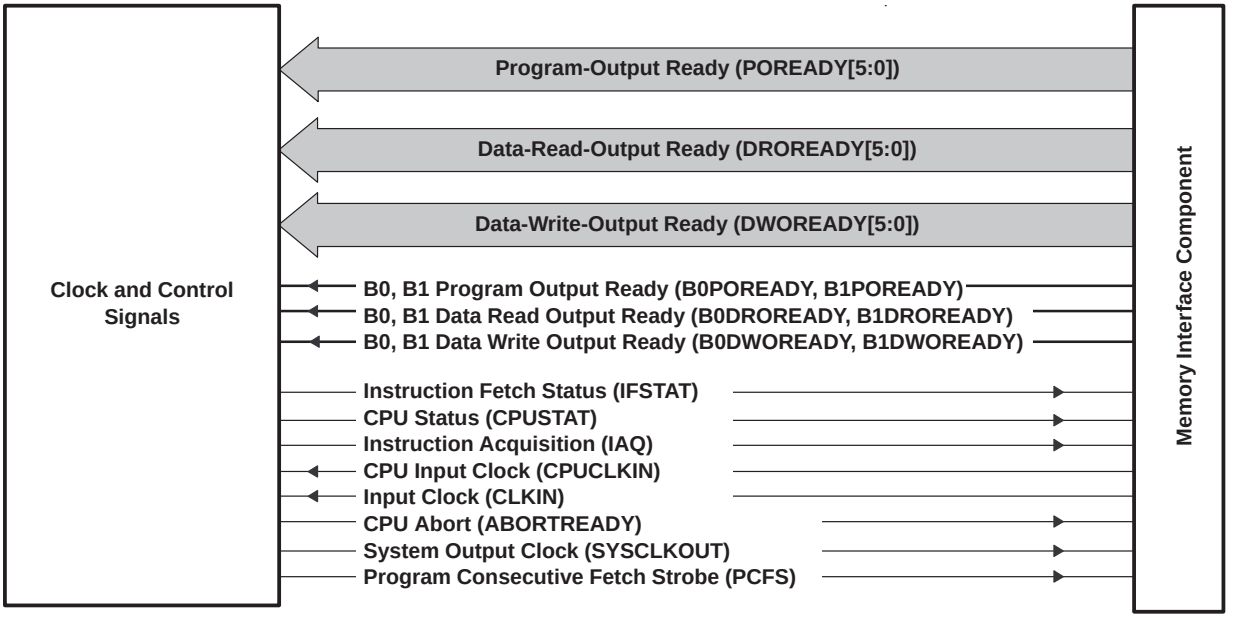

Figure 4. Clock and Control Signal Diagram

signal descriptions (continued)

Table 3. Clock and Control Signals

SIGNAL NAME	TYPE†	DESCRIPTION
ABORTREADY	O	CPU aborting all requests. ABORTREADY is an output signal that must be connected to all memory interface components. This signal, when active (high), indicates that the CPU is aborting all the existing requests.
B0POREADY	I	Program-space-memory output ready for the B0 memory block. B0POREADY is identical to the POREADY signal except that B0POREADY is meant for connection to the B0 block. No other memory block can be connected to this signal.
B1POREADY	I	Program-space-memory output ready for the B1 memory block. B1POREADY is identical to the POREADY signal except that B1POREADY is meant for connection to the B1 block. No other memory block can be connected to this signal and B1 can be mapped only to data memory. B1POREADY must be tied high.
B0DROREADY	I	Data-space memory-read output ready for connection to the B0 memory block. B0DROREADY is identical to the DROREADY signal except that this is for connection to the B0 block. No other memory can be connected to B0DROREADY.
B1DROREADY	I	Data-space memory-read output ready for connection to the B1 memory block. B1DROREADY is identical to the DROREADY signal except that this is for connection to the B1 block. No other memory can be connected to B1DROREADY.
B0DWOREADY	I	Data-space memory-write output ready for the B0 memory block. B0DWOREADY is identical to the DWOREADY signal except that this is for connection to the B0 memory block. No other memory must connect to this signal.
B1DWOREADY	I	Data-space memory-write output ready for the B1 memory block. B1DWOREADY is identical to the DWOREADY signal except that this is for connection to the B1 memory block. No other memory must connect to this signal.
CLKIN	I	Input clock. CLKIN is the input-clock feed to the device core. The input frequency is proportional to the CPU cycle time. For example, for a device operating at CLKIN = 100 MHz, CPU cycle time is 10 ns.
CPUCLKIN	I	CPU input-clock signal. The output CPUCLKOUT should be connected through a clock-tree synthesis (CTS) macro to CPUCLKIN.
CPUCLKOUT	O	CPU output clock. CPUCLKOUT is generated by the CPU. For details on connecting CPUCLKOUT, see the clocking section.
CPUSTAT	O	CPU status. CPUSTAT, when active (high), indicates that the CPU is ready to start the memory cycles requested for the memory interface. If CPUSTAT is inactive (low), the CPU is in a CPU wait stated cycle and cannot accept data.
DROREADY[5:0]	I	Data-space memory-read output ready. The six DROREADY signals are used by memories and interface bridges to request waitstates on data-read operation. When a memory or interface bridge cannot complete the requested data-read access, it pulls the DROREADY[5:0] signals low. Unused DROREADY signals must be tied high. The memory read operation is two-staged and the CPU expects data to be driven one cycle after it samples the DROREADY signal to be high. *This relationship is very important, and memories and interface bridges must adhere to this. If not, the CPU can produce erroneous results.*
DWOREADY[5:0]	I	Data-space memory-write output ready. The six DWOREADY signals are connected to the CPU. The devices that have a pending data-write operation must generate a ready (high) or not-ready (low) condition on their respective DWOREADY signals to keep the CPU from completing the machine cycle until all scheduled memory operations are complete. All unused DWOREADY signals must be tied high. A not-ready condition on the DWOREADY line does not necessarily stall the fetch mechanism.
IAQ	O	Instruction acquisition. IAQ, when active (high), indicates that the current bus cycle is performing an instruction fetch. If IAQ is low and a program-space operation is in progress, a program-space data-read or -write operation is being performed. This signal is used to distinguish between an instruction fetch and a program read or write operation (performed by the PREAD, PWRITE, and MAC instructions). IAQ is valid on the rising edge of SYSCLKOUT and remains valid until the next memory cycle starts (determined by POREADY signals to the core).
IFSTAT	O	Instruction-fetch status. IFSTAT, when active (high), indicates that the instruction-fetch mechanism is ready to start the memory cycles requested for the memory interface. If IFSTAT is inactive (low), the instruction-fetch mechanism is in a program-space waitstated cycle.

† I = Input, O = Output

signal descriptions (continued)

Table 3. Clock and Control Signals (Continued)

SIGNAL NAME	TYPE†	DESCRIPTION
IMUCLKIN	I	Emulation domain input-clock signal. The output IMUCLKOUT must be connected through a CTS macro to IMUCLKIN.
IMUCLKOUT	O	Emulation domain clock output. For details of connecting IMUCLKOUT see the CTS section.
PCFS	O	Program consecutive fetch strobe. PCFS indicates that the current fetch is consecutive to the previous fetch operation. PCFS is valid on the rising edge of SYSCLKOUT and remains valid until the end of the program read cycle.
POREADY[5:0]	I	Program-space-memory output ready. POREADY signals are used by memories and interface bridges to request wait states on program memory operations. When a memory or interface bridge cannot complete the requested program-space access, POREADY is pulled low. Multiple signals are provided so that each block can have an independent POREADY line to the CPU. Unused POREADY signals must be tied high. A not-ready condition on the POREADY line does not necessarily stall the CPU.
SYSCLKOUT	O	System output clock. SYSCLKOUT is generated by the core. The memory-interface components should connect to SYSCLKOUT.

† I = Input, O = Output

signal descriptions (continued)

Table 4. Write/Read Protection Mode Signals

SIGNAL NAME	TYPE†	DESCRIPTION
ENPROT	I	Enable write followed by read-protection mode. ENPROT, when high, enables the write followed by read protection mode within the memory range specified by the PROTSTART and PROTRANGE inputs. If ENPROT is low, the protection mode is disabled and the PROTRANGE and PROTSTART inputs are ignored. ENPROT must be latched on every cycle.
PROTSTART[15:0]	I	Write followed by read-protection mode start-address inputs. These sixteen input signals specify the protection mode start address. The minimum resolution is 64 words. The start address must be a multiple of the protrange value. For example, if the PROTRANGE value is set for 4K, the start address must be a multiple of 4K. The mapping of the PROTSTART signals to the memory-bus address lines is as follows: Address lines A21 A20 A19 . . A8 A7 A6 PROTSTART signal 15 14 13 . . 2 1 0 PROTSTART[15:0] must be latched on every cycle.
PROTRANGE[15:0]	I	Write followed by read-protection mode address-range inputs. These sixteen input signals specify the protection mode range from the start address. The minimum block size is 64 words. The valid combinations of input signals is as follows: Range size 15 14 13 12 . . . 3 2 1 0 4M 1 1 1 1 . . . 1 1 1 1 2M 0 1 1 1 . . . 1 1 1 1 1M 0 0 1 1 . . . 1 1 1 1 512K 0 0 0 1 . . . 1 1 1 1 . . . . 512 0 0 0 0 . . . 0 1 1 1 256 0 0 0 0 . . . 0 0 1 1 128 0 0 0 0 . . . 0 0 0 1 64 0 0 0 0 . . . 0 0 0 0 PROTRANGE[15:0] must be latched on every cycle.

† I = Input, O = Output

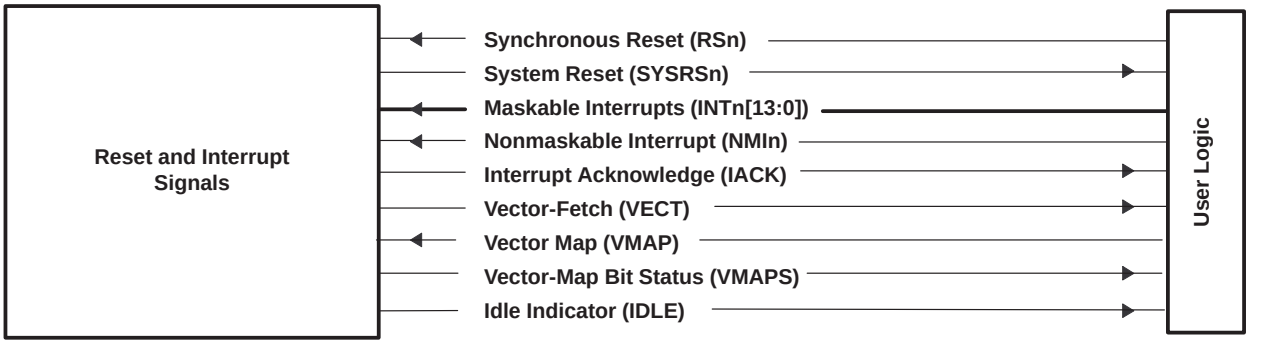

Figure 5. Reset and Interrupt Signal Diagram

signal descriptions (continued)

Table 5. Reset and Interrupt Signals

SIGNAL NAME	TYPE†	DESCRIPTION
IACK	O	Interrupt acknowledge. IACK is driven active (high) by the execution of the IACK 16-bit instruction. The IACK instruction writes the 16-bit immediate value to the data-write bus, DWDB[15:0]. The data-write-address bus, DWAB[21:0], contains the address of the last operation on the bus prior to the IACK instruction and has no relationship to the IACK operation. This data is written out on the rising edge of SYSCLKOUT and remains active until the end of the data-write cycle.
IDLE	O	Idle indicator. IDLE, when active (high), indicates that the CPU has executed an IDLE instruction. The IDLE signal can be used to turn off customer-generated logic while the CPU is idling.
INTn[13:0]	I	Maskable interrupts, 0 – 13. INTn[13:0] are external interrupts that are prioritized and maskable. All INT inputs are level sensitive. All inputs are not synchronized to the core clock and feed directly to the interrupt-flag register (IFR). Synchronization and/or edge-detection circuits can be implemented outside of the core.
NMIn	I	Nonmaskable interrupt. NMIn is an external interrupt that cannot be masked. NMIn input is level-sensitive. The input is not synchronized to the core clock. Synchronization and/or edge-detection circuits can be implemented outside of the core.
RSn	I	Synchronous reset. When RSn is brought low, it causes the device to terminate execution, forcing internal-operating modes to a known state, and forcing the program to the RESET vector location (dependent on VMAP-signal input). When the signal is brought to a high level, the address located at the reset vector is fetched and written into the program counter (PC). Execution then begins at the vector location. An appropriate number of machine cycles are necessary to completely initialize internal states.
SYSRSn	O	System reset. SYSRSn goes active (low) when RSn is latched by the core. SYSRSn goes high when the core has completed all internal-reset sequences and is ready to fetch the reset vector. SYSRSn is synchronized to the rising edge of SYSCLKOUT.
VECT	O	Vector fetch. VECT is driven high for the duration of the reset and interrupt vector-fetch operation. VECT is valid on the rising edge of SYSCLKOUT and remains valid until the end of the program-read cycle. VECT can be used, in conjunction with the program-address-bus value, to fetch vectors from special interrupt-processing blocks external to the core.
VMAP	I	Vector map. VMAP is an input signal that selects the mapping of the reset and interrupt vectors. VMAP = 1 forces the vector table to high memory space starting at address 0x3FFFC0. VMAP = 0 forces the vector table to low memory space starting at address 0x000000. The VMAP signal is sampled on a reset, RSn, and the value mirrored in the VMAP bit in status register 1. The SETC/CLRC instructions can be used to modify the bit, thus remapping the vector table. This bit is accessible by the emulation hardware via the scan port and enables the test software to map the reset and interrupt vector table to low or high memory.
VMAPS	O	Vector-map bit status. VMAPS is an output signal that mirrors the status of the VMAP bit in status register 1.

† I = Input, O = Output

A set of core output signals is defined in Table 6 to indicate the test mode in which the core is currently operating.

signal descriptions (continued)

Table 6. Emulation Signals

SIGNAL NAME	TYPE†	DESCRIPTION
COREATPG	O	COREATPG is an output signal that goes active (high) when the core is put in core automatic test-pattern generation (ATPG) mode.
COREFTEST	O	COREFTEST is an output signal that goes active (high) when the core is put in core functional test mode.
ET0I	I	Emulator input 0. ET0I is used by the emulator to force the CPU to trap to an emulator interrupt or to stop altogether. ET0I is also used for device operational mode control when TRSTn is low. ET0I is the output of an input buffer. The input side is the dedicated pin ET0.
ET0O	O	Emulator output 0. ET0O flags the emulator of an internally generated emulator event. ET0O can be configured to output various CPU events. ET0O is the input of an output buffer to form the dedicated pin ET0.
ET0Z	O	Emulator output 0 enable. ET0Z, when active (low), indicates ET0O is active. ETOZ is the 3-state enable of an output buffer to form the dedicated pin ET0.
ET1I	I	Emulator input 1. ET1I is used by the emulator to force the CPU to trap to an emulator interrupt or to stop altogether. This signal is also used for device operational mode control when TRSTn is low. ET1I is the output of an input buffer. The input side is the dedicated pin ET1.
ET1O	O	Emulator output 1. ET1O flags the emulator of an internally generated emulator event. ET1O can be configured to output varous CPU events. ET1O is the input of an output buffer.
ET1Z	O	Emulator output 1 enable. ET1Z, when active (low), indicates that ET1O is active. ET1Z is the 3-state enable of an output buffer.
MEMXFTEST	O	MEMXFTEST is an output signal that goes active (high) when the core is put in memory interface functional test mode.
PERISCANEN	O	Peripheral scan enable. PERISCANEN is used for peripheral ATPG and is connected to all the components.
PERIATPG	O	PERIATPG is an output signal that goes active (high) when the core is put in peripheral ATPG mode.
PERISCOUT	I	PERISCOUT is the scan out of the peripheral scan chain.
PERISCPATH	I	PERISCPATH is tied high or low depending on whether the peripheral scan chain is active.
SLAVEIN	I	SLAVEIN is an input signal that puts the core in slave mode and it must be brought out directly on the pins or it must be tied low.
TCK	I	Test clock. TCK is the input clock for the IEEE Standard 1149.1 (JTAG‡) serial scan operations and it is a free-running clock signal with a 50 percent duty cycle. The changes on test access port (TAP) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK. This signal must be brought to a dedicated pin of the device for test and emulation purposes.
TDI	I	Test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. TDI must be brought to a dedicated pin of the device for test and emulation purposes.
TDO	O	Test data out. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in high impedance state except when scanning of data is in progress. TDO must be brought to a dedicated pin of the device for test and emulation purposes.
TDOZ	O	Emulator scan out enable. $\overline{\text{TDOZ}}$, when active (low), indicates TDO is active. It is connected to the 3-state control of the input/output buffer cell to form the dedicated pin TDO.
TMS	I	Test mode select. TMS control input is clocked into the TAP controller on the rising edge of TCK. If TMS is held high for five TCK cycles, the port shuts down and the device operates in its functional mode (i.e., the same effect as TRSTn low). TMS must be brought to a dedicated pin of the device for test and emulation purposes.

† I = Input, O = Output
‡ IEEE Standard 1149.1–1990, IEEE Standard Test Access Port and Boundary-Scan Architecture

signal descriptions (continued)

Table 6. Emulation Signals (Continued)

SIGNAL NAME	TYPE†	DESCRIPTION
TRSTn	I	Test reset. TRSTn, when high, gives the scan system control of operations of the device. If this signal is driven low, the device operates in its functional mode and the test signals are ignored. This signal is asynchronous. If the device is taken to functional mode by clocking in a high TMS, TRSTn must be tied high. When TRSTn is low, ET0 and ET1 are inputs and indicate test modes of the device.
XLOGOFF	O	XLOGOFF is an output signal that must be connected to all of the memory interface components. XLOGOFF, when active (high), indicates that the CPU is either in slave mode or in core ATPG. The CPU outputs on the memory interface can contain invalid values.

† I = Input, O = Output
‡ IEEE Standard 1149.1–1990, IEEE Standard Test Access Port and Boundary-Scan Architecture

signal descriptions (continued)

CAUTION:

Signals in Table 7 are reserved for TI emulation use and must not be connected or used in the cDSP design.

Table 7. Emulation and Visibility Port Signals

SIGNAL NAME	TYPE†	DESCRIPTION	SIGNAL NAME	TYPE†	DESCRIPTION
AEVTQUAL	I	Reserved	RSTAT	O	Reserved
ANASTOP	I	Reserved	RTOSINTn	I	Reserved
BREAKHI	I	Reserved	TRACEHI	I	Reserved
BREAKLO	I	Reserved	TRACELO	I	Reserved
CSTOPPING	O	Reserved	UBUS[31:0]	I	Reserved
CTOOLSACK	I	Reserved	USER0[3:0]	I	Reserved
DBGACCESSP	O	Reserved	USER1[3:0]	I	Reserved
DBGACCESSR	O	Reserved	VCOND	O	Reserved
DBGACCESSW	O	Reserved	VBANZ	O	Reserved
DBGACK	O	Reserved	VDISCINSTR	O	Reserved
DBGM	O	Reserved	VDRDB[31:0]	O	Reserved
DBGPTYPE	O	Reserved	VHPI	O	Reserved
DBGRTYPE[1:0]	O	Reserved	VINDRCT	O	Reserved
DBGWTYPE	O	Reserved	VINSTRJAM	O	Reserved
DCON	O	Reserved	VIREG[31:0]	O	Reserved
DEVTQUAL	I	Reserved	VMAC	O	Reserved
DFC	O	Reserved	VNEWINSTR	O	Reserved
EALLOW	O	Reserved	VPAGE0	O	Reserved
EXTTRGR	I	Reserved	VPIPEPROT	O	Reserved
EXTCNT0	I	Reserved	VPRDB	O	Reserved
EXTCNT1	I	Reserved	VPREAD	O	Reserved
HERMIT	O	Reserved	VPWRITE	O	Reserved
MONPRIV	I	Reserved	VPC	O	Reserved
MONPRIVO	O	Reserved	VPCDISC	O	Reserved
PSTAT	O	Reserved	VRESET	O	Reserved
PWRABORT	O	Reserved	VRPTINSTR	O	Reserved
RESERVED1	O	Reserved	VSPR	O	Reserved
RESERVED2	O	Reserved	VSPW	O	Reserved
RESETOUT	O	Reserved	WSTAT	O	Reserved

† I = Input, O = Output

architecture

The T320C2700B0 uses a modified Harvard architecture to maximize processing power by using separate bus structures for data memory and for program memory. Separate program and data spaces allow simultaneous access to program instructions and data, providing a high degree of parallelism. For example, a read and write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that all can be performed in a single machine cycle. In addition, the TMS320C2700B0 includes the control mechanisms to manage interrupts, repeated operations, and function calling.

memory interface

No memory is provided with the core; however, the memory interface allows the use of a variety of memory types. The core has a total address reach of 4M words (16-bit words) each in the program and data spaces.

The memory interface works with the following components:

- Memories such as single-access RAM (SARAM), or ROM
- External interface bridges
- Peripherals

Memory-mapped registers can be realized by having registers that decode and respond to the memory interface signals.

memory operations

The ’C27xx instruction set has a variety of instructions performing different kinds of operations, including arithmetic operations, address manipulation, data transfer, program-flow control, and others. Instruction operation consists of the following stages:

- Instruction fetch
- Instruction decode
- Operand fetch
- Execution
- Writeback

The core contains separate hardware to perform each operation so that the operations can run in parallel. The memory interface supports full utilization of parallel operations. Separate memory spaces are defined for instructions and operands, referred to as program and data space, respectively. Special instructions also allow data to reside in program space.

The memory operations can be classified in the following types:

- Instruction fetch from program space
- Data (operand) read from program space
- Data (operand) write to program space
- Data (operand) read from data space
- Data (operand) write to data space

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memory operations (continued)

To obtain maximum performance, the memory interface must support combinations of these operations in parallel. Data (operand) accesses from program space are supported by very few instructions and these accesses are relatively infrequent; therefore, data reads from program space share the same set of buses and signals as instruction fetches. Similarly, data writes to program space share the same write data bus with data space writes and address bus with instruction fetches. Separate signals and buses are defined for data reads and data writes to the data space.

daisy chaining PRDY and DRDY

The PRDY and DRDY signals are defined as inputs to the core that indicate to the CPU that a memory is responding with valid data to a read request from the CPU. Since many memories and other components can be connected to the memory interface, the PRDY and DRDY signals must be driven active to the CPU every time a component is responding to a read request by having each component generate a PRDY or DRDY output and “ORing” all these before sending them to the CPU. For systems where multiple banks of memory are present, the TI-defined wrappers and interfaces use a daisy-chain for the PRDY or DRDY signals. Every component has a PRDY/DRDY input and a PRDY/DRDY output. The first component has its PRDY/DRDY input tied low and all subsequent components have their PRDY/DRDY inputs tied to the output of the previous component, with the output of the last component going to the core. The output signal of any component goes active when either it is responding to a memory request or its input signal is active. See Figure 6.

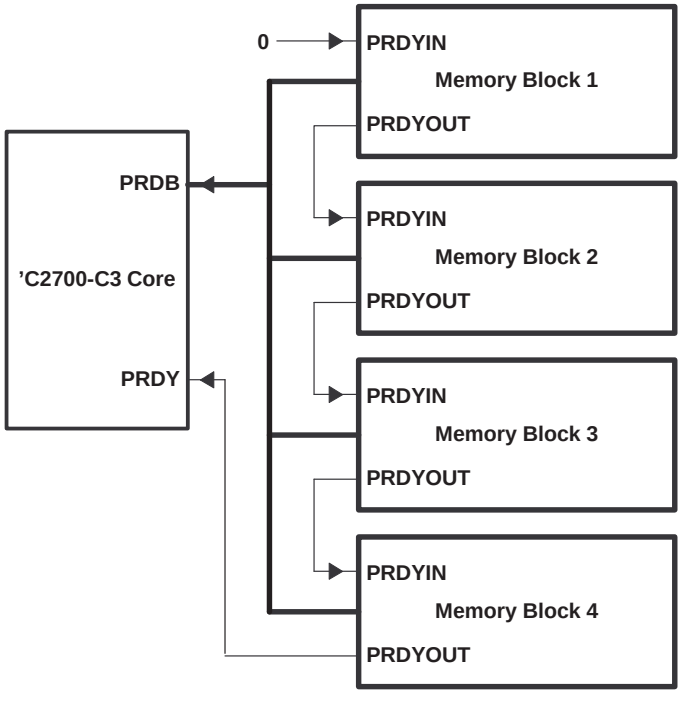

Figure 6. Daisy-Chaining of PRDY

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POREADY, DROREADY, DWOREADY, B0/B1POREADY, B0/B1DROREADY, B0/B1DWOREADY

POREADY, DROREADY, DWOREADY, B0/B1POREADY, B0/B1DROREADY, and B0/B1DWOREADY are the signals that are used by the components to send a request for additional wait states when they cannot complete an operation within one cycle. All memories and components connected to the memory interface normally have the POREADY, DROREADY, and DWOREADY output held high. Only when a component recognizes that an access requires wait states does it pull the POREADY, DROREADY, and DWOREADY low. All components that connect to the memory interface must be designed such that POREADY, DROREADY, and DWOREADY are held high to the CPU unless there is a valid access that requires a wait state.

program space and data space read timing

Memory reads are pipelined in two stages. The CPU has two pipeline stages for all read operations. The core uses single-edge clocking; therefore, all core output signals are driven out on a clock edge and all input signals are sampled during a clock edge.

- At the start of a read cycle, address and strobes are asserted by the CPU.
- Memory wrappers and other components decode the address and strobes to identify if the access is meant for that block.
- If the access is meant for that block and the block needs more cycles to complete the read operation, POREADY or DROREADY is pulled low before the next clock edge.
- This causes the CPU to freeze the pipeline (on data reads) and remain in this condition until the memory component that requested the wait state pulls the POREADY or DROREADY signal high again.
- On the cycle after POREADY or DROREADY goes high, the data is driven to the CPU along with PRDY or DRDY. The CPU latches the data at the next clock edge. This timing relation is important and must be followed. POREADY or DROREADY must be asserted high exactly one cycle before the data and PRDY or DRDY is to be driven back to the CPU.

program space and data space write timing

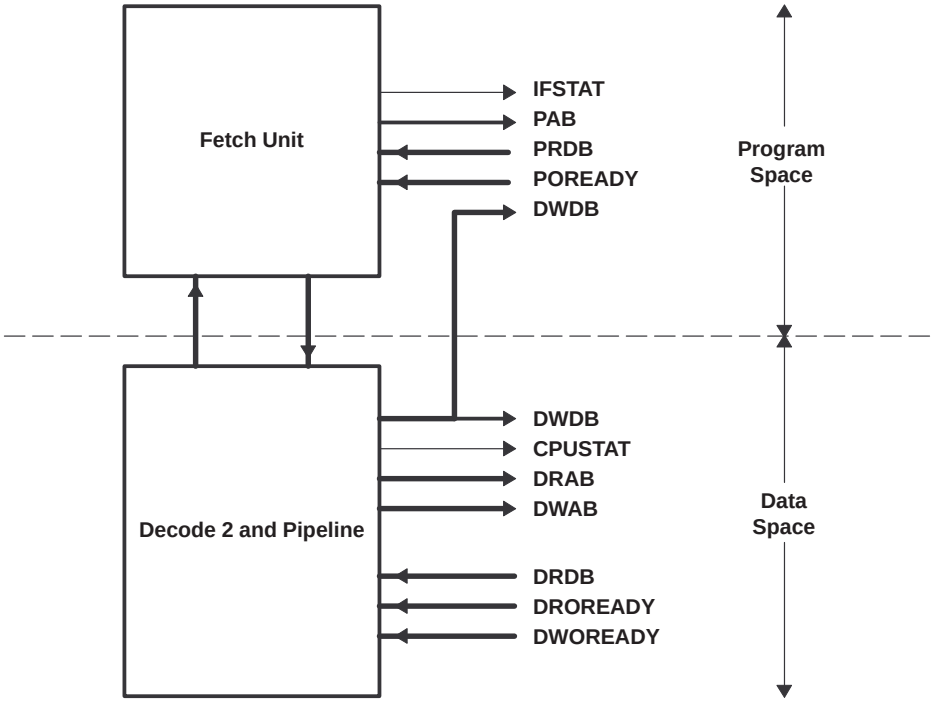
Program space writes use PAB as the address bus, DWDB as the data bus and PWDS0 and PWDS1 as the write-select strobes. Data space writes use DWAB as the address bus, DWDB as the data bus, and DWDS0 and DWDS1 as the write-select strobes. Address, data, and write-select strobes are asserted by the CPU on clock edge1. If a data-space write requires wait states, the DWOREADY signal must be pulled low before clock edge 2. If the write completed successfully, DWOREADY goes high and the pipeline advances.

decoupled program and data space accesses

Figure 7 shows the decoupled fetch unit. The decoupled fetch unit runs independently of the CPU pipeline, allowing the fetch unit to continue issuing fetches while the CPU pipeline has stalled. The reverse is also true. The CPU pipeline can continue with its operations even if the fetch unit is stalled.

The fetch unit uses the program space memory interface signals to perform instruction fetches and data accesses to program space. The fetch unit keeps the internal buffer full by prefetching instructions. The CPU pipeline works off the internal buffers and freezes the pipeline only when there are no instructions in the buffer.

decoupled program and data space accesses (continued)



NOTE A: Not all memory interface signals are shown.

Figure 7. Decoupled Fetch Unit

wait state accesses on the memory interface

A memory can request wait states whenever it needs extra cycles to complete a request. Even though the core has a two-staged pipelined read, the memory must request wait states for a read at the first cycle where the read request is sent out by the CPU. It cannot request a wait state when it is driving the data out on the second phase of the read.

clocking

For the chip to function properly, the three independent clocks CPUCLK, IMUCLK, and SYSCLK must be balanced within reasonable skew because of the exchange of data between these three clock domains. The CPUCLK domain starts from the CPUCLKOUT pin of the core and goes inside the core again through the CPUCLKIN pin after passing through a chip-level clock tree synthesis (CTS) buffer. Similarly, IMUCLK domain starts from IMUCLKOUT pin of the core and goes inside the core again through IMUCLKIN pin after passing through a chip-level CTS buffer. SYSCLK domain is a chip-level clock domain that starts from the SYSCLKOUT pin of the core and is used for chip-level clocking. In a cDSP using the T320C2700B0 core, the skew across the three clock domains is balanced by ensuring that all three see the same insertion delay.

Within the core, CPUCLK and IMUCLK are matched; therefore, they have the same insertion delay.

Figure 8 shows the clocking scheme for the T320C2700B0 core.

clocking (continued)

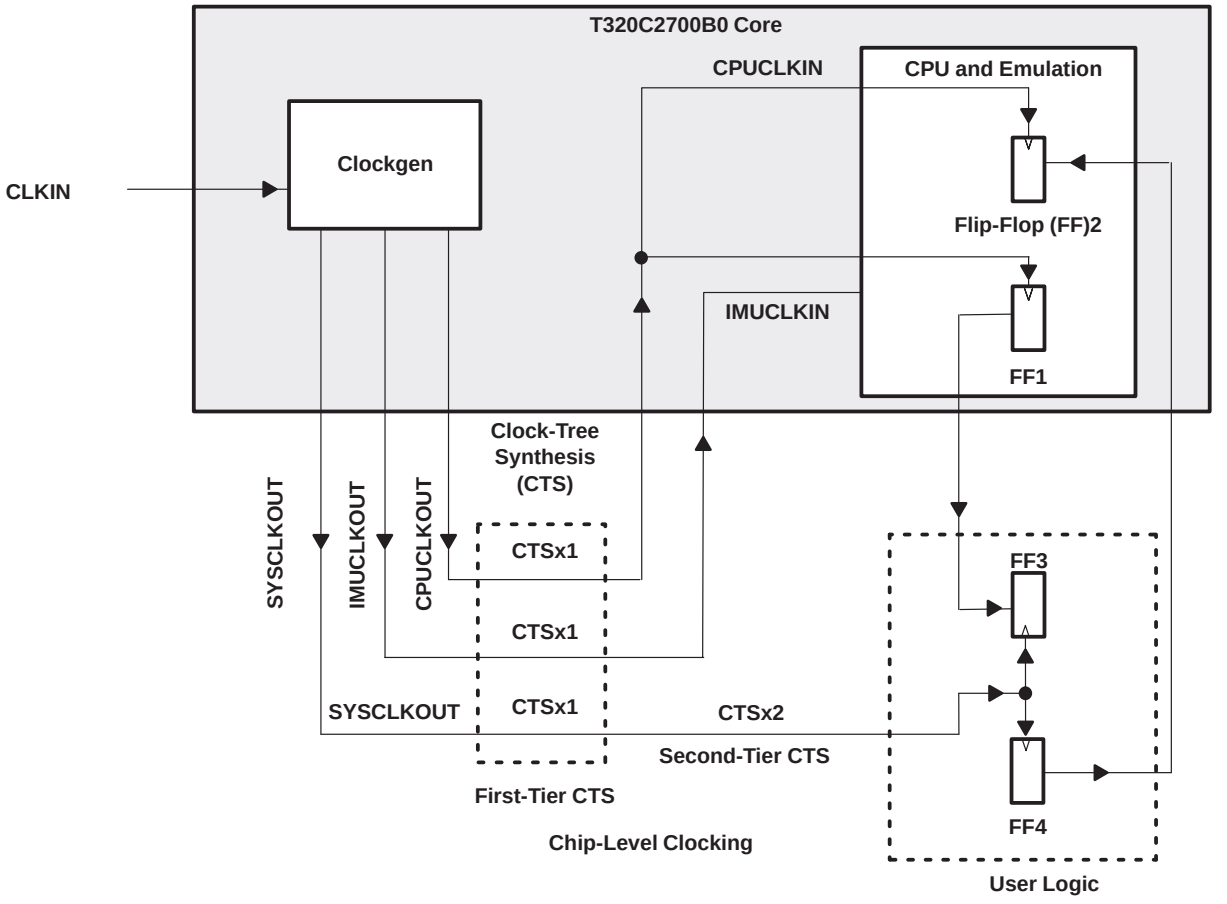


Figure 8. Clocking Scheme of the Core

The value of the insertion delay to be specified for each CTS buffer is determined as follows:

Where

Tins_CORE = Insertion delay of the clock tree within the core

Tins_CTSx1 = Insertion delay of the CTS macro used for first-tier clocking for the user logic

Tins_CTSx2 = Insertion delay of the CTS macro used for second-tier clocking for the user logic

Tins_CPUCLK = Insertion delay that must be specified for the chip-level CPU_CLOCK

Tins_IMUCLK = Insertion delay that must be specified for chip-level IMU_CLOCK

For all the clocks to be balanced, the insertion delays must be specified such that the following condition holds true:

Tins_CORE + Tins_CPUCLK = Tins_CTSx1 + Tins_CTSx2

Since the insertion delay for the CPUCLK and IMUCLK inside the core are the same, Tins_IMUCLK equals Tins_CPUCLK at the chip level.

clocking (continued)

A second level of fine tuning could be needed if there is any skew between the arrival of CPUCLKOUT, IMUCLKOUT, and SYSCLKOUT to the root of the respective CTS buffers in the chip. This skew must be extracted after the layout and must be fed to the CTS flow for a second level of fine tuning. If the CTS buffers at the chip level are placed close to the core clock outputs, there is not much difference between the arrival time of the three clocks to the root of CTS buffers, and the second level of fine tuning could be avoided.

CPUCLK and IMUCLK are brought out of the core instead of being connected internally to the CPU to compensate for the case when Tins_CTSxx > Tins_CORE. In this case, the addition of some insertion delay in the CPUCLK and IMUCLK domains is required. This delay can be done only at the chip level because the the core is a fixed module.

See the *TSC6000 0.18-* μ*m CMOS Standard Cell Macro Library Summary* (literature number SRSS040) for more information on the clocking scheme.

reset and interrupt

Reset (RSn) is a nonmaskable external interrupt that can be used to put the core in a known state at any time. RSn has the highest priority and no other interrupt takes precedence over reset. Reset is typically applied during power up to put the core in a known state. It is also applied at any time there is a need to abort all operations and put the core into a known state.

RSn signal

The reset operation is initiated by driving the RSn signal low with a synchronous input that satisfies a constraint at the rising edge of the clock as shown in Figure 9. The core latches the active reset input and extends it long enough to ensure a proper termination of all operations in the pipeline and setting all the registers to their initialization values. The core also has an output signal (SYSRSn) that indicates that the core is undergoing a reset operation.

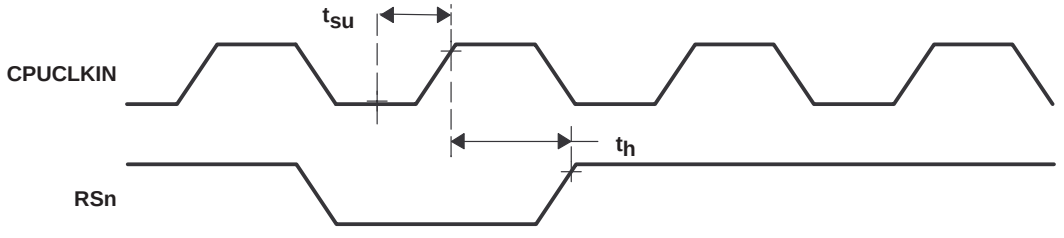


Figure 9. RSn/Clock Waveform

SYSRSn

SYSRSn is a synchronous output signal generated by the core to indicate that the CPU is undergoing a reset operation. This signal goes active (low) two cycles after the RSn signal goes active (low). Since the reset is internally extended, the duration for which SYSRSn remains active (low) depends on how long the RSn signal was held low. If the RSn signal is held low for more than nine cycles, the SYSRSn signal goes inactive (high) six cycles after RSn goes inactive (high). An RSn input signal at least nine cycles wide is recommended to ensure a definite cycle delay between RSn and SYSRSn.

The purpose of the SYSRSn signal is to have a synchronous output from the CPU that notifies all connected components that the CPU is undergoing a reset operation. The components can use this output signal to reset their respective internal logic and states. New requests from the CPU commence only after the SYSRSn signal goes inactive (high). No request or useful operation can be performed by the CPU when SYSRSn is active (low).

SYSRSn (continued)

The implications of SYSRSn going active for components like memory wrappers and interface bridges are as follow:

- Memory wrappers and interface bridges must abort currently active requests and drive all the READY (POREADY, DROREADY, AND DWOREADY) signals high.
- Stored requests must be cleared and all state machines that are used to manipulate wait state generation, write buffering, and other operations must be reset to their initialization states.
- All wrappers and interface bridges synchronously change states to an inactive condition and wait for a new CPU request to be issued.

RSn operation

The following operations are performed inside the CPU whenever it undergoes a reset:

- All instructions in the pipeline are flushed out and are treated as NOPs.
- No further memory requests are made by the CPU. Data being driven back for an earlier read request are ignored.
- All NOT-READY (low input on DROREADY, DWOREADY, OR POREADY) conditions are ignored.
- All CPU registers are initialized as follow:

T = 0	AR3 = 0	ST1 = B/3h†
P = 0	AR4 = 0	DP = 0
ACC = 0	AR5 = 0	SP = 0
AR0 = 0	XAR6 = 0	IER = 0
AR1 = 0	XAR7 = 0	IFR = 0
AR2 = 0	ST0 = 0	

† VMAP signal sampled on the rising edge of SYSRSn is written into bit 3 of ST1.

- Once RSn goes inactive (high), program execution commences by performing a reset-vector fetch. The reset vector location is determined by the VMAP input signal that is sample on the rising edge of SYSRSn. If VMAP is sampled high, the reset vector is fetched from location 0x3FFFC0 in program space. If VMAP is sampled low, the reset vector is fetched from location 0x000000.

debug and emulation considerations

During debug and emulation, certain special conditions can arise and these must be considered when designing a system. The core adopts a debug and emulation mechanism that is activated by way of the test access port (TAP). Driving the TRSTn signal low disables all the debug- and emulation-related logic and puts the CPU in the normal user mode. However, when debug and emulation are active, the following operations (related to reset) are possible:

- Through the TAP, it is possible to disconnect the RSn input internally so that it does not affect the CPU. In this mode, driving RSn active has no effect on the CPU operations since it has been disconnected internally.
- Through the TAP, it is possible to set the reset control logic in a mode where active resets are extended indefinitely. This means that if RSn pulses low for even one cycle, the CPU enters a reset state and remains in this state indefinitely until the reset control logic is modified through the debug interface.

debug and emulation considerations (continued)

- It is possible to mask the RSn input during stop mode emulation. RSn going active is recorded, but does not take effect until the time a suitable execution control directive occurs from the TAP. Therefore, if RSn goes active multiple times before the first one takes effect, the CPU and the rest of the system see it as a single reset.
- Through the TAP, it is possible to put the CPU in a reset state, hold it in the reset state for any desired amount of time, and also to bring it out of a reset state.

test considerations

For test reasons, two memory blocks, B0 and B1, are essential on every cDSP device using the T32C2700 core. During core test, it is important to isolate the core, B0 and B1 from other logic. For this reason, separate control signals are defined for B0 and B1 even though they are like any other memory block connecting to the memory interface.

Two types of control signals related to memory reads and writes are driven by the memory devices and interface bridges to the CPU. The purpose of each signal type is as follows:

- To request a wait state from the CPU
  Example: POREADY[5:0], DWOREADY[5:0], or DROREADY[5:0]

  These signals indicate to the CPU whether the requested operation can be completed in the same cycle. Driving these signals low indicates to the CPU that the requested operation cannot be completed in the same cycle.

  This class of signals is normally held high and is pulled low only if extra cycles are needed for an operation to complete. Unused signals of this class must be tied high.
- To indicate data being driven to the CPU
  Example: PRDY and DRDY

  These signals indicate to the CPU that the data bus of the corresponding port is being driven. The signals are driven active (high) on the same cycle as the data is driven. For example, PRDY is driven high on the same cycle a memory drives PRDB[31:0] in response to a program-space-read access.

  This class of signals is normally held low. Only when data is being driven to the core should these signals be driven high by memory devices and interface bridges. Unused signals of this class must be tied low.

timing tables

Table 8 through Table 10 list the input capacitances, setup, hold, minimum pulse, and delay times. Figure 10

Table 8. Input Capacitances

REFERENCE SIGNAL	CAPACITANCE	UNITS	REFERENCE SIGNAL	CAPACITANCE	UNITS
AEVTQUAL	11.66	SL	EXTTRGR	17.97	SL
ANASTOP	12.40	SL	IMUCLKIN	5.75	SL
B0B1DRDY	29.41	SL	INTn[13:0]	28.67	SL
B0B1PRDY	48.90	SL	MONPRIV	28.75	SL
B0DROREADY	32.81	SL	NMIn	34.77	SL
B0DWOREADY	34.95	SL	PERISCOUT	28.77	SL
B0POREADY	6.75	SL	PERISCPATH	68.42	SL
B1DROREADY	32.50	SL	POREADY(5:0)	6.63	SL
B1DWOREADY	33.77	SL	PRDB(31:0)	6.84	SL
B1POREADY	10.59	SL	PRDY	22.44	SL
BREAKHI	18.18	SL	PROTRANGE[15:0]	7.51	SL
BREAKLO	17.45	SL	PROTSTART[15:0]	15.26	SL
CLKIN	8.00	SL	RSn	12.97	SL
CPUCLKIN	5.93	SL	RTOSINTn	20.69	SL
CTOOLSACK	50.10	SL	SLAVEIN	5.76	SL
DEVTQUAL	20.76	SL	TCK	33.98	SL
DRDB[31:0]	22.18	SL	TDI	66.74	SL
DRDY	5.49	SL	TMS	111.38	SL
DROREADY[5:0]	8.23	SL	TRACEHI	8.09	SL
DWOREADY[5:0]	6.52	SL	TRACELO	8.68	SL
ENPROT	75.16	SL	TRSTn	97.86	SL
ET0I	87.51	SL	UBUS[31:0]	4.68	SL
ET1I	96.28	SL	USER0[3:0]	3.24	SL
EXTCNT0	19.94	SL	USER1[3:0]	3.27	SL
EXTCNT1	23.34	SL	VMAP	52.53	SL

timing tables (continued)

Table 9. Setup, Hold, and Minimum Pulse-Width Data (See Notes 1 through 9)

PARAM	SIG1	SIG2	MIN	NOM	MAX
t_{su}	AEVTQUAL	CPUCLKIN	–0.1074	–0.2246	–0.3418
t_{su}	AEVTQUAL	IMUCLKIN	1.2305	1.6602	2.3438
t_{su}	ANASTOP	CPUCLKIN	–0.1074	–0.2148	–0.3320
t_{su}	ANASTOP	IMUCLKIN	0.0781	0.0488	0.0293
t_{su}	B0B1DRDY	CPUCLKIN	1.7969	2.4512	3.5254
t_{su}	B0B1PRDY	CPUCLKIN	1.8262	2.4609	3.5254
t_{su}	B0DROREADY	CPUCLKIN	1.2035	1.7699	2.6195
t_{su}	B0DROREADY	IMUCLKIN	1.1816	1.5918	2.2266
t_{su}	B0DWOREADY	CPUCLKIN	1.4012	1.8406	2.5633
t_{su}	B0DWOREADY	IMUCLKIN	1.0547	1.5723	2.2949
t_{su}	B0POREADY	CPUCLKIN	1.5598	2.1555	3.0441
t_{su}	B0POREADY	IMUCLKIN	1.4356	1.9238	2.6172
t_{su}	B1DROREADY	CPUCLKIN	1.3035	1.8699	2.7098
t_{su}	B1DROREADY	IMUCLKIN	1.2402	1.6602	2.3047
t_{su}	B1DWOREADY	CPUCLKIN	1.3402	1.7992	2.5219
t_{su}	B1DWOREADY	IMUCLKIN	1.0547	1.5625	2.2852
t_{su}	B1POREADY	CPUCLKIN	1.6305	2.2066	3.0856
t_{su}	B1POREADY	IMUCLKIN	1.4551	1.9531	2.6465
t_{su}	BREAKHI	CPUCLKIN	–0.0977	–0.2051	–0.3223
t_{su}	BREAKHI	IMUCLKIN	0.1758	0.1465	0.1953
t_{su}	BREAKLO	CPUCLKIN	–0.1074	–0.2148	–0.3320
t_{su}	BREAKLO	IMUCLKIN	0.1562	0.1172	0.1270
t_{su}	CTOOLSACK	CPUCLKIN	2.0312	2.7441	3.9258
t_{su}	DEVTQUAL	CPUCLKIN	–0.0781	–0.1953	–0.3125
t_{su}	DEVTQUAL	IMUCLKIN	1.1621	1.7285	2.5098
t_{su}	DRDB	CPUCLKIN	0.4199	0.6641	0.9766
t_{su}	DRDY	CPUCLKIN	1.5137	2.1973	3.1445
t_{su}	DROREADY	CPUCLKIN	1.3109	1.7699	2.5023
t_{su}	DROREADY	IMUCLKIN	1.0254	1.5332	2.2461
t_{su}	DWOREADY	CPUCLKIN	1.1914	1.6309	2.3340
t_{su}	DWOREADY	IMUCLKIN	1.0059	1.4551	2.1387
t_{su}	ENPROT	CPUCLKIN	0.2344	0.1172	0.0000

NOTES:
1. Timing values are in nanoseconds.
2. t_{su} denotes setup time for input port (signal 1) with respect to clock (signal 2).
3. th denotes hold time for input port (signal 2) with respect to clock (signal 1).
4. $\overline{tw}$ denotes minimum pulse width.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
8. Setup time values were characterized a slew of 2 ns on the input port (SIG1) and a slew of 0.083 ns on the clock (SIG2).
9. Hold time values were characterized a slew of 0.083 ns on the input port (SIG2) and a slew of 2 ns on the clock (SIG1).

timing tables (continued)

Table 9. Setup, Hold, and Minimum Pulse-Width Data (See Notes 1 through 9) (Continued)

PARAM	SIG1	SIG2	MIN	NOM	MAX
t_{su}	ET0I	IMUCLKIN	0.5859	0.8887	1.2598
t_{su}	ET0I	TRSTn	0.3320	0.4980	0.7227
t_{su}	ET1I	IMUCLKIN	0.6641	0.9668	1.3477
t_{su}	ET1I	TRSTn	0.4199	0.5078	0.7129
t_{su}	EXTCNT0	CPUCLKIN	–0.0977	–0.2051	–0.3223
t_{su}	EXTCNT0	IMUCLKIN	0.0684	0.0195	–0.0098
t_{su}	EXTCNT1	CPUCLKIN	–0.0781	–0.1855	–0.3125
t_{su}	EXTCNT1	IMUCLKIN	0.0586	–0.0098	–0.0586
t_{su}	EXTTRGR	CPUCLKIN	–0.0977	–0.2148	–0.3320
t_{su}	EXTTRGR	IMUCLKIN	1.0254	1.3477	1.8359
t_{su}	INTn	CPUCLKIN	0.0879	0.0391	–0.0195
t_{su}	INTn	IMUCLKIN	0.1074	0.1953	0.3027
t_{su}	MONPRIV	CPUCLKIN	–0.0684	–0.1758	–0.3027
t_{su}	MONPRIV	IMUCLKIN	1.8262	2.4707	3.4473
t_{su}	MONPRIV	TCK	0.7031	1.0156	1.5723
t_{su}	NMIn	CPUCLKIN	0.0586	0.0000	–0.0586
t_{su}	NMIn	IMUCLKIN	0.4492	0.7227	1.0059
t_{su}	POREADY	CPUCLKIN	1.4426	2.0383	2.9562
t_{su}	POREADY	IMUCLKIN	1.3770	1.8555	2.5391
t_{su}	PRDB	CPUCLKIN	1.3965	1.9727	2.8516
t_{su}	PRDB	IMUCLKIN	0.7520	1.1816	1.7871
t_{su}	PRDY	CPUCLKIN	1.6504	2.2754	3.3496
t_{su}	PROTRANGE	CPUCLKIN	–0.3613	–0.5859	–0.9570
t_{su}	PROTSTART	CPUCLKIN	–0.3809	–0.6055	–0.9766
t_{su}	RSn	CPUCLKIN	0.0195	–0.0293	–0.0977
t_{su}	RSn	IMUCLKIN	0.7227	1.1328	1.6602
t_{su}	RTOSINTn	CPUCLKIN	0.0000	–0.0488	–0.1074
t_{su}	RTOSINTn	IMUCLKIN	0.5078	0.8008	1.1719
t_{su}	TDI	TCK	0.2832	0.3320	0.4492
t_{su}	TMS	TCK	0.3711	0.5176	0.7617
t_{su}	TRACEHI	CPUCLKIN	–0.0977	–0.2051	–0.3223
t_{su}	TRACEHI	IMUCLKIN	0.0293	–0.0391	–0.0879

NOTES: 1. Timing values are in nanoseconds.
2. t_{su} denotes setup time for input port (signal 1) with respect to clock (signal 2).
3. th denotes hold time for input port (signal 2) with respect to clock (signal 1).
4. tw denotes minimum pulse width.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
8. Setup time values were characterized a slew of 2 ns on the input port (SIG1) and a slew of 0.083 ns on the clock (SIG2).
9. Hold time values were characterized a slew of 0.083 ns on the input port (SIG2) and a slew of 2 ns on the clock (SIG1).

timing tables (continued)

Table 9. Setup, Hold, and Minimum Pulse-Width Data (See Notes 1 through 9) (Continued)

PARAM	SIG1	SIG2	MIN	NOM	MAX
t_{su}	TRACELO	CPUCLKIN	–0.0977	–0.2051	–0.3223
t_{su}	TRACELO	IMUCLKIN	–0.0684	–0.1758	–0.3516
t_{su}	TRSTn	TCK	0.0195	0.0781	0.1172
t_{su}	UBUS	CPUCLKIN	–0.0684	–0.1758	–0.2930
t_{su}	UBUS	IMUCLKIN	2.2754	3.1738	4.5606
t_{su}	USER0	IMUCLKIN	1.0938	1.4453	2.0898
t_{su}	USER1	IMUCLKIN	1.1426	1.5137	2.0703
t_{su}	VMAP	CPUCLKIN	0.0781	–0.0293	–0.1465
t_{su}	VMAP	IMUCLKIN	0.4980	0.6934	0.9961
t_h	CPUCLKIN	AEVTQUAL	0.6445	0.8789	1.1816
t_h	IMUCLKIN	AEVTQUAL	–0.0977	–0.1367	–0.2246
t_h	CPUCLKIN	ANASTOP	0.6445	0.8789	1.1816
t_h	IMUCLKIN	ANASTOP	0.3418	0.4883	0.7227
t_h	CPUCLKIN	B0B1DRDY	0.6445	0.8984	1.2207
t_h	CPUCLKIN	B0B1PRDY	0.5957	0.8398	1.1621
t_h	CPUCLKIN	B0DROREADY	0.5762	0.7812	1.0352
t_h	IMUCLKIN	B0DROREADY	–0.4004	–0.5762	–0.8594
t_h	CPUCLKIN	B0DWOREADY	0.5469	0.7324	0.9863
t_h	IMUCLKIN	B0DWOREADY	–0.4492	–0.6348	–0.9375
t_h	CPUCLKIN	B0POREADY	0.3320	0.4492	0.5859
t_h	IMUCLKIN	B0POREADY	–0.3320	–0.4785	–0.7617
t_h	CPUCLKIN	B1DROREADY	0.5664	0.7715	1.0156
t_h	IMUCLKIN	B1DROREADY	–0.3516	–0.4980	–0.7520
t_h	CPUCLKIN	B1DWOREADY	0.5371	0.7324	0.9570
t_h	IMUCLKIN	B1DWOREADY	–0.4590	–0.6543	–0.9668
t_h	CPUCLKIN	B1POREADY	0.4395	0.5957	0.8301
t_h	IMUCLKIN	B1POREADY	–0.3320	–0.4883	–0.7715
t_h	CPUCLKIN	BREAKHI	0.6348	0.8691	1.1719
t_h	IMUCLKIN	BREAKHI	0.2734	0.3809	0.5469
t_h	CPUCLKIN	BREAKLO	0.6445	0.8789	1.1719
t_h	IMUCLKIN	BREAKLO	0.3027	0.4199	0.5957
t_h	CPUCLKIN	CTOOLSACK	0.5566	0.7910	1.0840

NOTES:
1. Timing values are in nanoseconds.
2. t_{su} denotes setup time for input port (signal 1) with respect to clock (signal 2).
3. th denotes hold time for input port (signal 2) with respect to clock (signal 1).
4. tw denotes minimum pulse width.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
8. Setup time values were characterized a slew of 2 ns on the input port (SIG1) and a slew of 0.083 ns on the clock (SIG2).
9. Hold time values were characterized a slew of 0.083 ns on the input port (SIG2) and a slew of 2 ns on the clock (SIG1).

timing tables (continued)

**Table 9. Setup, Hold, and Minimum Pulse-Width Data
(See Notes 1 through 9) (Continued)**

PARAM	SIG1	SIG2	MIN	NOM	MAX
t_h	CPUCLKIN	DEVTQUAL	0.6348	0.8789	1.1816
t_h	IMUCLKIN	DEVTQUAL	0.0488	0.0586	0.0195
t_h	CPUCLKIN	DRDB	0.7227	1.0352	1.5039
t_h	CPUCLKIN	DRDY	0.6445	0.8789	1.1719
t_h	CPUCLKIN	DROREADY	0.4395	0.5859	0.7422
t_h	IMUCLKIN	DROREADY	–0.3809	–0.5469	–0.8398
t_h	CPUCLKIN	DWOREADY	0.4590	0.6152	0.7812
t_h	IMUCLKIN	DWOREADY	–0.3809	–0.5371	–0.8105
t_h	CPUCLKIN	ENPROT	0.4785	0.7031	0.9863
t_h	IMUCLKIN	ET0I	0.4785	0.7031	1.0449
t_h	TRSTn	ET0I	–0.1465	–0.1465	–0.2051
t_h	IMUCLKIN	ET1I	0.4687	0.6934	1.0449
t_h	TRSTn	ET1I	–0.1855	–0.1855	–0.2246
t_h	CPUCLKIN	EXTCNT0	0.6348	0.8789	1.1719
t_h	IMUCLKIN	EXTCNT0	0.3613	0.5176	0.7715
t_h	CPUCLKIN	EXTCNT1	0.6348	0.8691	1.1719
t_h	IMUCLKIN	EXTCNT1	0.3906	0.5566	0.8203
t_h	CPUCLKIN	EXTTRGR	0.6445	0.8789	1.1816
t_h	IMUCLKIN	EXTTRGR	0.2148	0.3223	0.4687
t_h	CPUCLKIN	INTn	0.6152	0.8398	1.1426
t_h	IMUCLKIN	INTn	0.3418	0.4687	0.6836
t_h	CPUCLKIN	MONPRIV	0.6250	0.8691	1.1719
t_h	IMUCLKIN	MONPRIV	0.0586	0.0781	0.0977
t_h	TCK	MONPRIV	–0.0684	–0.1562	–0.3613
t_h	CPUCLKIN	NMIn	0.6055	0.8301	1.1328
t_h	IMUCLKIN	NMIn	0.0879	0.1074	0.0488
t_h	CPUCLKIN	POREADY	0.3027	0.3906	0.4687
t_h	IMUCLKIN	POREADY	–0.3027	–0.4590	–0.7520
t_h	CPUCLKIN	PRDB	0.6738	0.9180	1.2402
t_h	IMUCLKIN	PRDB	0.1562	0.2051	0.2344
t_h	CPUCLKIN	PRDY	0.6250	0.8691	1.1621
t_h	CPUCLKIN	PROTRANGE	0.7422	1.0547	1.5234

NOTES: 1. Timing values are in nanoseconds.
2. t_{su} denotes setup time for input port (signal 1) with respect to clock (signal 2).
3. th denotes hold time for input port (signal 2) with respect to clock (signal 1).
4. tw denotes minimum pulse width.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
8. Setup time values were characterized a slew of 2 ns on the input port (SIG1) and a slew of 0.083 ns on the clock (SIG2).
9. Hold time values were characterized a slew of 0.083 ns on the input port (SIG2) and a slew of 2 ns on the clock (SIG1).

timing tables (continued)

**Table 9. Setup, Hold, and Minimum Pulse-Width Data
(See Notes 1 through 9) (Continued)**

PARAM	SIG1	SIG2	MIN	NOM	MAX
t_h	CPUCLKIN	PROTSTART	0.7324	1.0449	1.5234
t_h	CPUCLKIN	RSn	0.6250	0.8594	1.1523
t_h	IMUCLKIN	RSn	–0.0586	–0.0977	–0.2441
t_h	CPUCLKIN	RTOSINTn	0.6250	0.8594	1.1523
t_h	IMUCLKIN	RTOSINTn	–0.0293	–0.0391	–0.1074
t_h	TCK	TDI	0.3320	0.4492	0.5762
t_h	TCK	TMS	0.1953	0.3613	0.5762
t_h	CPUCLKIN	TRACEHI	0.6348	0.8789	1.1816
t_h	IMUCLKIN	TRACEHI	0.3906	0.5469	0.7715
t_h	CPUCLKIN	TRACELO	0.6348	0.8789	1.1816
t_h	IMUCLKIN	TRACELO	0.4883	0.6836	0.9766
t_h	TCK	TRSTn	0.7129	1.0156	1.4648
t_h	CPUCLKIN	UBUS	0.6543	0.8887	1.1914
t_h	IMUCLKIN	UBUS	0.1270	0.1465	0.1172
t_h	IMUCLKIN	USER0	–0.5078	–0.7715	–1.2305
t_h	IMUCLKIN	USER1	–0.4297	–0.6738	–1.1426
t_h	CPUCLKIN	VMAP	0.5566	0.7910	1.0840
t_h	IMUCLKIN	VMAP	–0.0098	–0.0195	–0.0684
t_w	CPUCLKIN	CPUCLKIN	3.7500	3.7500	3.7500
t_w	CPUCLKIN	CPUCLKIN	3.7500	3.7500	3.7500
t_w	EXTTRGR	EXTTRGR	20.0000	20.0000	20.0000
t_w	EXTTRGR	EXTTRGR	20.0000	20.0000	20.0000
t_w	IMUCLKIN	IMUCLKIN	3.7500	3.7500	3.7500
t_w	IMUCLKIN	IMUCLKIN	3.7500	3.7500	3.7500
t_w	TCK	TCK	3.7500	3.7500	3.7500
t_w	TCK	TCK	3.7500	3.7500	3.7500
t_w	TRSTn	TRSTn	20.0000	20.0000	20.0000
t_w	TRSTn	TRSTn	20.0000	20.0000	20.0000

NOTES: 1. Timing values are in nanoseconds.
2. t_{su} denotes setup time for input port (signal 1) with respect to clock (signal 2).
3. th denotes hold time for input port (signal 2) with respect to clock (signal 1).
4. tw denotes minimum pulse width.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
8. Setup time values were characterized a slew of 2 ns on the input port (SIG1) and a slew of 0.083 ns on the clock (SIG2).
9. Hold time values were characterized a slew of 0.083 ns on the input port (SIG2) and a slew of 2 ns on the clock (SIG1).

timing tables (continued)

Table 10. Output Delays (See Notes 1, 5, 6, 7, and 10)

INPUT PORT	OUTPUT PORT	T_{PLH}		T_{PHL}	
		MIN	MAX	MIN	MAX
IMUCLKIN	ABORTREADY	1.70	2.97	1.60	3.01
TCK	COREATPG	2.53	5.13	2.43	4.90
TCK	COREFTEST	1.47	2.87	1.31	2.62
CPUCLKIN	CPUSTAT	1.71	2.93	1.61	2.98
IMUCKLIN	CSTOPPING	1.55	2.79	1.47	2.83
CPUCLKIN	DBGACCESSP	1.66	2.88	1.60	2.96
CPUCLKIN	DBGACCESSR	1.65	3.06	1.52	2.97
CPUCLKIN	DBGACCESSW	1.97	3.18	1.93	3.34
IMUCKLIN	DBGACK	1.93	3.39	1.85	3.47
IMUCKLIN	DBGM	1.43	2.65	1.37	2.68
CPUCLKIN	DBGPTYPE	1.64	3.29	1.59	3.26
IMUCKLIN	DBGPTYPE	2.30	4.58	2.20	4.47
CPUCLKIN	DBGRTYPE	1.61	2.85	1.53	2.89
CPUCLKIN	DBGWTYPE	2.00	4.03	1.82	3.66
IMUCLKIN	DCON	1.87	3.14	1.75	3.19
IMUCLKIN	DFC	1.82	3.21	1.67	3.17
CPUCLKIN	DRAB	1.75	3.51	1.58	3.23
CPUCLKIN	DRDS0	1.75	3.18	1.60	3.08
CPUCLKIN	DRDS1	1.75	3.16	1.61	3.08
CPUCLKIN	DRLSB	1.54	3.06	1.41	2.83
CPUCLKIN	DRMSB	1.53	3.03	1.40	2.83
CPUCLKIN	DWAB	1.48	2.99	1.39	2.86
CPUCLKIN	DWDB	1.57	3.21	1.45	3.02
CPUCLKIN	DWDS0	1.46	2.90	1.34	2.73
CPUCLKIN	DWDS1	1.54	3.06	1.39	2.83
CPUCLKIN	DWLSB	1.48	2.93	1.36	2.77
CPUCLKIN	DWMSB	1.56	3.08	1.41	2.87
IMUCLKIN	EALLOW	1.55	2.79	1.46	2.83
IMUCLKIN	ET0O	1.24	2.46	1.18	2.44
IMUCLKIN	ET0Z	1.94	3.80	1.82	3.81
IMUCLKIN	ET1O	1.26	2.49	1.20	2.46
IMUCLKIN	ET1Z	1.81	3.61	1.72	3.69
IMUCLKIN	HERMIT	1.59	2.79	1.53	2.88
CPUCLKIN	IACK	1.75	2.96	1.66	3.05
CPUCLKIN	IAQ	1.50	2.70	1.44	2.75
CPUCLKIN	IDLE	1.68	3.04	1.57	3.02

NOTES: 1. Timing values are in nanoseconds.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
10. The timing values were measured assuming a slew of 1.5 ns on the input port and a load of 64 SL (1SL = 0.00766 pF) on the output port.

timing tables (continued)

Table 10. Output Delays (See Notes 1, 5, 6, 7, and 10) (Continued)

INPUT PORT	OUTPUT PORT	T_{PLH}		T_{PHL}	
		MIN	MAX	MIN	MAX
CPUCLKIN	IFSTAT	1.62	3.00	1.50	2.93
TCK	MEMXFTEST	1.53	3.03	1.62	3.22
IMUCLKIN	MONPRIVO	1.37	2.72	1.33	2.76
TCK	MONPRIVO	3.54	6.88	3.48	7.03
CPUCLKIN	PAB	1.74	3.39	1.54	3.04
CPUCLKIN	PCFS	1.89	3.13	1.80	3.22
TCK	PERIATPG	2.24	4.68	2.22	4.57
TCK	PERISCANEN	2.05	3.94	2.02	3.90
CPUCLKIN	PRDS0	1.61	3.15	1.45	2.91
CPUCLKIN	PRDS1	1.47	2.94	1.34	2.75
CPUCLKIN	PSTAT	1.51	3.00	1.38	2.81
CPUCLKIN	PWDS0	1.47	2.94	1.35	2.75
CPUCLKIN	PWDS1	1.45	2.88	1.34	2.72
TCK	PWRABORT	1.30	2.38	1.24	2.38
TCK	RESERVED1	1.65	3.22	1.57	3.14
TCK	RESERVED2	2.01	3.89	1.87	3.80
IMUCLKIN	RESETOUT	1.86	3.46	1.80	3.59
CPUCLKIN	RSTAT	1.71	2.95	1.63	3.00
CPUCLKIN	SYSRSn	1.37	2.58	1.30	2.57
TCK	TDOZ	2.79	4.99	2.74	4.88
TCK	TDO	2.70	5.23	2.67	5.52
CPUCLKIN	VBANZ	1.45	2.69	1.37	2.69
CPUCLKIN	VCOND	1.58	2.94	1.48	2.88
CPUCLKIN	VDISCINSTR	1.39	2.60	1.32	2.62
CPUCLKIN	VDRDB	1.65	2.85	1.57	2.93
CPUCLKIN	VECT	1.42	2.66	1.34	2.66
IMUCLKIN	VHPI	1.58	3.08	1.44	2.89
CPUCLKIN	VINDRCT	1.33	2.55	1.26	2.55
CPUCLKIN	VINSTRJAM	1.31	2.53	1.24	2.52
CPUCLKIN	VIREG	1.66	3.30	1.56	3.17
CPUCLKIN	VMAC	1.31	2.53	1.24	2.52
IMUCLKIN	VMAPS	1.44	2.71	1.34	2.69
CPUCLKIN	VNEWINSTR	1.32	2.56	1.25	2.54
CPUCLKIN	VPAGE0	1.77	3.27	1.61	3.11
CPUCLKIN	VPCDISC	1.45	2.68	1.38	2.70
CPUCLKIN	VPC	1.63	3.23	1.45	2.92

NOTES: 1. Timing values are in nanoseconds.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
10. The timing values were measured assuming a slew of 1.5 ns on the input port and a load of 64 SL (1SL = 0.00766 pF) on the output port.

PRODUCT PREVIEW

timing tables (continued)

Table 10. Output Delays (See Notes 1, 5, 6, 7, and 10) (Continued)

INPUT PORT	OUTPUT PORT	T_{PLH}		T_{PHL}	
		MIN	MAX	MIN	MAX
CPUCLKIN	VPIPEPROT	1.36	2.58	1.29	2.58
CPUCLKIN	VPRDB	1.46	2.70	1.38	2.70
CPUCLKIN	VPREAD	1.38	2.60	1.31	2.60
CPUCLKIN	VPWRITE	1.45	2.66	1.38	2.69
CPUCLKIN	VRESET	1.58	3.08	1.44	2.90
CPUCLKIN	VRPTINSTR	1.52	2.83	1.42	2.79
CPUCLKIN	VSPR	1.48	2.70	1.40	2.72
CPUCLKIN	VSPW	1.55	2.76	1.47	2.80
CPUCLKIN	WSTAT	1.54	2.89	1.44	2.82
TCK	XLOGOFF	3.01	5.93	2.87	5.67
CLKIN	CPUCLKOUT	0.75	1.64	0.85	1.47
CLKIN	IMUCLKOUT	0.74	1.64	0.84	1.47
CLKIN	SYSCLKOUT	0.74	1.63	0.84	1.46
ET0I	COREATPG	1.20	2.49	0.99	1.91
ET0I	COREFTEST	1.27	2.50	1.06	1.95
ET0I	MEMXFTEST	1.21	2.53	0.99	1.87
ET0I	PERIATPG	1.16	2.41	1.00	1.91
ET0I	CPUCLKOUT	1.53	3.12	1.26	2.50
ET0I	IMUCLKOUT	1.53	3.12	1.26	2.50
ET0I	SYSCLKOUT	1.53	3.12	1.26	2.50
ET0I	XLOGOFF	1.36	2.44	1.48	3.01
ET1I	COREATPG	1.20	2.47	1.08	2.00
ET1I	COREFTEST	1.27	2.49	1.15	2.04
ET1I	MEMXFTEST	1.21	2.52	1.08	1.96
ET1I	PERIATPG	1.15	2.39	1.09	2.00
ET1I	CPUCLKOUT	1.53	3.11	1.35	2.59
ET1I	IMUCLKOUT	1.53	3.11	1.35	2.59
ET1I	SYSCLKOUT	1.53	3.11	1.35	2.59
ET1I	XLOGOFF	1.46	2.53	1.48	2.99
MONPRIV	MONPRIVO	0.96	1.76	1.00	1.65
PERISCOUT	TDO	1.38	2.50	1.62	2.73
PERISCPATH	TDO	1.37	2.45	1.70	2.82
SLAVEIN	COREATPG	0.98	1.63	0.80	1.65
SLAVEIN	COREFTEST	1.04	1.65	0.86	1.69
SLAVEIN	CPUCLKOUT	1.32	2.28	1.08	2.25
SLAVEIN	IMUCLKOUT	1.32	2.28	1.08	2.25

NOTES: 1. Timing values are in nanoseconds.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
10. The timing values were measured assuming a slew of 1.5 ns on the input port and a load of 64 SL (1SL = 0.00766 pF) on the output port.

timing tables (continued)

Table 10. Output Delays (See Notes 1, 5, 6, 7, and 10) (Continued)

INPUT PORT	OUTPUT PORT	T_{PLH}		T_{PHL}	
		MIN	MAX	MIN	MAX
SLAVEIN	MEMXFTEST	0.99	1.68	0.80	1.62
SLAVEIN	PERIATPG	0.94	1.55	1.81	1.66
SLAVEIN	SYSCLKOUT	1.32	2.28	1.08	2.25
SLAVEIN	XLOGOFF	1.19	2.19	1.27	2.17
TCK	CPUCLKOUT	1.07	2.44	1.32	2.48
TCK	IMUCLKOUT	1.07	2.44	1.31	2.48
TCK	SYSCLKOUT	1.04	2.39	1.29	2.44
TRSTn	COREATPG	1.28	2.33	0.97	1.87
TRSTn	COREFTEST	1.35	2.34	1.03	1.91
TRSTn	CPUCLKOUT	1.62	2.96	1.24	2.46
TRSTn	IMUCLKOUT	1.62	2.96	1.24	2.46
TRSTn	ET0Z	0.89	1.28	0.61	1.28
TRSTn	ET1Z	0.76	1.09	0.51	1.10
TRSTn	MEMXFTEST	1.29	2.37	0.97	1.83
TRSTn	PERIATPG	1.24	2.24	0.97	1.87
TRSTn	SYSCLKOUT	1.62	2.96	1.24	2.46
TRSTn	XLOGOFF	1.34	2.40	1.56	2.85

NOTES: 1. Timing values are in nanoseconds.
5. MIN condition is V_{DD} = 1.95 V, t_j = –40°C, strong process.
6. NOM condition is V_{DD} = 1.8 V, t_j = 25°C, nominal process.
7. MAX condition is V_{DD} = 1.65 V, t_j = 125°C, weak process.
10. The timing values were measured assuming a slew of 1.5 ns on the input port and a load of 64 SL (1SL = 0.00766 pF) on the output port.

timing requirements for reset signals (see Figure 10)

		CONDITION 1†	CONDITION 2‡	UNIT
t_{d1}	Delay time, SYSRSn relative to SYSCLKOUT	1.37/1.30	2.58/2.57	ns
t_{d2}	Delay time, IDLE relative to SYSCLKOUT	1.68/1.57	3.04/3.02	ns
t_{h1}	Hold time, VMAP to IMUCLKIN	–0.01	– 0.07	ns
t_{su}	Setup time, VMAP to IMUCLKIN	0.50	1.0	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

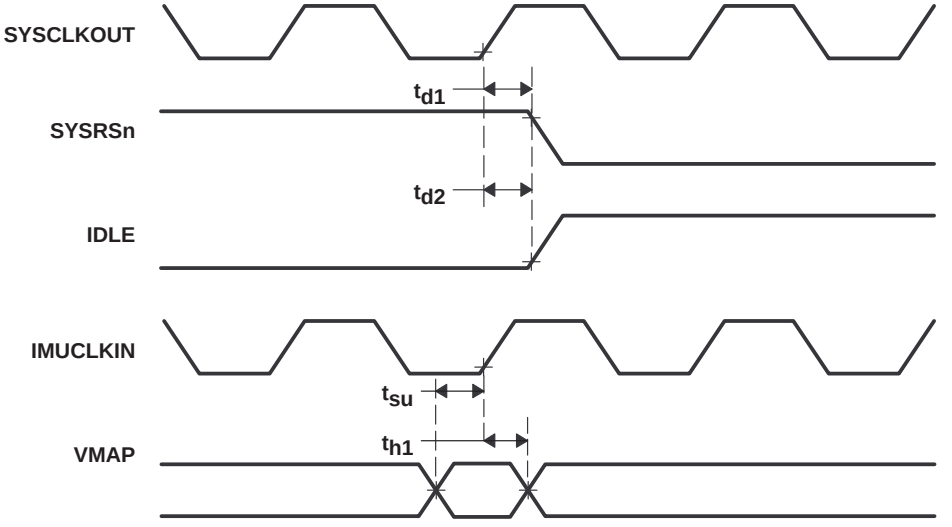


Figure 10. RESET Signal Waveform

timing requirements for reset and vector-fetch (see Figure 11)

		CONDITION 1†	CONDITION 2‡	UNIT
t_{d1}	Delay time, CPUCLKIN to SYSRSn	1.37/1.30	2.58/2.57	ns
t_{d2}	Delay time, CPUCLKIN to VECT	1.42/1.34	2.66/2.66	ns
t_{h1}	Hold time, RSn to CPUCLKIN	0.63	1.15	ns
t_{su1}	Setup time, RSn to CPUCLKIN	0.02	– 0.1	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

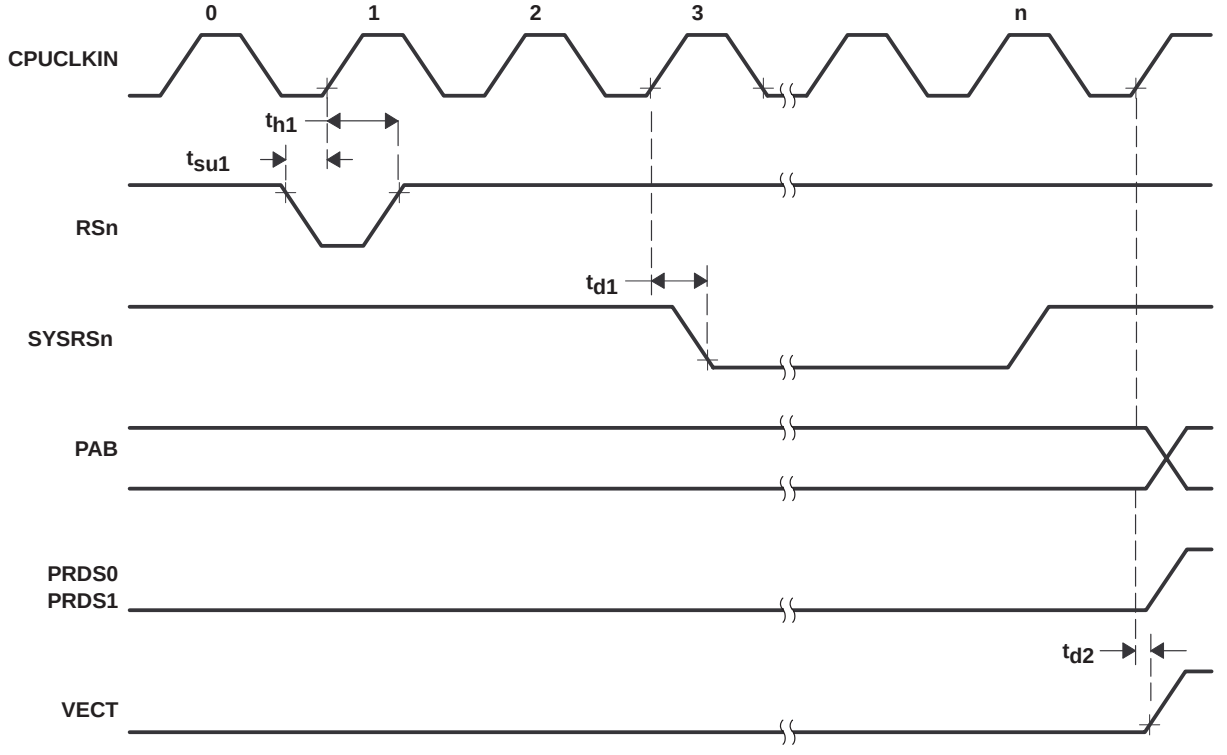


Figure 11. Reset and Vector-Fetch Waveform

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timing requirements for test mode signals (see Figure 12)

		CONDITION 1† Low to High/ High to Low	CONDITION 2‡ Low to High/ High to Low	UNIT
t_{d1}	Delay time, TCK to XLOGOFF	3.01/2.87	5.93/5.67	ns
t_{d2}	Delay time, TCK to COREFTEST	1.47/1.31	2.86/2.62	ns
t_{d3}	Delay time, TCK to MEMXFTEST	1.53/1.62	3.03/3.22	ns
t_{d4}	Delay time, TCK to COREATPG	2.53/2.43	5.13/4.90	ns
t_{d5}	Delay time, TCK to PERIATPG	2.24/2.22	4.68/4.57	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

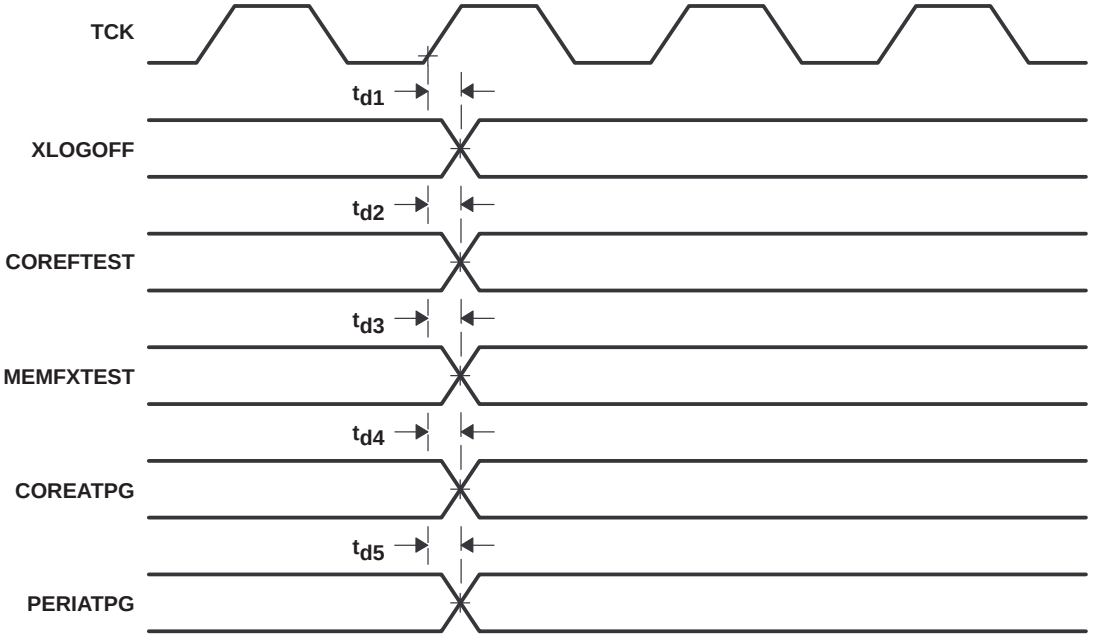


Figure 12. Test Mode Signal Waveform

timing requirements for test-access port signals (see Figure 13)

		CONDITION 1†	CONDITION 2‡	UNIT
t_{h1}	Hold time, TMS to the rising edge of TCK	0.20	0.58	ns
t_{h2}	Hold time, TDI to the rising edge of TCK	0.33	0.58	ns
t_{h3}	Hold time, ET0I/ET1I to the rising edge of TRSTn	– 0.15	– 0.20	ns
t_{su1}	Setup time, TMS to the rising edge of TCK	0.37	0.76	ns
t_{su2}	Setup time, TDI to the rising edge of TCK	0.28	0.45	ns
t_{su3}	Setup time, ET0I/ET1I to the rising edge of TRSTn	0.42	0.72	ns
		Low to High/ High to Low	Low to High/ High to Low	
t_{d1}	Delay time, falling edge of TCK to TDO	2.70/2.67	5.23/5.52	ns
t_{d2}	Delay time, falling edge of TCK to TDOZ	2.79/2.74	4.99/4.88	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

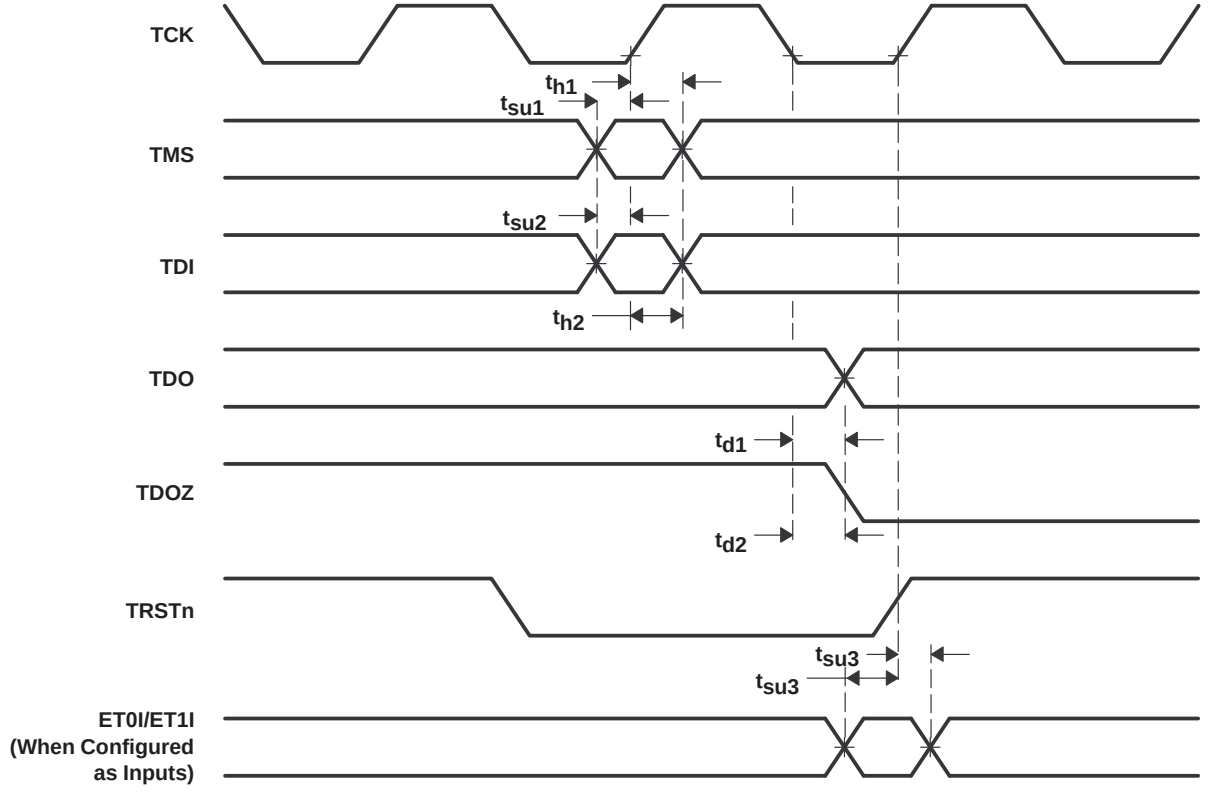


Figure 13. Test-Access Port Signal Timings

PRODUCT PREVIEW

timing requirements for interrupt (see Figure 14)

		CONDITION 1†	CONDITION 2‡	UNIT
t_{h1}	Hold time, NMIn to IMUCLKIN	0.09	0.05	ns
t_{su1}	Setup time, NMIn to IMUCLKIN	0.45	1.01	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

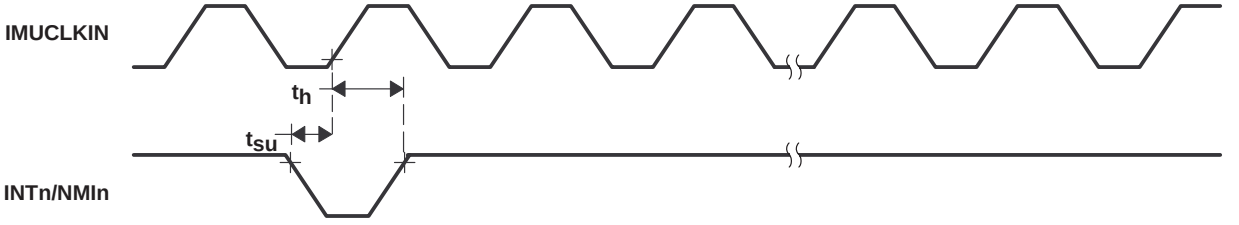


Figure 14. Interrupt and IACK Waveform

PRODUCT PREVIEW

timing requirements for data memory read cycle with no wait states (see Figure 15)

		CONDITION 1†	CONDITION 2‡	UNIT
t_{d1}	Delay time, CPUCLKIN to CPUSTAT	1.71/1.61	2.93/2.98	ns
t_{d2}	Delay time, CPUCLKIN to DRAB	1.75/1.58	3.51/3.23	ns
t_{d2}	Delay time, CPUCLKIN to DRDS0	1.75/1.60	3.18/3.08	ns
t_{d2}	Delay time, CPUCLKIN to DRDS1	1.75/1.61	3.16/3.08	ns
t_{h1}	Hold time, DRDB to CPUCLKIN	0.72	1.50	ns
t_{h2}	Hold time, DRDY to CPUCLKIN	0.64	1.17	ns
t_{h3}	Hold time, DROREADY to CPUCLKIN	0.44	0.74	ns
t_{su1}	Setup time, DRDB to CPUCLKIN	0.42	0.98	ns
t_{su2}	Setup time, DRDY to CPUCLKIN	1.51	3.14	ns
t_{su3}	Setup time, DROREADY to CPUCLKIN	1.31	2.50	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

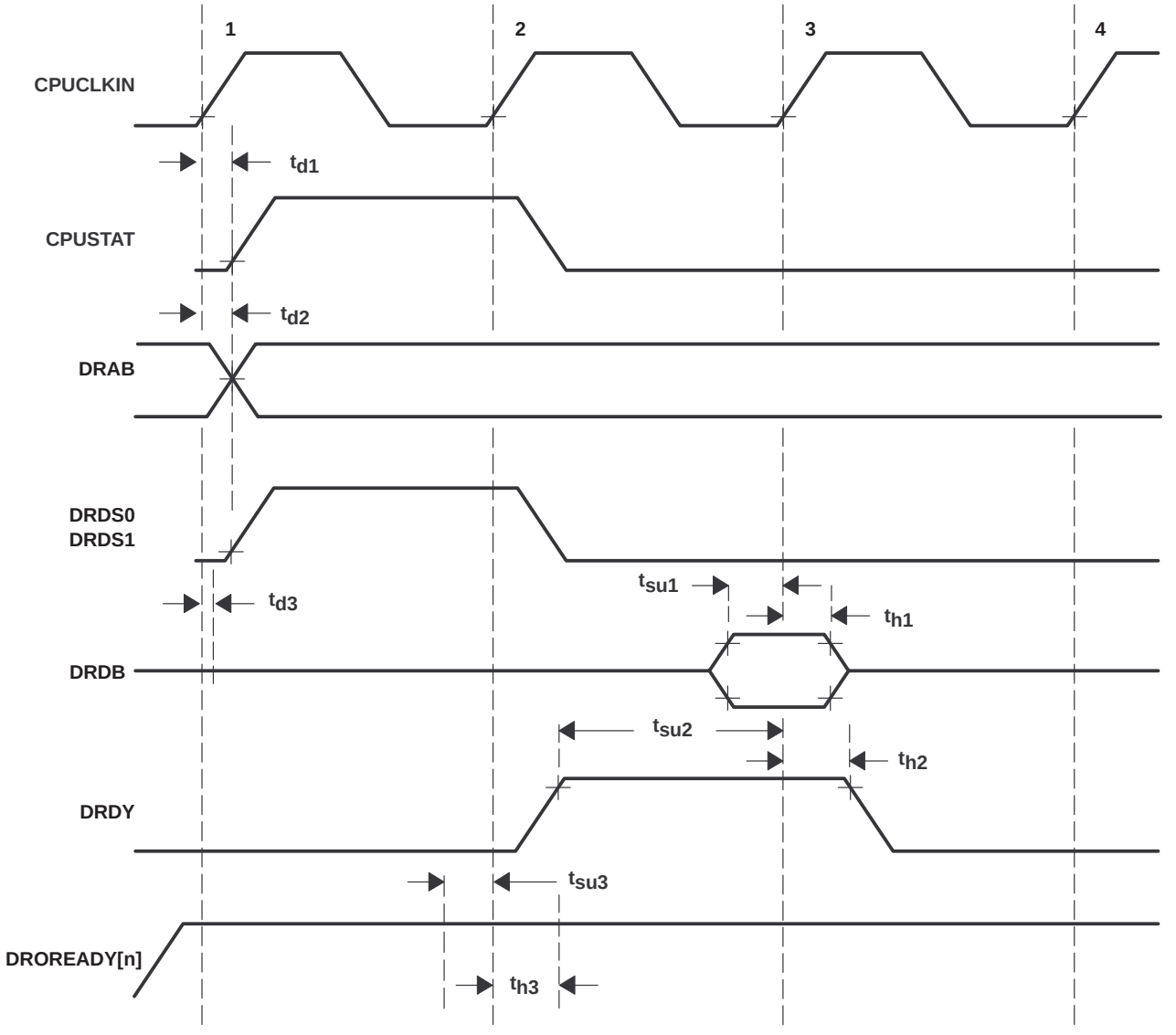


Figure 15. Data Memory Read Cycle (With No Wait States) Waveform

timing requirements for memory write cycle (with no wait states) (see Figure 16)

		CONDITION 1†	CONDITION 2‡	UNIT
t_{d4}	Delay time, CPUCLKIN to DWAB	1.48/1.39	2.99/2.86	ns
t_{d5}	Delay time, CPUCLKIN to DWDB	1.57/1.45	3.21/3.02	ns
t_{d6}	Delay time, CPUCLKIN to DWDS0	1.46/1.34	2.90/2.73	ns
t_{d6}	Delay time, CPUCLKIN to DWDS1	1.54/1.39	3.06/2.83	ns
t_{h8}	Hold time, DWOREADY to CPUCLKIN	0.46	0.78	ns
t_{su8}	Setup time, DWOREADY to CPUCLKIN	1.19	2.33	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

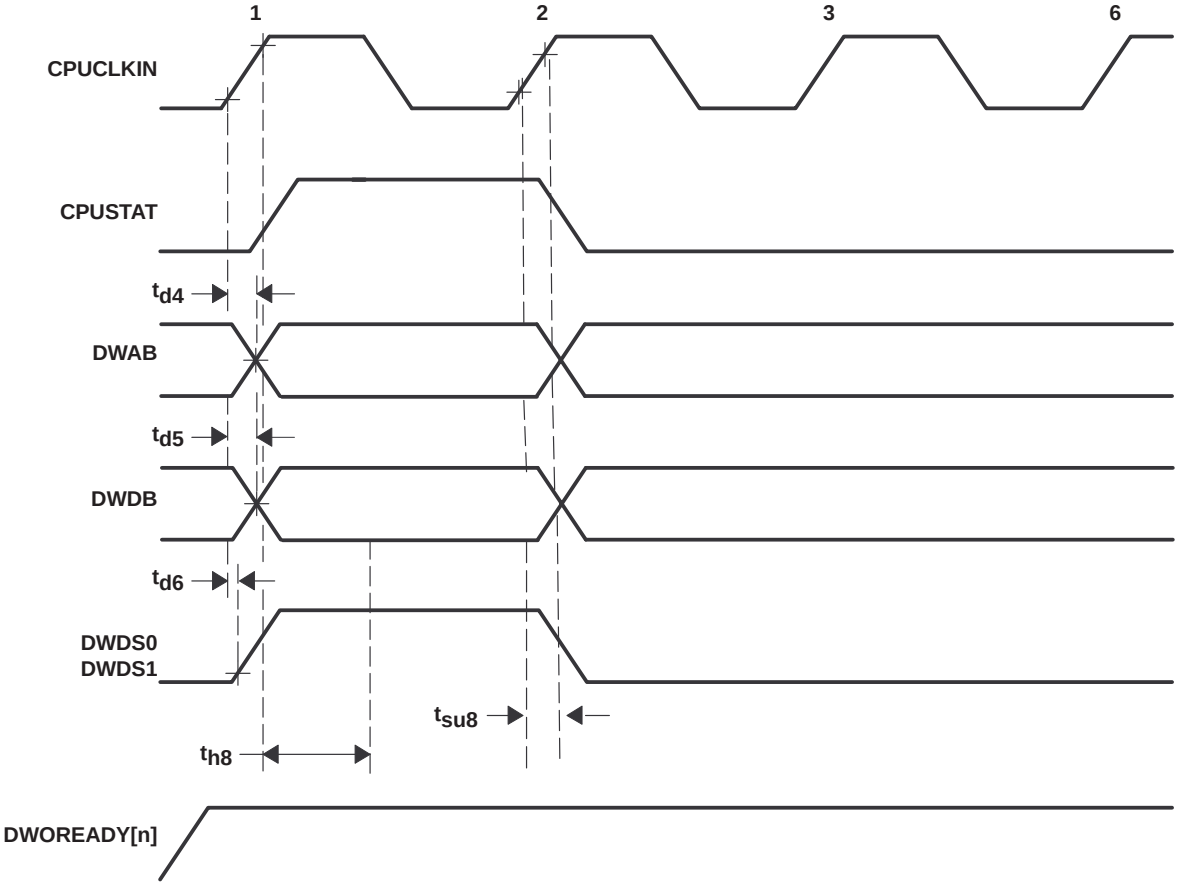


Figure 16. Memory Write Cycle Waveform

timing requirements for program read see Figure 17)

		CONDITION 1†	CONDITION 2‡	UNIT
t_{d7}	Delay time, CPUCLKIN to PAB	1.74/1.54	3.39/3.04	ns
t_{d8}	Delay time, CPUCLKIN to PRDS0	1.61/1.45	3.15/2.91	ns
t_{d8}	Delay time, CPUCLKIN to PRDS1	1.47/1.34	2.94/2.75	ns
t_{d9}	Delay time, CPUCLKIN to IFSTAT	1.62/1.50	3.00/2.93	ns
t_{h4}	Hold time, POREADY to CPUCLKIN	0.30	0.47	ns
t_{h6}	Hold time, PRDY to CPUCLKIN	0.63	1.16	ns
t_{h7}	Hold time, PRDB to CPUCLKIN	0.67	1.24	ns
t_{su4}	Setup time, POREADY to CPUCLKIN	1.44	2.96	ns
t_{su6}	Setup time, PRDY to CPUCLKIN	1.65	3.35	ns
t_{su7}	Setup time, PRDB to CPUCLKIN	1.40	2.85	ns

† Condition 1 is V_{DD} = 1.95 V, t_j = – 40°C, strong process.
‡ Condition 2 is V_{DD} = 1.65 V, t_j = 125°C, weak process.

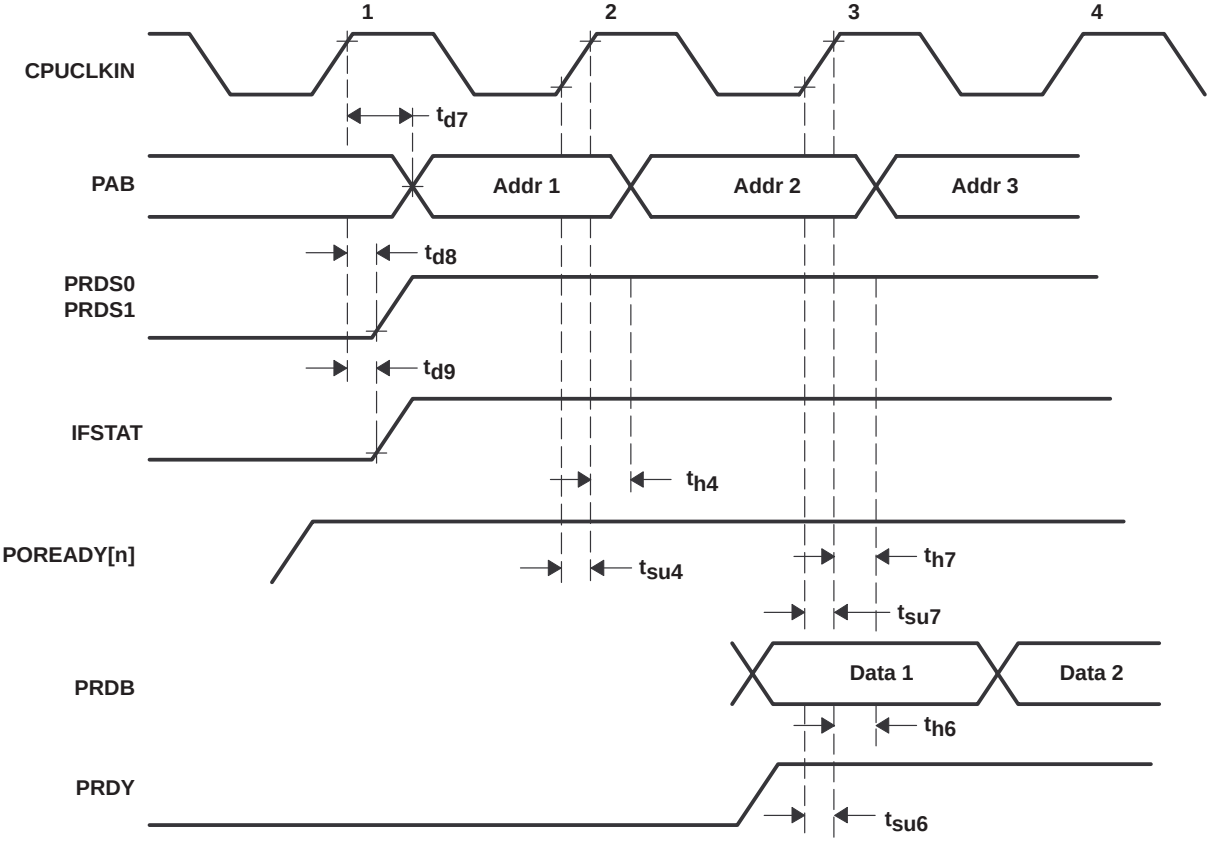


Figure 17. Program Space Read Access With No Wait States

PARAMETER MEASUREMENT INFORMATION

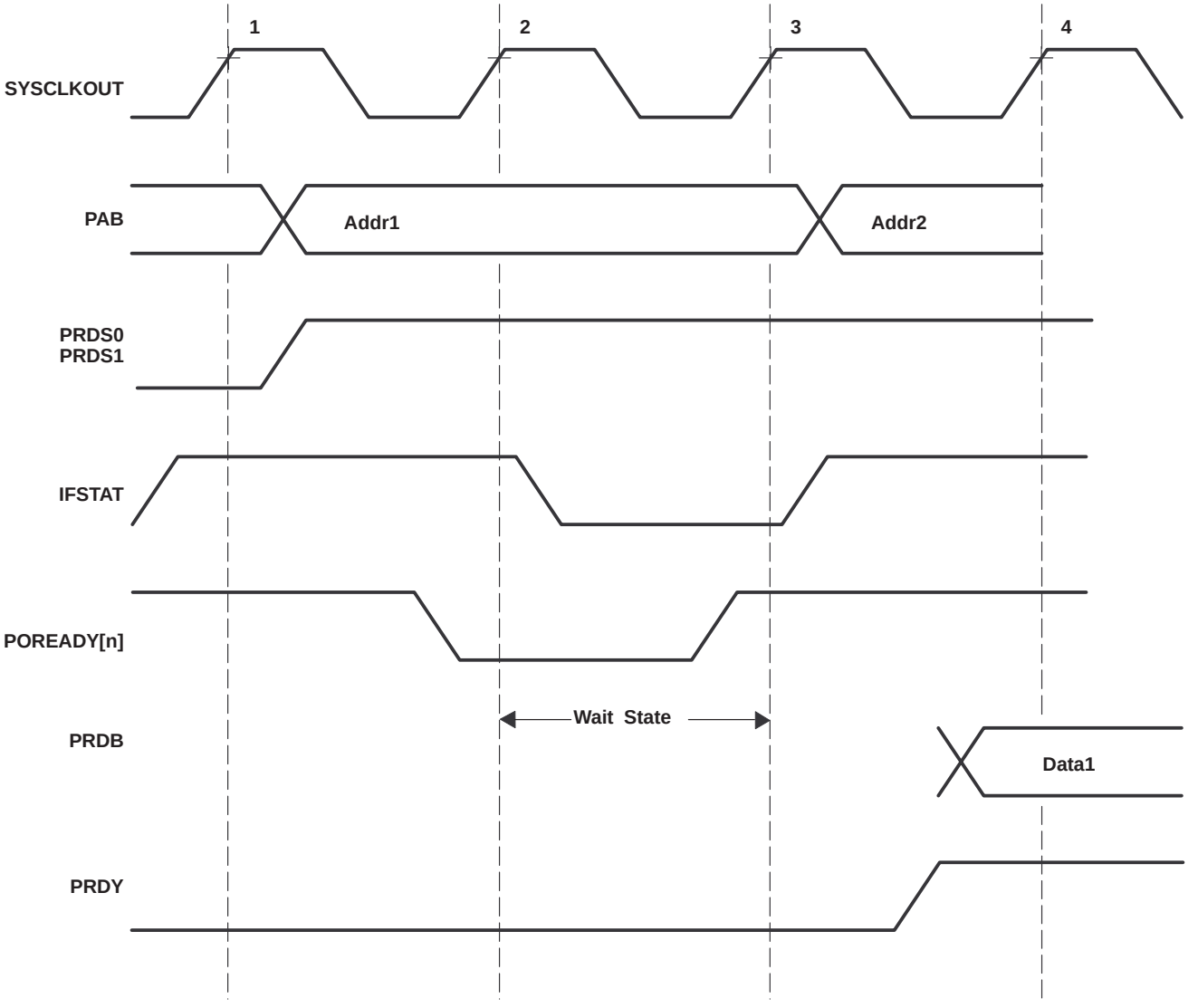
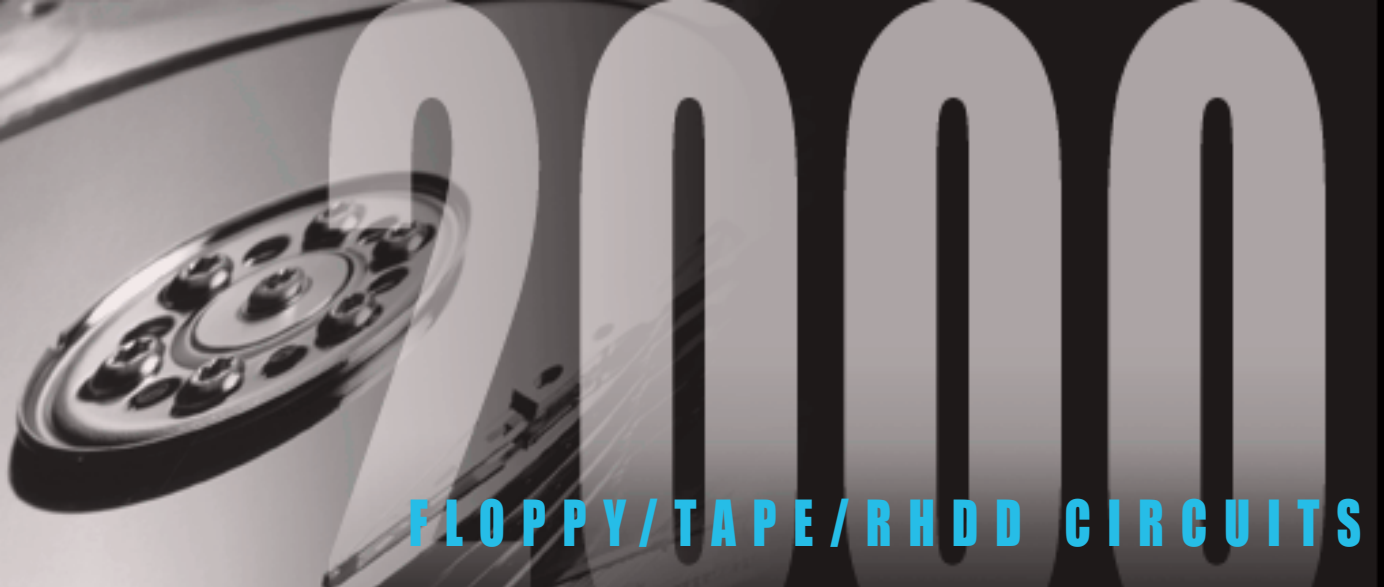


Figure 18. Program Space Read Access With One Wait State



2000

FLOPPY/TAPE/RHDD CIRCUITS

*Data sheet available upon request

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Abridged Version

SSI 34H3306
Servo Combo Driver

Preproduction

March 1999

DESCRIPTION

The SSI 34H3306 provides the capability to drive a voice-coil motor (VCM) and spindle motor of a disk drive system. The spindle section is a complete speed control servo system including power and pre-drivers requiring only a few additional discrete components for full functionality. The VCM section is a complete feedback controlled transconductance amplifier with power and pre-drivers. Only a few external compensation components is necessary to reshape the VCM closed-loop response. Serial interface is provided to program the internal registers for all user-selectable functions. Other supporting functions are also provided to facilitate the control of VCM during tracking. A functional block diagram of the SSI 34H3306 chip is shown on the next page.

FEATURES

GENERAL

- **3.3 V operation**
- **Serial port interface (16 Mbit/s data transfer rate)**

VOICE COIL MOTOR (VCM) DRIVER

- **High efficiency drivers, 1.5 Ω Rds(on) total (worst case)**
- **0.3 A capability**
- **Sense resistor current control**
- **4-bit programmable gain for CPES signal**
- **3-bit programmable gain for sense amplifier**
- **2-mode window comparator with 4-bit programmable threshold**

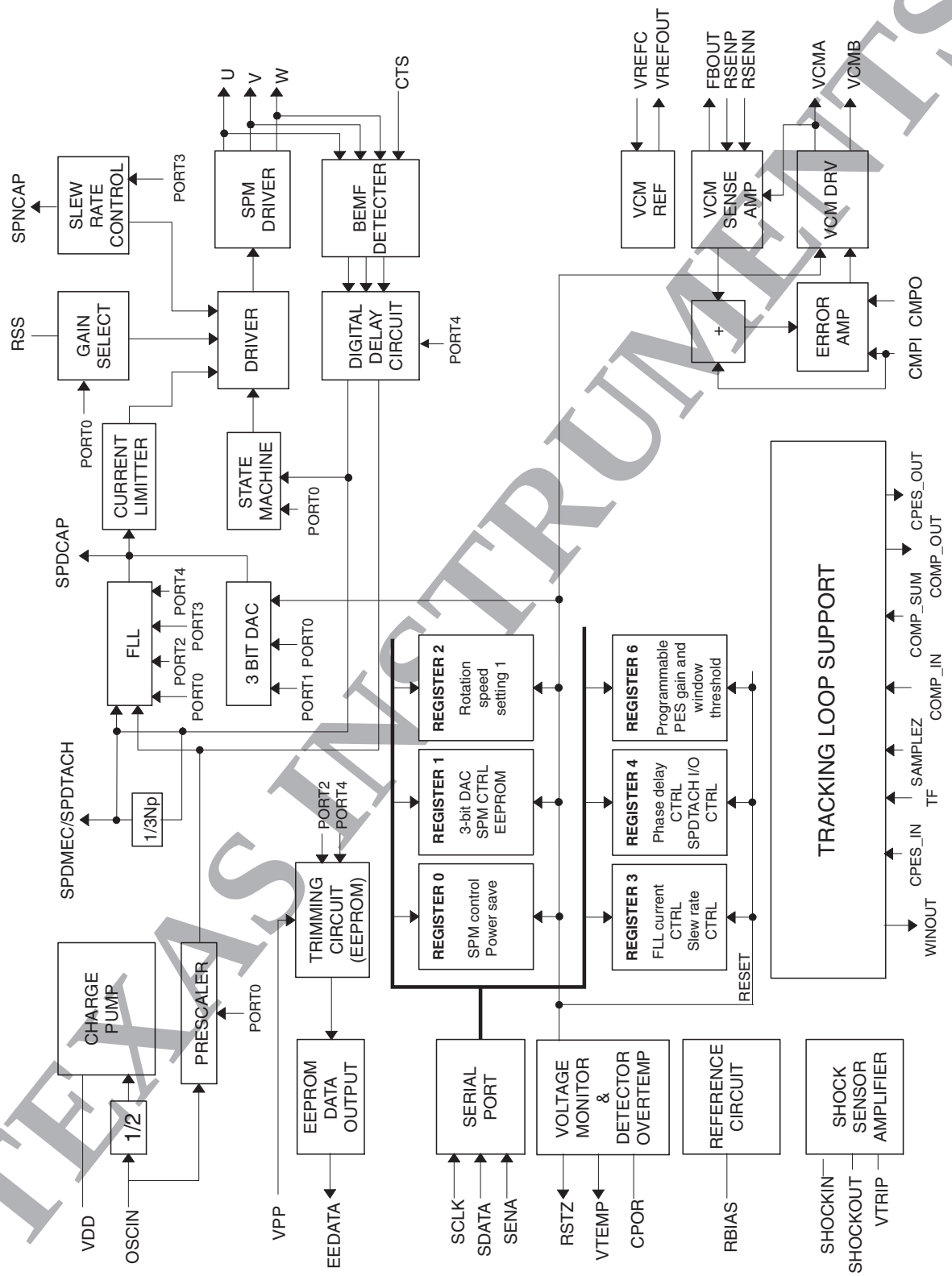
SPINDLE MOTOR DRIVER

- **High efficiency drivers, 1.5 Ω Rds(on) total (worst case)**
- **0.8 A capability**
- **Digital commutation delay and blanking**
- **Bipolar drive**
- **3-bit DAC for start up current**
- **Driver slew rate control by setting an external capacitor**
- **FLL rotation speed control**

VOLTAGE MONITOR/VOLTAGE REFERENCE

- **Supply voltage fault/reset detector provides ±3% tolerance**
- **One channel shock sensor amplifier**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

SERIAL PORT

The serial port facilitates programming of the SSI 34H3306's six internal registers, via sixteen bit data packets. Each data packet contains register address and control information. The maximum serial clock frequency is 16 MHz.

SERIAL PORT TIMING

The serial port uses three control lines: SCLK (serial port clock), SDATA (serial port data), and SENA (serial port enable, active HIGH). SDATA is the serial data signal and must be synchronous with the rising edge of SCLK. When SENA is LOW the input bit counter is reset. When SENA is HIGH the next rising edge of SCLK begins loading SDATA into the 16-bit input data register. After the sixteenth clock the Input Register is transferred to the Selected Port Register. SENA must return LOW between each 16-bit data transfer to ensure proper synchronization. The serial port timing and bit numbering are shown in Figure 1. The Serial Port sub-section of the Electrical Specifications section contains all serial port timing specifications.

REGISTER AND DATA-BIT DEFINITIONS

The SSI 34H3306 serial port contains internal registers that are programmed via the SCLK, SDATA, and SENA signals. Data bits 15-13 are used as an address indicator to determine which register is selected. See Table 3.

The Register Description section defines the contents of each register. Table 9 summarizes the Internal Register contents.

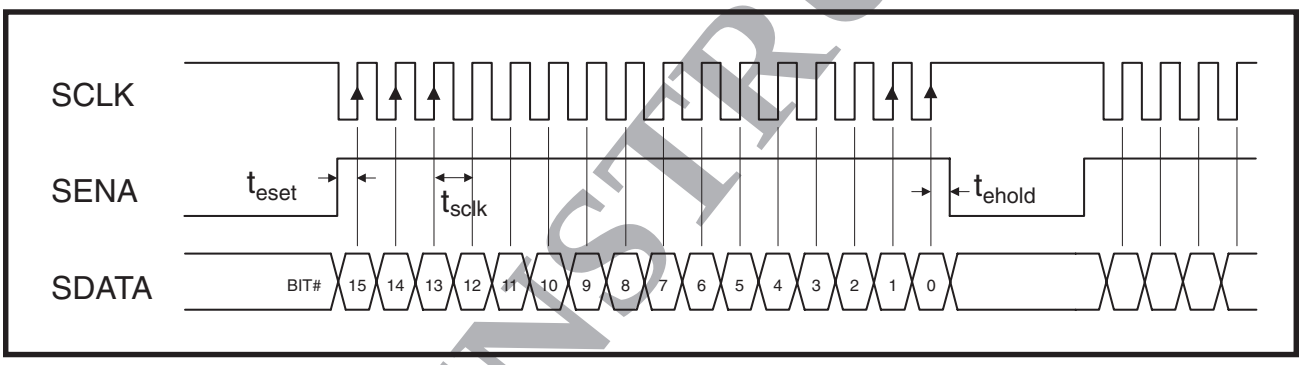


FIGURE 1: Serial-Port Data Transfer

FUNCTIONAL DESCRIPTION (continued)

VOLTAGE MONITOR/OVER-TEMPERATURE DETECTOR

The voltage monitor circuit, shown in Figure 2, has 2 external outputs (RSTZ and VTEMP). This circuit monitors the AVCC power source and generates an external reset signal (RSTZ) any time the voltage is less than Vpor. The IRSTZ signal is the same as the RSTZ signal or'd with the over temperature condition and is used internally to reset the chip. The CPOR output is for an external capacitor that determines the desired RSTZ delay. No other component should be connected to this terminal. The signal from the over-temperature detector is also brought out through pin VTEMP so that user can monitor the die temperature.

DETAILED CIRCUIT DESCRIPTION

As the power supply (AVcc) ramps up and reaches Vop, RSTZ becomes active low. When it reaches Vpor + Vh, CMP1 output switches to low and the external capacitor connected to CPOR starts to charge up at a rate determined by the current generator and the CPOR capacitor. When CPOR reaches the reference voltage, CMP2 switches and RSTZ goes inactive high. If AVcc then drops below Vpor, the capacitor discharges rapidly and RSTZ goes low. If AVcc starts to ramp up after falling below Vpor, CPOR stays low (0 V) until AVcc again goes above Vpor + Vh at which point CPOR starts to charge up and after the delay, enables RSTZ to go high. See Figure 16 in the Electrical Specifications section.

TABLE 1: Power Fail and Over-temperature Consequence

	INTERNAL RESET	EXTERNAL RESET	RESET SERIAL PORT	VCM	SPM	WINDOW COMPARATOR OUTPUT
Power Fail	Yes	Yes	Yes	Retract	Disable	
Over-temp	Yes	No	Yes	Brake	Brake	H

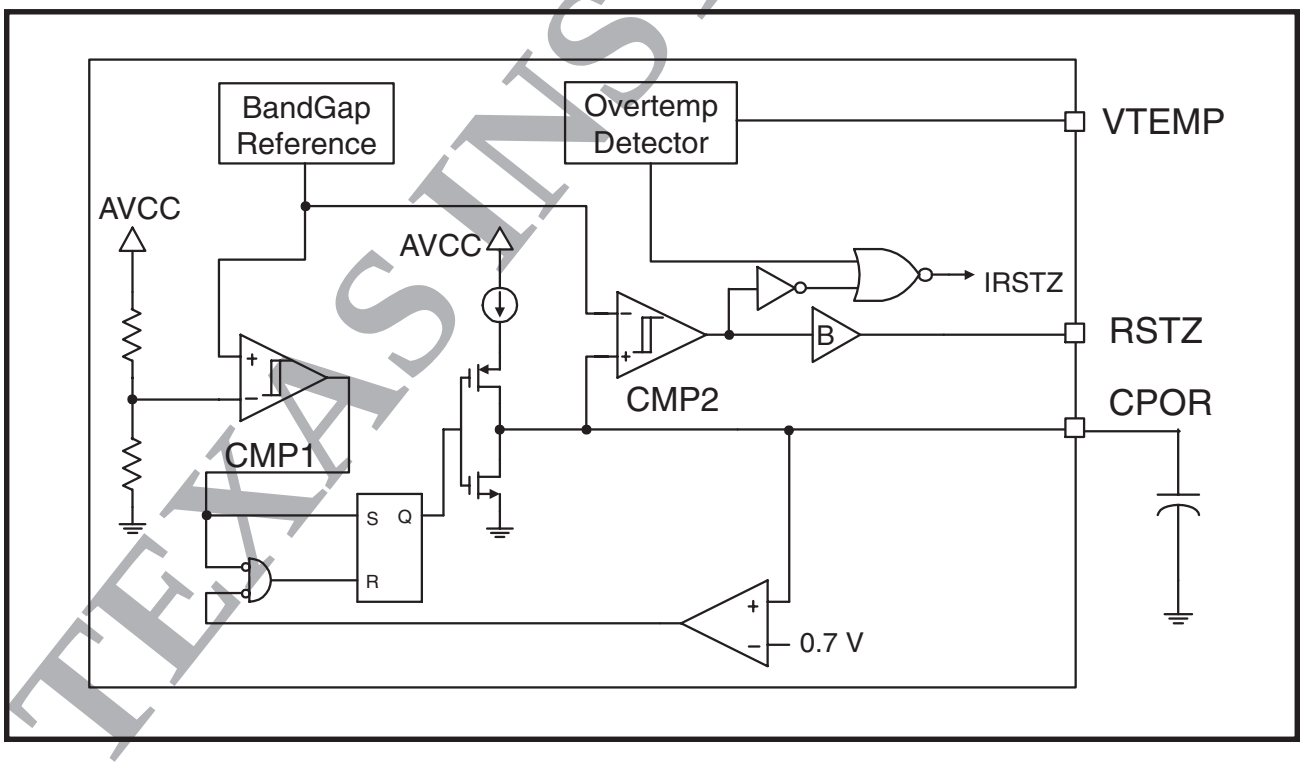


FIGURE 2: Voltage Monitor Circuit

CHARGE PUMP

The function of the charge pump circuit is to generate an 8.25 V power source (VDD) from the AVCC power source. A higher voltage is required for the SPM and VCM high side MOSFET gate control. The VDD pin is to allow for the connection of an external filtering/storage capacitor.

DETAILED CIRCUIT DESCRIPTION

As soon as the chip is powered up, the charge pump becomes activated. The charge pump uses three internal capacitors and digital control logic to pass the charge on to the VDD pin to charge up an external capacitor. A fraction of the voltage on the VDD pin is compared with VREFCP (which is equal to (14/33) • AVCC) to enable or disable charging the external capacitor so that the output voltage on the charge pump is regulated to 8.4 V (@ AVCC = 3.3 V). Since AVCC is used as the reference, the charge pump voltage is directly proportional to AVCC. The relation between VDD and AVCC is as follows:

$$VDD = 6 \bullet (14/33) \bullet AVCC \qquad \text{(Equation 1)}$$

SHOCK SENSOR AMPLIFIER

The purpose of the shock sensor section is to detect a signal generated by an external sensor and produce a digital output when the input signal meets a predetermined level. This section consists of an amplifier and a comparator. The input and output pins of the shock sensor amplifier are brought out so that a compensation network can be connected externally to shape the input signal. The amplifier output connects to a window comparator circuit which produces a HIGH if the signal exceeds a certain level. This HIGH signal can be used to drive other external circuits.

VCM DRIVE

The Voice Coil Motor (VCM) drive system is a complete feedback controlled current amplifier for operating a VCM mechanism in a disk drive unit. It consists of a full bridge power drive and a pre-driver. The power driver is an amplifier using an external sense resistor for current feedback. The feedback gain (8 levels) can be adjusted by a programmable sense amplifier through the serial port. The pre-driver provides for external bandwidth limiting via discrete components for tailoring to particular mechanisms.

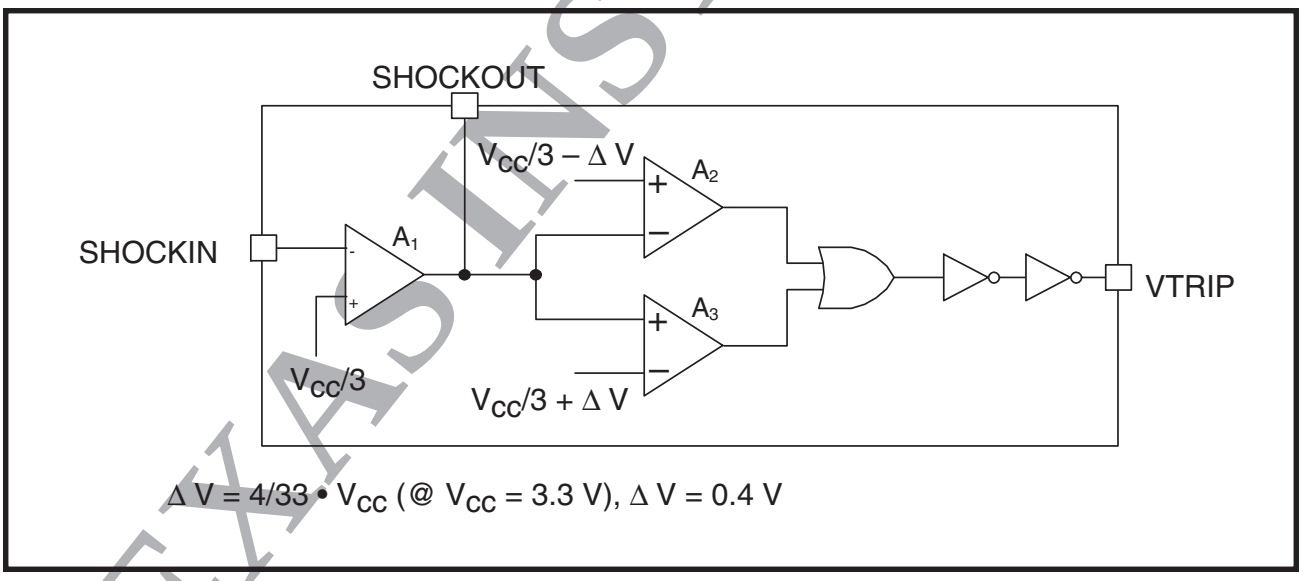


FIGURE 3: Shock Sensor Amplifier

FUNCTIONAL DESCRIPTION (continued)

VCM DETAILED DESCRIPTION

The voice-coil full-bridge power amplifier is capable of ±0.3 A output current and has a maximum $r_{DS(on)}$ resistance of 1.5 Ω. The voice coil control system uses an external sense resistor in series with the motor to detect load current. The six amplifiers, A_1 to A_6, together with the sense resistor and the external resistors, R_i and R_f, make up a current feedback control loop. The result is a transconductance gain from the input resistor to the VCM load current that is:

$$G_{vcm} = I_m / V_{in} = R_f / (2\ G_{SENGN}\ R_i\ Rs)$$

for the values shown in Figure 4

(Equation 2)

This transconductance gain is programmable from 1.65 to 4.0 through the serial interface (SENGN, R6, B4-6). A programmable attenuator controlled by SENGN appears after the compensation amplifier, so as to maintain a fixed loop gain for stability reasons. The VCM loop includes provision for an external compensation network for shaping the frequency response of the transconductance amplifier. The compensation network is usually a simple R-C circuit. The output voltage of the power amplifier is limited to 3.9 V by active clamp circuitry (not shown).

One bit, ENVCM, in the Internal Register is provided to disable VCM loop while still keeping the tracking loop enabled. The control logic is shown in a simplified block diagram in Figure 5.

TRACKING LOOP SUPPORT

The tracking loop circuits are comprised of 1) a zero order sample and hold, 2) an inverting opamp stage to support an external compensation filter with switches that can be used to enable/disable the compensation filter, 3) a position error amplifier with 16-level programmable gains in equal steps, and 4) a 16-level threshold window comparator operating in two modes: sign mode and window mode.

The tracking loop support provides several functions to facilitate the VCM control during tracking. Figure 6 gives a simplified block diagram of these functions. The input position error signal (CPES_IN) is sampled by a zero-order sample and hold. The sampled signal is then amplified by opamp A_1 with a programmable gain. The gain is controlled by a switching network and a resistor chain. Finally, the position error signal or the compensated signal (COMP_OUT) is passed through the window comparator. The window comparator operates in two modes: sign mode and window mode. The window threshold is programmable with 15 levels in linear scale. The operating modes and the thresholds are controlled by 4 bits in an internal register. All bits being zeros indicates that the window comparator is in the sign mode. Other bit combinations (e.g., 1010) are used for setting the ± window thresholds. The window comparator accepts two inputs, CPES_OUT and COMP_OUT, multiplexed by another bit in the Internal Register. The window thresholds are symmetrical to the window center point VREF (VCC/3) and independent of the power supply voltage since they are derived from the bandgap reference voltage. The transfer curves of the window comparator in sign mode and threshold mode are shown in Figures 7 and 8.

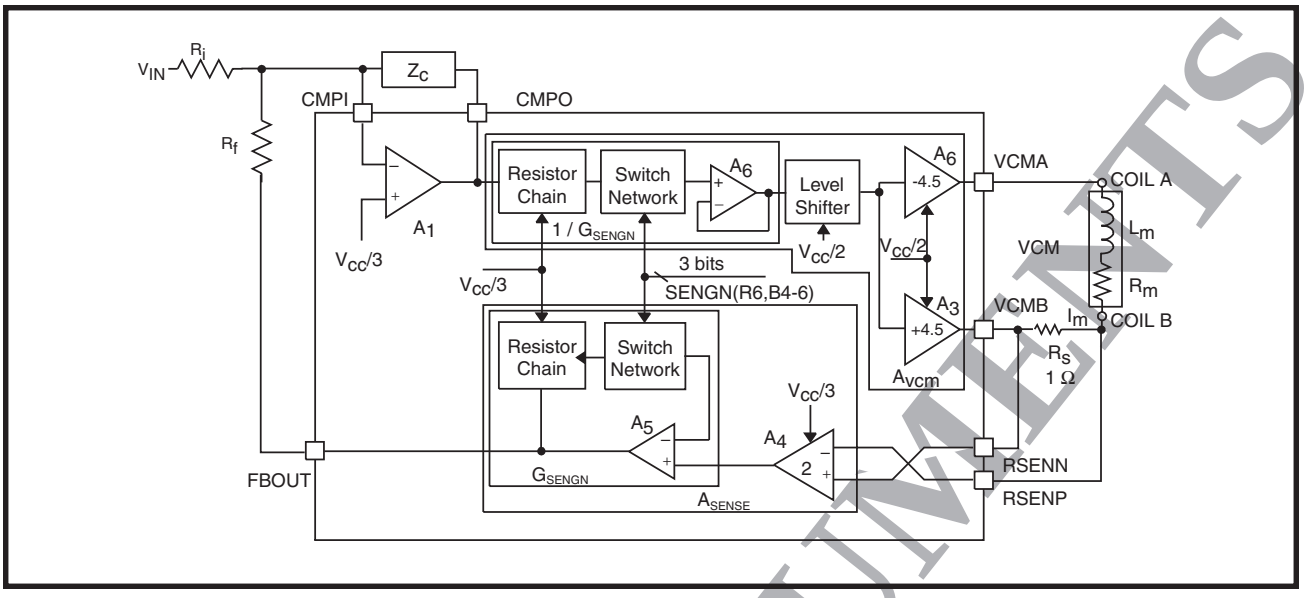


FIGURE 4: VCM Control Circuit

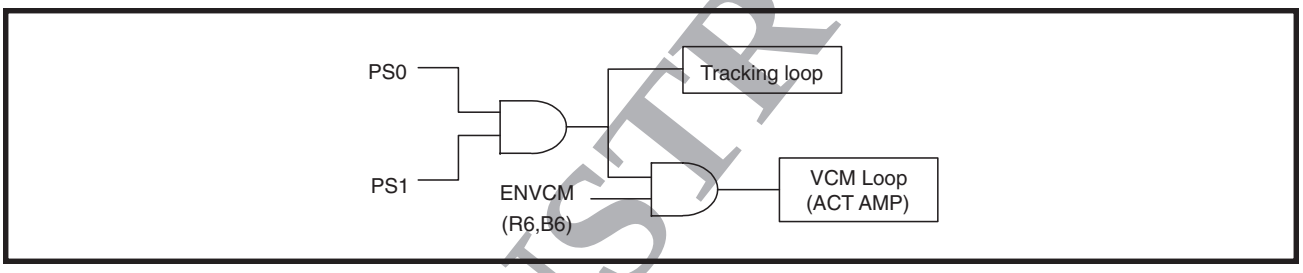


FIGURE 5: Tracking Loop Control Logic

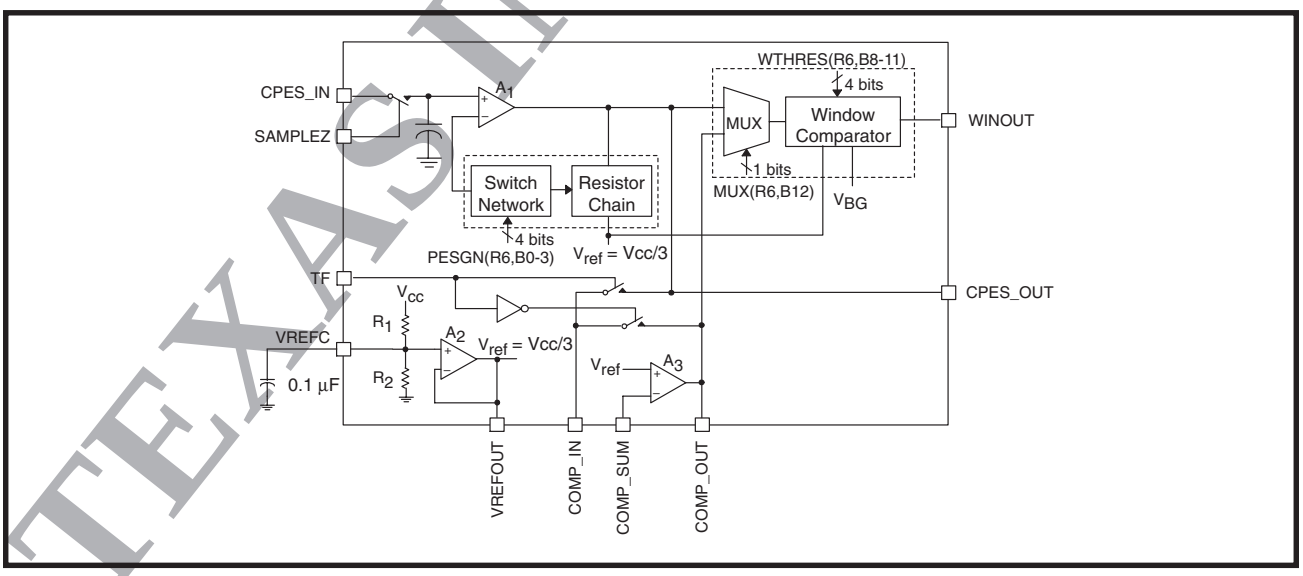


FIGURE 6: Tracking Loop Support

FUNCTIONAL DESCRIPTION (continued)

VCM DRIVER PROTECTION CIRCUITRY

Since the output of the VCM driver is an inductive load, it is necessary to provide active clamp circuitry that limits the signal swing on the output terminals of the VCM driver. There are two sets of clamps—a low-swing and a high-swing clamp—for each of the two outputs. The low swing clamps restrict VCMA and VCMB from swinging below a half of a diode drop below AGND. This protects the junctions tied to the low-side drivers from becoming forward biased. The high-swing clamps restrict VCMA and VCMB from swinging above 3.9 V. This keeps the common-mode input range of RSENP and RSENN within the operating range of amplifier A_4. This also protects the driver devices from being damaged.

Also provided in the VCM driver is active shoot-through protection that prevents both the low-side and high-side drivers of the same output from turning on at the same time. Since the on-resistance of the drivers are so low, this protects the driver devices and eliminates high shoot-through currents that can occur during fast transitions.

This driver protects the heads and media by automatically retracting the heads by turning on the high-side driver of VCMB and the low-side driver of VCMA, whenever the voltage monitor detects a power fault condition. In the event a over temperature condition occurs the VCM driver turns on both low-side drivers so as to brake the VCM's movement.

SPINDLE MOTOR DRIVE

The Spindle Motor (SPM) drive system controls the spindle/disk assembly in a disk drive. The complete servo system includes three identical power drivers and a pre-drive system. Each power driver is a transconductance amplifier with user selectable gain and slew rate. The pre-drive provides for frequency lock servo control. A state machine controls the motor commutation sequence by means of the EXCOMM bit in a serial port register or by the motor's back EMF (BEMF) zero crossings.

SPINDLE MOTOR CONTROL SYSTEM

The spindle motor system is a complete frequency lock loop (FLL) speed feedback control system for controlling the speed of a three-phase brushless motor. It consists of two main sections: (1) speed control circuits and (2) phase winding commutation and current slewing circuits. The digital feedback signal, derived either internally from the BEMF zero crossings of the motor or externally from the data written on the disk, is compared with a digital reference signal. The error signal produced is then amplified and applied to the motor. The motor thus accelerates or decelerates until the two frequencies are the same. The power section of the spindle motor system converts the voltage at the SPDCAP to a proportional peak current level in the three spindle motor windings . It also performs the commutation and current slewing that allows the motor to be treated in the system as a simple DC motor. Control of the transconductance gain and slewing rate is programmed through the serial port.

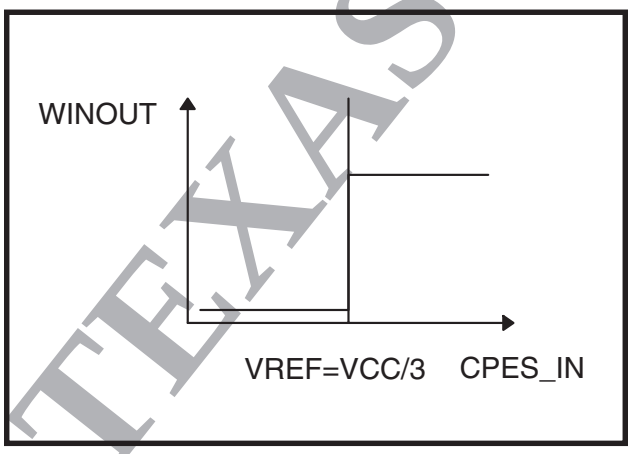


FIGURE 7: Transfer Curve For Sign Mode

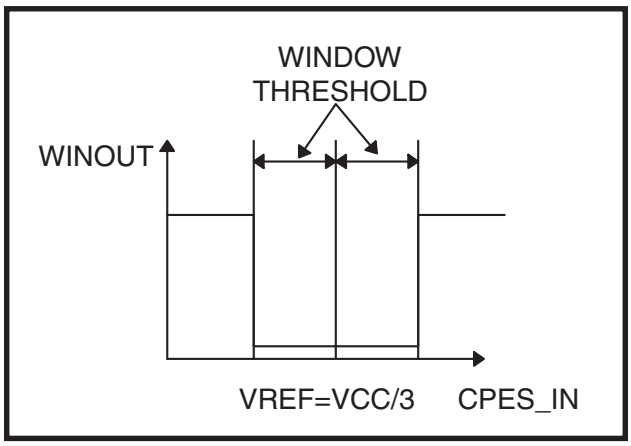


FIGURE 8: Transfer Curve for Threshold Mode

BEMF DETECT CIRCUIT

The BEMF detect circuit measures the voltage on the unexcited motor phase, and compares it to the center-tap (CTS) voltage. The BEMF detect circuit (Figure 9) consists of a comparator, and three transmission gates.

The state machine knows which phase is the unexcited phase and will assert one of the ZCU, ZCV and ZCW signals to open one of the transmission gates so that the unexcited phase is connected to the positive input of the comparator. The negative input of the comparator is always connected to the center-tap. The output of the comparator (ZCRS) goes to the spindle state machine.

The 10 kΩ resistor divider connected to the CTS pin sets it to middle supply voltage to ensure proper BEMF detection during HIZ mode.

The ZCRS signal thus produced makes a transition for each zero crossing of the BEMF of each of the three motor windings. This is at every 60 electrical degrees of actual motor rotation or $6N_p/2$ transitions per revolution where N_p is the number of motor poles per revolution.

SPINDLE CONTROL LOGIC

The spindle control logic consists of a 12-bit commutation delay counter and a spindle motor (brushless DC) state machine (Figure 10). The commutation delay counter serves a dual purpose of 1) providing commutation delay, and 2) it filters out noise spikes that occur around the commutation point.

The ZCRS signal is either inverted or not inverted by the XOR circuit depending on the POS signal from the state machine. The POS signal is high when a positive going zero crossing of the BEMF is anticipated for starting the delay counter and low when a negative transition is expected.

A low LDZ signal input at the 12-bit counter causes it to be reloaded with the 12-bit PDT (phase delay time) value at each positive clock edge. When LDZ is high the counter will count until end of count is reached, at which point the EOC signal goes high for one clock cycle. The ZCU, ZCV, and ZCW signals go to the BEMF detect circuit where they will open one of the transmission gates to select the undriven phase prior to when it is expected.

The state machine follows the states indicated in Table 2, and can be advanced either manually, using the EXCOMM signal (if COMS = 0), or by BEMF zero-crossings, using the COMM (if COMS = 1) signal. Other control options for the state machine are also shown in the table. The state machine is reset and outputs are disabled if either PS1 = 0 or SPNENA = 0.

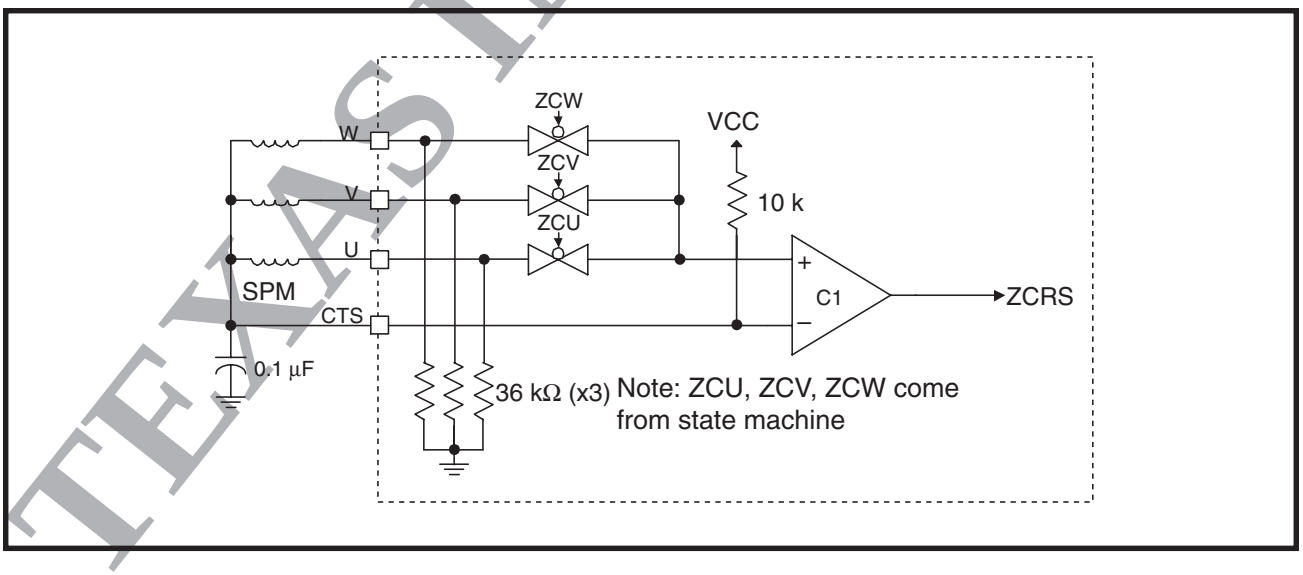


FIGURE 9: BEMF Detect Circuit

SPINDLE CONTROL LOGIC (continued)

Assuming a positive transition is expected, and POS is high, the ZCRS signal is then passed unchanged to the LDZ input on the 12-bit counter. As long as the ZCRS signal is low the counter is continually reloaded (with PDT value). At the BEMF zero crossing, the ZCRS goes high and the counter starts counting. Any noise spike on the ZCRS signal shorter than PDT clock times will be ignored since the counter will be reloaded after the noise spike goes away prior to the EOC pulse.

When a negative BEMF is expected, the POS signal is low and the ZCRS signal is inverted before reaching the LDZ input. In this case the counter will be reloaded when ZCRS is high and allowed to count when it is low.

After PDT clock pulses the counter generates the EOC pulse which advances the state machine causing the outputs to change to the next state. See the section, Programming the SSI 34H3306 for how to select the PDT value.

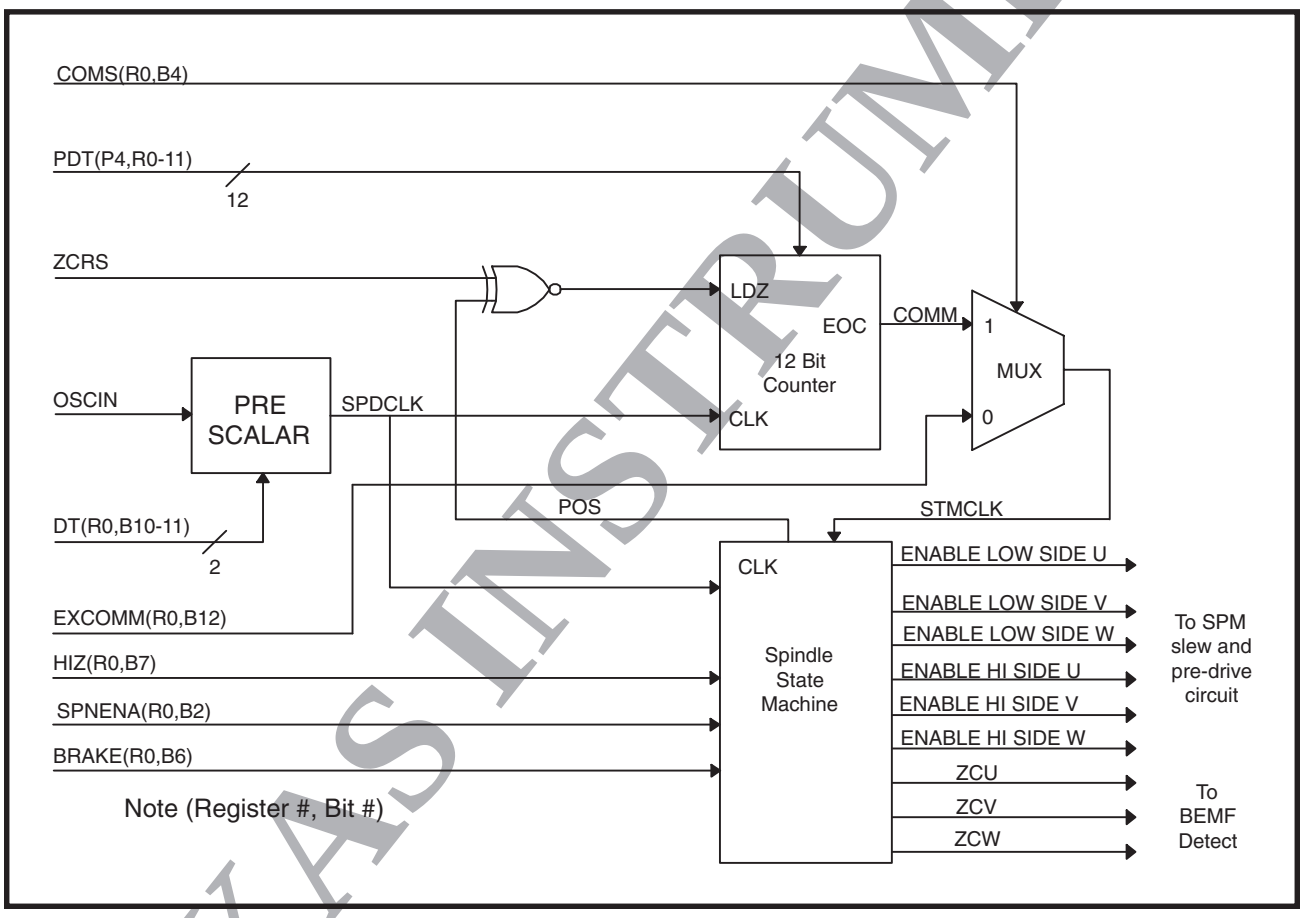


FIGURE 10: Spindle State Machine and Phase Delay Circuit

SPM SERIAL PORT REGISTER CONTROL BITS (SEE SERIAL PORT SECTION)

Register 0

PS1 = 1 and SPNENA = 1: Enables the spindle drivers and enables the state machine

PS1 = 0 or SPNENA = 0: Disables the spindle drivers and resets the state machine

COMS = 0: Selects manual/forced commutation using EXCOMM

COMS = 1: Selects hardware (automatic) state machine advance using the BEMF

EXCOMM: Manually advances the state machine on positive going edge if COMS = 0, PS1 = 1, SPNENA = 1

BRAKE = 1: Quickly brakes the motor by enabling all three low-side drivers and disabling all high-side drivers if PS1 and SPNENA are high

HIZ = 1: Disables spindle drivers without resetting state machine if PS1 = 1. U, V, and W pins go to a high impedance state which allows verification of rotation after manually commutating the motor. The state machine continues to advance and select the inactive phase for BEMF monitoring.

Register 4

PDT(0,11): 12-bit commutation delay count. Valid delay range 1 to 4095.

Manual (Software) Commutation Mode

In manual commutation mode the state machine is advanced by each positive transition of the EXCOMM bit in Serial Register 0.

To manual commutate the state machine:

1. Write COMS = 0
2. Write EXCOMM = 0
3. Write PS1 = 1, SPNENA = 1
4. Write EXCOMM = 1 (State machine advances)
5. Write EXCOMM = 0
6. Write EXCOMM = 1 (State machine advances)

Once the COMS bit is set high the state machine will advance automatically using the BEMF detect and delay circuit.

TABLE 2: State machine outputs

DESCRIPTION	STATE #	CURRENT DIRECTION	HIGHSIDE U	LOWSIDE U	HIGHSIDE V	LOWSIDE V	HIGHSIDE W	LOWSIDE W	POS
Basic	1	U-V	ON	OFF	OFF	ON	OFF	OFF	0
Commutation	2	U-W	ON	OFF	OFF	OFF	OFF	ON	1
PS1 = 1	3	V-W	OFF	OFF	ON	OFF	OFF	ON	0
SPNENA = 1	4	V-U	OFF	ON	ON	OFF	OFF	OFF	1
	5	W-U	OFF	ON	OFF	OFF	ON	OFF	0
	6	W-V	OFF	OFF	OFF	ON	ON	OFF	1
Power save	0	NA	OFF	OFF	OFF	OFF	OFF	OFF	0
PS1 = 0 or SPNENA = 0 State machine reset.									
PS1 = 1, SPNENA = 1	0	NA	OFF	OFF	OFF	OFF	OFF	OFF	0
Start mode, on first positive COMM/EXCOMM edge state machine goes to state #1.									
HIZ = 1	1-6	NA	OFF	OFF	OFF	OFF	OFF	OFF	NOTE
BRAKE = 1	1-6	NA	OFF	ON	OFF	ON	OFF	ON	NOTE

NOTE: POS level corresponds to state

FUNCTIONAL DESCRIPTION (continued)

PROGRAMMING THE SSI 34H3306 SPM CONTROL

This section gives a step by step description of how to program the SPM-control section of the SSI 34H3306 (see speed-control covered in the FLL SPM Speed Control Circuit section)

1. First power-up the charge pump and SPM control circuitry by entering power save mode 3. Program PS(1) = 0.
2. Initialize Phase Delay Time Register. The phase delay time is usually set to the equivalent of 30 electrical degrees. The delay time needed for 30 °e is:

   $$T_{delay}\ (s) = (60/RPM) \bullet (2 / N_p) \bullet (30°/360°) = 10/(RPM \bullet N_p)$$

   (Equation 3)

   where N_p = number of motor poles.

   The T_{delay} value can be converted to the number that needs to be programmed into the PDT (phase delay time) register using the following equation:

   $$PDT_{value} = T_{delay}\ (s) / (PRESCALE / f_{OSCIN})$$

   (Equation 4)

   where f_{OSCIN} is in Hz, and PRESCALE is DT value in Register 0.

   Program the PDT_{value} into the PDT bits of Register 4.

NOTE: Slow-slewing delays the commutation point which requires advancing (shortening) the commutation delay by 1/2 the slew time in order to center the commutation on the BEMF.

3. Disconnect the 3-bit DAC from the VCM and connect it to the SPM SPDCAP voltage limit circuit by setting DACS = 0.
4. Select manual current control (no speed control) by setting CCS = 0. This disconnects the SPDCAP pin from the SPM control amplifier and, instead, connects the 3 bit DAC to control the motor current.
5. Wait until charge pump has reached 8.25 V (@ V_{cc} = 3.3 V). (Depends on size of capacitor on Vdd pin, and on f_{OSCIN}).
6. The motor is now ready to start.
7. Select desired current range by setting SPMG high or low.
8. Program desired start current by programming the desired current level into SPMDAC(0-2).
9. Select manual/forced commutation by setting COMS = 0. Also set EXCOMM = 0 at this point.
10. Enable SPM-state machine by setting SPNENA = 1. The output drivers are still in a HIZ at this point.
11. Force the state machine to go to state #1 by setting EXCOMM = 1.
12. Prepare for next forced commutation by setting EXCOMM = 0.
13. Wait desired time according to starting algorithm, then repeat steps 11 and 12 above. Continue this until the starting algorithm is complete.
14. (This step is optional) Once the motor has been manually commutated to a point where the BEMF may be detected the motor can be put in a HIZ mode by setting HIZ = 1. By observing the transitions on the SPDTACH pin it can now be determined if the motor is stuck or if it rotating. The state machine is not advanced at this point unless the EXCOMM bit is toggled low to high.
15. Once the motor has been manually commutated to a point where the BEMF may be used to reliably commutate the motor the hardware commutation can be enabled by setting COMS = 1. Once COMS = 1 the device will automatically advance the state machine T_{delay} after a zero crossing is detected on the non-exited phase.
16. (This step is optional) Once the motor is in hardware commutation mode it can again be put into to HIZ mode by setting HIZ = 1 and zero crossings may be observed at the SPDTACH pin. In this case the motor is automatically advanced T_{delay} after a zero crossing.
17. At this point closed loop hardware speed control could be enabled (see the FLL SPM Speed Control Circuit section)
18. If it is desired to close the speed control loop externally it can be done using the serial port. Commutation could be controlled by the EXCOMM bit in Register 0 and the speed could be controlled using the 3 bit DAC to set the motor current. Speed feedback is available at the SPDTACH pin where a positive pulse of width, PRESCALE / f_{OSCIN}, will appear once per 60 electrical degrees of motor rotation.

SPINDLE MOTOR CURRENT CONTROL AND COMMUTATION CIRCUITS

This system controls the amplitude and coil current slew rate in a three phase disk drive motor by controlling two phases while in steady state control and all three phases during commutations. Three sense FETs and six drivers (three pair of half H-bridges) are used to sense and control the steady state current through the coils, and control the current slew rate during commutations. The amplitude of the coil current is controlled by the low side drivers which operate in the MOS saturation region unless they are commutating or turned off. The high side drivers operate in the linear (resistive) region with their gates pulled to 5 V above the positive rail, unless they are commutating or turned off. Active clamp circuits limit the output voltage of the three amplifiers to 4.25 V.

A functional diagram of the SPM current control (neglecting commutation) is shown in Figure 11. The input voltage is either from the SPDCAP or the 3-bit DAC, controlled by the CCS bit in Register 0 of the Serial Register. The amplitude of the SPM coil currents is controlled by current mirror amplification. The voltage at the SPDCAP pin (or DAC), which can vary between 0.5 and 1.5 V, is first level shifted to vary between 0 and 1 V at the RSS pin. The external resistance at this pin determines the current into the current mirror which is amplified by 4-level gains as controlled by the serial register SPMG bits in Register 1. This resistor thus sets the transconductance gain of the amplifier and current limits to the motor. With proper commutation the motor torque is directly proportional to this current level or:

$$T = K_t I_m \qquad \text{(Equation 5)}$$

which is the same as a DC motor. In equation 5, K_t is the motor torque constant and I_m is the amplitude of the commutating current into each phase of the motor.

The commutating current slew rate is controlled by applying a constant di/dt to the sense transistors. By mirroring this constant di/dt to the driver transistor, a constant di/dt, or current slew rate is obtained in the motor winding. The purpose of controlling the slew rate of the commutating current is to limit the audible noise from the motor caused by this switching current.

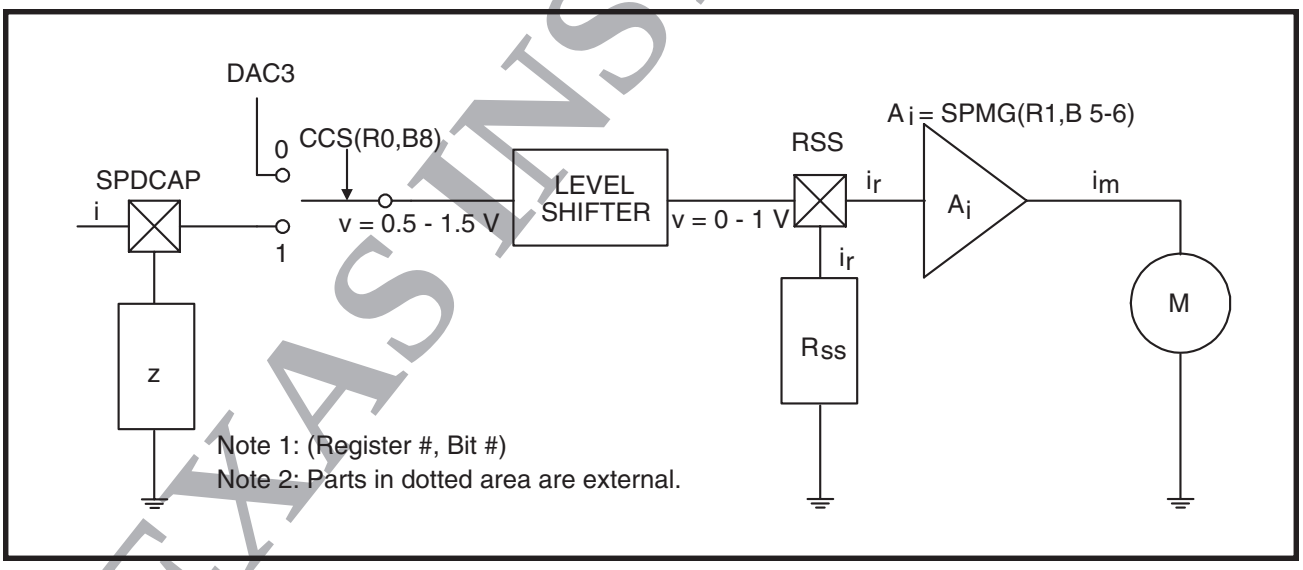


FIGURE 3.6-3: SPM Current Control

FUNCTIONAL DESCRIPTION (continued)

FLL SPM SPEED CONTROL CIRCUIT

The speed control circuit for the SSI 34H3306 is shown functionally in Figure 12. It consists of charge and discharge current sources that feed the external network connected to the SPDCAP pin, two sets of identical circuits consisting of a velocity (frequency) comparator and a 15-bit preset counter, and a rotational signal generator.

Each comparator-counter pair controls the current sources for half the time period as determined by the timing signals from the rotation signal generator. The two current sources are individually controlled for two possible values by the VCC bit in Register 3 (see the Register 3 Definition (Slew Rate/FLL Current Control) subsection of the Register Description section and the FLL Speed Control Circuit subsection of the Pin Description section). Since the voltage on the SPDCAP pin sets the desired output current level of the spindle motor pre-drive and control circuit, the FLL circuit controls the motor's torque, thus controlling the motor's speed.

Both counters in the FLL are programmed with the same count value from the RSD (Rotational Speed Data) value in Registers 2 and 3. The FLL counters are setup as two digital one-shot delays triggered by commutation in a way that will speed locks the motor. Each counter is triggered by the beginning of separate 120° electrical periods of actual motor rotation. The feedback control loop tries to make each of the 120° motor periods equal to the corresponding counter (one shot) periods. See Figure 13 and the Frequency Comparator section for more details.

The count that should be programmed into the counters (RSD) is the number of speed clock cycles in the time taken for the motor to rotate 120° electrical at the desired speed (RPM). It can be calculated as follows:

$$T_{120°} = (60/RPM) \bullet (2/N_p) \bullet (120°/360°) = 40/(RPM \bullet N_p)$$

(Equation 6)

$$RSD = T_{120°} \bullet (f_{OSCIN}/PRESCALE)$$

(Equation 7)

where N_p is the number of motor poles and PRESCALE is the programmed prescaler division ratio.

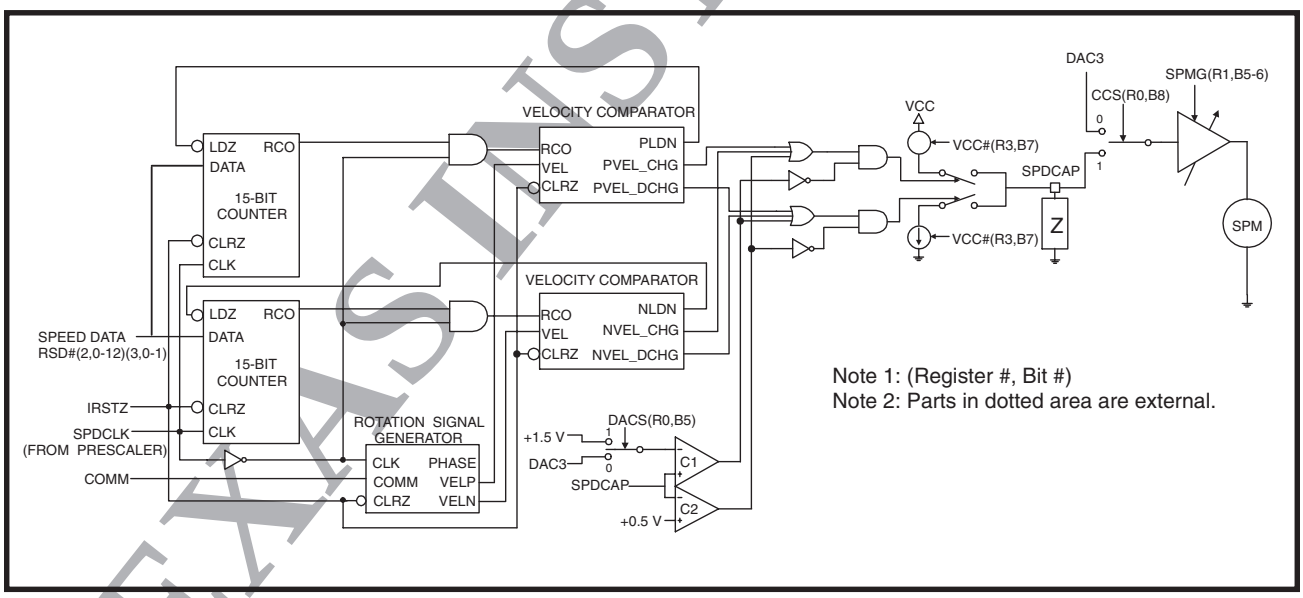


FIGURE 12: FLL Circuit

SPDTMECH/SPDTACH PIN

This pin has 2 multiplexed signals, SPDMECH or SPDTACH. The selection is done with Register 3, bit 9. SPDMECH is an index signal. It is a 50% duty cycle square wave with a period of once per SPM revolution. SPDTACH is the SPM commutation signal. It has a period of 60° electrical and is identical to the internal COMM signal except that the positive pulse is 6 SPDCLK bits wide. For an Np pole motor there are 3 • Np SPDTACH pulses per revolution.

The normal mode of operation of the FLL and speed error circuit, that uses the delayed BEMF zero crossings to measure the motor speed, requires that SPDTACH (P4,B12) bit is reset. In this case the COMM signal, described in the Spindle Control Logic section, is connected to the FLL circuits as shown in Figure 12 and to the SPDTACH pin as an output signal.

If the SPDTACH bit (R3,B9) is set, the SPDTACH pin is an input signal which is connected in place of the COMM signal in Figure 12. This mode can be used where it is desirable to use speed information from the disk sector data rather than from the BEMF. The waveform applied to the SPDTACH pin should have a positive edge for every 60° electrical of actual rotor rotation ($6N_p/2$ pulses per rev).

SPDCAP VOLTAGE CLAMP

The voltage on SPDCAP is effectively limited to from 0.5 V to 1.5 V by the comparator circuits, C1 and C2, in Figure 12. If either limit is reached the corresponding comparator output goes high which disconnects the current source connected to SPDCAP that is causing the problem and forces the opposite polarity current source to be on.

When DACS is low during startup, the DAC is used as the C1 limit voltage instead of the 1.5 V reference. This indirectly sets the SPDCAP voltage since the speed control is limiting during acceleration. However, since CCS is low at this time, the SPDCAP is not connected to the motor drive control. Instead, the CCS signal connects the 3-bit DAC to control the motor current. When the motor is close to operating speed, the CCS signal is set high connecting the SPDCAP to the motor drive control which allows the speed control to operate the motor. Since the 3-bit DAC is still connected to the limit circuit it can be used in a way that limits speed overshoot. Once the motor speed is stabilized, DACS is set high, which switches the DAC from the SPM limit circuit to the VCM where it is used as an offset compensation. The SPM current limit is now set to the maximum current for the selected range by the 1.5 V reference.

FREQUENCY COMPARATOR

A typical frequency comparator timing diagram is shown in Figure 13. The frequency control circuit in Figure 12 consists of two identical frequency (velocity) comparator (or detector) circuits. They compare the frequency of two input signals, f_{ref} and f_{fb}. The output is ideally proportional to the difference. The update rate for each of the frequency comparator circuits is once every 240° electrical of motor rotation and the current output of each is summed at the SPDCAP pin. The total output over the full 240° period is thus twice the output of one of the frequency detectors or, in other words, the overall detector gain is twice the gain of one detector over the 240° period.

The two frequency comparator circuits work on different 120° halves of the 240° cycle as determined by the complimentary VELP and VELN signals derived from the COMM motor feedback signal. The frequency of these two signals is one fourth the frequency of the COMM signal and 180° out of phase with each other. So another way to look at the system is that each detector is trying to control its corresponding half period of the feedback signal. This is the same as saying the overall detector gain is equal to either detector gain over a 120° period. This makes the effective update rate twice per 240° period which is equivalent to once per 120° period.

Since the two frequency comparators are identical only the one connected to VELN signal, the bottom circuit in Figure 12, is described in detail. The VELP signal is just the compliment of the VELN signal so that everything for the other circuit is the same but shifted by 120°.

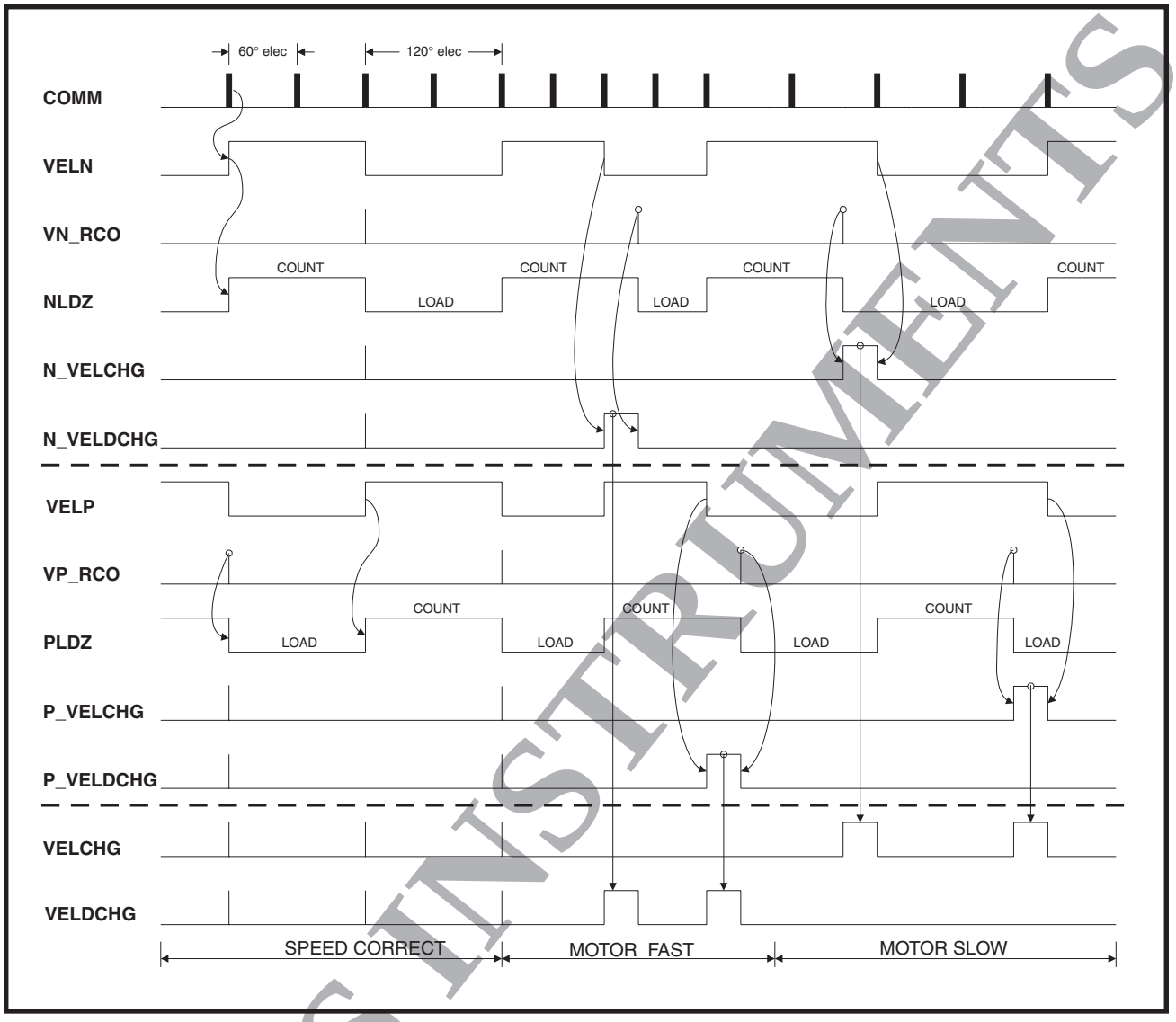


FIGURE 13: Frequency Comparator Timing

FREQUENCY COMPARATOR (continued)

Each frequency comparator circuit consists of a single 15-bit counter and a velocity comparator circuit. The VELN signal is the COMM (motor commutation signal) divided by 4 which means that it goes high on every fourth COMM pulse. This represents the feedback motor speed in terms of frequency. The pulse width of the VELN signal is thus equivalent to the rotor moving 120° electrical or the full period is 240° electrical. The count length of the 15-bit counter is programmed (by RSD) to be equivalent to the time for a 120° electrical of desired rotor movement.

Once the velocity comparator circuit receives a positive going edge on VELN, the counter is started and at the same time it sets the NLDZ flop. The counter produces an end of count signal (RCO) after a fixed time equivalent to the desired 120° electrical period which resets the NLDZ flop. The NLDZ signal can be looked at as a digital, fixed period, one-shot triggered on every fourth COMM pulse. This is the feedback signal into the frequency detector. It is easily shown that the average dc level of this signal is proportional to its frequency which is proportional to the motor speed. Since this signal is one of the inputs to the phase detector which controls the current source of value Ics connected to the SPDCAP pin, its amplitude is effectively I_{cs}.

The resulting average current into the SPDCAP pin due to the feedback signal alone is:

$$(I_{dc})_{fb} = I_{cs} \bullet T_{ref}/t_{fb} = I_{cs} \bullet T_{ref} \bullet f_{fb} = (I_{cs}/f_{ref})\, f_{fb}$$

(Equation 8)

Where I_{dc} is the average NLDZ signal of amplitude I_{cs},T_{ref} is the constant time period of 120° electrical, and f_{fb} is the feedback frequency from the motor.

The net current into the SPDCAP pin is the sum of this current and that due to the reference signal.

The two signals, N_VEL_CHG and N_VEL_DCHG, control the connection of the corresponding charge and discharge current source to the SPDCAP pin. These signals are FF outputs. The CHG FF is set when the trailing (negative) edge of the VELN signal lags the trailing edge of the NLDZ signal and the DCHG FF is set when the trailing edge of the VELN signal leads the trailing edge of the NLDZ signal. Thus it is seen that the CHG FF is set when the feedback frequency is low (slow) and the DCHG FF is set when the feedback frequency is high (fast). Since the peak motor current (and torque) is directly proportional to the voltage at the SPDCAP pin, the CHG FF tries to speed up the motor and the DCHG FF tries to slow it down.

Both flip flops are reset whenever both are set simultaneously. This means that when one is set first it resets as soon as the other one tries to set.

If the motor is running at the correct speed, the negative edges of the VELN and NLDZ signals coincide and each FF sets at the same time and immediately resets.

The other velocity compare circuit functions the same way on the positive half of the VELP signal which is the same as the negative half of the VELN signal. P_VEL_CHG and P_VEL_DCHG are generated that tend, respectively, to speed up and slow down the spindle motor. So it is seen that each half of the 240° feedback signal (VELN or VELP) is controlled separately by the 120° reference pulse of the counter such that they are equal to 120° electrical of motor rotation at the commanded speed.

It can be shown that the average value of each frequency Detector output is proportional to the difference between the reference frequency ($1/T_{ref}$) and the feedback frequency. In this case the feedback frequency period is 120° electrical or half the period of the VELN or VELP signals.

FREQUENCY COMPARATOR GAIN FACTOR

The gain function of the frequency detector block (average DC current output per cycle of frequency difference) is:

$$G_{fd} = I_{cs}/f_{ref} = I_{cs}\, T_{ref} \text{ in amps per Hz}$$

(Equation 9)

I_{cs} is the current source programmed to the SPDCAP pin, and T_{ref} is $T_{120°}$ given in Equation 6.

G_{fd} is defined by:

$$I_{dc}(A) = G_{fd}(f_{ref} - f_{fb})$$

(Equation 10)

I_{dc} is the average DC current at the SPDCAP pin.

FUNCTIONAL DESCRIPTION (continued)

SPDCAP PIN COMPENSATION NETWORK

To have a true frequency lock loop speed control where there is no average frequency error there must be an integrator in the forward loop. The only place to do this in the SSI 34H3306 is at the SPDCAP pin. If a simple capacitor is used the system is unstable. A more complex network must be used. The simplest of these is a lead-lag network consisting of one resistor and two capacitors as shown in Figure 14.

Since the SPDCAP pin is fed from a current source the transfer function of current to voltage is just the complex impedance to ground which is also given in Figure 14. Normally this network is designed to make the overall open loop transfer function cross the zero db point at the desired loop bandwidth and to cross at a slope of 20 dB/decade. The two break frequencies of the network are normally chosen such that the zero db point Is at the geometric mean of the two and the ratio of f_2 to f_1 is about 10. This usually will result in enough phase margin for a stable system but other performance factors may need to be considered. Since this system is actually a sampled data system, one criteria for the closed loop band width is that it should be at most 1/5 of the sampling rate to avoid excessive sampled data lag. This allows the system to be treated as a linear system.

SPEED CONTROL SERVO LOOP BLOCK DIAGRAM

An overall speed control system block diagram is shown in Figure 15. The reference frequency, f_{ref}, is $1/T_{120}$ given in Equation 6. G_{fd} is the frequency discriminator gain factor and is given in the Frequency Comparator Gain Factor section. The motor transfer function, G_m, can usually be simplified to K_t/Js when the viscous damping constant, K_d, is small. $Z_c(s)$ is the compensation network connected to the SPDCAP pin as discussed in the SPDCAP Pin Compensation Nework section. R_{ss} is the resistor connected to the RSS pin which is 2 kΩ for nominal output current ranges. The power amplifier current gain, G_a, is selectable through the serial port as 4 different levels.

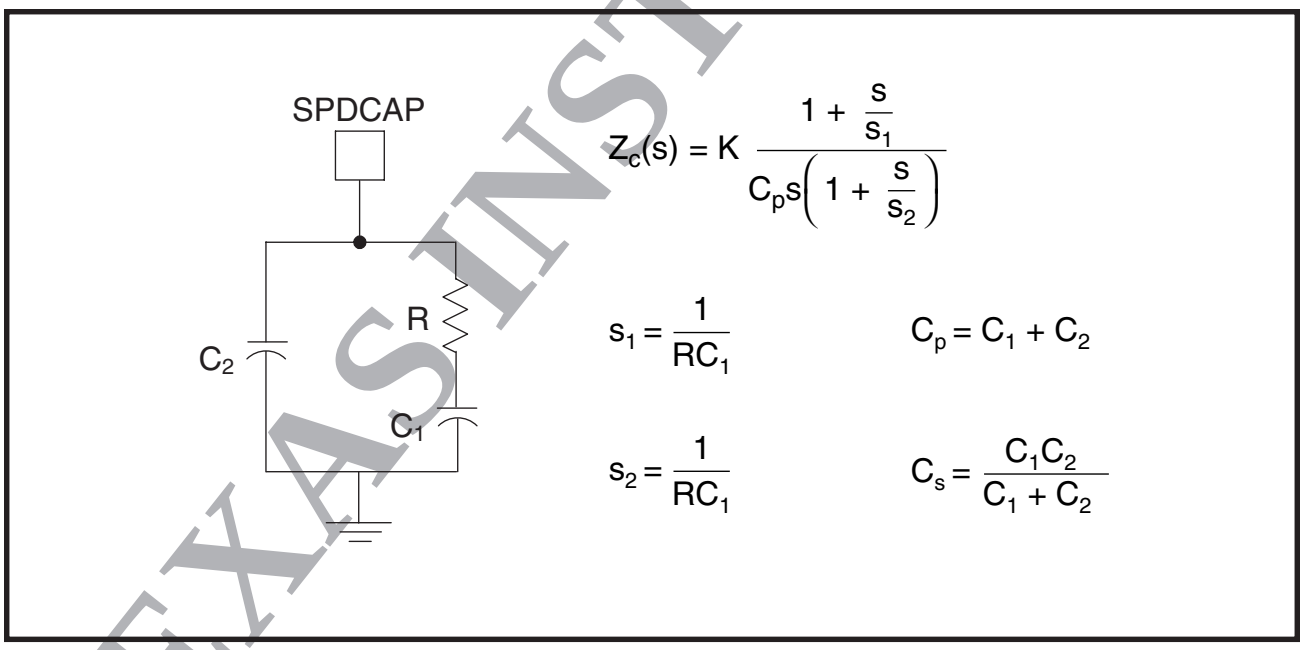


FIGURE 14: Lead-Lag Compensation Network

The generalized open loop gain is given in Figure 15. The open loop transfer function for this system using a compensation network as in the SPDCAP Pin Compensation Network section is:

$$GH(s) = K\frac{1+\frac{s}{s_1}}{s^2\left(1+\frac{s}{s_2}\right)}, \text{ where } K = \frac{30\,G_a K_t I_{cs}}{\pi(RPM)R_{ss}J_l Cp}$$

$$s_1 = \frac{1}{RC_1},\ C_p = C_1 + C_2$$

$$s_2 = \frac{1}{RC_s},\ C_s = \frac{C_1C_2}{C_1 + C_2}$$

(Equation 11)

For these equations K_t is the motor torque constant in Nm/A, J_L is the load moment of inertia in Kgm^2, G_a is the programmed power amplifier current gain and I_{cs} is the programmed charge and discharge current which are assumed equal.

SPM CLAMP

There are three different clamp circuits connected to the driver transistors. One protects the V_{ds} of the LSD driver transistors and limits V_{ds} to 4.25 V maximum. The other two prevent V_{gs} of both HSD and LSD driver transistors from going beyond 6 V.

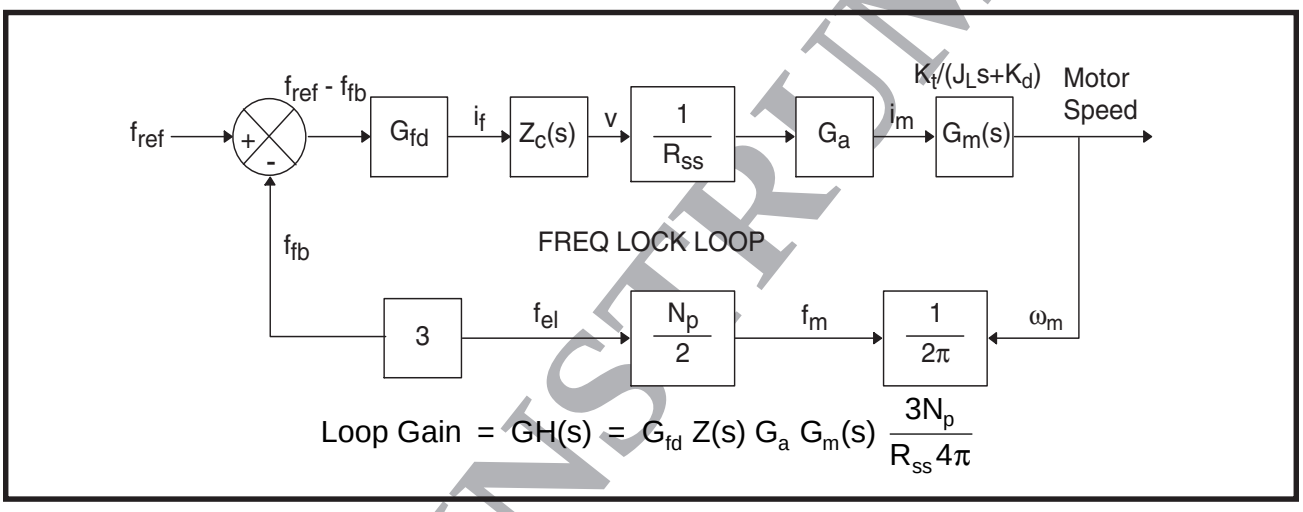


FIGURE 15: Speed Control Block Diagram

REGISTER DESCRIPTION

TABLE 3: Register Selection

REGISTER #	PT3	PT2	PT1	DESCRIPTION
0	0	0	0	SPM control circuit mode set/power save control
1	0	0	1	3-bit DAC
2	0	1	0	Rotation control 1
3	0	1	1	Rotation control 2/Slew rate/FLL current control
4	1	0	0	Phase delay control/SPDTACH I/O CTRL
6	1	1	0	Programmable PES gain and window threshold

REGISTER 0 DEFINITION (SPM CONTROL CIRCUIT MODE SET/POWER SAVE CONTROL)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	PS0		Enable VCM
1	PS1		Enable SPM
2	SPNENA	Spindle	SPM ENABLE
3	0		TI reserved (always set to 0)
4	COMS	Spindle	1: Hardware (BEMF) 0: Software (EXCOMM)
5	DACS	Spindle	Select FLL clamp 1: 1.5 V 0: 3-Bit DAC
6	BRAKE	Spindle	Dynamic brake 1: Enable 0: Disable
7	HIZ	Spindle	All phases Hi-Z 1: Enable 0: Disable
8	CCS	Spindle	FLL mode control 1: FLL 0: 3-bit DAC
9	ENNCP	Spindle	0: Disable negative clamp 1: Enabled
10	DT0	Spindle	OSCIN prescaler divider 0 (Table 5)
11	DT1	Spindle	OSCIN prescaler divider 1 (Table 5)
12	EXCOMM	Spindle	Manual state machine advance
13	PT1 = 0		Register select address 1 (Table 3)
14	PT2 = 0		Register select address 2 (Table 3)
15	PT3 = 0		Register select address 3 (Table 3)

TABLE 4: POWER SAVE MODE SELECT IN REGISTER 0

MODE SELECT	PS1	PS0	RESET CIRCUIT, AND BANDGAP REFERENCE	SPM CIRCUIT CHARGE PUMP	VCM CIRCUIT TRACKING LOOP
MODE1	0	0	ON	OFF	OFF
MODE2	1	0	ON	ON	OFF
MODE3	1	1	ON	ON	ON

TABLE 5: PRESCALER SETTING IN REGISTER 0

DT1	DT0	RATIO
0	0	2
0	1	4
1	0	8
1	1	16

REGISTER 1 DEFINITION (3-BIT DAC/SPM CONTROL)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	SPMDAC0	Spindle	3-bit DAC data (LSB)
1	SPMDAC1	Spindle	3-bit DAC data
2	SPMDAC2	Spindle	3-bit DAC data
3	MECDIV0	Spindle	Programmable divider, bit 0 (Table 6)
4	MECDIV1	Spindle	Programmable divider, bit 1 (Table 6)
5	SPMG0	Spindle	Current gain select 0 00: GAIN0 01: GAIN1 (Table 7)
6	SPMG1	Spindle	Current gain select 1 10: GAIN2 11: GAIN3 (Table 7)
7	0		TI reserved (always set to 0)
8	0		TI reserved (always set to 0)
9	FLTZCRSENA	Spindle	0: SPDTACH 1: FILTERED BEMF
10	0		TI reserved (always set to 0)
11	0		TI reserved (always set to 0)
12	0		TI reserved (always set to 0)
13	PT1 = 1		Register select address (Table 3)
14	PT2 = 0		Register select address (Table 3)
15	PT3 = 0		Register select address (Table 3)

REGISTER DESCRIPTION (continued)

TABLE 6: PROGRAMMABLE DIVIDER IN REGISTER 1

MECDIV1	MECDIV0	MOTOR POLE	DIVIDER BY
0	0	16	12
0	1	8	6
1	0	20	15
1	1	-	-

TABLE 7: SPINDLE CURRENT GAIN IN REGISTER 1

	SPMG1	SPMG0	GAIN
GAIN0	0	0	1700
GAIN1	0	1	
GAIN2	1	0	570
GAIN3	1	1	340

REGISTER 2 DEFINITION (ROTATION CONTROL 1)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	RSD2	Spindle	Rotation speed data (see Note 1).
1	RSD3	Spindle	Rotation speed data
2	RSD4	Spindle	Rotation speed data
3	RSD5	Spindle	Rotation speed data
4	RSD6	Spindle	Rotation speed data
5	RSD7	Spindle	Rotation speed data
6	RSD8	Spindle	Rotation speed data
7	RSD9	Spindle	Rotation speed data
8	RSD10	Spindle	Rotation speed data
9	RSD11	Spindle	Rotation speed data
10	RSD12	Spindle	Rotation speed data
11	RSD13	Spindle	Rotation speed data
12	RSD14	Spindle	Rotation speed data(MSB)
13	PT1 = 0		Register select address (Table 3)
14	PT2 = 1		Register select address (Table 3)
15	PT3 = 0		Register select address (Table 3)

NOTE 1: RSD L.O. bits are in Register 3

TABLE 3.1-5 REGISTER 3 DEFINITION (SLEW RATE/FLL CURRENT CONTROL)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	RSD0	Spindle	Rotation speed data (see Note 2)
1	RSD1	Spindle	Rotation speed data
2	0		TI reserved (always set to 0)
3	0		TI reserved (always set to 0)
4	0		TI reserved (always set to 0)
5	0		TI reserved (always set to 0)
6	VCMBRK	VCM	VCM brake
7	VCC	Spindle	Velocity current control (chg/dischg) 0: 150 1: 300
8	0		TI reserved (always set to 0)
9	SPDTACH/ SPDMEC	Spindle	Selects multiplexed output 0: SPDMEC 1: SPDTACH
10	SR	Spindle	Slew rate 1: on(slow) 0: off(fast)
11	0		TI reserved (always set to 0)
12	0		TI reserved (always set to 0)
13	PT1 = 1		Register select address (Table 3)
14	PT2 = 1		Register select address (Table 3)
15	PT3 = 0		Register select address (Table 3)

NOTE 2: RSD H.O. bits are in Register 2

REGISTER DESCRIPTION (continued)

REGISTER 4 DEFINITION (PHASE DELAY CONTROL)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	PDT0	Spindle	Phase delay time data (LSB)
1	PDT1	Spindle	Phase delay time data
2	PDT2	Spindle	Phase delay time data
3	PDT3	Spindle	Phase delay time data
4	PDT4	Spindle	Phase delay time data
5	PDT5	Spindle	Phase delay time data
6	PDT6	Spindle	Phase delay time data
7	PDT7	Spindle	Phase delay time data
8	PDT8	Spindle	Phase delay time data
9	PDT9	Spindle	Phase delay time data
10	PDT10	Spindle	Phase delay time data
11	PDT11	Spindle	Phase delay time data (MSB)
12	SPDTACH	Spindle	SPDTACH I/O Select 1: Input 0: Output
13	PT1 = 0		Register select address (Table 3)
14	PT2 = 0		Register select address (Table 3)
15	PT3 = 1		Register select address (Table 3)

REGISTER 5 DEFINITION - RESERVED FOR TI USE ONLY (SEE NOTE 1)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0-12	T0-T12		Reserved (always set to 0)
13	PT1 = 1		Register select address (Table 3)
14	PT2 = 0		Register select address (Table 3)
15	PT3 = 1		Register select address (Table 3)

NOTE 1: To access this register bit 3 of Register 0 must be high (1)

REGISTER 6 DEFINITION: TRACKING LOOP SUPPORT

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	PESGN0	VCM	PES amplifier programmable gain
1	PESGN1	VCM	PES amplifier programmable gain
2	PESGN2	VCM	PES amplifier programmable gain
3	PESGN3	VCM	Sense amplifier programmable gain
4	SENGN0	VCM	Sense amplifier programmable gain
5	SENGN1	VCM	Sense amplifier programmable gain
6	SENGN2	VCM	Sense amplifier programmable gain
7	ENVCM	VCM	0: Disable actuator amplifier 1: Enabled
8	WTHRES0	VCM	Programmable window threshold
9	WTHRES1	VCM	Programmable window threshold
10	WTHRES2	VCM	Programmable window threshold
11	WTHRES3	VCM	Programmable window threshold
12	MUX	VCM	1: CPES_OUT 0: COMP_OUT
13	PT1 = 0		Register select address (Table 3)
14	PT2 = 1		Register select address (Table 3)
15	PT3 = 1		Register select address (Table 3)

TABLE 8: ENVCM CONTROL LOGIC

PS0	PS1	ENVCM	DESCRIPTION
1	1	0	VCM loop is disabled
1	1	1	VCM loop is enabled

REGISTER DESCRIPTION (continued)

TABLE 9: INTERNAL REGISTER SUMMARY

BIT #	REGISTER 0	REGISTER 1	REGISTER 2	REGISTER 3	REGISTER 4	REGISTER 5	REGISTER 6
0	PS0	SPMDAC0	RSD2	RSD0	PDT0	0	PESGN0
1	PS1	SPMDAC1	RSD3	RSD1	PDT1	0	PESGN1
2	SPNENA	SPMDAC2	RSD4	0	PDT2	0	PESGN2
3	0	MECDIV0	RSD5	0	PDT3	0	PESGN3
4	COMS	MECDIV1	RSD6	0	PDT4	0	SENGN0
5	DACS	SPMG0	RSD7	0	PDT5	0	SENGN1
6	BRAKE	SPMG1	RSD8	VCMBRK	PDT6	0	SENGN2
7	HIZ	0	RSD9	VCC	PDT7	0	ENVCM
8	CCS	0	RSD10	0	PDT8	0	WTHRES0
9	ENNCP	FLTZCRSENA	RSD11	SPDTACH/ SPDMEC	PDT9	0	WTHRES1
10	DT0	0	RSD12	SR	PDT10	0	WTHRES2
11	DT1	0	RSD13	0	PDT11	0	WTHRES3
12	EXCOMM	0	RSD14	0	SPDTACH	0	MUX
13	PT1 = 0	PT1 = 1	PT1 = 0	PT1 = 1	PT1 = 0	PT1 = 1	PT1 = 0
14	PT2 = 0	PT2 = 0	PT2 = 1	PT2 = 1	PT2 = 0	PT2 = 0	PT2 = 1
15	PT3 = 0	PT3 = 0	PT3 = 0	PT3 = 0	PT3 = 1	PT3 = 1	PT3 = 1

PIN DESCRIPTION

Pin types are defined as: A = Analog; D = Digital; G = Ground; I = Input; O = Output; Power = P

The pin functions are listed below grouped by function

SUPPLIES

PIN #S	NAME	TYPE	DESCRIPTION
54	AVCC	P	3.3 V analog power supply
8	DVCC	P	3.3 V digital power supply
34	VCMVCC	P	VCM power supply (2 bond pads)
14,18	SPNVCC	P	Spindle power supply (2 bond pads)
*1,12,*28, *29,42,52,*56	AGND	A/G	Analog ground
10	DGND	D/G	Digital ground
37	VCMGND	G	VCM ground (2 bond pads)
16,20	SPNGND	G	Spindle ground (2 bond pads)
2	VPP	P	3 V power supply and EEPROM programming voltage

NOTE: In the above table the symbol (*) indicates that additional pins can be used for heat sinking.

MISCELLANEOUS

50	VTEMP	A	Temperature sense output
7	OSCIN	D/I	Charge pump and commutating clock
48	RBIAS	A	Internal bias current setting
53	VDD	A	Charge pump capacitor pin

VOLTAGE MONITOR

49	CPOR	A	Power-on reset delay capacitor
51	RSTZ	D/O	Power-on reset output

SERIAL PORT

4	SCLK	D/I	Serial port input clock
5	SDATA	D/I	Serial port data
6	SENA	D/I	Serial port select (Active High)

PIN DESCRIPTION (continued)

Pin types are defined as: A = Analog; D = Digital; G = Ground; I = Input; O = Output; Power = P

VCM

PIN #S	NAME	TYPE	DESCRIPTION
32	CMPI	A	VCM current loop compensation filter
31	CMPO	A	VCM current loop compensation filter
40	VREFOUT	A	VCM reference voltage output
41	VREFC	A	VCM reference voltage capacitor input
39	RSENP	A	Positive VCM current loop sense
38	RSENN	A	Negative VCM current loop sense
33	FBOUT	A	Current sense amplifier output
36	VCMB	A	VCM driver output B
35	VCMA	A	VCM driver output A

TRACKING LOOP SUPPORT

47	COMP_OUT	A	Tracking loop compensation output
46	COMP_IN	A	Tracking loop compensation input
45	CPES_OUT	A	Composite position error output
44	COMP_SUM	A	Loop compensation summing point
43	CPES_IN	A	Position error input
30	WINOUT	D	Window comparator output
27	TF	D	Track following control input
26	SAMPLEZ	D	Sample position error/hold

SPINDLE MOTOR

3	SPDMEC/ SPDTACH	D/O	Spindle speed mech output/tachometer output
9	SPDCAP	A	Speed loop compensation network connection
11	CTS	A	Center tap sense
15	U	A	Spindle phase U output
17	V	A	Spindle phase V output
19	W	A	Spindle phase W output
21	RSS	A	Maximum SPM current limiting resistor
22	SPNCAP	A	Spindle slew rate control cap

SHOCK SENSOR

PIN #S	NAME	TYPE	DESCRIPTION
24	SHOCKIN	A	Shock sensor amplifier input
25	SHOCKOUT	A	Shock sensor amplifier output
23	VTRIP	D	Shock sensor output

OTHER PINS

13			No Connects
55			Reserved

MECHANICAL DATA

The SSI 34H3306 mechanical outline dimensions are shown below. (TBR)

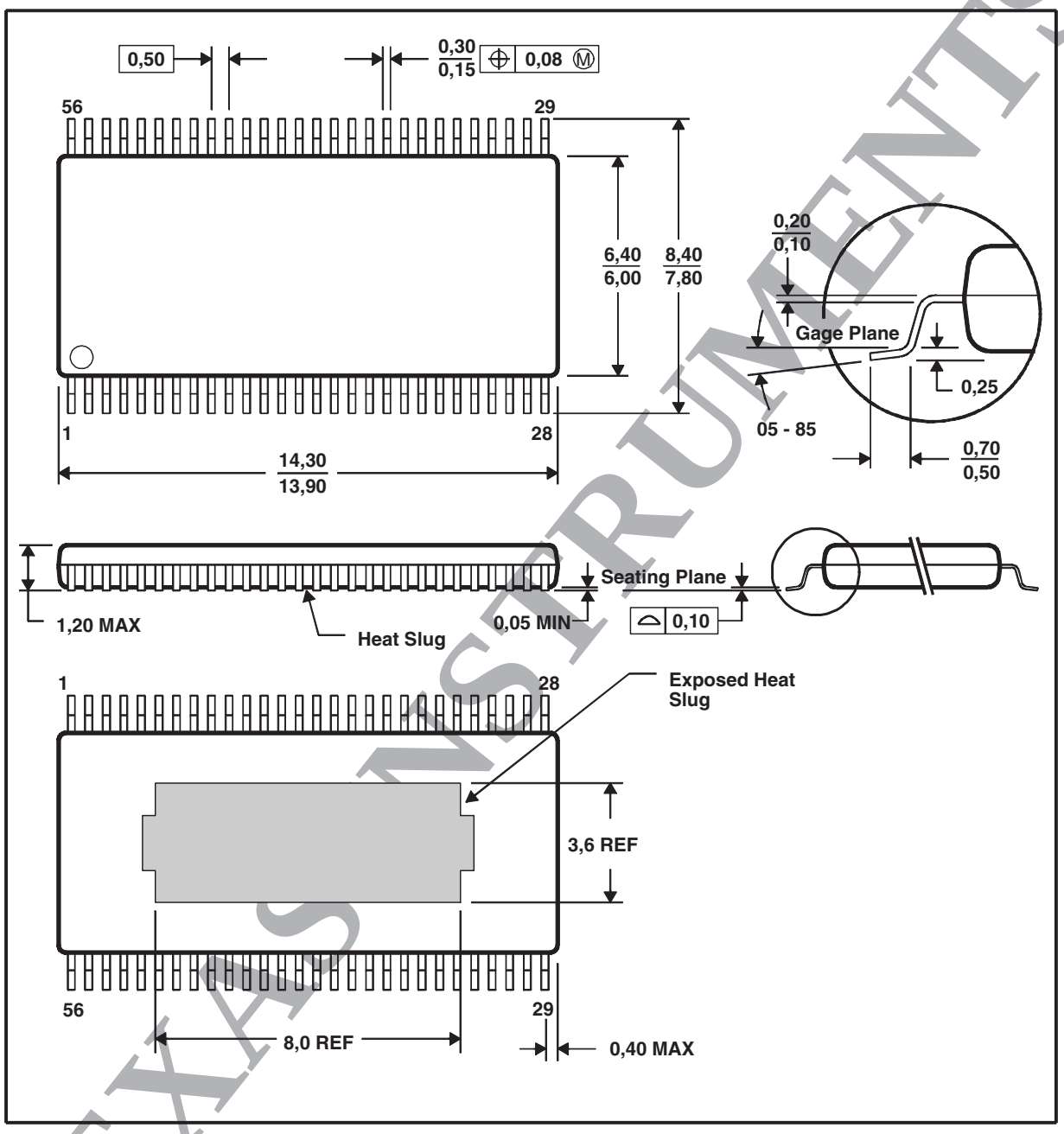


FIGURE 17: Mechanical Data

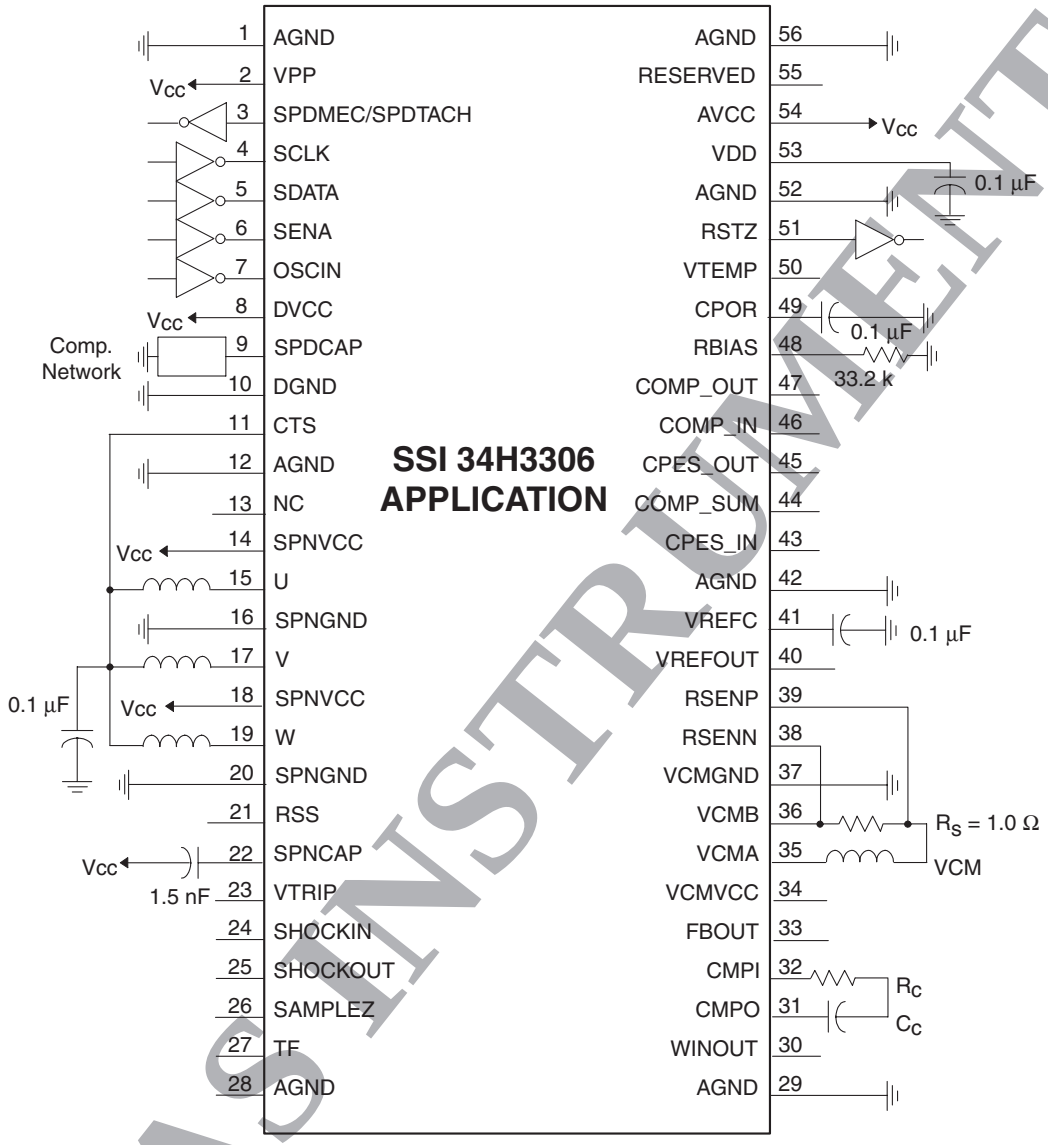
NOTES: A. All linear dimensions are in millimeters

B. This drawing is subject to change without notice

C. Thermally enhanced molded plastic package with a exposed heat slug (HSL) on bottom

PACKAGE PIN DESIGNATIONS

(Top View)



56-Pin Package

CAUTION: Use handling procedures necessary for a static sensitive component.

Preproduction: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

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SSI 34H3307
Servo Combo Driver

Prototype

March 1999

DESCRIPTION

The SSI 34H3307 provides the capability to drive a voice-coil motor (VCM) and spindle motor of a disk drive system. The spindle section is a complete speed control servo system including power and pre-drivers requiring only a few additional discrete components for full functionality. The VCM section is a complete feedback controlled transconductance amplifier with power and pre-drivers. Only a few external compensation components are necessary to reshape the VCM closed-loop response. A serial interface is provided to program and read back the internal registers for all user-selectable functions. Other supporting functions are provided to facilitate the control of VCM during tracking. The SSI 34H3307 also includes a voltage monitor circuit, a 1.8 V voltage regulator, and a 3.3 V voltage regulator. The diagram on the following page shows a functional block diagram of the SSI 34H3307 chip.

FEATURES

GENERAL

- **5 V operation, 3.3 V/5 V digital inputs**
- **Serial port interface (20 Mbit/s data transfer rate)**

VOICE COIL MOTOR (VCM) DRIVER

- **High efficiency drivers, 1.5 Ω Rds(on) total**
- **0.6 A capability**
- **Sense resistor current control**
- **5-bit programmable gain for CPES signal**
- **2-mode window comparator with 4-bit programmable threshold**
- **4-bit programmable gain for sense amplifier**

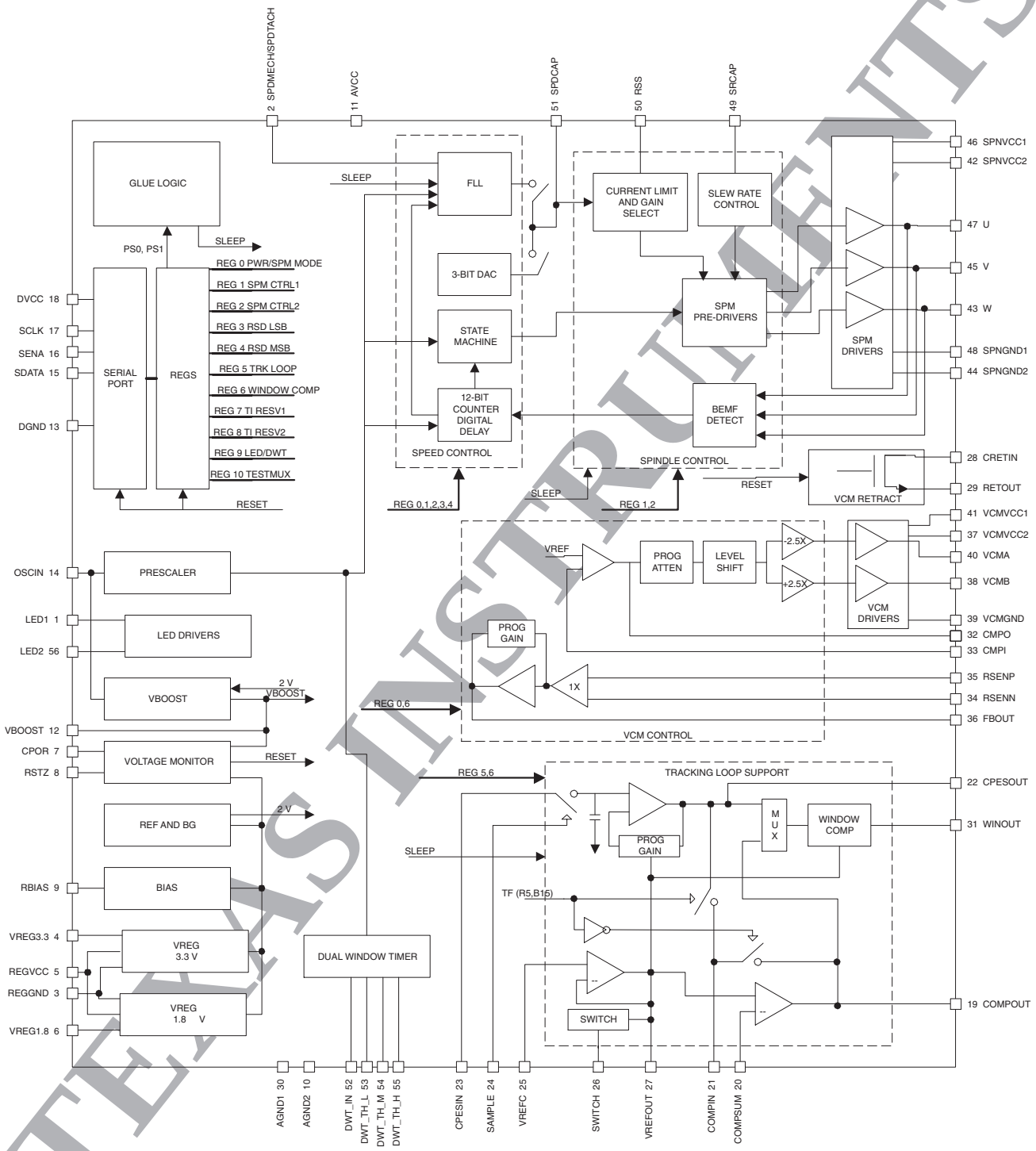
SPINDLE MOTOR DRIVER

- **High efficiency drivers, 1.0 Ω Rds(on) total**
- **1.0 A capability**
- **Digital commutation delay and blanking**
- **Bipolar drive**
- **3-bit DAC for start up current**
- **Driver slew rate control by setting an external capacitor**
- **FLL rotation speed control**

VOLTAGE MONITOR/VOLTAGE REFERENCE

- **Supply voltage fault/reset detector provides ±1% tolerance**
- **3.3 V voltage regulator with 120 mA load capability**
- **1.8 V voltage regulator with 50 mA load capability**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

SERIAL PORT AND REGISTER MAP

The serial port interface is a bi-directional data port for writing to and reading from the SSI 34H3307's ten internal registers (see the Register Description section for information about the SSI 34H3307's internal registers). The serial port is enabled for data transfers when the Serial Data Enable (SENA) pin is high ("1"). SENA should be asserted high prior to any transmission and it should remain high until the completion of the transfer. At the end of each transfer SENA should be brought low ("0"). Upon power up, the serial port Registers default to the state shown in Table 4. Register values are not reset by setting the SSI 34H3307 into sleep mode (see the Power Management Modes section for a description of sleep mode).

When SENA is high, data applied to the Serial Data (SDATA) pin can be clocked into the device. The data is clocked serially into an internal shift register on each rising edge of the Serial Clock (SCLK). The SCLK should toggle only when a valid bit of address/ instruction or data is being transferred across the serial data line. The maximum serial clock frequency is 20 MHz. Serial data is transmitted across the interface in 16-bit packets. If more than 16 SCLK pulses are received during the time that SENA is high, the additional SCLK and SDATA information will be ignored. During a serial data transmission, if SENA is switched low before 16 SCLK pulses are received, that serial transmission will be aborted. For all valid transmissions during write, the data is latched into the internal register on the falling edge of SENA. SCLK, SENA, SDATA are 3.3 V/5 V compatible.

Each transmission includes 1 R/W instruction bit, 3 device identificaton (DID) bits, 4 register address bits, and 8 data bits. The R/W instruction bit is used as a flag to put the port into read mode or write mode. The DID bits are used to select the chip for serial transmission and the DID of 111b is reserved for all servo devices. The SSI 34H3307's DID is 111b. The address bits select the internal register to be written to or read from (depending on the state of the R/W bit.) The address and data fields are input LSB first, MSB last, where LSB is defined as Bit 0. Figure 19 shows the serial interface timing diagram. Detailed timing information is given in the Serial Interface Timing section of the Electrical Specifications.

FUNCTIONAL DESCRIPTION (continued)

POWER MANAGEMENT MODES

There are four power modes in the SSI 34H3307: sleep mode, standby mode, active mode and calibrate mode. These modes are selected by setting the PS0 and PS1 bits in Register 0.

Sleep Mode

Selecting serial port bit PS0 = 0, PS1 = 1 puts the SSI 34H3307 in sleep mode. In sleep mode, VCM, tracking loop, and spindle are OFF. The bandgap is ON. 3.3 V and 1.8 V regulators are both ON. Voltage Monitor is up with fine voltage sensing, but a coarse POR current is used for timing. Over temperature detection circuit is turned off. Voltage boost circuit (charge pump) is OFF. Register values are not reset in sleep mode. A power fault resets the registers and also puts the chip into sleep mode.

Standby Mode

Selecting PS0 = 1, PS1 = 0 puts the SSI 34H3307 in standby mode. Bandgap and two voltage regulators are ON in standby mode. POR circuits are ON including the over temperature detection function. Voltage boost

circuit is also ON. VCM, tracking loop and spindle are OFF. Register values are not reset in standby mode.

Active Mode

Selecting PS0 = 1, PS1 = 1 puts the SSI 34H3307 in active mode. In active mode, all the SSI 34H3307 functions are ON.

Calibrate Mode

Selecting PS0 = 0, PS1 = 1 puts the SSI 34H3307 in calibrate mode. Calibrate mode turns on all the SSI 34H3307 functions except VCM.

VOLTAGE MONITOR/OVER-TEMPERATURE DETECTOR

The voltage monitor circuit monitors the AVCC power source and generates an internal (IRSTZ) and external (RSTZ) power-on-reset signal anytime the voltage is less than Vpor. The IRSTZ signal is the same as the RSTZ signal or'd with the over-temperature detector. IRSTZ is used as a general reset, to retract the VCM actuator, and to coast the SPM when power is turned off or a power fault exists. A second pin (CPOR pin) is provided for a large capacitor that generates a power-on delay before the reset condition is released on power-up. The capacitor is sized for the desired RSTZ delay. No other component should be connected to this terminal. For low overall power supply current, a coarse charging current is used. For CPOR this will add to variability in the CPOR timing.

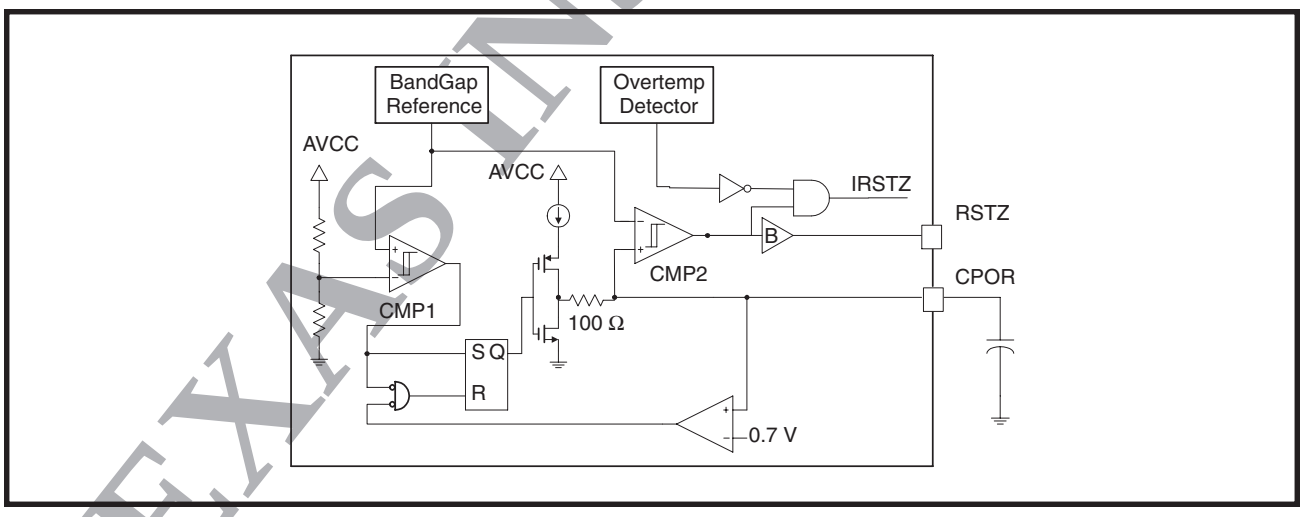


FIGURE 1: Voltage Monitor Circuit

Detailed Circuit Description

As the power supply (AVcc) ramps up and reaches Vop (see Figure 20), RSTZ becomes active (low). When it reaches Vpor+Vh, CMP1 output switches to low and the external capacitor connected to CPOR starts to charge up at a rate determined by the current generator and the CPOR capacitor. When CPOR reaches the reference voltage, CMP2 switches and RSTZ goes inactive (high). If AVcc then drops below Vpor, the capacitor discharges rapidly and RSTZ goes low. If Vcc starts to ramp up after falling below Vpor, CPOR stays low (0 V) until AVcc again goes above Vpor + Vh at which point CPOR starts to charge up and after the delay, enables RSTZ to go high (see Figure 20).

VBOOST

The function of the charge pump circuit (Figure 2) is to generate a VCC + 5 V power source (VBOOST) from the AVCC power source. This higher voltage is required for the SPM and VCM high side MOSFET gate control and to power internal circuits for the retract functions during a power fault condition. The VBOOST pin out is to allow for the connection of an external filtering/ storage capacitor. The charge pump is clocked directly from the external oscillator.

Detailed Circuit Description

When the chip is brought out of sleep mode, the charge pump becomes activated. During the negative half cycle of OSCIN signal, the negative sides of C1 and C3 are at ground, while the negative side of C2 is at the supply voltage (nominally 5 V). During this time, C1 charges through the Schottky diode, and any charge on C2 is passed to C3. During the positive half cycle, the positive sides of C1 and C3 are pushed up to the supply voltage, while the negative side of C2 is at ground. During this time, the positive sides of C1 and C3 are elevated above the power supply rails by the pair of inverters so that the charge on C1 is passed to C2 through the second Schottky diode, and the charge on C3 is likewise passed on to the external capacitor. A fraction of the charge pump output on the VBOOST pin is compared with an internally generated voltage reference in order to regulate the output voltage to VCC + 5 V. Once the output reaches VCC + 5 V, the comparator trips, which resets the latch and the charge pump is disabled. Should the voltage fall below VCC + 5 V, the comparator will trip again to re-enable the charge pump. The diode between VBOOST and AVCC is to ensure there is always enough voltage on the charge cap for the other circuits supplied by VBOOST to function at startup.

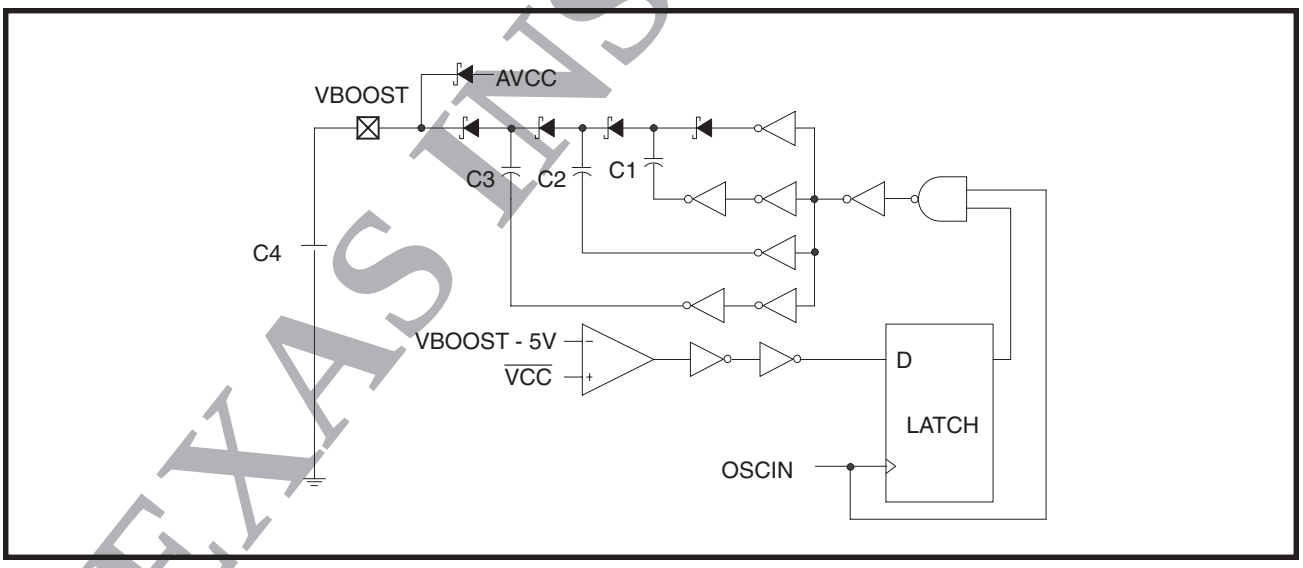


FIGURE 2: VBOOST Circuit

FUNCTIONAL DESCRIPTION (continued)

3.3 V VOLTAGE REGULATOR

The 3.3 V voltage regulator provides 120 mA (max.) DC output for other external circuits. The maximum loading it can sustain is 300 mA peak for 10 µs. The output voltage level is in the range of 3 to 3.6 V (i.e.; ±10% tolerance). The regulator can provide full current in all power management modes. Figure 3 shows a simplified block diagram of the 3.3 V voltage regulator.

1.8 V VOLTAGE REGULATOR

The 1.8 V voltage regulator provides 50 mA (max.) DC output for other external circuits. The maximum loading it can sustain is 95 mA peak for 10 µs. The output voltage level is in the range of 1.62 to 1.98 V (i.e.; ±10% tolerance). The regulator can provide full current in all power management modes. Figure 4 shows a simplified block diagram of the 1.8 V voltage regulator.

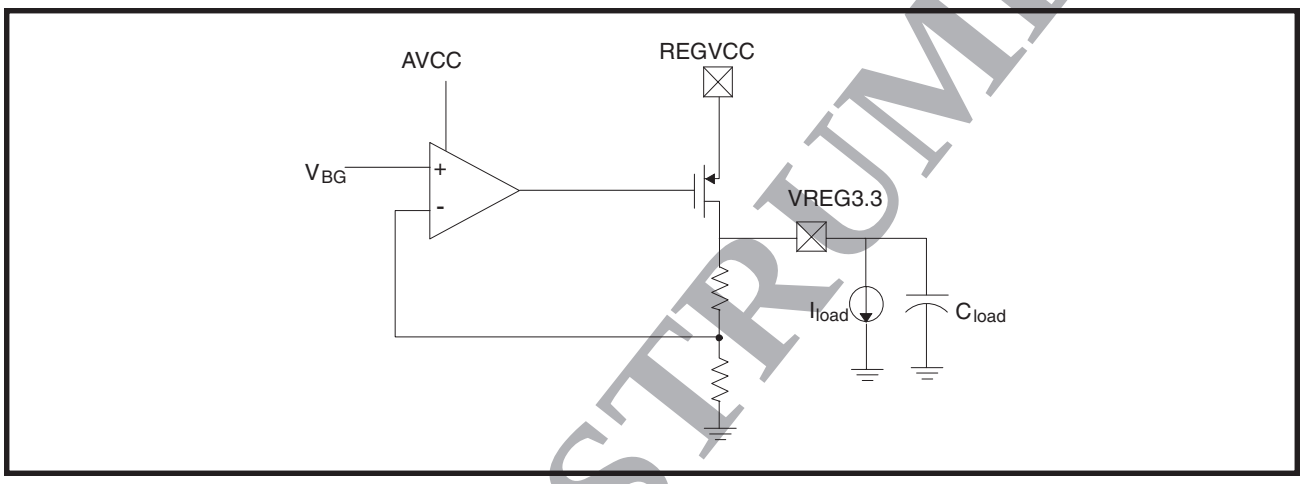


FIGURE 3: 3.3 V Voltage Regulator

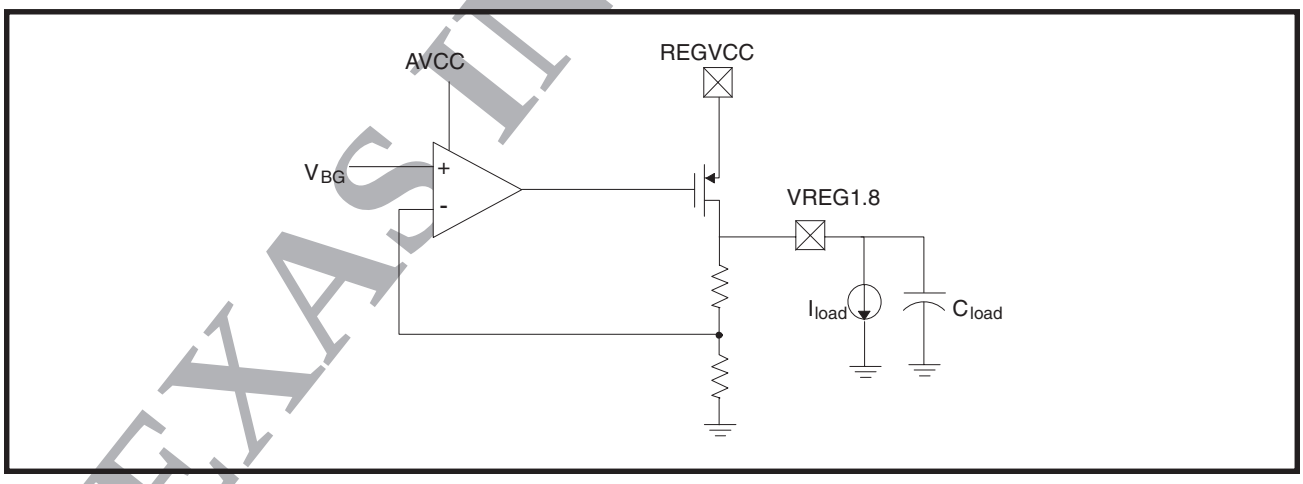


FIGURE 4: 1.8 V Voltage Regulator

VOICE COIL MOTOR CONTROL

The Voice Coil Motor (VCM) Control system (see Figure 5) is a complete feedback controlled current amplifier for operating a VCM mechanism in a disk drive unit. It consists of a full bridge power drive and a pre-driver. The power driver is an amplifier using an external sense resistor for current feedback. The feedback gain (16 levels) can be adjusted by a programmable sense amplifier through the serial port. The VCM reference voltage can be toggled between VCC/2 and 3.3 V/2 by Register 2, bit 10. External connections are provided for a compensation network to set gain, bandwidth and phase response of the current amplifier. Provision is also made for a position loop compensation network.

VCM Detailed Description

The voice-coil full-bridge power amplifier is capable of ±0.6 A output current and has a maximum $r_{DS(on)}$ resistance of 1.5 Ω. The voice coil control system uses an external sense resistor in series with the motor to detect load current. The six amplifiers, A_1 to A_6, together with the sense resistor and the external resistors, R_i and R_f, make up a current feedback control loop. The result is a transconductance gain from the input resistor to the VCM load current that is:

$$G_{vcm} = I_m/V_{in} = R_f/(G_{SENGN}\, R_i\, R_s)$$
for the values shown in Figure 5

(Equation 1)

This transconductance gain is programmable from 2.67 to 6.34 through the serial interface (SENGN, R6, B12-15). A programmable attenuator controlled by SENGN appears after the compensation amplifier, so as to maintain a fixed loop gain for stability reasons. The VCM loop includes provision for an external compensation network for shaping the frequency response of the transconductance amplifier. The compensation network is usually a simple R-C circuit. The output voltage of the power amplifier is limited to 6.3 V by active clamp circuitry (not shown).

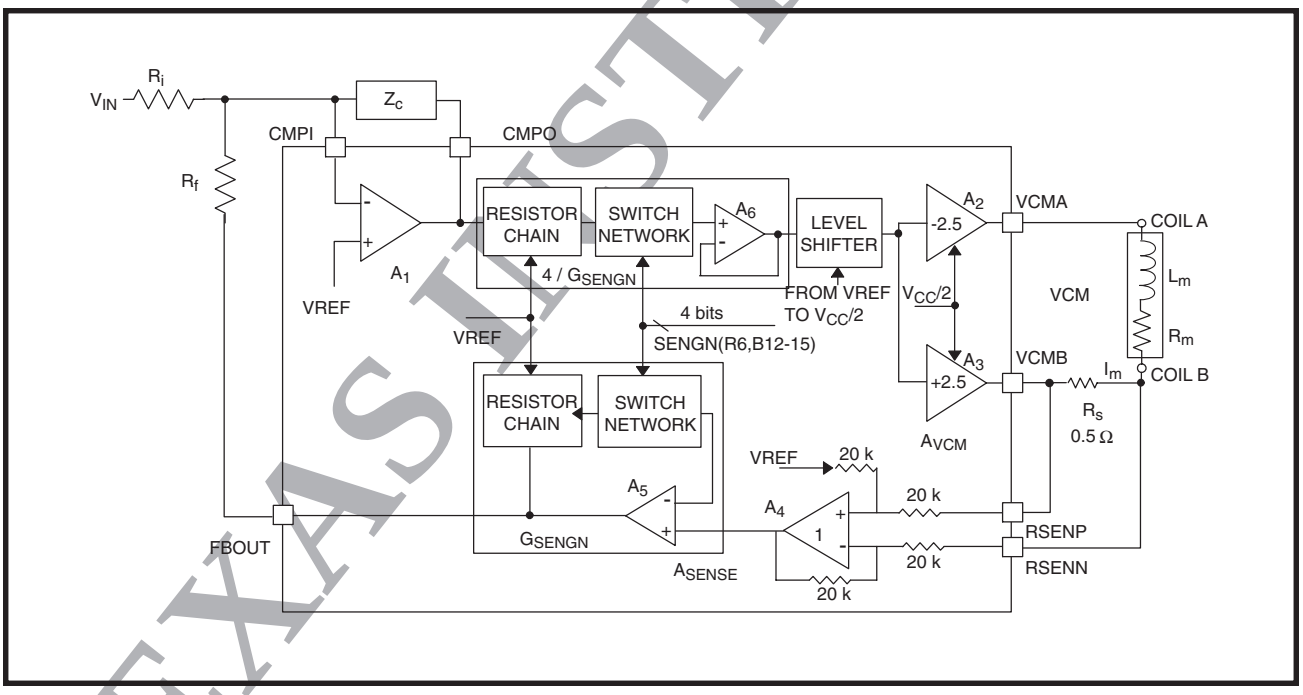


FIGURE 5: VCM Control Circuit

VCM Detailed Description (continued)

The calibration "CAL" mode is activated using the register databits PS0 and PS1. In this mode, the VCM section is disabled while the tracking loop is enabled. The control logic is show in Figure 6.

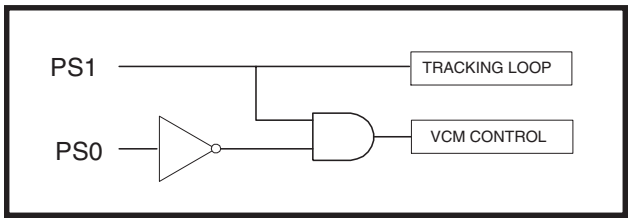


FIGURE 6: Tracking Loop Control Logic

VCM Driver Protection Circuitry

Since the output of the VCM driver is an inductive load, it is necessary to provide active clamp circuitry that limits the signal swing on the output terminals of the VCM driver. There are two sets of clamps—a low-swing and a high-swing clamp—for each of the two outputs. The low swing clamps restrict VCMA and VCMB from swinging below a half of a diode drop below AGND. This protects the junctions tied to the low-side drivers from becoming forward biased. The high-swing clamps restrict VCMA and VCMB from swinging above 6.3 V. This keeps the common-mode input range of RSENP and RSENN within the operating range of amplifier A_4. This also protects the driver devices from being damaged.

Also provided in the VCM driver is active shoot-through protection that prevents both the low-side and high-side drivers of the same output from turning on at the same time. Since the on-resistance of the drivers are so low, this protects the driver devices and eliminates high shoot-through currents that can occur during fast transitions.

RETRACT

Two retract functions are available in this circuit as controlled by the HHB_SEL bit (R2, B11). The first retract function responds to a power fault by retracting the VCM. In the second retract mode, two bits from the serial port can control a half H-bridge that drives an external retract module. Figure 7 is a simplified circuit diagram of the Retract circuit. When HHB_SEL = 0 the purpose of the Retract circuit is to retract and park the read/write heads away from the media when power is turned on or off or when a fault exists. This is accomplished by turning on the Retract and the VCMA Low-Side Drive FETs whenever the RST signal is active. When HHB_SEL = 1, a half H-Bridge is connected to an external retract module. The high and low side drivers are controlled by two bits from the serial port. HHB_HSD (R2, B12) controls the high-side driver FET. HHB_LSD (R2, B13) controls the low_side driver FET. An internal circuit prevents both FETs from being on at the same time if both HHB_LSD and HHB_HSD are set high.

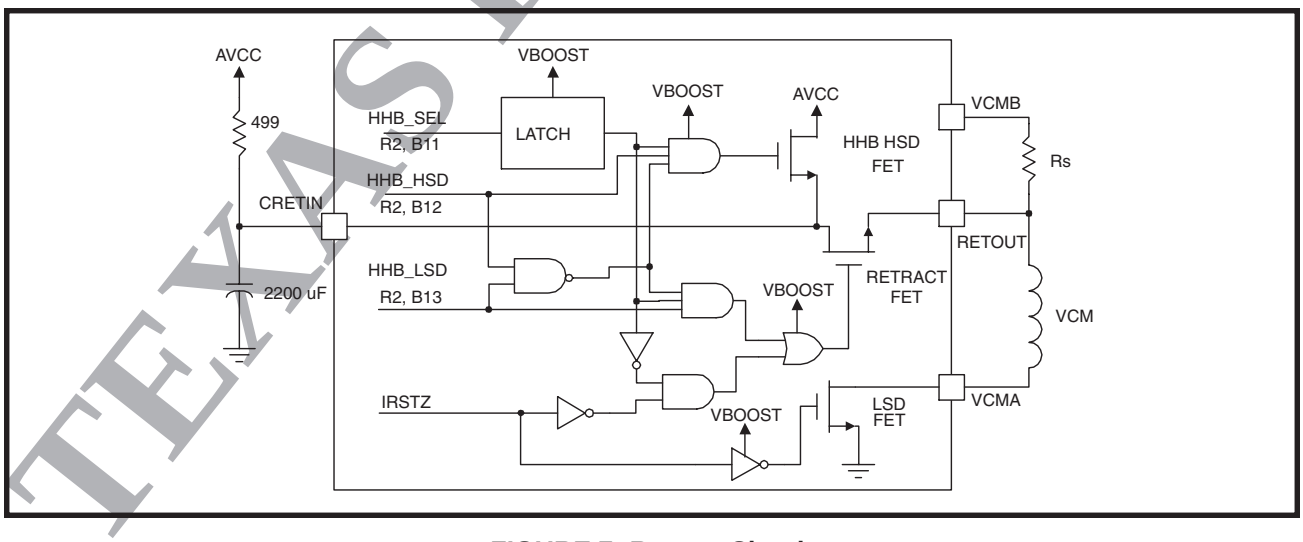


FIGURE 7: Retract Circuit

TRACKING LOOP SUPPORT

The tracking loop supprt provides several functions to facilitate VCM control during tracking. Figure 6 gives a simplified block diagram of these functions. The tracking loop circuit comprises 1) an inverting opamp stage to support an external compensation filter with switches that can be used to enable, disable or change the compensation filter dynamics, 2) a zero order sample and hold, 3) a position error amplifier with 32-level programmable gains in equal steps, and 4) a 16-level threshold window comparator operating in two modes: sign mode and window mode. The tracking loop reference, as in the VCM section, is toggled between VCC/2 and 3.3 V/2 by register 2, bit 10 in the serial port.

The SWITCH pin is used to change the external compensation filter dynamics. With SWITCH open (R5, B14 = 0), an external cap can add a lag function to a filter network. When SWITCH is closed (R5, B14 = 1), the external cap is shorted to VREF, and the lag function is removed from the filter network. The input position error signal (CPES_IN) is sampled by a zero-order sample and hold. The sampled signal is then amplified by opamp A_1 with a programmable gain. The gain is controlled by a switching network and a resistor chain. Finally, the position error signal (CPES_OUT) or the compensated signal (COMP_OUT) is passed through the window comparator.

The window comparator accepts two inputs, CPES_OUT and COMP_OUT, multiplexed by register 5, bit 13. It is programmed from register 6, bits 8-11. If register 6 bits 8-11 are written as zeros (0000) the window comparator operates in sign mode. In sign mode, the window comparator's output is high if its input is above VREF. If its input is below VREF, the window comparator output is low. Figure 9 shows the transfer curve of the window comparator in sign mode. If register 6, bits 8-11 are not all zeros (e.g.; 1010), then the window comparator operates in threshold mode. In threshold mode, the output of the window comparator is high only when its input is outside positive and negative thresholds that are centered at VREF. The window thresholds are symmetrical to the window center point VREF (VCC/2 or 3.3 V/2) and are independent of the power supply voltage since they are derived from the bandgap reference voltage. The value written in bits 8-11 are used for setting positive and negative thresholds. The transfer curves of the window comparator in threshold mode are shown in Figure 10. The SAMPLE pin is 3.3 V or 5 V compatible.

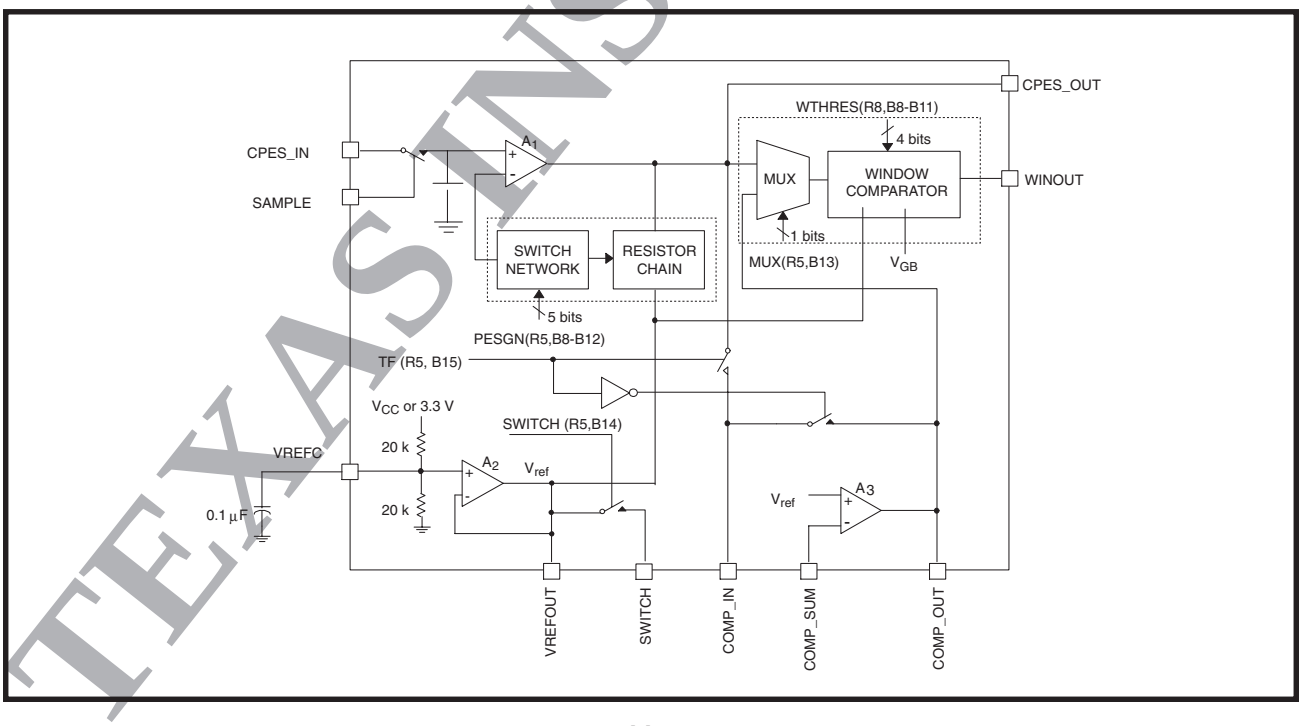


FIGURE 8: Tracking Loop Support

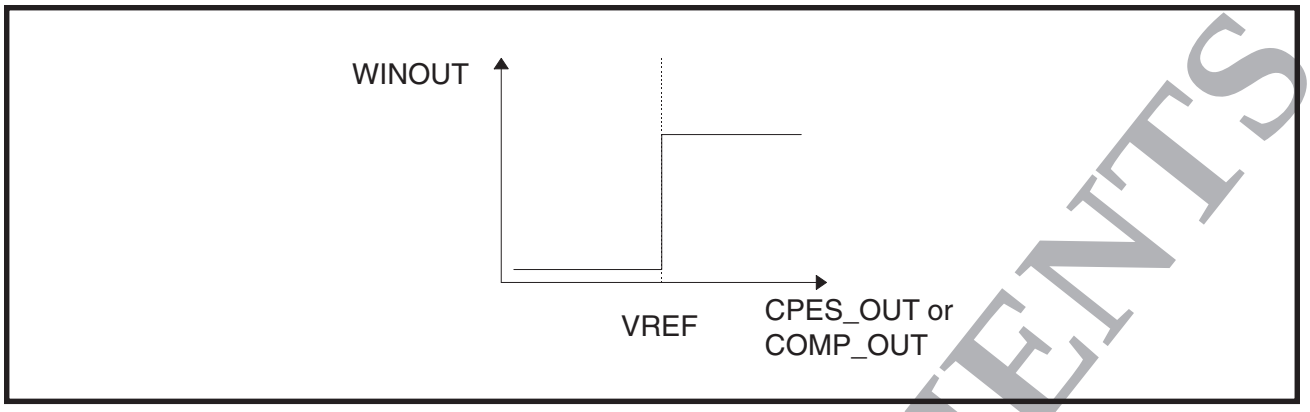


FIGURE 9: Transfer Curve for Sign Mode

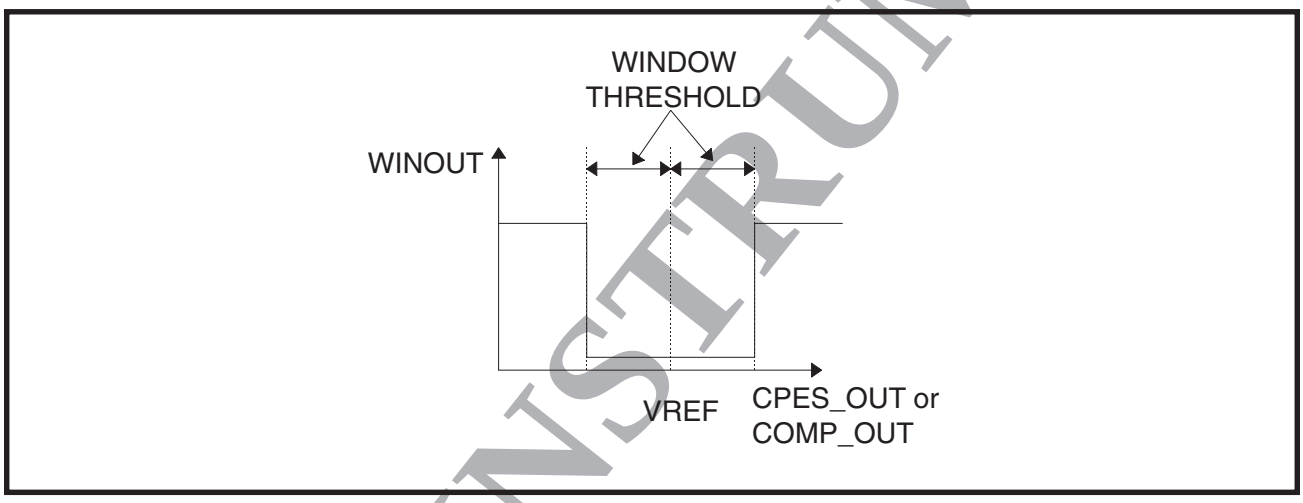


FIGURE 10: Transfer Curve for Threshold Mode

FUNCTIONAL DESCRIPTION (continued)

DUAL WINDOW TIMER

The dual window timer circuit allows for two separate timing measurements. One timing measures the count of the prescaler frequency as an analog input voltage at DWT_IN as it transitions between the two comparator thresholds, DWT_TH_L and DWT_TH_M. The other timing measures the count of the prescalar frequency as an analog input voltage at DWT_IN as it transitions between the two comparator thresholds, DWT_TH_M and DWT_TH_H. The resulting counts are sent to registers that can be read from the serial port. The three thresholds are set by a voltage divider at the DWT_TH_L, DWT_TH_M, and DWT_TH_H pins.

The DWT consists of three comparators and two 15-bit count-up counters. The two counters' (counter 0 and counter 1 in Figure 11) contents and overflow bits can be reset to zero by the DWT_RST bit (R9, B8). As the analog input voltage moves between the thresholds set by DWT_TH_L and DWT_TH_M, the N counter (see Figure 11) is enabled and counts up. As the analog input voltage moves between the thresholds set by DWT_TH_M and DWT_TH_H, the P counter is enabled and counts up. The counters are clocked from the output of the prescaler. If the counter reaches a maximum count of 15 bits, an overflow bit is set to a 1 and the counter will wrap around and continue counting from zero. Once the overflow bit is set it will remain set until the counter is reset. Writing a 1 to DWT_RST (R9, B8) causes either counter 1 or counter 0 to reset to 0. DWT_SEL (R2, B15) selects which counter is reset.

The counter contents can be read back at register 3, B8-B15 and register 4, B8-14. Setting DWT_SEL (R2, B15) = 1 allows the contents of the P counter to be read back through registers 3 and 4. Setting DWT_SEL (R2, B15) = 0 allows the contents of the N counter to be read back through registers 3 and 4. The three comparator outputs can be read back through the serial port to determine where the voltage of the DWT_IN pin lies within the three thresholds during circuit operation.

SPINDLE MOTOR DRIVE

The spindle motor (SPM) drive system controls the spindle/disk assembly in a disk drive. The complete servo system includes three identical power drivers and a pre-drive system. Each power driver is a transconductance amplifier with user selectable gain and slew rate. The pre-drive provides for frequency lock servo control. A state machine controls the motor commutation sequence by means of the EXCOMM bit (register 0, bit 12) in the serial port or by the motor's back EMF (BEMF) zero crossings. The REVR bit in Register 1, bit 14 of the serial port controls whether the commutation runs in forward or reverse. The SPM will be dynamically braked by setting register 0, bit 14 in the serial port. Overtemp and power-on reset do not brake the SPM.

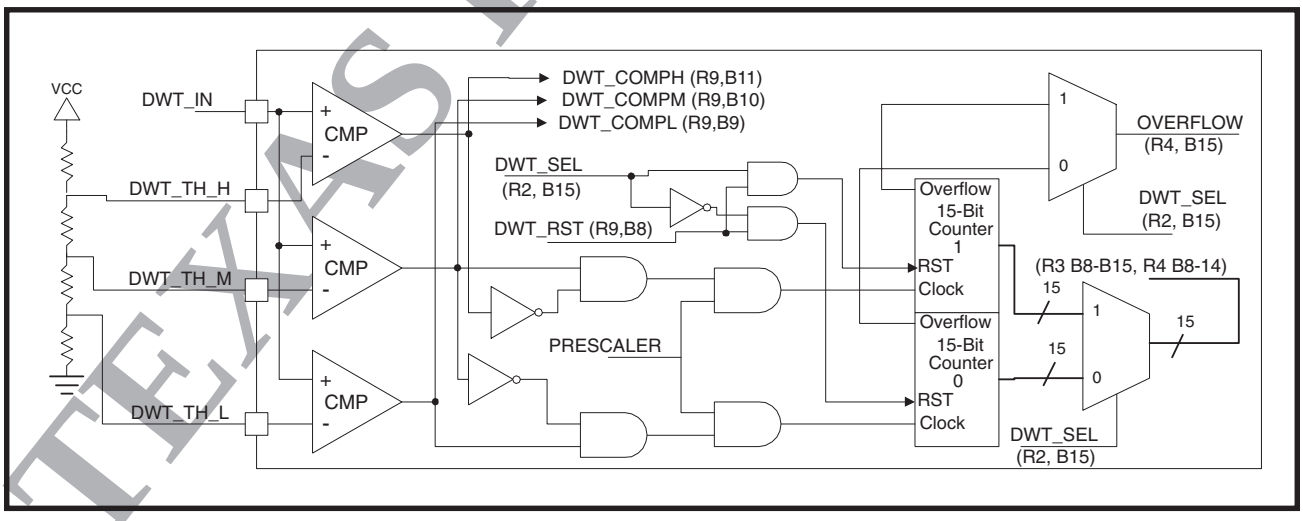


FIGURE 11: Dual Window Timer Circuit

SPINDLE MOTOR DRIVE (continued)

The spindle motor system is a complete frequency lock loop (FLL) speed feedback control system for controlling the speed of a three-phase brushless motor. It consists of two main sections: (1) speed control circuits and (2) phase winding commutation and current slewing circuits. The digital feedback signal, derived either internally from the BEMF zero crossings of the motor or externally from the data written on the disk, is compared to a digital reference signal. The error signal produced is then amplified and applied to the motor. The motor thus accelerates or decelerates until the two frequencies are the same. The power section of the spindle motor system converts the voltage at the SPDCAP to a proportional peak current level in the three spindle motor windings. It also performs the commutation and current slewing that allows the motor to be treated in the system as a simple DC motor. Control of the transconductance gain and slewing rate is programmed through the serial port.

BEMF DETECT CIRCUIT

The BEMF detect circuit measures the voltage on the unexcited motor phase, and compares it to the virtual center-tap voltage. The BEMF detect circuit (Figure 12) consists of a comparator, and three switches.

The state machine knows which phase is the unexcited phase and will assert one of the ZCU, ZCV and ZCW signals to open one of the switches so that the unexcited phase is connected to the non-inverting input of the comparator. The inverting input of the comparator is always connected to the center-tap. The output of the comparator (ZCRS) goes to the spindle state machine. Three 12 kΩ resistors are 'Y' connected between the three phases to emulate a center-tap.

The ZCRS signal thus produced makes a transition for each zero crossing of the BEMF of each of the three motor windings. This is at every 60 electrical degrees of actual motor rotation or $6N_p/2$ transitions per revolution where N_p is the number of motor poles per revolution.

SPINDLE CONTROL LOGIC

The spindle control logic consists of a 12-bit commutation delay counter and a spindle motor (brushless DC) state machine (Figure 13). The commutation delay counter serves a dual purpose of 1) providing commutation delay, and 2) it filters out noise spikes that occur around the commutation point.

The ZCRS signal is either inverted or not inverted by the XOR circuit depending on the POS signal from the state machine. The POS signal is high when a positive going zero crossing of the BEMF is anticipated for starting the delay counter and low when a negative transition is expected.

A low LDZ signal input at the 12-bit counter causes it to be reloaded with the 12-bit phase delay time value at each positive clock edge. The 12-bit phase delay time value is taken from RSD bits 2..13 (R3 B10-B15, R4 B8-B13). When LDZ is high the counter will count until end of count is reached, at which point the EOC signal goes high for one clock cycle. The ZCU, ZCV, and ZCW signals go to the BEMF detect circuit where they will open one of the transmission gates to select the undriven phase prior to when it is expected.

The state machine follows the states indicated in Figure 13 and can be advanced either manually, using the EXCOMM signal (if RUN = 0), or by BEMF zero-crossings, using the COMM (if RUN = 1) signal. Before spin-up it may be desirable to spin the disk in reverse. Reverse commutation is selected through the REVR bit (R1, B14). When reverse commutation is asserted, the state machine starts at state 6 in Figure 13 and runs backwards to state 1.

Assuming a positive transition is expected, and POS is high, the ZCRS signal is then passed unchanged to the LDZ input on the 12-bit counter. As long as the ZCRS signal is low the counter is continually reloaded (with PDT value). At the BEMF zero crossing, the ZCRS goes high and the counter starts counting. Any noise spike on the ZCRS will be ignored since the counter will be reloaded after the noise spike goes away prior to the EOC pulse.

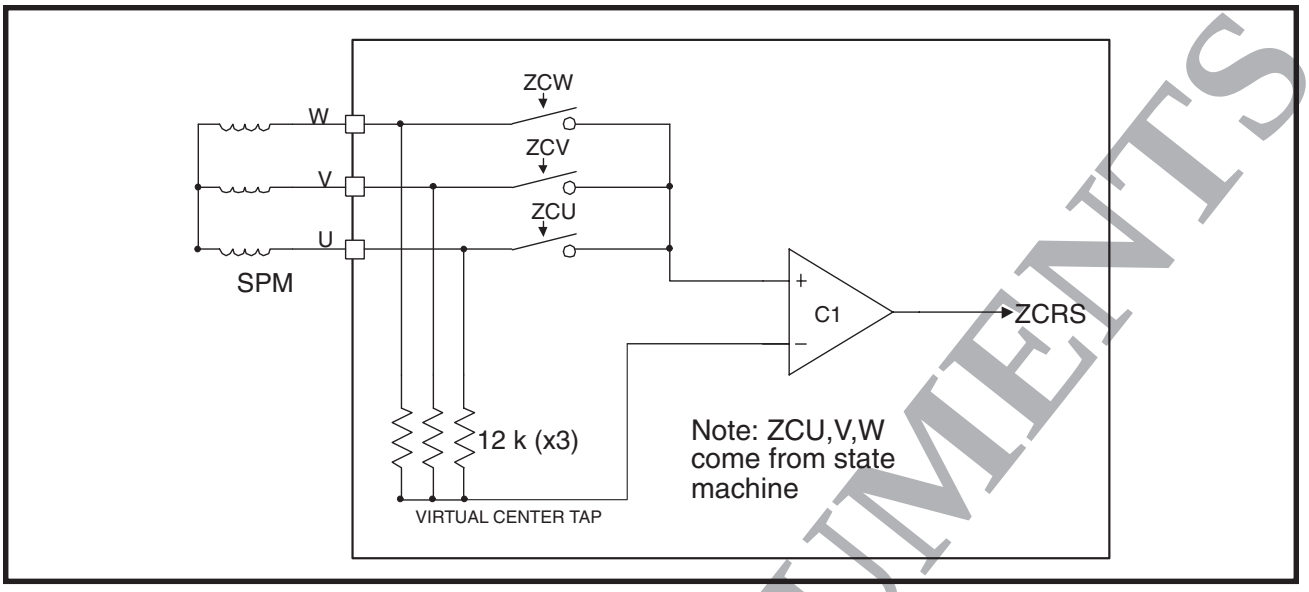


FIGURE 12: BEMF Detect Circuit

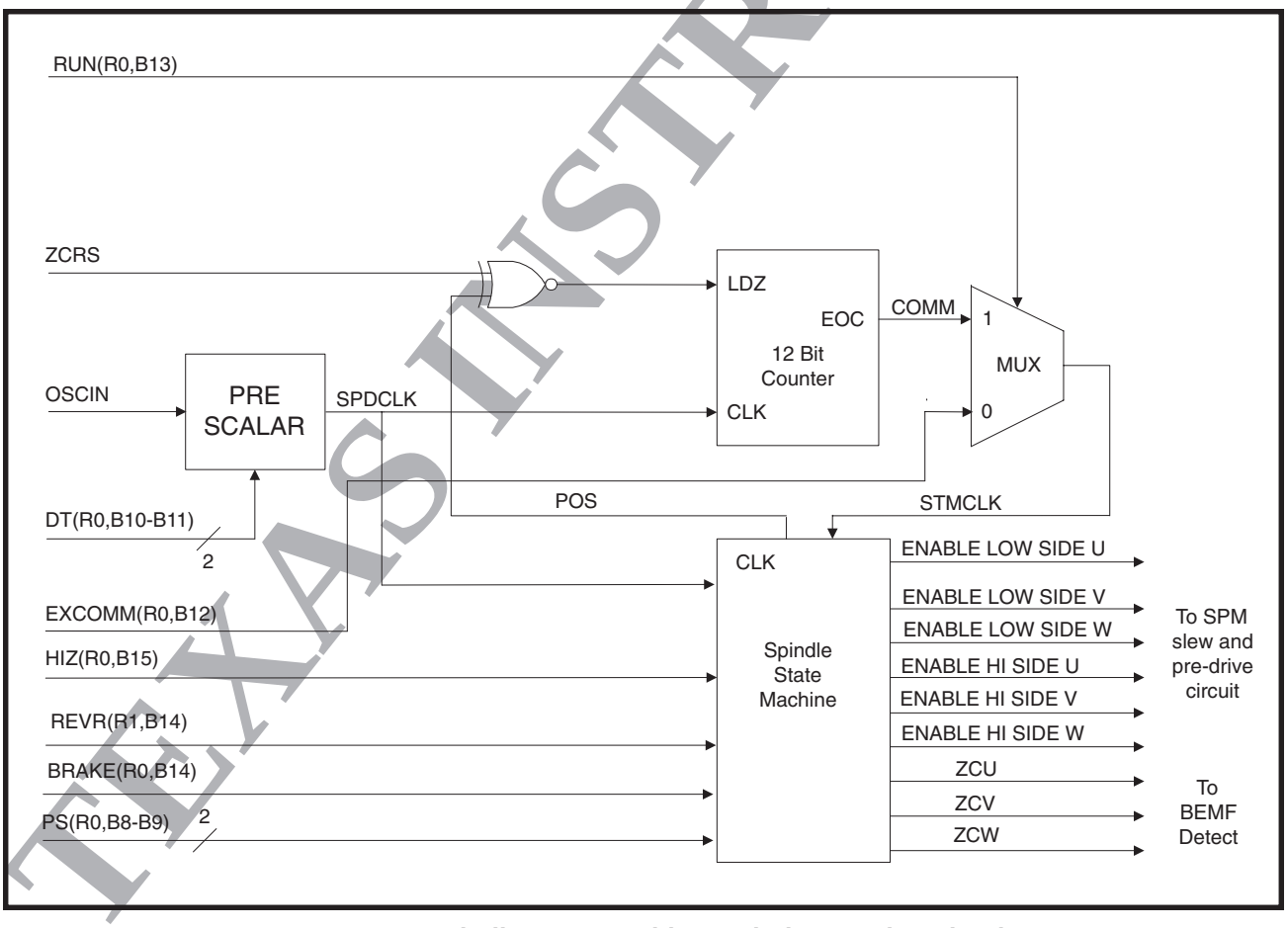


FIGURE 13: Spindle State Machine and Phase Delay Circuit

SPINDLE CONTROL LOGIC (continued)

When a negative BEMF is expected, the POS signal is low and the ZCRS signal is inverted before reaching the LDZ input. In this case the counter will be reloaded when ZCRS is high and allowed to count when it is low.

After PDT clock pulses the counter generates the EOC pulse which advances the state machine causing the outputs to change to the next state.

SPM SERIAL PORT REGISTER CONTROL BITS

Register 0 (see the Spindle Control Logic section)

PS0 = X and PS1 = 1: Enables the spindle drivers and enables the state machine.

PS0 = X and PS1 = 0: Disables the spindle drivers and resets the state machine.

RUN = 0: Selects manual/forced commutation using EXCOMM.

RUN = 1: Selects hardware (automatic) state machine advance using the BEMF.

EXCOMM: Manually advances the state machine on positive going edge if RUN = 0, PS0 = 1, PS1 = 1.

BRAKE = 1: Quickly brakes the motor by enabling all three low-side drivers and disabling all high-side drivers if PS0 and PS1 are high.

HIZ = 1: Disables spindle drivers without resetting state machine if PS0 = 1 and PS1 = 1. U, V, and W pins go to a high impedance state which allows verification of rotation after manually commutating the motor. The state machine continues to advance and select the inactive phase for BEMF monitoring.

MANUAL (SOFTWARE) COMMUTATION MODE

In manual commutation mode the state machine is advanced by each positive transition of the EXCOMM bit in serial register 0.

To manually commutate the state machine:

Write RUN = 0

Write EXCOMM = 0

Write PS0 = 1, PS1 = 1

Write EXCOMM = 1 (State machine advances)

Write EXCOMM = 0

Write EXCOMM = 1 (State machine advances)

Once the RUN bit is set high the state machine will advance automatically using the BEMF detect and delay circuit.

TABLE 1: State Machine Outputs

DESCRIPTION	STATE #	CURRENT DIRECTION	HIGHSIDE U	LOWSIDE U	HIGHSIDE V	LOWSIDE V	HIGHSIDE W	LOWSIDE W
Basic	1	U-V	ON	OFF	OFF	ON	OFF	OFF
Commutation	2	U-W	ON	OFF	OFF	OFF	OFF	ON
PS0 = X	3	V-W	OFF	OFF	ON	OFF	OFF	ON
PS1 = 1.	4	V-U	OFF	ON	ON	OFF	OFF	OFF
	5	W-U	OFF	ON	OFF	OFF	ON	OFF
	6	W-V	OFF	OFF	OFF	ON	ON	OFF
HIZ = 1	1-6	NA	OFF	OFF	OFF	OFF	OFF	OFF
BRAKE = 1	1-6	NA	OFF	ON	OFF	ON	OFF	ON
Sleep and Standby	0	NA	OFF	OFF	OFF	OFF	OFF	OFF

Note: POS level corresponds to state.

SPINDLE MOTOR CURRENT CONTROL AND COMMUTATION CIRCUITS

This system controls the amplitude and coil current slew rate in a three phase disk drive motor by controlling two phases while in steady state control and all three phases during commutations. Three sense FETs and six drivers (three pair of half H-bridges) are used to sense and control the steady state current through the coils, and control the current slew rate during commutations. The amplitude of the coil current is controlled by the low side drivers which operate in the MOS saturation region unless they are commutating or turned off. The high side drivers operate in the linear (resistive) region with their gates pulled to 5 V above the positive rail, unless they are commutating or turned off. Active clamp circuits limit the output voltage of the three amplifiers to 6.3 V.

A functional diagram of the SPM current control (neglecting commutation) is shown in Figure 14. The input voltage is either from the FLL or the 3-bit DAC, controlled by the RUN bit (R0, B13). The amplitude of the SPM coil currents is controlled by current mirror amplification. The voltage at the SPDCAP pin (or DAC), which can vary between 1 and 3 volts, is first level shifted to vary between 0 and 2 volts at the RSS pin. The external resistance at this pin determines the current into the current mirror which is amplified by either high or low gain as controlled by the serial register SPMG bit in register 1. This resistor thus sets the transconductance gain of the amplifier and current limits to the motor. With proper commutation the motor torque is directly proportional to this current level or:

$$T = K_t I_m \qquad \text{(Equation 2)}$$

the same as for a dc motor. Where K_t is the motor torque constant and I_m is the amplitude of the commutating current into each phase of the motor.

The commutating current slew rate is controlled by applying a constant dV/dt to the two motor phases that are turning off. The BEMF over a small region, close to the zero crossing, can also be approximated as a constant dV/dt, so the difference between the BEMF voltage and the phase voltage is approximately a constant voltage. This constant voltage is the voltage between the phase turning off and the center tap of the motor, or the voltage across the inductive part of the winding. A constant voltage across the motor winding (v = LdI/dt) causes a constant dI/dt or current slew rate in that winding. The purpose of controlling the slew rate of the commutating current is to limit the audible noise from the motor caused by this switching current.

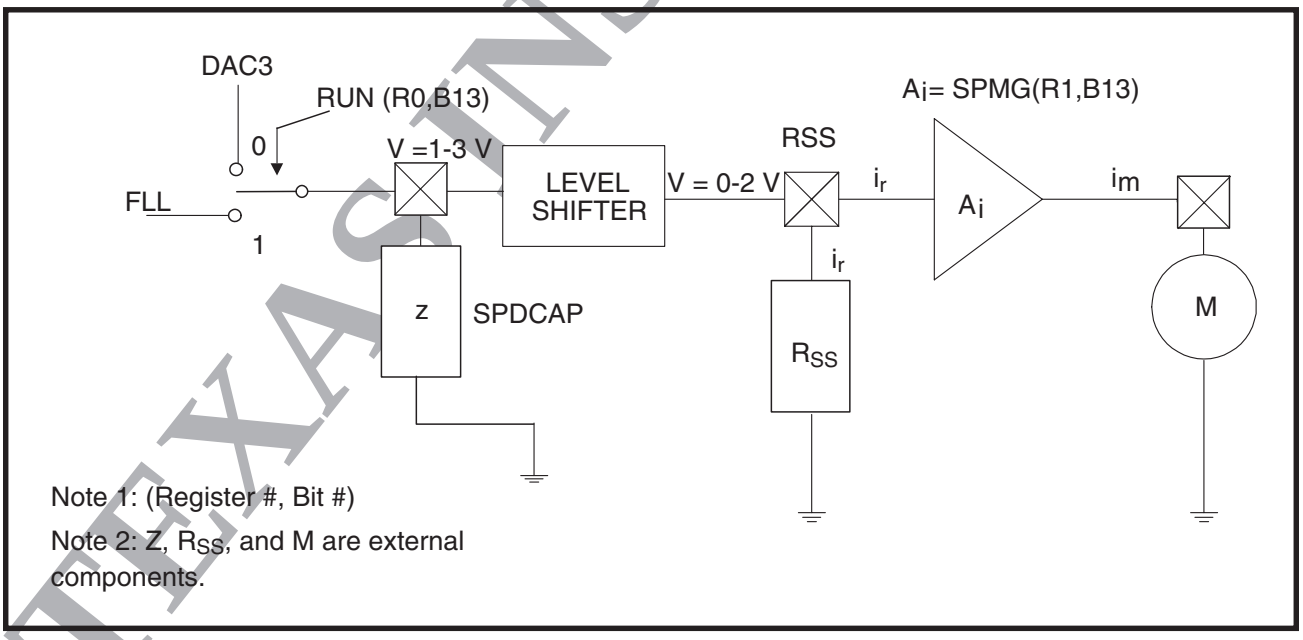


FIGURE 14: SPM Current Control

FUNCTIONAL DESRIPTION (continued)

FLL SPM SPEED CONTROL CIRCUIT

The speed control circuit for the SSI 34H3307 is shown functionally in Figure 15. It Consists of charge and discharge current sources that feed the external network connected to the SPDCAP pin, two sets of identical circuits consisting of a velocity (frequency) comparator and a 15-bit preset counter, and a rotational signal generator.

Each comparator-counter pair controls the current sources for half the time period as determined by the timing signals from the Rotation Signal Generator. Since the voltage on the SPDCAP pin sets the desired output current level of the spindle motor pre-drive and control circuit, the FLL circuit controls the motor's torque, thus controlling the motor's speed.

Both counters in the FLL are programmed with the count value from the RSD (Rotational Speed Data) value in registers 7 and 8. They then count down from this value to zero. The count that should be programmed into the counters (RSD) is the number of speed clock cycles in the time taken for the motor to rotate 120° electrical at the desired speed (RPM). It can be calculated as follows:

$$T_{120^\circ} = (60 / RPM) \bullet (2 / N_p) \bullet (120^\circ / 360^\circ)$$
$$= 40 / (RPM \bullet N_p)$$

(Equation 3)

$$RSD = T_{120^\circ} \bullet (f_{oscin} / PRESCALE)$$

(Equation 4)

where N_p is the number of motor poles and PRESCALE is the programmed prescaler division ratio.

The FLL counters are setup as two digital one-shot delays triggered by commutation in a way that will speed lock the motor. Each counter is triggered by the beginning of separate 120° electrical periods of actual motor rotation. The feedback control loop tries to make each of the 120° motor periods equal to the corresponding counter (one shot) periods. See Figure 16 and the Frequency Comparator section for more details.

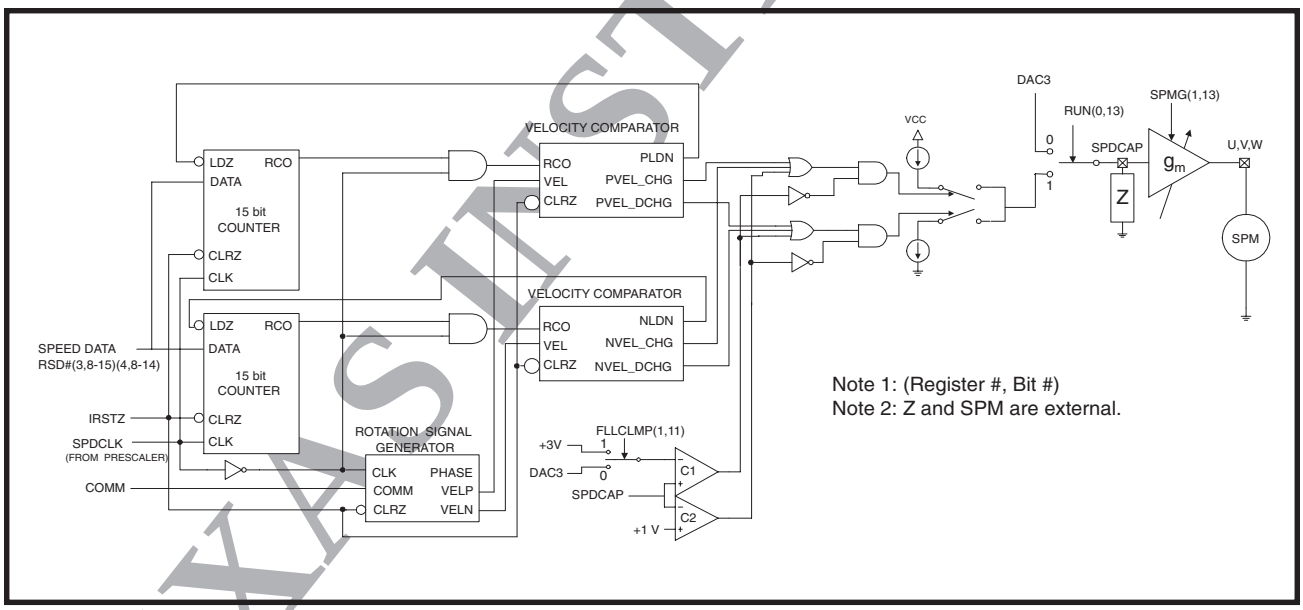


FIGURE 15: FLL Circuit

SPDMECH/SPDTACH PIN

This pin has 2 multiplexed signals, SPDMECH or SPDTACH. The selection is done with the TACH bit (R1, B15). When TACH = 1, the pin is the SPDMECH index signal. It is a 50% duty cycle square wave with a period of once per commutation, once per 24 commutations, or once per 60 commutations as set by register 2, bits 9 and 10. When TACH = 1, the COMM signal, described in the Spindle Control Logic section, is connected to the FLL circuits as shown in Figure 15. The normal mode of operation of the FLL and Speed Error circuit, that uses the delayed BEMF zero crossings to measure the motor speed, requires that TACH is set to 1.

If the TACH bit = 0, the SPDTACH pin is an input signal which is connected in place of the COMM signal in Figure 15. This mode can be used where it is desirable to use speed information from the disk sector data rather than from the BEMF. The waveform applied to the SPDTACH pin should have a positive edge for every 60° electrical of actual rotor rotation ($6N_p/2$ pulses per rev).

SPDCAP VOLTAGE CLAMP

The voltage on SPDCAP is effectively limited to from 1 V to 3 V by the comparator circuits, C1 and C2, in Figure 15. If either limit is reached the corresponding comparator output goes high which disconnects the current source connected to SPDCAP that is causing the problem and forces the opposite polarity current source to be on.

When FLLCLMP is low during startup, the DAC is used as the C1 limit voltage instead of the 3 volt reference. This indirectly sets the SPDCAP voltage since the speed control is limiting during acceleration. However, since RUN (R0, B13) is low at this time, the SPDCAP is not connected to the motor drive control. Instead, the RUN signal connects the 3-bit DAC to control the motor current. When the motor is close to operating speed, the RUN signal is set high connecting the SPDCAP to the motor drive control which allows the speed control to operate the motor. Since the 3-bit DAC is still connected to the limit circuit it can be used in a way that limits speed overshoot. Once the motor speed is stabilized, FLLCLMP is set high, which switches the DAC from the SPM limit circuit to the VCM where it is used as an offset compensation. The SPM current limit is now set to the maximum current for the selected range by the 3 volt reference.

FREQUENCY COMPARATOR

A typical frequency comparator timing diagram is shown in Figure 16. The frequency control circuit in Figure 15 consists of two identical frequency (velocity) comparator (or detector) circuits. They compare the frequency of two input signals, f_{ref} and f_{fb}. The output is ideally proportional to the difference. The update rate for each of the frequency comparator circuits is once every 240° electrical degrees of motor rotation and the current output of each is summed at the SPDCAP pin. The total output over the full 240° period is thus twice the output of one of the frequency detectors or, in other words, the overall detector gain is twice the gain of one detector over the 240° period.

The two frequency comparator circuits work on different 120° halves of the 240° cycle as determined by the complimentary VELP and VELN signals derived from the COMM motor feedback signal. The frequency of these two signals is one fourth the frequency of the COMM signal and 180° out of phase with each other. So another way to look at the system is that each detector is trying to control its corresponding half period of the feedback signal. And this is the same as saying the overall detector gain is equal to either detector gain over a 120° period. This makes the effective update rate twice per 240° period which is equivalent to once per 120° period.

Since the two frequency comparators are identical only the one connected to VELN signal, the bottom circuit in Figure 15, is described in detail. The VELP signal is just the compliment of the VELN signal so that everything for the other circuit is the same but shifted by 120°.

Each frequency comparator circuit consists of a single 15-bit counter and a velocity comparator circuit. The VELN signal is the 'COMM' (motor commutation signal) divided by 4 which means that it goes high on every fourth COMM pulse. This represents the feedback motor speed in terms of frequency. The pulse width of the VELN signal is thus equivalent to the rotor moving 120° electrical or the full period is 240° electrical. The count length of the 15-bit counter is programmed (by RSD) to be equivalent to the time for a 120° electrical of desired rotor movement.

FREQUENCY COMPARATOR (continued)

Once the velocity comparator circuit receives a positive going edge on VELN, the counter is started and at the same time it sets the NLDZ flop. The counter produces an end of count signal (RCO) after a fixed time equivalent to the desired 120° electrical period which resets the NLDZ flop. The NLDZ signal can be looked at as a digital, fixed period, one-shot triggered on every fourth COMM pulse. This is the feedback signal into the frequency detector. It is easily shown that the average dc level of this signal is proportional to its frequency which is proportional to the motor speed. Since this signal is one of the inputs to the phase detector which controls the current source of value I_{cs} connected to the SPDCAP pin, its amplitude is effectively I_{cs}.

The resulting average current into the SPDCAP pin due to the feedback signal alone is:

$$(I_{dc})f_b = I_{cs} \bullet T_{ref}/t_{fb} = I_{cs} \bullet T_{ref} \bullet f_{fb} = (I_{cs}/f_{ref})\, f_{fb}$$

(Equation 5)

Where I_{dc} is the average NLDZ signal of amplitude I_{cs}, T_{ref} is the constant time period of 120° electrical, and f_{fb} is the feedback frequency from the motor.

The net current into the SPDCAP pin is the sum of this current and that due to the reference signal.

The two signals, N_VEL_CHG and N_VEL_DCHG, control the connection of the corresponding charge and discharge current source to the SPDCAP pin. These signals are FF outputs. The CHG FF is set when the trailing (negative) edge of the VELN signal lags the trailing edge of the NLDZ signal and the DCHG FF is set when the trailing edge of the VELN signal leads the trailing edge of the NLDZ signal. Thus it is seen that the CHG FF is set when the feedback frequency is low (slow) and the DCHG FF is set when the feedback frequency is high (fast). Since the peak motor current (and torque) is directly proportional to the voltage at the SPDCAP pin, the CHG FF tries to speed up the motor and the DCHG FF tries to slow it down.

Both flip flops are reset whenever both are set simultaneously. This means that when one is set first it resets as soon as the other one tries to set.

If the motor is running at the correct speed, the negative edges of the VELN and NLDZ signals coincide and each FF sets at the same time and immediately resets.

The other velocity compare circuit functions the same way on the positive half of the VELP signal which is the same as the negative half of the VELN signal. P_VEL_CHG and P_VEL_DCHG are generated that tend, respectively, to speed up and slow down the spindle motor. So it is seen that each half of the 240° feedback signal (VELN or VELP) is controlled separately by the 120° reference pulse of the counter such that they are equal to 120° electrical of motor rotation at the commanded speed.

It can be shown that the average value of each frequency detector output is proportional to the difference between the reference frequency ($1/T_{ref}$) and the feedback frequency. In this case the feedback frequency period is 120° electrical or half the period of the VELN or VELP signals..

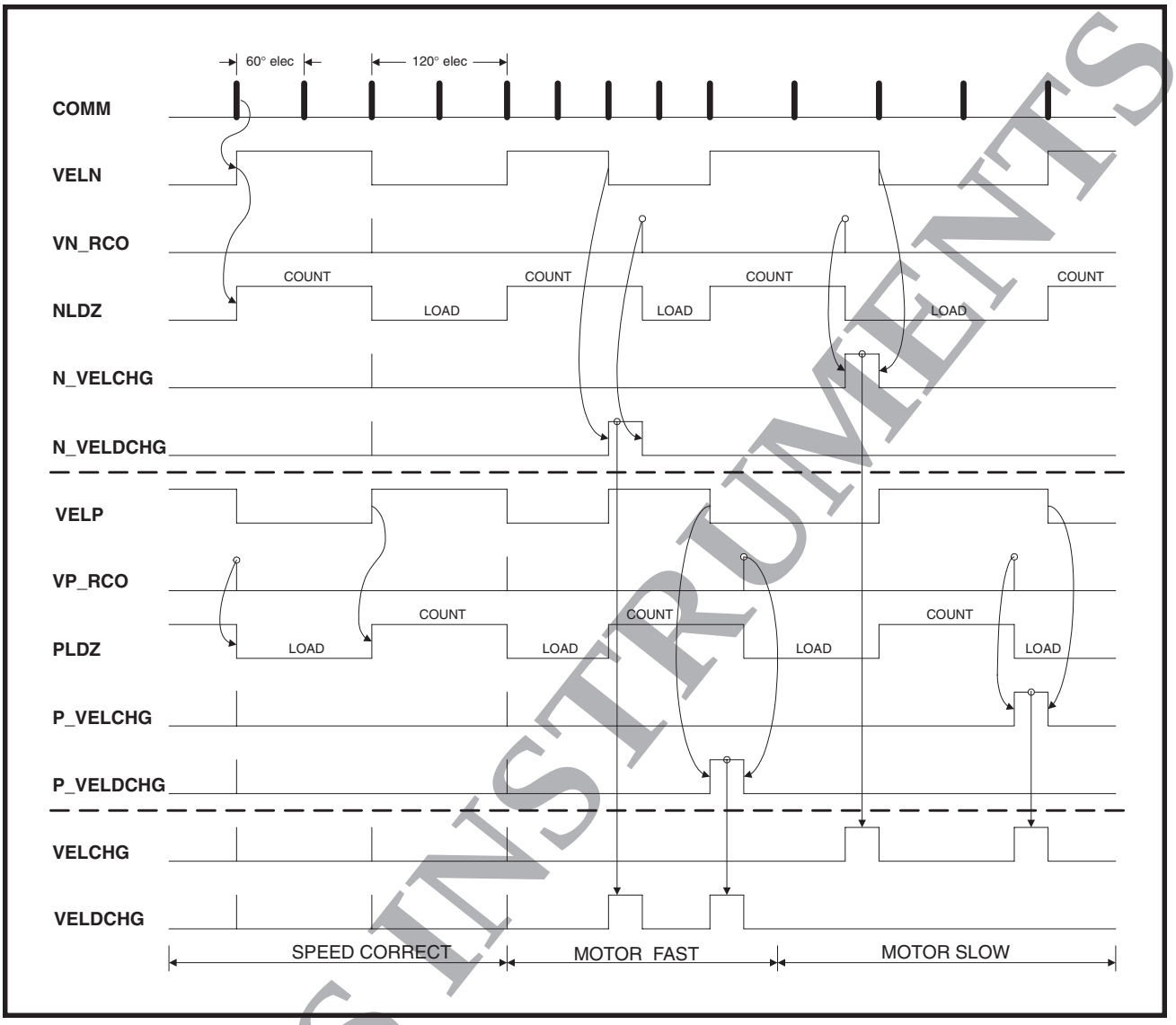


FIGURE 16: Frequency Comparator Timing

FUNCTIONAL DESRIPTION (continued)

FREQUENCY COMPARATOR GAIN FACTOR

The gain function of the frequency detector block (average DC current output per cycle of frequency difference) is:

$$G_{fd} = I_{cs}/f_{ref} = I_{cs}\, T_{ref} \text{ in amps per Hz} \quad \text{(Equation 6)}$$

I_{cs} is the current source programmed to the SPDCAP pin, and T_{ref} is $T_{120°}$ given in Equation 5.

G_{fd} is defined by:

$$I_{dc}\,(A) = G_{fd}(f_{ref} - f_{fb}) \quad \text{(Equation 7)}$$

I_{dc} is the average dc current at the SPDCAP pin.

SPDCAP PIN COMPENSATION NETWORK

A true frequency locked loop speed control with no average frequency error has an integrator in the forward loop. This is done with a lead-lag network consisting of one resistor and two capacitors at the SPDCAP pin as in Figure 17.

Since the SPDCAP pin is fed from a current source the transfer function of current to voltage is just the complex impedance to ground which is also given in Figure 17. Normally this network is designed to make the overall open loop transfer function cross the zero db point at the desired loop bandwidth and to cross at a slope of 20 dB/decade. The two break frequencies of the network are normally chosen such that the zero db point Is at the geometric mean of the two and the ratio of f_2 to f_1 is about 10. This usually will result in enough phase margin for a stable system but other performance factors may need to be considered. Since this system is actually a sampled data system, one criteria for the closed loop band width is that it should be at most 1/5 of the sampling rate to avoid excessive sampled data lag. This allows the system to be treated as a linear system.

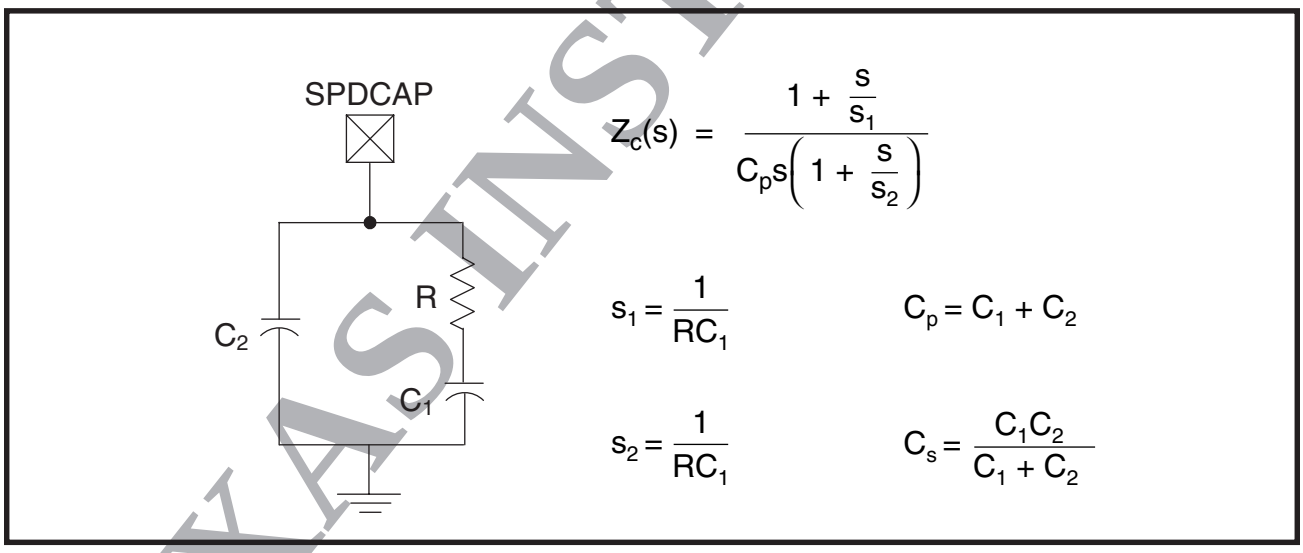


FIGURE 17: Lead-Lag Compensation Network

SPEED CONTROL SERVO LOOP BLOCK

An overall speed control system block diagram is shown in Figure 18. The reference frequency, f_{ref}, is $1/T_{120}$ given in Equation 3. G_{fd} is the frequency discriminator gain factor and is given in the Frequency Comparator Gain Factor section. The motor transfer function, G_m, can usually be simplified to K_t / Js when the viscous damping constant, K_d, is small. $Z_c(s)$ is the compensation network connected to the SPDCAP pin as discussed in the SPDCAP Pin Compensation Network section. R_{ss} is the resistor connected to the RSS pin which is 2 k for nominal output current ranges. The power amplifier current gain, G_a, is selectable through the serial port as either 375 or 1500. The lower gain corresponding to the 375 mA output current range is sufficient for most HDD motors.The generalized open loop gain is given in Figure 18.

The open loop transfer function for this system using a compensation network as in the SPDCAP Pin Compensation Network section is:

$$GH(s) = K\frac{1 + \frac{s}{s_1}}{s^2\left(1 + \frac{s}{s_2}\right)} \qquad K = \frac{30\, G_a K_t I_{cs}}{\pi (RPM) R_{ss} J Cp}$$

$$s_1 = \frac{1}{RC_1},\ C_p = C_1 + C_2 \qquad s_2 = \frac{1}{RC_s},\ C_s = \frac{C_1 C_2}{C_1 + C_2}$$

(Equation 8)

For these equations K_t is the motor torque constant in Nm/A, J_L is the load moment of inertia in Kgm^2, G_a is the programmed power amplifier current gain and I_{cs} is the programmed charge and discharge current which are assumed equal.

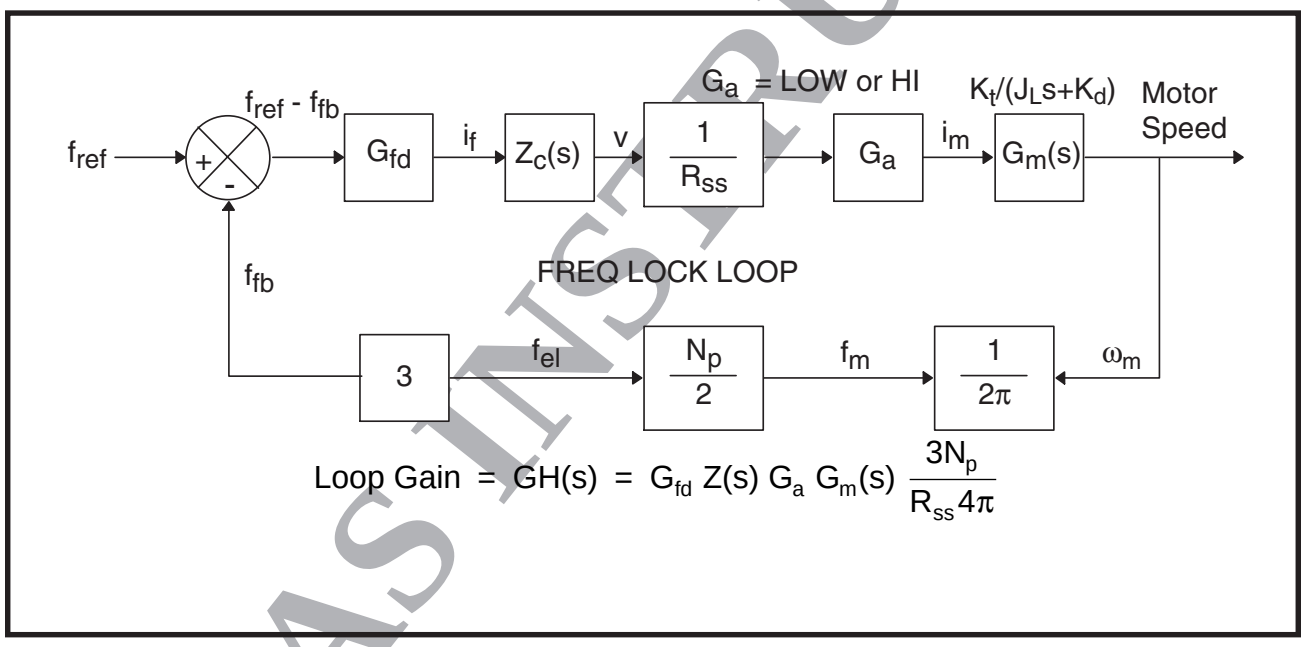


FIGURE 18: Speed Control Block Diagram

REGISTER DESCRIPTION

REGISTER 0:POWER MANAGMENT AND SPINDLE MODE CONTROL
(ADDRESS : A3..A0 = 0000, DEVICE ID: DID2..DID0 = 111)

BIT	NAME	DESCRIPTION
8	PS0	PS0 and PS1 are two bits used for power management mode settings
9	PS1	See Table 2 for mode definitions
10	DT0	Two bits for system clock prescaler. Incoming clock is 16 - 40 MHz
11	DT1	See Table 3 for prescaler ratios
12	EXCOMM	External commutation during start-up
13	RUN	0: start-up using EXCOMM to advance commutation 1: during run, using Back-EMF event for commutation
14	BRAKE	SPM brake
15	HIZ	SPM drivers in Hi-Z state

TABLE 2: POWER MANAGEMENT MODES

PS1	PS0	Mode	VCM	TRK	SPM	DWT	PRESCALER	VBOOST
0	0	Sleep	Off	Off	Off	Off	Off	Off
0	1	Standby	Off	Off	Off	Off	On	On
1	1	Active	On	On	On	On	On	On
1	0	Calibrate	Off	On	On	On	On	On

NOTE: Registers are not reset in the standby mode. Registers are reset by the power-on-reset circuit during power up or after recovery from a power fault. See the Power Management Modes section for further details on the SSI 34H3307 power management modes.

TABLE 3: PRESCALER RATIOS

DT1	DT0	PRESCALER RATIO
0	0	1
1	0	2
0	1	4
1	1	8

REGISTER 1:SPINDLE FLL CONTROL
(ADDRESS : A3..A0 = 0000, DEVICE ID: DID2..DID0 = 111)

BIT	NAME	DESCRIPTION
8	SPMDAC0	Three bits for spindle motor dac settings. DAC range is from 1 V to 3 V (typical)
9	SPMDAC1	Three bits for spindle motor dac settings. DAC range is from 1 V to 3 V (typical)
10	SPMDAC2	Three bits for spindle motor dac settings. DAC range is from 1 V to 3 V (typical)
11	FLLCLMP	0: 3-bit DAC is used to set the limit of comparator C1 in Figure 3 1: 3 V is used to as the limit of comparator C1 in Figure 3
12	FLTBEMF	0: The signal at SPDMECH/SPDTACH is the BEMF zero crossing without extra filtering. 1: The signal at SPDMECH/SPDTACH is the BEMF zero crossing with extra filtering. NOTE: This function is only effective during SPM startup
13	SPMG	Transconductance gain select. 0: Low gain: I_{OUT} / I_{RSS} = 475 (typ) 1: High gain: I_{OUT} / I_{RSS} = 1900 (typ)
14	REVR	Select forward or backward commutation sequences 0: Forward 1: Reverse
15	TACH	SPDTACH Pin I/O Select: 0: SPDTACH pin is an output connected to the SPDMECH signal 1: SPDTACH pin is an input and is connected to the FLL in place of the internal COMM signal. (see the SPDMECH/SPDTACH Pin section)

REGISTER DESCRIPTION (continued)

REGISTER 2: SPINDLE SLEW RATE AND TEST CONTROL
(ADDRESS : A3..A0 = 0010, DEVICE ID: DID2..DID0 = 111)

BIT	NAME	DESCRIPTION
8	SPDMECH	Select multiplexed tachometer ouput 0: every commutation/2; each commutation causes a change of state in this signal 1: divided as set in the MECH bit
9	MECH	Mechanical revolution control 0: divide by 24 1: divide by 60
10	VREFSEL	0: VREF = VCC / 2 1: VREF = 3.3 V / 2
11	HHB_SEL	0: Retract circuit is set to retract and park the read/write heads 1: Retract circuit is used to control an external retract module
12	HHB_HSD	0: Retract circuit high-side driver FET is disabled 1: Retract circuit high-side driver FET is enabled
13	HHB_LSD	0: Retract circuit low-side driver FET is disabled 1: Retract circuit low-side driver FET is enabled
14	RSD_SEL	0: Dual window timer counters contents (either P or N depending on R2, B15) can be read back through the RSD registers 1: RSD Register contents are read back from the RSD Registers
15	DWT_SEL	0: Dual window timer counter 0 1: Dual window timer counter 1

REGISTER 3: SPINDLE ROTATION SPEED DATA LSBS
(ADDRESS : A3..A0 = 0011, DEVICE ID: DID2..DID0 = 111)

BIT	NAME	DESCRIPTION
8	RSD0	Spindle Rotation Speed Data 8-bit LSBs: RSD0..RSD7.
9	RSD1	
10	RSD2	
11	RSD3	
12	RSD4	
13	RSD5	
14	RSD6	
15	RSD7	
NOTE: During read back and with R2, B14 = 0, Register 3 looks like this:		
8	COUNT0	DWT Counter LSBs
9	COUNT1	
10	COUNT2	
11	COUNT3	
12	COUNT4	
13	COUNT5	
14	COUNT6	
15	COUNT7	

REGISTER DESCRIPTION (continued)

REGISTER 4: SPINDLE ROTATION SPEED DATA MSBS

(ADDRESS : A3..A0 = 0100, DEVICE ID: DID2..DID0 = 111)

BIT	NAME	DESCRIPTION
8	RSD8	Spindle Rotation Speed Data 7-bit MSBs: RSD8..RSD14.
9	RSD9	
10	RSD10	
11	RSD11	
12	RSD12	
13	RSD13	
14	RSD14	
15		
NOTE: During read back and with R2, B14 = 0, Register 4 looks like this:		
8	COUNT8	DWT Counter MSBs
9	COUNT9	
10	COUNT10	
11	COUNT11	
12	COUNT12	
13	COUNT13	
14	COUNT14	
15	OVERFLOW	DWT Counter Overflow Bit

REGISTER 5: TRACKING LOOP SUPPORT

(ADDRESS : A3..A0 = 0101, DEVICE ID: DID2..DID0 = 111)

8	PESGN0	PES amp programmable gain bits 0..4
9	PESGN1	
10	PESGN2	
11	PESGN3	
12	PESGN4	
13	MUX	Input to MUX is: 1: CPES_OUT 0: COMP_OUT
14	SWITCH	Compensator switch control 0: Switch open, external cap creates lag function 1: Switch closed, external cap shorted, removes lag function
15	TF	Track following control 0: Connects COMP_IN to COMP_OUT 1: Connects CPES_OUT to COMP_IN

REGISTER 6: WINDOW COMPARATOR
(ADDRESS : A3..A0 = 0110, DEVICE ID: DID2..DID0 = 111)

BIT	NAME	DESCRIPTION
8	WTHRES0	Programmable window threshold
9	WTHRES1	
10	WTHRES2	
11	WTHRES3	
12	SENGN0	Sense amplifier programmable gain
13	SENGN1	
14	SENGN2	
15	SENGN3	

REGISTER 7: TI RESERVED REGISTER 1
(ADDRESS : A3..A0 = 0111, DEVICE ID: DID2..DID0 = 111)

8	TI0	TI reserved bits [0..7] used for trim
9	TI1	
10	TI2	
11	TI3	
12	TI4	
13	TI5	
14	TI6	
15	TI7	

REGISTER 8: TI RESERVED REGISTER 2
(ADDRESS : A3..A0 = 1000, DEVICE ID: DID2..DID0 = 111)

8	TI8	TI reserved bits [8..15] used for trim
9	TI9	
10	TI10	
11	TI11	
12	TI12	
13	TI13	
14	TI14	
15	TI15	

REGISTER DESCRIPTION (continued)

REGISTER 9: LED/DWT
(ADDRESS : A3..A0 = 1001, DEVICE ID: DID2..DID0 = 111)

BIT	NAME	DESCRIPTION
8	DWT_RST	Bit to reset DWT counters. Writing a 1 resets the DWT counters to zero, writing a 0 has no effect on the DWT counters.
9	DWT_COMPL	Output of the DWT low comparator
10	DWT_COMPM	Output of the DWT med comparator
11	DWT_COMPH	Output of the DWT high comparator
12	LED1	0: LED1 driver is off 1: LED1 driver is on
13	LED2	0: LED1 driver is off 1: LED1 driver is on
14		
15		

REGISTER 10: TESTMUX
(ADDRESS : A3..A0 = 1010, DEVICE ID: DID2..DID0 = 111)

8	TEST0	TEST MUX BITS WARNING: Writing to this register could adversely affect the functionality of the SPDMECH/SPDTACH pin.
9	TEST1	
10	TEST2	
11	TEST3	
12	SPM_STRESS	
13	SPM_GIN	
14	WIN_TEST	
15		

TABLE 4: REGISTER MAP AND DEFAULTS

NOTE: bit 15 is the MSB, bit 0 is the LSB

DATA BIT MAP										ADDRESS BITS				DID BITS			R/W
	BIT # →	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG #	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	DID2	DID1	DID0	R/W
0	PWR/ SPM Mode	HIZ	BRAKE	RUN	EXCOMM	DT1	DT0	PS1	PS0	0	0	0	0	1	1	1	0
1	SPM CTRL1	TACH	REVR	SPMG	FLTBEMF	FLLCLMP	SPMDAC2	SPMDAC1	SPMDAC0	0	0	0	1	1	1	1	0
2	SPM CTRL2	DWT_SEL	RSD_SEL	HHB_LSD	HHB_HSD	HHB_SEL	VREFSEL	MECH	SPDMECH	0	0	1	0	1	1	1	0
3	RSD_LSB	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0	0	0	1	1	1	1	1	0
4	RSD_MSB		RSD14	RSD13	RSD12	RSD11	RSD10	RSD9	RSD8	0	1	0	0	1	1	1	0
5	TRK LOOP	TF	SWITCH	MUX	PESGN4	PESGN3	PESGN2	PESGN1	PESGN0	0	1	0	1	1	1	1	0
6	WINDOW COMP	SENGN3	SENGN2	SENGN1	SENGN0	WTHRES3	WTHRES2	WTHRES1	WTHRES0	0	1	1	0	1	1	1	0
7	TI RESV 1	TI7	TI6	TI5	TI4	TI3	TI2	TI1	TI0	0	1	1	1	1	1	1	0
8	TI RESV 2	TI15	TI14	TI13	TI12	TI11	TI10	TI9	TI8	1	0	0	0	1	1	1	0
9	LED/DWT			LED2	LED1	DWT_ COMPH*	DWT_ COMPM*	DWT_ COMPL*	DWT_RST	1	0	0	1	1	1	1	0
10	TESTMUX (see Warning)		WIN_TEST	SPM_GIN	SPM_ STRESS	TEST3	TEST2	TEST1	TEST0	1	0	1	0	1	1	1	0

*NOTE: These bits are read only.

WARNING: Writing to register 10 could adversely affect the functionality of the SPDMECH/SPDTACH pin.

NOTE: During read back and with R2, B14 = 0, Register 3 and Register 4 look like this:

DATA BIT MAP										ADDRESS BITS				DID BITS			R/W
	BIT # →	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG #	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	DID2	DID1	DID0	R/W
3	RSD_LSB	COUNTER 7	COUNTER 6	COUNTER 5	COUNTER 4	COUNTER 3	COUNTER 2	COUNTER 1	COUNTER 0	0	0	1	1	1	1	1	0
4	RSD_MSB	OVERFLOW	COUNTER 14	COUNTER 13	COUNTER 12	COUNTER 11	COUNTER 10	COUNTER 9	COUNTER 8	0	1	0	0	1	1	1	0

PIN DESCRIPTION

Pin types are defined as: A = Analog; D = Digital; G = Ground; I = Input; O = Output; P = Power

TERMINAL FUNCTIONS

The terminal functions listed below are grouped by function.

SUPPLIES

NAME	TYPE	DESCRIPTION
AVCC	P	5 V analog power supply
DVCC	P	5 V digital power supply
VCMVCC1	P	VCM power supply
VCMVCC2	P	VCM power supply
SPNVCC1	P	Spindle power supply
PNVCC2	P	Spindle power supply
AGND1	G	Analog ground
AGND2	G	Analog ground
DGND	G	Digital ground
VCMGND	G	VCM ground
SPNGND1	G	Spindle ground
SPNGND2	G	Spindle ground
REGVCC	P	3.3 V and 1.8 V regulator DC Input
REGGND	G	3.3 V and 1.8 V regulator ground

MISCELLANEOUS

OSCIN	D/I	External clock input
RBIAS	A	External resistor connected to this pin to set an internal bias current
VBOOST	A	Charge pump voltage connected to an external filter capacitor
LED1	A	LED driver.
LED2	A	LED driver.
DWT_IN	A	Dual window timer input.
DWT_TH_L	A	DWT low threshold input.
DWT_TH_M	A	DWT mid threshold input.
DWT_TH_H	A	DWT high threshold input.

VOLTAGE MONITOR

CPOR	A	Power-on reset delay capacitor
RSTZ	D/O	Power-on reset output & input

SERIAL PORT

NAME	TYPE	DESCRIPTION
SCLK	D/I	Serial port input clock
SDATA	D/I/O	Serial port data
SENA	D/I	Serial port select (Active “H”)

VCM

RETOUT	A	Retract drive output
CRETIN	A	Retract drive capacitor voltage input
CMPI	A	VCM current loop compensation filter
CMPO	A	VCM current loop compensation filter
VREFOUT	A	VCM reference voltage output
VREFC	A	VCM reference voltage capacitor input
RSENP	A	Positive VCM current loop sense
RSENN	A	Negative VCM current loop sense
FBOUT	A	Current sense amplifier output
VCMB	A	VCM driver output B
VCMA	A	VCM driver output A

TRACKING LOOP SUPPORT

COMPOUT	A	Tracking loop compensation output
COMPIN	A	Tracking loop compensation input
CPESOUT	A	Composite position error output
COMPSUM	A	Loop compensation summing point
CPESIN	A	Position error input
WINOUT	D	Window comparator output
SWITCH	A	Compensator switch output
SAMPLE	D	Sample position error/Hold. This pin is 3.3 V or 5 V compatible.

SPINDLE MOTOR

SPDMECH/ SPDTACH	D/O	Spindle speed mech output/tachometer output or external tachometer signal input
SPDCAP	A	Speed loop compensation network connection
U	A	Spindle phase U output
V	A	Spindle phase V output
W	A	Spindle phase W output
SRCAP	A	Spindle slew rate control cap
RSS	A	Maximum SPM current limiting resistor

PIN DESCRIPTION (continued)

Pin types are defined as: A = Analog; D = Digital; G = Ground; I = Input; O = Output; P = Power

TERMINAL FUNCTIONS

The terminal functions listed below are grouped by function.

3.3 V AND 1.8 V REGULATORS

NAME	TYPE	DESCRIPTION
VREG1.8	A	1.8 V regulator output
VREG3.3	A	3.3 V regulator output

ELECTIRCAL SPECIFICATIONS

AV_{CC} = 5.0, DV_{CC} = 5.0 V, T_A = 25 °C (unless noted otherwise)

ABSOLUTE MAXIMUM RATINGS

Over free-air temperature range (unless otherwise noted) (See Note 0)

PARAMETER		RATING
Motor supply: $SPMV_{CC}$, $VCMV_{CC}$ (See Note 1)		-0.3 V to 6 V
Bias supply voltage: AV_{CC}, DV_{CC} (See Note 1)		-0.3 V to 6 V
Input voltage range, V_i (See Note 2)		-0.3 V to 6 V
Spindle DC current, $I_{S\text{-}DC}$: U,V,W (See Note 3)		1.2 A
Spindle PEAK current, $I_{S\text{-}PEAK}$: U,V,W		1.5 A
VCM DC current, $I_{V\text{-}DC}$: VCMA, VCMB (See Note 2)		±0.6 A
VCM PEAK current, $I_{V\text{-}PEAK}$: VCMA, VCMB		±0.7 A
Operating virtual junction temperature, T_J		$0 \le T_J \le 150$ °C
Thermal resistance:	junction-to case, $R\theta_{JC}$	10 °C/W
	junction-to-ambient, $R\theta_{JA}$ (See Note 4)	85 °C/W
Storage temperature range		-55 °C to 125 °C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		250 °C

NOTE 0: Stresses beyond those under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to ground.

NOTE 2: Since VCMA, VCMB, RSENN and RSENP are connected to inductive loads, particular care must be taken to not let these pins exceed 6 V. Snubbers or some other voltage limiting devices may be required.

NOTE 3: To be limited to less than 2 seconds.

NOTE 4: A lower $R\theta_{JC}$ is attainable if the exposed pad is connected to a large copper ground plane. $R\theta_{JC}$ and $R\theta_{JA}$ are values for TSSOP56 without an exposed pad. Actual thermal resistance would be better than the above values.

ELECTIRCAL SPECIFICATIONS (conditions)

RECOMMENDED OPERATING CONDITIONS

Spec items that only have “TYP” values only are not 100% tested.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Supply voltage on DV_{CC}, AV_{CC}, $SPMV_{CC}$, $VCMV_{CC}$		4.5	5.0	5.5	V
Digital high level input voltage on SCLK, SDATA, SENA, TEST, OSCIN SAMPLE, V_{IH} @ (3.3 V/5 V)			2		V
Low level input voltage on SCLK, SDATA, SENA, TEST, OSCIN SAMPLE, V_{IL} @ (3.3 V/5 V)				0.8	V
Supply current Icc, (Total for DV_{CC} & AV_{CC})	PS1 = 0 PS0 = 0 (SLEEP MODE)		150	300	µA
	PS1 = 0 PS0 = 1 (STANDBY MODE)			14	mA
	PS1 = 1 PS0 = 1 (ACTIVE MODE)			20	mA
Power-on reset delay time setting range trdsr		1		150	ms
SPM current range		0		1.0	A
Start up current (less than 2 sec and 50% duty cycle)				1.0	A
Acceleration current (less than 3 sec and 50% duty cycle)				0.5	A
Rotation current (after acceleration) (Note 1)				0.35	A
Slew rate(SR) control range (Note 2)			2.0		mA/µs
VCM current range		0		±0.7	A
OSCIN input frequency range (Note 3)		16		40	MHz
OSCIN rise time				3	ns
OSCIN fall time				3	ns
RBIAS output current			20		µA
Operating ambient temperature		0		70	°C

NOTE 1: For proper commutation, the SPM current (ISPM) must be limited by the slew rate (SR) and rotation speed (RPM) according to the following equation:
$I_{SPM}(mA) = 10{,}000 \bullet SR(mA/\mu s)/(Np \bullet RPM)$, where Np = number of poles

NOTE 2: Using a 1.0 nF capacitor at SPNCAP pin

NOTE 3: OSCIN has a 50% ±5% duty cycle

SERIAL INTERFACE TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK clock period	T_C		50			ns
SCLK low time	T_{CKL}		20			ns
SCLK high time	T_{CKH}		20			ns
Enable to SCLK	T_{SENS}		20			ns
SCLK to disable	T_{SENH}		100			ns
SDEN min low time	T_{SL}		100			ns
Internal bus turnaround time	T_{trn}	read	15			ns
Data set-up time	T_{DE}	read	15			ns
Data hold time	T_{DH}	read	15			ns
Falling SCLK to data valid	T_{skew1}	read	15			ns
Falling SCLK to data valid	T_{skewe}	read	15			ns
Falling SDEN to SDATA tri-state	T_{sendl}	read	50			ns
Data set-up time	TDE	write	15			ns
Data hold time	TDH	write	15			ns

NOTE: Cload = 40 pf

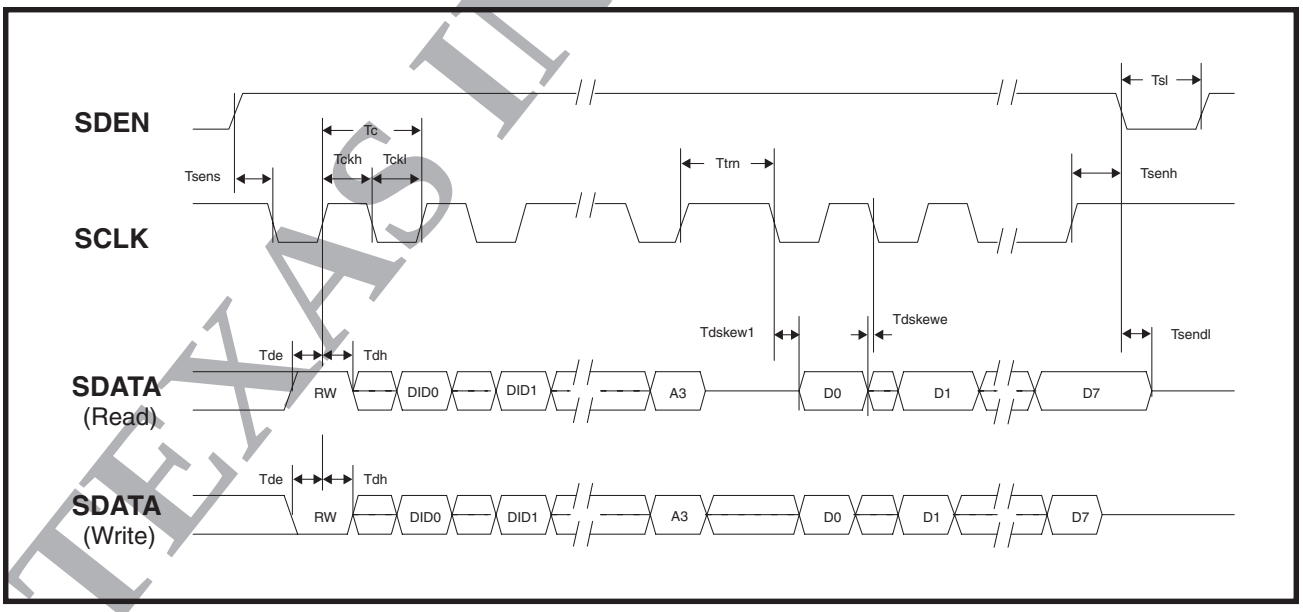


FIGURE 19: Serial Interface Timing Diagram

ELECTIRCAL SPECIFICATIONS (conditions)

DIGITAL I/O

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
High level logic input current I_{IH}				1.0	µA
Low level logic input current I_{IL}				-1.0	µA
Low level output voltage V_{OL}	Io = 100 µA			0.8	V
High level output voltage V_{OH}	Io = -100 µA	2			V

VOLTAGE/TEMPERATURE MONITOR AND RSTZ SINK CURRENT

Power-on reset threshold voltage Vpor		4.06	4.1	4.14	V
Power-on reset hysterisis Vh		50	100	150	mV
Minimum operating voltage Vop			0.7	0.8	V
CPOR source current Ipors		1.2	1.5	1.8	µA
CPOR H voltage V_{CPORH}		Avcc - 0.5 V	Avcc		V
Minimum power fault time tpw		25			ns
Reset response time 1 trpd1				5	µs
Reset response time 2 trpd2				10	µs
Thermal shutdown hysterisis Tsdh	Note 1	10	30	50	°C
Thermal shutdown temperature Tsd	Note 1	150	170	190	°C
Voltage at Rbias pin Vrbias	Rbias = 80 kΩ	1.56	1.6	1.64	V
RSTZ sink current IRSTZS	VCC = 4 V, VRSTZ = 1 V		4		mA
(Note 2)	VCC = 3 V, VRSTZ = 1 V		4		mA
	VCC = 2 V, VRSTZ = 1 V		0.8		mA
	VCC = 4 V, VRSTZ = 0.5 V		2		mA
	VCC = 3 V, VRSTZ = 0.5 V		2		mA
	VCC = 2 V, VRSTZ = 0.5 V		0.35		mA

NOTE 1: Not tested, guaranteed by design.

NOTE 2: Output has internal 50 k pull-up to Vcc which is additional load to that in table.

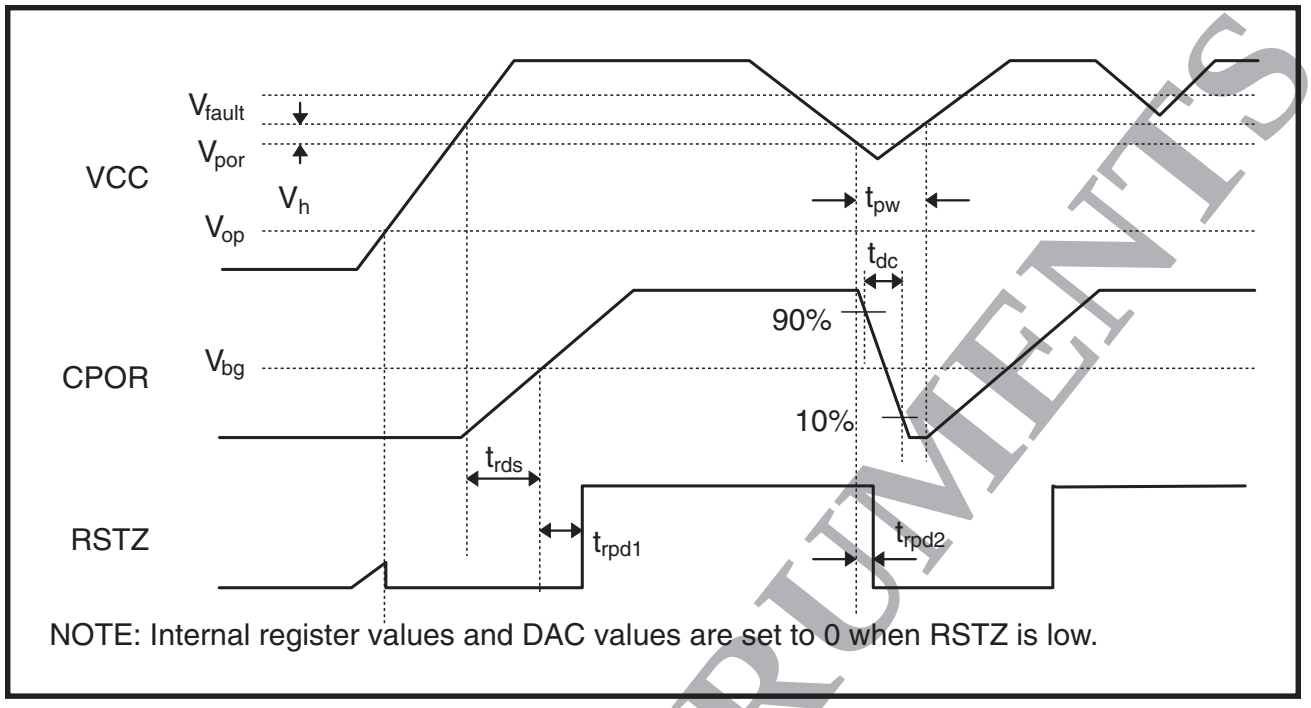


FIGURE 20: Voltage Monitor Timing Chart

ELECTIRCAL SPECIFICATIONS (conditions)

VBOOST

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VBOOST voltage	I_{LOAD} = 800 µA*, f = 16 - 40 MHz	VCC+ 4.75	VCC + 5	VCC + 5.25	V
VBOOST voltage ripple	C_{LOAD} = 0.68 µF		±20		mV_{p-p}
Rise time	VBOOST rise to AVCC + 4.75 V, C_{LOAD} = 0.68 µf			10	ms
Fall time	AVCC + 4.75 V down to 4.0 V, C_{LOAD} = 0.68 µf, I_{LOAD} = 800 µA*		6.5		ms

* The I_{LOAD} is internal current consumption, not external current loading.

3.3 V REGULATOR SPECIFICATION

Output voltage		3	3.3	3.6	V
Output current		<1 µA		120	mA
Peak current loading	Lasts for <10 µs	200		300	mA
Capacitor loading		0.5		1.0	µF
Quiescent current in sleep or active mode			50	100	µA

NOTE: Regulator can supply full current in all power management modes

1.8 V REGULATOR SPECIFICATION

Output voltage		1.62	1.80	1.98	V
Output current		<1 µA		50	mA
Peak current loading	Lasts for <10 µs			95	mA
Capacitor loading		0.5		1.0	µF
Quiescent current in sleep or active mode			50	100	µA

NOTE: Regulator can supply full current in all power management modes.

VCM DRIVER AMPLIFIER

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Total Rds(on) for HSD and LSD	IVCM = 400 mA @ T_A = 25 °C		1.0	1.5	Ω
Amplifier reference voltage VREFOUT	1 mA source/sink				V
	VREFSEL = 0	0.47 • Vcc		0.53 • Vcc	
	VREFSEL = 1	0.47 • V3.3		0.53 • V3.3	
Input referenced common mode voltage gain		50			dB
VCM offset current $V_{vcmofsi}$	Rs = 0.5 Ω, Ri = Rf = 20 kΩ	-35		+35	mA
VCM clamp voltage V_{vcmcl}	I_{VCM} = 600 mA	5.7	6	6.3	V
Negative clamp voltage V_{vcmncl}	I_{VCM} = 300 mA	-0.25	-0.35	-0.45	V

SENSE AMPLIFIER PROGRAMMABLE GAIN SPECIFICATION

Relative accuracy	$\frac{G(n) - G(n-1) - step}{step}$	-3		+3	%
Sense amp gain: A_{SENSE} RSENP - RSENN to FBOUT	SENGN = 0000	TYP-10%•TYP	2.67	TYP+10%•TYP	V/V
	SENGN = 0001	TYP-10%•TYP	2.83	TYP+10%•TYP	
	SENGN = 0010	TYP-10%•TYP	3.00	TYP+10%•TYP	
	SENGN = 0011	TYP-10%•TYP	3.18	TYP+10%•TYP	
	SENGN = 0100	TYP-10%•TYP	3.37	TYP+10%•TYP	
	SENGN = 0101	TYP-10%•TYP	3.56	TYP+10%•TYP	
	SENGN = 0110	TYP-10%•TYP	3.78	TYP+10%•TYP	
	SENGN = 0111	TYP-10%•TYP	4.00	TYP+10%•TYP	
	SENGN = 1000	TYP-10%•TYP	4.24	TYP+10%•TYP	
	SENGN = 1001	TYP-10%•TYP	4.49	TYP+10%•TYP	
	SENGN = 1010	TYP-10%•TYP	4.75	TYP+10%•TYP	
	SENGN = 1011	TYP-10%•TYP	5.04	TYP+10%•TYP	
	SENGN = 1100	TYP-10%•TYP	5.33	TYP+10%•TYP	
	SENGN = 1101	TYP-10%•TYP	5.65	TYP+10%•TYP	
	SENGN = 1110	TYP-10%•TYP	5.98	TYP+10%•TYP	
	SENGN = 1111	TYP-10%•TYP	6.34	TYP+10%•TYP	

ELECTIRCAL SPECIFICATIONS (conditions)

VCM DRIVER GAIN SPECIFICATION

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Relative accuracy		$\frac{G(n) - G(n-1) - step}{step}$	-3		+3	%
VCM drive gain:	AVCM	SENGN = 0000	TYP-20%•TYP	3.74	TYP+20%•TYP	V/V
CMPO to VCMA		SENGN = 0001	TYP-20%•TYP	3.53	TYP+20%•TYP	
or VCMB		SENGN = 0010	TYP-20%•TYP	3.33	TYP+20%•TYP	
		SENGN = 0011	TYP-20%•TYP	3.15	TYP+20%•TYP	
		SENGN = 0100	TYP-20%•TYP	2.97	TYP+20%•TYP	
		SENGN = 0101	TYP-20%•TYP	2.81	TYP+20%•TYP	
		SENGN = 0110	TYP-20%•TYP	2.65	TYP+20%•TYP	
		SENGN = 0111	TYP-20%•TYP	2.50	TYP+20%•TYP	
		SENGN = 1000	TYP-20%•TYP	2.36	TYP+20%•TYP	
		SENGN = 1001	TYP-20%•TYP	2.23	TYP+20%•TYP	
		SENGN = 1010	TYP-20%•TYP	2.10	TYP+20%•TYP	
		SENGN = 1011	TYP-20%•TYP	1.99	TYP+20%•TYP	
		SENGN = 1100	TYP-20%•TYP	1.87	TYP+20%•TYP	
		SENGN = 1101	TYP-20%•TYP	1.77	TYP+20%•TYP	
		SENGN = 1110	TYP-20%•TYP	1.67	TYP+20%•TYP	
		SENGN = 1111	TYP-20%•TYP	1.58	TYP+20%•TYP	

RETRACT

Voltage drop of half H-Bridge high side driver FET		ICRET = 30 mA R2, B11 = 1 R2, B12 = 1			0.12	V
Total voltage drop of retract MOS drivers	Vretd	ICRET = 0.5 A R2, B11 = 0			1.0	V

TRACKING LOOP SPECIFICATIONS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
CPES input switch resistance	Rdson	See Note			1.5	kΩ
Sample and hold capacitor	C_{hold}			20		pF
Sample on time	Ton	See Note	4			µs
COMP input offset voltage	VOSCOMP	COMP_SUM = VREFOUT			±10	mV
Offset @ CPES_OUT	CPESOS	PESGAIN = 2.5	-40		+40	mV
Input offset voltage	VOSCPES	CPES_IN = VREFOUT SAMPLE = VCC (switch on)			VREFOUT ±10	V mV
Bandwidth	BW	See Note	1.0			MHz
CPES_OUT	VOL	Isink = 1 mA	AVCC-0.4		0.3	V
voltage swing	VOH	Isource = 1 mA	AVCC-0.4		0.3	V
CPES amplifier input common mode voltage	VICPES			VREF ±1.25 V		V
COMP_OUT	VOL	Isink = 500 µA	AVCC-0.4		0.3	V
output voltage	VOH	Isource = 500 µA	AVCC-0.4		0.3	V
Hold droop rate at CPES_OUT	CPESDR	@ CPES_OUT with CPES_OUT = VREF			100	µV/µs
SWITCH to VREFOUT resistance		SWITCH = 1			165	Ω
ON resistance	Ron	R_L = 10 k between output and Vcc/2 input = 0 to Vcc				
CPES_OUT to COMP_IN		TF = 1			500	Ω
COMP_OUT to COMP_IN		TF = 0			3 k	Ω

NOTE: Guaranteed by design

ELECTIRCAL SPECIFICATIONS (conditions)

PES PROGRAMMABLE GAIN SPECIFICATION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Relative accuracy	$\frac{G(n) - G(n-1) - step}{step}$	-3		+3	%
Composite gain: PESGAIN CPES_IN to CPES_OUT	PESGN = 00000	TYP-10%•TYP	1.675	TYP+10%•TYP	V/V
	PESGN = 00001	TYP-10%•TYP	1.75	TYP+10%•TYP	
	PESGN = 00010	TYP-10%•TYP	1.825	TYP+10%•TYP	
	PESGN = 00011	TYP-10%•TYP	1.9	TYP+10%•TYP	
	PESGN = 00100	TYP-10%•TYP	1.975	TYP+10%•TYP	
	PESGN = 00101	TYP-10%•TYP	2.05	TYP+10%•TYP	
	PESGN = 00110	TYP-10%•TYP	2.125	TYP+10%•TYP	
	PESGN = 00111	TYP-10%•TYP	2.2	TYP+10%•TYP	
	PESGN = 01000	TYP-10%•TYP	2.275	TYP+10%•TYP	
	PESGN = 01001	TYP-10%•TYP	2.35	TYP+10%•TYP	
	PESGN = 01010	TYP-10%•TYP	2.425	TYP+10%•TYP	
	PESGN = 01011	TYP-10%•TYP	2.5	TYP+10%•TYP	
	PESGN = 01100	TYP-10%•TYP	2.575	TYP+10%•TYP	
	PESGN = 01101	TYP-10%•TYP	2.65	TYP+10%•TYP	
	PESGN = 01110	TYP-10%•TYP	2.725	TYP+10%•TYP	
	PESGN = 01111	TYP-10%•TYP	2.8	TYP+10%•TYP	
	PESGN = 10000	TYP-10%•TYP	2.875	TYP+10%•TYP	
	PESGN = 10001	TYP-10%•TYP	2.95	TYP+10%•TYP	
	PESGN = 10010	TYP-10%•TYP	3.025	TYP+10%•TYP	
	PESGN = 10011	TYP-10%•TYP	3.1	TYP+10%•TYP	
	PESGN = 10100	TYP-10%•TYP	3.175	TYP+10%•TYP	
	PESGN = 10101	TYP-10%•TYP	3.25	TYP+10%•TYP	
	PESGN = 10110	TYP-10%•TYP	3.325	TYP+10%•TYP	
	PESGN = 10111	TYP-10%•TYP	3.4	TYP+10%•TYP	
	PESGN = 11000	TYP-10%•TYP	3.475	TYP+10%•TYP	
	PESGN = 11001	TYP-10%•TYP	3.55	TYP+10%•TYP	
	PESGN = 11010	TYP-10%•TYP	3.625	TYP+10%•TYP	
	PESGN = 11011	TYP-10%•TYP	3.7	TYP+10%•TYP	
	PESGN = 11100	TYP-10%•TYP	3.775	TYP+10%•TYP	
	PESGN = 11101	TYP-10%•TYP	3.85	TYP+10%•TYP	
	PESGN = 11110	TYP-10%•TYP	3.925	TYP+10%•TYP	
	PESGN = 11111	TYP-10%•TYP	4	TYP+10%•TYP	

WINDOW COMPARATOR SPECIFICATION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Response time WREPT (sign mode)	WTHRES = 0000@ 100 mV overdrive			3	µs
Offset (sign mode) WOFFSET	WTHRES = 0000			20	mV
Window comparator WTHRES threshold for VREFSEL (R2, B11) = 0; VREF = VCC / 2	WTHRES = 0000		Sign mode		V
	WTHRES = 0001	TYP - 40 mV	0.1	TYP + 40 mV	
	WTHRES = 0010	TYP - 40 mV	0.2	TYP + 40 mV	
	WTHRES = 0011	TYP - 40 mV	0.3	TYP + 40 mV	
	WTHRES = 0100	TYP - 40 mV	0.4	TYP + 40 mV	
	WTHRES = 0101	TYP - 40 mV	0.5	TYP + 40 mV	
	WTHRES = 0110	TYP - 40 mV	0.6	TYP + 40 mV	
	WTHRES = 0111	TYP - 40 mV	0.7	TYP + 40 mV	
	WTHRES = 1000	TYP - 40 mV	0.8	TYP + 40 mV	
	WTHRES = 1001	TYP - 40 mV	0.9	TYP + 40 mV	
	WTHRES = 1010	TYP - 40 mV	1.0	TYP + 40 mV	
	WTHRES = 1011	TYP - 40 mV	1.1	TYP + 40 mV	
	WTHRES = 1011	TYP - 40 mV	1.2	TYP + 40 mV	
	WTHRES = 1101	TYP - 40 mV	1.3	TYP + 40 mV	
	WTHRES = 1110	TYP - 40 mV	1.4	TYP + 40 mV	
	WTHRES = 1111	TYP - 40 mV	1.5	TYP + 40 mV	
Window comparator WTHRES threshold for VREFSEL (R2, B11) = 1; VREF = 3.3 V / 21	WTHRES = 0000		Sign mode		V
	WTHRES = 0001	TYP - 40 mV	0.05	TYP + 40 mV	
	WTHRES = 0010	TYP - 40 mV	0.1	TYP + 40 mV	
	WTHRES = 0011	TYP - 40 mV	0.15	TYP + 40 mV	
	WTHRES = 0100	TYP - 40 mV	0.2	TYP + 40 mV	
	WTHRES = 0101	TYP - 40 mV	0.25	TYP + 40 mV	
	WTHRES = 0110	TYP - 40 mV	0.3	TYP + 40 mV	
	WTHRES = 0111	TYP - 40 mV	0.35	TYP + 40 mV	
	WTHRES = 1000	TYP - 40 mV	0.4	TYP + 40 mV	
	WTHRES = 1001	TYP - 40 mV	0.45	TYP + 40 mV	
	WTHRES = 1010	TYP - 40 mV	0.5	TYP + 40 mV	
	WTHRES = 1011	TYP - 40 mV	0.55	TYP + 40 mV	
	WTHRES = 1011	TYP - 40 mV	0.6	TYP + 40 mV	
	WTHRES = 1101	TYP - 40 mV	0.65	TYP + 40 mV	
	WTHRES = 1110	TYP - 40 mV	0.7	TYP + 40 mV	
	WTHRES = 1111	TYP - 40 mV	0.75	TYP + 40 mV	

ELECTIRCAL SPECIFICATIONS (conditions)

DUAL WINDOW TIMER

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Low, Mid, and High comparator offset voltage	Vos				15	mV

SPINDLE DRIVER

Total FET resistance	RON1	ISPM = 1.0 A, T_A = 25 °C		0.9	1.0	Ω
SPM Drivers current range						
Minimum Current		RSS = 2.0 kΩ		0		A
Maximum Current (Note 1)		RSS = 2.0 kΩ		1		A
SPM current gain where the SPM current gain = I_{OUT} / I_{RSS}	SPGM0	SPMG = 0, RSS = 2 k, VRSS ≤ 1 V	350	475	600	mA/mA
	SPGM1	SPMG = 1, RSS = 2 k, VRSS ≤ 1 V	1400	1900	2400	mA/mA
Charge/discharge current in SR cap	SR			10		µA
Relative slew rate accuracy 1 HSD to HSD between phases		See (Note 2 and 3)	-3		+3	%
Relative slew rate accuracy 2 LSD to LSD between phases		See (Note 2 and 3)	-3		+3	%
Relative slew rate accuracy 3 HSD to HSD vs. LSD to LSD		See (Note 2 and 3)	-10		+10	%
SPM clamp voltage	V_{spmcl}	See (Note 2 and 3)	VCC + 0.2	6.0	VCC + 0.6	V

NOTE 1: Spindle current should be limited by the following equation.

Vcc = VBEMF + ISPM • (RSPM + 1.0) + VSAT

where,
Vcc : Supply voltage
VBEMF : SPM back EMF voltage
ISPM : SPM current
VSAT : LSD saturation voltage and this voltage is dependent on I_{SPM}.

NOTE 2: The slew rate depends on the spindle motor parameters, peak current, and value of the SRCAP. The SR table values are for the following conditions:
SRCAP = 1 nf, ISPM = 100 mA, R_M = 4.8 Ω, L_M = 430 µH, RPM = 4000, and k_t = 83 g cm/A, PDT commutation delay = 100 µs.

NOTE 3: These parameters cannot be measured. They are determined by design characterization.

SPM BEMF PHASE COMPARATOR

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Offset voltage			10		mV
Delay	See Note 2			1	µs

NOTE 1: To be measured at test output

NOTE 2: Guaranteed by design

FLL SPEED CONTROL CIRCUIT

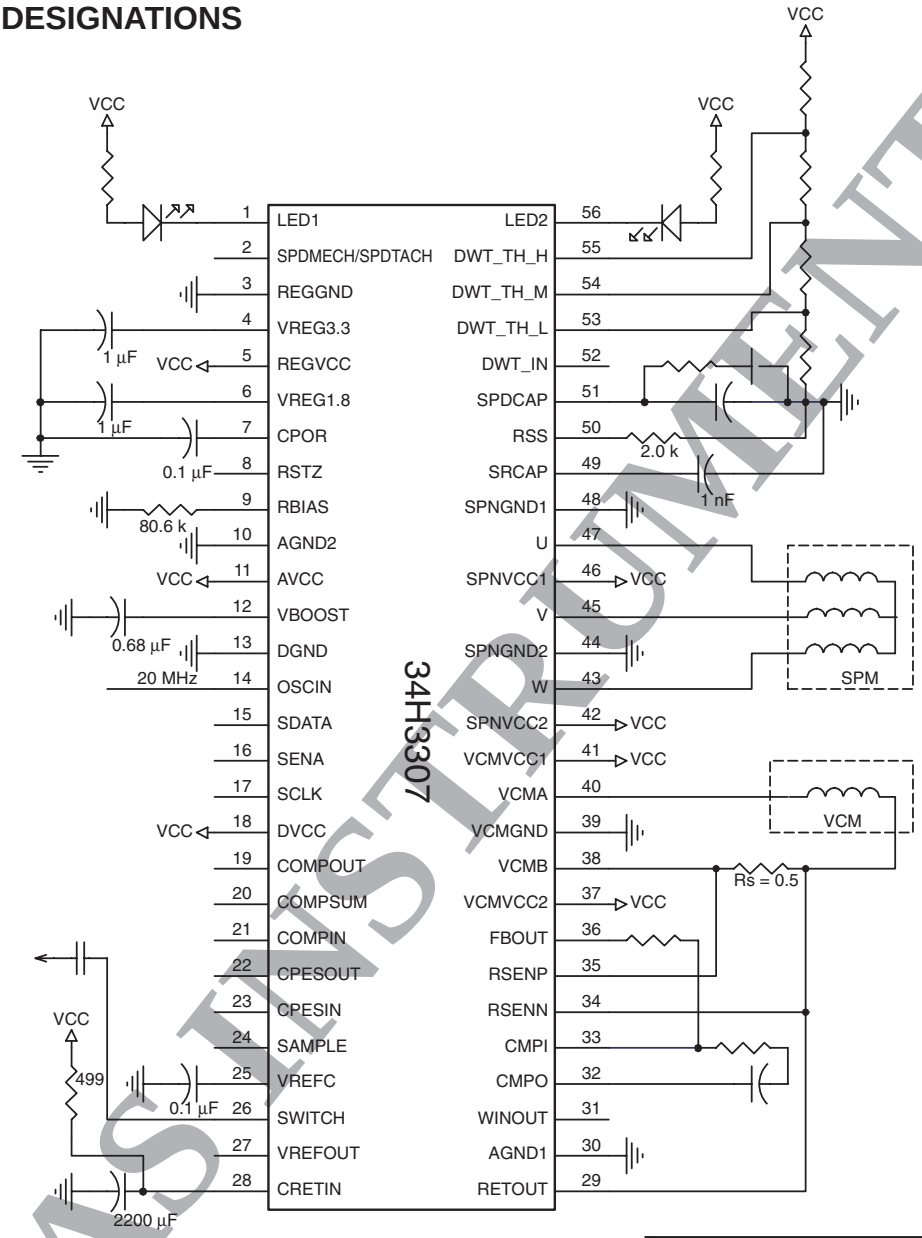
Velocity charge current			100		µA
Velocity discharge current			100		µA
Absolute accuracy		-15		+15	%
Relative accuracy		-15		+15	%

LED DRIVER SPECIFICATION

LED1	Voh	Isink = 40 mA			0.5	V
LED2	Voh	Isink = 40 mA			0.5	V

PACKAGE PIN DESIGNATIONS

(Top View)



56-Pin Package

CAUTION: Use handling procedures necessary for a static sensitive component.

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

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TLS2247
Servo-Combination Driver

February 1999

DESCRIPTION

The TLS2247 provides the capability to drive a voice-coil motor (VCM) and spindle motor of a hard disk drive system. The spindle section is a complete speed control servo system including power and predrivers requiring only a few additional discrete components for full functionality. The VCM section is a complete feedback controlled transconductance amplifier with power and pre-drivers. Only a few external compensation components is necessary to reshape the VCM closed-loop response. Serial interface is provided to program the internal registers for all user-selectable functions. Other supporting functions are also provided to facilitate the control of VCM during tracking. A functional block diagram of the TLS2247 chip is shown on page 2.

FEATURES

GENERAL

- **5 V operation, 3.3 V/5 V digital inputs**
- **Serial port interface (20 Mbit/s data transfer rate)**

VOICE COIL MOTOR (VCM) DRIVER

- **High efficiency drivers, 1.5 Ω Rds(on) total (worst case)**
- **0.6 A capability**
- **Sense resistor current control**
- **5-bit programmable gain for CPES signal**
- **2-mode window comparator with 4-bit programmable threshold**

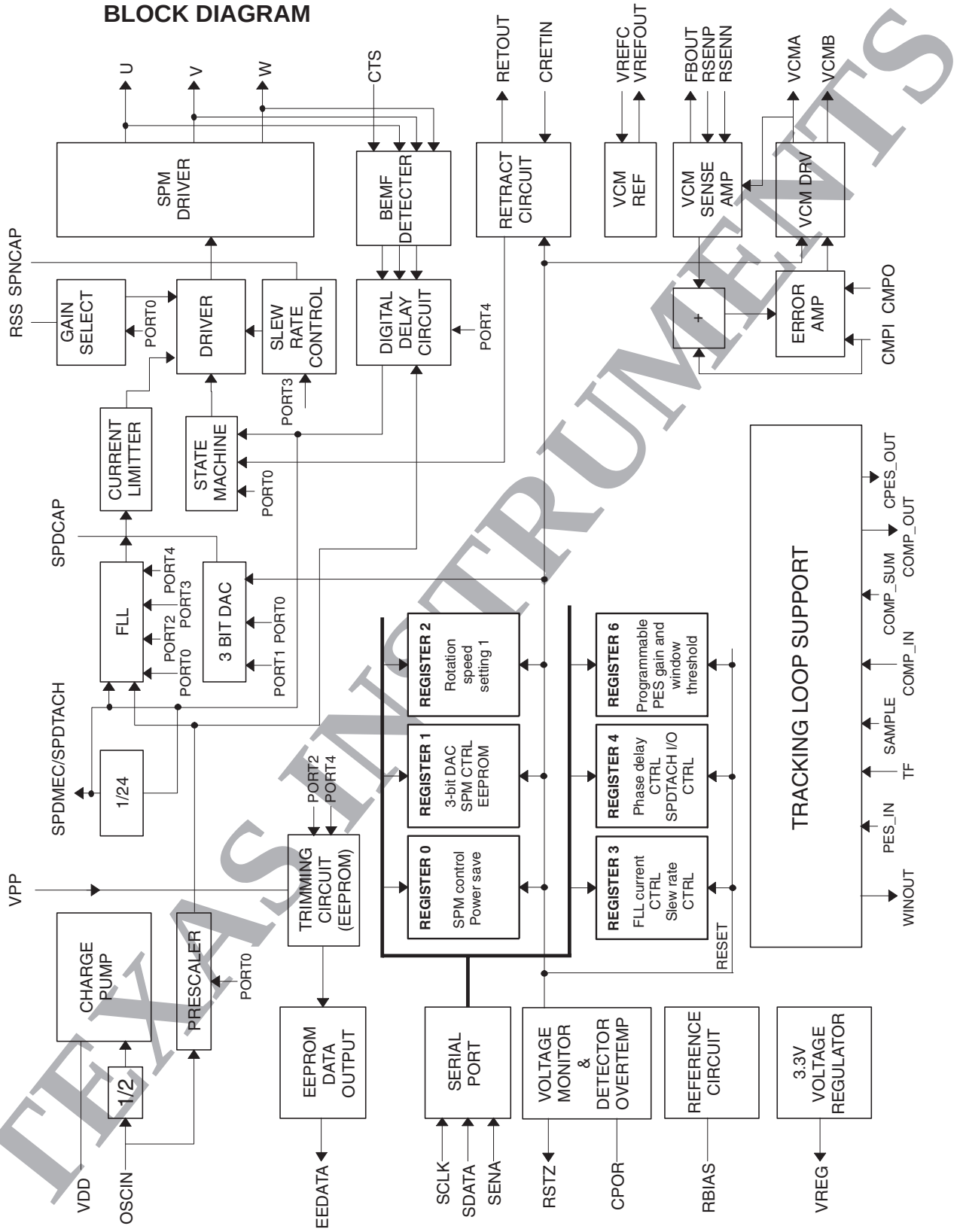
SPINDLE MOTOR DRIVER

- **High efficiency drivers, 1.0 Ω Rds(on) total (worst case)**
- **1.0 A capability**
- **Digital commutation delay and blanking**
- **Bipolar drive**
- **3 bit DAC for start up current**
- **Driver slew rate control by setting an external capacitor**
- **FLL rotation speed control**

VOLTAGE MONITOR/VOLTAGE REFERENCE

- **Supply voltage fault/reset detector provides ±2% tolerance**
- **3.3 V voltage regulator with 125 mA load capability**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

SERIAL PORT

The serial port facilitates programming of the TLS2247's six internal registers via sixteen bit data packets. Each data packet contains register address and control information. The maximum serial clock frequency is 20 Mhz. The digital inputs are 3.3 V/5 V compatible.

SERIAL PORT TIMING

The serial port uses three control lines: SCLK (serial port clock), SDATA (serial port data), and SENA (serial port enable, active HIGH). SDATA is the serial data signal and must be synchronous with the rising edge of SCLK. When SENA is LOW the input bit counter is reset. When SENA is HIGH the next rising edge of SCLK begins loading SDATA into the 16 bit input data register. After the sixteenth clock the input register is transferred to the selected port register. SENA must return LOW between each 16 bit data transfer to ensure proper synchronization. The serial port timing and bit numbering are shown in Figure 1. The Serial Port Timing Table on page 34 contains all serial port timing specifications.

REGISTER AND DATA-BIT DEFINITIONS

The TLS2247 serial port contains internal registers that are programmed via the SCLK, SDATA, and SENA signals. Data bits 15-13 are used as an address indicator to determine which register is selected.

The Register Description section and sub-tables define the contents of each register. Table 7 summarizes the internal register contents.

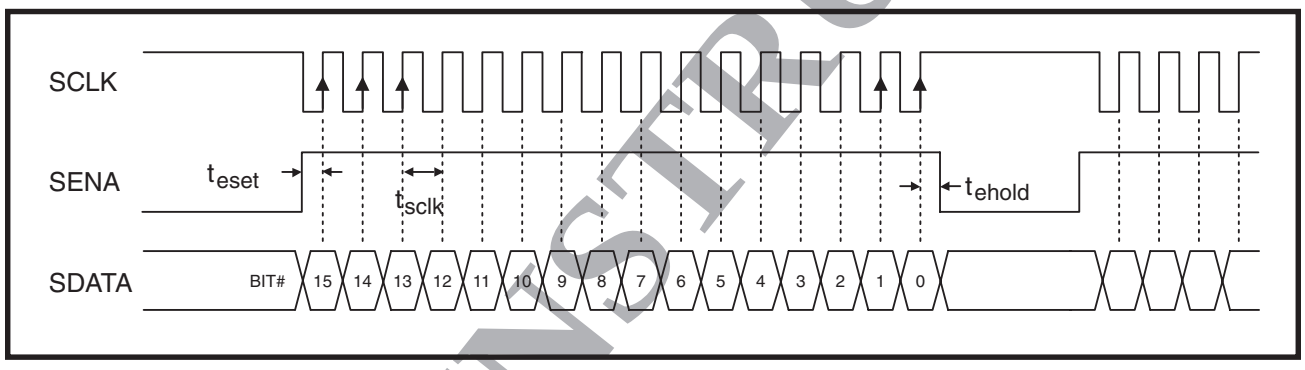


FIGURE 1: Serial-Port Data Transfer

FUNCTIONAL DESCRIPTION (continued)

VOLTAGE MONITOR/OVER-TEMPERATURE DETECTOR

The voltage monitor circuit, shown in Figure 2, has 2 external outputs. This circuit monitors the AVCC power source and generates an external reset signal (RSTZ) any time the voltage is less than Vpor. The IRSTZ signal is the same as the RSTZ signal or'd with the over temperature condition and is used internally by the brake and retract functions. The CPOR output is for an external capacitor that determines the desired RSTZ delay. No other component should be connected to this terminal.

DETAILED CIRCUIT DESCRIPTION

As the power supply (AVcc) ramps up and reaches Vop, RSTZ becomes active(low). When it reaches Vpor + Vh, CMP1 output switches to low and the external capacitor connected to CPOR starts to charge up at a rate determined by the current generator and the CPOR capacitor. When CPOR reaches the reference voltage, CMP2 switches and RSTZ goes inactive(high). If AVcc then drops below Vpor, the capacitor discharges rapidly and RSTZ goes low. If Vcc starts to ramp up after falling below Vpor, CPOR stays low (0 V) until AVcc again goes above Vpor + Vh at which point CPOR starts to charge up and after the delay, enables RSTZ to go high. See Figure 2 in this section and Figure 18 in the Electrical Specifications.

CHARGE PUMP

The function of the charge pump circuit (Figure 3) is to generate a 10 V power source (VDD) from the AVCC power source. A higher voltage is required for the SPM and VCM high side MOSFET gate control and to power internal circuits for the brake and retract functions during a power fault condition, and for 3.3 V voltage regulator. The VDD pin is to allow for the connection of an external filtering/storage capacitor.

DETAILED CIRCUIT DESCRIPTION

As soon as the chip is powered up, the charge pump becomes activated. The OSCIN/2 signal, with half frequency of the external oscillator, is divided into two phases. During the positive half cycle of OSCIN/2 signal, the negative sides of C1 and C3 are at ground, while the negative side of C2 is at the supply voltage (nominally 5 V). During this time, C1 charges through the Schottky diode, and any charge on C2 is passed to C3. During the negative half cycle, the negative sides of C1 and C3 are pushed up to the supply voltage, while the negative side of C2 is at ground. During this time, the positive sides of C1 and C3 are elevated above the power supply rails by the pair of inverters so that the charge on C1 is passed to C2 through the second Schottky diode, and the charge on C3 is likewise passed on to the external capacitor. A fraction of the charge pump output on the VDD pin is compared with an internally generated voltage reference in order to regulate the output voltage to 10 V. Once the output reaches 10 V, the comparator trips, which resets the latch and the charge pump is disabled. Should the voltage fall below 10 V, the comparator will trip again to re-enable the charge pump. The diode between VDD and AVCC is to ensure there is always enough voltage on the charge cap for the other circuits supplied by Vdd to function at startup. The leakage current through the voltage divider is negligible.

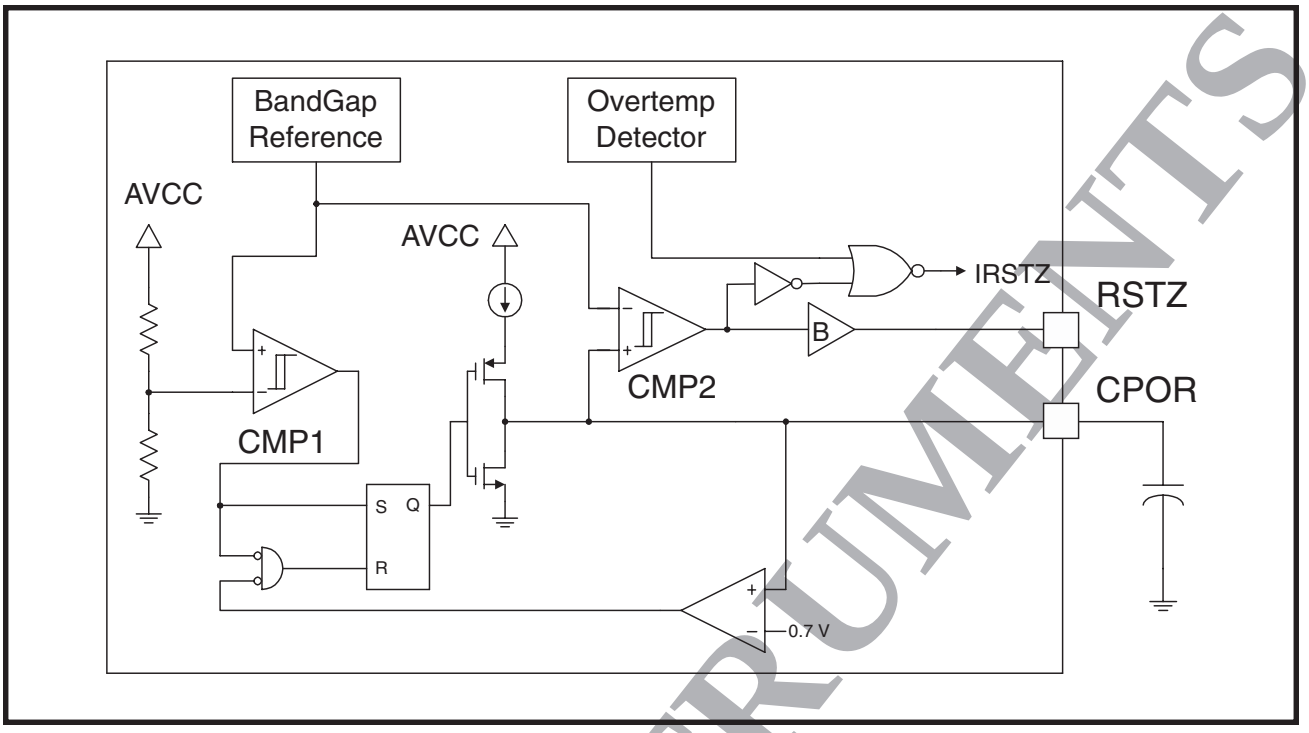


FIGURE 2: Voltage Monitor Circuit

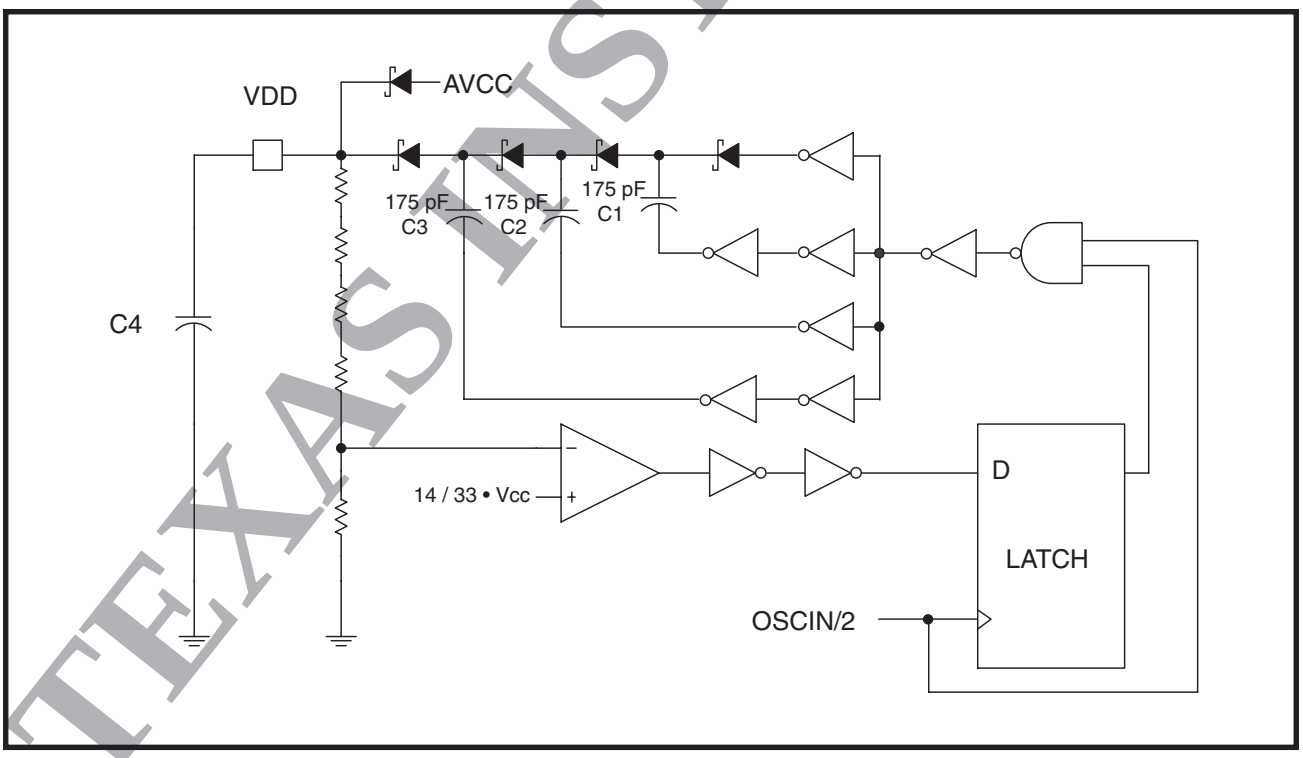


FIGURE 3: Charge Pump Circuit

FUNCTIONAL DESCRIPTION (continued)

3.3 V VOLTAGE REGULATOR

The 3.3 V voltage regulator provides 125 mA (max) DC output for other external circuits. The maximum loading can reach 250 mA peak. The output voltage level is in the range of 3 to 3.6 V (i.e., ±10% tolerance). Figure 4 shows a simplified block diagram of the 3.3 V voltage regulator. The output of the voltage regulator is given by:

$$VREG = VBG \bullet \left(1 + \frac{R_1}{R_2}\right)$$

(Equation 1)

RETRACT

Figure 5 is a simplified circuit diagram of the retract circuit. The purpose of the retract circuit is to retract and park the read/write heads away from the media when power is turned on or off or when a fault exists. This is accomplished by turning on the retract and the VCMA Low-Side Drive FETs whenever the RST signal is active.

VOICE COIL MOTOR CONTROL

The voice coil motor (VCM) drive system shown in Figure 6 is a complete feedback controlled current amplifier for operating a VCM mechanism in a disk drive unit. It consists of a full bridge power drive and a pre-driver. The power driver is an amplifier using an external sense resistor for current feedback. The pre-driver provides for external bandwidth limiting via discrete components for tailoring to particular mechanisms.

VCM DETAILED DESCRIPTION

The voice-coil full-bridge power amplifier is capable of ±0.6 A output current and has a maximum Rds(on) resistance of 1.5 Ω. The voice coil control system uses an external sense resistor in series with the motor to detect load current. The four amplifiers, A1 to A4, together with the sense VCM detailed description

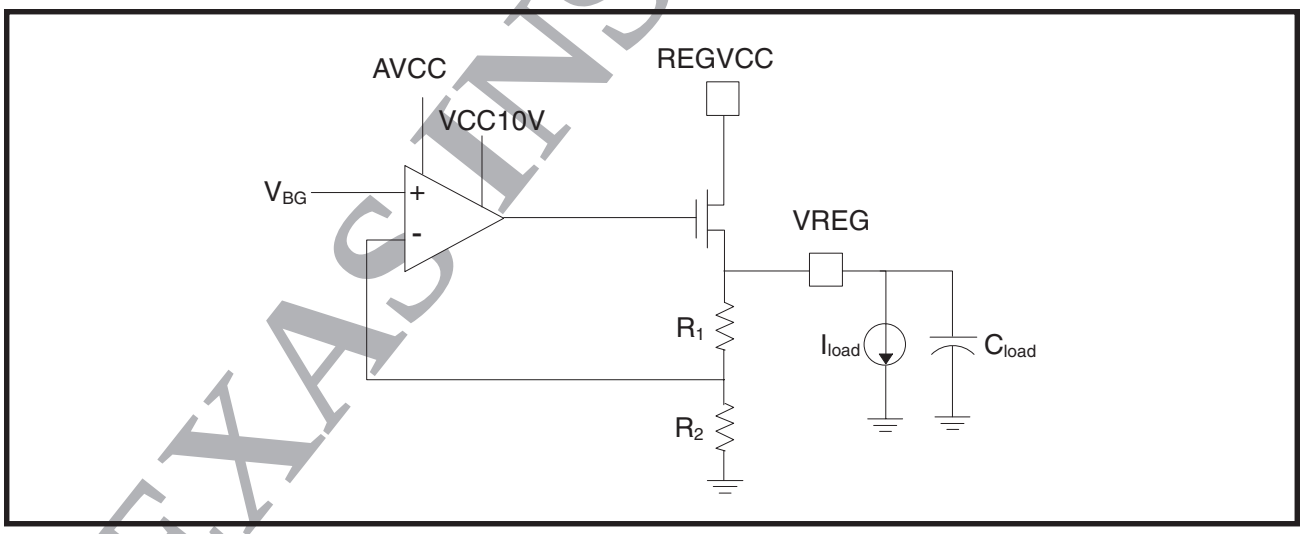


FIGURE 4: 3.3 V Voltage Regulator

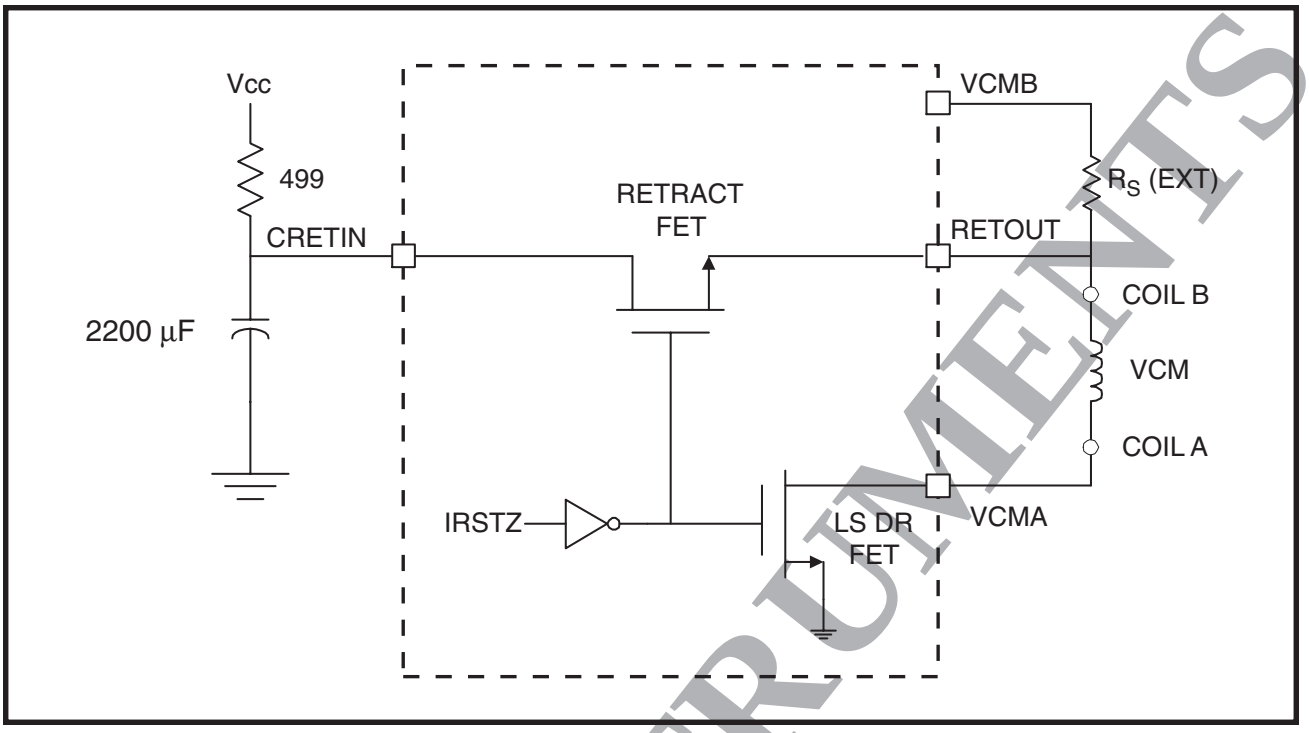


FIGURE 5: Retract Circuit

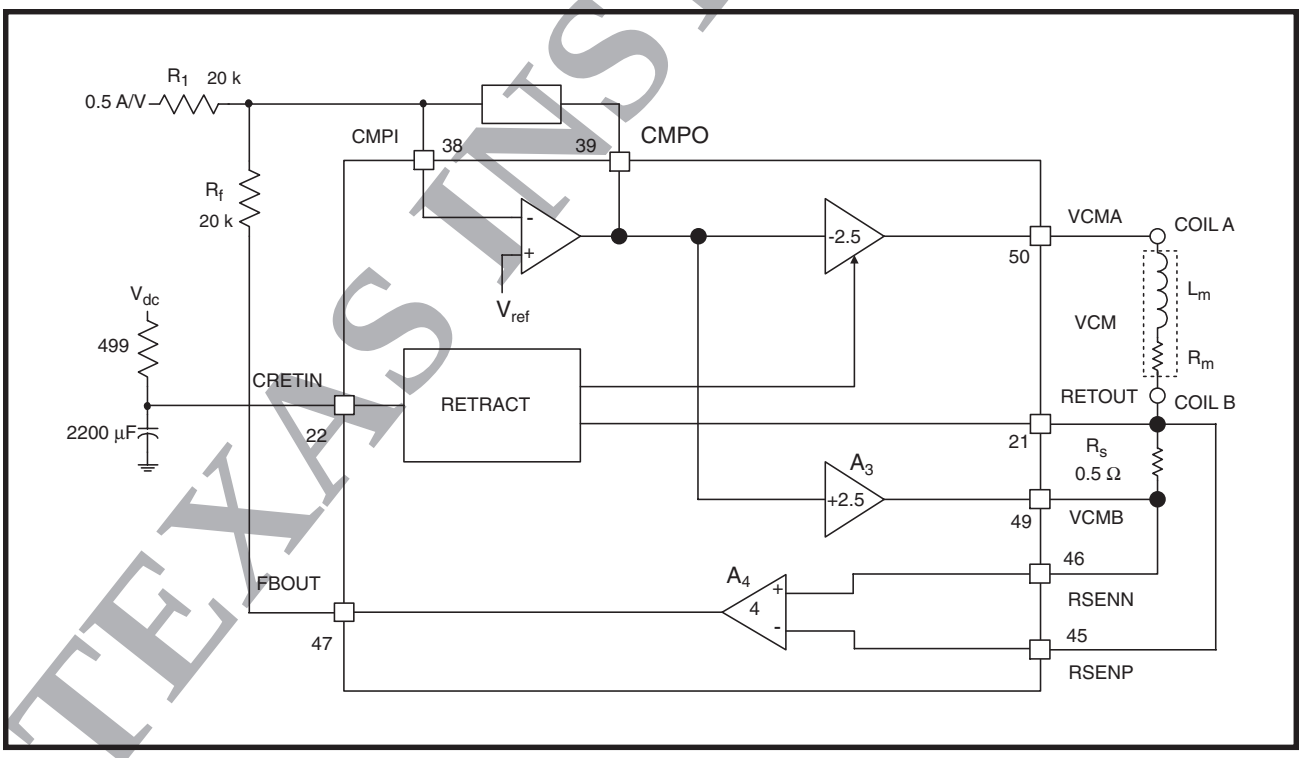


FIGURE 6: VCM Control Circuit

VCM DETAILED DESCRIPTION (continued)

resistor and the external resistors, Ri and Rf, make up a current feedback control loop. The result is a transconductance gain from the input resistor to the VCM load current that is:

$$G_{vcm} = I_m / V_{in} = R_f/(4R_iR_s) = 0.5(A/V)$$

for the values shown in Figure 6

(Equation 2)

The VCM loop includes provision for an external compensation network for shaping the frequency response of the transconductance amplifier. The compensation network is usually a simple R-C circuit. The output voltage of the power amplifier is limited to 6.3 V by active clamp circuits (not shown).

One bit, ENVCM, in the internal register is provided to disable VCM loop while still keeping the tracking loop enabled. The control logic is shown in a simplified block diagram in Figure 7.

TRACKING LOOP SUPPORT

The tracking loop circuits are comprised of 1) a zero order sample and hold, 2) an inverting opamp stage to support an external compensation filter with switches that can be used to enable/disable the compensation filter, 3) a position error amplifier with 32-level programmable gains in equal steps, and 4) a 16-level threshold window comparator operating in two modes: sign mode and window mode.

The tracking loop support provides several functions to facilitate the VCM control during tracking. Figure 8 gives a simplified block diagram of these functions. The input position error signal (CPES_IN) is sampled by a zero-order sample and hold. The sampled signal is then amplified by opamp A1 with a programmable gain. The gain is controlled by a switching network and a resistor chain. Finally, the position error signal (CPES_OUT) or the compensated signal (COMP_OUT) is passed through the window comparator. The window comparator operates in two modes: sign mode and window mode.

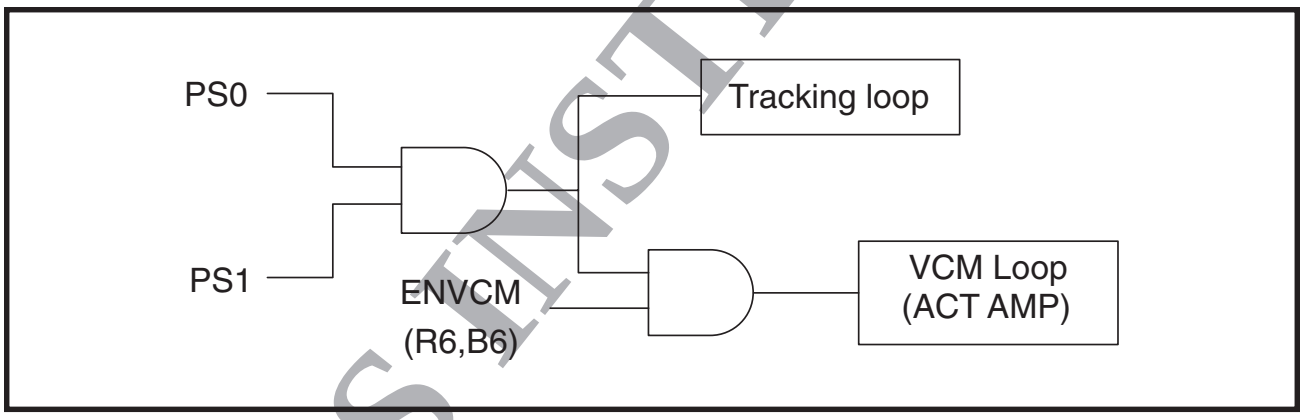


FIGURE 7: Tracking Loop Control Logic

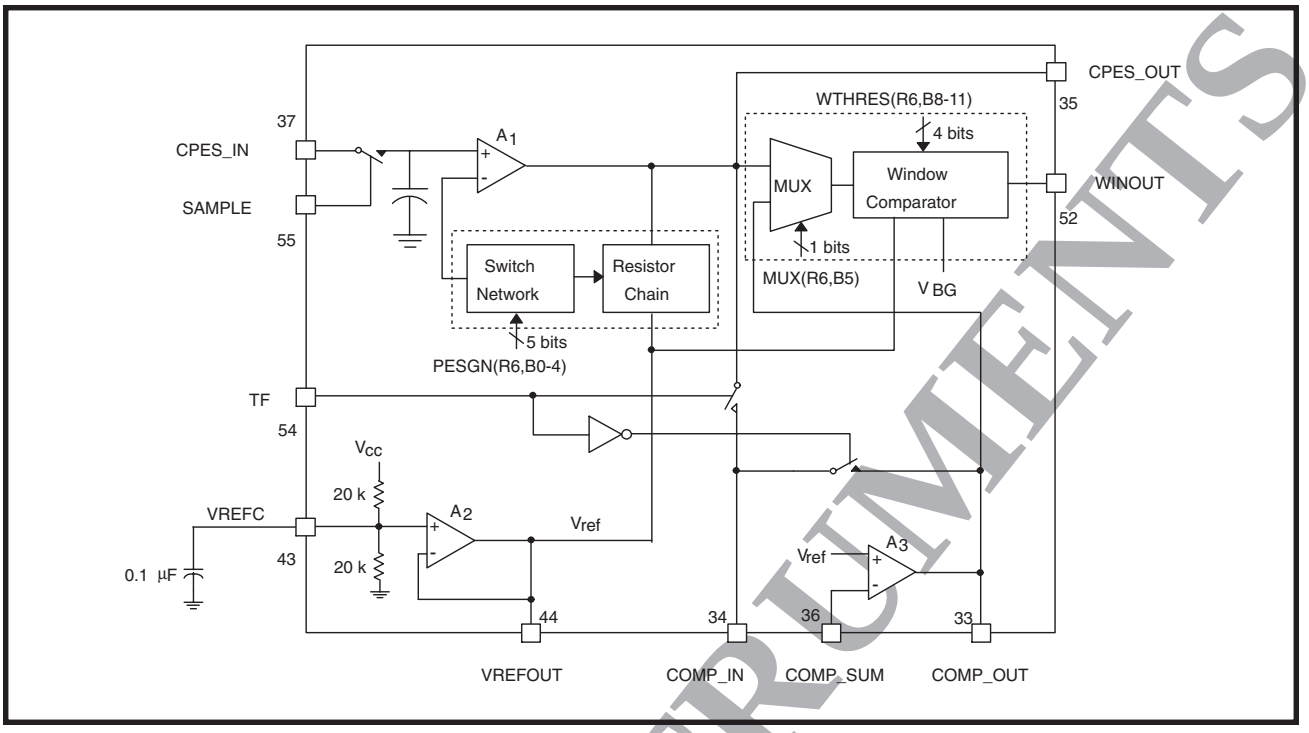


FIGURE 8: Tracking Loop Support

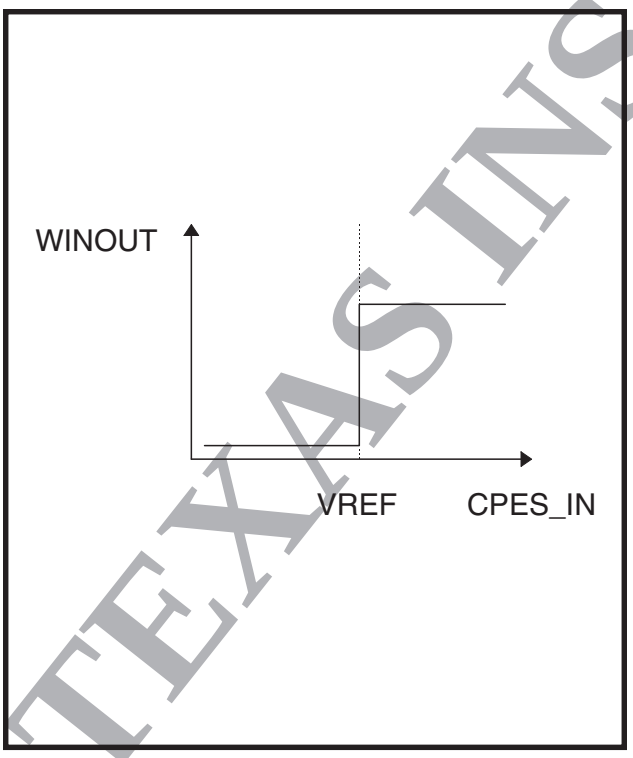


FIGURE 9: Transfer Curves for Sign Mode

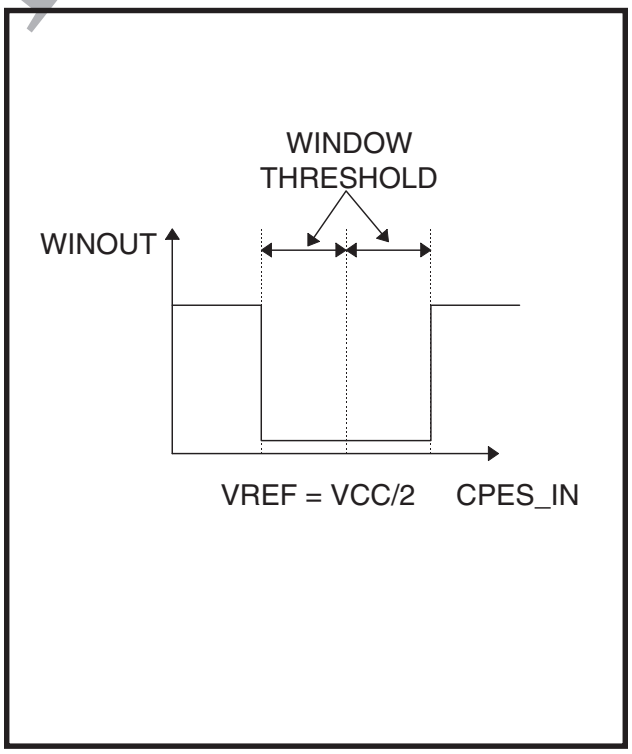


FIGURE 10: Transfer Curves for Threshold Mode

TRACKING LOOP SUPPORT (continued)

The window threshold is programmable with 15 levels in linear scale. The operating modes and the thresholds are controlled by 4 bits in an internal register. All bits being zeros indicates that the window comparator is in the sign mode. Other bit combinations (e.g., 1010) are used for setting the ± window thresholds. The window comparator accepts two inputs, CPES_OUT and COMP_OUT, multiplexed by another bit in the internal register. The window thresholds are symmetrical to the window center point VREF (VCC/2) and independent of the power supply voltage since they are derived from the bandgap reference voltage. The transfer curves of the window comparator in sign mode and threshold mode are shown in Figures 9 and 10.

SPINDLE MOTOR DRIVE

The Spindle Motor (SPM) Drive system controls the spindle/disk assembly in a disk drive. The complete servo system includes three identical power drivers and a pre-drive system. Each power driver is a transconductance amplifier with user selectable gain and slew rate. The pre-drive provides for frequency lock servo control. A state machine controls the motor commutation sequence by means of the EXCOMM bit in a serial port register or by the motor's back EMF (BEMF) zero crossings. The spindle motor system is a complete frequency lock loop (FLL) speed feedback control system for controlling the speed of a three-phase brushless motor. It consists of two main sections: (1) speed control circuits and (2) phase winding commutation and current slewing circuits. The digital feedback signal, derived either internally from the BEMF zero crossings of the motor or externally from the data written on the disk, is compared to a digital reference signal. The error signal produced is then amplified and applied to the motor. The motor thus accelerates or decelerates until the two frequencies are the same. The power section of the spindle motor system converts the voltage at the SPDCAP to a proportional peak current level in the three spindle motor windings . It also performs the commutation and current slewing that allows the motor to be treated in the system as a simple DC motor. Control of the transconductance gain and slewing rate is programmed through the serial port.

BEMF DETECT CIRCUIT

The BEMF detect circuit measures the voltage on the unexcited motor phase, and compares it to the center-tap (CTS) voltage. The BEMF detect circuit (Figure 11) consists of a comparator, and three transmission gates.

The state machine knows which phase is the unexcited phase and will assert one of the ZCU, ZCV and ZCW signals to open one of the transmission gates so that the unexcited phase is connected to the positive input of the comparator. The negative input of the comparator is always connected to the center-tap. The output of the comparator (ZCRS) goes to the spindle state machine.

The 10 kΩ resistor divider connected to the CTS pin sets it to mid supply voltage to ensure proper BEMF detection during HIZ mode.

The ZCRS signal thus produced makes a transition for each zero crossing of the BEMF of each of the three motor windings. This is at every 60 electrical degrees of actual motor rotation or 6Np/2 transitions per revolution where Np is the number of motor poles per revolution.

SPINDLE CONTROL LOGIC

The spindle control logic consists of a 12 bit commutation delay counter and a spindle motor (brushless DC) state machine (Figure 12). The commutation delay counter serves a dual purpose of 1) providing commutation delay, and 2) it filters out noise spikes that occur around the commutation point.

The ZCRS signal is either inverted or not inverted by the XOR circuit depending on the POS signal from the state machine. The POS signal is high when a positive going zero crossing of the BEMF is anticipated for starting the delay counter and low when a negative transition is expected.

A low LDZ signal input at the 12 bit counter causes it to be reloaded with the 12 bit PDT (phase delay time)

value at each positive clock edge. When LDZ is high the counter will count until end of count is reached, at which point the EOC signal goes high for one clock cycle. The ZCU, ZCV, and ZCW signals go to the BEMF detect circuit where they will open one of the transmission gates to select the undriven phase prior to when it is expected.

The state machine follows the states indicated in Table 1, and can be advanced either manually, using the EXCOMM signal (if COMS = 0), or by BEMF zero-crossings, using the COMM (if COMS = 1) signal. Other control options for the state machine are also shown in Table 1. The state machine is reset and outputs are disabled if either PS1 = 0 or SPNENA = 0.

Assuming a positive transition is expected, and POS is high, the ZCRS signal is then passed unchanged to the LDZ input on the 12 bit counter. As long as the ZCRS signal is low the counter is continually reloaded (with PDT value). At the BEMF zero crossing, the ZCRS goes high and the counter starts counting. Any noise spike on the ZCRS signal shorter than PDT clock times will be ignored since the counter will be reloaded after the noise spike goes away prior to the EOC pulse.

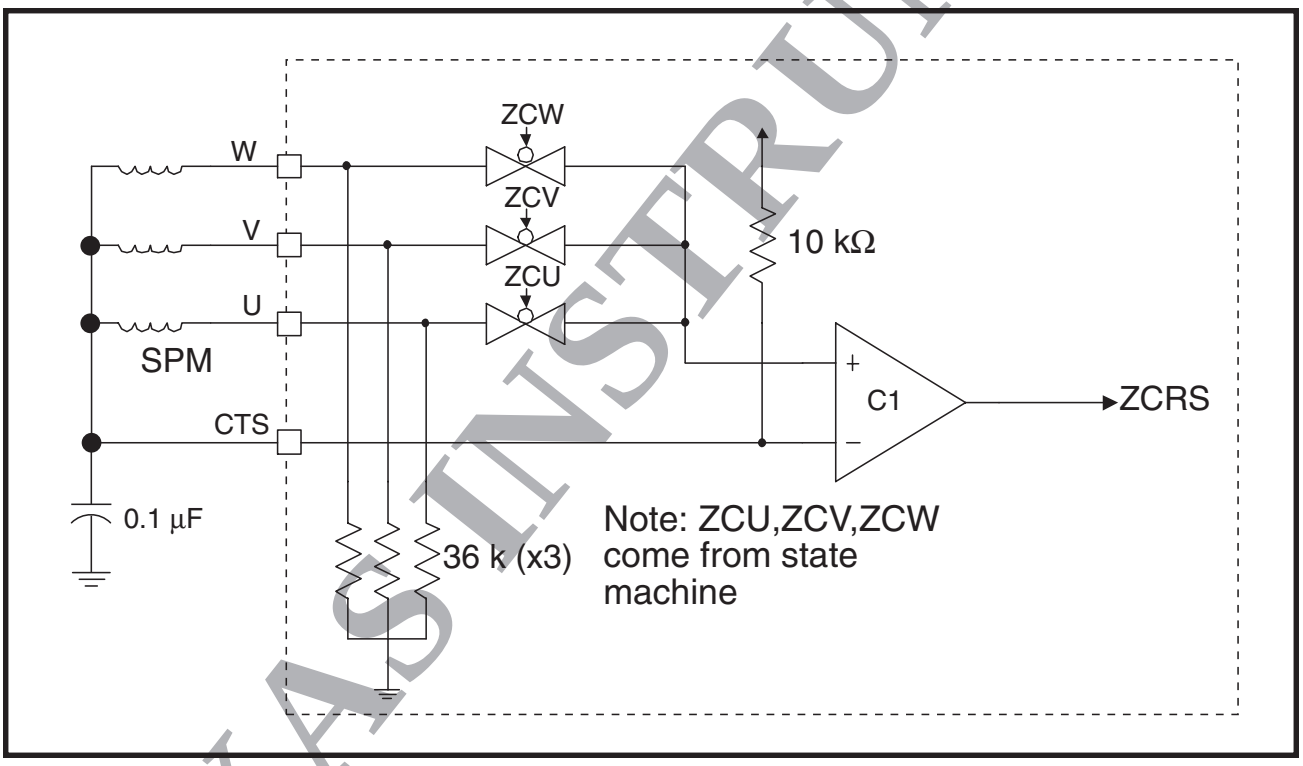


FIGURE 11: BEMF Detect Circuit

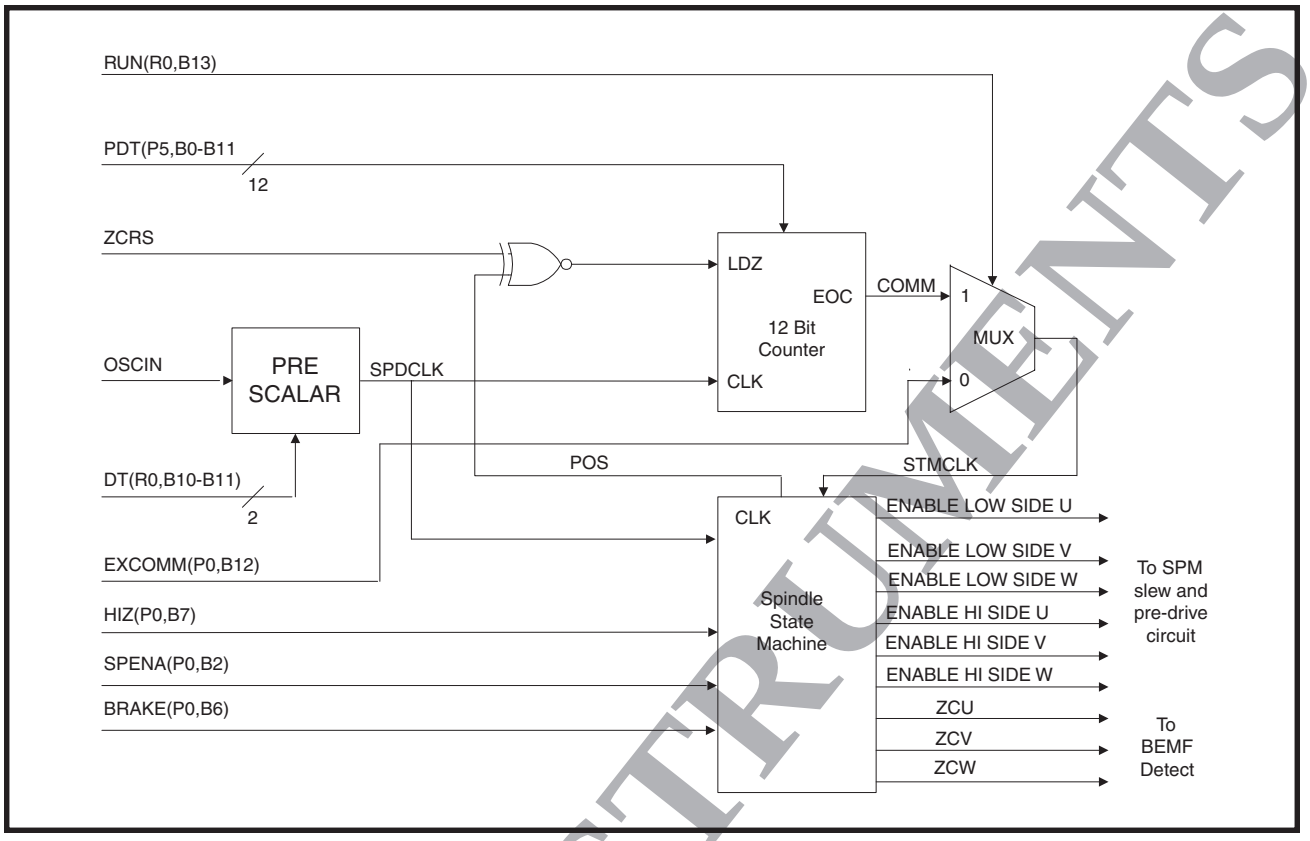


FIGURE 12: Spindle State Machine and Phase Delay Circuit

TABLE 1: State Machine Outputs

DESCRIPTION	STATE #	CURRENT DIRECTION	HIGHSIDE U	LOWSIDE U	HIGHSIDE V	LOWSIDE V	HIGHSIDE W	LOWSIDE W	POS
Basic	1	U-V	ON	OFF	OFF	ON	OFF	OFF	0
Commutation	2	U-W	ON	OFF	OFF	OFF	OFF	ON	1
PS1 = 1	3	V-W	OFF	OFF	ON	OFF	OFF	ON	0
SPNENA = 1	4	V-U	OFF	ON	ON	OFF	OFF	OFF	1
	5	W-U	OFF	ON	OFF	OFF	ON	OFF	0
	6	W-V	OFF	OFF	OFF	ON	ON	OFF	1
Power save	0	NA	OFF	OFF	OFF	OFF	OFF	OFF	0
PS1 = 0 or SPNENA = 0 State machine reset									
PS1 = 1, SPNENA = 1	0	NA	OFF	OFF	OFF	OFF	OFF	OFF	0
Start mode, on first positive COMM/EXCOMM edge state machine goes to state #1.									
HIZ = 1	1-6	NA	OFF	OFF	OFF	OFF	OFF	OFF	NOTE
BRAKE = 1	1-6	NA	OFF	ON	OFF	ON	OFF	ON	NOTE

NOTE: POS level corresponds to state

FUNCTIONAL DESCRIPTION (continued)

When a negative BEMF is expected, the POS signal is low and the ZCRS signal is inverted before reaching the LDZ input. In this case the counter will be reloaded when ZCRS is high and allowed to count when it is low.

After PDT clock pulses the counter generates the EOC pulse which advances the state machine causing the outputs to change to the next state. See the Programming the TLS2247 SPM Control section for how to select the PDT value.

SPM SERIAL PORT REGISTER CONTROL BITS (SEE REGISTER DESCRIPTION SECTION)

Register 0

PS1 = 1 and SPNENA = 1: Enables the spindle drivers and enables the state machine.

PS1 = 0 or SPNENA = 0: Disables the spindle drivers and resets the state machine.

COMS = 0: Selects manual/forced commutation using EXCOMM.

COMS = 1: Selects hardware (automatic) state machine advance using the BEMF.

EXCOMM: Manually advances the state machine on positive going edge if COMS = 0, PS1 = 1, SPNENA = 1.

BRAKE = 1: Quickly brakes the motor by enabling all three low-side drivers and disabling all high-side drivers if PS1 and SPNENA are high.

HIZ = 1: Disables spindle drivers without resetting state machine if PS1 = 1. U, V, and W pins go to a high impedance state which allows verification of rotation after manually commutating the motor. The state machine continues to advance and select the 'inactive phase' for BEMF monitoring.

Register 4

PDT(0,11): 12 bit commutation delay count. Valid delay range 1 to 4095.

Manual (Software) Commutation Mode

In manual commutation mode the state machine is advanced by each positive transition of the EXCOMM bit in serial register 0.

To manual commutate the state machine:

1. Write COMS = 0
2. Write EXCOMM = 0
3. Write PS1 = 1, SPNENA = 1
4. Write EXCOMM = 1 (State machine advances)
5. Write EXCOMM = 0
6. Write EXCOMM = 1 (State machine advances)

Once the COMS bit is set high the state machine will advance automatically using the BEMF detect and delay circuit.

FUNCTIONAL DESCRIPTION (continued)

PROGRAMMING THE TLS2247 SPM CONTROL

This section gives a step by step description of how to program the SPM-control section of the TLS2247 (see speed-control covered in FLL SPM Speed Control Circuit section).

1. First power-up the charge pump and SPM control circuitry by entering power save mode 3. Program PS(1) = 0.
2. Initialize Phase Delay Time Register. The phase delay time is usually set to the equivalent of 30 electrical degrees. The delay time needed for 30°e is:

$$T_{delay}\ (sec) = (60/RPM) \bullet (2 / N_p) \bullet (30°/360°) = 10/(RPM\ (N_p)$$

(Equation 3)

where N_p = number of motor poles.

The T_{delay} value can be converted to the number that needs to be programmed into the PDT (phase delay time) register using the following equation:

$$PDT_{value} = T_{delay}\ (sec) / (PRESCALE / f_{OSCIN})$$

(Equation 4)

where f_{OSCIN} is in Hz, and PRESCALE is DT value in Register 0.

Program the PDT_{value} into the PDT bits of Register 4.

NOTE: Slow-slewing delays the commutation point which requires advancing (shortening) the commutation delay by 1/2 the slew time in order to center the commutation on the BEMF.

3. Disconnect the 3-bit DAC from the VCM and connect it to the SPM SPDCAP voltage limit circuit by setting DACS = 0.
4. Select manual current control (no speed control) by setting CCS = 0. This disconnects the SPDCAP pin from the SPM control amplifier and, instead, connects the 3-bit DAC to control the motor current.
5. Wait until charge pump has reached 10 V. (Depends on size of capacitor on Vdd pin, and on f_{OSCIN}).
6. The motor is now ready to start.
7. Select desired current range by setting SPMG high or low.
8. Program desired start current by programming the desired current level into SPMDAC(0-2).
9. Select manual/forced commutation by setting COMS = 0. Also set EXCOMM = 0 at this point.
10. Enable SPM-state machine by setting SPNENA = 1. The output drivers are still in a HIZ at this point.
11. Force the state machine to go to state #1 by setting EXCOMM = 1.
12. Prepare for next forced commutation by setting EXCOMM = 0.
13. Wait desired time according to starting algorithm, then repeat steps 11 and 12 above. Continue this until the starting algorithm is complete.
14. (This step is optional) Once the motor has been manually commutated to a point where the BEMF may be detected the motor can be put in a HIZ mode by setting HIZ = 1. By observing the transitions on the SPDTACH pin it can now be determined if the motor is stuck or if it is rotating. The state machine is not advanced at this point unless the EXCOMM bit is toggled low to high.
15. Once the motor has been manually commutated to a point where the BEMF may be used to reliably commutate the motor the hardware commutation can be enabled by setting COMS = 1. Once COMS = 1 the device will automatically advance the state machine T_{delay} after a zero crossing is detected on the non-exited phase.
16. (This step is optional) Once the motor is in hardware commutation mode it can again be put into to HIZ mode by setting HIZ = 1 and zero crossings may be observed at the SPDTACH pin. In this case the motor is automatically advanced T_{delay} after a zero crossing.
17. At this point closed loop hardware speed control could be enabled (see the FLL SPM Speed Control Circuit section)
18. If it is desired to close the speed control loop externally it can be done using the serial port. Commutation could be controlled by the EXCOMM bit in Register 0 and the speed could be controlled using the 3-bit DAC to set the motor current. Speed feedback is available at the SPDTACH pin where a positive pulse of width, PRESCALE / f_{OSCIN}, will appear once per 60 electrical degrees of motor rotation.

SPINDLE MOTOR CURRENT CONTROL AND COMMUTATION CIRCUITS

This system controls the amplitude and coil current slew rate in a three phase disk drive motor by controlling two phases while in steady state control and all three phases during commutations. Three sense FETs and six drivers (three pair of half H-bridges) are used to sense and control the steady state current through the coils, and control the current slew rate during commutations. The amplitude of the coil current is controlled by the low side drivers which operate in the MOS saturation region unless they are commutating or turned off. The high side drivers operate in the linear (resistive) region with their gates pulled to 5 V above the positive rail, unless they are commutating or turned off. Active clamp circuits limit the output voltage of the three amplifiers to 6.3 V.

A functional diagram of the SPM current control (neglecting commutation) is shown in Figure 13. The input voltage is either from the SPDCAP or the 3-bit DAC, controlled by the CCS bit in Register 0 of the Serial Register. The amplitude of the SPM coil currents is controlled by current mirror amplification. The voltage at the SPDCAP pin (or DAC), which can vary between 1 and 3 V, is first level shifted to vary between 0 and 2 V at the RSS pin. The external resistance at this pin determines the current into the current mirror which is amplified by either high or low gain as controlled by the serial register SPMG bit in Register 0. This resistor thus sets the transconductance gain of the amplifier and current limits to the motor. With proper commutation the motor torque is directly proportional to this current level or:

$$T = K_t I_m \qquad \text{(Equation 5)}$$

the same as for a dc motor. Where K_t is the motor torque constant and I_m is the amplitude of the commutating current into each phase of the motor.

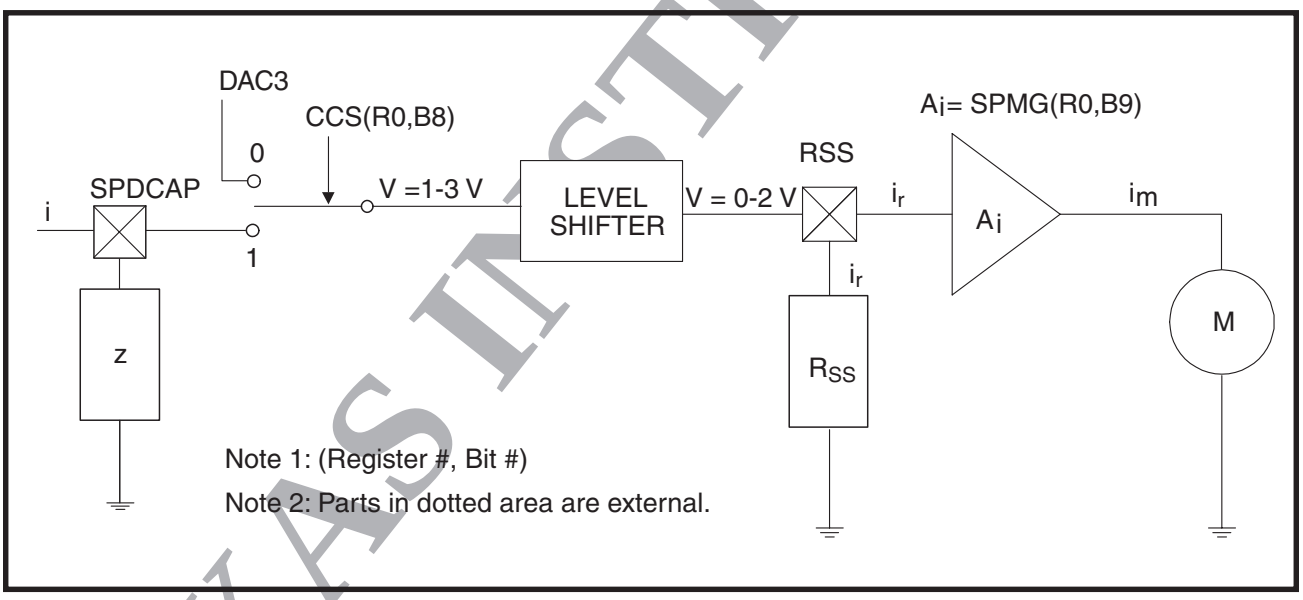


FIGURE 13: SPM Current Control

FUNCTIONAL DESCRIPTION (continued)

The commutating current slew rate is controlled by applying a constant dV/dt to the two motor phases that are turning off. The BEMF over a small region, close to the zero crossing, can also be approximated as a constant dV/dt, so the difference between the BEMF voltage and the phase voltage is approximately a constant voltage. This constant voltage is the voltage between the phase turning off and the center tap of the motor, or the voltage across the inductive part of the winding. A constant voltage across the motor winding (v = LdI/dt) causes a constant dI/dt or current slew rate in that winding. The purpose of controlling the slew rate of the commutating current is to limit the audible noise from the motor caused by this switching current.

FLL SPM SPEED CONTROL CIRCUIT

The speed control circuit for the TLS2247 is shown functionally in Figure 14. It consists of charge and discharge current sources that feed the external network connected to the SPDCAP pin, two sets of identical circuits consisting of a velocity (frequency) comparator and a 15-bit preset counter, and a rotational signal generator.

Each comparator-counter pair controls the current sources for half the time period as determined by the timing signals from the Rotation Signal Generator. The two current sources are individually controlled for four possible values by the VCC bits in Register 3 (see Figure 14 and Register 3 Description). Since the voltage on the SPDCAP pin sets the desired output current level of the spindle motor pre-drive and control circuit, the FLL circuit controls the motor's torque, thus controlling the motor's speed.

Both counters in the FLL are programmed with the same count value from the RSD (Rotational Speed Data) value in registers 2 and 3. The FLL counters are setup as two digital one-shot delays triggered by commutation in a way that will speed locks the motor. Each counter is triggered by the beginning of separate 120° electrical periods of actual motor rotation. The feedback control loop tries to make each of the 120° motor periods equal to the corresponding counter (one shot) periods. See Figure 15 and the Frequency Comparator section for more details.

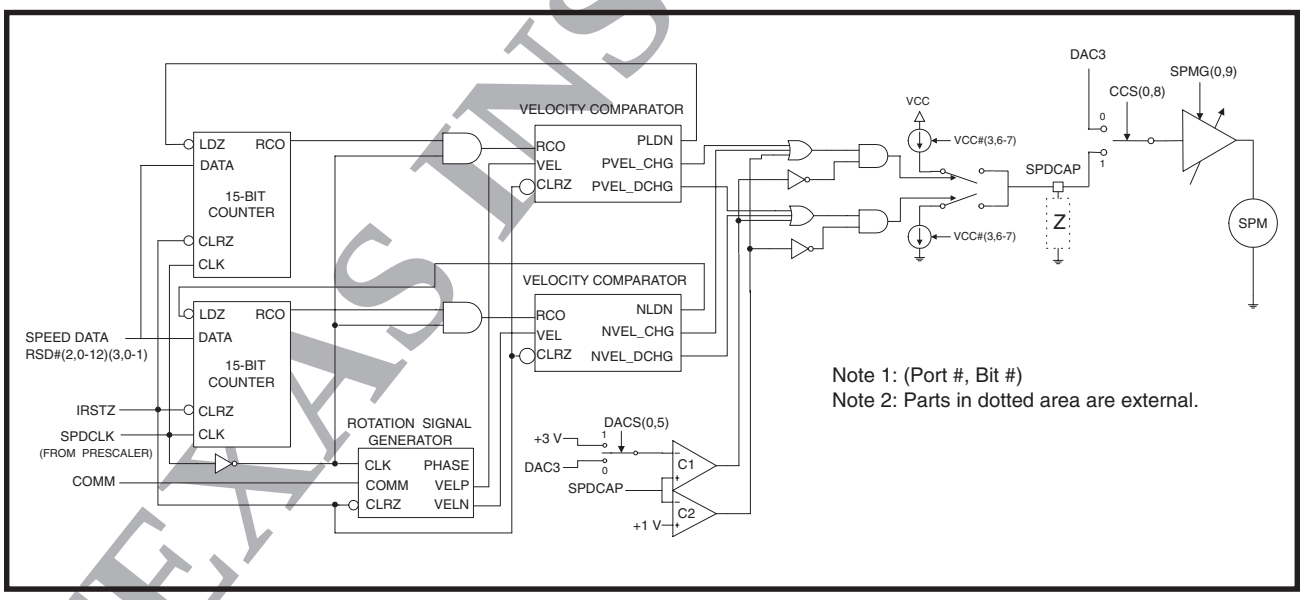


FIGURE 14: FLL Circuit

The count that should be programmed into the counters (RSD) is the number of speed clock cycles in the time taken for the motor to rotate 120° electrical at the desired speed (RPM). It can be calculated as follows:

$$T_{120°} = (60 / RPM) \bullet (2 / N_p) \bullet (120°/360°) = 40/(RPM \bullet N_p)$$

(Equation 6)

$$RSD = T_{120°} \bullet (f_{OSCIN}/PRESCALE)$$

(Equation 7)

where N_p is the number of motor poles and PRESCALE is the programmed prescaler division ratio.

SPDMECH/SPDTACH PIN

This pin has 2 multiplexed signals, SPDMEC or SPDTACH. The selection is done with Register 3, bit 9. SPDMECH is an index signal. It is a 50% duty cycle square wave with a period of once per SPM revolution. SPDTACH is the SPM commutation signal. It has a period of 60° electrical and is identical to the internal COMM signal except that the positive pulse is 6 SPDCLK bits wide. For an 8 pole motor there are 24 SPDCLK pulses per revolution.

The normal mode of operation of the FLL and Speed Error circuit, that uses the delayed BEMF zero crossings to measure the motor speed, requires that SPDTACH (P4,B12) bit is reset. In this case the COMM signal, described in the Spindle Control Logic section, is connected to the FLL circuits as shown in Figure 14 and to the SPDTACH pin as an output signal.

If the SPDTACH bit is set the SPDTACH pin is an input signal which is connected in place of the COMM signal shown in Figure 14. This mode can be used where it is desirable to use speed information from the disk sector data rather than from the BEMF. The waveform applied to the SPDTACH pin should have a positive edge for every 60° electrical of actual rotor rotation ($6N_p/2$ pulses per rev).

SPDCAP VOLTAGE CLAMP

The voltage on SPDCAP is effectively limited to from 1 V to 3 V by the comparator circuits, C1 and C2, in Figure 14. If either limit is reached the corresponding comparator output goes high which disconnects the current source connected to SPDCAP that is causing the problem and forces the opposite polarity current source to be on.

When DACS is low during startup, the DAC is used as the C1 limit voltage instead of the 3 V reference. This indirectly sets the SPDCAP voltage since the speed control is limiting during acceleration. However, since CCS is low at this time, the SPDCAP is not connected to the motor drive control. Instead, the CCS signal connects the 3-bit DAC to control the motor current. When the motor is close to operating speed, the CCS signal is set high connecting the SPDCAP to the motor drive control which allows the speed control to operate the motor. Since the 3-bit DAC is still connected to the limit circuit it can be used in a way that limits speed overshoot. Once the motor speed is stabilized, DACS is set high, which switches the DAC from the SPM limit circuit to the VCM where it is used as an offset compensation. The SPM current limit is now set to the maximum current for the selected range by the 3 V reference.

FREQUENCY COMPARATOR

A typical frequency comparator timing diagram is shown in Figure 15. The frequency control circuit in Figure 14 consists of two identical frequency (velocity) comparator (or detector) circuits. They compare the frequency of two input signals, f_{ref} and f_{fb}. The output is ideally proportional to the difference. The update rate for each of the frequency comparator circuits is once every 240° electrical degrees of motor rotation and the current output of each is summed at the SPDCAP pin. The total output over the full 240° period is thus twice the output of one of the frequency detectors or, in other words, the overall detector gain is twice the gain of one detector over the 240° period.

The two frequency comparator circuits work on different 120° halves of the 240° cycle as determined by the complimentary VELP and VELN signals derived from the COMM motor feedback signal. The frequency of these two signals is one fourth the frequency of the COMM signal and 180° out of phase with each other. So another way to look at the system is that each detector is trying to control its corresponding half period of the feedback signal. And this is the same as saying the overall detector gain is equal to either detector gain over a 120° period. This makes the effective update rate twice per 240° period which is equivalent to once per 120° period.

FREQUENCY COMPARATOR (continued)

Since the two frequency comparators are identical only the one connected to VELN signal, the bottom circuit in Figure 14, is described in detail. The VELP signal is just the compliment of the VELN signal so that everything for the other circuit is the same but shifted by 120°.

Each frequency comparator circuit consists of a single 15-bit counter and a velocity comparator circuit. The VELN signal is the COMM (motor commutation signal) divided by 4 which means that it goes high on every fourth COMM pulse. This represents the feedback motor speed in terms of frequency. The pulse width of the VELN signal is thus equivalent to the rotor moving 120° electrical or the full period is 240° electrical. The count length of the 15 bit counter is programmed (by RSD) to be equivalent to the time for a 120° electrical of desired rotor movement.

Once the velocity comparator circuit receives a positive going edge on VELN, the counter is started and at the same time it sets the NLDZ flop. The counter produces an end of count signal (RCO) after a fixed time equivalent to the desired 120° electrical period which resets the NLDZ flop. The NLDZ signal can be looked at as a digital, fixed period, one-shot triggered on every fourth COMM pulse. This is the feedback signal into the frequency detector. It is easily shown that the average DC level of this signal is proportional to its frequency which is proportional to the motor speed. Since this signal is one of the inputs to the phase detector which controls the current source of value I_{cs} connected to the SPDCAP pin, its amplitude is effectively I_{cs}.

The resulting average current into the SPDCAP pin due to the feedback signal alone is:

$$(I_{dc})_{fb} = I_{cs} \bullet (T_{ref}/t_{fb} = I_{cs} \bullet T_{ref} \bullet f_{fb} = (I_{cs}/f_{ref})\, f_{fb}$$

(Equation 8)

Where I_{dc} is the average NLDZ signal of amplitude I_{cs},T_{ref} is the constant time period of 120° electrical, and f_{fb} is the feedback frequency from the motor.

The net current into the SPDCAP pin is the sum of this current and that due to the reference signal.

The two signals, N_VEL_CHG and N_VEL_DCHG, control the connection of the corresponding charge and discharge current source to the SPDCAP pin. These signals are FF outputs. The CHG FF is set when the trailing (negative) edge of the VELN signal lags the trailing edge of the NLDZ signal and the DCHG FF is set when the trailing edge of the VELN signal leads the trailing edge of the NLDZ signal. Thus it is seen that the CHG FF is set when the feedback frequency is low (slow) and the DCHG FF is set when the feedback frequency is high (fast). Since the peak motor current (and torque) is directly proportional to the voltage at the SPDCAP pin, the CHG FF tries to speed up the motor and the DCHG FF tries to slow it down.

Both flip flops are reset whenever both are set simultaneously. This means that when one is set first it resets as soon as the other one tries to set.

If the motor is running at the correct speed, the negative edges of the VELN and NLDZ signals coincide and each FF sets at the same time and immediately resets.

The other velocity compare circuit functions the same way on the positive half of the VELP signal which is the same as the negative half of the VELN signal. P_VEL_CHG and P_VEL_DCHG are generated that tend, respectively, to speed up and slow down the spindle motor. So it is seen that each half of the 240° feedback signal (VELN or VELP) is controlled separately by the 120° reference pulse of the counter such that they are equal to 120° electrical of motor rotation at the commanded speed.

It can be shown that the average value of each frequency Detector output is proportional to the difference between the reference frequency ($1/T_{ref}$) and the feedback frequency. In this case the feedback frequency period is 120° electrical or half the period of the VELN or VELP signals.

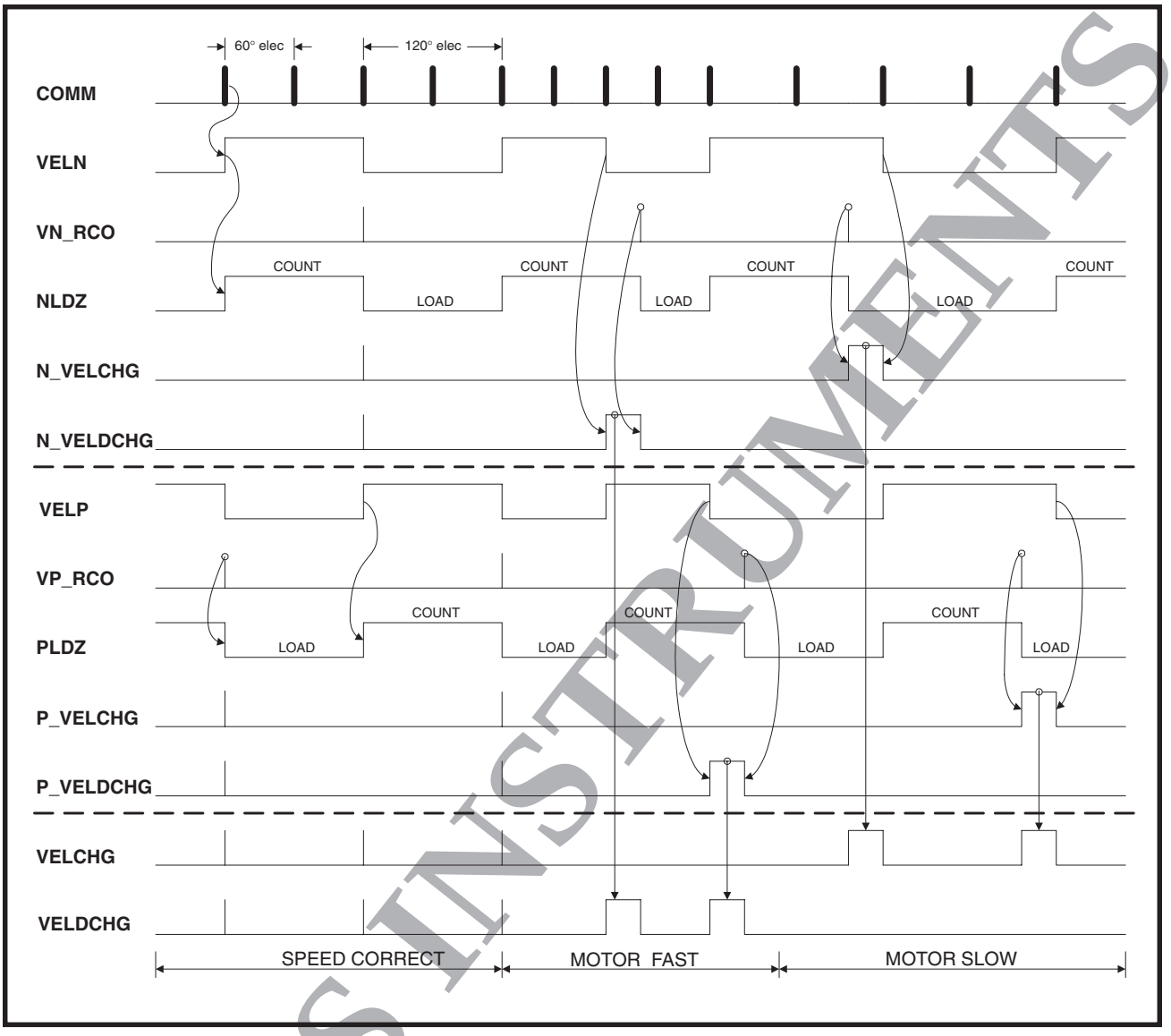


FIGURE 15: Frequency Comparator Timing

FUNCTIONAL DESCRIPTION (continued)

FREQUENCY COMPARATOR GAIN FACTOR

The gain function of the frequency detector block (Average DC current output per cycle of frequency difference) is:

$$G_{fd} = I_{cs}/f_{ref} = I_{cs}\, T_{ref} \text{ in amps per Hz}$$

(Equation 9)

I_{cs} is the current source programmed to the SPDCAP pin, and T_{ref} is $T_{120°}$ given in Equation 6.

G_{fd} is defined by:

$$I_{dc}(\text{amps}) = G_{fd}(f_{ref} - f_{fb})$$

(Equation 10)

I_{dc} is the average DC current at the SPDCAP pin.

SPDCAP PIN COMPENSATION NETWORK

To have a true frequency lock loop speed control where there is no average frequency error there must be an integrator in the forward loop. The only place to do this in the TLS2247 is at the SPDCAP pin. If a simple capacitor is used the system is unstable. A more complex network must be used. The simplest of these is a lead-lag network consisting of one resistor and two capacitors as shown in Figure 16.

Since the SPDCAP pin is fed from a current source the transfer function of current to voltage is just the complex impedance to ground which is also given in Figure 16. Normally this network is designed to make the overall open loop transfer function cross the zero db point at the desired loop bandwidth and to cross at a slope of 20 dB/decade. The two break frequencies of the network are normally chosen such that the zero db point Is at the geometric mean of the two and the ratio of f_2 to f_1 is about 10. This usually will result in enough phase margin for a stable system but other performance factors may need to be considered. Since this system is actually a sampled data system, one criteria for the closed loop band width is that it should be at most 1/5 of the sampling rate to avoid excessive sampled data lag. This allows the system to be treated as a linear system.

SPEED CONTROL SERVO LOOP BLOCK DIAGRAM

An overall speed control system block diagram is shown in Figure 17. The reference frequency, f_{ref}, is $1/T_{120}$ given in Equation 6. G_{fd} is the frequency discriminator gain factor and is given in the Frequency

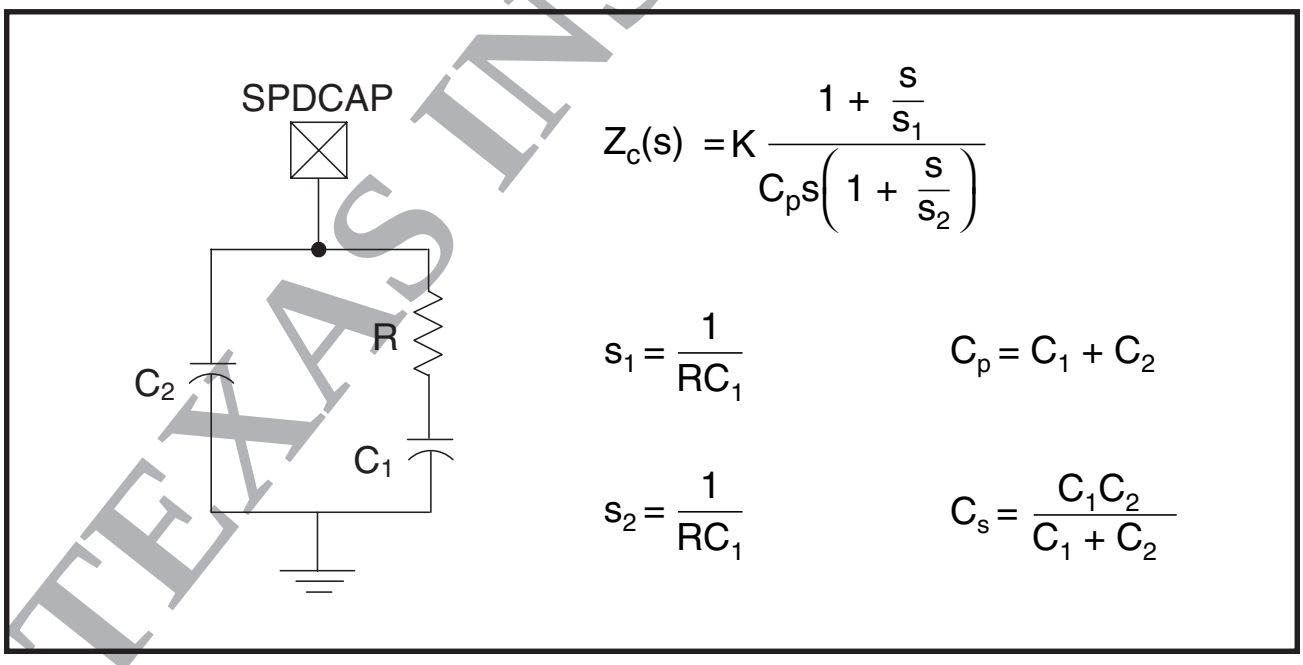


FIGURE 16: Lead-Lag Compensation Network

Comparator Gain Factor section. The motor transfer function, G_m, can usually be simplified to K_t/Js when the viscous damping constant, K_d, is small. $Z_c(s)$ is the compensation network connected to the SPDCAP pin as discussed in the SPDCAP Pin Compensation Network section. R_{ss} is the resistor connected to the RSS pin which is 2 kΩ for nominal output current ranges. The power amplifier current gain, G_a, is selectable through the serial port as either 375 or 1500. The lower gain corresponding to the 375 mA output current range is sufficient for most HDD motors.

The generalized open loop gain is given in Equation 11. The open loop transfer function for this system using a compensation network as in the SPDCAP Pin Compensation Network section is:

$$GH(s) = K\frac{1 + \frac{s}{s_1}}{s^2\left(1 + \frac{s}{s_2}\right)} \qquad K = \frac{30\, G_a K_t I_{cs}}{\pi (RPM) R_{ss} J_l Cp}$$

$$s_1 = \frac{1}{RC_1},\ C_p = C_1 + C_2 \qquad s_2 = \frac{1}{RC_s},\ C_s = \frac{C_1 C_2}{C_1 + C_2}$$

(Equation 11)

For these equations K_t is the motor torque constant in Nm/A, J_L is the load moment of inertia in Kgm^2, G_a is the programmed power amplifier current gain and I_{cs} is the programmed charge and discharge current which are assumed equal.

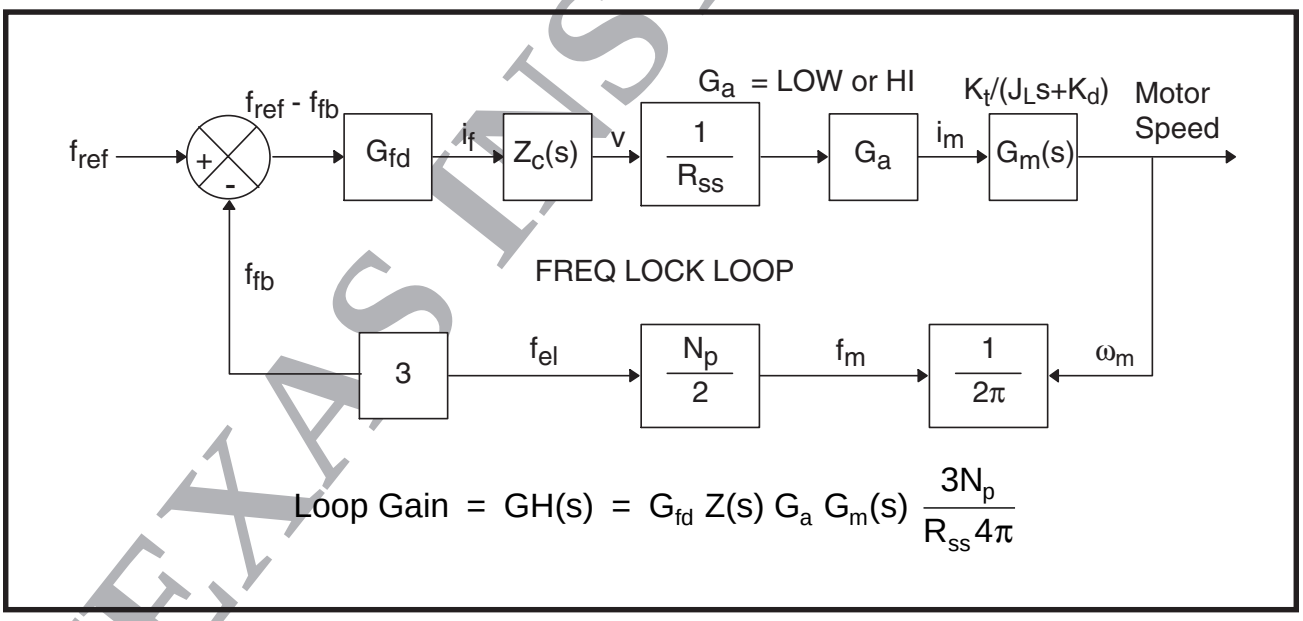


FIGURE 17: Speed Control Block Diagram

REGISTER DESCRIPTION

TABLE 2: REGISTER SELECTION

REGISTER #	PT3	PT2	PT1	DESCRIPTION
0	0	0	0	SPM control circuit mode set/power save control
1	0	0	1	3-bit DAC
2	0	1	0	Rotation control 1
3	0	1	1	Rotation control 2/slew rate/FLL current control
4	1	0	0	Phase delay control/SPDTACH I/O CTRL
6	1	1	0	Programmable PES gain and window threshold

REGISTER 0 DEFINITION (SPM CONTROL CIRCUIT MODE SET/POWER SAVE CONTROL)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	PS0		Enable VCM
1	PS1		Enable SPM
2	SPNENA	Spindle	SPM ENABLE
3	0		TI reserved (always set to 0)
4	COMS	Spindle	1: Hardware (BEMF) 0: Software (EXCOMM)
5	DACS	Spindle	Select FLL clamp 1: 3 V 0: 3-bit DAC
6	BRAKE	Spindle	Dynamic brake 1: Enable 0: Disable
7	HIZ	Spindle	All phases Hi-Z 1: Enable 0: Disable
8	CCS	Spindle	FLL mode control 1: FLL 0: 3-bit DAC
9	SPMG	Spindle	Current gain select 1: GAIN1 0: GAIN0
10	DT0	Spindle	OSCIN prescaler divider 0 (see Table 4)
11	DT1	Spindle	OSCIN prescaler divider 1 (see Table 4)
12	EXCOMM	Spindle	Manual state machine advance
13	PT1 = 0		Register select address 1 (see Table 7)
14	PT2 = 0		Register select address 2 (see Table 7)
15	PT3 = 0		Register select address 3 (see Table 7)

TABLE 3: POWER SAVE MODE SELECT IN REGISTER 0

MODE SELECT	PS1	PS0	RESET CIRCUIT, CHARGE PUMP, 3.3 V REGULATOR, AND BANDGAP REFERENCE	SPM CIRCUIT	VCM CIRCUIT
MODE1	0	0	ON	OFF	OFF
MODE2	1	0	ON	ON	OFF
MODE3	1	1	ON	ON	ON

TABLE 4: PRESCALER SETTING IN REGISTER 0

DT1	DT0	RATIO
0	0	1
0	1	2
1	0	4
1	1	8

REGISTER 1 DEFINITION (3-BIT DAC/SPM CONTROL)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	SPMDAC0	Spindle	3-bit DAC data (LSB)
1	SPMDAC1	Spindle	3-bit DAC data
2	SPMDAC2	Spindle	3-bit DAC data
3	SPMCAS	Spindle	1: Cascode enable 0: Cascode disable To improve rotation speed control accuracy in RUN mode
4-6			
7	0		TI reserved (always set to 0)
8	0		TI reserved (always set to 0)
9	FLTZCRSENA	Spindle	0: SPDTACH 1: FILTERED BEMF
10	0		TI reserved (always set to 0)
11	0		TI reserved (always set to 0)
12	0		TI reserved (always set to 0)
13	PT1 = 1		Register select address (see Table 7)
14	PT2 = 0		Register select address (see Table 7)
15	PT3 = 0		Register select address (see Table 7)

REGISTER DESCRIPTION (continued)

REGISTER 2 DEFINITION (ROTATION CONTROL 1)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	RSD2	Spindle	Rotation speed data (see Note 1)
1	RSD3	Spindle	Rotation speed data
2	RSD4	Spindle	Rotation speed data
3	RSD5	Spindle	Rotation speed data
4	RSD6	Spindle	Rotation speed data
5	RSD7	Spindle	Rotation speed data
6	RSD8	Spindle	Rotation speed data
7	RSD9	Spindle	Rotation speed data
8	RSD10	Spindle	Rotation speed data
9	RSD11	Spindle	Rotation speed data
10	RSD12	Spindle	Rotation speed data
11	RSD13	Spindle	Rotation speed data
12	RSD14	Spindle	Rotation speed data (MSB)
13	PT1 = 0		Register select address (see Table 7)
14	PT2 = 1		Register select address (see Table 7)
15	PT3 = 0		Register select address (see Table 7)

Note 1: RSD L.O. bits are in Register 3

REGISTER 3 DEFINITION (SLEW RATE/FLL CURRENT CONTROL)

0	RSD0	Spindle	Rotation speed data (see Note 2)
1	RSD1	Spindle	Rotation speed data
2	0		TI reserved (always set to 0)
3	0		TI reserved (always set to 0)
4	0		TI reserved (always set to 0)
5	0		TI reserved (always set to 0)
6	VCC0	Spindle	Velocity current control data (chg/dischg) (see Table 7)
7	VCC1	Spindle	Velocity current control data (chg/dischg) (see Table 7)
8	0		TI reserved (always set to 0)
9	SPDTACH/	Spindle	Selects multiplexed output 0: SPDMEC 1: SPDTACH
10	SR	Spindle	Slew rate 1: on (slow) 0: off (fast)
11	0		TI reserved (always set to 0)

REGISTER 3 DEFINITION (SLEW RATE/FLL CURRENT CONTROL) (continued)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
12	0		TI reserved (always set to 0)
13	PT1 = 1		Register select address (see Table 7)
14	PT2 = 1		Register select address (see Table 7)
15	PT3 = 0		Register select address (see Table 7)

NOTE 2: RSD H.O. bits are in Register 2

TABLE 5: FLL Speed Control Charge/Discharge Current Source In Register 3

VCC1	VCC0	VELOCITY CHARGE CURRENT
0	0	100 μA
0	1	200 μA
1	0	400 μA
1	1	800 μA

REGISTER 4 DEFINITION (PHASE DELAY CONTROL)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	PDT0	Spindle	Phase delay time data (LSB)
1	PDT1	Spindle	Phase delay time data
2	PDT2	Spindle	Phase delay time data
3	PDT3	Spindle	Phase delay time data
4	PDT4	Spindle	Phase delay time data
5	PDT5	Spindle	Phase delay time data
6	PDT6	Spindle	Phase delay time data
7	PDT7	Spindle	Phase delay time data
8	PDT8	Spindle	Phase delay time data
9	PDT9	Spindle	Phase delay time data
10	PDT10	Spindle	Phase delay time data
11	PDT11	Spindle	Phase delay time data (MSB)
12	SPDTACH	Spindle	SPDTACH I/O Select 1: Input 0: Output
13	PT1 = 0		Register select address (see Table 7)
14	PT2 = 0		Register select address (see Table 7)
15	PT3 = 1		Register select address (see Table 7)

REGISTER DESCRIPTION (continued)

REGISTER 5 DEFINITION-RESERVED FOR TI USE ONLY (SEE NOTE 1)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0-12	T0-T12		Reserved (always set to 0)
13	PT1 = 1		Register select address (see Table 7)
14	PT2 = 0		Register select address (see Table 7)
15	PT3 = 1		Register select address (see Table 7)

NOTE 1: To access this register, bit 3 of Register 0 must be high (1)

REGISTER 6 DEFINITION: TRACKING LOOP SUPPORT

0	PESGN0	VCM	PES amplifier programmable gain
1	PESGN1	VCM	PES amplifier programmable gain
2	PESGN2	VCM	PES amplifier programmable gain
3	PESGN3	VCM	PES amplifier programmable gain
4	PESGN4	VCM	PES amplifier programmable gain
5	MUX	VCM	1: CPES_OUT 0: COMP_OUT
6	ENVCM	VCM	0: Disable actuator amplifier 1: Enabled
7	ENNCP	VCM	0: Disable negative clamp 1: Enabled
8	WTHRES0	VCM	Programmable window threshold
9	WTHRES1	VCM	Programmable window threshold
10	WTHRES2	VCM	Programmable window threshold
11	WTHRES3	VCM	Programmable window threshold
12			
13	PT1 = 0		Register select address (see Table 7)
14	PT2 = 1		Register select address (see Table 7)
15	PT3 = 1		Register select address (see Table 7)

TABLE 6: ENVCM Control Logic

PS0	PS1	ENVCM	DESCRIPTION
1	1	0	VCM loop is disabled
1	1	1	VCM loop is enabled

TABLE 7: Internal Register Summary

BIT #	REGISTER0	REGISTER1	REGISTER2	REGISTER 3	REGISTER 4	REGISTER 5	REGISTER 6
0	PS0	SPMDAC0	RSD2	RSD0	PDT0	0	PESGN0
1	PS1	SPMDAC1	RSD3	RSD1	PDT1	0	PESGN1
2	SPNENA	SPMDAC2	RSD4	0	PDT2	0	PESGN2
3	0	SPMCAS	RSD5	0	PDT3	0	PESGN3
4	COMS		RSD6	0	PDT4	0	PESGN4
5	DACS		RSD7	0	PDT5	0	MUX
6	BRAKE		RSD8	VCC0	PDT6	0	ENVCM
7	HIZ	0	RSD9	VCC1	PDT7	0	ENNCP
8	CCS	0	RSD10	0	PDT8	0	WTHRES0
9	SPMG	FLTZCRSENA	RSD11	SPDTACH/MEC	PDT9	0	WTHRES1
10	DT0	TI Test	RSD12	SR	PDT10	0	WTHRES2
11	DT1	TI Test	RSD13	0	PDT11	0	WTHRES3
12	EXCOMM	TI Test	RSD14	0	SPDTACH	0	
13	PT1 = 0	PT1 = 1	PT1 = 0	PT1 = 1	PT1 = 0	PT1 = 1	PT1 = 0
14	PT2 = 0	PT2 = 0	PT2 = 1	PT2 = 1	PT2 = 0	PT2 = 0	PT2 = 1
15	PT3 = 0	PT3 = 0	PT3 = 0	PT3 = 0	PT3 = 1	PT3 = 1	PT3 = 1

PIN DESCRIPTION (continued)

Pin types are defined as: A = Analog; D = Digital; G = Ground; I = Input; O = Output; P = Power

The pin functions are listed in the following tables and are grouped by function.

SUPPLIES (NOTE)

PIN #S	NAME	TYPE	DESCRIPTION
40	AVCC	P	5 V analog power supply
8	DVCC	P	5 V digital power supply
51	VCMVCC	P	VCM power supply (2 bond pads)
14,18	SPNVCC	P	Spindle power supply (2 bond pads)
*1,12, *28,*29, 42,*56	AGND	A/G	Analog ground
10	DGND	D/G	Digital ground
48	VCMGND	G	VCM ground (2 bond pads)
16,20	SPNGND	G	Spindle ground (2 bond pads)
32	REGVCC	A	3.3 V regulator DC Input
30	REGGND	A	3.3 V regulator ground
2	VPP	P	5 V power supply and EEPROM programming voltage

NOTE: In the above table the symbol (*) indicates that additional pins can be used for heat sinking

MISCELLANEOUS

7	OSCIN	D/I	Charge pump and commutating clock
27	RBIAS	A	Internal bias current setting
41	VDD	A	Charge pump capacitor pin

VOLTAGE MONITOR

25	CPOR	A	Power-on reset delay capacitor
26	RSTZ	D/O	Power-on reset output and input

SERIAL PORT

4	SCLK	D/I	Serial port input clock
5	SDATA	D/I	Serial port data
6	SENA	D/I	Serial port select (active H)

VCM

PIN #S	NAME	TYPE	DESCRIPTION
21	RETOUT	A	Retract drive output
22	CRETIN	A	Retract drive capacitor voltage input
38	COMPI	A	VCM current loop compensation filter
39	CMPO	A	VCM current loop compensation filter
44	VREFOUT	A	VCM reference voltage output
43	VREFC	A	VCM reference voltage capacitor input
45	RSENP	A	Positive VCM current loop sense
46	RSENN	A	Negative VCM current loop sense
47	FBOUT	A	Current sense amplifier output
49	VCMB	A	VCM driver output B
50	VCMA	A	VCM driver output A

TRACKING LOOP SUPPORT

33	COMP_OUT	A	Tracking loop compensation output
34	COMP_IN	A	Tracking loop compensation input
35	CPES_OUT	A	Composite position error output
36	COMP_SUM	A	Loop compensation summing point
37	CPES_IN	A	Position error input
52	WINOUT	D	Window comparator output
54	TF	D	Track following control input
55	SAMPLE	D	Sample position error/hold

SPINDLE MOTOR

3	SPDMEC/ SPDTACH	D/O	Spindle speed mech output/tachometer output
9	SPDCAP	A	Speed loop compensation network connection
11	CTS	A	Center tap sense
15	U	A	Spindle phase U output
17	V	A	Spindle phase V output
19	W	A	Spindle phase W output
23	RSS	A	Maximum SPM current limiting resistor
24	SPNCAP	A	Spindle slew rate control cap

PIN DESCRIPTION (continued)

3.3 V REGULATOR

PIN #S	NAME	TYPE	DESCRIPTION
31	VREG	A	3.3 V regulator output

OTHER PINS

13			No Connects
53			Reserved

MECHANICAL DATA

The SSI 34H3307 mechanical outline dimensions are shown below. (TBR)

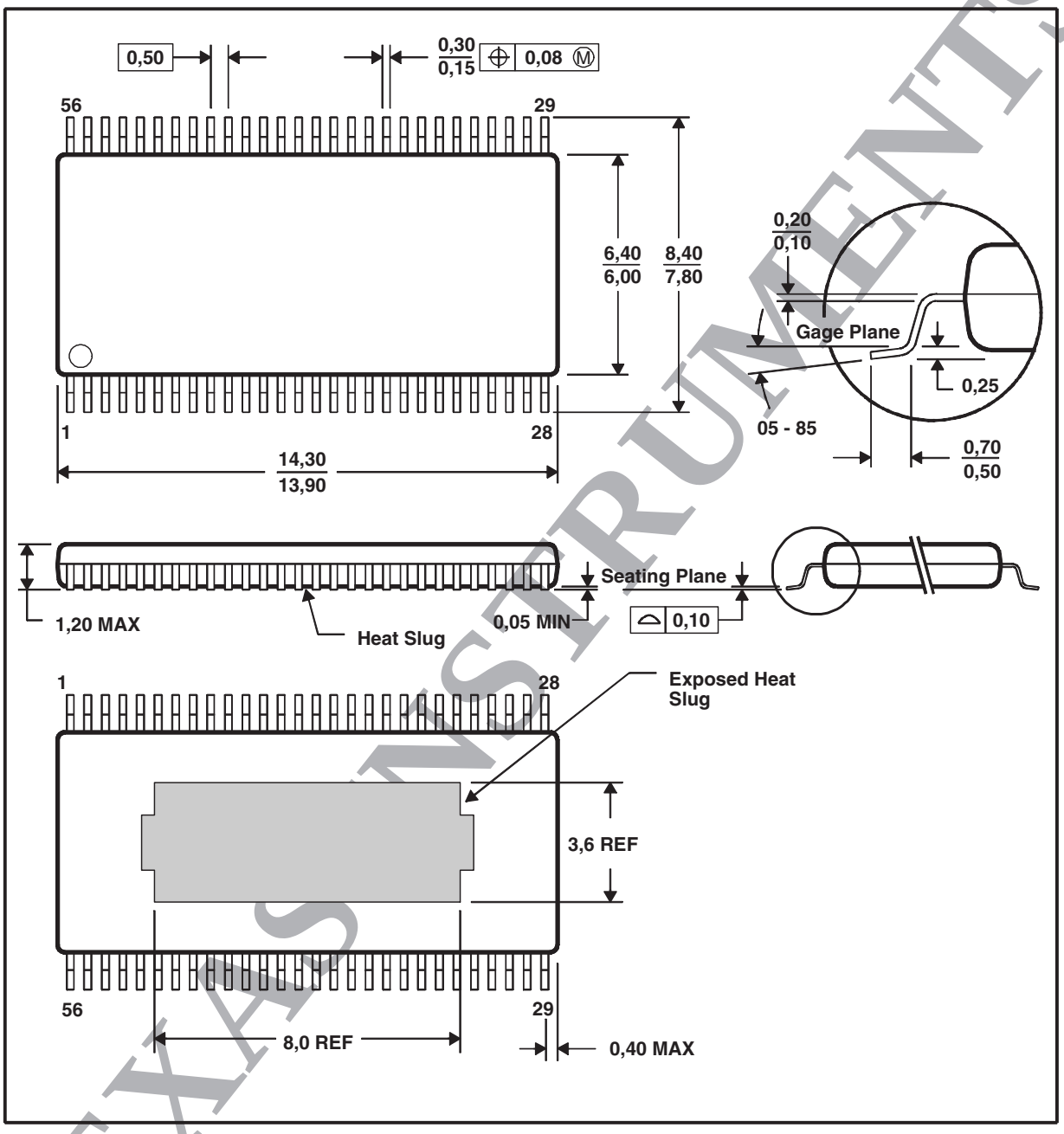


FIGURE 19: Mechanical Data

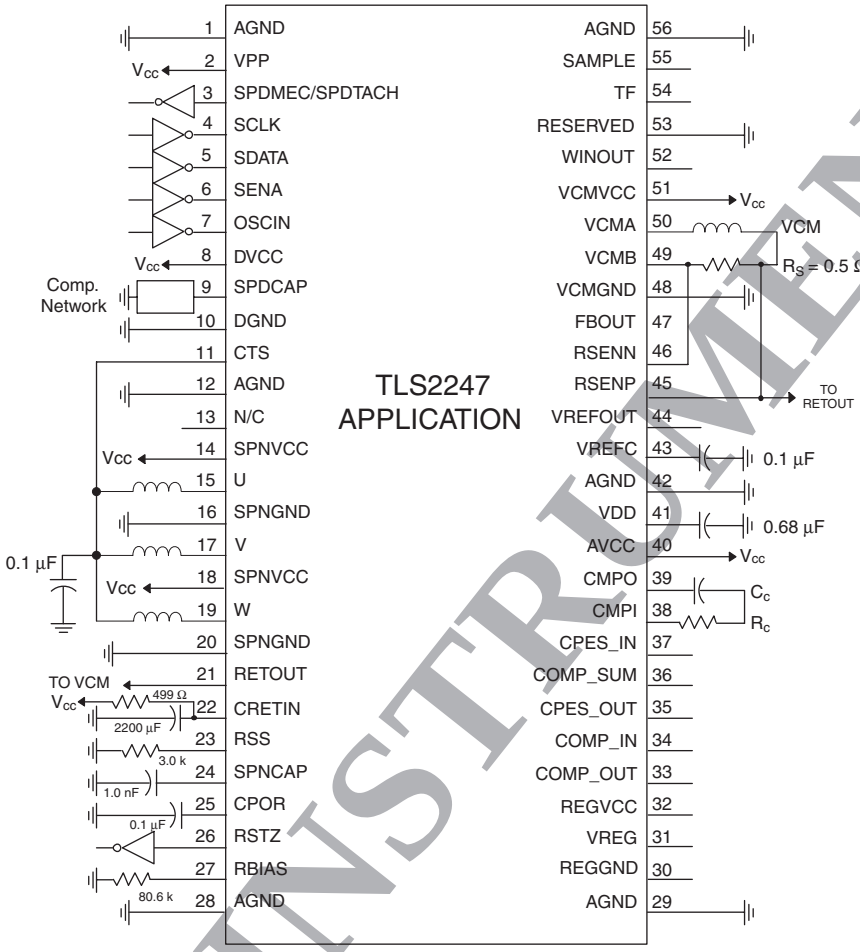
NOTES: A. All linear dimensions are in millimeters

B. This drawing is subject to change without notice

C. Thermally enhanced molded plastic package with a exposed heat slug (HSL) on bottom

PACKAGE PIN DESIGNATIONS

(Top View)



56-Pin Package

CAUTION: Use handling procedures necessary for a static sensitive component.

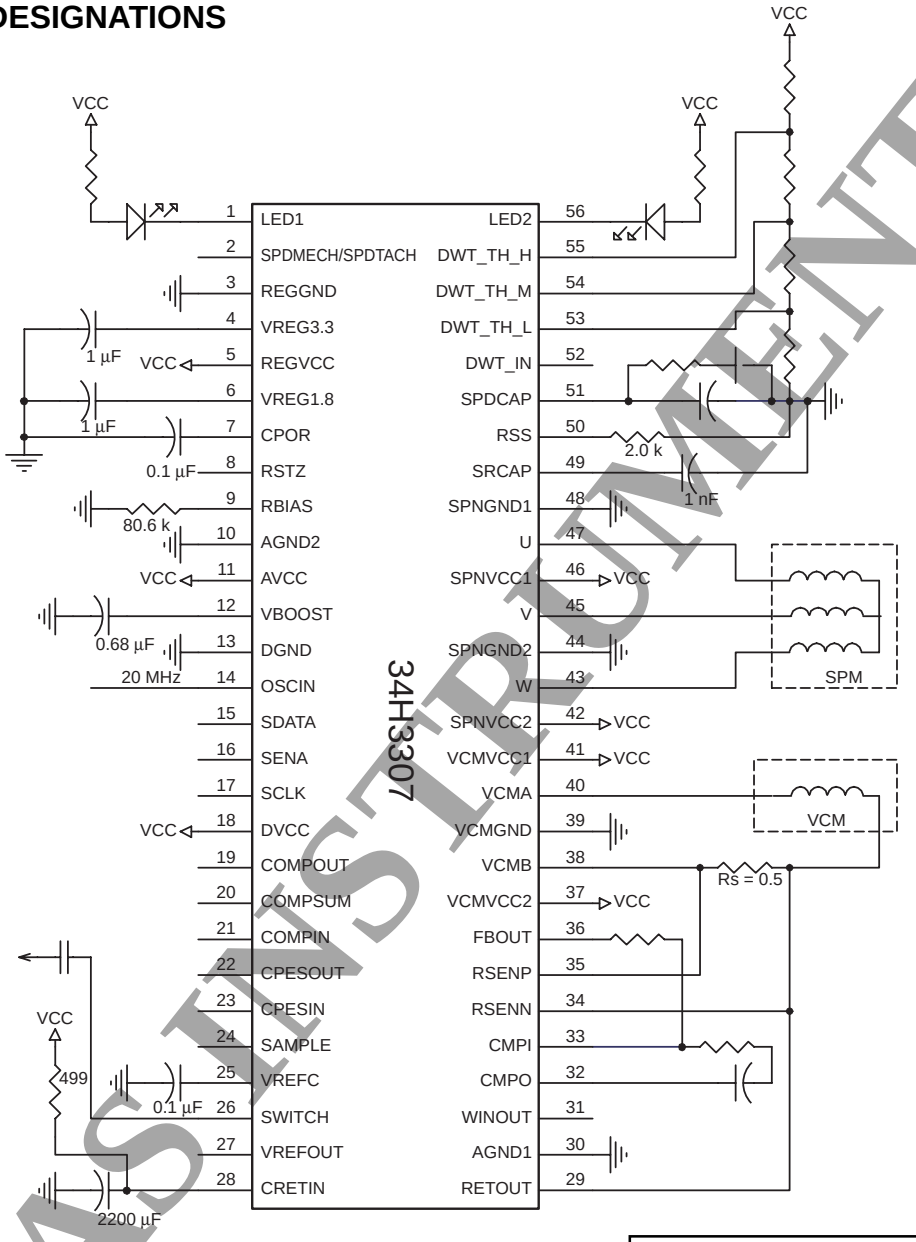
ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
TLS2247	56-Pin TSSOP	TLS2247DCA	TLS2247

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

PACKAGE PIN DESIGNATIONS

(Top View)



56-Pin Package

CAUTION: Use handling procedures necessary for a static sensitive component.

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

Abridged Version

SSI 34P3211B
Read Channel for Tape Storage

August1999

DESCRIPTION

The SSI 34P3211B is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement zoned recording for high density tape storage applications. Functional blocks include the pulse detector, programmable filter, time base generator, and data synchronizer. VCO range of 0.6 MHz to 13 MHz is selectable through the serial port.

Programmable functions of the SSI 34P3211B device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 34P3211B utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption. The SSI 34P3211B supports a sleep mode for minimal power dissipation in non-operational periods.

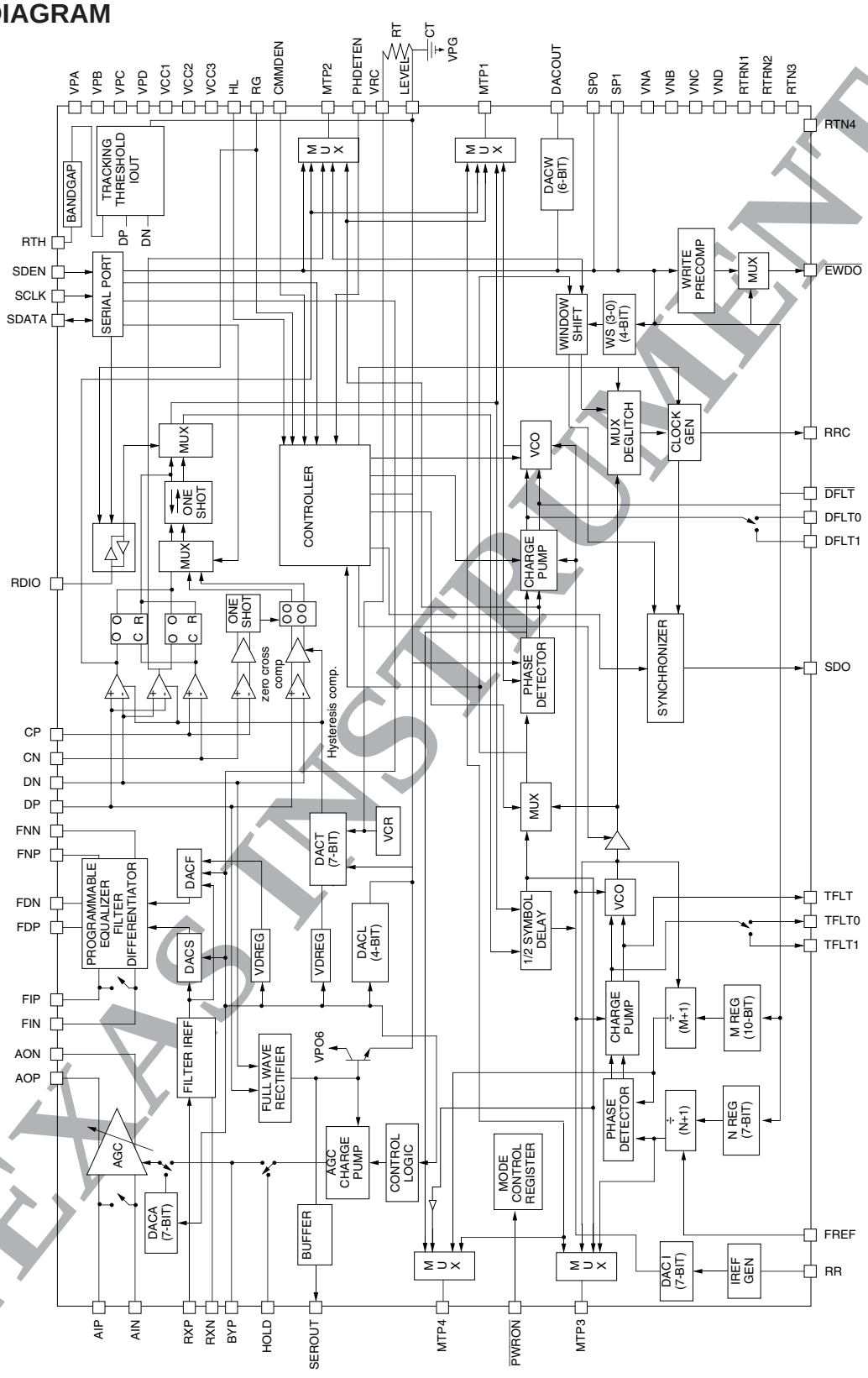
The SSI 34P3211B is available in a 64-Lead TQFP package.

FEATURES

- **Complete zoned recording application support**
- **VCO range: 0.6 MHz to 13 MHz selectable through the serial port**
- **Supports 1,7 RLL, MFM, FM, and GCR Encoding Format**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Programmable cutoff frequency of 0.4 to 4 MHz**
- **Tracking Threshold for rapid LEVEL discharge**
- **Time base generator with better than 1% frequency resolution**
- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data synchronizer with programmable window shift control**
- **Programmable write precompensation**
- **Write current DAC**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode < 5 mW)**
- **Low Operating Power (500 mW typical @ 5 V)**

SSI 34P3211B
Read Channel for
Tape Storage

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 34P3211B implements a high performance complete read channel, including pulse detector, programmable active filter, time base generator, data synchronizer, and VCO range of 0.6 MHz to 13 MHz.

PULSE DETECTOR

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier, a precision wide bandwidth full wave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC Circuit

The gain of the AGC amplifier is controlled by the voltage (VBYP) stored on the BYP hold capacitor (CBYP). A dual rate charge pump drives CBYP with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower VBYP which reduces the amplifier gain, while decay currents increase VBYP which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the correct AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the correct AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 μA acts to increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA : 4 μA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 21.

When the chip is in power down mode, the AGC dual rate charge pump is disabled.

The AGC amplifier can be set into a fixed gain mode. The gain is programmable over a 2 to 51 V/V range in 0.4 V/V steps by a 7-bit DAC (DACA). If DACA = 0, the amplifier is in AGC mode.

BYP Control Voltage

The BYP capacitor voltage will be held constant (subject to leakage currents) during sleep mode, write mode, or when the HOLD signal is high. Upon the transition of $\overline{\text{PWRON}}$ from high to low, there is a 1 μs delay inserted before the AGC charge pump is allowed to drive the BYP capacitor.

AGC Mode Control

When the pulse detector is powered-down, VBYP will be held constant subject to leakage currents only. Upon power-up, the Low-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor.

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, VBYP will be held constant subject to leakage currents only.

Fwr Output

A buffered output of the full wave rectifier is provided at the SEROUT pin. A 1 Vp-p signal at DP-DN will result in a 0.75 Vpk full wave rectified signal at SEROUT.

PULSE DETECTOR (continued)

RDIO Output Pin

The RDIO output is a CMOS compatible output that is selectable between a 30 ns wide Raw Data signal and the RDQ signal, i.e. Q in Figures 1A and 1B. RDQ is the output of a Toggle Flip Flop which is clocked by the Raw Data output signal. The signal at this pin is controlled through several bits in the serial port as shown in Table 1.

When RG = 0, either Read Data Output or RDQ will appear at RDIO depending on R21 Bit D7. When RG = 1, RDIO depends on several bits as shown above. With RG = 1 and R21 Bit 6 = 1, then RDIO will be in HIZ mode. With RG = 1 and R21 Bit 6 = 0, then R20 Bit 7 determines if a signal appears on RDIO: that signal will be either Read Data Output or RDQ depending on R21 Bit 7.

Qualifier Selection

The SSI 34P3211B provides both hysteresis and dual comparator pulse qualification circuits that may be selected for read mode operation. The dual comparator method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the hysteresis level of the comparators for read mode. The option of using a fixed threshold is also provided. R34 bit 4 allows the user to set the data threshold as fixed or driven by the LEVEL pin. If set as fixed the threshold is set as if the DP/DN amplitude is 1 Vp-pd. Whether fixed or floating the threshold is set by the DACT value in the DTCR. The formula for the threshold level is shown below.

Thresh = DACT • 0.93/127 (for $38 \leq$ DACT ≤ 109)

Dual Comparator Qualification

When in dual comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The floating hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by LEVEL and referenced to VRC. Hysteresis thresholds from 30 to 80% may be set with a resolution of 1%. An external resistor/capacitor combination (RT/CT) sets the hysteresis threshold time constant. An internal DAC, DACL, can also be used to discharge the LEVEL pin. The four LSBs of the Hysteresis Decay Control Register (HDCR) determine the value of the pull-down current. The LSB value of DACL is 3.125 µA, and DACL is offset by 1 LSB such that "0000" corresponds to 3.125 µA, and "1111" results in 50 µA. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot. Dual comparator timing is shown in Figure 1A.

TABLE 1: RDIO Control

RG	Reg 12 Bit 5 RDIO	Reg 20 Bit 6 WCLK IN	Reg 20 Bit 7 Gtd RDIO	Reg 21 Bit 7 RDIO/RDQ	Reg 21 Bit 6 RDIO HIZ	RDIO SIGNAL
0	1	1	X	X	X	WCLK Input
1	1	0	X	X	X	Read Data Input
0	0	0	0	1	X	Read Data Output
0	0	0	0	0	X	RDQ
1	0	0	0	X	0	No Output
1	0	0	X	X	1	HIZ
1	0	0	1	1	0	Read Data Output
1	0	0	1	0	0	RDQ

Hysteresis Comparator Qualification

When the hysteresis qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bi-directional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bi-directional one-shot. Hysteresis comparator timing is shown in Figure 1B.

Tracking Threshold

The SSI 34P3211B also provides a tracking threshold. This threshold is set as a function of the Qualifier threshold, and whenever the signal at DP-DN is greater than the tracking threshold, the LEVEL pin has an extra discharge current. The magnitude of the discharge current is determined by the RTH resistor and Bits D0-D2 of R28. The value of the tracking threshold depends on Bits D4-D6 of R28 and the formula for the threshold is:

Tracking threshold = (0.3 + (n1 • 0.1)) • Thresh

Thresh = Qualifier threshold as defined above and n1 is defined below.

The formula for the tracking threshold discharge current is: I(LEVEL) = (1.5/RTH) • (n2/2)

Where n2 is defined in Table 2.

The tracking threshold current is in addition to the LEVEL Decay Current set in R34 and the 2 currents are independent of each other. The minimum value of the Rth resistor is 30 kΩ. The entire tracking threshold circuit can be disabled and powered down by setting D6 of R34 to 1.

TABLE 2

R28 BIT D6	R28 BIT D5	R28 BIT D4	n1	R28 BIT D2	R28 BIT D1	R28 BIT D0	n2
0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1
0	1	0	2	0	1	0	2
0	1	1	3	0	1	1	3
1	0	0	4	1	0	0	4
1	0	1	5	1	0	1	5
1	1	0	6	1	1	0	6
1	1	1	7	1	1	1	7

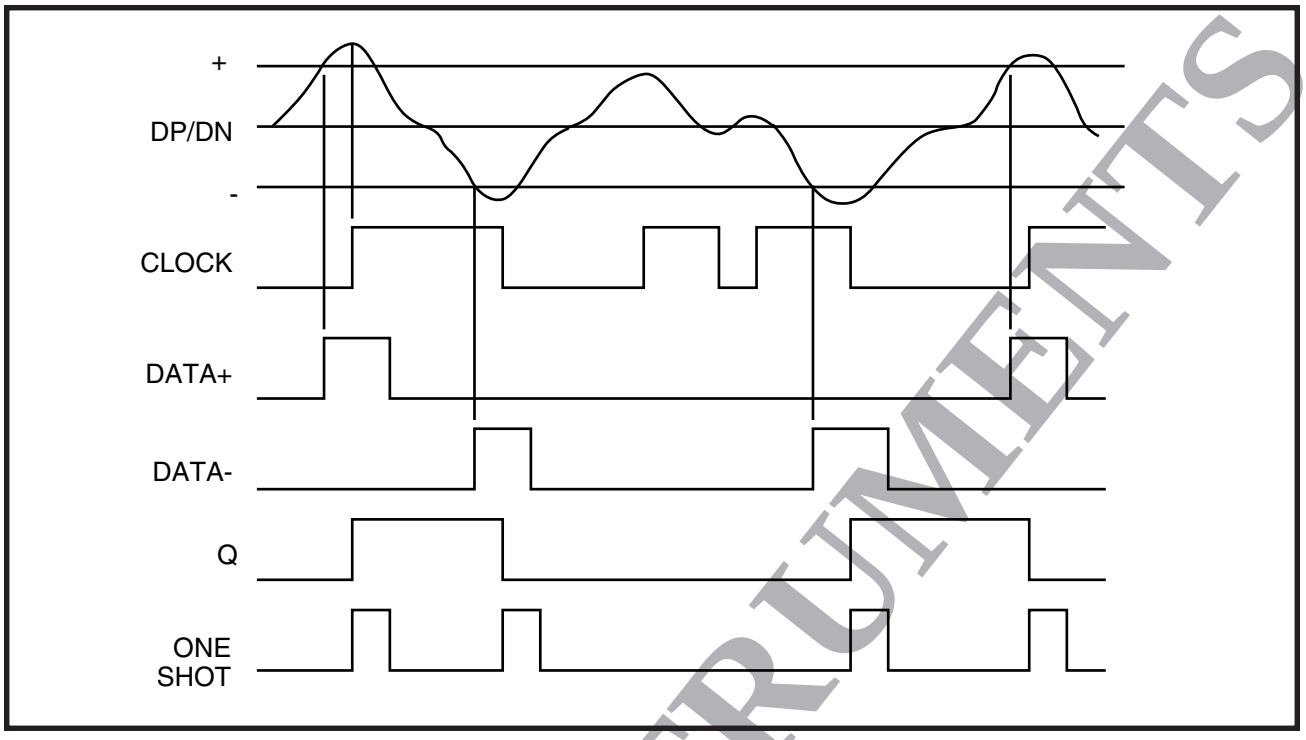


FIGURE 1A: Dual Comparator Timing Diagram

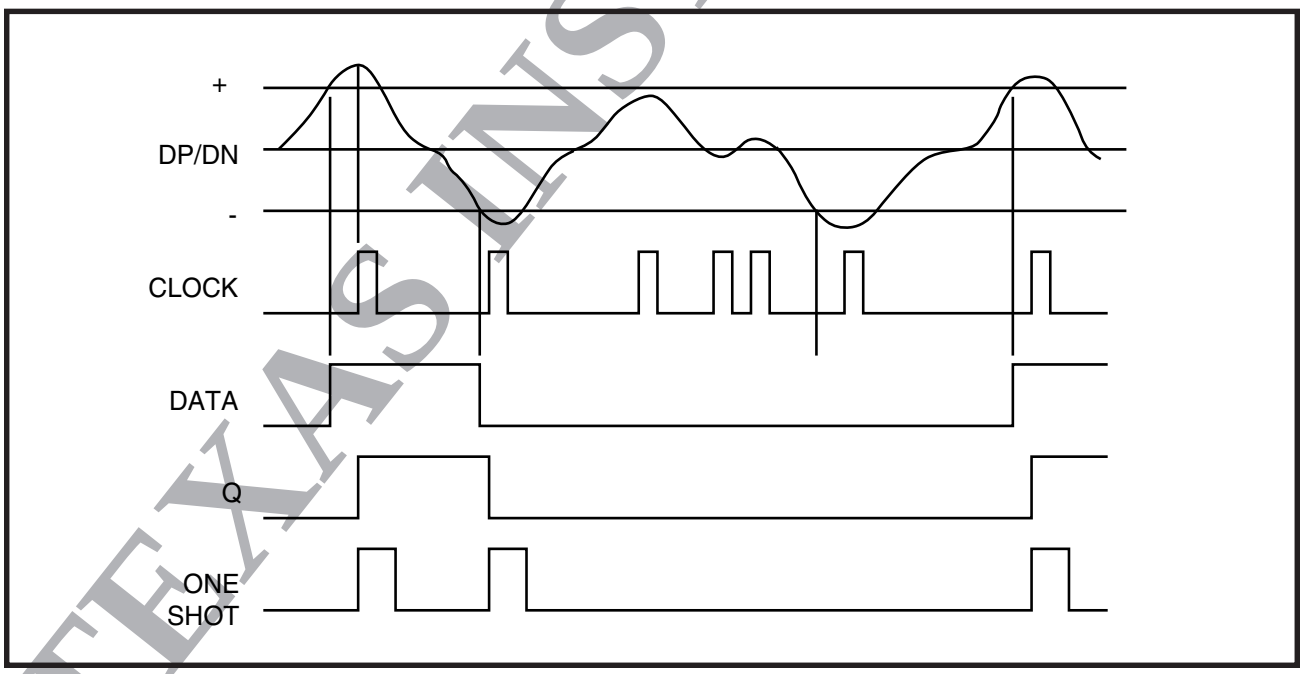


FIGURE 1B: Hysteresis Comparator Timing Diagram

FUNCTIONAL DESCRIPTION (continued)

PROGRAMMABLE FILTER

The SSI 34P3211B contains an electronically controlled 7-pole low-pass filter. The transconductance-capacitance (gm-C) filter approximates a linear phase or constant group delay response. Programmable bandwidth and boost/equalization are provided by internal 7-bit control DACs. Differentiation pulse slimming equalization which does not affect the filter's group delay response is accomplished by two programmable complimentary real axis zeros. Programmable phase equalization is also available, providing up to ±20% variation in low-frequency group delay value.

The filter implements a 0.05° equiripple linear phase response. The normalized transfer function (i.e. $s = jwc = j2\pi fc$, where $j^2 = -1$) is:

$Vo/Vi = H14 \bullet H2 \bullet H3$

where

$H14 = [-2.54628\ \alpha\ s^2 + 2.76833\ ß\ s + 1.13440\ (1 - \alpha)]/(s^3 + 2.54628\ s^2 + 2.76833\ s + 1.13440)$

$H2 = 5.37034/(s^2 + 1.14558\ s + 5.37034)$

$H3 = 2.95139/(s^2 + 1.54203\ s + 2.95139)$

The normalized pole frequencies and quality factors of the biquads and bicubic sections are:

$w1 = 1.14762 \quad Q1 = 0.68110$

$w2 = 2.3174 \quad Q2 = 2.02290$

$w3 = 1.71746 \quad Q3 = 1.11409$

$w4 = 0.86133$

The frequency is denormalized by replacing s by $s/2\pi Fc$. The parameters α and ß are discussed below. α is always positive, and ß can be positive or negative.

The differential signals from the AGC are AC coupled to the inputs of the filter. The programmable bandwidth and boost/equalization features are controlled by internal DACs whose registers are programmable by the serial port. The current reference for the frequency DACF is set using a single external resistor connected from pin RXP to RXN. No external components are required for the boost/equalization control.

The programmable bandwidth is set by the filter cutoff DACF according to the following equation.

$$Fc = DACF^2 \bullet 0.0000052 + DACF \bullet 0.029812 - 0.004376\ (MHz)$$

The data mode cutoff register is used to determine the filter's unboosted -3 dB cutoff frequency (Fc). This is the -3 dB frequency for both α and ß equal to 0. When boost/equalization is added, the actual -3 dB point will move out, as discussed below.

The filter's magnitude and group delay characteristics can be altered by adjusting the parameters α and ß. α boosts the filter response at high frequencies while leaving the group delay unaltered. The effect on read data pulses is symmetrical slimming. ß controls the filter's phase or group delay response. ß boost is necessary to correct asymmetry in incoming data pulses. A side effect of ß group delay equalization is a slight change in magnitude response.

Alpha Boost (Magnitude Equalization)

The SSI 34P3211B employs a novel magnitude equalization scheme in which the filter's magnitude characteristics for different values of α pivot around a point of constant gain. The normalized constant gain pivot point is wp = 0.6675. As shown in Figure 2, for nonzero values of α, the filter gain for frequencies above wp is increased, while frequencies below wp are attenuated. The advantages of this new technique over the conventional realization, which only boosts higher frequencies, are faster AGC recovery between modes and reduced AGC dynamic range requirements.

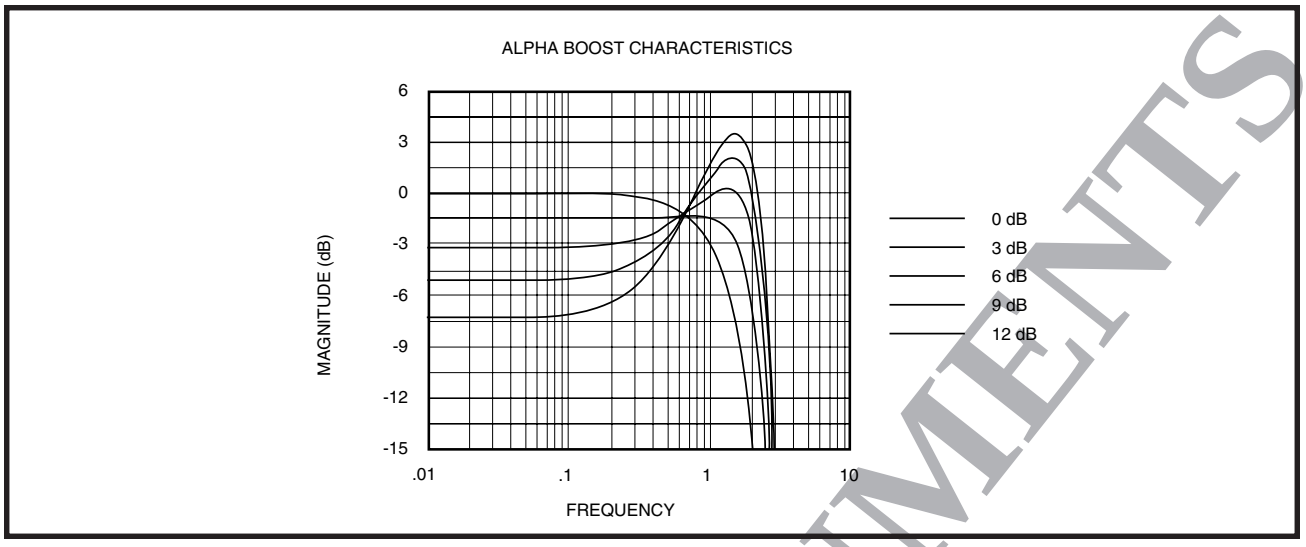


FIGURE 2: Pivoting Alpha Boost Magnitude Characteristics

Alpha Boost (Magnitude Equalization) (continued)

Alpha Boost ($\alpha \neq 0$, ß = 0) does not affect the filter's group delay response. The amount of alpha boost that will be added to the unboosted -3 dB cutoff frequency (Fc) is set by the Filter Boost DACS according to the following equation:

$$\text{Alpha Boost} = DACS^2 \bullet 0.0001666 + DACS \bullet 0.065067 - DACF \bullet 0.002177 + 0.536 \text{ (dB)}$$

For example, with DACS set for maximum output, there will be 11.21 dB of boost added at Fc. This will result in the gain at Fc being 9 dB higher than at DC, versus being -3 dB when unboosted. In absolute values, the DC gain will become -7.35 dB and the gain at Fc will equal 1.65 dB. Table 3 provides information on alpha boost versus α (ß = 0), DACS, DC gain and gain at Fc.

TABLE 3: Alpha Boost Versus α (ß = 0)

α BOOST (dB)	α	DACS	DC GAIN (w = 0) (dB)	GAIN AT Fc (dB)
0	0.00000	0	0	-3
1	0.05156	5	-0.47	-2.47
2	0.10342	11	-0.95	-1.95
3	0.15526	18	-1.47	-1.47
4	0.20671	25	-2.02	-1.02
5	0.25746	33	-2.59	-0.59
6	0.30719	42	-3.19	-0.19
7	0.35562	53	-3.82	0.18
8	0.40247	64	-4.48	0.52
9	0.44755	77	-5.16	0.84
10	0.49066	92	-5.86	1.14
11	0.53167	109	-6.59	1.41
12	0.57047	127	-7.35	1.65

If alpha boost is applied, the minimum amount must be 1 dB. DACS values should equal 0 or 5 - 127. Values 1, 2, 3, and 4 are invalid.

Beta Boost (Group Delay Equalization)

When ß = 0, the 7-pole filter approximates a constant group delay response delay response in equiripple sense over a normalized frequency range between DC and w ≅ 2. For w = 0, the group delay equals:

$$GDL(0) = 1/(w1Q1) + 1/(w2Q2) + 1/(w3Q3) + 1/w4 \quad (ß = 0)$$

The denormalized filter group delay at DC as a function of Fc is therefore:

$$GDL(0) = 3.17630 / (2\pi Fc) \quad \text{(seconds, ß =0)}$$

By applying beta boost (a = 0, ß ≠ 0) the group delay response of the filter can be altered, and given a positive or negative slope as shown in Figure 3.

The group delay Δ% is defined as the percentage change in absolute group delay value at Fc/10 with respect to that without the equalization applied (ß = 0). The group delay Δ% at low frequencies can be programmed between -20% and +20% by means of DACG which is controlled by R27. The MSB of R27 acts as a sign bit, as follows:

$$\text{Group Delay } \Delta\% = -0.15748 \bullet DACG \ (\%)$$

where $0 \le DACG \le 127$

or

$$\text{Group Delay } \Delta\% = 0.15748 \bullet (DACG - 128) \ (\%)$$

where $128 \le DACG \le 255$

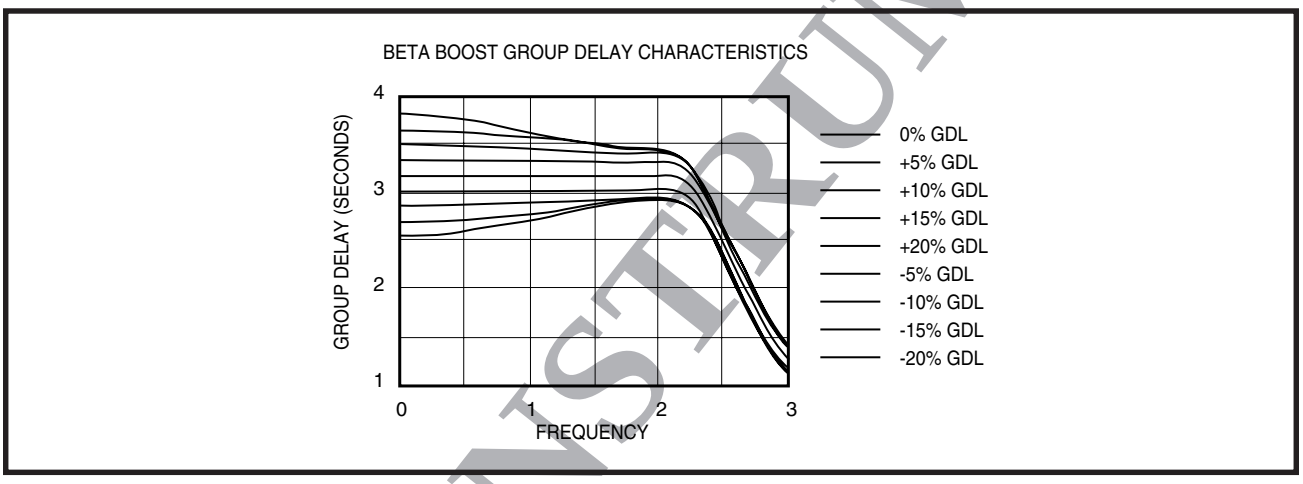


FIGURE 3: Beta Boost Group Delay Characteristics

The relationship between ß, DACG and group delay Δ% is given in Table 4.

TABLE 4: Group Delay Δ%, ß and Beta Boost (a = 0)

GROUP DELAY (Δ%)	ß	DACG
-20	0.26030	127
-15	0.19523	96
-10	0.13015	64
-5	0.06508	32
0	0.00000	0
5	-0.06508	160
10	-0.13015	192
15	-0.19523	224
20	-0.26030	255

PROGRAMMABLE FILTER (continued)

Combined Alpha and Beta Boost

A side effect of ß group delay equalization is a small amount of non-pivoting high-frequency magnitude boost. However, when both $\alpha \neq 0$ and $ß \neq 0$, the total amount of boost is largely dominated by alpha boost only. Table 5 lists the actual boost versus alpha boost and percentage group delay variation. Figures 4 and 5 illustrate the effect of beta boost for alpha boost equal to 0 dB and 12 dB respectively.

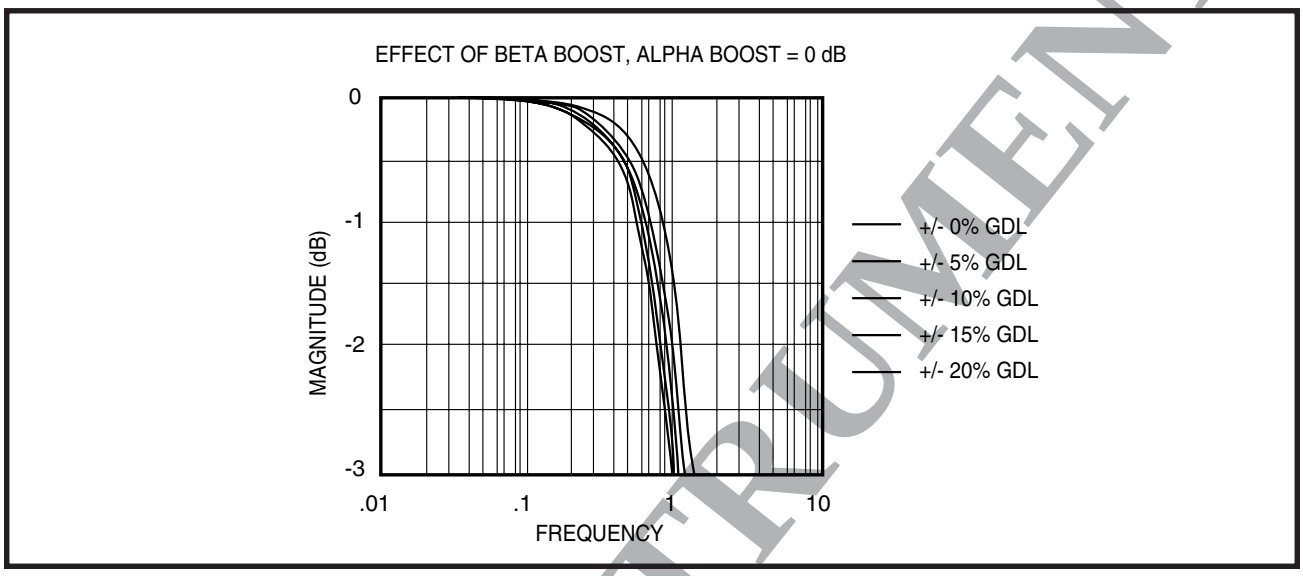


FIGURE 4: Effect of Beta Boost for Alpha Boost = 0 dB

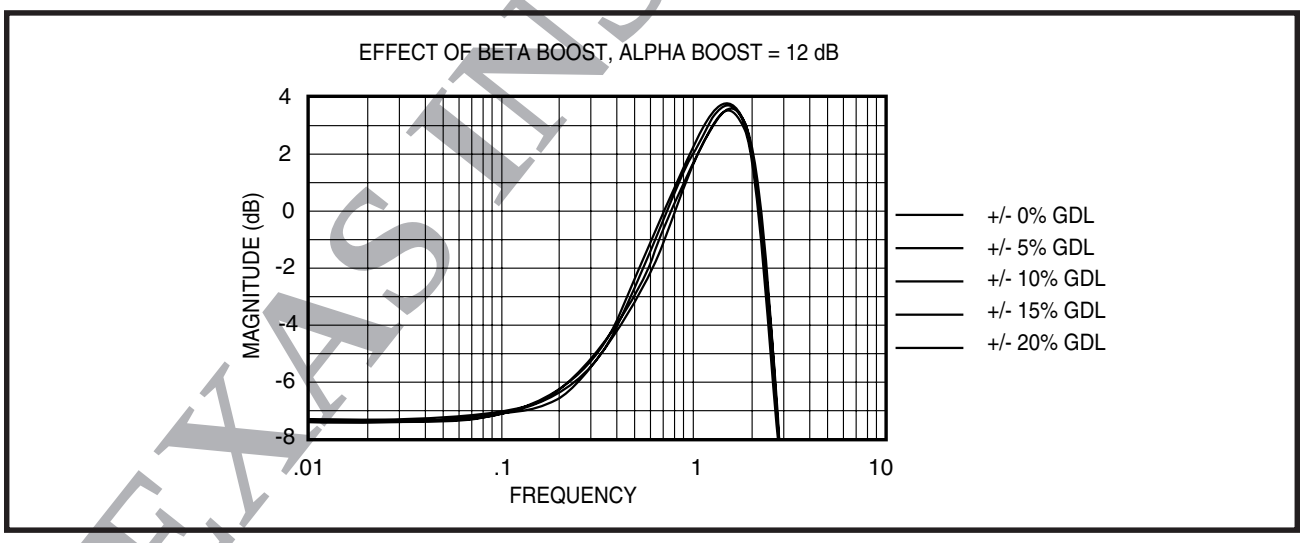


FIGURE 5: Effect of Beta Boost for Alpha Boost = 12 dB

TABLE 5: Actual Boost Vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%
0	1.46	0.88	0.41	0.09	0.00
1	2.31	1.78	1.36	1.09	1.00
2	3.18	2.70	2.32	2.08	2.00
3	4.07	3.63	3.29	3.07	3.00
4	4.98	4.57	4.26	4.06	4.00
5	5.89	5.59	5.23	5.05	5.00
6	6.82	6.48	6.21	6.05	6.00
7	7.76	7.44	7.20	7.04	7.00
8	8.71	8.41	8.18	8.04	8.00
9	9.66	9.38	9.17	9.03	9.00
10	10.62	10.35	10.16	10.03	10.00
11	11.58	11.33	11.15	11.03	11.00
12	12.55	12.32	12.14	12.03	12.00

The -3 dB frequency (F-3 dB) is defined as the frequency for which the filter gain is 3 dB below the gain at DC. For α = 0 and ß = 0, F-3 dB = Fc and the gain at F- 3 dB equals -3 dB. When boost is applied F-3 dB increases. As a result of the pivoting alpha boost, the DC gain and hence the gain at F-3 dB also changes. Table 6 gives the ratio between Fc and F-3 dB as a function of alpha boost and Δ% group delay variation and the gain at F-3 dB.

While the amount of boost is defined at Fc, the peak in the magnitude transfer function occurs at a different frequency. Tables 7 and 8 contain the ratios of Fpeak/ Fc and the gain at Fpeak as a function of alpha boost and Δ% group delay variation, respectively.

TABLE 6: F-3 dB/Fc Vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%	GAIN AT F-3 dB (dB)
0	1.32	1.18	1.07	1.02	1.00	-3.00
1	1.54	1.41	1.30	1.23	1.21	-3.47
2	1.76	1.66	1.58	1.52	1.51	-3.95
3	1.95	1.89	1.85	1.81	1.80	-4.47
4	2.12	2.09	2.06	2.04	2.04	-5.02
5	2.25	2.23	2.21	2.21	2.20	-5.59
6	2.35	2.34	2.33	2.33	2.33	-6.19
7	2.44	2.43	2.43	2.43	2.43	-6.82
8	2.52	2.52	2.51	2.51	2.51	-7.48
9	2.60	2.59	2.59	2.59	2.59	-8.16
10	2.67	2.67	2.66	2.66	2.66	-8.86
11	2.74	2.73	2.73	2.73	2.73	-9.59
12	2.81	2.80	2.80	2.80	2.80	-10.35

PROGRAMMABLE FILTER (continued)

TABLE 7: Fpeak/Fc Vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%
0	no peak	no peak	no peak	no peak	no peak
1	no peak	no peak	no peak	no peak	no peak
2	0.74	0.56	no peak	no peak	no peak
3	0.95	0.88	0.80	0.73	0.71
4	1.10	1.08	1.06	1.05	1.04
5	1.22	1.22	1.22	1.22	1.22
6	1.30	1.30	1.31	1.32	1.32
7	1.35	1.37	1.37	1.38	1.38
8	1.39	1.41	1.42	1.42	1.42
9	1.43	1.44	1.45	1.45	1.46
10	1.45	1.46	1.47	1.48	1.48
11	1.47	1.48	1.49	1.49	1.50
12	1.49	1.50	1.51	1.51	1.51

TABLE 8: dB Gain @ Fpeak Vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%
0	no peak	no peak	no peak	no peak	no peak
1	no peak	no peak	no peak	no peak	no peak
2	-0.59	-0.89	no peak	no peak	no peak
3	-0.38	-0.80	-1.09	-1.27	-1.32
4	0.00	-0.42	-0.74	-0.95	-1.02
5	0.48	0.10	-0.19	-0.37	-0.43
6	1.00	0.68	0.43	0.27	0.22
7	1.53	1.25	1.04	0.90	0.86
8	2.04	1.79	1.61	1.50	1.47
9	2.52	2.31	2.15	2.06	2.03
10	2.97	2.79	2.65	2.57	2.54
11	3.39	3.22	3.10	3.03	3.00
12	3.77	3.62	3.51	3.45	3.43

TIME BASE GENERATOR

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

In read, write and idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1))FREF

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the data recovery control register (DRCR). This DAC, DACI, also sets the 1/2 symbol delay, VCO center frequency, and phase detector gain for the data synchronizer circuitry. The VCO center frequency is also a function of bit 7 in the DRCR. The formula for the VCO center frequency is:

$$FVCO = [12.5/(RR + 0.4)] \bullet S \bullet (42 \bullet DACI + 16.5) \quad kHz$$

S = 3 if R4 (DRCR) bit 7 = 1

S = 1 if R4 (DRCR) bit 7 = 0

When changing frequencies, the M and N registers must be loaded first, followed by the DRCR register. A frequency change is initiated only when the DRCR register has been changed.

To optimize the TBG PLL performance over the wide range of M counter values available, provision is made to select one of the two external loop filters via serial port control. If R29 Bit D7 = 1, then TFLT1 & $\overline{\text{TFLT}}$ are chosen, and if R29 Bit D6 = 1, then TFLT0 & $\overline{\text{TFLT}}$ are chosen.

DATA SYNCHRONIZER

In the read mode, the data synchronizer performs data synchronization. In the write mode, the circuit provides write precompensation or equalization. Data rate is established by the time base generator and the internal reference DACI controlled by the DR register. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/2 symbol delay.

Phase Locked Loop

The circuit employs a dual mode phase detector; harmonic in the read mode when HL = 1 and non-harmonic in the write and idle modes and in read mode when HL = 0. In harmonic read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{\text{DRD}}$ pulse. In non harmonic read mode the PLL phase and frequency locks VCO/2 to the incoming data. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL. Provision for two loop filters is made with the selection control provided via the serial port. If R12 Bit D7 = 1, then DFLT1 & $\overline{\text{DFLT}}$ are chosen, and if R12 Bit D6 = 1, then DFLT0 & $\overline{\text{DFLT}}$ are chosen.

The phase detector enabler pin, PHDETEN must be set to 1 to enable the phase detector. If PHDETEN is low, then there will be no updates to the PLL and loop will coast, subject to leakage currents. Similarly, the common mode enable pin must be set to 1 to enable the common mode current. This common mode current on both filter pins keeps the average voltage of the loop filter pins at an internal reference of approximately 2 V.

DATA SYNCHRONIZER (continued)

Mode Control

The read gate (RG) and harmonic lock (HL) inputs control the device operating mode. RG and HL are asynchronous inputs and may be initiated or terminated at any time. When RG = 0 the SDO output is put in HIZ mode.

Read Mode (HL = 1)

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/2 symbol wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock. Read data synchronization waveforms are shown in Figure 6. Bit 5 of register 34 controls the input to the data synchronizer. If bit 5 = 1 then RD is the input to the synchronizer instead of $\overline{DRD}$. This mode can have advantages when the data contains consecutive ones. If this is the case and two of these pulses are shifted towards one another, the $\overline{DRD}$ one shot may mask the second pulse. For normal operation bit 5 of Register 34 should be set low.

Read Mode (HL = 0)

The HL pin can be used to lock non harmonically to a 2T pattern. When HL = 0, the inputs to the phase detector will be VCO/2 and $\overline{DRD}$ and VCO/2 will be phase and frequency locked to $\overline{DRD}$. When HL switches from 1 to 0, RRC will switch to DS VCO and SDO will become active once RG = 1. With HL = 0 there is no zero phase restart or VCO lock as described below and KD remains at 1X. For normal operation, HL should be set to 1.

Preamble Search (HL = 1)

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read data, RD. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO Lock and Bit Sync Enable (HL = 1)

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 3, in the Control B register. If GS = “1”, the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 11 transitions of the internal DRD signal, the gain is reduced by a factor of 3. This reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the data follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 pulses from assertion of RG) and then asserts an internal VCO lock signal. When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period, the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the GS bit is set to “0” the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 11 transitions.

Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR).

Window Shift Control

Window shift magnitude is set by the value in the Window Shift Control Register (WSCR). The WSCR register bits are as follows:

BIT	NAME	DESCRIPTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0 = early, 1 = late
5	WSE	Window shift enable
6	—	
7	—	

Window shift early and window shift late waveforms are shown in Figure 6. The window shift magnitude is set as a percentage of the full decode window, in 2.4% steps. This results in a window shift capability of ± 36%. The tolerance of the window shift magnitude is ± 20%. Window shift should be set during idle mode.

TABLE 9

WS3	WS2	WS1	WS0	SHIFT MAGNITUDE
1	1	1	1	No shift
1	1	1	0	2.4% (minimum shift)
1	1	0	1	4.8%
1	1	0	0	7.2%
1	0	1	1	9.6%
1	0	1	0	12%
1	0	0	1	14.4%
1	0	0	0	16.8%
0	1	1	1	19.2%
0	1	1	0	21.6%
0	1	0	1	24%
0	1	0	0	26.4%
0	0	1	1	28.8%
0	0	1	0	31.2%
0	0	0	1	33.6%
0	0	0	0	36% (maximum shift)

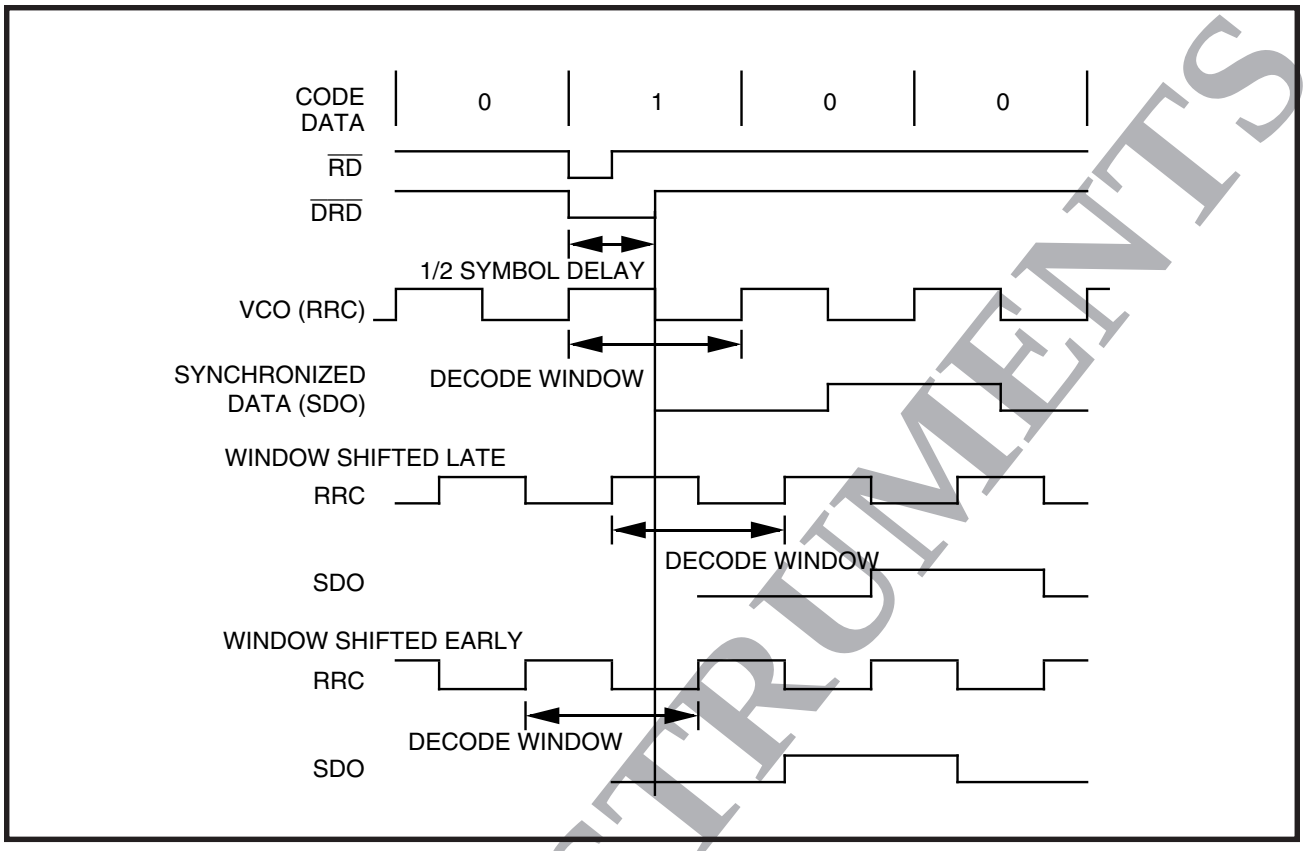


FIGURE 6: Read Data Synchronization Waveforms

DATA SYNCHRONIZER (continued)

Non Read Mode

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

Write DAC

A 6-bit write DAC, DACW, is provided for current reference for the R/W chip. This is enabled by setting bit 5 of register 29 (CAR), and the output is provided at DACOUT. This output is a current sink and the voltage at DACOUT must be ≥ 1.75 V. The output current sink is programmable from 0 to 2.52 mA as follows:

$$IWRITE = 2.52\ MA \bullet DACW/63$$

Head Select

Two serial port bits, bits 6 and 7 of R2 (PDCR) are buffered and provided as CMOS outputs. These outputs can be used for head select or other customized control logic.

Operating Modes and Control

The SSI 34P3211B has several operating modes that support read, write, and power management functions. Mode selection is accomplished by controlling the read gate (RG), harmonic lock (HL), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), and the Control B register (CBR) via the serial port.

External Mode Control

All operating modes of the device are controlled by driving the read gate (RG), write gate ($\overline{WG}$), harmonic lock (HL), and $\overline{PWRON}$ pins with CMOS compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the SSI 34P3211B is controlled by RG and HL pins. When RG is high, the device is in read mode. When $\overline{WG}$ is low and RG is low the device is in write mode. If the RG is low the device will be in idle mode.

DATA SYNCHRONIZER (continued)

TABLE 10: Mode Control Table

CONTROL LINE		DEVICE MODE	DAC CONTROL			
$\overline{PWRON}$	RG		VTH	FC	BOOST	HYSTERESIS
1	X	SLEEP MODE: All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	1	READ MODE: The pulse detector is active. The data synchronizer begins the preamble lock sequence. RDIO is inactive.	DR	DR	DR	DR
0	0	IDLE MODE: The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC.	DR	DR	DR	DR

DAC Control Key: DR = Data Register, off = disabled

Control Registers

Control registers CAR and CBR and R21 allow the user to configure the SSI 34P3211B test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the time base generator. CBR controls functions of the data synchronizer. R21 controls test point output selection and DAC test points. The bits of the CA and CB registers are defined as follows:

CONTROL REGISTER CAR:

BIT	NAME	DESCRIPTION
0	EPDT	Enable Phase Detector (Time Base Generator)
1	UT	Pump Up (TFLT sources current, $\overline{TFLT}$ sinks Current)
2	DT	Pump Down (TFLT sinks current, $\overline{TFLT}$ sources Current)
3	TBG KD	Change phase detector gain by a factor of 3
4	BYPT	Bypass Time Base Generator Circuit Function
5	WR_DAC EN	Enables Write DAC
6	TBG LF0	Select TBG PLL loop filter 0
7	TBG LF1	Select TBG PLL loop filter 1

CONTROL REGISTER CBR

BIT	NAME	DESCRIPTION
0	EPDD	Enable Phase Detector (Data synchronizer)
1	UD	Pump Up (sources current, $\overline{\text{DFLT}}$ sinks current)
2	DD	Pump Down (DFLT sinks current, $\overline{\text{DFLT}}$ sources current)
3	GS	Enable Phase Detector Gain Switching
4	DST	DS Test Mode
5	RDIO	Select input (logic 1) or output (logic 0)
6	DSF0	Select DS PLL Loop Filter 0
7	DSF1	Select DS PLL Loop Filter 1

TABLE 11: Multiplexed Test Point Signal Selection
Test point selection and DAC testing is defined as follows:

MTPE	TMS1	TMS0	MTP1	MTP2	MTP3	MTP4
1	X	X	OFF	OFF	OFF	OFF
0	0	0	VCOREF	$\overline{\text{VCOREF}}$	TTCOMP	$\overline{\text{DRD}}$
0	0	1	SET	RESET	DSREF	MCTR
0	1	0	SSI Test Mode			
0	1	1	RD	SET	NCTR	MCTR

VCOREF = Data synchronizer VCO reference clock

DSREF = Output of the time base generator

MCTR = M counter output of the time base generator

RD = Read MO data output from the pulse qualifier

PDQ/PUQ = Data synchronizer phase detector monitor points

NCTR = N counter output of the time base generator

RESET = Output of the negative threshold comparator

SET = Output of the positive threshold comparator

TTCOMP = Output of the Tracking Threshold comparator

TABLE 12: DACOUT Signal Selection

WR DAC EN	TDAC1	TDAC0	DAC MONITORED
1	0	0	Filter DACs
1	0	1	Qualifier threshold DAC (VTH)
1	1	0	Window shift DAC
0	X	X	Write Current DAC

CONTROL REGISTERS (continued)

The test of the filter DACs is controlled through the serial port. When the MSB of R11 is set to 1, the Fc DAC test is selected. When the MSB of R3 is set to 1, the Boost DAC test is selected. When the MSBs of R3 and R11 are set to 0, the DAC tests are disabled and testing of the MOS Vt can be performed.

Power Down Control

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into sleep mode (< 5 mW) and all circuits are powered down except the serial port and the power-on reset circuitry. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is driven low ("0"), the contents of the PDCR, R29 Bit 5, and R34 Bit 6 determine which blocks will be active. Register mapping for the PDCR is shown in Table 5. To improve recovery time from the sleep mode, the $\overline{\text{WG}}$ pin should be asserted following power down to initiate the AGC recovery sequence. Power control timing is shown in Figure 7.

Bits 7 and 6 of the PDCR register control the speed of the CMOS output buffers according to the following table:

TABLE 13

BIT 1	BIT 0	
0	0	slow
0	1	medium
1	0	fast
1	1	very fast

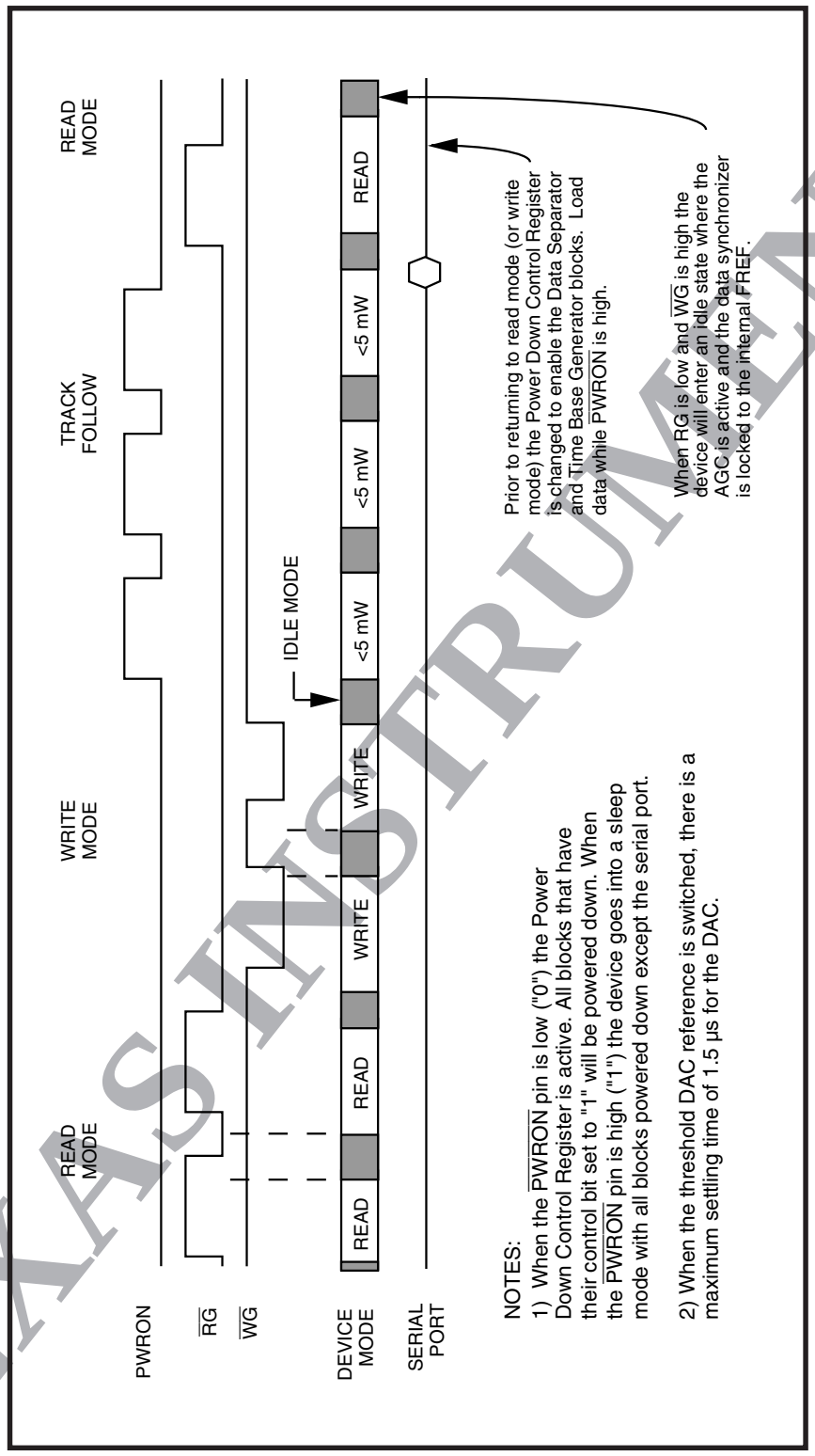


FIGURE 7: Power Control Timing

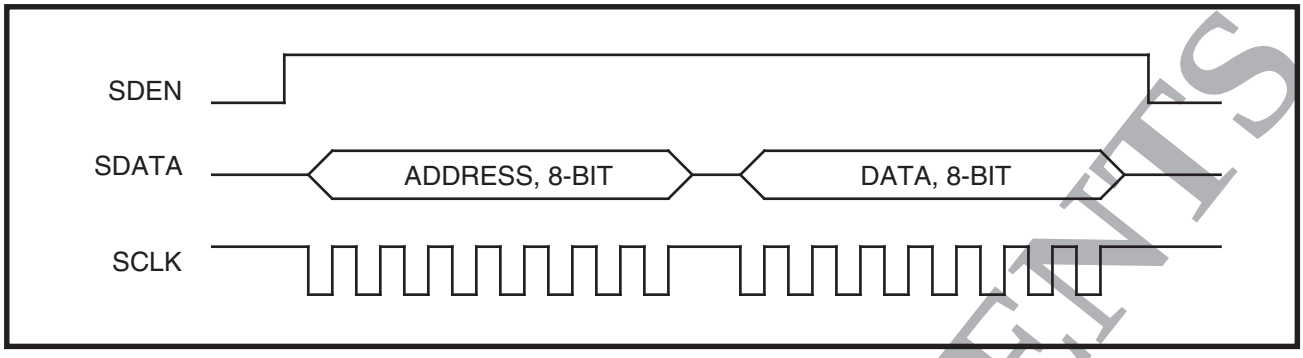


FIGURE 8: Serial Port Data Transfer Format

SERIAL INTERFACE

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 34P3211B. The serial port data transfer format is shown in Figure 8. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits determine the internal register to be accessed. Table 5 provides register mapping information. The second byte contains the programming data. In read mode (R/W = 1) the SSI 34P3211B will output the register contents of the selected address. In write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 9.

REG#	REGISTER NAME	ADDRESS A6						A0	R/W	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R2	POWER DOWN CONTROL REGISTER (PDCR)	0	0	0	0	0	1	0	0	I/O SPEED Bit 1	I/O SPEED Bit 0	MTPE 1 = Disable 0 = Enable	DS 1 = Disable 0 = Enable	TBG 1 = Disable 0 = Enable	FILTER 1 = Disable 0 = Enable	WR PRE 1 = Disable 0 = Enable	PD 1 = Disable 0 = Enable
R11	DATA MODE CUTOFF REGISTER (DMCR)	0	0	0	1	0	1	1	0	fc dac tst 0 = Disable 1 = Enable	DACF Bit 6	DACF Bit 5	DACF Bit 4	DACF Bit 3	DACF Bit 2	DACF Bit 1	DACF Bit 0
R4	DATA RECOVERY CONTROL REGISTER (DRCR)	0	0	0	0	1	0	0	0	Vco Freq 1 = High 0 = Low	DACI Bit 6	DACI Bit 5	DACI Bit 4	DACI Bit 3	DACI Bit 2	DACI Bit 1	DACI Bit 0
R5	N COUNTER CONTROL REGISTER (NCCR)	0	0	0	0	1	0	1	0	gd dac tst 1 = Enable 0 = Disable	N Count Bit 6	N Count Bit 5	N Count Bit 4	N Count Bit 3	N Count Bit 2	N Count Bit 1	N Count Bit 0
R10	DATA THRESHOLD CONTROL REGISTER(DTCR)	0	0	0	1	0	1	0	0	Data Qual 1 = Dual 0 = Hyst	DACT Bit 6	DACT Bit 5	DACT Bit 4	DACT Bit 3	DACT Bit 2	DACT Bit 1	DACT Bit 0
R3	FILTER BOOST CONTROL REGISTER (FBCR)	0	0	0	0	0	1	1	0	bst dac tst 1 = Enable 0 = Disable	DACS Bit 5	DACS Bit 5	DACS Bit 5	DACS Bit 5	DACS Bit 2	DACS Bit 1	DACS Bit 0
R12	CONTROL B REGISTER (CBR)	0	0	0	1	1	0	0	0	DSLF Select 1 1 = Enable	DSLF Select 0 1=Enable	RDIO 1 = Input 0 = Output	DS Test 1 = Enable 0 = Disable	Gain Shift 1 = On 0 = Off	Pump Down 1 = On 0 = Off	Pump Up 1 = On 0 = Off	Unused
R13	M COUNTER LSB REGISTER (MCLCR)	0	0	0	1	1	0	1	0	M Count Bit 7	M Count Bit 6	M Count Bit 5	M Count Bit 4	M Count Bit 3	M Count Bit 2	M Count Bit 1	M Count Bit 0
R18	AGC GAIN CONTROL REGISTER (AGCR)	0	0	1	0	0	1	0	0	FD TST 1 = Enable 0 = Disable	DACA Bit 6	DACA Bit 5	DACA Bit 4	DACA Bit 3	DACA Bit 2	DACA Bit 1	DACA Bit 0
R20	WINDOW SHIFT CONTROL REGISTER (WSCR)	0	0	1	0	1	0	0	0	Gtd RDIO 0 = Gated 1 = On	WCLK/RDIO 1 = Enable 0 = Disable	WIN SHFT 1 = Enable 0 = Disable	WS DIR 1 = Late 0 = Early	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
R21	M COUNTER MSB REGISTER (MCMCR)	0	0	1	0	1	0	1	0	RDIO/RDQ 1 = RDIO 0 = RDQ	RDIO hiz 1 = Rg Cont 0 = Off	TMS1	TMS0	TDAC1	TDAC0	M Count Bit 9	M Count Bit 8
R28	WRITE PRECOMP CONTROL REGISTER (WPCR)	0	0	1	1	1	0	0	0	Equalization 1 = Enable 0 = Disable	$\overline{WL2}$/ TTH2	$\overline{WL1}$/ TTH1	$\overline{WL0}$/ TTH0	WR PRCMP 1 = Enable 0 = Disable	$\overline{WE2}$/ TTHI2	$\overline{WE1}$/ TTHI1	$\overline{WE0}$/ TTHI0
R29	CONTROL A REGISTER (CAR)	0	0	1	1	1	0	1	0	TBG LF Select 1 1 = Enable	TBG LF Select 0 1=Enable	WR DAC EN 1 = Disable 0 = Enable	TBG Bypass 1 = Enable 0 = Disable	TBG KD 0 = 1 x KD 1 = 3 X KD	Pump Down 1 = On 0 = Off	Pump Up 1 = On 0 = Off	Phase Det 1 = Enable 0 = Disable
R36	WRITE CURRENT CONTROL REGISTER (WCCR)	0	1	0	0	1	0	0	0	Serial Port Out 1	Serial Port Out 0	DACW Bit 5	DACW Bit 4	DACW Bit 3	DACW Bit 2	DACW Bit 1	DACW Bit 0
R34	HYSTERESIS DECAY CONTROL REGISTER(HDCR)	0	1	0	0	0	1	0	0	--	TTHEN 0 = Enable 1 = Disable	DS REF 0 = $\overline{DRD}$ 1 = RD	Threshold 0 = Fixed 1 = Level	DACL Bit 3	DACL Bit 2	DACL Bit 1	DACL Bit 0
R27	GROUP DELAY EQ REGISTER	0	0	1	1	0	1	1	0	Sign	DACG Bit 6	DACG Bit 5	DACG Bit 4	DACG Bit 3	DACG Bit 2	DACG Bit 1	DACG Bit 0

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data synchronizer PLL power supply pin
VPB	-	Time base generator PLL power supply pin
VPC	-	Pulse detector, serial port power supply pin
VPG	-	AGC, filter power supply pin
VCC1	-	Write data I/O power supply pin
VCC2	-	Read data I/O power supply pin
VCC3	-	RDIO I/O power supply pin
VNA	-	Data synchronizer PLL ground pin
VNB	-	Time base generator PLL ground pin
VNC	-	Pulse detector, serial port ground pin
vng	-	AGC, filter ground pin
RTRN1	-	Write data I/O ground pin
RTRN2	-	Read data I/O ground pin
RTRN3	-	RRC ground pin
RTRN4	-	RDIO ground pin

INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full wave rectifiers.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{\text{PWRON}}$	I	POWER ENABLE: CMOS compatible power control circuit. A low level CMOS input enables power to circuitry according to the contents of the power enable bits. A high level CMOS input shuts down all circuitry.
HOLD	I	HOLD CONTROL: CMOS compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FIP, FIN	I	FILTER INPUT SIGNALS: The AGC output signals must be coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF has an internal pull down resistor. FREF should be driven by an AC coupled signal between 1.2 Vp-p and 2 Vp-p.
PHDETEN	1	DS PHASE DETECTOR ENABLE: CMOS compatible input. A high level CMOS input enables the DS Phase Detector. A low level disables the DS Phase Detector, thus preventing updates to the loop.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RG	I	READ GATE: CMOS compatible read gate input. A high level CMOS input selects the RD input and enables the read mode/address detect sequences. A low level selects the FREF input.
HL	I	HARMONIC LOCK: CMOS compatible input. A high level CMOS input selects harmonic read mode. A low level selects non-harmonic read mode.
CMMDEN	I	DS COMMON MODE ENABLE: CMOS compatible write input. A high level CMOS input enables the common mode current on the DS loop filter. A low level disables the common mode current.

OUTPUT PINS

MTP1-4	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the MCTR MSB register. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYCHRONIZED READ DATA: CMOS output pin. Read data output when RG is high. In Hi-Z mode when RG = 0.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
RDIO	O	READ DATA I/O: Bi-directional CMOS output/input pin. See RDIO control table on page 5. The minimum RDIO input pulse width is 10 ns. When RDIO is used as an input pin, the 1/2 symbol delay in the data synchronizer is made from the rising edge. When RDIO is an input and $\overline{WG}$ = 0 and WS bit 6 = 1, RDIO is used to clock the write precomp/equalization.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. Then RRC will switch to the DS VCO after the 19th data pulse. When RG goes low, RRC is synchronized back to the reference clock.
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).
SP1, SP0	O	CMOS buffered serial port bits from DACW register.

PIN DESCRIPTION (continued)

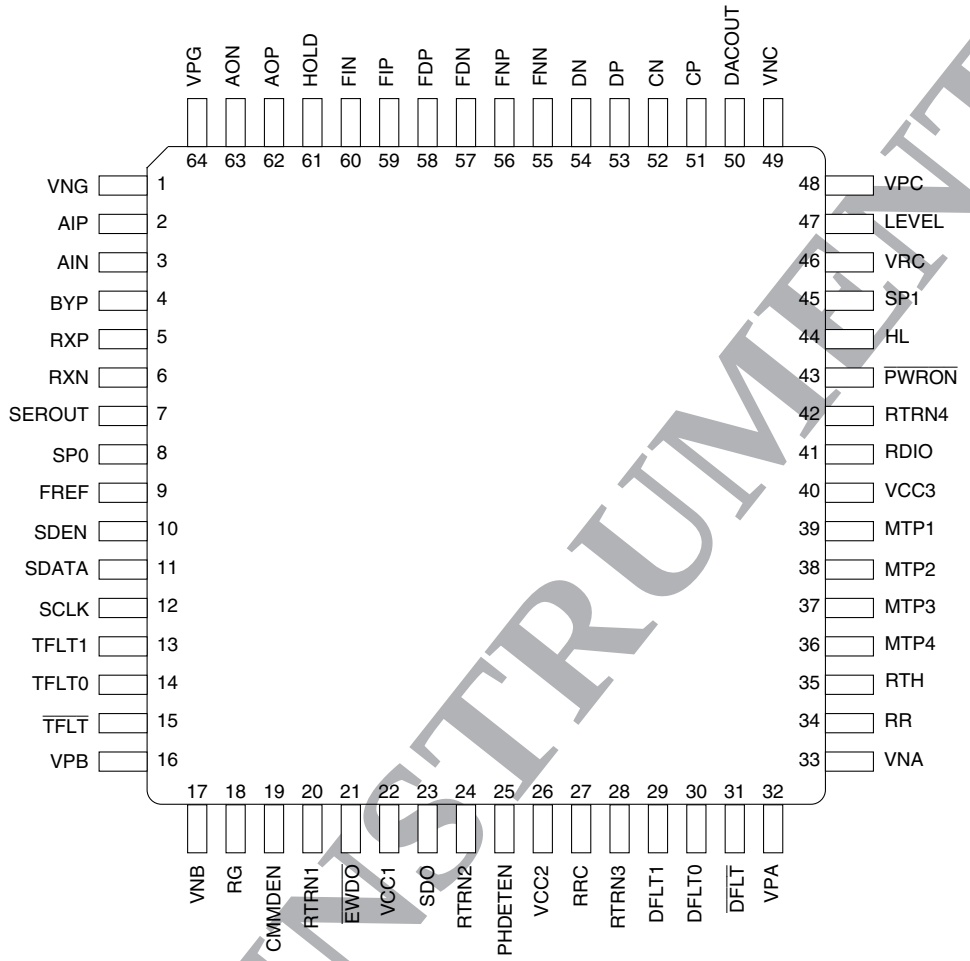
ANALOG PINS

NAME	TYPE	DESCRIPTION
BYP	-	The AGC read mode integration capacitor CBYP, is connected between BYP and VPG.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the Control B register (see Table 4). When the Write DAC is enabled by R29 Bit D5, this pin is used as the output sink.
TFLT0, TFLT1, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filters. Selection between TFLT0 and TFLT1 is done through the CA register (CAR).
DFLT0, DFLT1, $\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data synchronizer loop filters. Selection between DFLT0 and DFLT1 is done through the CB register (CBR).
LEVEL	-	An NPN emitter output that provides a full wave rectified signal from the DP, DN inputs. An external capacitor should be connected from the LEVEL to VCC to set the hysteresis threshold time constant in conjunction with the level decay current DAC (R34). The tracking threshold circuit also affects the discharge current on the LEVEL pin when enabled.
RTH	-	REFERENCE RESISTOR INPUT: An external resistor connected from this pin to VNA establishes the reference for the Tracking Threshold discharge current.
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data synchronizer and time base generator.
SEROUT	-	Buffered output of the full wave rectifier referenced to VRC.
RXP	-	REFERENCE RESISTOR INPUT: An external 9.09 kΩ, 1% resistor is connected from this pin to RXN to establish a precise reference current for the filter.
RXN	-	REFERENCE RESISTOR INPUT: An external 9.09 kΩ, 1% resistor is connected from this pin to RXP to establish a precise reference current for the filter.
VRC	-	Internal bandgap reference voltage, with respect to VCC.

SERIAL PORT PINS

SDEN	-	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDATA	-	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	-	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

PACKAGE PIN DESIGNATIONS



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 34P3211B 64-Lead TQFP	34P3211B-CGT	34P3211B-CGT

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

Abridged Version

SSI 34P3214A

Read Channel for High Density Floppy and Disk/Tape Drives

Prototype

July 1998

DESCRIPTION

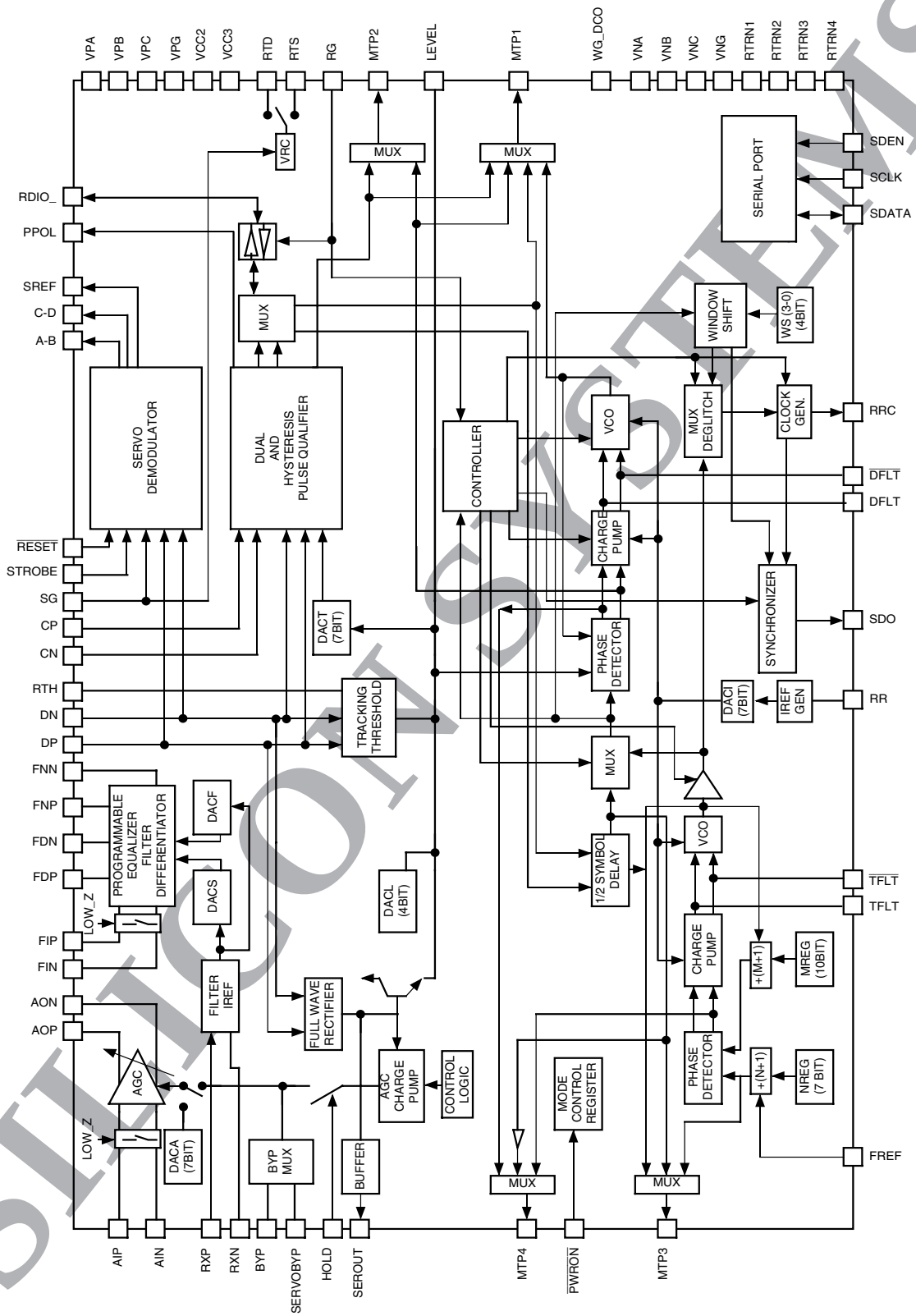
The SSI 34P3214A is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement zoned recording for high density floppy disk drive and tape applications. Functional blocks include the pulse detector, programmable filter, servo demodulator, time base generator, and data synchronizer. VCO range of 0.6 MHz to 15 MHz is selectable through the serial port. Programmable functions of the SSI 34P3214A device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone. The SSI 34P3214A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption. The SSI 34P3214A supports a sleep mode for minimal power dissipation in non-operational periods. The SSI 34P3214A is available in a 64-lead TQFP package.

FEATURES

- **Complete zoned recording application support**
- **VCO range: 0.6 MHz to 15 MHz selectable through the serial port**
- **Supports 1,7 RLL, MFM, FM, and GCR encoding format**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Programmable cutoff frequency of 0.4 to 4 MHz in data mode and servo mode**
- **Tracking threshold for rapid LEVEL discharge**
- **Time base generator with better than 1% frequency resolution**
- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data synchronizer with programmable window shift control**
- **4-burst servo capture with (A-B), (C-D) and Pulse Polarity (PPOL) ouputs**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode <8 mW)**
- **Separate settings for filter cut-off, filter boost, AGC bypass capacitor and hysteresis threshold for data mode and servo mode**
- **Low operating power (400 mW typical @ 5 V)**

SSI 34P3214A
Read Channel for High Density Floppy and Disk/Tape Drives

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 34P3214A implements a high performance complete read channel, including pulse detector, programmable active filter, servo demodulator, time base generator, data synchronizer, servo demodulator and VCO range of 0.6 MHz to 15 MHz.

PULSE DETECTOR

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (VBYP) stored on the BYP (SERVOBYP in Servo mode) hold capacitor (CBYP). A dual rate charge pump drives CBYP with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower VBYP which reduces the amplifier gain, while decay currents increase VBYP which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the correct AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the correct AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 μA acts to increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA:4 μA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 21.

When the chip is in power down mode, the AGC dual rate charge pump is disabled.

The AGC amplifier can be set into a fixed gain mode. The gain is programmable over a 2 to 51 V/V range in 0.4 V/V steps by a 7-bit DAC (DACA). If DACA = 0, the amplifier is in AGC mode. This DAC setting is stored in Bit D0 through Bit D6 of Register 9 (AGCR).

BYP CONTROL VOLTAGE

The BYP capacitor (SERVOBYP in servo mode) voltage will be held constant (subject to leakage currents) during sleep mode or when the HOLD signal is high. Upon the transition of $\overline{\text{PWRON}}$ from high to low, there is a 1 μs delay inserted during which the LOW-Z mode is activated, before the AGC charge pump is allowed to drive the BYP capacitor.

AGC MODE CONTROL

In all modes the nominal decay, nominal attack and fast attack modes are active based on the instantaneous DP/DN voltage.

HOLD SIGNAL

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, BYP (SERVOBYP in servo mode) voltage will be held constant subject to leakage currents only.

WG- SIGNAL VERSUS READ AND SERVO MODES

The WG_DCO pin is used to input WG signal to the chip when Bit D6 of Register 10 (WSCR) is set 0 (default value). While WG (i.e. Write Gate NOT) is LOW the chip is kept in LOW-Z mode, When the chip is in LOW-Z mode, the input impedances of the AGC, the filter and the pulse qualifier are kept low to allow for quick recovery of the AC coupling capacitors.

When WG has a transition from LOW to HIGH, LOW-Z modes continues for an additional 1.5 μs (nominal) and terminates. It is followed by a fast decay mode operation that provides fast recovery of the AGC gain. If RG⊕SG goes HIGH before WG signal goes HIGH, RG⊕SG takes over. It behaves as if WG is being asserted concurrently with RG⊕SG.

LOW-Z/FAST DECAY SEQUENCE AND SG SIGNAL

The Low-Z/Fast Decay sequence is triggered at the rising and falling edges of the SG signal. This is intended to recover from the possible droop in SERVOBYP and BYP capacitor voltages when either capacitor has been disconnected from the AGC.

FUNCTIONAL DESCRIPTION (continued)

FULL WAVE RECTIFIER OUTPUT

A buffered output of the Full Wave Rectifier is provided at the SEROUT pin. A 1 Vp-p signal at DP-DN will result in a 0.75 V_{pk} full wave rectified signal at SEROUT.

RDIO OUTPUT PIN

The RDIO_ output is a CMOS compatible output that is selectable between a 30 ns wide raw data signal and the RDQ signal, i.e. Q in Fig 1A & 2B. RDQ is the output of a toggle flip flop which is clocked by the raw data output signal. The signal at this pin is controlled through several bits in the serial port as shown in TABLE 1.

When RG = 0, either read data output or RDQ will appear at RDIO_ depending on R11 Bit D7. When RG = 1, RDIO_ depends on several bits as shown above. With RG = 1 and R11 Bit 6 = 1, then RDIO_ will be in HIZ mode. With RG = 1 and R11 Bit 6 = 0, then R10 (WSCR) Bit D7 determines if a signal appears on RDIO_: that signal will be either read data output or RDQ depending on R11 (MCMCR) Bit D7. When SG = 1, inverted read data output appears at RDIO_.

QUALIFIER SELECTION

The SSI 34P3214A provides both hysteresis and dual comparator pulse qualification circuits that may be selected for read mode operation. The dual comparator method is selected by setting the MSB (D7) in the data threshold control register, Register 5 (DTCR). The lower 7 bits of the DTCR also sets the hysteresis level of the comparators for read mode. The option of using a fixed threshold is also provided. Register 15 (HDCR) bit D4 allows the user to set the data threshold as fixed or driven by the LEVEL pin. If set as fixed, the threshold is set as if the DP/DN amplitude is 1 Vp-pd. Whether fixed or floating the threshold is set by the DACT value in the Bits D0-D7 of Register 5 DTCR in data mode (Register 19, SHCR in servo mode). The formula for the threshold level is shown below.

Thresh = DACT • 0.93 /127

The Threshold accuracy is ± 5% for 38 ≤ DACT ≤ 109.

TABLE 1: RDIO_ Control

		Reg 7 Bit 5	Reg 10 Bit 7	Reg 11 Bit 7	Reg 11 Bit 6	
RG	**SG**	**RDIO_**	**Gtd RDIO_**	**RDIO_/RDQ**	**RDIO_ HIZ**	**Signal**
X	X	1	X	X	X	Inverted Read Data Input
0	1	0	X	1	X	Read Data Output
0	1	0	X	0	X	RDQ
X	X	0	1	1	X	Read Data Output
X	X	0	1	0	X	RDQ
X	0	0	0	X	0	No Output
1	0	0	X	X	1	HIZ

DUAL COMPARATOR QUALIFICATION

When in dual comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The floating hysteresis threshold, VTH, is driven by a multiplying DAC (DACT) which is driven by LEVEL and referenced to VRC. The DACT setting is stored in Bits D0-D6 of the Register 5 (DTCR) (SHCR in Servo mode). Hysteresis thresholds from 30 to 80% may be set with a resolution of 1%. An external resistor/capacitor combination (RTD/CT in Data Mode and RTS/CT in Servo Mode) sets the hysteresis threshold time constant. RTD resistor is connected between LEVEL and RTD pins. RTS resistor is connected between LEVEL and RTS pins. SG signal determines which resistor is to determine the hysteresis threshold time constant. CT capacitor is connected between LEVEL pin and the positive power supply terminal. An internal DAC, DACL, can also be used to discharge the LEVEL pin. The four LSBs of the Hysteresis Decay Control Register (Register R15, HDCR) determine the value of the pull-down current. The LSB value of DACL is 3.125 μA, and DACL is offset by 1 LSB such that “0000” corresponds to 3.125 μA, and “1111” results in 50 μA. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot. Dual comparator timing is shown in Figure 1.

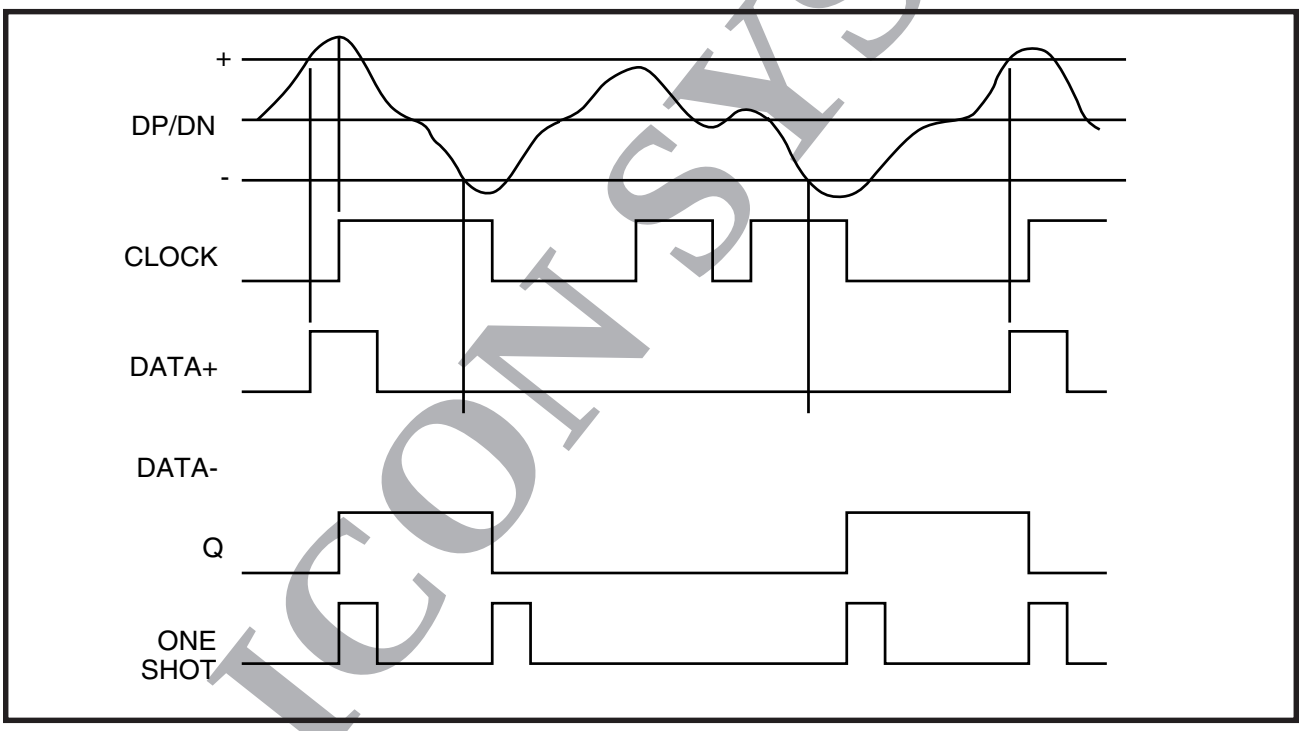


FIGURE 1: Dual Comparator Timing

FUNCTIONAL DESCRIPTION (continued)

HYSTERESIS COMPARATOR QUALIFICATION

When the hysteresis qualification mode is selected (i.e., by setting Register 5, DTCR bit D7 LOW), the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bi-directional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bi-directional one-shot. Hysteresis comparator timing is shown in Figure 2.

TRACKING THRESHOLD

The SSI 34P3214A also provides a tracking threshold. This threshold is set as a function of the Qualifier threshold, and whenever the signal at DP-DN is greater than the tracking threshold, the LEVEL pin has an extra discharge current. The magnitude of the discharge current is determined by the RTH resistor and Bits D0-D2 of R13 (TTCR). The value of the tracking threshold depends on Bits D4-D6 of R13(TTCR) and the formula for the threshold is:

Tracking threshold = (0.3 +(n1 • 0.1)) • Thresh

Thresh = qualifier threshold as defined above and n1 is defined below.

The formula for the tracking threshold discharge current is:

I(LEVEL) = (1.5/RTH) • (n2/2)

Where n2 is defined in TABLE 2.

The tracking threshold current is in addition to the LEVEL Decay Current set in R15 (HDCR) and the two currents are independent of each other. The minimum value of the RTH resistor is 30 kΩ. The entire tracking threshold circuit can be disabled and powered down by setting D6 of R15 to HIGH.

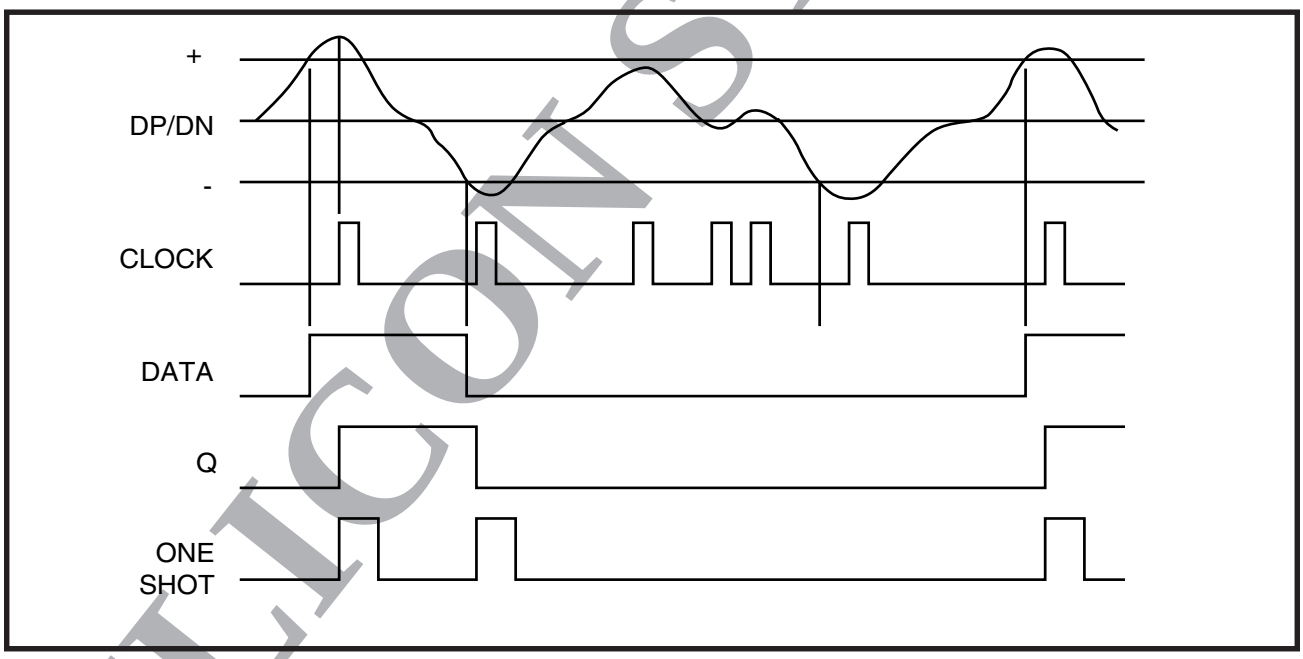


FIGURE 2: Hysteresis Comparator Timing Diagram

TABLE 2

R13 Bit D6	R13 Bit D5	R13 Bit D4	n1	R13 Bit D2	R13 Bit D1	R13 Bit D0	n2
0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1
0	1	0	2	0	1	0	2
0	1	1	3	0	1	1	3
1	0	0	4	1	0	0	4
1	0	1	5	1	0	1	5
1	1	0	6	1	1	0	6
1	1	1	7	1	1	1	7

SERVO DEMODULATOR

The SSI 34P3214A servo section captures four separate servo bursts and provides (A-B) and (C-D) burst outputs. The pulse polarity signal, PPOL, is also provided at the PPOL pins. Internal burst hold capacitors are provided to support low leakage burst capture and reduce external component count. To support embedded servo applications, the SSI 34P3214A provides additional programming registers that sets the filter cutoff frequency (FC), filter boost (FB) and hysteresis threshold level (VTH), for servo mode. The programmable functions are switched automatically when servo gate (SG) is asserted, reducing the transition time between mode changes.

Servo mode operation: With SG transition from Logic-0 to Logic-1, i.e., into servo mode, the following events occur:

- the filter cutoff frequency FC is controlled by the Servo Cutoff Register (R16, SFCR)
- the filter boost function is controlled by the Servo Boost Register (R17, SBCR)
- the qualification threshold percentage is controlled by the Servo Threshold Register (Register 19, SHCR)
- RTS servo time constant setting resistor is connected to VRC, the internal bandgap reference. RTD is disconnected.
- SERVOBYP capacitor is connected to AGC

By providing the servo cutoff control register for FC and servo boost control register for FB, the servo signal to noise ratio can be greatly improved. When SG is activated or deactivated, there is a nominal 0.3 ms settling time for the internal DACs to recover from the register switching.

Typically, a servo preamble is used to achieve the desired AGC level and then the HOLD pin is asserted to hold the AGC gain.

Burst Capture: Burst capture for the SSI 34P3214A is controlled by a single external pin designated STROBE and an internal counter. When SG is active, the first pulse on the STROBE pin gates the output of the servo peak detector to the A burst hold capacitor. The capacitor charges for as long as the STROBE pulse is HIGH. On the falling edge of STROBE, the internal counter is incremented . The next STROBE pulse will then gate the servo peak detector output to the B burst hold capacitor. Again the capacitor charges as long as the STROBE pulse is HIGH. On the falling edge of STROBE, the counter is incremented again and the C burst is captured on the next STROBE pulse. On the next falling edge of STROBE, the counter is incremented again and the D burst is captured on the next STROBE pulse. After the falling edge of the fourth STROBE pulse, the counter is set to zero and the burst capture process can be repeated. The internal counter is also reset when the SG pin is deactivated. The voltage level on each hold capacitor is then provided to subtracting buffer amplifiers which generate the (A-B) and (C-D) servo output signals. (A-B) and (C-D) signals are referenced to the voltage at SREF output pin. SREF pin provides a zero-signal baseline voltage, which is nominally 2.51 V. A 1.0 Vp-p differential voltage at the DP/DN pins will result in 1 V peak burst amplitude around SREF voltage. That is for instance, if A burst is

1.0 Vp-p and B burst is 0.6 Vp-p, then (A-B) output is 3.11 V, i.e., equals 2.51 + 1 - 0.6. The hold capacitors are discharged when $\overline{\text{RESET}}$ pin is driven LOW. The $\overline{\text{RESET}}$ control input overrides the STROBE signals. The drive current of the servo peak detector charge pump is set by a 4-bit word addressed through the serial port. The LSB is 6 μA, and the offset is 1 LSB such that "0000" corresponds to 6 μA and "1111" results in 96 μA. Maximum noise immunity is obtained in the servo peak detector by choosing the smallest value of charge current to the internal 10 pF hold capacitor during the burst acquisition time.

PROGRAMMABLE FILTER

The SSI 34P3214A contains an electronically controlled 7-pole low-pass filter. The transconductance-capacitance (gm-C) filter approximates a linear phase or constant group delay response. Programmable bandwidth and boost/equalization are provided by internal 7-bit control DACs. Differentiation pulse slimming equalization which does not affect the filter's group delay response is accomplished by two programmable complimentary real axis zeros. Programmable phase equalization is also available, providing up to ±20% variation in low-frequency group delay value.

The filter implements a 0.05° equiripple linear phase response. The normalized transfer function (i.e. $s = j\omega_c = j2\pi f_c$, where $j^2 = -1$) is:

$$V_o/V_i = H_{14} \bullet H_2 \bullet H_3$$

where

$$H_{14} = \frac{[-2.54628\ \alpha\ s^2 + 2.76833\ \beta\ s + 1.13440\ (1 - \alpha)]}{(s^3 + 2.54628\ s^2 + 2.76833\ s + 1.13440)}$$

$$H_2 = 5.37034/(s^2 + 1.14558\ s + 5.37034)$$

$$H_3 = 2.95139/(s^2 + 1.54203\ s + 2.95139)$$

The normalized pole frequencies and quality factors of the biquads and bicubic sections are:

$\omega_1 = 1.14762$ $Q_1 = 0.68110$

$\omega_2 = 2.3174$ $Q_2 = 2.02290$

$\omega_3 = 1.71746$ $Q_3 = 1.11409$

$\omega_4 = 0.86133$

The frequency is denormalized by replacing s by $s/2\pi F_c$. The parameters α and β are discussed below. α is always positive, and β can be positive or negative.

The differential signals from the AGC are AC coupled to the inputs of the filter. The programmable bandwidth and boost/equalization features are controlled by internal DACs whose registers are programmable by the serial port. The current reference for the frequency DACF is set using a single external resistor connected from pin RXP to RXN. No external components are required for the boost/equalization control.

The programmable bandwidth is set by the filter cutoff register DACF in data mode according to the following equation.

$$Fc = 4/127 \bullet FCDAC$$

The data mode cutoff register R6, DMCR (Bits D0-D6 of R16, SFCR in Servo mode) is used to determine the filter's unboosted -3 dB cutoff frequency (Fc). This is the -3 dB frequency for both α and β equal to 0. When boost/equalization is added, the actual -3 dB point will move out, as discussed below.

The filter's magnitude and group delay characteristics can be altered by adjusting the parameters α and β. α boosts the filter response at high frequencies while leaving the group delay unaltered. The effect on read data pulses is symmetrical slimming. β controls the filter's phase or group delay response. β boost is necessary to correct asymmetry in incoming data pulses. A side effect of β group delay equalization is a slight change in magnitude response.

ALPHA BOOST (MAGNITUDE EQUALIZATION)

The SSI 34P3214A employs a novel magnitude equalization scheme in which the filter's magnitude characteristics for different values of α pivot around a point of constant gain. The normalized constant gain pivot point is $\omega_p = 0.6675$. As shown in Figure 3, for nonzero values of α, the filter gain for frequencies above ωp is increased, while frequencies below ωp are attenuated. The advantages of this new technique over the conventional realization, which only boosts higher frequencies, are faster AGC recovery between modes and reduced AGC dynamic range requirements.

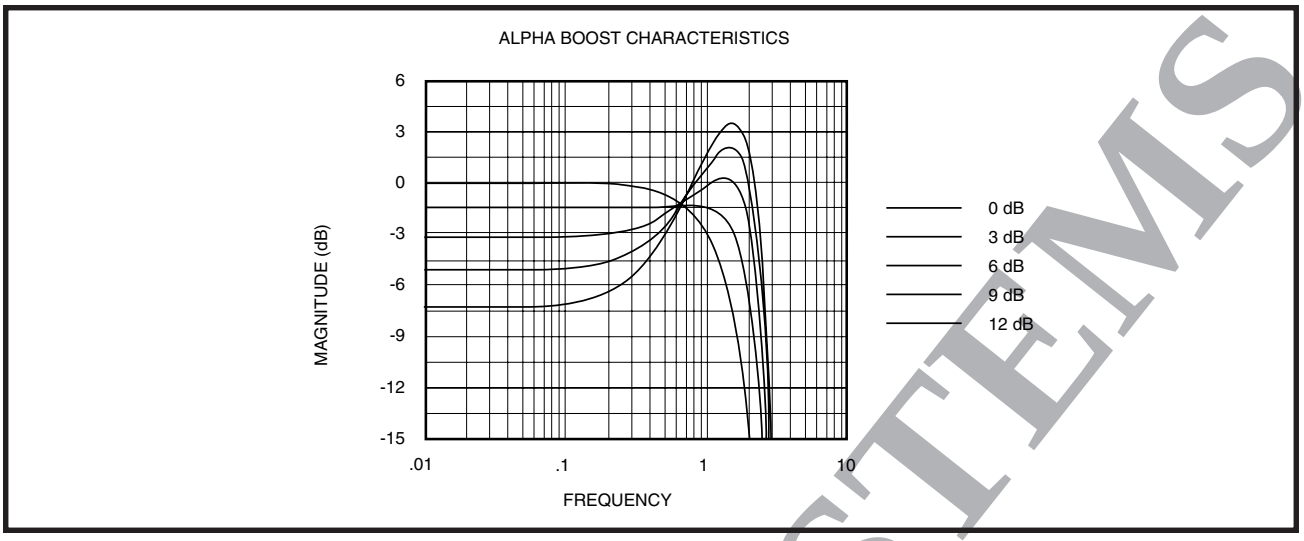


FIGURE 3: Pivoting Alpha Boost Magnitude Characteristics

Alpha Boost ($\alpha \neq 0$, $\beta = 0$) does not affect the filter's group delay response. The Data Mode Boost Register R2, DBCR is used to determine the filter's Alpha Boost. The Alpha boost is controlled by R17, SBCR if Servo mode gate (SG) is asserted. The amount of alpha boost that will be added to the unboosted -3 dB cutoff frequency (F_c) is set by the Filter Boost DACS according to the following equation:

Alpha Boost = 20 log10 [0.02 • DACS + 1] (dB)

For example, with DACS set for maximum output, there will be 12 dB of boost added at F_c. This will result in the gain at F_c being 9 dB higher than at DC, versus being -3 dB when unboosted. In absolute values, the DC gain will become -7.35 dB and the gain at F_c will equal 1.65 dB. TABLE 2 provides information on alpha boost versus α ($\beta = 0$), DACS, DC gain and gain at F_c.

If alpha boost is applied, the minimum amount must be 1 dB. DACS values should equal 0 or 5 - 127. Values 1, 2, 3, and 4 are invalid.

TABLE 2: Alpha Boost Versus α ($\beta = 0$)

α BOOST (dB)	α	DACS	DC GAIN ($\omega = 0$) (dB)	GAIN AT F_c (dB)
0	0.00000	0	0	-3
1	0.05156	5	-0.47	-2.47
2	0.10342	11	-0.95	-1.95
3	0.15526	18	-1.47	1.47
4	0.20671	25	-2.02	-1.02
5	0.25746	33	-2.59	-0.59
6	0.30719	42	-3.19	-0.19
7	0.35562	53	-3.82	0.18
8	0.40247	64	-4.48	0.52
9	0.44755	77	-5.16	0.84
10	0.49066	92	-5.86	1.14
11	0.53167	109	-6.59	1.41
12	0.57047	127	-7.35	1.65

PROGRAMMABLE FILTER (continued)

BETA BOOST (GROUP DELAY EQUALIZATION)

When $\beta = 0$, the 7-pole filter approximates a constant group delay response delay response in equiripple sense over a normalized frequency range between DC and $\omega \cong 2$. For $\omega = 0$, the group delay equals:

$GDL(0) = 1/(\omega_1 Q_1) + 1/(\omega_2 Q_2) + 1/(\omega_3 Q_3) + 1/\omega_4$ ($\beta = 0$)

The denormalized filter group delay at DC as a function of F_c is therefore:

$GDL(0) = 3.17630 / (2\pi F_c)$ (seconds, $\beta = 0$)

By applying beta boost ($\alpha = 0$, $\beta \neq 0$) the group delay response of the filter can be altered, and given a positive or negative slope as shown in Figure 4.

The group delay Δ% is defined as the percentage change in absolute group delay value at $F_c/10$ with respect to that without the equalization applied ($\beta = 0$). The group delay Δ% at low frequencies can be programmed between -20% and +20% by means of DACG which is controlled by R12, GDCR. The MSB of R12 acts as a sign bit, as follows:

Group Delay Δ% = -0.15748 • DACG (%)

where $0 \leq DACG \leq 127$
or

Group DelayΔ% = 0.15748 • (DACG - 128) (%)

where $128 \leq DACG \leq 255$

The relationship between β, DACG and group delay Δ% is given in TABLE 3.

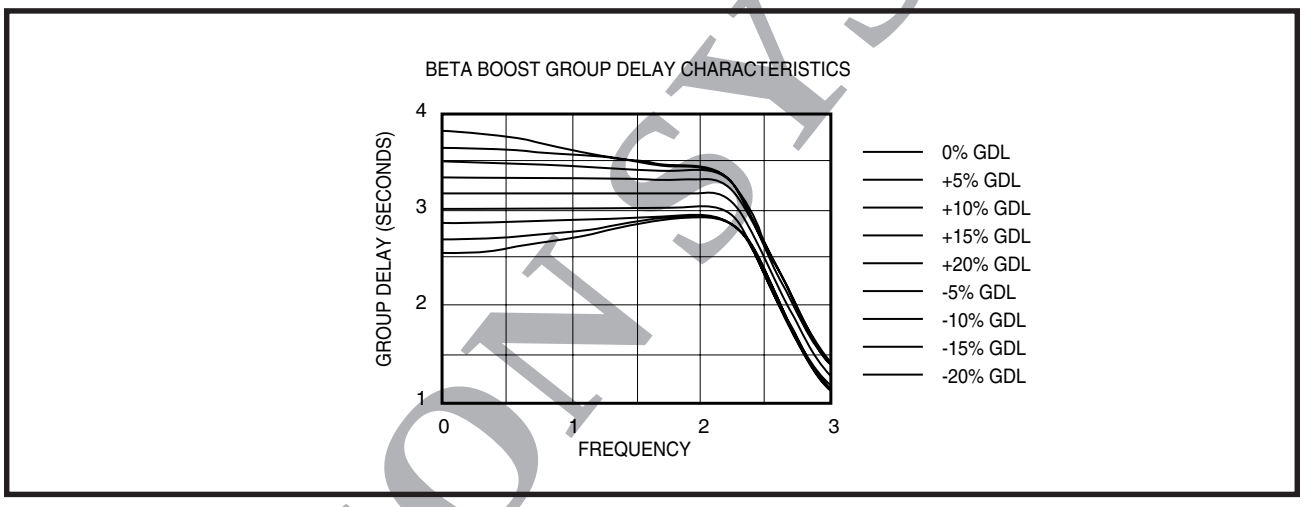


FIGURE 4: Beta Boost Group Delay Characteristics

TABLE 3: Group Delay Δ%, β and Beta Boost ($\alpha = 0$)

GROUP DELAY (Δ%)	β	DACG
-20	0.26030	127
-15	0.19523	96
-10	0.13015	64
-5	0.06508	32
0	0.00000	0
5	-0.06508	160
10	-0.13015	192
15	-0.19523	224
20	-0.26030	255

COMBINED ALPHA AND BETA BOOST

A side effect of β group delay equalization is a small amount of non-pivoting high-frequency magnitude boost. However, when both $\alpha \neq 0$ and $\beta \neq 0$, the total amount of boost is largely dominated by alpha boost only. TABLE 4 lists the actual boost versus alpha boost and percentage group delay variation. Figures 5 and 6 illustrate the effect of beta boost for alpha boost equal to 0 dB and 12 dB respectively.

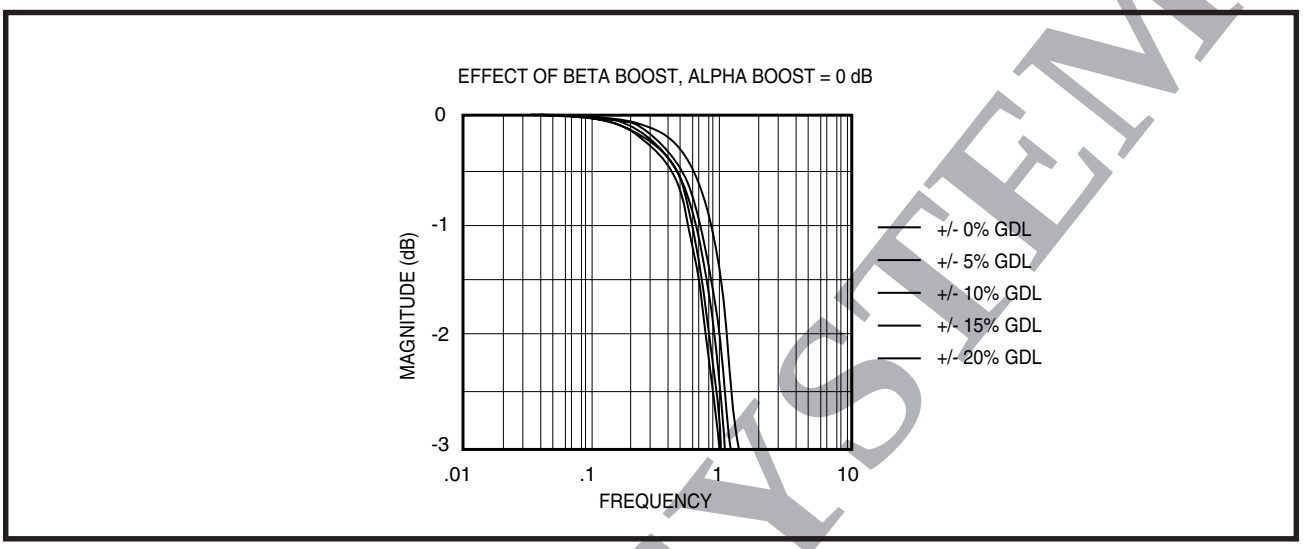


FIGURE 5: Effect of Beta Boost for Alpha Boost = 0 dB

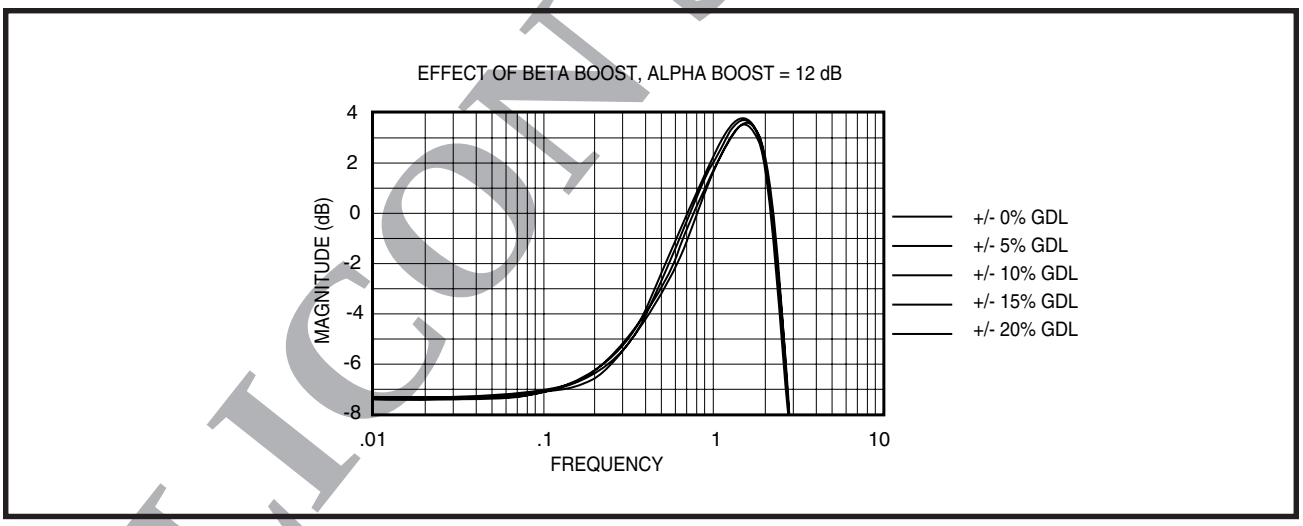


FIGURE 6: Effect of Beta Boost for Alpha Boost = 12 dB

PROGRAMMABLE FILTER (continued)

TABLE 4: Actual Bosost vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%
0	1.46	0.88	0.41	0.09	0.00
1	2.31	1.78	1.36	1.09	1.00
2	3.18	2.70	2.32	2.08	2.00
3	4.07	3.63	3.29	3.07	3.00
4	4.98	4.57	4.26	4.06	4.00
5	5.89	5.59	5.23	5.05	5.00
6	6.82	6.48	6.21	6.05	6.00
7	7.76	7.44	7.20	7.04	7.00
8	8.71	8.41	8.18	8.04	8.00
9	9.66	9.38	9.17	9.03	9.00
10	10.62	10.35	10.16	10.03	10.00
11	11.58	11.33	11.15	11.03	11.00
12	12.55	12.32	12.14	12.03	12.00

The -3 dB frequency (F_{-3dB}) is defined as the frequency for which the filter gain is 3 dB below the gain at DC. For $\alpha = 0$ and $\beta = 0$, $F_{-3dB} = F_c$ and the gain at F_{-3dB} equals -3 dB. When boost is applied F_{-3dB} increases. As a result of the pivoting alpha boost, the DC gain and hence the gain at F_{-3dB} also changes. TABLE 5 gives the ratio between F_c and F_{-3dB} as a function of alpha boost and Δ% group delay variation and the gain at F_{-3dB}.

While the amount of boost is defined at F_c, the peak in the magnitude transfer function occurs at a different frequency. Tables 6 and 7 contain the ratios of F_{peak}/ F_c and the gain at F_{peak} as a function of alpha boost and Δ% group delay variation, respectively.

TABLE 5: F_{-3dB}/F_c vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%	GAIN AT F-3 dB (dB)
0	1.32	1.18	1.07	1.02	1.00	-3.00
1	1.54	1.41	1.30	1.23	1.21	-3.47
2	1.76	1.66	1.58	1.52	1.51	-3.95
3	1.95	1.89	1.85	1.81	1.80	-4.47
4	2.12	2.09	2.06	2.04	2.04	-5.02
5	2.25	2.23	2.21	2.21	2.20	-5.59
6	2.35	2.34	2.33	2.33	2.33	-6.19
7	2.44	2.43	2.43	2.43	2.43	-6.82
8	2.52	2.52	2.51	2.51	2.51	-7.48
9	2.60	2.59	2.59	2.59	2.59	-8.16
10	2.67	2.67	2.66	2.66	2.66	-8.86
11	2.74	2.73	2.73	2.73	2.73	-9.59
12	2.81	2.80	2.80	2.80	2.80	-10.35

TABLE 6: Fpeak/Fc vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%
0	no peak	no peak	no peak	no peak	no peak
1	no peak	no peak	no peak	no peak	no peak
2	0.74	0.56	no peak	no peak	no peak
3	0.95	0.88	0.80	0.73	0.71
4	1.10	1.08	1.06	1.05	1.04
5	1.22	1.22	1.22	1.22	1.22
6	1.30	1.30	1.31	1.32	1.32
7	1.35	1.37	1.37	1.38	1.38
8	1.39	1.41	1.42	1.42	1.42
9	1.43	1.44	1.45	1.45	1.46
10	1.45	1.46	1.47	1.48	1.48
11	1.47	1.48	1.49	1.49	1.50
12	1.49	1.50	1.51	1.51	1.51

TABLE 7: dB Gain @ F_{peak} vs. Alpha Boost and Δ% Group Delay Variation

α BOOST (dB)	±20%	±15%	±10%	±5%	0%
0	no peak	no peak	no peak	no peak	no peak
1	no peak	no peak	no peak	no peak	no peak
2	-0.59	-0.89	no peak	no peak	no peak
3	0.38	0.80	1.09	1.27	1.32
4	0.00	-0.42	-0.74	-0.95	-1.02
5	0.48	.10	-0.19	-0.37	-0.43
6	1.00	0.68	0.43	0.27	0.22
7	1.53	1.25	1.04	0.90	0.86
8	2.04	1.79	1.61	1.50	1.47
9	2.52	2.31	2.15	2.06	2.03
10	2.97	2.79	2.65	2.57	2.54
11	3.39	3.22	3.10	3.03	3.00
12	3.77	3.62	3.51	3.45	3.43

FUNCTIONAL DESCRIPTION (continued)

TIME BASE GENERATOR

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL. The filter is connected to pins TFLT & $\overline{\text{TFLT}}$.

In read, servo and idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1))FREF

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the data recovery control register R3, (DRCR). This DAC, DACI, also sets the 1/2 symbol delay, VCO center frequency, and phase detector gain for the data synchronizer circuitry. The VCO center frequency is also a function of bit 7 in the DRCR. The formula for the VCO center frequency is:

FVCO = [12.5/(RR + .4)] • S •
(42 • DACI + 16.5) kHz

S = 3, if R3 (DRCR) bit7 = 1

S = 1, if R3 (DRCR) bit7 = 0

When changing frequencies, the M and N registers must be loaded first, followed by the DRCR register. A frequency change is initiated only when the DRCR register has been changed.

DATA SYNCHRONIZER

In the read mode, the data synchronizer performs data synchronization. Data rate is established by the time base generator and the internal reference DACI controlled by the DRCR register. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/2 symbol delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the read mode and servo and non-harmonic in the idle and servo modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{\text{DRD}}$ pulse. In the idle mode and servo mode the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL. The filter is connected to pins DFLT & $\overline{\text{DFLT}}$.

MODE CONTROL

The read gate (RG) and servo gate (SG) inputs control the device operating mode. RG and SG are asynchronous inputs and may be initiated or terminated at any time. When RG = 0 the SDO output is put in HIZ mode.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/2 symbol wide (A VCO period, TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock. Read data synchronization waveforms are shown in Figure 7. Bit D5 of register R15 (HDCR) controls the input to the data synchronizer. If bit D5 is HIGH then RD is the input to the synchronizer instead of $\overline{DRD}$. This mode can have advantages when the data contains consutive 1's. If this is the case and two of these pulses are shifted towards one another, the $\overline{DRD}$ one shot may mask the second pulse. For normal operation bit D5 of register R15 should be set LOW.

PREAMBLE SEARCH

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read data, RD. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time, an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit D3, in the Control B (Register 7, CBR) register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 11 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the data follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 pulses from assertion of RG) and then asserts an internal VCO lock signal. When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period, the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the "gain shift" bit (Register 7 (CBR) , bit D3) is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 11 transitions.

WINDOW SHIFT

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (Register R10, WSCR).

DATA SYNCHRONIZER (continued)

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift Control Register (Register R10, WSCR). The description of the six LSB's of WSCR register (R10) are as follows:

WINDOW SHIFT CONTROL REGISTER (R10, WSCR)

BIT	NAME	FUNCTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0 = early, 1 = late
5	WSE	Window shift enable

Window shift early and window shift late waveforms are shown in Figure 7. The window shift magnitude is set as a percentage of the full decode window, in 2.4% steps. This results in a window shift capability of ± 36%. The tolerance of the window shift magnitude is ± 20%. Window shift should be set during idle mode.

WS3	WS2	WS1	WS0	SHIFT MAGNITUDE
1	1	1	1	No shift
1	1	1	0	2.4% (minimum shift)
1	1	0	1	4.8%
1	1	0	0	7.2%
1	0	1	1	9.6%
1	0	1	0	12%
1	0	0	1	14.4%
1	0	0	0	16.8%
0	1	1	1	19.2%
0	1	1	0	21.6%
0	1	0	1	24%
0	1	0	0	26.4%
0	0	1	1	28.8%
0	0	1	0	31.2%
0	0	0	1	33.6%
0	0	0	0	36% (maximum shift)

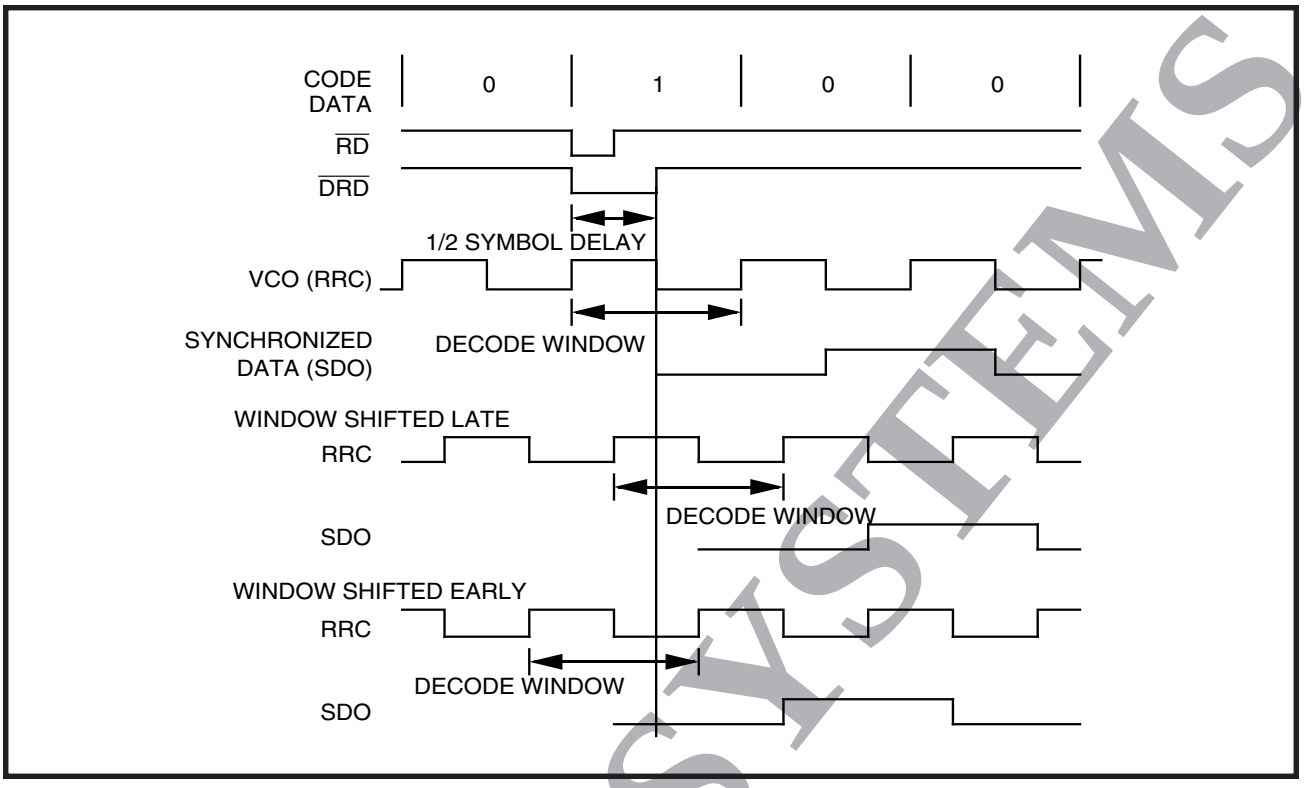


FIGURE 7: Read Data Synchronization Waveforms

NON READ MODE (RG = 0)

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

SERVO MODE (SG = 1)

Servo mode is entered by asserting the servo gate (SG) while the RG is held low. During servo mode the VCO and the RRC are referenced to the internal time base generator signal.

OPERATING MODES AND CONTROL

The SSI 34P3214A has several operating modes that support read, servo, and power management functions. Mode selection is accomplished by controlling the read gate (RG), servo gate (SG), and $\overline{\text{PWRON}}$ pins. Additional modes are also controlled by programming the Power Down Control Register (Register R1, PDCR), the Control A Register (Register R14, CAR), and the Control B Register (Register R7, CBR) via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), servo gate (SG), and $\overline{\text{PWRON}}$ pins with CMOS compatible signals. For normal operation the $\overline{\text{PWRON}}$ pin is driven low. During normal operation the SSI 34P3214A is controlled by RG and SG pins. When RG is HIGH and SG is LOW the device is in read mode. When SG is HIGH and RG is LOW the device is in servo mode. If RG and SG are both LOW or both HIGH the device will be in idle mode.

TABLE 8: Mode Control TABLE

CONTROL LINE $\overline{\text{PWRON}}$	RG	SG	DEVICE MODE
1	X	X	SLEEP MODE: All functions are powered down. The serial port registers remain active and register programming data is saved.
0	0	1	SERVO MODE: Pulse detector and the servo demodulator are active. RDIO_ is on.
0	1	0	READ MODE : The pulse detector is active. The data synchronizer begins preamble lock sequence. RDIO_ is inactive.
0	0	0	IDLE MODE: The contents of the PDCR determine which blocks are powered up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC.
0	1	1	Conflict: mapped to IDLE mode internally

CONTROL REGISTERS

Control registers R14 (CAR) and R7 (CBR) and R11(MCMCR) allow the user to configure the SSI 34P3214A test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the time base generator. CBR controls functions of the data synchronizer. R11 controls test point output selection and DAC test points. The bits of the CAR and CBR registers are defined as follows:

CONTROL REGISTER CAR (R14):

BIT	NAME	DESCRIPTION
0	EPDT	Enable phase detector (time base generator)
1	UT	Pump up (TFLT sources current, $\overline{\text{TFLT}}$ sinks current)
2	DT	Pump down (TFLT sinks current, $\overline{\text{TFLT}}$ sources current)
3	TBG KD	Change phase detector gain by a factor of 3
4	BYPT	Bypass time base generator circuit function

CONTROL REGISTER CBR (R7):

BIT	NAME	DESCRIPTION
0	EPDD	Enable phase detector (data synchronizer)
1	UD	Pump up (sources current, $\overline{\text{DFLT}}$ sinks current)
2	DD	Pump down (DFLT sinks current, $\overline{\text{DFLT}}$ sources current)
3	GS	Enable phase detector gain shifting
4	DST	DS test mode
5	RDIO_	Select input (logic 1) or output (logic 0)

TABLE 9: Multiplexed Test Point Signal Selection

Test point selection and DAC testing is defined as follows:

MTPE	TMS1	TMS0	MTP1	MTP2	MTP3	MTP4
1 X	X	OFF	OFF	OFF	OFF	
0 0	0	VCOREF	$\overline{\text{VCOREF}}$	OFF	$\overline{\text{DRD}}$	
0 0	1	SET	RESET	DSREF	MCTR	
0 1	0	PDQ	$\overline{\text{PDQ}}$	$\overline{\text{PUQ}}$	PUQ	
0 1	1	RD	SET	NCTR	MCTR	

VCOREF = Data synchronizer VCO reference clock

DSREF = Output of the time base generator

MCTR = M counter output of the time base generator

RD = Read MO data output from the pulse qualifier

PDQ/PUQ = Data synchronizer phase detector monitor points

NCTR = N counter output of the time base generator

RESET = Output of the negative threshold comparator

SET = Output of the positive threshold comparator

TTCOMP = Output of the Tracking Threshold comparator

TABLE 10: DACOUT Signal Selection

TDAC1	TDAC0	DAC MONITORED
0	0	Filter DACs
0	1	Qualifier threshold DAC (VTH)
1	0	Window shift DAC
1	1	Servo peak detector

The test of the filter DACs is controlled through the serial port. When the MSB of R6 (DMCR) is set to 1, the Fc DAC test is selected. When the MSB of R2 (DBCR) is set to 1, the Boost DAC test is selected. When the MSBs of R4 (NCCR) Group Delay DAC is selected.

POWER DOWN CONTROL

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (Register 1, PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought HIGH, the device is placed into sleep mode (<5 mW) and all circuits are powered down except the serial port and the power-on reset circuitry. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is driven LOW, the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in TABLE 11. Power control timing is shown in Figure 9.

Bits 7 and 6 of the PDCR register control the speed of the CMOS output buffers according to the following table:

TABLE 16

BIT 1	BIT 0	
0	0	slow
0	1	medium
1	0	fast
1	1	very fast

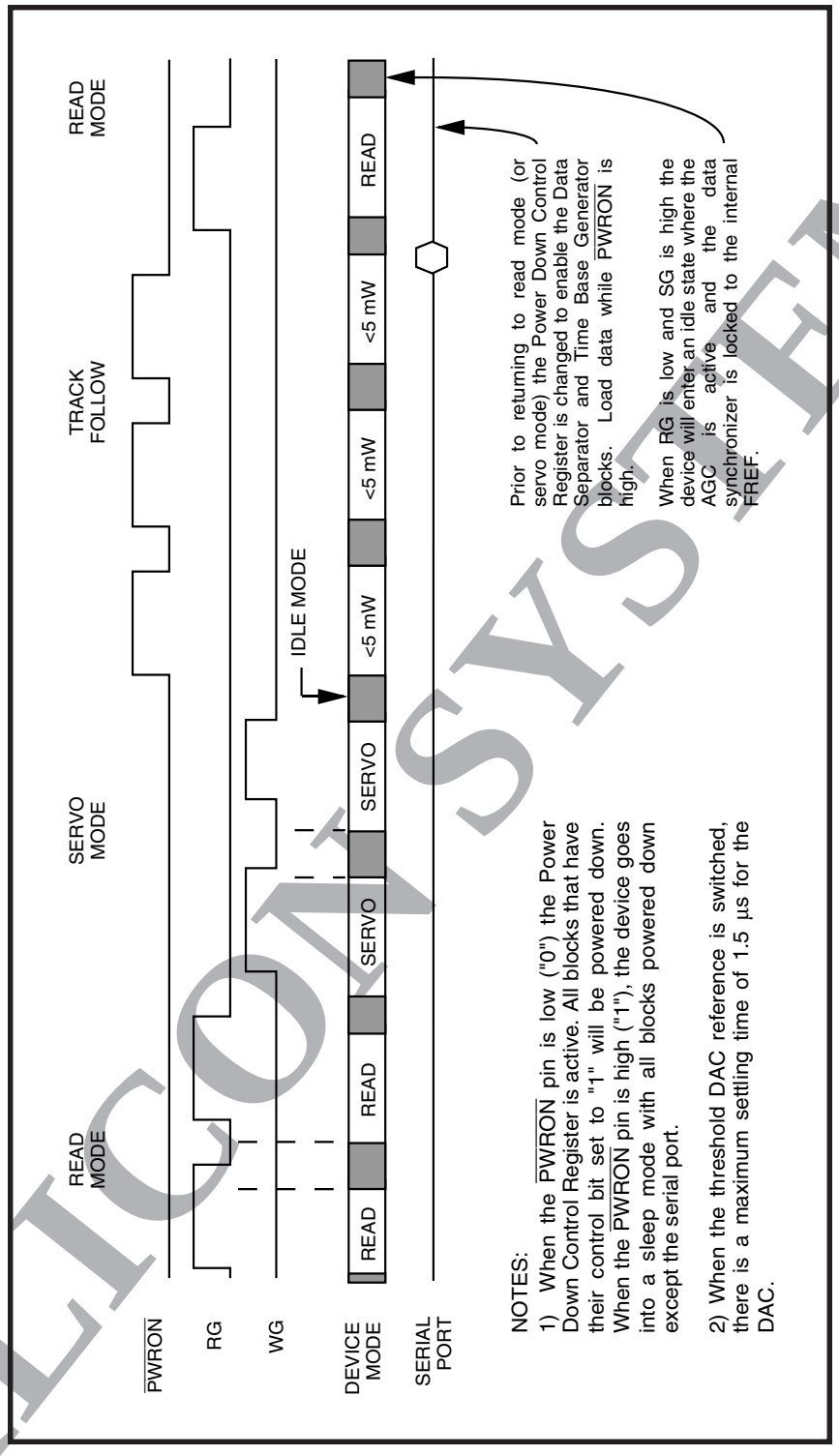


FIGURE 9: Power Control Timing

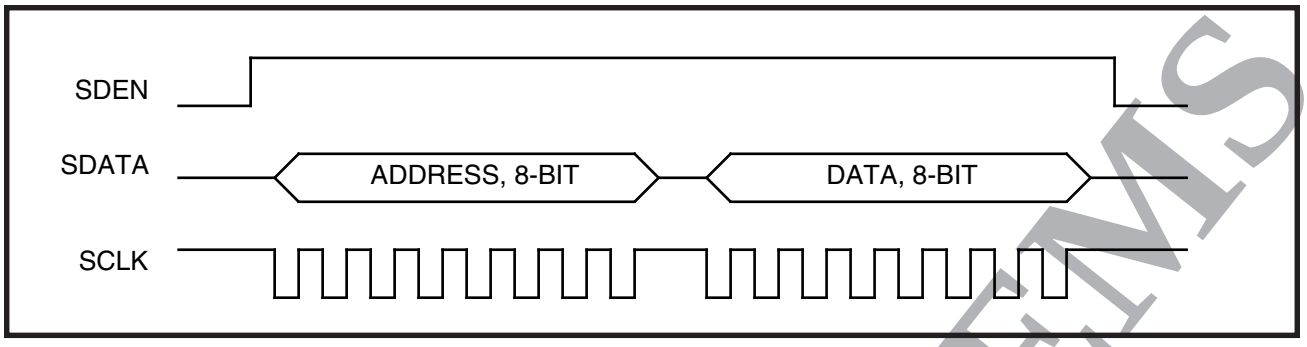


FIGURE 10: Serial Port Data Transfer Format

SERIAL INTERFACE

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 34P3214A. There exist twenty registers and an ID register. The ID register is register zero, can not be programmed and provides identification and version information. The register mapping information of the twenty registers are listed in TABLE 11. The serial port data transfer format is shown in Figure 10. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

Each 16-bit transfer consists of 1 Read/Write instruction bit (R/W), 7 address bits, and 8 data bits. The instruction bit is used as a flag to put the port into read or write mode. The address bits select the desired device and an internal data register. The address and data fields are transmitted MSB first (where MSB is defined as Bit 7), LSB last. When writing to the internal registers, R/W must be LOW (logic “0”), followed by the address and data packets. When reading from the internal registers, R/W must be HIGH (logic “1”), followed by the address field. The SSI 34P3214A will return the contents of the addressed register during the 8-bit data field. Note that in read mode there is a turn-around time (T_{trn}) for the selected register to respond with data.

The serial port has a power-on reset function which loads default values into the registers when power is first applied to the chip, or when a write is attempted to the I.D. register. The default values for twenty registers are listed in TABLE 12.

During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 11. The bits of Register 19 (STCR) will be ineffective after packaging.

TABLE 11: Serial Port Register Map

REG#	REGISTER NAME	ADDRESS A6						A0	R/W	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R1	POWER DOWN CONTROL REGISTER (PDCR)	0	0	0	0	0	0	1	0	I/O SPEED Bit 1	I/O SPEED Bit 0	MTPE 1 = Disable 0 = Enable	DS 1 = Disable 0 = Enable	TBG 1 = Disable 0 = Enable	FILTER 1 = Disable 0 = Enable	SERVO 1 = Disable 0 = Enable	PD 1 = Disable 0 = Enable
R2	DATA MODE BOOST COUNT REGISTER (PDCR)	0	0	0	0	0	0	1	0	bstdac tst 1 = Enable 0 = Disable	DACS Bit 6	DACS Bit 5	DACS Bit 4	DACS Bit 3	DACS Bit 2	DACS Bit 1	DACS Bit 0
R3	DATA RECOVERY CONTROL REGISTER (DRCR)	0	0	0	0	0	0	1	1	Vco Freq 1 = High 0 = Low	DACI Bit 6	DACI Bit 5	DACI Bit 4	DACI Bit 3	DACI Bit 2	DACI Bit 1	DACI Bit 0
R4	N COUNTER CONTROL REGISTER (NCCR)	0	0	0	0	0	1	0	0	gd dac tst 1 = Enable 0 = Disable	N Count Bit 6	N Count Bit 5	N Count Bit 4	N Count Bit 3	N Count Bit 2	N Count Bit 1	N Count Bit 0
R5	DATA THRESHOLD CONTROL REGISTER(DTCR)	0	0	0	0	0	1	0	1	Data Qual 1 = Dual 0 = Hyst	DACT Bit 6	DACT Bit 5	DACT Bit 4	DACT Bit 3	DACT Bit 2	DACT Bit 1	DACT Bit 0
R6	DATA MODE CUTOFF REGISTER (DMCR	0	0	0	0	0	1	1	0	fc dac tst 1 = Enable 0 = Disable	DACF Bit 5	DACF Bit 5	DACF Bit 5	DACF Bit 5	DACF Bit 2	DACF Bit 1	DACF Bit 0
R7	CONTROL B REGISTER (CBR)	0	0	0	0	0	1	1	1		WG_DCO 0 = WG_ 1 = DACOUT	RDIO 1 = Input 0 = Output	DS Test 1 = Enable 0 = Disable	Gain Shift 1 = On 0 = Off	Pump Down 1 = On 0 = Off	Pump Up 1 = On 0 = Off	Phase Det 1 = Enable 0 = Disable
R8	M COUNTER LSB REGISTER (MCLCR)	0	0	0	0	1	0	0	0	M Count Bit 7	M Count Bit 6	M Count Bit 5	M Count Bit 4	M Count Bit 3	M Count Bit 2	M Count Bit 1	M Count Bit 0
R9	AGC GAIN CONTROL REGISTER (AGCR)	0	0	0	0	1	0	0	1	FD TST 1 = Enable 0 = Disable	DACA Bit 6	DACA Bit 5	DACA Bit 4	DACA Bit 3	DACA Bit 2	DACA Bit 1	DACA Bit 0
R10	WINDOW SHIFT CONTROL REGISTER (WSCR)	0	0	0	0	1	0	1	0	Gtd RDIO 0 = Gated 1 = On		WIN SHFT 1 = Enable 0 = Disable	WS DIR 1 = Late 0 = Early	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$

TABLE 11: Serial Port Register Map (continued)

REG#	REGISTER NAME	ADDRESS A6						A0	R/W	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R11	M COUNTER MSB REGISTER (MCMCR)	0	0	0	0	1	0	1	1	RDIO/RDQ 1 = RDIO 0 = RDQ	RDIO hiz 1 = Rg Cont 0 = Off	TMS1	TMS0	TDAC1	TDAC0	M Count Bit 9	M Count Bit 8
R12	GROUP DELAY EQ REGISTER (GDCR)	0	0	0	0	1	1	0	0	SIGN	DACG BIT 6	DACG BIT 6	DACG BIT 6	DACG BIT 6	DACG BIT 6	DACG BIT 6	DACG BIT 6
R13	TRACKING THRESHOLD CONTROL REGISTER (TTCR)	0	0	0	0	1	1	0	1		TTH2	TTH1	TTH0		TTHI2	TTHI1	TTHI0
R14	CONTROL A REGISTER (CAR)	0	0	0	0	1	1	1	0				TBGByp 0 = Enable 1 = Disable	TBG KD 0 = 1 • KD 1 = 3 • KD	PMP DN 1 = On 0 = Off	PMP UP 1 = On 0 = Off	Phase Dt 1 = Enable 0 = Disable
R15	HYSTERESIS DECAY CONTROL REGISTER (HDCR)	0	0	0	0	1	1	1	1		TTHEN 1 = Enable 0 = Disable	DS REF 0 = $\overline{DRD}$ 1 = RD	Threshold 0 = Fixed 1 = Level	DACL Bit 3	DACL Bit 2	DACL Bit 1	DACL Bit 0
R16	SERVO MODE CUTOFF REGISTER (SFCR)	0	0	0	1	0	0	0	0		DACF Bit 6	DACF Bit 5	DACF Bit 4	DACF Bit 3	DACF Bit 2	DACF Bit 1	DACF Bit 0
R17	SERVBO MODE BOOST REGISTER (SFCR)	0	0	0	1	0	0	0	1		DACS Bit 6	DACS Bit 5	DACS Bit 4	DACS Bit 3	DACS Bit 2	DACS Bit 1	DAS Bit 0
R18	SERVO PEAK DETECT REGISTER (PKCR)	0	0	0	1	0	0	1	0					PK Bit 3	PK Bit 2	PK Bit 1	PK Bit 0
R19	THRESHOLD CONTROL IN SERVO MODE (SHCR)	0	0	0	1	0	0	1	1	Data Qual 1 = Dual 0 = Hyst	DACT Bit 6	DACT Bit 5	DACT Bit 4	DACT Bit 3	DACT Bit 2	DACT Bit 1	DACT Bit 0

TABLE 12: Serial Port Register Default Values

REG#	REGISTER NAME	ADDRESS							DATA BIT MAP							
		A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
R1	POWER DOWN CONTROL REGISTER (PDCR)	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
R2	DATA MODE BOOST CONTROL REGISTER (PDCR)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R3	DATA RECOVERY CONTROL REGISTER (DRCR)	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0
R4	N COUNTER CONTROL REGISTER (NCCR)	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0
R5	DATA THRESHOLD CONTROL REGISTER (DTCR)	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0
R6	DATA MODE CUTOFF REGISTER (DMCR)	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0
R7	CONTROL B REGISTER (CBR)	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
R8	M COUNTER LSB REGISTER (MCLCR)	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0
R9	AGC GAIN CONTROL REGISTER (AGCR)	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
R10	WINDOW SHIFT CONTROL REGISTER (WSCR)	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1	1

TABLE 12: Serial Port Register Default Values (continued)

REG#	REGISTER NAME	ADDRESS								DATA BIT MAP							
		A6					A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
R11	M COUNTER MSB REGISTER (MCMCR)	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0
R12	GROUP DELAY EQ REGISTER (GDCR)	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
R13	TRACKING THRESHOLD CONTROL REGISTER (TTCR)	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1
R14	CONTROL A REGISTER (CAR)	0	0	0	0	1	1	1	0	0	0	1	0	0	0	1
R15	HYSTERESIS DECAY CONTROL REGISTER (HDCR)	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0
R16	SERVO MODE CUTOFF REGISTER (SFCR)	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
R17	SERVO MODE BOOST REGISTER (SFCR)	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
R18	SERVO PEAK DETECT REGISTER (PKCR)	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
R19	THRESHOLD CONTROL IN SERVO MODE (SHCR)	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data synchronizer PLL power supply pin
VPB	-	Time base generator PLL power supply pin
VPC	-	Pulse detector, serial port power supply pin
VPG	-	AGC, filter, servo demodulator, power supply pin
VCC2	-	Read data I/O power supply pin
VCC3	-	RDIO_ I/O power supply pin
VNA	-	Data synchronizer PLL ground pin
VNB	-	Time base generator PLL ground pin
VNC	-	Pulse detector, serial port ground pin
VNG	-	AGC, filter, servo demodulator
RTRN1	-	PPOL ground pin
RTRN2	-	Read data I/O ground pin
RTRN3	-	RRC ground pin
RTRN4	-	RDIO_ ground pin

INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{\text{PWRON}}$	I	POWER ENABLE: CMOS compatible power control input. A low level CMOS input enables power to circuitry according to the contents of the power enable bits. A high level CMOS input shuts down all circuitry.
HOLD	I	HOLD CONTROL: CMOS compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FIP,FIN	I	FILTER INPUT SIGNALS: The AGC output signals must be coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF has an internal pull down resistor. FREF should be driven by an AC coupled signal between 1.2 Vp-p and 2 Vp-p.
RG	I	READ GATE: CMOS compatible read gate input. A HIGH level CMOS input enables the read mode/address detect sequences. A low level selects the FREF input.
SG	I	SERVO GATE: CMOS compatible input that when pulled HIGH, enables the servo mode and corresponding internal settings as described in the section describing the servo demodulator.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
STROBE	I	BURST STROBE: CMOS compatible burst strobe input. A high level CMOS input will enable the servo peak detector to charge one of the burst capacitors. The falling edge of STROBE increments an internal counter that determines which burst capacitor will charge on the next STROBE pulse.
$\overline{\text{RESET}}$	I	RESET CONTROL INPUT: CMOS compatible reset input . A low level CMOS input wil discharge on the internal servo burst hold capacitors on channels A to D.

OUTPUT PINS

MTP1-4	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the MCTR MSB register. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYNCHRONIZED READ DATA: CMOS output pin. Read data output when RG is high. In HIZ mode when RG = 0.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
RDIO_	O	INVERTED READ DATA I/O: Bidirectional CMOS output/input pin. See TABLE 1. The minimum RDIO_ input pulse width is 10 ns. When RDIO_ is used as an input pin, the 1/2 symbol delay in the data synchronizer is made from the rising edge.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. Then RRC will switch to the DS VCO after the 19th data pulse. When RG goes low, RRC is synchronized back to the reference clock.
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).

ANALOG PINS

BYP	-	The AGC read mode integration capacitor CBYP, is connected between BYP and VPG.
SERVOBYP	-	The AGC read mode integration capacitor CSBYP, is connected between SERVOBYP and VPG.
WG_DCO	-	WG Pin when the Bit D6 of Serial Port Register R7 (CAR) is set LOW. WG signal terminates the LOW-Z mode with 1 ms delay and followed by a 1 ms fast decay mode operation. When the Bit D6 of Serial Port Register R7 (CAR) is set HIGH, It serves as DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the Control B register (see TABLE 10).

OUTPUT PINS

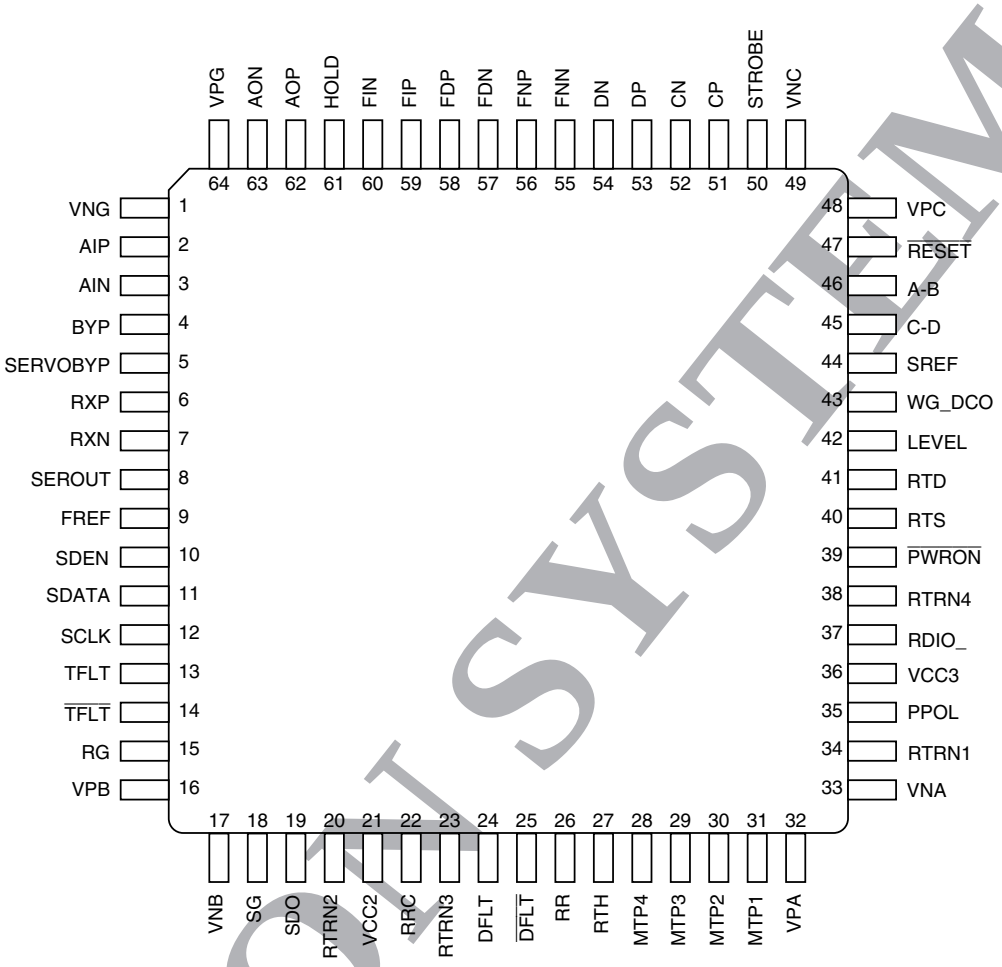
NAME	TYPE	DESCRIPTION
TFLT, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filters.
DFLT, $\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data synchronizer loop filters.
LEVEL	O	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VCC to set the hysteresis threshold time constant in conjunction with the level decay current DAC (R15, HDCR). The tracking threshold circuit also affects the discharge current on the LEVEL pin when enabled.
RTH	-	REFERENCE RESISTOR INPUT: An external resistor connected form this pin to VNA establishes the reference for the tracking threshold discharge current
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data synchronizer and time base generator.
SEROUT	O	Buffered output of the full wave rectifier referenced to VRC voltage which is available in RTD pin in non-servo modes and RTS in servo mode.
RXP, RXN	-	REFERENCE RESISTOR PINS: An external 9.09 kΩ, 1% resistor is connected between these pins to establish a precise reference current for the filter.
RTD	-	DATA TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant in data mode.
RTS	-	SERVO TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant in servo mode.
(A-B) (C-D)	O	SERVO OUTPUT: A,B,C and D bursts are captured and (A-B) and (C-D) are provided at these pins. They are referenced to an internally generated 2.5 V baseline, SREF.
SREF	O	SERVO REFERENCE: An external voltage output represents zero-signal baseline for (A-B) and (C-D) output signals.
PPOL	O	PULSE POLARITY: This is a CMOS compatible output and ouputs pulses which are coincident with the positive peak of the DP/DN signal.

SERIAL PORT PINS

SDEN	I	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDATA	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Abridged Version

SSI 34P3402A

8 to 53 Mbit/s Read Channel w/Adaptive Threshold Qualifier

September 1998

DESCRIPTION

The SSI 34P3402A device is a high performance BiCMOS single chip read channel IC that contains all the functions necessary to implement an adaptive threshold read channel. Functional blocks include a pulse detector with adaptive threshold qualifier, programmable filter, and data synchronizer. Raw data rates from 8 to 53 Mbit/s can be programmed by digital commands.

The SSI 34P3402A allows complete flexibility in read channel configuration. All critical parameters can be programmed by a microprocessor via a bi-directional serial port and a bank of internal registers.

The SSI 34P3402A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

- **8 to 53 Mbit/s raw data rate**
- **Bi-directional serial port for access to internal registers**
- **Low power operation (<550 mW typical @ RRC = 53 MHz and 5 V)**
- **Programmable power management (sleep mode <1 mW)**
- **Power supply range (4.5 to 5.5 V)**
- **Small footprint 48-Pin TQFP package**

PULSE DETECTOR

- **Temperature compensated, exponential control AGC**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low drift AGC hold circuitry**
- **Programmable AGC fixed gain mode**
- **Adaptive threshold qualifier for data extraction**
- **Traditional window qualifier for timing extraction**
- **Programmable pulse qualification threshold level**
- **CMOS RDIO signal output for servo timing support**
- **Internal LOW-Z and fast decay timing for rapid transient recovery and AGC acquisition**
- **Fast decay mode is self-timed for optimal AGC recovery**
- **0.5 ns maximum pulse pairing with sine wave input**
- **Independent qualification thresholds for data and timing extraction**

PROGRAMMABLE FILTER

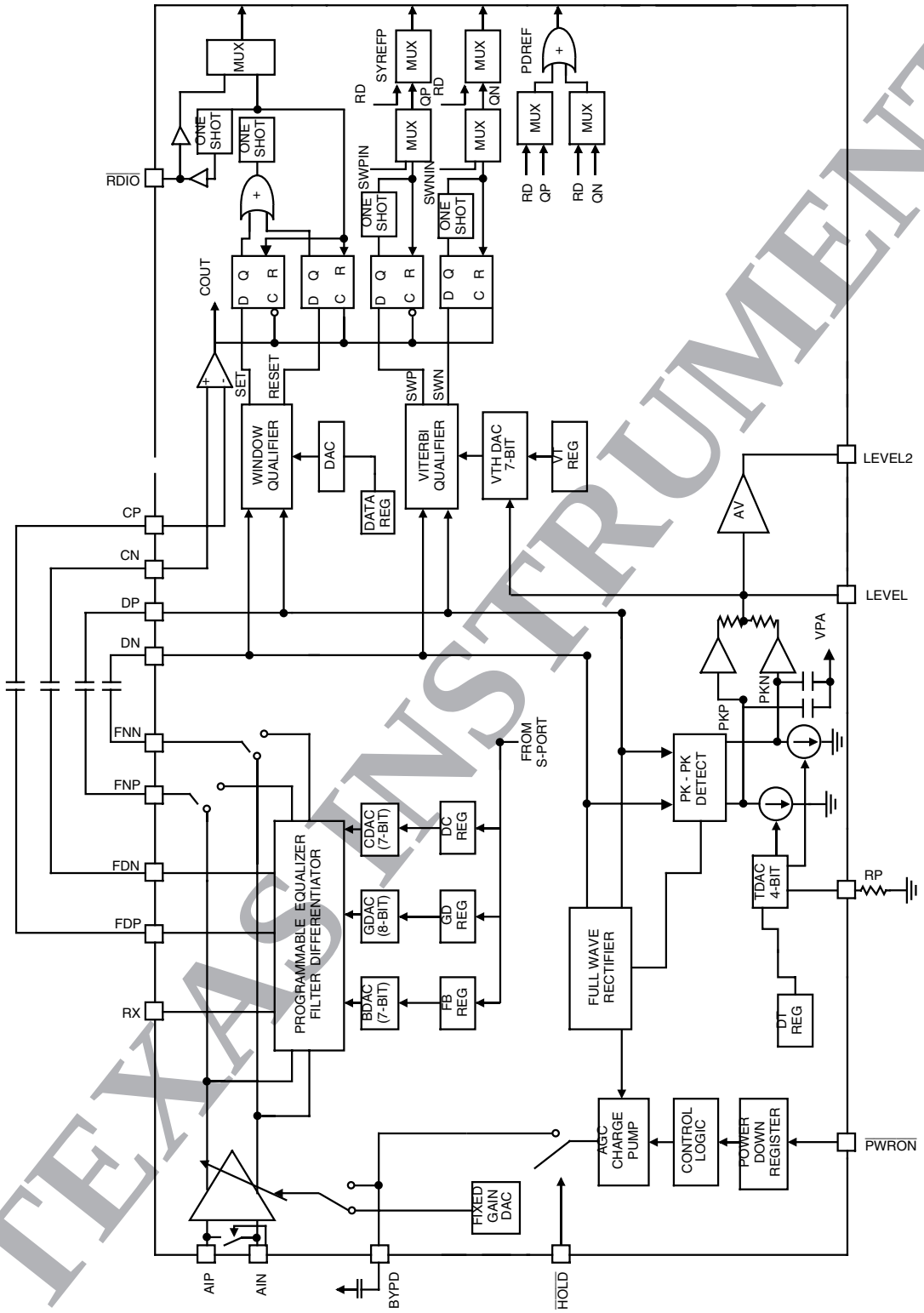
- **Programmable cutoff frequency of 2 to 16 MHz**
- **Programmable boost of 0 to 13 dB**
- **Programmable group delay equalization (up to 38% change in group delay)**
- **Matched normal and differentiated outputs**
- **±10% Fc accuracy from 10 to 16 MHz**
- **Less than 1% total harmonic distortion**

DATA SYNCHRONIZER

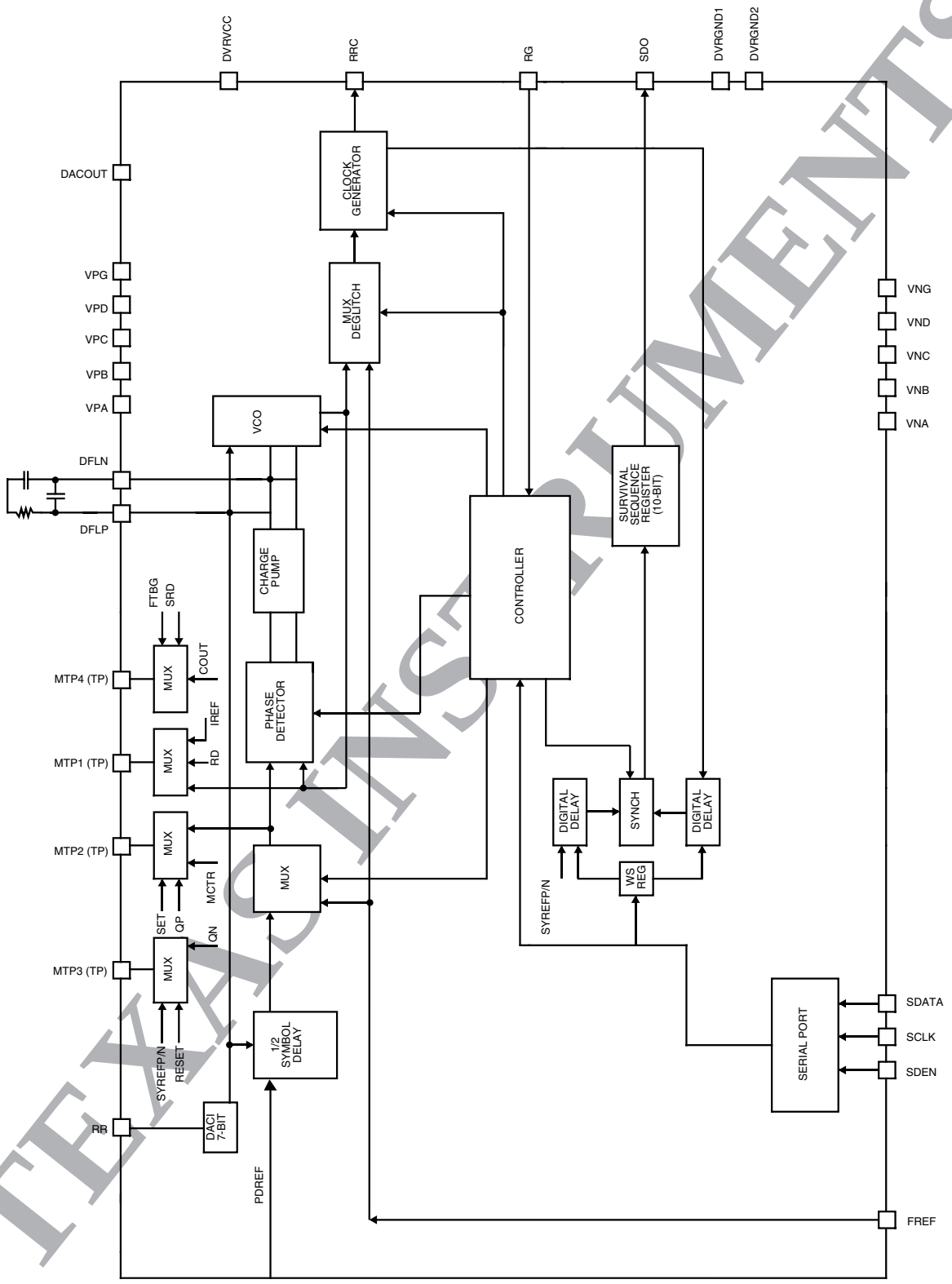
- **Fully integrated data synchronizer**
  - **No external delay lines or active components required**
  - **No external active PLL components required**
- **Selectable PLL input from adaptive threshold qualifier or traditional window qualifier**
- **Selectable data synchronizer input from adaptive threshold qualifier or traditional window qualifier**
- **Fast PLL acquisition phase lock loop**
  - **Zero phase restart technique**
  - **Programmable phase detector gain gear shift**
- **Programmable decode window symmetry**
  - **Window shift control ±15% of decode window**
  - **Includes delayed read data and VCO reference monitor points**

SSI 34P3402A
8 to 53 Mbit/s Read Channel w/Adaptive Threshold Qualifier

BLOCK DIAGRAM A



BLOCK DIAGRAM B



Abridged Version

SSI 34R3430R

+5 V, 2, 4-Channel, 3-Terminal Read/Write Device

July 1996

DESCRIPTION

The SSI 34R3430R is a BiCMOS monolithic integrated circuit designed for use with center-tapped ferrite or MIG recording heads. It provides a low noise read path with selectable gains of 85 and 250 V/V, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. A power down mode (idle) is provided to reduce power consumption to 3 mW nominal.

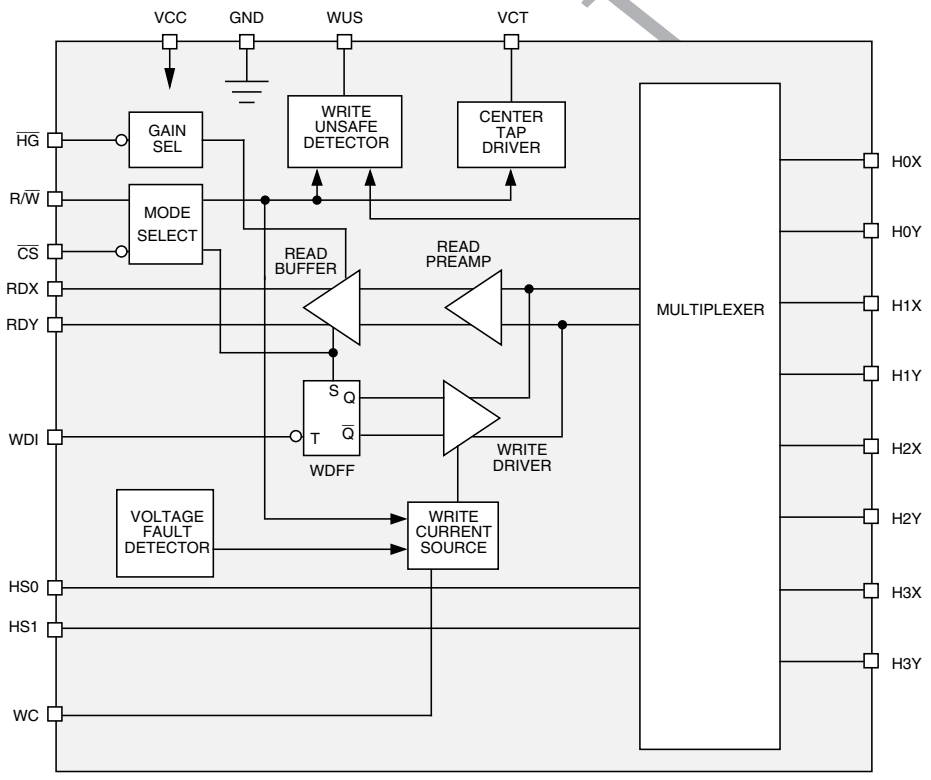
Internal 750 Ω damping resistors are provided. It requires only a +5 V power supply and is available in a surface mount package.

The SSI 34R3430R replaces the 32R1203R.

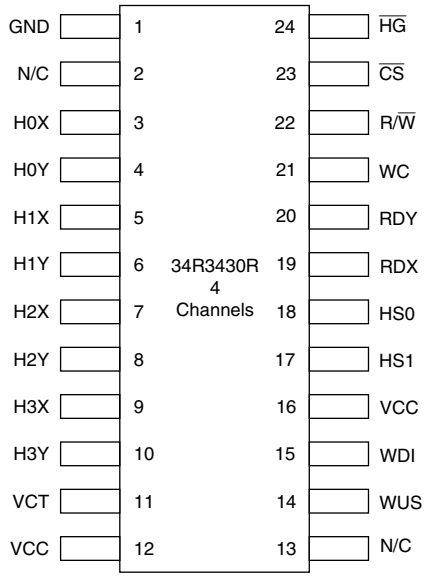
FEATURES

- **Pin selectable gain, 250 V/V and 85 V/V**
- **+5 V only power supply**
- **Low power**
  - **125 mW nom read mode**
  - **3 mW nom idle mode**
- **High Performance**
  - **Input noise = 1.2 nV/√Hz max**
  - **Input capacitance = 17 pF max**
  - **Write current range = 10 - 50 mA**
  - **Head voltage swing = 6 Vpk**
- **Designed for center-tapped ferrite or MIG heads**
- **Power supply fault protection**
- **Includes write unsafe detection**
- **Enhanced write to read recovery**

BLOCK DIAGRAM



PIN DIAGRAM



24-Lead VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the write data input line (WDI). A preceding read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = write current constant

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high level will be present at the write unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in read or idle mode

The write unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

A safe condition, WUS low , requires alternating voltage spikes on both HnX and HnY that exceed VCT + 1.5 V at a rate equal to or higher than the minimum rate of WDI for safe condition.

In addition, the power supply voltage level is monitored by a circuit that inhibits the write current if VCC is too low to permit valid data recording.

READ MODE

In read mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise gain selectable differential amplifier. The read amplifier input terminals are determined by the head select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs. Taking $\overline{HG}$ low selects high gain (250 V/V). Taking $\overline{HG}$ high or open selects low gain (85 V/V).

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table 1 and Table 2.

TABLE 1: Head Select Table

Head Selected	HS1	HS0
0	0	0
1	0	1
2	1	0
3	1	1

TABLE 2: Mode Select Table

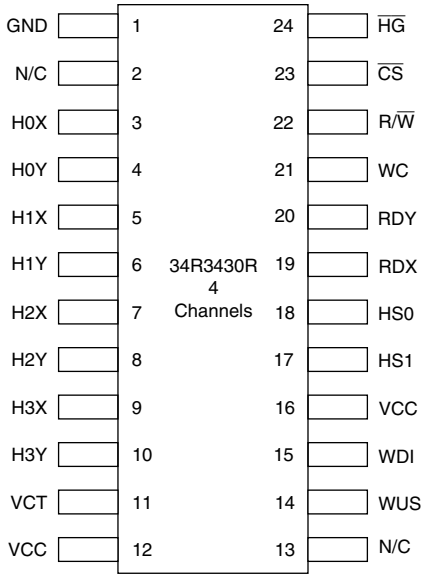
Mode Select		Selected Mode	Indicating & Fault Outputs
$\overline{CS}$	R/$\overline{W}$		WUS
1	X	Idle	high
0	1	Read	high
0	0	Write	active

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1	I*	HEAD SELECT: Logical combinations select one of four heads (see Table 1)
$\overline{CS}$	I	CHIP SELECT: A low level enables device. Has internal pull-up resistor.
R/$\overline{W}$	I*	READ/WRITE: A high level selects read mode. Has internal pull-up resistor.
WUS	O*	WRITE UNSAFE: A high level indicates an unsafe writing condition.
WDI	I*	WRITE DATA IN: Negative transition toggles direction of head current.
H0X-H3X H0Y-H3Y	I/O	X, Y head connections
RDX, RDY	O*	X, Y READ DATA: Differential read signal output
WC	-	WRITE CURRENT: Used to set the magnitude of the write current
VCT	-	VOLTAGE CENTER TAP: Voltage source for head center tap
VCC	-	+5 V
GND	-	Ground
$\overline{HG}$	I*	GAIN SELECT: $\overline{HG}$ low selects 250 V/V. $\overline{HG}$ high or open selects 85 V/V.

* When more than one R/W device is used, these signals can be wire OR'ed with unselected R/W devices.

PACKAGE PIN DESIGNATIONS (Top View)



24-Lead VSOP

THERMAL CHARACTERISTICS: tja

24-Lead VSOP	110° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

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SSI 34R3433R
3.3 V/5 V 2-Channel Read/Write Device

September 1998

DESCRIPTION

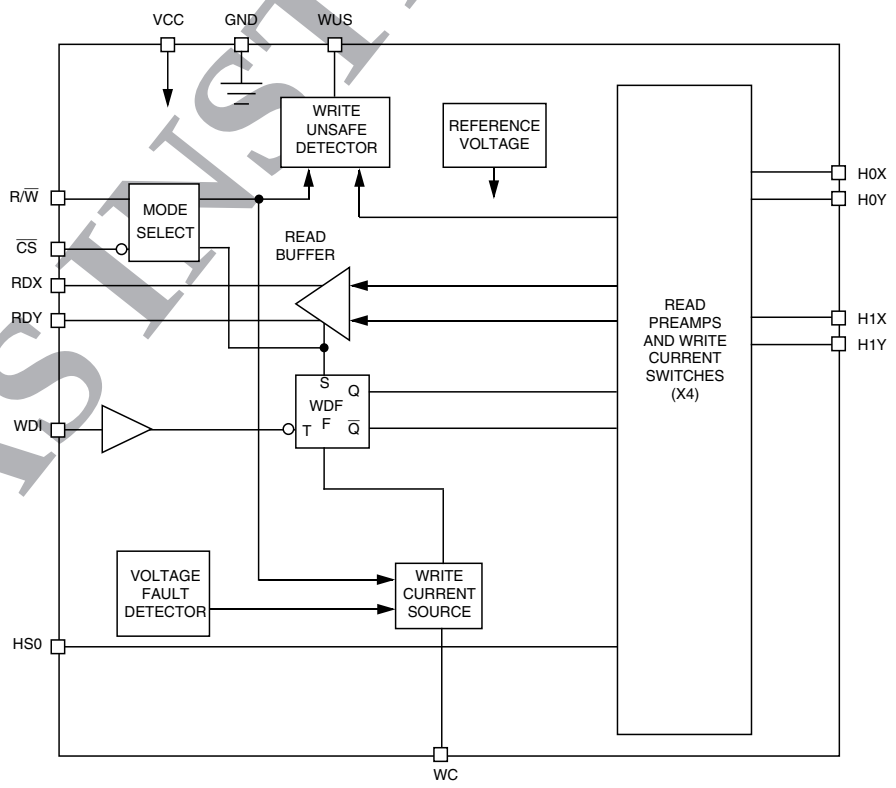
The SSI 34R3433R is a BiCMOS monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to four channels. Internal 350Ω damping resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance during write mode.

The SSI 34R3433R requires a single 3 to 5.5 V power supply.

FEATURES

- **+3 V - 5.5 V voltage supply**
- **Low power**
  - **PD = 73 mW read mode (Nom) (@3.3 V supply)**
  - **PD = 75 μW Idle (Max @ Vcc = 3.3 V)**
- **High Performance:**
  - **Read mode gain = 300 V/V**
  - **Input noise = 0.5 nV/√Hz (Nom)**
  - **Input capacitance = 9 pF (Nom)**
  - **Write current range = 2-30 mA**
- **Power supply fault protection**

BLOCK DIAGRAM



SSI 34R3433R
3.3 V/5 V 2-Channel Read/Write Device

FUNCTIONAL DESCRIPTION

The SSI 34R3433R has the ability to address up to 2 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$, $\overline{CS}$ and DMP have internal pull-up resistors. The TTL input HSO has an internal pull down resistor.

TABLE 1: Mode Select

CS	R/W	WUS	Mode
0	0	1	Write
0	1	X	Read
1	0	X	Idle
1	1	X	Idle
0	0	0	Servo Write

TABLE 2: Head Select

HS0	Head
0	0
1	1

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the device as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read to write transition or idle to write transition initializes the write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \bullet \frac{Vwc}{Rwc} = K \diagup Rwc$$

where Aw is the write current gain.

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 350 Ω damping resistor is switched in across the Hx, Hy ports.

SERVO WRITE MODE

This mode allows for writing to multiple channels at once, which is useful during servo formatting. When this mode is activated the write driver will drive all channels simultaneously.

The servo write mode can be enabled by using the WUS bi-directional pin depending on the device option (table 1). Both the $\overline{CS}$ and R/$\overline{W}$ inputs have to be low to activate servo bank write. When using the WUS pin to enable servo write, the pin voltage is driven to 1.5 V (nom) above VCC. The WUS pin voltage should not exceed VCC + 2 V or + 7 V, whichever is greater. The servo enable delay is about 1 µs typical.

VOLTAGE FAULT

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup in read or write mode.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in read mode
- Device not selected
- Open head
- Head short to ground
- No write current

WUS is valid in the write current/head characteristic region defined by 5 < Ih • Lh < 50 mA • µH, and 1 < Rh < 1.25/Ih. After the fault condition is removed, one negative transition on WDI is required to clear WUS.

READ MODE

The read mode configures the chip as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in idle or write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from write to read mode. Note also that the write current source is deactivated for both the read and idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum at $\overline{CS}$, input is greater than (Vcc - 0.3 V).

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0	I	Head Select: selects heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write: a high selects read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI †	I	Write Data Input: On TTL versions, a negative transition on WDI changes the direction of the current in the recording head.
H0X - H1X; H0Y - H1Y	I/O	X, Y Head Connections
RDX, RDY†	O	X, Y Read Data: differential read data output
WC		Write Current: used to set the magnitude of the write current
VCC	I	Power Supply
GND	I	Ground
WUS	I	Write Unsafe: Under normal operation, a high level output on this pin indicates a write unsafe condition. When this pin is driven externally above VCC and CS and R/W are both low, servo write mode is activated.

† When more that one R/W device is used, signals can be wire OR'ed

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC	-0.3 to +7 VDC
Write Current	Iw	30 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
WUS Pin Voltage	Vwus	+7 VDC
Output Current: RDX, RDY	I0	-10 mA
	WUS	+8 mA
Storage Temperature	Tstg	-55 to +150°

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage		3.3 ±10%, 5 ±10% VDC
Recommended Head Load Range	Lh	0.3 - 5 µH
WUS Operating Range, Iw • Lh		5 - 50 mA • µH
Head Differential Load Capacitance		15 pF max
Ambient Operating Temperature*	Ta	0 - 70°C

* Derating is required when in servo write mode.

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	Vcc = 3.3 V ±10% read		22	30	mA
	Vcc = 3.3 V ±10% write		5+1.2 • Iw	9+1.4 • Iw	mA
	Vcc = 3.3 V ±10% servo		6+4.5 • Iw	11+4.7 • Iw	mA
	Vcc = 3.3 V ±10% idle, CS = Vcc		3	20	µA
	Vcc = 3.3 V ±10% idle, CS = 2.7 V		30	200	µA
Power Dissipation	Vcc = 3.3 V ±10% read		73	110	mW
	Vcc = 3.3 V ±10% write		17+4 • Iw	33+5 • Iw	mW
	Vcc = 3.3 V ±10% servo		20+15 • Iw	40+17 • Iw	mW
	Vcc = 3.3 V ±10% idle, CS = Vcc		9	75	µW
	Vcc = 3.3 V ±10% idle, CS = 2.7 V		100	730	µW

DC CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	Vcc = 5 V ±10% read		23	32	mA
	Vcc = 5 V ±10% write		6+1.2 • Iw	10+1.3 • Iw	mA
	Vcc = 5 V ±10% servo		7+4.4 • Iw	12+4.7 • Iw	mA
	Vcc = 5 V ±10% idle, $\overline{CS}$ = Vcc		5	30	µA
	Vcc = 5 V ±10% idle, $\overline{CS}$ = 2.7 V		250	450	µA
Power Dissipation	Vcc = 5 V ±10% read		115	180	mW
	Vcc = 5 V ±10% write		30+6 • Iw	55+7 • Iw	mW
	Vcc = 5 V ±10% servo		35+22 • Iw	66+26 • Iw	mW
	Vcc = 5 V ±10% idle, $\overline{CS}$ = Vcc		0.03	0.17	mW
	Vcc = 5 V ±10% idle, CS = 2.7 V		1.25	2.5	mW

DIGITAL INPUTS

Input Low voltage	VIL	$\overline{CS}$, R/$\overline{W}$, WDI, HSO		0.8	VDC
Input High Voltage	VIH	$\overline{CS}$, R/$\overline{W}$, WDI, HSO	2		VDC
Input Low Current		VIL = 0.4 Vcc = 3.6 V $\overline{CS}$, R/$\overline{W}$, WDI, Vcc = 5.5 V	-0.4 -0.4	-.09 -0.13	mA mA
Input High Current		VIH = 2.7 V $\overline{CS}$, R/$\overline{W}$, WDI		0 20	mA
WUS Output Low Voltage	VOL	Iol = 2 mA max		0.35 0.5	VDC
Input Low Current		HSO VIL = 0.4 V		10 40	µA
Input High Current		HSO VIH = 2.7 V		100 400	µA
Input Low Voltage		WD	Vcc -1	Vcc -0.4	V
Input High Voltage		WD	Vcc -2	Vcc -0.8	V
Δ VIN		|WD - $\overline{WD}$|	0.4 0.8		V
Input Low Current		WD Vcc = 5 V VIH = Vcc - 0.8 V		100 200	µA
Input High Current		WD Vcc = 5 V VIL = Vcc - 1.6 V		75 150	µA

ELECTRICAL SPECIFICATIONS (continued)

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Fault Voltage	Iw < 0.2 mA		2.5	2.75	VDC
Write Current Gain Aw	Iw = 2-5 mAVcc = 3.3 V±10%	20	24	29	mA/mA
	Iw = 5-30 mAVcc = 3.3 V±10%	19	22	25	mA/mA
	Iw = 2-5 mAVcc = 5.0 V±10%	21	25	30	mA/mA
	Iw = 5-30 mAVcc = 5.0 V±10%	20	23	26	mA/mA
Write Current Error	Rwc = 2 kΩ, head to head @ write mode*	-5		+5	%
	Rwc = 2 kΩ, head to head @ servo mode*	-5		+5	%
	Rwc = 2 kΩ, write to servo	-7		+7	%
Write Current Voltage VWC		1.2	1.3	1.4	V
Differential Head Voltage Swing	open head, WUS = 1	4	4.8		Vp-p
	open head, Vcc = 5 V, WUS = 0	4	4.8		Vp-p
	open head, Vcc = 3.3 V, WUS = 0	3.4	4.8		Vp-p
Unselected Head Current	AC			1	mA (pk)
	DC			0.1	mA
Head Differential Load Resistance Rd	R version	300	400	500	Ω
	non-R version	2400	3000	3600	Ω
WDI Pulse Width	Vil ≤ 0.8 V, Vih ≥ 2 V PWH	5			ns
	$t_f = t_r$ = 1 ns PWL	10			ns
Write Current Range Iw		2		30	mA

* Error from average of the four heads.

SERVO WRITE CHARACTERISTICS

WUS Voltage	servo bank write enabled	VCC + 1.5		VCC + 2	V
WUS Sink Current	servo bank write ennabled Vwus = VCC +1.5 V		70	200	µA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVp-p @1 MHz	240	300	360	V/V
Voltage BW	-1 dB	|Zs| < 5 Ω, Vin = 1 mVp-p	20	40		MHz
	-3 dB		40	80		MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0		0.5	0.75	nV/√Hz
Differential Input Capacitance		Vin = 1 mVp-p, f = 5 MHz		9	14	pF
Differential Input Resistance		Vin = 1 mVp-p, f = 5 MHz	500	750	1800	Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	5		mVp-p
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVp-p @ 5 MHz	45	60		dB
Power Supply RejectionRatio		100 mVp-p @ 5 MHz on VCC	40	70		dB
Channel Separation		Unselected channels driven with Vin = 0 VDC + 100 mVp-p	45	60		dB
Output Offset Voltage		Head shorted	-250		+250	mV
		Head loaded 200 Ω	-400		+400	mV
Single Ended Output Resistance		f = 5 MHz		60	100	Ω
Output Current		AC coupled load, RDX to RDY	1	2		mA
RDX, RDY Common Mode Output Voltage			Vcc-1	Vcc-1.35	Vcc-1.7	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. Rwc = 2 kΩ, Lh = 1.0 µH, Rh = 30 Ω *f* (Data) = 5 MHz.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current; WUS valid		0.3	1	µs
	Write to Read	R/$\overline{W}$ to 90% of 100 mV Read signal envelope		0.4	1	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of 100 mV 10 MHz Read signal envelope		0.6	2	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1	µs
WUS*	Safe to Unsafe TD1	Write mode, loss of WDI transitions; Defines max WDI period for WUS operation	0.6	2	3.6	µs
	Unsafe to Safe TD2	Fault cleared: from first negative WDI transition		0.2	1	µs
WDI	Frequency Range	Valid WUS	1.67		25	MHz
Head Current	WDI to Ix - Iy TD3	Lh = 0, Rh = 0 from 50% points		25	40	ns
	Asymmetry	WDI has 1 ns rise/fall time			1.5	ns
	Rise/fall Time	10% to 90% points Rwc = 2 kΩ, Rh = 0, Lh = 0		2	9	ns
		Rwc = 2 kΩ, Rh = 30 Ω, Lh = 1µH		14	18	ns

* 5 < Iw • Lh < 50 mA • µH, 1 < Rh ≤ 1.25/Iw

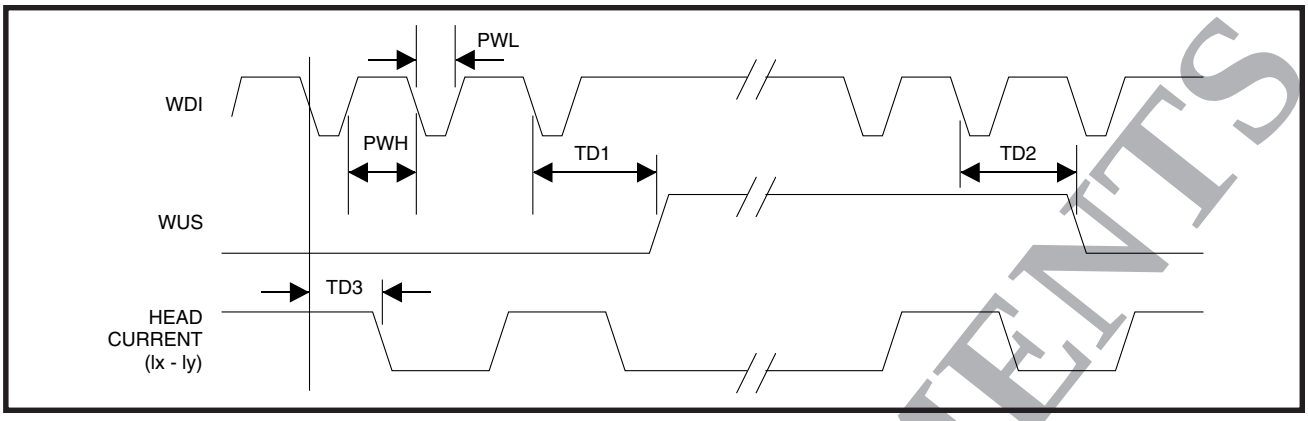
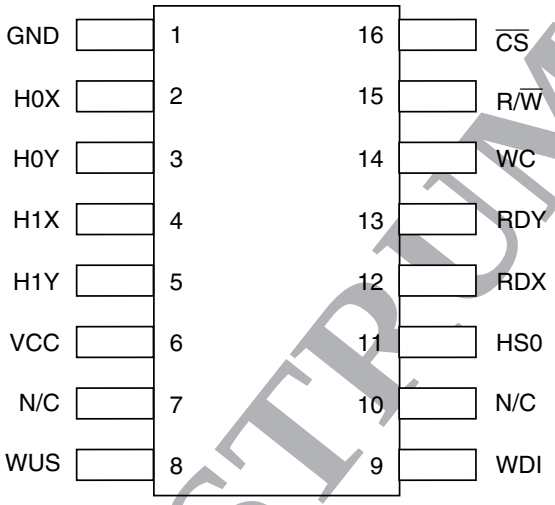


FIGURE 1: Write Mode Timing Diagram

PACKAGE PIN DESIGNATION
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



16-Lead VTSOP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 34R3433R 16-VTSOP	34R3433RX-2CVT	34R3433RX

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000 FAX (714) 573-6914

Abridged Version

SSI 34R3435

5/12 V 1-Channel BiCMOS Thin Film & MR Tape Drive R/W Device

May 1997

DESCRIPTION

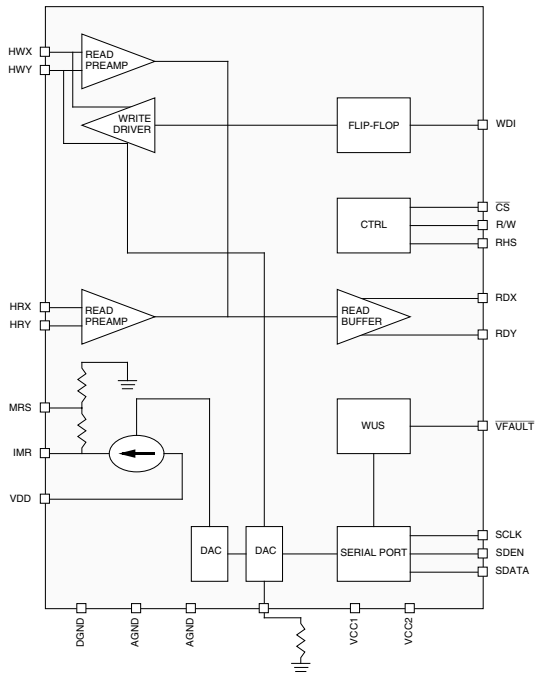
The SSI 34R3435 is a BiCMOS monolithic integrated circuit designed for use with one 2-terminal thin film recording head and one MR sensing element. It provides a low noise read amplifier and write driver for the thin film head, a low noise read amplifier and bias current for the MR element, and data protection circuitry. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write-to-read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The SSI 34R3435 provides the user with a serial port controllable write-current and MR bias adjustment feature. Fault conditions are indicated through the serial port and an external pin.

The SSI 34R3435 requires both a +5 V and +12 V power supply and is available in a 24-Lead VSOP package.

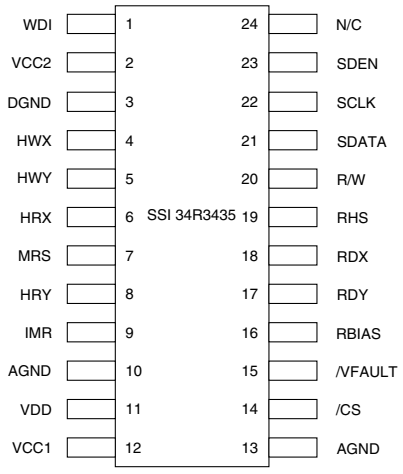
FEATURES

- **+5 V ±10% supply and +12 V ±10% supply**
- **Low power 3 mA idle mode current**
- **High performance:**
  - **MR read mode gain = 100 V/V**
  - **TFH read mode gain = 300 V/V**
  - **MR input current noise = 3.2 pA/√Hz max**
  - **MR input capacitance = 5 pF nom**
  - **Write current range = 5.4 - 55 mA**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**
- **Write-mode head swing 8 Vp-p diff (typical)**
- **24-Lead VSOP package**
- **Serial port controllable write current and read bias**
- **Serial port controllable flip-flop**
- **Head open or shorted detection**

BLOCK DIAGRAM



PIN DIAGRAM



24-Lead VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 34R3435 has the ability to address one thin film head and provide write drive or read amplification, as well as providing bias current and read amplification for one MR element. Mode control is described in Table 1. The TTL inputs R/W and CS have internal pull-up to prevent an accidental write condition. Internal clamp circuitry will prevent DC erase from a head short to ground in any mode.

TABLE 1: Mode Select

MODE		/CS	R/W	RHS	SERIAL A5-B1	SERIAL A5-B0
MR Read		0	1	1	X	0
Thin Film Read	Case 1	0	1	0	X	X
	Case 2	0	1	1	X	1
Write-Reader Off	Case 1	0	0	0	X	X
	Case 2	0	0	1	0	X
	Case 3	0	0	1	1	1
Simultaneous Write/MR Read		0	0	1	1	0
Idle		1	X	X	X	X

PIN DESCRIPTION

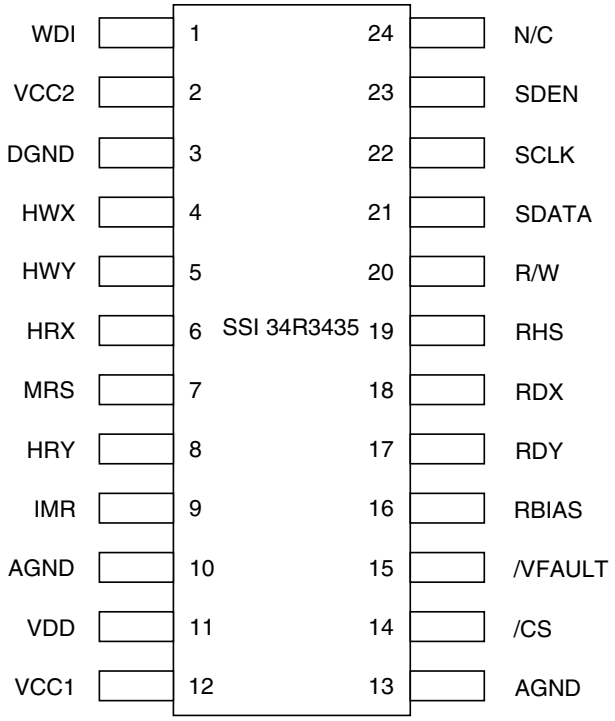
NAME	TYPE	DESCRIPTION
/CS	I	CHIP SELECT: A high inhibits the chip
R/W	I	READ/WRITE: A high selects read mode, low write mode
RHS	I	READ HEAD SELECT: A high selects the MR head for read. Low selects the thin film head.
/VFAULT	O	VOLTAGE FAULT: A low indicates V_{CC} fault
WDI	I	WRITE DATA IN: Changes the direction of the write current (Iw) in the recording head.
HWX, HWY	I/O	X, Y thin film head connections, used for both read and write
HRX, HRY	I	X, Y MR head connections
MRS	O	MR shield bias
IMR	O	MR current bias
RDX, RDY	O	X, Y READ DATA: Differential read data output
RBIAS	DC Bias	DAC BIAS RESISTOR: 15 kΩ
SDEN	I	SERIAL PORT ENABLE: Sets start of serial transfer
SCLK	I	SERIAL PORT CLOCK: Clocks data into serial port
SDATA	I/O	SERIAL PORT DATA: Data stream to/from serial port
VCC1	Power	Analog +5 V ±10% supply
VCC2	Power	Digital +5 V ±10% supply
VDD	Power	+12 V ±10% supply
DGND	GND	DIGITAL GROUND
AGND	GND	ANALOG GROUND

SERIAL PORT ADDRESSES
Bit 0 is LSB

ADDRESS	TYPE	DESCRIPTION	INITIALIZE
0000	I/O	MR current 4 LSB — $B_3B_2B_1B_0$	0000
0001	I/O	MR current MSB — B_VXXB_4 (B_V = vendor ID)	1000
0010	I/O	Write current 4 LSB — $B_3B_2B_1B_0$	0000
0011	I/O	Write current 2 MSB — XXB_5B_4	0000
0100	O	WUS — B_1 = VDD fault, B_0 = open/shorted head	0000
0101	I/O	Read mode — XXB_1B_0; Refer to Table 1	0000
0110	I/O	Flip-Flop disable B_0 = disable (0 = flip-flop, 1 = no flip-flop)	0000
0111	I/O	Damping resistor select - $XB_2B_1B_0$	0000
1111	I/O	Read-back register	XXXX

PACKAGE PIN DESIGNATIONS

(Top View)



24-Lead VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 34R3435 24-Lead VSOP	34R3435-CV	34R3435-CV

Silicon Systems reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

Abridged Version

SSI 34R3436
+5/+12 V 1-Channel TFH/MR Tape Drive Read/Write IC

February 1998

DESCRIPTION

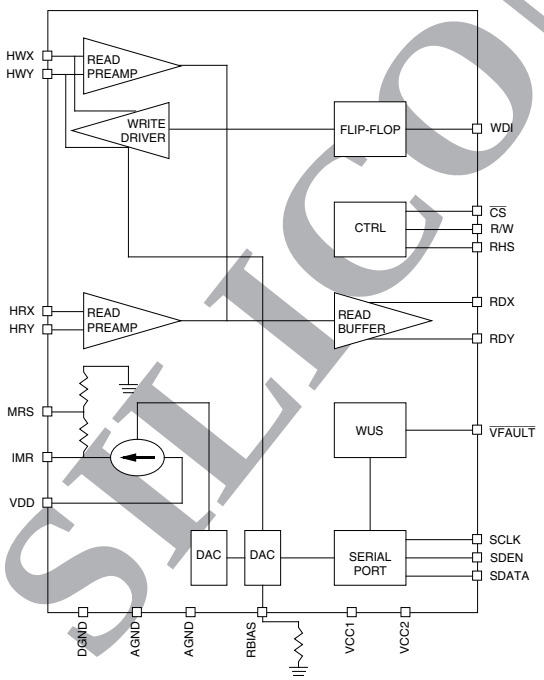
The SSi 34R3436 is a BiCMOS monolithic integrated circuit designed for use with one 2-terminal thin film recording head and one MR sensing element. It provides a low noise read amplifier and write driver for the thin film head, a low noise read amplifier and bias current for the MR element, and data protection circuitry. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write-to-read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The SSI34R3436 provides the user with a serial port controllable write-current and MR bias adjustment feature. Fault conditions are indicated through the serial port.

The SSI 34R3436 requires both a +5 V and +12 V power supply.

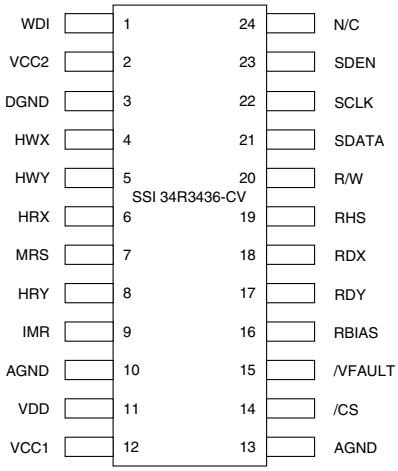
FEATURES

- **+5 V ±10% supply and +12 V ±10% supply**
- **Low power 3 mA ICC (idle mode)**
- **High Performance**
  - **MR read mode gain = 100 V/V**
  - **TFH read mode gain = 300 V/V**
  - **Input noise = 1.1 nV√Hz max**
  - **Input capacitance = 5 pF nom**
  - **Write current range = 5.4-55 mA**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**
- **Increased write-mode head swing 8 Vp-p diff (typical)**
- **24-Pin SOL, VSOP package**
- **Serial port controllable write current and read bias**
- **Serial port controllable flip-flop**
- **Head open or shorted detection**

BLOCK DIAGRAM



PIN DIAGRAM



24-Lead VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 34R3436 has the ability to address 1 thin film head and provide write drive or read amplification, as well as providing bias current and read amplification for 1 MR element. Mode control is described in Table 1. The TTL inputs R/$\overline{W}$ and CS have internal pull-up to prevent an accidental write condition. Internal clamp circuitry will prevent DC erase from a head short to ground in any mode.

TABLE 1: Mode Select

/CS	R/$\overline{W}$	RHS	SERIAL A5-B1	SERIAL A5-B0	MODE
0	1	1	X	0	MR Read
0	1	0	X	X	Thin Film Read (Case 1)
0	1	1	X	1	Thin Film Read (Case 2)
0	0	0	X	X	Write - Reader Off (Case 1)
0	0	1	0	X	Write - Reader Off (Case 2)
0	0	1	1	1	Write - Reader Off (Case 3)
0	0	1	1	0	Simultaneous Write/ MR Read
1	X	X	X	X	Idle

TABLE 2: R/$\overline{W}$ Pin Control

R/$\overline{W}$ PIN	SERIAL A6-B2	SERIAL A6-B3	R/$\overline{W}$ FOR TABLE 1
X	0	0	0
X	1	0	1
0	X	1	0
1	X	1	1

TABLE 3: RDX,Y Control

MODE	SERIAL A6-B1	READ OUTPUTS
MR Read	0	OFF (Hi-Z)
MR Read	1	ON
Thin Film Read	0	OFF (Hi-Z)
Thin Film Read	1	ON
Simultaneous Write/ MR Read	0	OFF (Hi-Z)
Simultaneous Write/ MR Read	1	ON
Write	X	OFF (Hi-Z)
Idle	X	OFF (Hi-Z)

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
/CS	I	Chip Select: a high inhibits the chip
R/$\overline{W}$	I	Read/Write: a high selects read mode, low write mode
RHS	I	Read Head Select: a high selects the MR head for read. Low selects the thin film head.
/VFAULT	O	Voltage Fault: a low indicates VCC fault
WDI	I	Write Data In: changes the direction of the write current (Iw) in the recording head
HWX, HWY	I/O	X, Y Thin Film Head Connections, used for both read and write
HRX, HRY	I	X, Y MR Head Connections
MRS	O	MR Shield Bias
IMR	O	MR Current Bias
RDX, RDY	O	X, Y Read Data: differential read data common emitter output
RBIAS	DC Bias	DAC Bias Resistor. 15 KΩ
SDEN	I	Serial Port Enable - Sets start of serial transfer
SCLK	I	Serial Port Clock - Clocks data into serial port
SDATA	I/O	Serial Port Data - Data stream to/from serial port
VCC1	Power	Analog +5 V ±10% Supply
VCC2	Power	Digital +5 V ±10% Supply
VDD	Power	+12 V ±10% Supply.
DGND	GND	Digital Ground
AGND	GND	Analog Ground

REGISTER DESCRIPTION

INITIALIZE VALUES

REG	MSB ADDRESS			LSB	TYPE	MSB DATA			LSB	REGISTER NAME
0	0	0	0	0	I/O	IMR3 0	IMR2 0	IMR 0	IMR0 0	MR Current LSB
1	0	0	0	1	I/O	VID 1	X 0	X 0	IMR4 0	Vendor ID/ MR Current MSB
2	0	0	1	0	I/O	IW3 0	IW2 0	IW1 0	IW0 0	Write Current LSB
3	0	0	1	1	I/O	X 0	X 0	IW5 0	IW4 0	Write Current MSB
4	0	1	0	0	I/O	X 0	X 0	VFLT 0	HUS 0	Write Unsafe
5	0	1	0	1	I/O	X 0	X 0	MSB1 0	MSB0 0	Mode Select
6	0	1	1	0	I/O	RWCTL 1	R/$\overline{W}$ 1	RDEN 1	FFD 0	Read Control/ FF Disable
7	0	1	1	1	I/O	X 0	RD2 0	RD1 0	D0 0	Damping Resistor Select
F	1	1	1	1	I/O	RB3	RB2	RB1	RB0	Readback Register

REGISTER 0 (MR CURRENT LSB)

BIT	NAME	DESCRIPTION
3:0	IMR3-IMR0	MR Current DAC: least significant 4 bits The magnitude of the MR bias current is given by: $I_{MR} = 2mA + \frac{M}{31} \bullet 18.6\ mA$ where M is the decimal value of bits IMR0-IMR4.

REGISTER 1 (VENDOR ID/MR CURRENT MSB)

3	VID	Vedor ID Bit = 1 (read only)
2:1	unused	
0	IMR4	MR Current DAC: most significant bit

REGISTER 2 (WRITE CURRENT LSB)

3:0	IW3-IW0	Write Current DAC: least significant 4 bits $I_W = 5.4\ mA + \frac{M}{63} \bullet 50.4\ mA$ where M is the decimal value of bits IW0 - IW5

REGISTER 3 (WRITE CURRENT MSB)

BIT	NAME	DESCRIPTION
3:2	unused	
1:0	IW5-IW4	Write Current DAC: most significant 2 bits

REGISTER 4 (WRITE UNSAFE) - READ ONLY

3:2	unused	
1	VFLT	High indicates VDD fault
0	HUS	High indicates open or shorted head

REGISTER 5 (MODE SELECT)

3:2	unused	
1:0	MSB1 - MSB0	Mode select (see table 1)

REGISTER 6 (READ CONTROL/FLIP-FLOP DISABLE)

3	RWCTL	Read/Write pin control High enables mode control from R/$\overline{W}$ pin Low enables mode control from R/$\overline{W}$ serial port bit. (see Table 2)
2	R/$\overline{W}$	Read/Write pin If RWCTL is low, setting this bit high enables read mode; setting this bit low enables write mode. (see Tables 1 and 2)
1	RDEN	Read output enable. High enables RDX/RDY pins. (see Table 3)
0	FFD	High disables flip-flop in write path

REGISTER 7 (DAMPING RESISTOR SELECT)

3	unused	
2:0	RD2-RD0	Selects write damping resistor (see Damping Resistors section in the Electrical Specifications)

REGISTER F (READBACK REGISTER)

3:0	RB0-RB3	Readback address. Write address to this register to initiate serial port readback

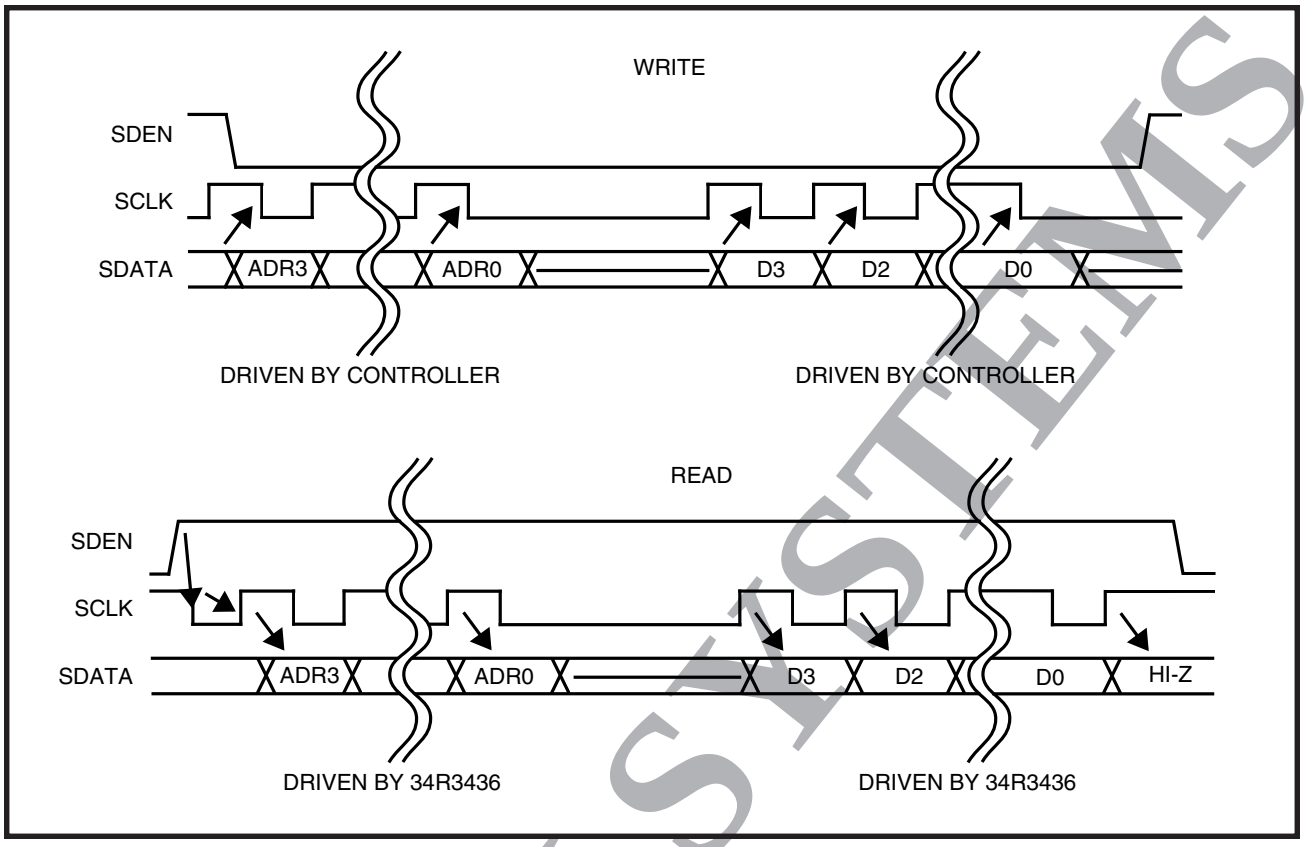
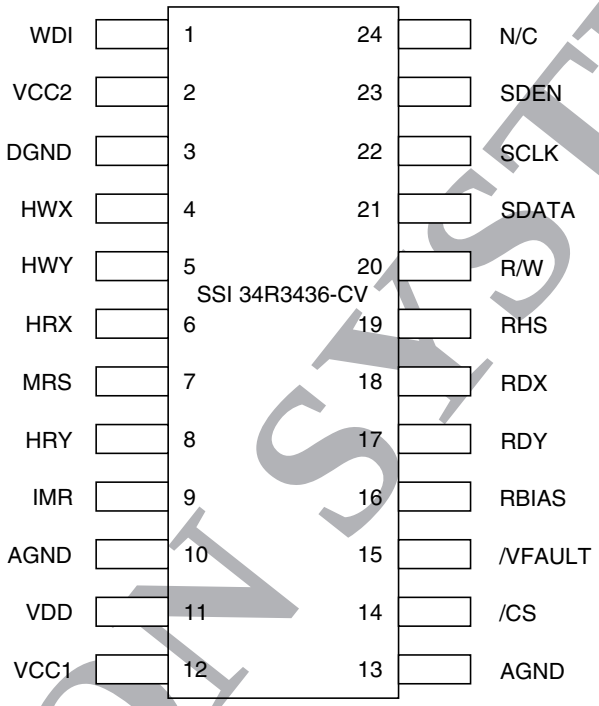


FIGURE 1: Typical Serial Port write and read sequences

PACKAGE PIN DESIGNATIONS

(Top View)



24-Lead VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

Abridged Version

SR3437B

5 V 2-Channel Write Coil Driver with Read Buffer

October 1999

DESCRIPTION

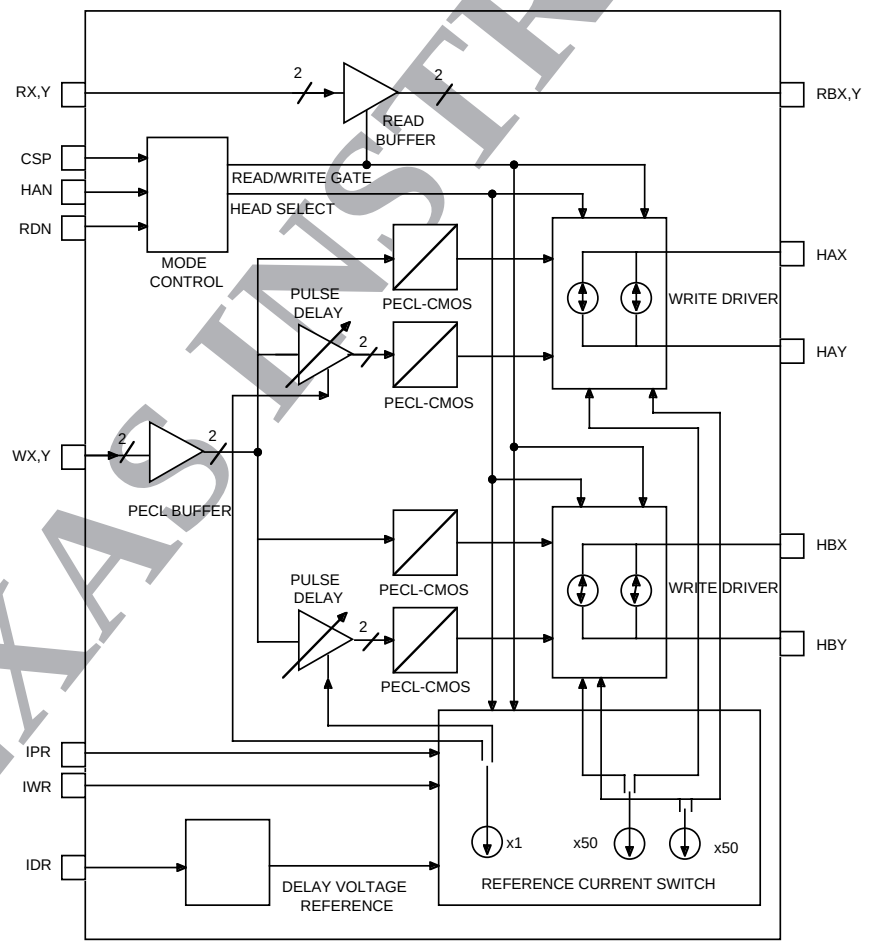
The SR3437B is a BiCMOS monolithic integrated circuit that includes a read buffer amplifer and a 2-channel, double pulse, write driver designed to drive a transformer coupled ferrite head. The read buffer amplifier is used to isolate the read channel transformer termination impedance from the flex circuit impedance and the read channel input circuitry. The write driver is an adaptation of a conventional H-bridge architecture, with additional circuitry that provides an extra current pulse to decrease head field rise time. The device requires +8 V and +5 V and comes in a 28-Pin VSOP package.

FEATURES

- **+5 V ±10%, +8 V ±10% suppliers**
- **28-Pin VSOP package**
- **2-channel multiplexed write drivers**
- **Read mode power = 165 mW**
- **Write mode power = 950 mW (nom)**
- **Sleep mode power = <3.5 mW (nom)**
- **Head voltage swing = 6.5 V_{PP} (min, open head)**
- **External damping resistor (175 Ω)**

(continued)

BLOCK DIAGRAM



FEATURES (continued)

- External DAC programmable write current range to 62.5 mA, current gain = 55
- External DAC programmable pulse current range to 62.5 mA, current gain = 55
- Programmable pulse current delay by external resistor; 2.0 V reference pin
- Write driver “trickle” current for fast read to write transitions = 200 ns (max)
- Read buffer gain = 1 (nom), -3 dB bandwidth = 300 MHz (min)
- Equivalent input noise 10 nV√Hz (nom)
- Supports requirements for DDS-4 tape standards

FUNCTIONAL DESCRIPTION

MODES

The device modes are controlled by three TTL pins: CSP (Chip Select Positive), RDN (Read Negative), and HAN (Head A Negative). These pins have an internal pull-down resistor and will be low when left open.

Table 1 shows the device modes.

SLEEP mode will shut down all the device circuitry to minimize power dissipation.

In READ mode, the buffer amplifier and RX,Y pin biasing circuitry are turned on. (Note: the read buffer is coupled to the read preamplifier through an external read channel transformer). A write pre-driver “trickle” current is activated to minimize read to write transitions.

In WRITE mode, the head current will toggle between the HX and HY side of the coil on each transition of the differential PECL input WX and WY. When WX is greater than WY, the write current I_W will flow from the HX to the HY pin. The buffer amplifier and RX,Y biasing circuitry is turned off.

WRITE CURRENT SETTING

The write current magnitude is set by an external DAC current sink connected to the IWR pin. The peak magnitude of the write current, I_W is:

$$I_W = [A_W \bullet I_{WR}] / [1 + (R_H / R_D)]$$

where A_W is 50 mA/mA, I_{WR} is the write DAC current reference, R_H is the head DC resistance, and R_D is the device damping resistance. The damping resistor is an external resistor.

PULSE CURRENT SETTING

The pulse current magnitude is set by an external DAC current sink connected to the IPR pin. The peak magnitude of the pulse current, I_P is:

$$I_P = [A_P \bullet I_{PR}] / [1 + (R_H / R_D)]$$

where A_P is 50 mA/mA, and I_{PR} is the pulse DAC current reference.

PULSE DELAY SETTING

The pulse current delay is set by an external resistor connected to the IDR pin. The delay is calculated by the following equation:

$$T_D \text{ (nom)} = K / (2.0 / R_{EXT})$$

where K = 1.26 µs/ µA, and R_{EXT} is the external resistor.

TABLE 1: Device Modes

CSP	RDN	HAN	MODE
HIGH	HIGH	LOW	Write to Head A
HIGH	HIGH	HIGH	Write to Head B
HIGH	LOW	X	Enable Read Buffer
LOW	X	X	Sleep

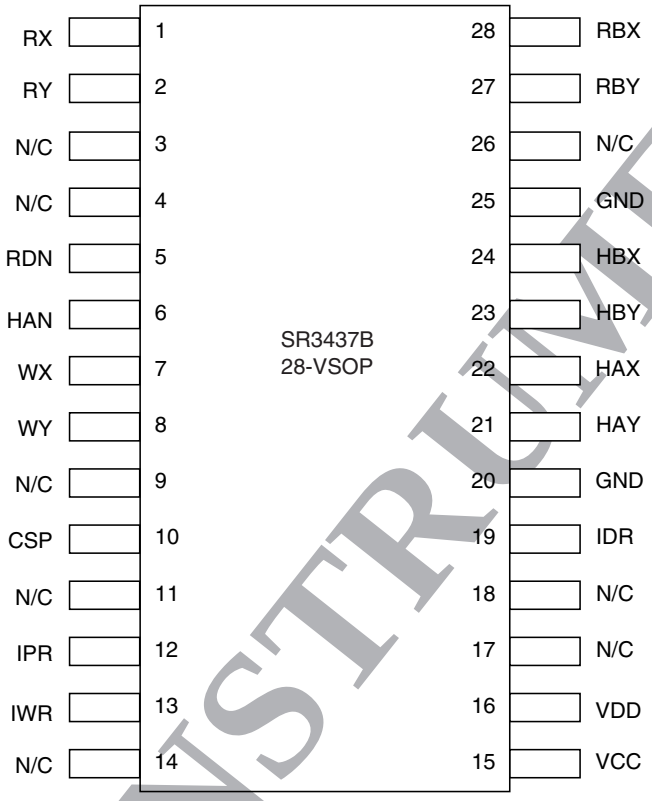
PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RX,Y	AI	Differential read signal from preamplifier
RDN	DI	Read Negative, TTL, internal pull-down resistor
HAN	DI	Head A Negative, TTL, internal pull-down resistor
WX,Y	DI	Write data input; PECL; WX > WY head current is sourced from HX to HY
N/C		No connection
CSP	DI	Chip Select Positive, TTL, internal pull-down resistor
IPR	AI	Pulse current reference (<1.25 mA); external current DAC sink
IWR	AI	Write current reference (<1.25 mA); external current DAC sink
VCC		+5 volts
VDD		+8 volts
IDR	AI	Delay current reference (<1.25 mA); 2.0 V output; external resistor
GND		Ground
HAX,HAY	AO	Head A coil output
HBX,HBY	AO	Head B coil output
GND		Ground
RBX,RBY	AO	Differential buffered read signal

AI = analog input, AO = analog output, DI = digital input

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SR3437B	28-Pin VSOP	SR3437BAA2DB	SR3437BAA2DB

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SR3440BC

PREAMP & ANALOG FRONT END/WRITE DRIVER FOR 4-CHANNEL MAGNETIC TAPE DRIVES

Preproduction

June, 2000

DESCRIPTION

The TI SR3440B integrates all the analog functions needed for a 4-channel magnetic tape drive. Included in one package are low-noise differential preamplifiers, automatic gain control (AGC), high-pass and low-pass filters, power supply and write-protection monitors, and quad H-bridge write drivers. Each major functional block may be programmed through a serial port interface and on-chip CMOS data registers.

Servo head selection, head bias current, gain, filter characteristics, and write current parameters can be controlled via the 53 programmable registers. All analog gain functions are fully differential to minimize noise pickup. In addition, programmable test modes allow the analog blocks (preamps, AGC, and filter) to be individually bypassed or tested in combination.

The preamplifier sections provide either 30 dB or 36 dB of fixed low-noise differential gain.

The AGC section controls the input signal level to the filter, and includes a voltage-controlled gain amplifier, full-wave rectifier, and dual-rate charge-pump. The AGC circuit has a gain range of -11dB to 21dB in data channels, -1.5dB to 30.5dB in servo channels, and may be forced to a fixed-gain mode by a control bit in the AGC control register. The AGC charge pump has a dual-rate mode which insures fast gain acquisition after mode transitions.

The channel high-pass filter has a single zero and single pole that yields a lower cutoff frequency, F_{cl}, which is programmable from 4.5 KHz to 45 KHz with 4-bit resolution. Two other zeros in the gain chain are introduced by the AC coupling circuitry, and are fixed at 4.5 KHz (nominal).

The data and servo 3-pole, linear-phase, 0.05°equiripple low-pass filters feature a programmable cutoff frequency range which is trimmed at wafer probe to insure accuracy. Filter functions are controlled by 7-bit DAC for high resolution. DC coupling with internal offset correction loops eliminates the need for external coupling capacitors.

The input referred noise of the entire channel is 1.25nV/√Hz.

The write drivers have an H-bridge configuration, and write current is programmable from 0 to at least 50 mA with a 7-bit DAC. A Write Unsafe monitor circuit detects an open or shorted write head and aborts write operations to safeguard existing data. An on-chip power supply monitor shuts down the driver if the VDD supply voltage falls below a predetermined value.

The device requires nominal +5 volt power supply and features several shutdown modes to conserve power.

The SR3440B utilizes an advanced BiCMOS process technology, along with advanced circuit design techniques which result in a high performance device. The device is available in a 100TQFP/PFD PowerPad® package for enhanced power dissipation capability.

FEATURES

HEAD READ PREAMPLIFIERS

- 8 differential preamps for 4 data heads and 4 servo heads
- Selectable 30 dB or 36 dB gain ± 2 dB
- Read preamp Input noise = 0.5 nV/√Hz typ

AUTOMATIC GAIN CONTROLLED AMPLIFIER

- Gain control range of -11 dB to +21 dB in 0.51 dB steps (6 bits) in data channels
- Gain control range of –1.5 dB to +30.5 dB in 0.51 dB steps (6 bits) in servo channels
- Amplitude control range of 0.8 V to 1.1 V in 0.1 V steps (2 bits)
- [D,S]AGCHOLDx pin can select analog memory or DAC gain control
- Analog gain-hold mode with controlled drift
- Precision full-wave rectifier with peak detect output ([D,S]LEVELx pin)
- Programmable peak detector droop current from 3 to 50 μA in 3.1 μA steps (4 bits)
- Dual rate charge pump for fast transient recovery
- Fast attack/decay modes at read/write transitions for rapid gain acquisition
- Fast recovery mode at power-up to minimize transients
- Locked 0 dB gain capability

AC COUPLERS

- Two AC couplers, one between preamp and AGC, one between AGC and the low pass filter.

HIGHPASS FILTER

- Programmable single pole from 4.5 to
- 45 KHz in 2.7 KHz steps (4 bits)

PROGRAMMABLE LOW PASS FILTER

- 3-pole equiripple lowpass filter
- Programmable data cutoff frequency from 0.96 to 9.3 MHz (Low range) 1.9 to 18.63 MHz (High Range)
- Programmable servo cutoff frequency from 0.65 to 6.25 MHz (Low range) 0.65 to 12.5 MHz (High Range)

HEAD WRITE DRIVERS

- Write data accepted in either WD (NRZ) or WDI format
- Write current range from 0 to 56 mA in 0.44 mA steps (7 bits)
- Head output voltage swing = 7 V peak-to-peak minimum
- Write driver inhibited for values of VDD below 4.2 volts

POWER FAULT MONITOR

- +5 volt supplies monitored for dropouts below +4.2 volts ± 0.25 volts
- Power Monitor Reset Not (PMR) digital output for +5 volt dropouts

PROGRAMMABILITY AND TEST MODES

- Full functional and parametric programmability through serial port interface
- Single or combination analog block bypassing
- Differential analog test points with access to major functional block outputs
- DACOUT analog test point to verify DAC monotonicity
- On-chip silicon diode available to monitor junction temperature

BLOCK DIAGRAMS

The block diagram of the TI SR3440B is shown in Figure 1. Figure 2 shows the sub-block diagram of the data channel, Figure 3 is the sub-block diagram of the servo channel, and Figure 4 is the sub-block diagram of the write channel. These sub-blocks are referenced by the chip block diagram.

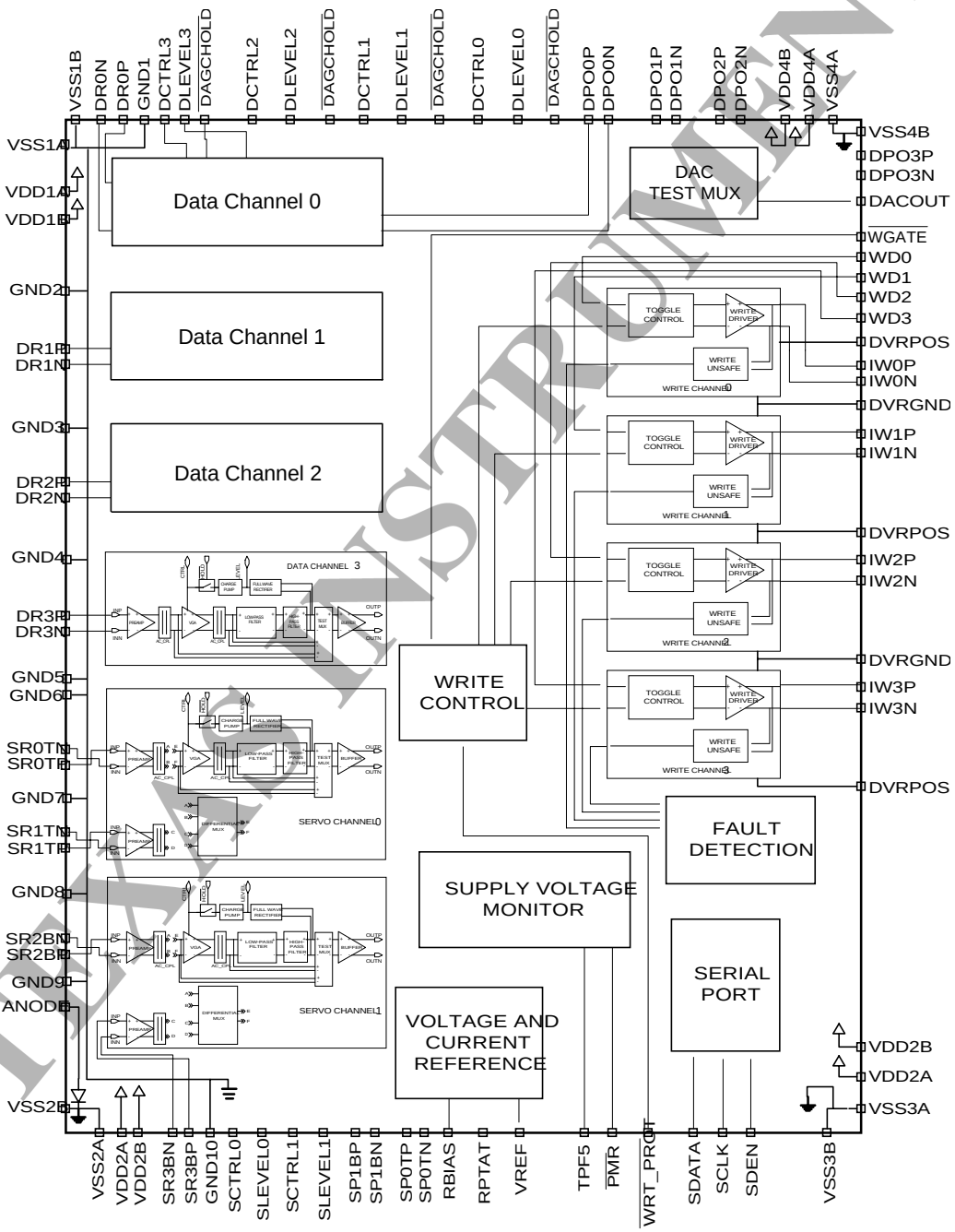


FIGURE 1: SR3440B Block Diagram

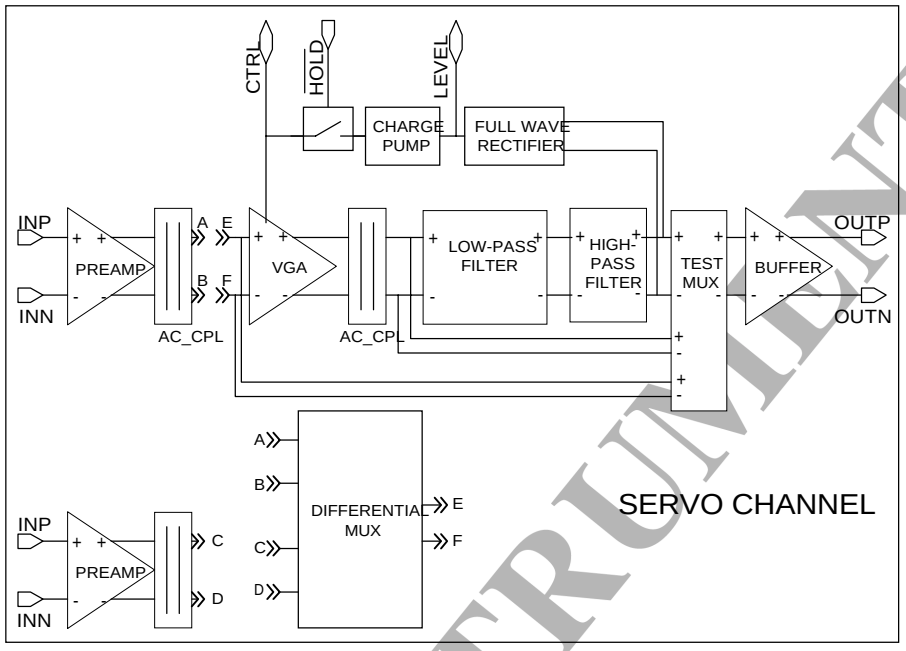


FIGURE 2: Data Channel Block Diagram

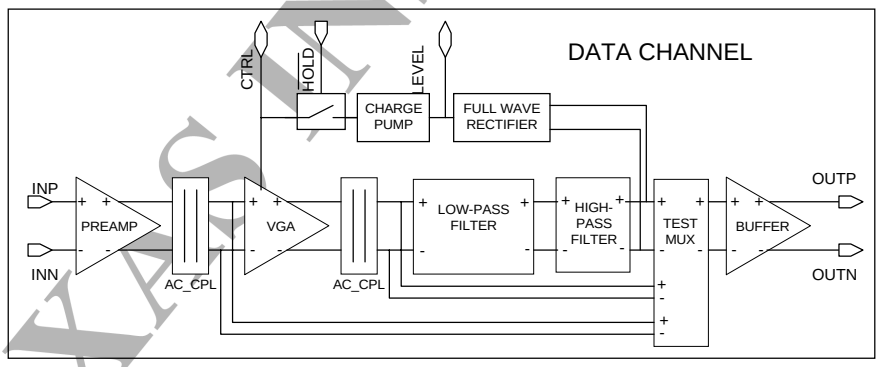


FIGURE 3: Servo Channel Block Diagram

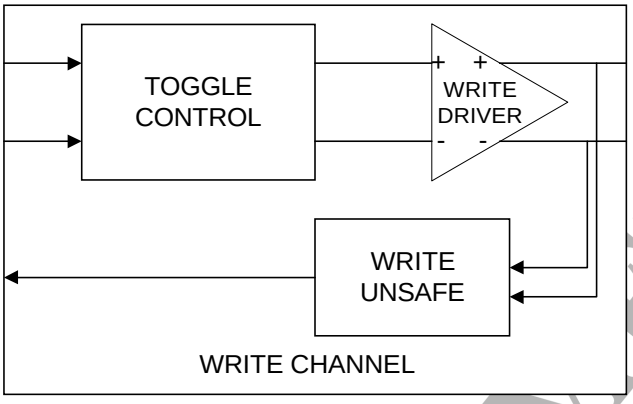


FIGURE 4: Write Channel Block Diagram

FUNCTIONAL DESCRIPTION

MODE AND POWER-DOWN CONTROL

The WGATE (WRITE GATE NOT) input controls the device operating mode. Initiation of Read Mode (WGATE= HIGH) is asynchronous, and may occur or terminate at any position on the media. Initiation of Write Mode (WGATE= LOW) is also asynchronous, but should not be terminated prior to the last output write data pulse.

Power-down is controlled by the POWER_EN bit [D0] in the CMOS Control A register (R1), accessed through the serial port interface. A "1" written to this bit location powers the device up; a "0" places the device in "sleep" or micropower mode. This bit does not affect the CMOS serial port logic or the VCC POWER_OK reference/comparator, which are always active.

Individual power enable bits allow selective shutdown of portions of the device. A description of the control bits is given in the serial port register description section.

HEAD PREAMPLIFIERS

Eight low-noise differential amplifiers with selectable gain of either 30 dB (32 V/V) or 36 dB (63 V/V) are provided to increase the signal amplitudes from four data heads and four servo heads. Each head output is AC-coupled into the appropriate preamp input. Internal biasing sets the correct DC common-mode voltage for the preamp input stage. An input signal range of 0.2 mV to 8 mV can be accommodated with full amplitude stabilization by the AGC block. Each preamp exhibits a minimum bandwidth of 50 MHz.

Each preamp has a bypass mode in which the gain is forced to +1.0. This facilitates testing of the analog blocks found later in the signal-processing path. The location of the bypass control bit for each preamp (AMPx_BYP) is given in the serial port map of Table 2.

AUTOMATIC GAIN-CONTROLLED AMPLIFIER

The automatic gain control (AGC) circuit maintains a constant amplitude at the lowpass filter outputs when in AGC mode. The amplitude can be programmed from 0.8 to 1.1 Vppd with an internal 2-bit control DAC. The AGC outputs are DC-coupled to the highpass filter inputs, and can be monitored for test purposes at the respective differential buffer output pins (DPxxp/DPxxn or SPxxp/SPxxn) by setting the two control bits in the associated Test MUX Control register.

The gain of the AGC amplifier is controlled by the voltage V(xCTRLx) stored on the external CxCTRLx hold capacitor. A dual-rate charge pump drives CxCTRLx with currents that depend on the instantaneous differential voltage at the lowpass filter outputs, FNP/FNN. Attack currents will lower V(xCTRLx), which reduces the amplifier gain; while decay currents increase V(xCTRLx), which increases the amplifier gain. When the signal is greater than 100% of the correct AGC level, the nominal attack current of 0.35 mA is used to reduce the gain. If the signal is greater than 125% of the correct AGC level, a fast attack current of 4 times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high, yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 3 μA acts to increases the amplifier gain when the signal at the filter outputs is less than the AGC reference. The large ratio of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 42. Fast decay mode is also initiated by a transition from micropower mode in order to rapidly recover from any transients or drift which may have occurred on the CxCTRLx hold capacitor. There is a 1-μS delay inserted before the AGC charge pump is allowed to drive the CxCTRLx capacitor. Fast decay mode also triggers an internal Low-z mode which allows the internal AC-coupling capacitors to recover more quickly from large accumulated voltages.

The charge pump which sets the AGC control voltage at the CTRL pin is modulated by the filtered output voltage of the peak detector, which appears at the LEVEL pin. The droop rate at the LEVEL pin is controlled by a 4-bit DAC which varies the discharge current at the CLEVEL capacitor from 3.125 μA to 50 μA. The LEVEL Control registers (R19-21) contain these bits.

A hold mode is provided to keep the AGC gain unchanged during a write operation. When the HOLD pin is driven LOW, the dual-rate charge pump

is disabled, and the voltage at xCTRLx will be held constant (subject to leakage currents). Four HOLD pins are provided for the data channels; the HOLD signals for the two servo channels are found in the serial port registers.

The AGC amplifier can also be set into a fixed gain mode. The gain is programmable over a -11 to +21 dB range in data channels and -1.5 to +30.5 dB range in servo channels by bits AGx[0:5] in the AGC Control registers (R13-R18). Selection of the AGC mode is controlled by the state of the AGCx_MODE bit in the AGC Mode register (R22). A description of the mode control bits is given in the serial port register description section.

The AGC block may also be switched between its normal analog AGC function and fixed gain mode with its associated [D,S]AGCHOLDx pin. HOLD[1-6]_MODE control bits in the AGC Hold Mode register (R23) determine the function of the [D,S]AGCHOLDx pin. When the bit is 0, the [D,S]AGCHOLDx pin switches the gain block between normal analog automatic gain control and analog memory hold. When the bit is 1, the pin switches the gain block between normal analog automatic gain control and digital fixed gain mode

For test purposes, each AGC amplifier can be set to a gain of 1 by the corresponding AGCx_BYP bit in the AGC Bypass register (R24).

PROGRAMMABLE LOW PASS FILTERS

The SR3440B contains six 3-pole low-pass filters. Each transconductance-capacitance (gm-C) filter approximates a linear phase or constant group delay response. Programmable bandwidth is provided by internal 7-bit control DACs.

The filter implements a 0.05° equiripple linear phase response. The normalized transfer function

(i.e. $s = j\omega_C = j2\pi f_C$, where $j^2 = -1$) is:

$$V_o/V_i = H_1 \times H_2$$

where

$$H_1 = [1.87974] / (s^2 + 1.7082s + 1.87974)$$

$$H_2 = 1.0459 / (s + 11.01459)$$

The normalized pole frequencies and quality factors of the biquads and bicubic sections are:

$$\omega_1 = 1.3710 \qquad Q_1 = 0.80262$$

$$\omega_2 = 1.0459$$

The frequency is denormalized by replacing s by $s/2\pi f_C$.

The differential signals from the AGC are internally coupled to the inputs of the filter. The programmable bandwidth is controlled by an internal DAC whose registers are programmable by the serial port. The current reference for the frequency control FC_DAC is set using a single external resistor connected from pin RPTAT to ground.

The programmable bandwidth is set by the filter cutoff DAC according to the following equations:

$$-3dB\ f_C = (D7+1) \bullet 0.07335 \bullet FCDAC\ MHz$$

for $13_{dec} \le FC\_DAC \le 127_{dec}$ in data channels

where D7 is the F16Mx bit value for the filter cutoff register.

$$-3dB\ f_C = (D7+1) \bullet 0.049213 \bullet FCDAC\ MHz$$

for $13_{dec} \le FC\_DAC \le 127_{dec}$ in servo channels

where D7 is the F16Mx bit value for the filter cutoff register.

Note that the specifications may not be satisfied for $FCDAC < 13_{dec}$.

TEST MULTIPLEXER/OUTPUT BUFFER

A wideband, full differential multiplexer selects the input signal of the output buffer driving each gain channel's output pins. In normal operation, the lowpass filter output is selected. The preamp output or AGC output may also be selected through two control bits in the serial port. This arrangement, in conjunction with the individual block bypass capability, allows the parameters of an individual section to be verified. Output buffer bandwidth is greater than 40 MHz, and each buffer may be switched into a high output impedance state to allow a single selected analog output to drive a common signal routing bus. The truth table for the test multiplexer is shown in Table 1.

TABLE 1: Multiplexed Test Point Output

TST_ MUXx [1]	TST_ MUXx [0]	[D,S]POxp	[D,S]POxn
0	0	HI-Z	HI-Z
0	1	PREAMPp	PREAMPn
1	0	AGCp	AGCn
1	1	FNp	FNn

HEAD WRITE DRIVER

Write mode is entered by driving the write gate NOT pin ($\overline{\text{WGATE}}$) LOW, activating the Write Unsafe (WUS) circuitry. Provision is made for input of either WD or WDI data. When the write mode bit WRT_MODE in the serial port is LOW (WD or NRZ mode), the head current reverses on each transition of the Write Data (WDx). When the write mode bit is HIGH (WDI mode), head current reverses on each low-to-high transition of the Write Data. Note that a preceding Read to Write transition initializes the Write Data flip-flop to pass write current into the "p" pin of the device. In this case, the "n" pin is at a higher potential than the "p" pin. Write current magnitude is controlled by 7 bits (WRx[0:7]) in the Head Write Current register. During read mode, or during a power fault, or if WRT_PROT is LOW, the H-bridge driver outputs are switched to ground. Both WGATE and WRT_PROT input pins are protected against broken external connections by two internal 100 K pullup resistors to the VDD3 supply.

The WUS circuitry detects a write head short to ground of approximately 5 Ω or less, as well as a head resistance above 150 Ω. If either of these faults occur, the associated write driver is inhibited, and the status bit WUS in the serial port will be set. The bit can be reset with a serial port write operation. WUS can be turned off during write current calibration by WUS_EN in the serial port

The two write modes are illustrated in the following figures. In Figure 5, the driver is in WD or NRZ mode, and the direction of the head current is determined by the state of the data. If the driver is switched to high impedance, the head current will decay to zero with a time constant determined by the write head inductance and the value of the external damping resistor.

In Figure 6, the driver is in WDI mode, and the direction of the head current toggles on each rising edge of the write data signal. Again, if the driver is switched to high impedance by either the internal WUS circuitry, the Power Fault Monitor, or the external write protect signal, the head current will decay to zero until the driver is again enabled.

POWER FAULT MONITOR

The Power Fault Monitor detects low voltage on the +5 volt supply. A power fault is declared when any supply falls below threshold for more than 1 μsec. A failure of any +5 volt supply will set the PF5 status bit in the serial port register HIGH and drive the PMR pin LOW, which disables the write drivers. The PMR pin will return to the HIGH state once the +5 volt supply fault disappears.

SERIAL PORT INTERFACE

The serial interface is a CMOS bi-directional port for reading and writing programming data to and from the 54 internal 8-bit registers of the SR3440B. The serial port data transfer format is shown in Figure 7. The serial port is enabled for data transfer when the Serial Data Enable (SDEN) pin is HIGH (logic "1"). SDEN must be forced HIGH prior to any transmission, and it should remain HIGH until the completion of the transfer. At the end of each transfer SDEN should be brought LOW (logic "0").

When SDEN is HIGH, the data presented to the Serial Data (SDATA) pin will be latched into the SR3440B on each rising edge of the Serial Clock (SCLK). Rising edges of SCLK should occur only when the desired bit of address or data is being presented on the SDATA line. Serial data transfers must occur in 16-bit packets. If less than 16 clocks occur, the data transfer is aborted. The data is latched into the internal register on the falling edge of SDEN.

Each 16-bit transfer consists of 1 Read/Write instruction bit (R/W), 7 address bits, and 8 data bits. The instruction bit is used as a flag to put the port into read or write mode. The address bits select the desired device and an internal data register. The address and data fields are transmitted **MSB first** (where MSB is defined as Bit 7), LSB last. When writing to the internal registers, R/W must be LOW (logic "0"), followed by the address and data packets. When reading from the internal registers, R/W must be HIGH (logic "1"), followed by the address field. The SR3440B will return the contents of the addressed register during the 8-bit data field. Note that in read mode there is a turn-around time (Ttrn) for the selected register to respond with data.

The serial port has a power-on reset function which loads default values into the registers when power is first applied to the chip, or when $5B_h$ (0101 1011) is written to the I.D. register. The default values are given in Table 2.

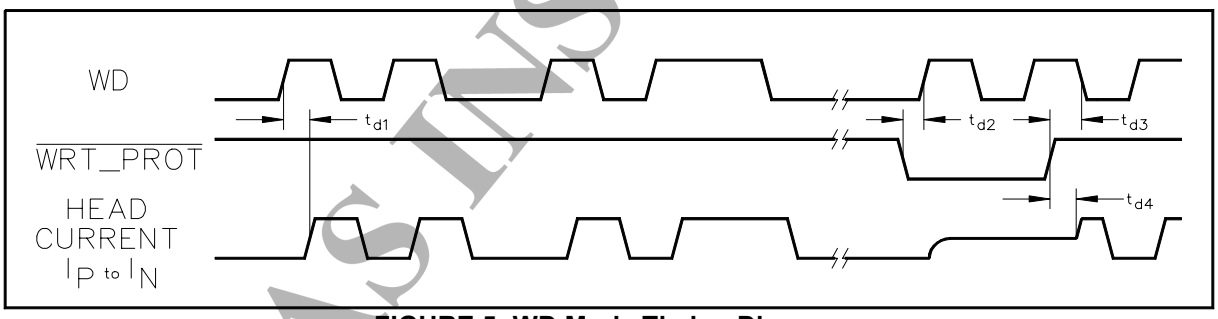


FIGURE 5: WD Mode Timing Diagram

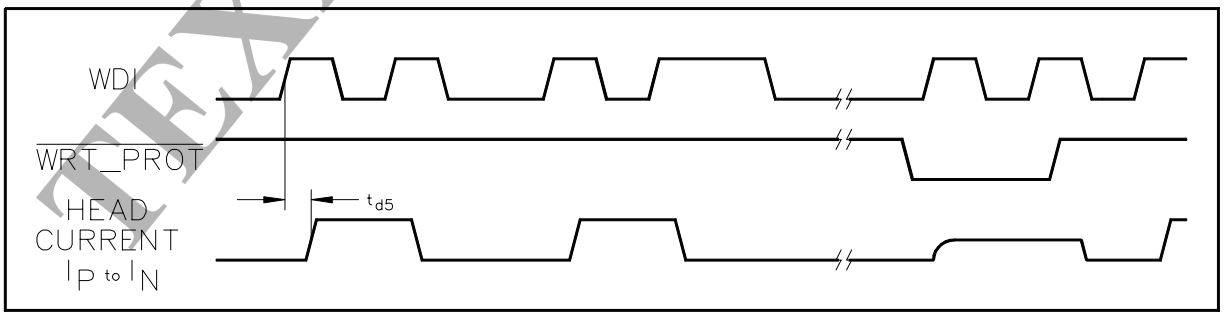


FIGURE 6: WDI Mode Timing Diagram

SERIAL PORT REGISTER MAP

Table 2 gives the location and function of the bits in the 54 serial port CMOS registers, which are R0 through R53 that will be used in application. The 8-bit address field is divided into a single Read/Write control bit A[7], followed by a 7-bit register address (bits A[6:0]). Register addresses start at zero, with the first register R0 containing the read-only I.D. byte.

It is very important that control routines for loading data into the registers via the serial port interface do not address registers above R53. This device has additional registers above R53 which are used only during parameter trim at wafer probe. Writing to these higher addresses could affect various parameters such as the RBIAS bandgap voltage, filter cutoff frequency, etc. If the register data at these upper addresses are accidentally modified, recovery is possible by writing the value $5B_h$ (0101 1011) to the ID register, which will reset the device to power-up default values.

SERIAL PORT REGISTER POWER-ON DEFAULT VALUES

The boxed values in Table 2 show the default values. Each register is set to this value when the SR3440B is first powered up, or when the serial port is reset by writing $5B_h$ to the read-only ID register (R0).

TEST REGISTERS

The SR3440B serial port contains several registers(R53 through R63) which are not intended to be used in the application, so they are called “test registers”. These test registers are used by Texas Instruments SPG during wafer probe to trim certain critical parameters of the device. The registers occupy the highest address space available with a 6-bit address length. **It is important that application firmware used to write configuration/mode data to the normal serial port control registers does not address these upper registers, or erratic circuit performance may result.**

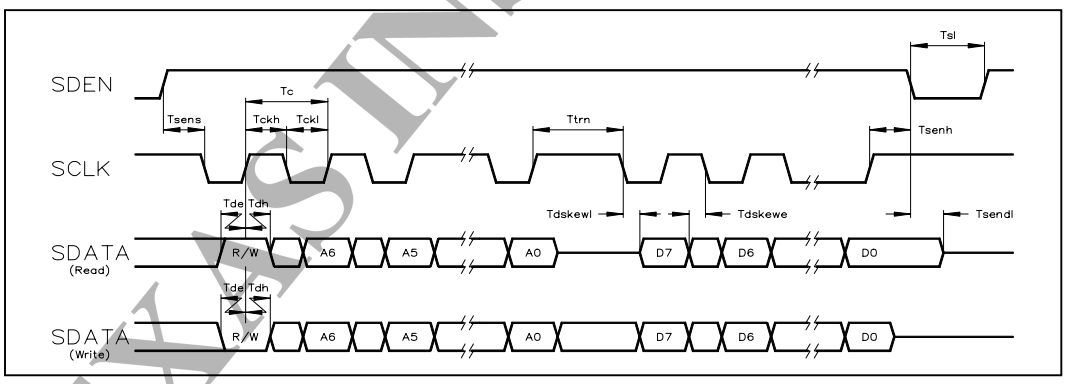


FIGURE 7: Serial Port Interface Format and Timing

TABLE 2: SR3440B Serial Port Register Map

REG #	REGISTER NAME	ADDRESS R/W							A6	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R0	I.D. / VERSION	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
R1	POWER CONTROL	∅	0	0	0	0	0	0	1	Default=0	SCH1_EN 0=Sleep 1=Normal	SCH0_EN 0=Sleep 1=Normal	DCH3_EN 0=Sleep 1=Normal	DCH2_EN 0=Sleep 1=Normal	DCH1_EN 0=Sleep 1=Normal	DCH0_EN 0=Sleep 1=Normal	POWER_EN 0=Sleep 1=Normal
R2	WRITE EN./FAULT STATUS	∅	0	0	0	0	0	1	0	Default=0	WCH3_EN 0=Sleep 1=Normal	WCH2_EN 0=Sleep 1=Normal	WCH1_EN 0=Sleep 1=Normal	WCH0_EN 0=Sleep 1=Normal	WUS 0=OK 1=Fault	Default=0	PF5 0=OK 1=Fault
R11	PREAMP GAIN	∅	0	0	0	1	0	1	1	PRMP8_GAIN 0=30dB 1=36dB	PRMP7_GAIN 0=30dB 1=36dB	PRMP6_GAIN 0=30dB 1=36dB	PRMP5_GAIN 0=30dB 1=36dB	PRMP4_GAIN 0=30dB 1=36dB	PRMP3_GAIN 0=30dB 1=36dB	PRMP2_GAIN 0=30dB 1=36dB	PRMP1_GAIN 0=30dB 1=36dB
R12	PREAMP BYPASS	∅	0	0	0	1	1	0	0	PRMP8_BYP 0=Normal 1=Bypass	PRMP7_BYP 0=Normal 1=Bypass	PRMP6_BYP 0=Normal 1=Bypass	PRMP5_BYP 0=Normal 1=Bypass	PRMP4_BYP 0=Normal 1=Bypass	PRMP3_BYP 0=Normal 1=Bypass	PRMP2_BYP 0=Normal 1=Bypass	PRMP1_BYP 0=Normal 1=Bypass
R13	AGC1 CONTROL	∅	0	0	0	1	1	0	1	AR1[1] Default=1	AR1[0] Default=1	AG1[5] Default=0	AG1[4] Default=1	AG1[3] Default=0	AG1[2] Default=0	AG1[1] Default=1	AG1[0] Default=0
R14	AGC2 CONTROL	∅	0	0	0	1	1	1	0	AR2[1] Default=1	AR2[0] Default=1	AG2[5] Default=0	AG2[4] Default=1	AG2[3] Default=0	AG2[2] Default=0	AG2[1] Default=1	AG2[0] Default=0
R15	AGC3 CONTROL	∅	0	0	0	1	1	1	1	AR3[1] Default=1	AR3[0] Default=1	AG3[5] Default=0	AG3[4] Default=1	AG3[3] Default=0	AG3[2] Default=0	AG3[1] Default=1	AG3[0] Default=0
R16	AGC4 CONTROL	∅	0	0	1	0	0	0	0	AR4[1] Default=1	AR4[0] Default=1	AG4[5] Default=0	AG4[4] Default=1	AG4[3] Default=0	AG4[2] Default=0	AG4[1] Default=1	AG4[0] Default=0
R17	AGC5 CONTROL	∅	0	0	1	0	0	0	1	AR5[1] Default=1	AR5[0] Default=1	AG5[5] Default=0	AG5[4] Default=1	AG5[3] Default=0	AG5[2] Default=0	AG5[1] Default=1	AG5[0] Default=0
R18	AGC6 CONTROL	∅	0	0	1	0	0	1	0	AR6[1] Default=1	AR6[0] Default=1	AG6[5] Default=0	AG6[4] Default=1	AG6[3] Default=0	AG6[2] Default=0	AG6[1] Default=1	AG6[0] Default=0
R19	LEVEL CONTROL A	∅	0	0	1	0	0	1	1	LV2[3] Default=0	LV2[2] Default=0	LV2[1] Default=0	LV2[0] Default=0	LV1[3] Default=0	LV1[2] Default=0	LV1[1] Default=0	LV1[0] Default=0
R20	LEVEL CONTROL B	∅	0	0	1	0	1	0	0	LV4[3] Default=0	LV4[2] Default=0	LV4[1] Default=0	LV4[0] Default=0	LV3[3] Default=0	LV3[2] Default=0	LV3[1] Default=0	LV3[0] Default=0
R21	LEVEL CONTROL C	∅	0	0	1	0	1	0	1	LV6[3] Default=0	LV6[2] Default=0	LV6[1] Default=0	LV6[0] Default=0	LV5[3] Default=0	LV5[2] Default=0	LV5[1] Default=0	LV5[0] Default=0
R22	AGC MODE / SERVO MUX	∅	0	0	1	0	1	1	0	BOT_MUX 0=SR2B 1=SR3B	TOP_MUX 0=SR0T 1=SR1T	AGC6_MODE 0=AGC 1=DAC	AGC5_MODE 0=AGC 1=DAC	AGC4_MODE 0=AGC 1=DAC	AGC3_MODE 0=AGC 1=DAC	AGC2_MODE 0=AGC 1=DAC	AGC1_MODE 0=AGC 1=DAC
R23	AGC HOLD MODE	∅	0	0	1	0	1	1	1	$\overline{\text{SAGC\_HLD1}}$ 0=Hold 1=Normal	$\overline{\text{SAGC\_HLD0}}$ 0=Hold 1=Normal	$\overline{\text{HLD6\_MODE}}$ 0=Analog 1=DAC	$\overline{\text{HLD5\_MODE}}$ 0=Analog 1=DAC	$\overline{\text{HLD4\_MODE}}$ 0=Analog 1=DAC	$\overline{\text{HLD3\_MODE}}$ 0=Analog 1=DAC	$\overline{\text{HLD2\_MODE}}$ 0=Analog 1=DAC	HLD*1_MODE 0=Analog 1=DAC

REG #	REGISTER NAME	ADDRESS R/W							A6	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R24	AGC BYPASS	∅	0	0	1	1	0	0	0	Default=0	Default=0	AGC6_BYP 0=Normal 1=Bypass	AGC5_BYP 0=Normal 1=Bypass	AGC4_BYP 0=Normal 1=Bypass	AGC3_BYP 0=Normal 1=Bypass	AGC2_BYP 0=Normal 1=Bypass	AGC1_BYP 0=Normal 1=Bypass
R25	HI-PASS CONTROL A	∅	0	0	1	1	0	0	1	HP2[3] Default=1	HP2[2] Default=1	HP2[1] Default=1	HP2[0] Default=1	HP1[3] Default=1	HP1[2] Default=1	HP1[1] Default=1	HP1[0] Default=1
R26	HI-PASS CONTROL B	∅	0	0	1	1	0	1	0	HP4[3] Default=1	HP4[2] Default=1	HP4[1] Default=1	HP4[0] Default=1	HP3[3] Default=1	HP3[2] Default=1	HP3[1] Default=1	HP3[0] Default=1
R27	HI-PASS CONTROL C	∅	0	0	1	1	0	1	1	HP6[3] Default=1	HP6[2] Default=1	HP6[1] Default=1	HP6[0] Default=1	HP5[3] Default=1	HP5[2] Default=1	HP5[1] Default=1	HP5[0] Default=1
R28	LO-PASS FILTER1 CUTOFF	∅	0	0	1	1	1	0	0	F16M1 Default=1	FC1[6] Default=1	FC1[5] Default=1	FC1[4] Default=1	FC1[3] Default=1	FC1[2] Default=1	FC1[1] Default=1	FC1[0] Default=1
R29	LO-PASS FILTER2 CUTOFF	∅	0	0	1	1	1	0	1	F16M2 Default=1	FC2[6] Default=1	FC2[5] Default=1	FC2[4] Default=1	FC2[3] Default=1	FC2[2] Default=1	FC2[1] Default=1	FC2[0] Default=1
R30	LO-PASS FILTER3 CUTOFF	∅	0	0	1	1	1	1	0	F16M3 Default=1	FC3[6] Default=1	FC3[5] Default=1	FC3[4] Default=1	FC3[3] Default=1	FC3[2] Default=1	FC3[1] Default=1	FC3[0] Default=1
R31	LO-PASS FILTER4 CUTOFF	∅	0	0	1	1	1	1	1	F16M4 Default=1	FC4[6] Default=1	FC4[5] Default=1	FC4[4] Default=1	FC4[3] Default=1	FC4[2] Default=1	FC4[1] Default=1	FC4[0] Default=1
R32	LO-PASS FILTER5 CUTOFF	∅	0	1	0	0	0	0	0	F16M5 Default=0	FC5[6] Default=1	FC5[5] Default=1	FC5[4] Default=1	FC5[3] Default=1	FC5[2] Default=1	FC5[1] Default=1	FC5[0] Default=1
R33	LO-PASS FILTER6 CUTOFF	∅	0	1	0	0	0	0	1	F16M6 Default=0	FC6[6] Default=1	FC6[5] Default=1	FC6[4] Default=1	FC6[3] Default=1	FC6[2] Default=1	FC6[1] Default=1	FC6[0] Default=1
R46	FILTER BYPASS	∅	0	1	0	1	1	1	0	Default=0	Default=0	FLT6_BYP 0=Normal 1=Bypass	FLT5_BYP 0=Normal 1=Bypass	FLT4_BYP 0=Normal 1=Bypass	FLT3_BYP 0=Normal 1=Bypass	FLT2_BYP 0=Normal 1=Bypass	FLT1_BYP 0=Normal 1=Bypass
R47	TEST MUX CONTROL A	∅	0	1	0	1	1	1	1	Default=0	Default=0	TST_MUX3[1] 10=AGC 11=Filter	TST_MUX3[0] 00=Hi-Z 01=Preamp	TST_MUX2[1] 10=AGC 11=Filter	TST_MUX2[0] 00=Hi-Z 01=Preamp	TST_MUX1[1] 10=AGC 11=Filter	TST_MUX1[0] 00=Hi-Z 01=Preamp
R48	TEST MUX CONTROL B	∅	0	1	1	0	0	0	0	Default=0	Default=0	TST_MUX6[1] 10=AGC 11=Filter	TST_MUX6[0] 00=Hi-Z 01=Preamp	TST_MUX5[1] 10=AGC 11=Filter	TST_MUX5[0] 00=Hi-Z 01=Preamp	TST_MUX4[1] 01=AGC 11=Filter	TST_MUX4[0] 00=Hi-Z 01=Preamp
R49	WRITE DRIVER0 CURRENT	∅	0	1	1	0	0	0	1	WRT_MODE1 1=WDI-	WD1[6] Default=0	WD1[5] Default=1	WD1[4] Default=1	WD1[3] Default=1	WD1[2] Default=1	WD1[1] Default=0	WD1[0] Default=0
R50	WRITE DRIVER1 CURRENT	∅	0	1	1	0	0	1	0	WRT_MODE2 1=WDI-	WD2[6] Default=0	WD2[5] Default=1	WD2[4] Default=1	WD2[3] Default=1	WD2[2] Default=1	WD2[1] Default=0	WD2[0] Default=0

REG #	REGISTER NAME	ADDRESS R/W						A6	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R51	WRITE DRIVER2 CURRENT	∅	0	1	1	0	0	1	1	WRT_MODE3 1=WDI-	WD3[6] Default=0	WD3[5] Default=1	WD3[4] Default=1	WD3[3] Default=1	WD3[2] Default=1	WD3[1] Default=0	WD3[0] Default=0
R52	WRITE DRIVER3 CURRENT	∅	0	1	1	0	1	0	0	WRT_MODE4 1=WDI-	WD4[6] Default=0	WD4[5] Default=1	WD4[4] Default=1	WD4[3] Default=1	WD4[2] Default=1	WD4[1] Default=0	WD4[0] Default=0

TABLE 3: SR3440B Test Register Serial Port Map

REG #	REGISTER NAME	ADDRESS R/W						A6	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R53	SSI TEST REGISTER	∅	0	1	1	0	1	0	1	Default=1	Default=0	Default=0	Default=0	Default=0	Default=0	Default=0	Default=0
R56	SSI TEST REGISTER	∅	0	1	1	1	0	0	0	Default=0	Default=0	Default=0	Default=0	Default=0	Default=0	Default=0	Default=0
R57	SSI TEST REGISTER	∅	0	1	1	1	0	0	1	Default=0	Default=1	Default=1	Default=0	Default=0	Default=0	Default=0	Default=0
R58	SSI TEST REGISTER	∅	0	1	1	1	0	1	0	Default=0	Default=1	Default=1	Default=0	Default=0	Default=0	Default=0	Default=0
R59	SSI TEST REGISTER	∅	0	1	1	1	0	1	1	Default=0	Default=1	Default=1	Default=0	Default=0	Default=0	Default=0	Default=0
R60	SSI TEST REGISTER	∅	0	1	1	1	1	0	0	Default=0	Default=1	Default=1	Default=0	Default=0	Default=0	Default=0	Default=0
R61	SSI TEST REGISTER	∅	0	1	1	1	1	0	1	Default=0	Default=1	Default=1	Default=0	Default=0	Default=0	Default=0	Default=0
R62	SSI TEST REGISTER	∅	0	1	1	1	1	1	0	Default=0	Default=1	Default=1	Default=0	Default=0	Default=0	Default=0	Default=0
R63	SSI TEST REGISTER	∅	0	1	1	1	1	1	1	Default=0	Default=0	Default=1	Default=0	Default=1	Default=1	Default=1	Default=1

[R0] DEVICE ID / VERSION REGISTER

Register 0 is a read-only register, and contains two nibbles (4 bits) which indicate respectively the type of device present (MSB), and the revision of the device (LSB).

BIT	NAME	DESCRIPTION
7:4	Device Type	
0:3	Device Revision	

[R1] POWER CONTROL REGISTER

Note: This power switch is wired in series with each of the following power enable switches, so a "0" always forces the entire device into micropower mode.

BIT	NAME	DESCRIPTION
7	unused	Default =0
6	SCH1_EN	1= enables power to the channel 0= switches the channel into micropower mode
5	SCH0_EN	1= enables power to the channel 0= switches the channel into micropower mode
4	DCH3_EN	1= enables power to the channel 0= switches the channel into micropower mode
3	DCH2_EN	1= enables power to the channel 0= switches the channel into micropower mode
2	DCH1_EN	1= enables power to the channel 0= switches the channel into micropower mode
1	DCH0_EN	1= enables power to the channel 0= switches the channel into micropower mode
0	POWER_EN	1= enables power to the entire device 0= switches the device into micropower mode

[R2] WRITE ENABLE / FAULT STATUS REGISTER

Bits D0 through D2 are intended to be read-only, although zeros can be written to them to clear existing fault flags.

BIT	NAME	DESCRIPTION
7	unused	Default =0
6	WCH3_EN	1= enables power to the entire device 0= switches the device into micropower mode
5	WCH2_EN	1= enables power to the entire device 0= switches the device into micropower mode
4	WCH1_EN	1= enables power to the entire device 0= switches the device into micropower mode
3	WCH0_EN	1= enables power to the entire device 0= switches the device into micropower mode
2	WUS	1 indicates a fault, and disables the write drivers 0 indicates normal conditions, and enables the write drivers
1	unused	Default =0
0	PF5	1 indicates a power fault 0 indicates the supplies are above the nominal +4.2 volt threshold

[R11] PREAMP GAIN REGISTER

BIT	NAME	DESCRIPTION
7	PRMP8_GAIN	selects the fixed gain of Preamp 8 in Servo Channel 1: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB
6	PRMP7_GAIN	selects the fixed gain of Preamp 7 in Servo Channel 1: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB
5	PRMP6_GAIN	selects the fixed gain of Preamp 6 in Servo Channel 0: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB
4	PRMP5_GAIN	selects the fixed gain of Preamp 5 in Servo Channel 0: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB
3	PRMP4_GAIN	selects the fixed gain of Preamp 4 in Data Channel 3: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB
2	PRMP3_GAIN	selects the fixed gain of Preamp 3 in Data Channel 2: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB
1	PRMP2_GAIN	selects the fixed gain of Preamp 2 in Data Channel 1: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB
0	PRMP1_GAIN	selects the fixed gain of Preamp 1 in Data Channel 0: 1 = selects a gain of 63 V/V, or 36 dB 0 = selects a gain of 32 V/V, or 30 dB

[R12] PREAMP BYPASS REGISTER

BIT	NAME	DESCRIPTION
7	PRMP8_BYP	enables the bypass mode of Preamp 8 in Servo Channel 1: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation
6	PRMP7_BYP	enables the bypass mode of Preamp 7 in Servo Channel 1: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation
5	PRMP6_BYP	enables the bypass mode of Preamp 6 in Servo Channel 0: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation
4	PRMP5_BYP	enables the bypass mode of Preamp 5 in Servo Channel 0: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation
3	PRMP4_BYP	enables the bypass mode of Preamp 4 in Data Channel 3: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation
2	PRMP3_BYP	enables the bypass mode of Preamp 3 in Data Channel 2: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation
1	PRMP2_BYP	enables the bypass mode of Preamp 2 in Data Channel 1: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation
0	PRMP1_BYP	enables the bypass mode of Preamp 1 in Data Channel 0: 1 = forces the preamp into a fixed gain of 1 for test purposes 0 = enables normal high-gain operation

[R13] AGC1 CONTROL REGISTER [DATA CHANNEL 0]

BIT	NAME	DESCRIPTION
7-6	AR1[1:0]	AGC Amplitude Reference = 0.8 + 0.10 x AR1 (V) where $0_{dec} \leq AR1 \leq 3_{dec}$ Total range = 0.8 to 1.1 Volts
5-0	AG1[5:0]	VGA Gain = -11 + 0.51 x AG1 (dB) where $0_{dec} \leq AG1 \leq 63_{dec}$ Total range = -11 to 21 dB

[R14] AGC2 CONTROL REGISTER [DATA CHANNEL 1]

BIT	NAME	DESCRIPTION
7-6	AR2[1:0]	AGC Amplitude Reference = 0.8 + 0.10 x AR2 (V) where $0_{dec} \leq AR2 \leq 3_{dec}$ Total range = 0.8 to 1.1 Volts
5-0	AG2[5:0]	VGA Gain = -11 + 0.51 x AG2 (dB) where $0_{dec} \leq AG2 \leq 63_{dec}$ Total range = -11 to 21 dB

[R15] AGC3 CONTROL REGISTER [DATA CHANNEL 2]

BIT	NAME	DESCRIPTION
7-6	AR3[1:0]	AGC Amplitude Reference = 0.8 + 0.10 x AR3 (V) where $0_{dec} \leq AR3 \leq 3_{dec}$ Total range = 0.8 to 1.1 Volts
5-0	AG3[5:0]	VGA Gain = -11 + 0.51 x AG3 (dB) where $0_{dec} \leq AG3 \leq 63_{dec}$ Total range = -11 to 21 dB

[R16] AGC4 CONTROL REGISTER [DATA CHANNEL 1]

BIT	NAME	DESCRIPTION
7-6	AR4[1:0]	AGC Amplitude Reference = 0.8 + 0.10 x AR4 (V) where $0_{dec} \leq AR4 \leq 3_{dec}$ Total range = 0.8 to 1.1 Volts
5-0	AG4[5:0]	VGA Gain = -11 + 0.51 x AG4 (dB) where $0_{dec} \leq AG4 \leq 63_{dec}$ Total range = -11 to 21 dB

[R17] AGC5 CONTROL REGISTER [SERVO CHANNEL 0]

BIT	NAME	DESCRIPTION
7-6	AR5[1:0]	AGC Amplitude Reference = 0.8 + 0.10 x AR5 (V) where $0_{dec} \leq AR5 \leq 3_{dec}$ Total range = 0.8 to 1.1 Volts
5-0	AG5[5:0]	VGA Gain = -1.5 + 0.51 x AG5 (dB) where $0_{dec} \leq AG5 \leq 63_{dec}$ Total range = -1.5 to 30.5 dB

[R18] AGC6 CONTROL REGISTER [SERVO CHANNEL 1]

BIT	NAME	DESCRIPTION
7-6	AR6[1:0]	AGC Amplitude Reference = 0.8 + 0.10 x AR6 (V) where $0_{dec} \leq AR6 \leq 3_{dec}$ Total range = 0.8 to 1.1 Volts
5-0	AG6[5:0]	VGA Gain = -1.5 + 0.51 x AG6 (dB) where $0_{dec} \leq AG6 \leq 63_{dec}$ Total range = -1.5 to 30.5 dB

[R19] LEVEL CONTROL A REGISTER

BIT	NAME	DESCRIPTION
7-4	LV2[3:0]	DLEVEL1 Droop Current = 3.125 +3.125 x LV2 (µA) where $0_{dec} \le LV2 \le 15_{dec}$ Total range = 3.125 to 50 µA
3-0	LV1[3:0]	DLEVEL0 Droop Current = 3.125 +3.125 x LV1 (µA) where $0_{dec} \le LV1 \le 15_{dec}$ Total range = 3.125 to 50 µA

[R20] LEVEL CONTROL B REGISTER

BIT	NAME	DESCRIPTION
7-4	LV4[3:0]	DLEVEL3 Droop Current = 3.125 +3.125 x LV4 (µA) where $0_{dec} \le LV4 \le 15_{dec}$ Total range = 3.125 to 50 µA
3-0	LV3[3:0]	DLEVEL2 Droop Current = 3.125 +3.125 x LV3 (µA) where $0_{dec} \le LV3 \le 15_{dec}$ Total range = 3.125 to 50 µA

[R21] LEVEL CONTROL C REGISTER

BIT	NAME	DESCRIPTION
7-4	LV6[3:0]	SLEVELB Droop Current = 3.125 +3.125 x LV6 (µA) where $0_{dec} \le LV6 \le 15_{dec}$ Total range = 3.125 to 50 µA
3-0	LV5[3:0]	SLEVELT Droop Current = 3.125 +3.125 x LV5 (µA) where $0_{dec} \le LV5 \le 15_{dec}$ Total range = 3.125 to 50 µA

[R22] AGC MODE /SERVO MUX REGISTER

BIT	NAME	DESCRIPTION
7	BOT_MUX	Selects the signal source for VGA 6 in the Bottom Servo Channel: 1 = selects the output of Preamp 8 with inputs SR3bp and SR3bn 0 = selects the output of Preamp 7 with inputs SR2bp and SR2bn
6	TOP_MUX	Selects the signal source for VGA 5 in the Top Servo Channel: 1 = selects the output of Preamp 6 with inputs SR1tp and SR1tn 0 = selects the output of Preamp 5 with inputs SR0tp and SR0tn
5	AGC6_MODE	Controls the gain mode of VGA 6 in Servo Channel 1: 1 = enables VGA mode, with gain controlled by AG6_DAC 0 = enables normal AGC action with stabilized output amplitude
4	AGC5_MODE	Controls the gain mode of VGA 5 in Servo Channel 0: 1 = enables VGA mode, with gain controlled by AG5_DAC 0 = enables normal AGC action with stabilized output amplitude
3	AGC4_MODE	Controls the gain mode of VGA 4 in Data Channel 3: 1 = enables VGA mode, with gain controlled by AG4_DAC 0 = enables normal AGC action with stabilized output amplitude
2	AGC3_MODE	Controls the gain mode of VGA 3 in Data Channel 2: 1 = enables VGA mode, with gain controlled by AG3_DAC 0 = enables normal AGC action with stabilized output amplitude
1	AGC2_MODE	Controls the gain mode of VGA 2 in Data Channel 1: 1 = enables VGA mode, with gain controlled by AG2_DAC 0 = enables normal AGC action with stabilized output amplitude
0	AGC1_MODE	Controls the gain mode of VGA 1 in Data Channel 0: 1 = enables VGA mode, with gain controlled by AG1_DAC 0 = enables normal AGC action with stabilized output amplitude

[R23] AGC HOLD_ MODE REGISTER

BIT	NAME	DESCRIPTION
7	SACG_HLD1*	Places the AGC6 gain block in Servo Channel 1 in HOLD mode: 1 = enables normal AGC action 0 = causes the gain block to go into Hold mode
6	SACG_HLD0*	Places the AGC5 gain block in Servo Channel 0 in HOLD mode: 1 = enables normal AGC action 0 = causes the gain block to go into Hold mode
5	HLD6_MODE*	Determines the AGC gain control source when the SAGC_HLD1* bit is LOW: 1 = causes the internal DAC of Register 18 to be selected 0 = causes the SCTRL1 analog memory to be selected
4	HLD5_MODE*	Determines the AGC gain control source when the SAGC_HLD0* bit is LOW: 1 = causes the internal DAC of Register 17 to be selected 0 = causes the SCTRL0 analog memory to be selected
3	HLD4_MODE*	Determines the AGC gain control source when the DAGCHOLD3* pin is LOW: 1 = causes the internal DAC of Register 16 to be selected 0 = causes the DCTRL3 analog memory to be selected
2	HLD3_MODE*	Determines the AGC gain control source when the DAGCHOLD2* pin is LOW: 1 = causes the internal DAC of Register 15 to be selected 0 = causes the DCTRL2 analog memory to be selected
1	HLD2_MODE*	Determines the AGC gain control source when the DAGCHOLD1* pin is LOW: 1 = causes the internal DAC of Register 14 to be selected 0 = causes the DCTRL1 analog memory to be selected
0	HLD1_MODE*	Determines the AGC gain control source when the DAGCHOLD0* pin is LOW: 1 = causes the internal DAC of Register 13 to be selected 0 = causes the DCTRL0 analog memory to be selected

[R24] AGC BYPASS REGISTER

BIT	NAME	DESCRIPTION
7	unused	Default =0
6	unused	Default =0
5	AGC6_BYP	enables the bypass mode of AGC 6 in Servo Channel 1: 1 = forces the VGA into a fixed gain of 1 for test purposes 0 = enables normal variable-gain operation
4	AGC5_BYP	Enables the bypass mode of AGC 5 in Servo Channel 0: 1 = forces the VGA into a fixed gain of 1 for test purposes 0 = enables normal variable-gain operation
3	AGC4_BYP	Enables the bypass mode of AGC 4 in Data Channel 3: 1 = forces the VGA into a fixed gain of 1 for test purposes 0 = enables normal variable-gain operation
2	AGC3_BYP	Enables the bypass mode of AGC 3 in Data Channel 2: 1 = forces the VGA into a fixed gain of 1 for test purposes 0 = enables normal variable-gain operation
1	AGC2_BYP	Enables the bypass mode of AGC 2 in Data Channel 1: 1 = forces the VGA into a fixed gain of 1 for test purposes 0 = enables normal variable-gain operation
0	AGC1_BYP	Enables the bypass mode of AGC 1 in Data Channel 0: 1 = forces the VGA into a fixed gain of 1 for test purposes 0 = enables normal variable-gain operation

[R25] HIGH PASS FILTER CONTROL A REGISTER

BIT	NAME	DESCRIPTION
7-4	HP2[3:0]	$f_C = f_{CL} \times 10^{HP2/15}$ (KHz) [Data Channel 1] where $0_{dec} \le HP2 \le 15_{dec}$ and f_{CL} frequency is the f_C obtained in HP2=0 Total range = 4.5 to 45 KHz
3-0	HP1[3:0]	$f_C = f_{CL} \times 10^{HP1/15}$ (KHz) [Data Channel 0] where $0_{dec} \le HP1 \le 15_{dec}$ and f_{CL} frequency is the f_C obtained in HP1=0 Total range = 4.5 to 45 KHz

[R26] HIGH PASS FILTER CONTROL B REGISTER

BIT	NAME	DESCRIPTION
7-4	HP4[3:0]	$f_C = f_{CL} \times 10^{HP4/15}$ (KHz) [Data Channel 3] where $0_{dec} \le HP4 \le 15_{dec}$ and f_{CL} frequency is the f_C obtained in HP1=0 Total range = 4.5 to 45 KHz
3-0	HP3[3:0]	$f_C = f_{CL} \times 10^{HP3/15}$ (KHz) [Data Channel 2] where $0_{dec} \le HP3 \le 15_{dec}$ and f_{CL} frequency is the f_C obtained in HP3=0 Total range = 4.5 to 45 KHz

[R27] HIGH PASS FILTER CONTROL C REGISTER

BIT	NAME	DESCRIPTION
7-4	HP6[3:0]	f_C = 4.5 +2.70 x HP6 (KHz) [Servo Channel 1] where $0_{dec} \le HP6 \le 15_{dec}$ Total range = 4.5 to 45 KHz
3-0	HP5[3:0]	f_C = 4.5 +2.70 x HP5 (KHz) [Servo Channel 0] where $0_{dec} \le HP5 \le 15_{dec}$ Total range = 4.5 to 45 KHz

[R28] LOW PASS FILTER1 CUTOFF REGISTER [DATA CHANNEL 0]

BIT	NAME	DESCRIPTION
7	F16M1	Range is 0.96 - 9.4 MHz if LOW 1.92 - 18.8 MHz if HIGH
6-0	FC1[6:0]	-3dB f_C = (D7+1)*0.07335 x FC1 (MHz) where $13_{dec} \le FC1 \le 127_{dec}$

[R29] LOW PASS FILTER2 CUTOFF REGISTER [DATA CHANNEL 1]

BIT	NAME	DESCRIPTION
7	F16M2	Range is 0.96 - 9.4 MHz if LOW 1.92 - 18.8 MHz if HIGH
6-0	FC2[6:0]	-3dB f_C = (D7+1)*0.07335 x FC2 (MHz) where $13_{dec} \le FC2 \le 127_{dec}$

[R30] LOW PASS FILTER3 CUTOFF REGISTER [DATA CHANNEL 2]

BIT	NAME	DESCRIPTION
7	F16M3	Range is 0.96 - 9.4 MHz if LOW 1.92 - 18.8 MHz if HIGH
6-0	FC3[6:0]	-3dB f_C = (D7+1)*0.07335 x FC3 (MHz) where $13_{dec} \le FC3 \le 127_{dec}$

[R31] LOW PASS FILtER4 CUTOFF REGISTER [DATA CHANNEL 3]

BIT	NAME	DESCRIPTION
7	F16M4	Range is 0.96 - 9.4 MHz if LOW 1.92 - 18.8 MHz if HIGH
6-0	FC4[6:0]	-3dB f_C = (D7+1)*0.07335 x FC4 (MHz) where $13_{dec} \le FC4 \le 127_{dec}$

[R32] LOW PASS FILTER5 CUTOFF REGISTER [SERVO CHANNEL 0]

BIT	NAME	DESCRIPTION
7	F16M5	Range is 0.65 – 6.25 MHz if LOW 1.3 – 12.5 MHz if HIGH
6-0	FC5[6:0]	-3dB f_C = (D7+1)*0.0 49213 x FC5 (MHz) where $13_{dec} \leq FC5 \leq 127_{dec}$

[R33] LOW PASS FILTER6 CUTOFF REGISTER [SERVO CHANNEL 1]

BIT	NAME	DESCRIPTION
7	F16M6	Range is 0.65 – 6.25 MHz if LOW 1.3 – 12.5 MHz if HIGH
6-0	FC6[6:0]	-3dB f_C = (D7+1)*0.0 49213 x FC6 (MHz) where $13_{dec} \leq FC6 \leq 127_{dec}$

[R46] FILTER BYPASS REGISTER

BIT	NAME	DESCRIPTION
7	unused	Default =0
6	unused	Default =0
5	FLT6_BYP	Enables the bypass mode of Filter 6 in Servo Channel 1: 1 = forces the filter into a fixed gain of 1 for test purposes 0 = enables normal filter operation
4	FLT5_BYP	Enables the bypass mode of Filter 5 in Servo Channel 0: 1 = forces the filter into a fixed gain of 1 for test purposes 0 = enables normal filter operation
3	FLT4_BYP	Enables the bypass mode of Filter 4 in Data Channel 3: 1 = forces the filter into a fixed gain of 1 for test purposes 0 = enables normal filter operation
2	FLT3_BYP	Enables the bypass mode of Filter 3 in Data Channel 2: 1 = forces the filter into a fixed gain of 1 for test purposes 0 = enables normal filter operation
1	FLT2_BYP	Enables the bypass mode of Filter 2 in Data Channel 1: 1 = forces the filter into a fixed gain of 1 for test purposes 0 = enables normal filter operation
0	FLT1_BYP	Enables the bypass mode of Filter 1 in Data Channel 0: 1 = forces the filter into a fixed gain of 1 for test purposes 0 = enables normal filter operation

[R47] TEST MUX CONTROL A REGISTER

BIT	NAME	DESCRIPTION
7	unused	Default =0
6	unused	Default =0
5-4	TST_MUX3[1:0]	select the signal source for the DPO2p and DPO2n output pins: 00 = High Impedance 01 = Preamp Output 10 = AGC Output 11 = Filter Output
3-2	TST_MUX2[1:0]	select the signal source for the DPO1p and DPO1n output pins: 00 = High Impedance 01 = Preamp Output 10 = AGC Output 11 = Filter Output
1-0	TST_MUX1[1:0]	select the signal source for the DPO0p and DPO0n output pins: 00 = High Impedance 01 = Preamp Output 10 = AGC Output 11 = Filter Output

[R48] TEST MUX CONTROL B REGISTER

BIT	NAME	DESCRIPTION
7	unused	Default =0
6	unused	Default =0
5-4	TST_MUX6[1:0]	select the signal source for the SPObp and SPObn output pins: 00 = High Impedance 01 = Preamp Output 10 = AGC Output 11 = Filter Output
3-2	TST_MUX5[1:0]	select the signal source for the SPOtp and SPOtn output pins: 00 = High Impedance 01 = Preamp Output 10 = AGC Output 11 = Filter Output
1-0	TST_MUX4[1:0]	select the signal source for the DPO3p and DPO3n output pins: 00 = High Impedance 01 = Preamp Output 10 = AGC Output 11 = Filter Output

[R49] WRITE DRIVER 0 CURRENT REGISTER

BIT	NAME	DESCRIPTION
7	WRT_MODE1	sets the write data mode of Driver 0: 1 = enables WDI mode, where the driver toggles state on positive edges 0 = enables WD mode, where driver state follows the input WD0
6-0	WD0[6:0]	Write Current = 0.44 x WD0 (mA) where $0_{dec} \leq WD0 \leq 127_{dec}$ Total range = 0 to 55.9 mA

[R50] WRITE DRIVER 1 CURRENT REGISTER

BIT	NAME	DESCRIPTION
7	WRT_MODE2	sets the write data mode of Driver 1: 1 = enables WDI mode, where the driver toggles state on positive edges 0 = enables WD mode, where driver state follows the input WD1
6-0	WD1[6:0]	Write Current = 0.44 x WD1 (mA) where $0_{dec} \leq WD1 \leq 127_{dec}$ Total range = 0 to 55.9 mA

[R51] WRITE DRIVER 2 CURRENT REGISTER

BIT	NAME	DESCRIPTION
7	WRT_MODE3	sets the write data mode of Driver 2: 1 = enables WDI mode, where the driver toggles state on positive edges 0 = enables WD mode, where driver state follows the input WD0
6-0	WD2[6:0]	Write Current = 0.44 x WD2 (mA) where $0_{dec} \leq WD2 \leq 127_{dec}$ Total range = 0 to 55.9 mA

[R52] WRITE DRIVER 3 CURRENT REGISTER

BIT	NAME	DESCRIPTION
7	WRT_MODE4	sets the write data mode of Driver 3: 1 = enables WDI mode, where the driver toggles state on positive edges 0 = enables WD mode, where driver state follows the input WD3
6-0	WD3[6:0]	Write Current = 0.44 x WD3 (mA) where $0_{dec} \leq WD3 \leq 127_{dec}$ Total range = 0 to 55.9 mA

[R53 – R63] TI TEST REGISTERS

BIT	NAME	DESCRIPTION
7	TI Test Register	DO NOT WRITE TO THIS REGISTER
6	TI Test Register	DO NOT WRITE TO THIS REGISTER
5	TI Test Register	DO NOT WRITE TO THIS REGISTER
4	TI Test Register	DO NOT WRITE TO THIS REGISTER
3	TI Test Register	DO NOT WRITE TO THIS REGISTER
2	TI Test Register	DO NOT WRITE TO THIS REGISTER
1	TI Test Register	DO NOT WRITE TO THIS REGISTER
0	TI Test Register	DO NOT WRITE TO THIS REGISTER

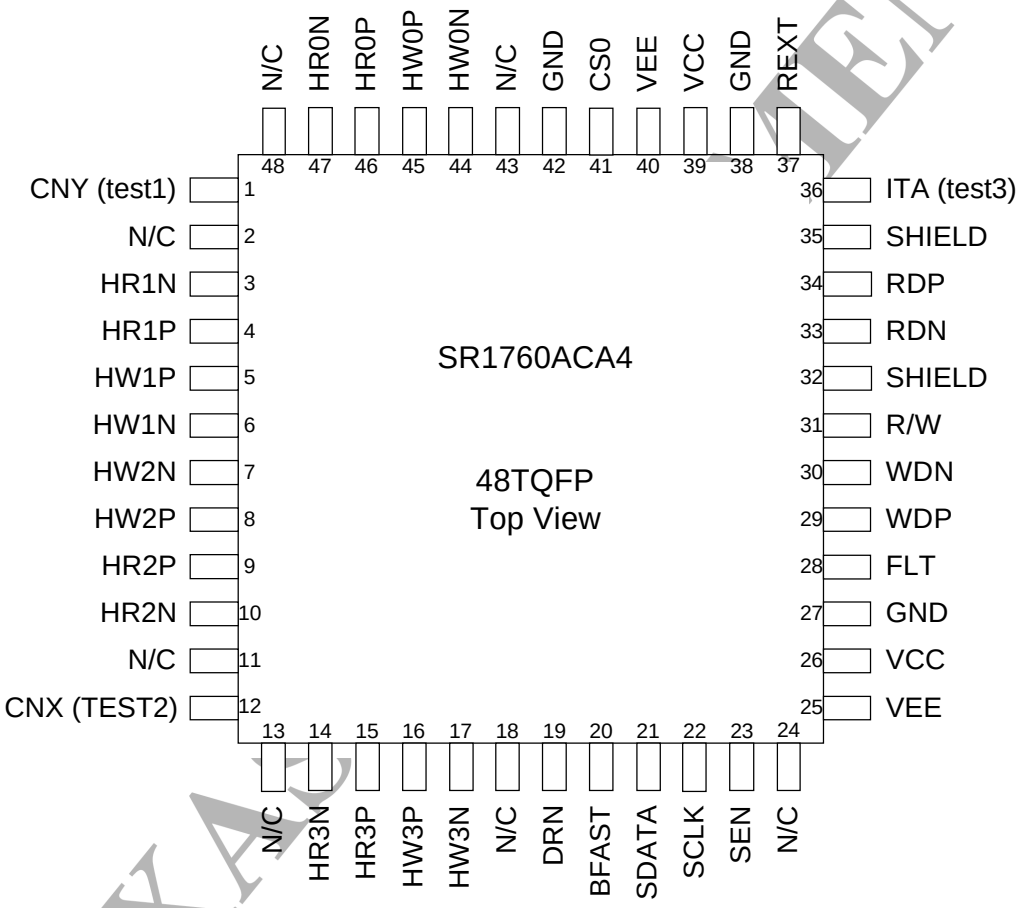
PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RWN	input*	Read/Write: a high level enables the read mode. Internal pull up.
SEN	input*	Serial Enable line. Active High. Internal pull down.
SCLK	input*	Serial Clock line. 40 MHz max.
SDAT	input*	Serial Data line. Bi-directional interface
FLT	output*	Fault active high in write mode, low in read mode. Open collector.
WDP, WDN	input*	Differential PECL or current mode write data inputs
HR0P-HR3P	input	MR head connections, positive end
HR0N-HR3N	input	MR head connections, negative end
HW0P-HW3P	output	Write head connections, positive end
HW0N-HW3N	output	Write head connections, negative end
RDP, RDN	output*	Read Data, Differential read signal outputs
Rext	output	Voltage global reference for the biassing circuits
CS0	input	Chip Select
VEE	input*	-5V supply
GND	input*	Ground
VCC	input*	+5V supply
BFAST	input*	Controls reader passband or enables the Imr generator depending on the state of BFCTL bit from Reg.01. Internal pull down.
DRN	input*	Selects the dummy head or performs a system reset depending on the state of RSTDMY bit from Reg.09. Internal pull up.
CNX, CNY, ITA	Test	TI Test pins. User setting = n/c

* When more than one device is used, these signals can be wire OR'd togetherWDP and WDN should not be wire OR'ed if used in current mode

PACKAGE PIN DESIGNATIONS

(Top View)



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Texas Instruments Storage Products, 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914

SR3443
+5V COIL DRIVER FOR TAPE DRIVERS

Preproduction

May, 2000

FUNCTIONAL DESCRIPTION

The SR3443 is a BiCMOS integrated circuit. It is designed for use in a 2-terminal linear tape data storage device. It contains 2 banks of coil drivers. Each bank has 4 individual drivers that operate simultaneously. One bank is for forward operation and one is for reverse operation. Only one bank can operate at any time.

Write current magnitude can have three states. It can be positive, negative or zero. Positive is defined as WDXn logic high and WDYn logic low. This implies the X side of the head is at a higher voltage than the Y side. Negative is defined as WDXn logic low and WDYn logic high. This implies the Y side of the head is at a higher voltage than the X side. Zero is defined as both WDXn and WDYn logic low. The X and Y sides of the head are at the same voltage and the current in the head is zero.

The magnitude of the write current for the forward and reverse directions can be set independently. This is done by a 3 wire serial port which contains separate registers for forward and reverse. Within each bank, however, all 4 channels are set to the same write current magnitude.

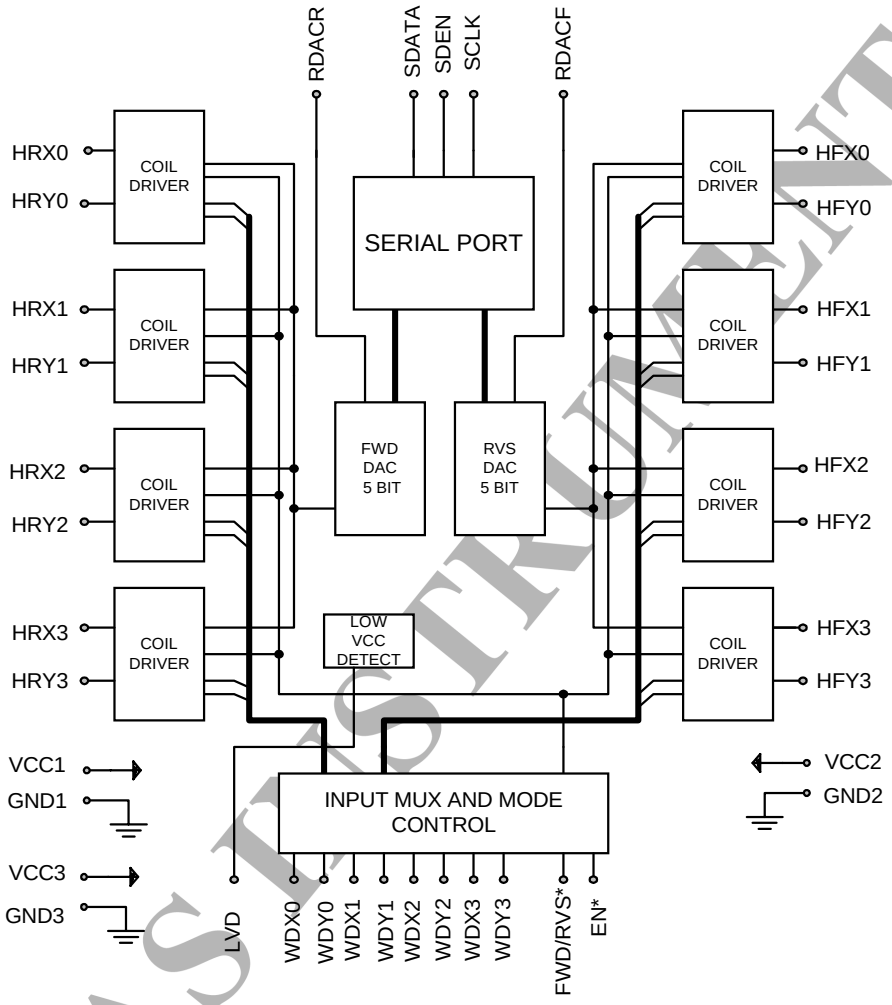
The device has an Enable line ($\overline{EN}$) which shuts down all write drivers when held high.

Also included is a low VCC detect circuit. This circuit has an open collector output.

FEATURES

- **+5 Volt +/- 10% power supply**
- **3 wire serial port for write current programming**
- **Write current range 10 to 50mA adjustable in 1.25mA steps**
- **Rise and fall times 7nS max with a 200nH/14ohm load**
- **1nS max asymmetry**
- **Extremely low coupling from selected to unselected head**

BLOCK DIAGRAM



SERIAL PORT OPERATION

The serial port interface is used to program the part's internal registers. The serial port is enabled for data transfer when the SDEN pin is logic high. SDEN must be asserted high prior to any transmission and it should remain high until the completion of the transfer. SDEN should be set to logic low at the end of each transfer.

When SDEN is high the data presented to the SDATA pin will be latched into the part on each rising edge of SCLK. Rising edges of SCLK should only occur when the desired bit of address or data is being presented on the SDATA line. Serial data transmissions must occur in 16 bit packets. The data is latched into the internal register on the rising edge of SDEN. Figure 2 shows the serial port timing diagram.

Each 16 bit transmission consists of a read/write control bit (write=0) followed by 7 address bits and 8 data bits. The address bits select the internal register to be written. The address and data fields are input LSB first, MSB last where LSB is defined as bit 0. The address bits A1,A2,A3 distinguish between types of devices using the SSI serial port protocol. This part uses 010 for A3,A2,A1 respectively (see serial port register definition table).

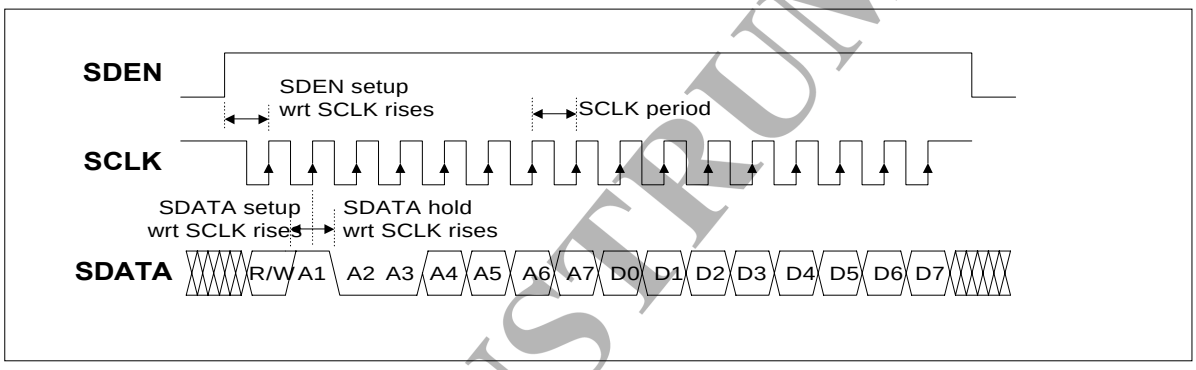


FIGURE 2: Serial Port Timing

The register values at power up and after a serial port reset are indicated below under REGISTER DEFAULT.

		REGISTER ADDRESS								REGISTER DEFAULT							
REG #	**REG NAME**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R0	ID	0	0	0	0	0	1	0	RWB	0	0	0	1	0	0	0	1
R1	IFWD	0	0	0	1	0	1	0	RWB	0	0	0	0	0	0	0	0
R2	IRVS	0	0	1	0	0	1	0	RWB	0	0	1	0	0	0	0	0
R3	RDMP /BST	0	0	1	1	0	1	0	RWB	0	0	0	0	0	0	0	0

DATA REGISTER BIT DEFINITIONS

REGISTER	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IFWD	X	X	X	WCF4	WCF3	WCF2	WCF1	WCF0
IRVS	X	X	$\overline{EN}$	WCR4	WCR3	WCR2	WCR1	WCR0
RDMP/BST	RBST1	RBST0	RDR1	RDR0	FBST1	FBST0	RDF1	RDF0

WCF4 – WCF0 Forward write current DAC bits

WCR4 – WCR0 Reverse write current DAC bits

$\overline{EN}$ Chip enable. This is in addition to the external enable pin. Both enables must be low to activate the chip.

RBST1,0 2 bit control of rise/fall time speed boost for reverse.

RDR1,0 2 bit control of on chip damping resistor for reverse .

FBST1,0 2 bit control of rise/fall time speed boost for forward.

RDF1,0 2 bit control of on chip damping resistor for forward.

PACKAGE PINOUT

TABLE 1: RDAMP CONTROL

RDR1/RDF1	RDR0/RDF0	RDAMP (on chip)
0	0	600
0	1	150
1	0	300
1	1	120

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC1	Power	+5V for forward head section
VCC2	Power	+5V for reverse head section
VCC3	Power	+5V for serial port and data input buffers
GND1	Ground	forward head section ground
GND2	Ground	Reverse head section ground
GND3	Ground	Serial port and data input buffers ground
HFXn,HFYn	O	X,Y forward head connection
HRXn,HRYn	O	X,Y reverse head connection
WDXn,WDYn	I	X,Y input data for forward and reverse
RDACF	Bias	Forward DAC bias resistor
RDACR	Bias	Reverse DAC bias resistor
$\overline{EN}$	I	Chip select: a high inhibits the chip
FWD/$\overline{RVS}$	I	Forward or reverse select: a high selects forward, a low selects reverse
LVD	O	Low voltage detect(open collector output)
SCLK	I	Serial port clock
SDATA	I/O	Serial port data
SDEN	I	Serial port enable

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

Storage Temperature	-65 to +150 deg C
Junction Operating Temperature	135 deg C
Supply Voltage	+6 Volt

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply voltage range		4.5	5.0	5.5	V
Supply current ICC1	active mode IW=50mA FWD RVS		 1 225		 mA mA
Supply current ICC2	active mode IW=50mA FWD RVS		 225 1		 mA mA
Supply current ICC3			3		mA
Total power dissipation	active mode		1.14	1.5	W
Total supply Current	idle mode		2		mA
Total power Dissipation	idle mode		10		mW
Ambient temperature		0		50	C
Package thermal resistance	Mounted, still air junction to ambient			57	deg/W
FWD/$\overline{RVS}$ and $\overline{EN}$ logic input levels Vih Vil Iil Iih		 2.4 0		 VCC .8 -0.4 100	 V V mA uA
SDATA, SCLK, SDEN logic input levels High Low		 VCC-1.0		 1.0	 V V
WDXn, WDYn logic input levels High Low		 2.0		 1.0	 V V
WDXn, WDYn input capacitance				5	pF
Low VCC threshold (note 1)	VCC1, VCC2, VCC3	3.6	3.9	4.2	V
RDACF,RDACR required value			5.77		kohm

NOTE 1: A fault on either VCC1, VCC2, or VCC3 will disable the chip. Normal operation will resume following recovery of a VCC fault.

WRITE CHARACTERISTICS

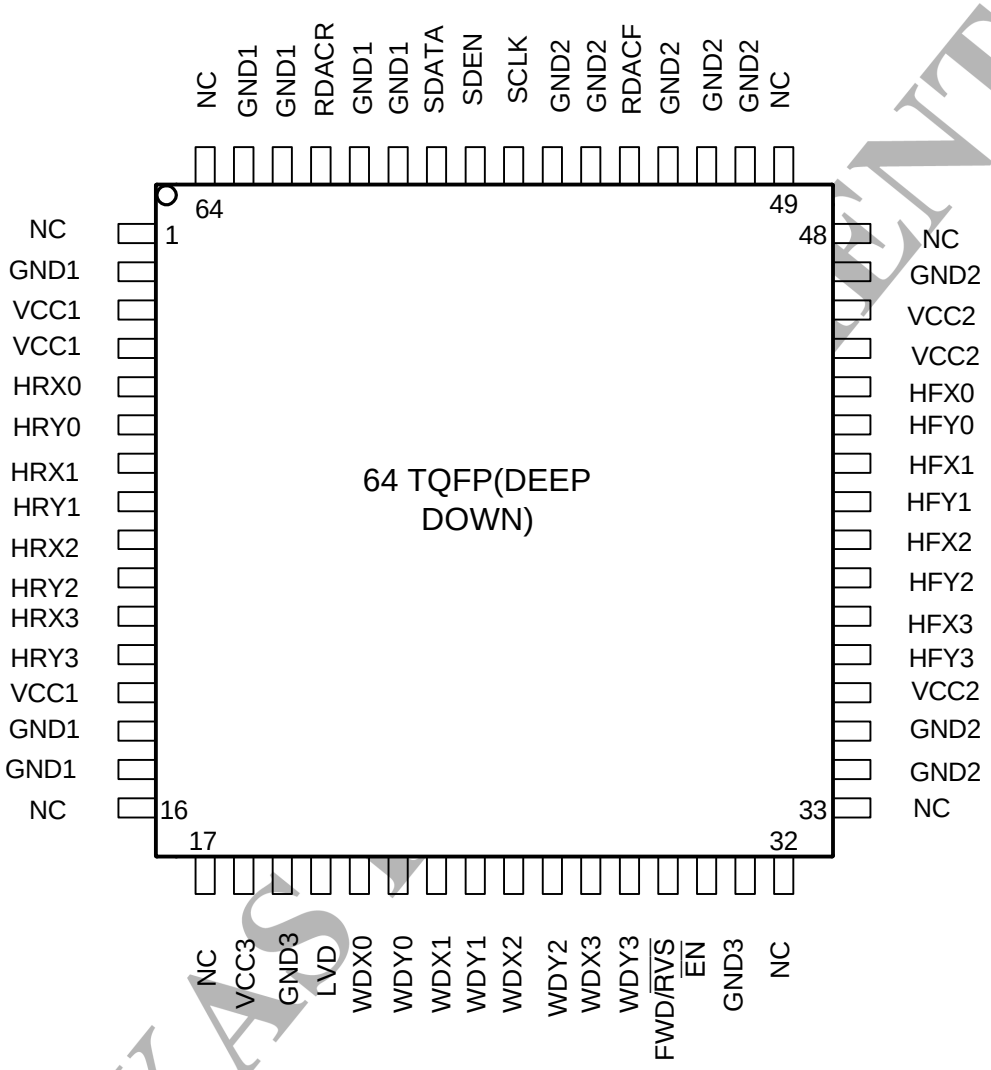
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Head + Flex Inductance		110		200	nH
Head Resistance		8		14	ohm
Head Current Range		10		50	mA
Head Current Accuracy	RDACF/RDACR 1% tol.			+/- 15	%
Head Current Resolution			1.25		mA
Rise and Fall Time				7	nS
Unselected Head Transient Current	peak to peak head load 100 ohm mounted 1cm max from the chip			1	uA
Unselected Head Differential Voltage	same as above			100	uV
Asymmetry	WDXn, WDYn can be 5V or 3.3V			1	nS
Overshoot	percent of peak value Rdamp=TBD IW 40 to 50mA IW 10 to 40mA			 15 TBD	 % %
Minimum Pulse Width		15			nS
Minimum Period		45			nS
WDXn to WDYn overlap				2	nS
Differential Head Voltage Swing	peak to peak	7			V

SERIAL PORT TIMING

PARAMETER	SYMBOL	CONDITION	MIN	NOM	MAX	UNIT
SCLK Clock Period	T_C	Write operation	25			nS
		Read operation	40			nS
SCLK Low Time	T_{CKL}		5			nS
SCLK High Time	T_{CKH}		5			nS
SDEN to SCLK setup time	T_{SENS}		10			nS
SDEN to SCLK hold time	T_{SENH}		10			nS
Data Set-up Time	T_{DS}		5			nS
Data Hold Time	T_{DH}		5			nS
SDEN min. Low Time	T_{SL}		25			nS
SCLK fall to data valid	T_{SDV}	Read operation			17	nS
SDATA hold time	T_{SDH}	Read operation	20			nS
SDEN fall to SDATA tristate	T_{SDTRI}	Read operation			20	nS

PACKAGE PIN DESIGNATIONS

(Top View)



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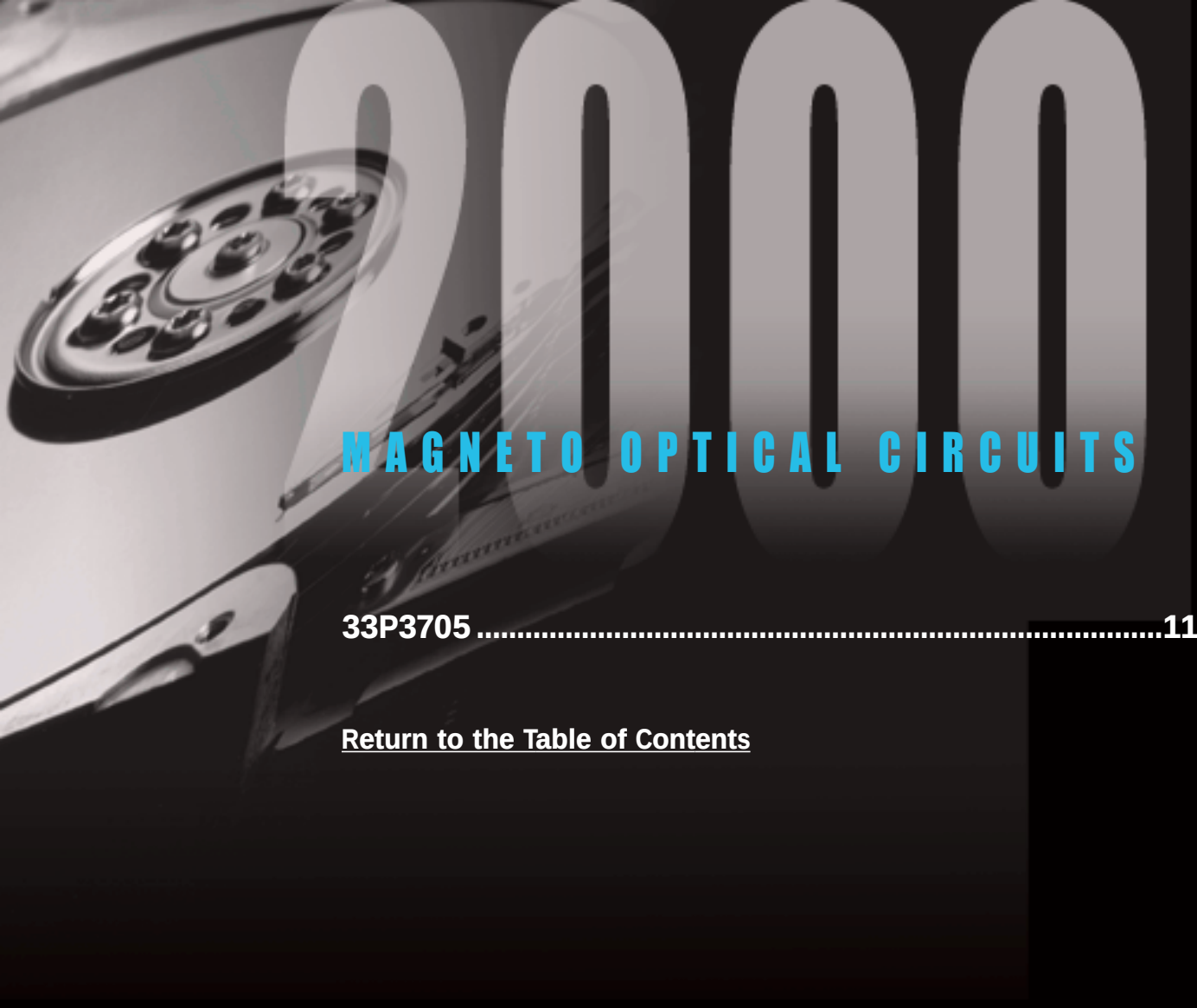

2000

MAGNETO OPTICAL CIRCUITS

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Texas Instruments

Abridged Version

SSI 33P3705

E²PR4ML Read Channel with 1,7 ENDEC, Data Resync Capability

Preproduction

July 1999

DESCRIPTION

The SSI 33P3705 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire E²PR4 1,7 code read channel for zoned recording Magneto-Optical disk drive systems with data rates from 30 to 120 Mbit/s.

Functional blocks include AGC, programmable Filter/Pre-Differentiator, Maximum Likelihood (ML) Detector, 1,7 ENDEC, data synchronizer, time base generator, servo data detector, and data resync logic.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones.

1,7 RLL code operation is used to reduce the magnetic media flux transitions per inch and the write current rise time requirements. The SSI 33P3705 architecture can be extended for use at data rates up to 160 Mbit/s for future applications.

FEATURES

GENERAL

- **Register programmable data rates from 30 to 120 Mbit/s**
- **Sampled data read channel with Maximum Likelihood (ML) Detector**
- **Programmable filter with asymmetrical zeros to compensate pulse asymmetry**
- **PreDifferentiator in signal path accommodates standard Magneto-Optical interface**
- **1,7 RLL ENDEC**
- **Data Scrambler/Descrambler**
- **Low operating power (0.95 W typical at 5 V)**
- **Register programmable power management (<5 mW power down mode)**
- **8 bit NRZ data interface**
- **Serial interface port for access to internal program storage registers**
- **Single power supply (5 V ± 10%)**
- **Small footprint 100-lead TQFP package**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents for data reads**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Automatic AGC fast recovery and input low-z modes with programmable time durations**
- **Programmable input impedance provides for selectable attenuation in data and servo modes**
- **Wide bandwidth, precision full-wave rectifier**
- **Optional internal timing disable and AGC direct control pins: LOWZ, FASTREC, $\overline{\text{HOLD}}$**

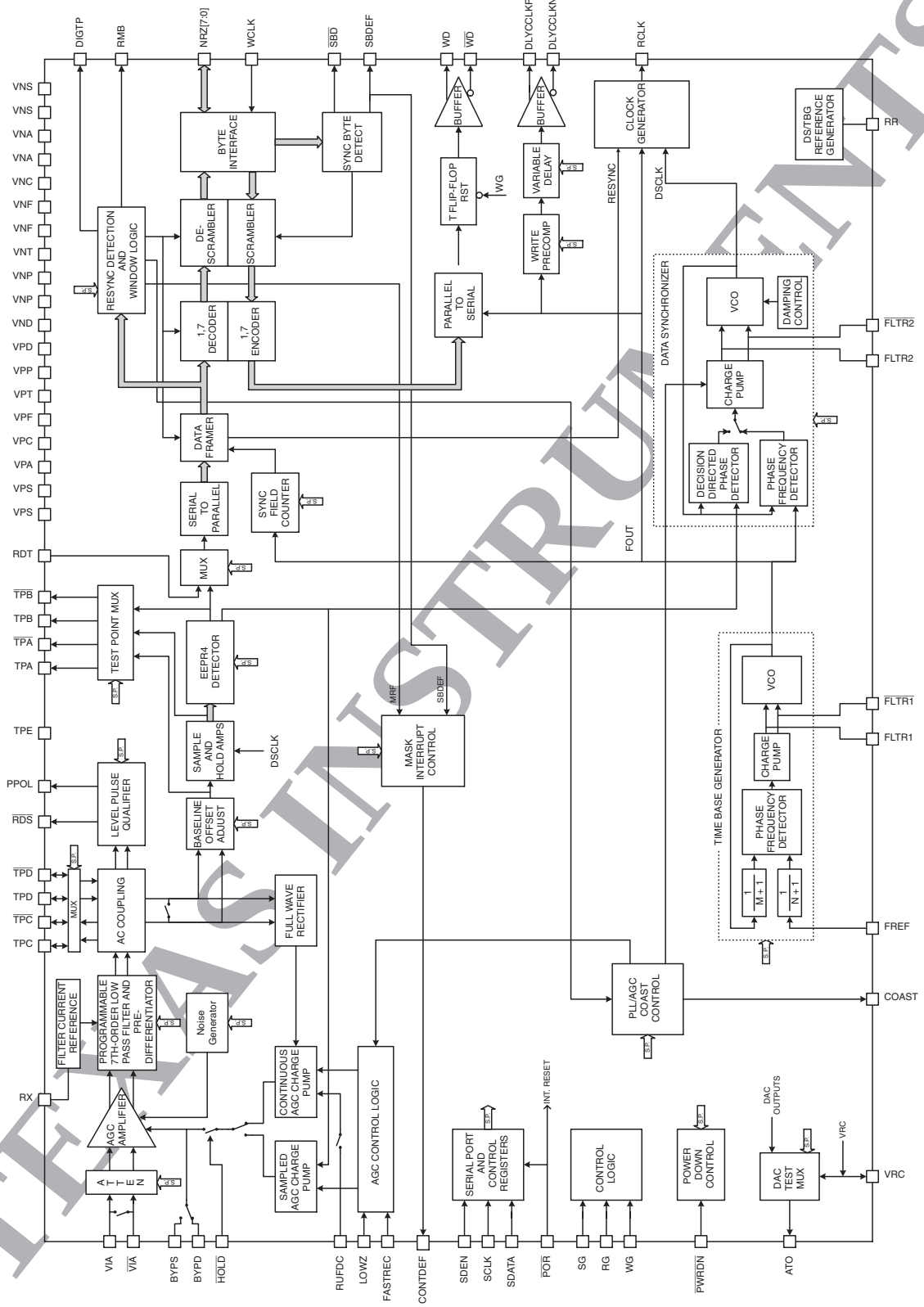
FILTER / PREDIFFERENTIATOR

- **Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:**
  - **Channel filter and pulse slimming equalization for equalization to E²PR4**
  - **Programmable cutoff frequency from 5 to 35 MHz**
  - **Programmable boost /equalization of 0 to 16 dB**
  - **Programmable asymmetrical zeros equalization to correct pulse shape asymmetry**
- **Selectable second-order Differentiator embedded in the Filter provides:**
  - **Conversion of MO interface waveforms to Lorentzian-like signal for E²PR4 equalization**
  - **Constant gain as a function of data rate**
- **Internal AC-coupling with fast offset recovery at Filter outputs**

(continued)

SSI 33P3705
E²PR4ML Read Channel with 1,7 ENDEC, Data Resync Capability

BLOCK DIAGRAM



FEATURES (continued)

PULSE QUALIFICATION

- Sampled Maximum Likelihood data detector with fixed E²PR4 target detection
- With white gaussian noise, within 0.5 dB of ideal Viterbi detector at user density of 2.0
- Register programmable qualification thresholds for servo reads
- Selectable hysteresis or window qualification modes for servo reads

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 180 MHz frequency output
- Independent M and N divide-by registers

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 1,7 RLL ENDEC
- Register programmable to 120 Mbit/s operation
- Fast acquisition, zero phase restart, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 8-bit NRZ data interface
- Differential PECL programmable-delay code clock outputs for laser driver
- Programmable write precompensation of code clock for non-linear transition shift
- Differential PECL write data outputs with power reduction
- Programmable sync byte detection
- Programmable offset to compensate for signal asymmetry

DATA RESYNC LOGIC

- Inserts one-byte resync pattern into every 15 bytes of user data in write mode
- Flags missing resyncs on readback for defect detection
- Defect location registers facilitate data recovery by Controller
- Defect recovery mode provided for loss of sync byte
- Programmable Controller Interrupt output for defect detection and recovery
- Programmable AGC / PLL coast mode to minimize defect-induced disturbances

FUNCTIONAL DESCRIPTION

The SSI 33P3705 implements a complete high performance E²PR4 read channel for magneto-optical disk drive systems, that supports data rates up to 120 Mbit/s. Functional blocks include an AGC, programmable Filter/Pre-Differentiator, sequence detector, time base generator, data separator with 1,7 ENDEC and scrambler/descrambler, and data resync logic.

A serial port is provided to write control data to the internal program storage registers.

AGC CIRCUIT DESCRIPTION

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input to the sampled data processor while the input from the Read/Write preamplifier varies. The circuit consists of an AGC loop that includes an AGC amplifier, charge pump, programmable continuous time filter, and a precise, wide band, full wave rectifier. Depending upon whether the read is of a servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to common mode noise. The AGC can be programmed for either direct or timed AGC control modes.

The behavior of the AGC circuit, prior to the sampled AGC mode, is controlled by the LOWZ, FASTREC, $\overline{\text{HOLD}}$, and RUFDC pins, the Timed AGC Mode Register bit, and the Low_Z, and fast recovery mode timers. The timers are programmable by the Time Control (TC) Register and count the periods of the TBG

AGC CIRCUIT DESCRIPTION (continued)

reference frequency (FREF). A resistor connected between the RUFDC pin and the positive supply provides additional decay current during the fast recovery (ultra fast recovery) period. An OpenZ mode of operation is also provided and may be invoked during the LOWZ time period, which will squelch the input signal completely by opening the VIA/$\overline{\text{VIA}}$ input signal lines.

The AGC circuit is limited to a maximum gain of 128 V/V to avoid transient recovery issues due to offsets.

LOW_Z, FAST RECOVERY, HOLD AND NORMAL PERIODS

During the Low-Z period, the AGC amplifier input resistance is reduced to allow quick recovery of the AGC amplifier input ac-coupling capacitors. This mode is activated for a programmable time period during and after a write operation, and after intial power up. It is also activated for a fixed time period after each transition of the SG input. Two Low-Z to Normal-Z ratios (i.e. time constants) are available with the use of the LZTCR Register bit. The input resistance can be reduced by a 15:1 or 5:1 ratio by setting the LZTCR bit = 0 or 1, respectively. If the OpenZ mode is enabled (N Register bit 7 = 1), the input signal present at the VIA/$\overline{\text{VIA}}$ inputs will be squelched completely during the Low-Z time period. In general, invoking OpenZ will improve transient recovery at SG or WG transitions, except during powerup when it is desirable to deassert OpenZ.

In the fast recovery period, the attack and decay currents are increased to allow faster recovery of the proper AGC level. During this period the ultra fast recovery may be effected with the aid of an external resistor connected between the positive supply and the RUFDC pin to pull up the voltage on the bypass capacitor. This will allow an extremely rapid increase of AGC amplifier gain. This mode shuts itself off when the signal at DP/DN reaches the 125% point. By adjusting the value of this resistor, the user can easily control the amount of gain change that can be accomplished during any Fast Recovery period. If the RUFDC pin is left open, then the ultra fast recovery mode is in effect disabled.

During the hold period, the AGC gain is held constant subject only to leakage currents at the BYP pins. The value of the capacitors placed at these pins should be selected to give adequate droop performance when in hold mode as well as to insure the stability of the AGC loop when not in hold mode. This mode is automatically asserted at the end of the Fast Recovery period in servo mode. The Fast Recovery period should be adjusted so that the AGC has time to settle to a 100% value before going into a hold mode.

During the normal period (i.e., the period other than Low_Z, fast recovery or hold prior to VCO lock), the normal attack and decay currents are used to maintain a constant signal level at the qualifier inputs.

AGC OPERATION IN SERVO MODE

During servo reads, the AGC loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (CBYPS) which is referenced to VPA. The dual rate charge pump drives CBYPS with currents that force the differential peak to peak voltage at DP/DN to a programmed peak to peak voltage. Attack currents lower the voltage at BYPS, which reduces the amplifier gain. Decay currents raise the voltage at BYPS, which increases the amplifier gain. The sensitivity of the amplifier gain to changes in the BYPS voltage is about 38 dB/V. When the voltage at BYPS is equal to VRC, the gain from AGC input to DP/DN will be about 24.9 dB. The charge pump is continuously driven by the instantaneous voltage at DP/DN. When the signal at DP/DN is greater than 100% of the programmed AGC level, the normal attack current (Ia) of 340 μA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, the fast attack current (Iaf) of 2.86 mA is used to reduce the gain very quickly. This dual rate approach allows the AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A normal decay current (Id) of 20 μA acts to increase the amplifier gain when the signal at DP/DN is less than 100% of the programmed AGC level. The large ratio (340 μA:20 μA) of the normal attack and normal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. This implies that the AGC loop will not be able to quickly increase its gain if required to do so. A fast recovery mode is provided to allow the AGC gain to be rapidly increased in order to reduce the recovery time between mode switches. In the fast recovery mode, the decay current is increased by a

factor of 8 to 160 µA (Idfr) and the attack current is increased by a factor of 4.18 to 1.42 mA (Iafr). This has the effect of speeding up the AGC loop by a factor somewhere between 4 and 8 times.

As shown in Figure 1, the fast recovery period should be asserted just after the Low-Z period that follows each transition of SG (servo gate). The AGC response is determined by the external capacitance and Idfr. For example, if CBYPS is 500 pF and FASTREC is asserted for 0.5 µs in servo mode, the voltage at BYPS can increase at most by 0.5 µs • 160 µA/500 pF = 160 mV, which will allow the gain to increase by 6 dB in that time. If FASTREC is asserted for 0.5 µs in non-servo mode and CBYPD is 1000 pF, then the voltage at BYPS can increase at most by 0.5 µs • 160 µA/1000 pF = 80 mV, which will allow the gain to increase by 3 dB in that time. A fast offset null time period (Tfosn) is also invoked when LOWZ is asserted to allow quick recovery of offsets at the Filter outputs. It is recommended that Low_Z period be asserted for 0.5 µs just prior to any assertion of the fast recovery period in order to quickly null out any internal DC offsets.

AGC OPERATION IN WRITE MODE

During a write operation the AGC loop is placed in a hold mode so that the CBYPD and CBYPS capacitors will retain the values obtained during the previous read or servo operation. As shown in Figure 2, the Low-Z mode should be invoked so that the Low-Z time occurs during and immediately following WG. The Open-Z mode may also be selected if so desired to provide additional squelching of the input signal. In addition, the Fast Recovery mode should be activated just after the Low-Z time period to enable fast recovery to the proper AGC level.

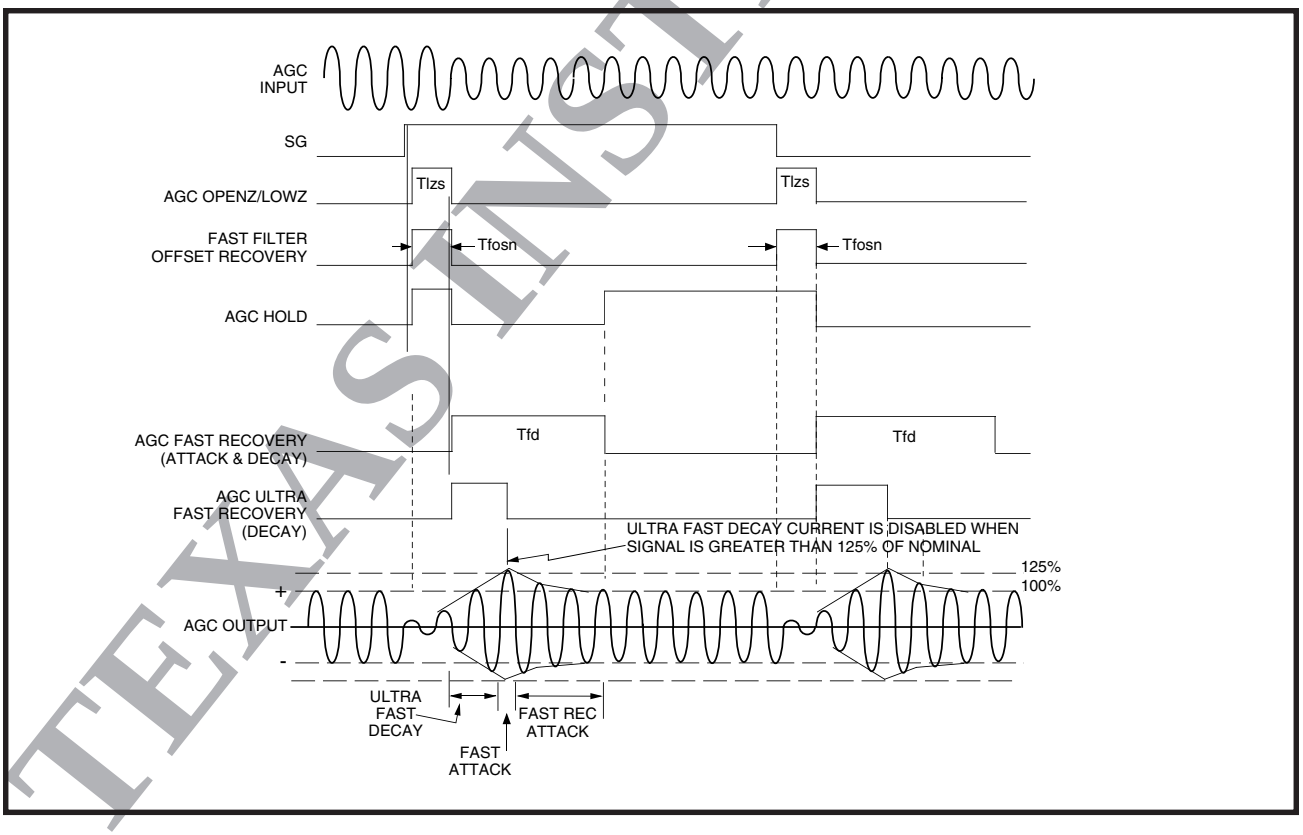


FIGURE 1: AGC Internal Timing Diagram for Servo Mode

FUNCTIONAL DESCRIPTION (continued)

AGC OPERATION IN DATA READ MODE

For data reads, the loop described above is used for one-half (or all) of the programmed sync field count during the VCO preamble except that the CBYPD hold capacitor is used instead of CBYPS. After 1/2 SFC (or SFC), the AGC loop is switched to include the AGC amplifier with a sampled charge pump, to more accurately control the signal amplitude into the Data Sequence Detector. In this sampled AGC mode, a symmetrical attack and decay charge pump is used. The "3" sample amplitudes are sampled, held, and compared to a threshold to generate the error current. With a 2T pattern, certain "2" samples are compensated and used for AGC. The maximum charge pump current value can be programmed with the SDVT[7:6] Register bits to 0, 20, 40, or 60 µA. This current will be proportional to the Data Rate register value.

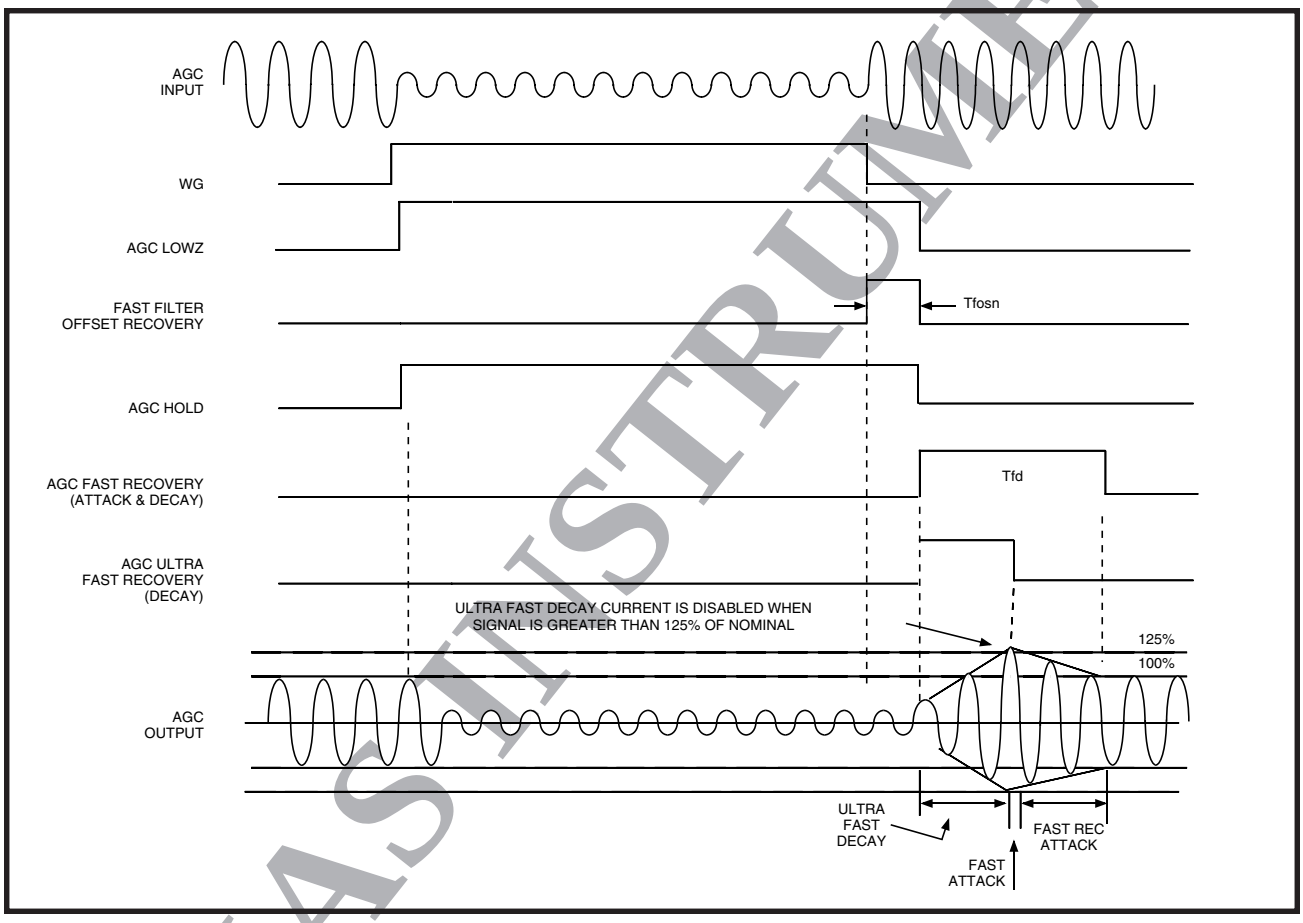


FIGURE 2: AGC Internal Timing Diagram for Write Mode

EXTERNAL AGC CONTROL MODE

For maximum application flexibility, all AGC modes may be externally controlled. By setting bit TAM = 0 (MC1[3]), the internal timing controls for Low-Z, fast recovery and hold modes will be disabled so that the modes may be completely controlled by the AGC control pins. When the internal timing controls are enabled, the AGC control pins, when enabled, will override the internal timings. When the LOW-Z input is high, Low-Z mode is activated. In the Low-Z mode, the AGC amplifier input resistance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. The ratio of Low-Z to non-Low-Z resistance can be selected as either 15:1 or 5:1 by programming the LZTCR bit in the NG Register. During Low-Z mode, the time constant of the internal AC coupling networks at the filter outputs are also reduced by the ratio

determined by the LZTCR bit. This time constant is 300 ns/630 ns in Low-Z mode, and 2.3 µs/ 7 µs when not in Low-Z mode, for LZTCR = 1/0, respectively. This mode should be activated during and for a short time after a write operation. It should also be activated for a short time after each transition of the SG input and on initial power up.

When the $\overline{\text{HOLD}}$ input is low, the charge pumps for the AGC control are disabled. This de-activates the AGC loop. The AGC amplifier gain will be held constant at a level set by the voltage at the BYPD or BYPS pins. The value of the capacitor placed at these pins should be selected to give adequate droop performance when in hold mode as well as to insure stability of the AGC loop when it is not in hold mode.

The signal provided to the FASTREC input pin determines if the AGC is in fast recovery mode. During the fast recovery mode (FASTREC = 1), the attack and decay currents are increased to allow faster recovery to the proper AGC level. If faster recovery than is provided by FASTREC alone is desired, and ultra fast recovery can be effected by connecting a resistor between the RUFDC pin and the positive supply. If this resistor is present, whenever fast recovery is entered, the voltage on the BYPD or BYPS capacitor will be pulled up. This causes an extremely rapid increase in the AGC amplifier gain. The ultra fast current will be disabled the first time that the signal at DP/DN reaches the 125% point. The fast recovery attack and decay currents are used as long as the FASTREC pin is held high.

INTERNALLY-TIMED AGC CONTROL MODE

When the internally timed AGC control mode is selected by setting bit TAM = 1 (MC1[3]), the external control inputs LOWZ, FASTREC, and $\overline{\text{HOLD}}$, are not used and must be deasserted. The equivalent signals are generated internal to the SSI 33P3705. These internal signals are generated by counters that are triggered by various conditions of WG, SG and $\overline{\text{PWRDN}}$ inputs, and clocked by the FREF reference input clock. The fast recovery mode immediately follows the end of each Low-Z mode. The counter timings for the Low-Z (Tlz) and fast recovery (Tfr) signals are set by the Time Control Register. The counter timing for the Low-Z following SG transitions (Tlzs) can be programmed with the LZSG register bit to one of two possible values. When LZSG = 0, the Low-Z time period will be equal to 10 cycles of the FREF reference. When LZSG = 1, the time period will be equal to 16 cycles of the FREF clock. The current for the ultra fast decay mode is set by the resistor connected between the RUFDC input pin and VPA. In timed AGC control mode, the LOWZ, FASTREC, and $\overline{\text{HOLD}}$ input pins are logically or'ed with the respective internal control signals but do not affect the internal sequencing of the counter generated AGC control signals.

PULSE QUALIFICATION CIRCUIT DESCRIPTION

This device utilizes two different types of pulse qualification, both of which may be used for servo reads while one is used exclusively for data reads.

Servo Read Mode

The Qualifier can operate in one of two modes- the window qualifier mode, or the polarity check mode. Both modes can be used with either a single qualification threshold, or dual thresholds which can be used to detect adjacent half-amplitude pulses. Unless otherwise specified, assume that SG is High and the Read Data Polarity bit (FC[7]) is Low, and the RDE bit (MC1[2]) is Low for discussions below. The Qualifier is only meant to detect Servo data. It's output does not interface with the read data detector, only to the external $\overline{\text{RDS}}$ pin.

The qualifier has a baseline shift feature which allows the differential baseline of the DP/DN undifferentiated signal input to be shifted positive or negative in linear steps based on the 4 register bits SBO[3:0]. This baseline shift works for both Qualifier modes.

Window Qualifier Mode

(Pulse Qualifier Mode bit FB[7] = L)

In the window Qualifier mode, a positive and negative threshold (Vth+; Vth-, same magnitude for both, set via 6 bit DAC by register SDVT) is compared against incoming undifferentiated waveform DP/DN. The DP/DN signal as well as its differentiated version CP/CN are both internally coupled to the Qualifier from the Filter, with internal DC offset nulling circuits. See the single ended behavioral block diagram in Figure 3 and corresponding timing diagram of Figure 4. If the signal exceeds the Vth threshold in either polarity, the differentiated version of this signal (CP/CN), whose differential zero crossing coincides with the peak of DP/DN is allowed to clock out a pulse, through the zero cross comparator, at the $\overline{\text{RDS}}$ output (whose pulse width is conditioned by the Nonretriggerable One Shot and asserted low) meaning that the DP/DN signal pulse

WINDOW QUALIFIER MODE (continued)

is a valid pulse rather than a noise excursion. If two or more threshold qualified pulses are detected within the output pulse width of the Nonretriggerable One Shot, only the first is pulsed out. If the DP/DN signal was not greater than the threshold, it is assumed that the pulse is just noise so it should not clock out a pulse at $\overline{RDS}$. Also a PPOL CMOS output will indicate the polarity of the most recent DP/DN signal pulse. It is high when the pulse is positive (PPOL transitions at the peak of the pulse) and low when the pulse is negative.

Polarity Check Mode

(Pulse Qualifier Mode bit FB[7] = H)

In the polarity check mode, the normal window qualifier mode detected pulses, as described above, are further polarity discriminated so that if two or more consecutive amplitude threshold qualified pulses of the same polarity occur, only the first will be allowed to be pulsed out at the $\overline{RDS}$ output pin.

Dual Threshold Mode

The dual threshold mode is enabled by setting register bit MRL2[7] = 1, and can be used in conjunction with the Window, Polarity, and Cluster Polarity modes of servo pulse detection. In addition to the normal Vth threshold, an upper VFATH (full amplitude) threshold and a lower V HATH (half-amplitude) threshold are provided for amplitude qualification. As shown in Figure 6, the servo pulses are initially qualified by the Vth threshold set by the SDVT[5:0] register bits. All pulses whose amplitude exceeds the Vth threshold will be detected. If the detected pulse amplitude exceeds Vth but does not exceed the upper VFATH threshold set by the FATH[3:0] register bits, the pulse is considered to be a half-amplitude pulse. If such a pulse is qualified, the nominal threshold Vth will be temporarily dropped to a lower threshold VHATH set by the HATH[3:0] register bits. The threshold drop occurs at the peak of the detected pulse so that a subsequent half-amplitude pulse can be more easily detected. The lower threshold will be maintained until another pulse exceeding the upper VFATH threshold is detected, after which the VHATH threshold will be reset to the nominal Vth value, the switch occurring at the peak of the pulse. These threshold levels and qualification criteria apply to positive as well as negative pulses.

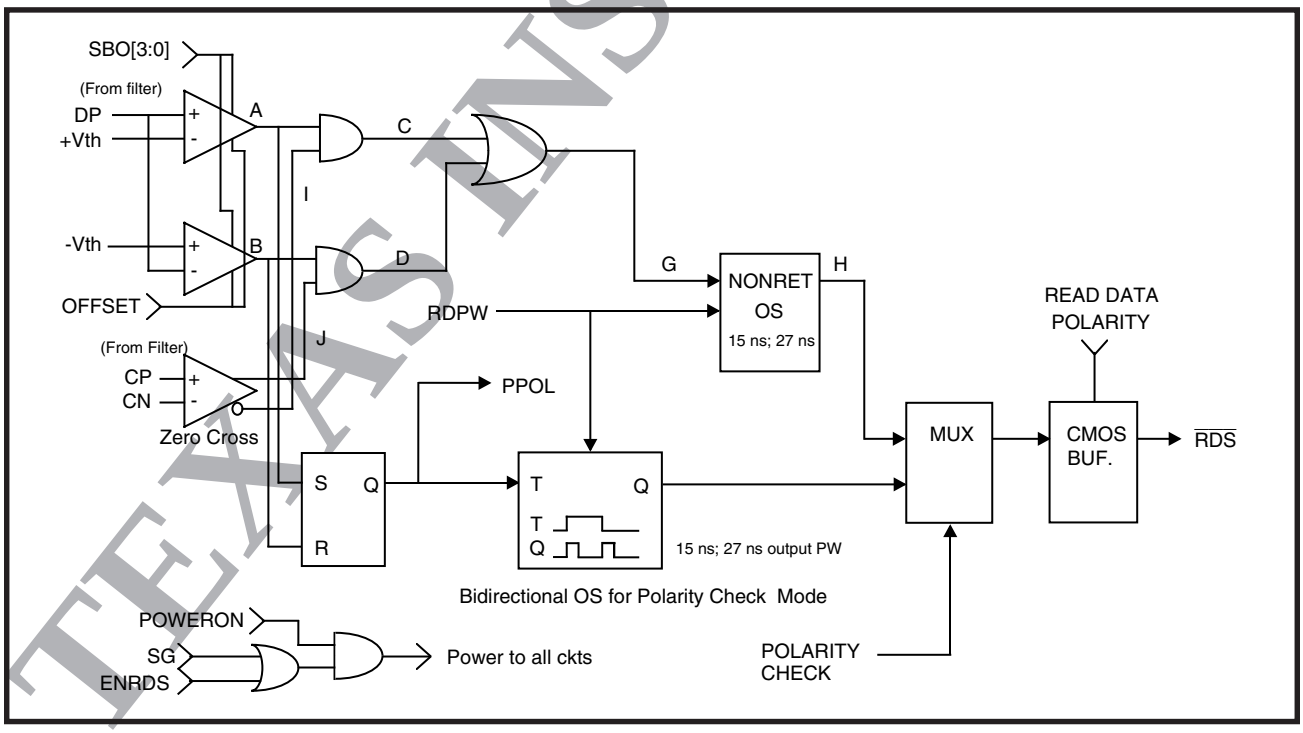


FIGURE 3: Qualifier Block Diagram

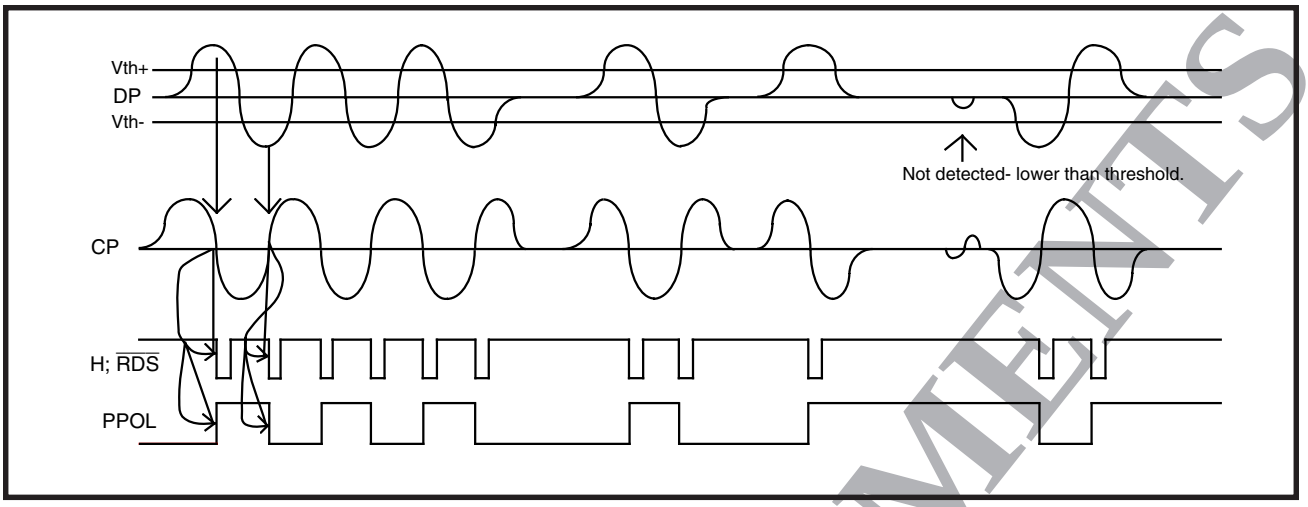


FIGURE 4: Window Qualifier Signals

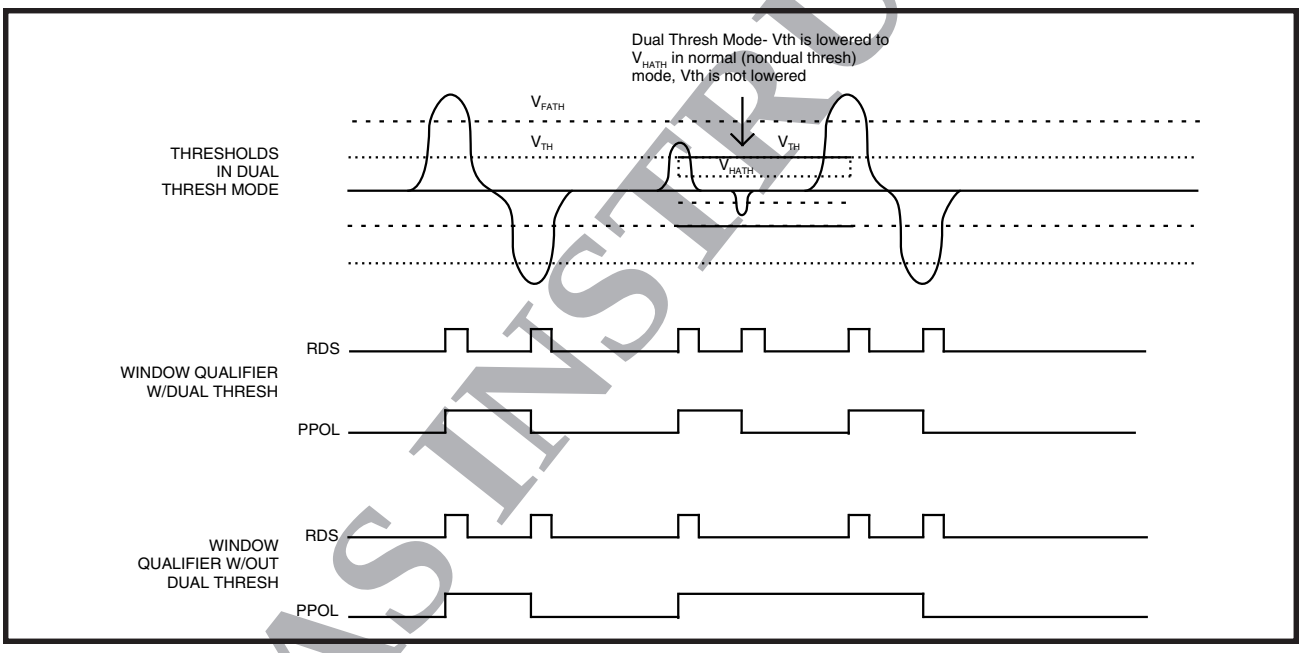


FIGURE 5: Dual Threshold Qualifier Signals

Data Read Mode

In data read mode (RG high), the TBG is used to determine the VCO sync field duration as set by the SFC bits in the SC Register. The $\overline{RDS}$ and the PPOL outputs of the level qualifier are not active in data read mode.

Sampled look-ahead with decision feedback is used to determine the data sequence. Decision feedback is incorporated by using the state of the 4 previous detected bits to set the thresholds of the sequence detector. In the range of operating user densities (UD = 1.75 to 2.25), the detector approaches the performance of a Viterbi detector without its complexity and large latency time. The target is fixed but to allow margin testing, the absolute value of the detector thresholds is programmable from the DVT Register. A programmable base line offset controlled by the DBO Register bits is included to compensate for signal amplitude asymmetry. The detector's low latency time

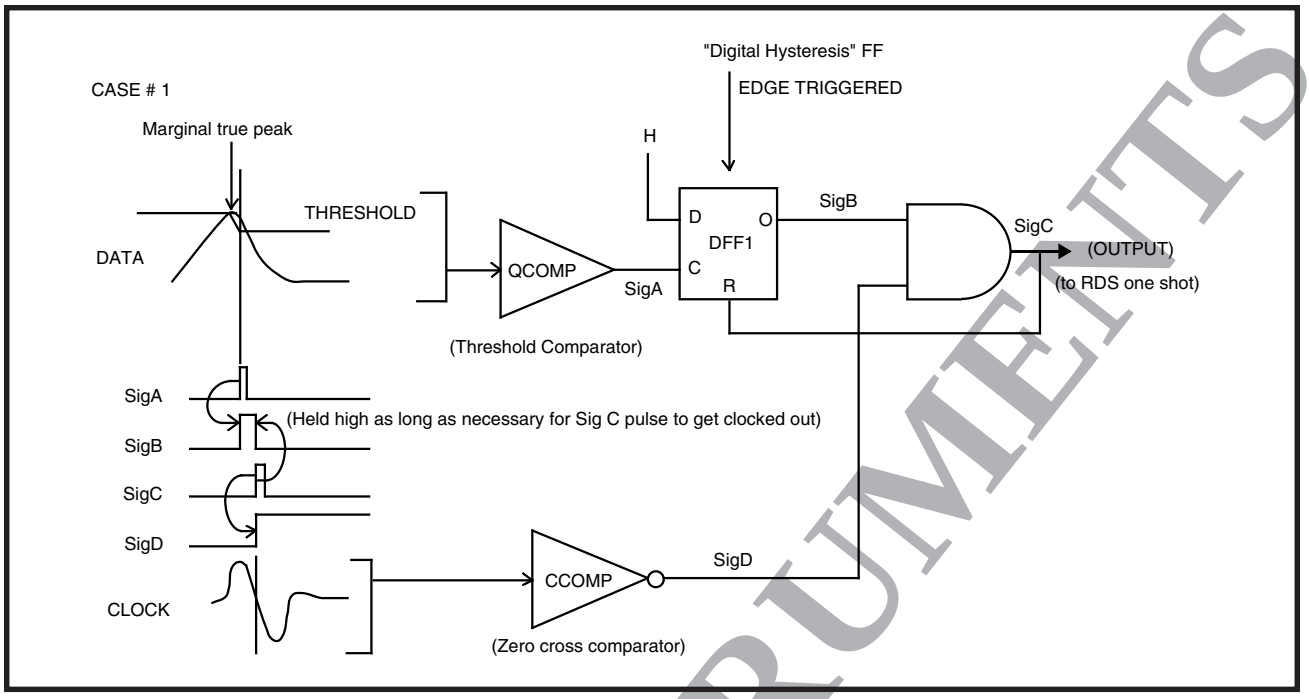


FIGURE 6: Digital Hysteresis Architecture

DATA READ MODE (continued)

allows it to be used for timing recovery during the data read mode.

Common Controls For All Qualifier Modes

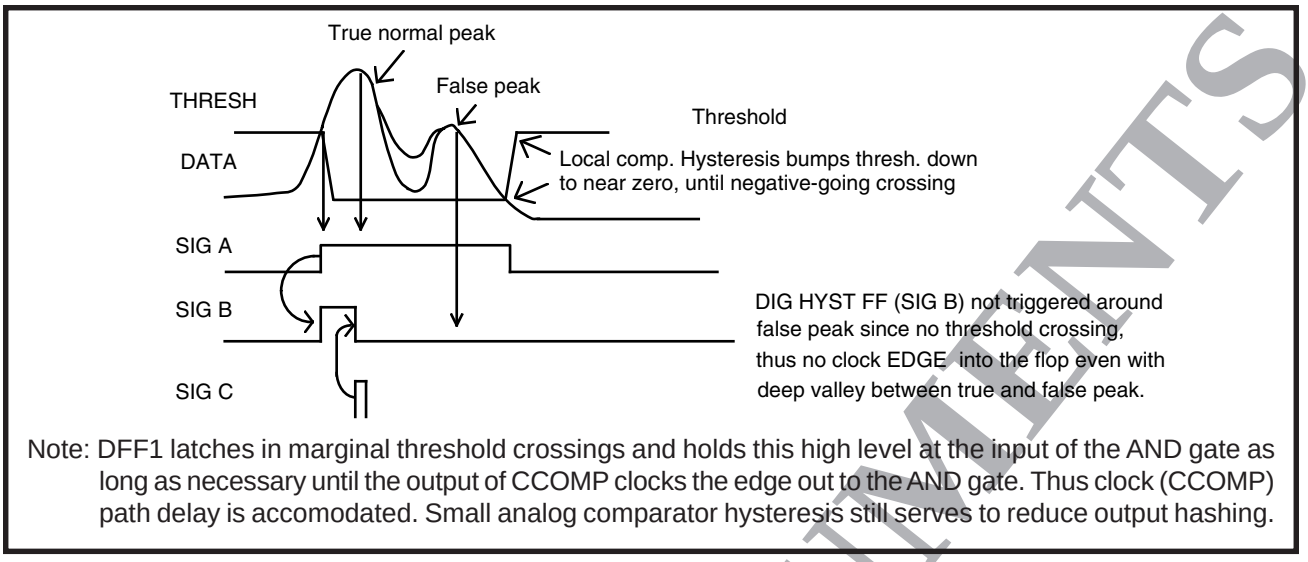
In all modes, the RDPW (Read Data Pulse Width) Register bit (Bit 0 of TC Register) controls the output pulse width duration from the Nonretriggerable One Shot. RDPW = High sets the $\overline{RDS}$ pulse width to 25 ns, and RDPW = Low sets $\overline{RDS}$ to 50 ns.

When SG = L, the Qualifier is powered down automatically to conserve power and reduce noise generation. When the RDE bit (MC1[2]) is High, the $\overline{RDS}$ output and the entire Qualifier will be enabled and powered up whether or not SG is asserted (unless the entire chip is in the sleep mode). If Low, the Qualifier and $\overline{RDS}$ output will be powered off automatically when SG is deasserted. In addition, if the $\overline{RDS}$ output is not needed it can be disabled at all times with the use of register bits DISRDS, to reduce unnecessary noise injection.

If the Read Data Polarity bit (FC[7]) is High, the $\overline{RDS}$ pulse output is asserted High and the reverse is true when Read Data Polarity is Low.

Digital Hysteresis (Used with Window Qualifier Mode)

The window qualifier mode normally implements Digital Hysteresis architecture shown in Figure 6 when the LTH bit (MC1[1]) is set Low. It allows marginal qualifier threshold crossings to be logically held indefinitely until the clock comparator's output switches at the zero crossing of the differentiated signal. A small amount of Local Analog Comparator Hysteresis is also implemented to reduce noise hashing of the comparator at marginal threshold crossings. Local Analog Comparator Hysteresis by itself can be used for this threshold crossing extension purpose as well to hold the comparator output high longer during marginal crossings, but it has the disadvantage that it disturbs the threshold (effectively lowering it after an initial crossing) and can therefore cause false peaks to be detected more easily possibly causing errors. The Digital Hysteresis can be used together with local analog comparator hysteresis since it negates the false double pulse detection side effect of Local Analog Comparator Hysteresis by itself, but maintains the local Analog Hysteresis' secondary advantage of reducing comparator noise hashing at marginal threshold crossings. This general ability to suppress double pulse detection is demonstrated in its extreme form in



Note: DFF1 latches in marginal threshold crossings and holds this high level at the input of the AND gate as long as necessary until the output of CCOMP clocks the edge out to the AND gate. Thus clock (CCOMP) path delay is accomodated. Small analog comparator hysteresis still serves to reduce output hashing.

FIGURE 7: Cluster Polarity Check Mode Timing

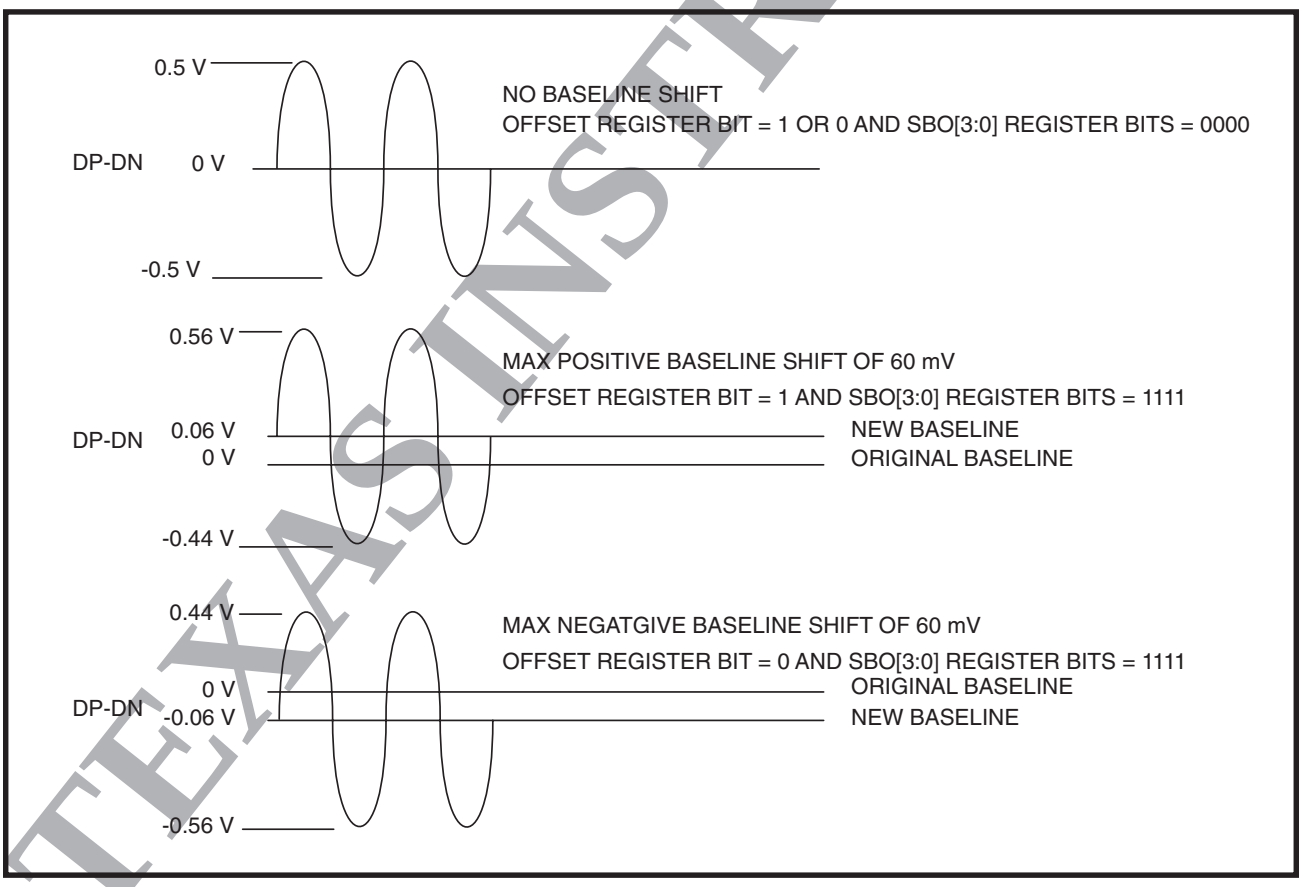


FIGURE 8: Baseline Offset

DIGITAL HYSTERESIS (continued)

Figure 7 in the following discussion of the new cluster polarity check mode which implements Digital Hysteresis with a register selected Large Local Analog Comparator Hysteresis (by setting the LTH bit High).

The Digital Hysteresis architecture is not used with the normal polarity check mode but small Analog Local Comparator Hysteresis by itself is still used with these modes to aid marginal threshold crossings somewhat as well as reduce noise hashing.

Cluster Polarity Check Mode

(PQM bit FB[7] = L; LTH bit MC1[1] = H)

The cluster polarity check mode is the normal window Qualifier Mode with Digital Hysteresis PLUS ADDITIONAL LARGE local analog comparator hysteresis. The large comparator hysteresis effectively lowers the threshold suddenly to near zero when the signal crosses positively through the threshold, and restores the threshold suddenly when signal crosses the threshold back down. See Figure 7. It will permit

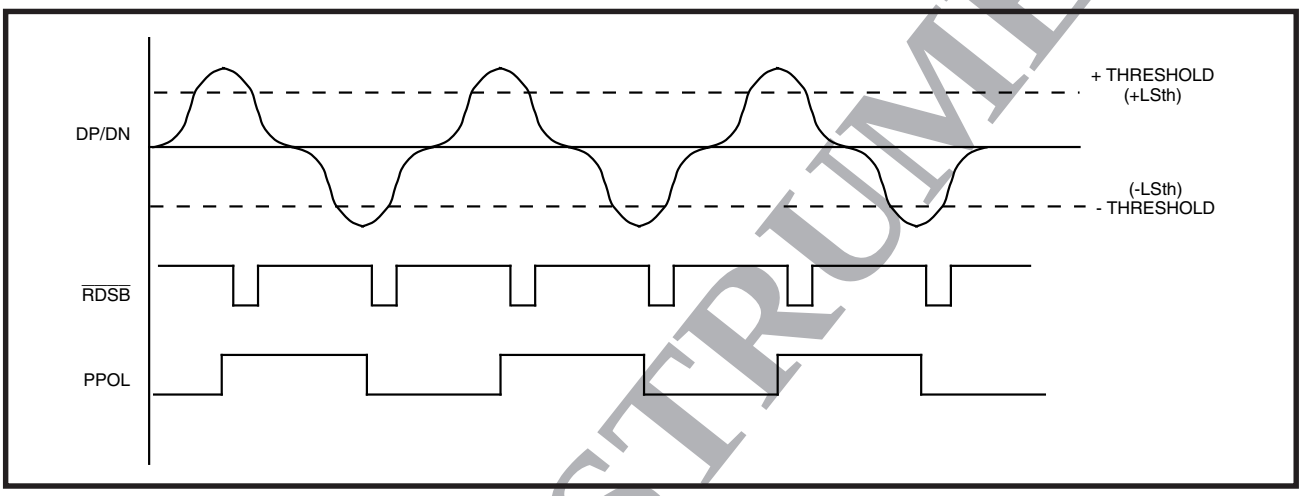


FIGURE 9: RDS and PPOL Relationship to DP/DN

only the first threshold qualified peak in a local cluster of large same polarity peaks to be detected. However, after the cluster of peaks is gone, the Qualifier does not have any memory of the cluster related events and allows subsequent amplitude qualified peaks to be detected of either polarity. Thus it does not have the error propagation effect of conventional polarity check mode where if a valid peak is missed due to a defect reducing its amplitude, the next valid peak of opposite polarity is masked . This new cluster polarity check mode does not discriminate between 2 amplitude qualified peaks if they are separated enough such that the first peak returns to zero baseline prior to the start of the second peak (whereas the conventional polarity check mode does) but in many systems the majority of same polarity peaks occur in clusters where a large false peak is "riding" on the skirt of a valid one, in which case the cluster polarity check mode will only detect the first large peak, and discriminate out the rest.

Baseline Offset

Differential baseline offset can be applied to the DP/DN signal input of the Qualifier prior to threshold qualification. The magnitude of this baseline shift is controlled by the SBO bits in the BLO Register for the servo mode qualifier and the DBO bits for the read mode qualifier. The polarity of this shift is controlled by the BOSP bit in the DVT Register. The shift is positive when the BOSP = 1. This works in all qualifier modes, prior to application of the amplitude threshold qualification. The magnitude of the baseline offset is 4 • SBO (mV).

The purpose of baseline shift is to compensate for positive/negative amplitude asymmetry of the DP-DN differential signal. However, the Filter output itself is not shifted, only the inputs to the Qualifier following the Filter. Thus the servo baseline shift is not observable at the Filter TPC output pins, but is observable at the detector input test points on TPA and TPB.

The baseline shift is not applied to the DP/DN in the conventional AGC feedback path, so the AGC always regulates the amplitude of unshifted signal. The Differential Baseline Offset can also be applied to the input to the Sequence Detector for read mode operation. The magnitude of this baseline shift is controlled by the DBO [3:0] Register bits in the BLO Register.

Servo Timing Outputs

The servo mode qualifier that was previously described is used to generate the $\overline{RDS}$ and PPOL timing signals. The $\overline{RDS}$ output pin pulses low for each positive or negative servo peak that is qualified by the dual level qualifier. The PPOL output pin provides the pulse polarity information for the qualified peaks, where PPOL = 1 for a positive peak and PPOL = 0 for a negative peak. To reduce noise propagation, the $\overline{RDS}$ and PPOL outputs are only active in servo mode. PPOL is guaranteed to precede $\overline{RDS}$ by at least 2.5 ns.

PROGRAMMABLE FILTER / PRE-DIFFERENTIATOR CIRCUIT DESCRIPTION

The on-chip, continuous time, low pass filter has register programmable cutoff and boost settings, and provides both normal and differentiated outputs. It is a 7th order filter that provides a 0.05° phase equiripple response. Embedded within the filter signal path is a separate second-order pre-differentiator, which can be selectively enabled or disabled by the user through the serial port. The Pre-Differentiator allows the traditional flux pattern signal of a Magneto-Optical interface to be input directly into the SSI 33P3705 Read channel and produces the derivative of the signal to convert the flux transition waveforms into Lorentzian-like pulses for equalization by the EEPR4 detector. Henceforth, the filter and pre-differentiator will be discussed separately below. The total channel response is now defined as the product of both the filter and pre-differentiator sections, described by the total channel peak frequency - Fpk, as noted in the pre-differentiator and total channel response section below.

Filter Description

The programmable filter is a 7th order filter that provides a 0.05° phase equiripple response, with a group delay that is relatively constant up to twice the cutoff frequency. For pulse slimming, two zero programmable boost equalization is provided with no degradation to the group delay performance. Both the boost and the filter cutoff frequency for data and servo reads are programmed through internal 7-bit DACs in the FC, FCS, FB and SRV Registers. The nominal boost range at the cutoff frequency is 0 to 16 dB for data reads and is controlled by the FB Register. In servo mode, the boost can be programmed in 2 dB steps from 0 to 6 dB by setting the FBS bits in the SRV Register. The cutoff frequency, Fc, is variable from 5 to 35 MHz and controlled by the FC Register in data mode or the FCS Register in servo mode. The cutoff and boost values for servo reads are automatically switched when servo mode is entered.

The filter zeros can be adjusted asymmetrically about zero to compensate for signal slope asymmetry. The asymmetry can be equalized by changing the group delay of the filter with the FGD bits of the FGD Register. The group delay can be varied up to 30% with 5 bits of resolution with the FGD[4:0] Register bits. The sign of the group delay can be set either positive or negative with the FGDS bit. The group delay of the filter may also be varied in the servo mode, although with less resolution. This control is provided with the SGDE[1:0] bits of the SRV Register, where the group delay can be varied up to 15% in steps of 5%. The sign of the group delay in the servo mode can be changed with

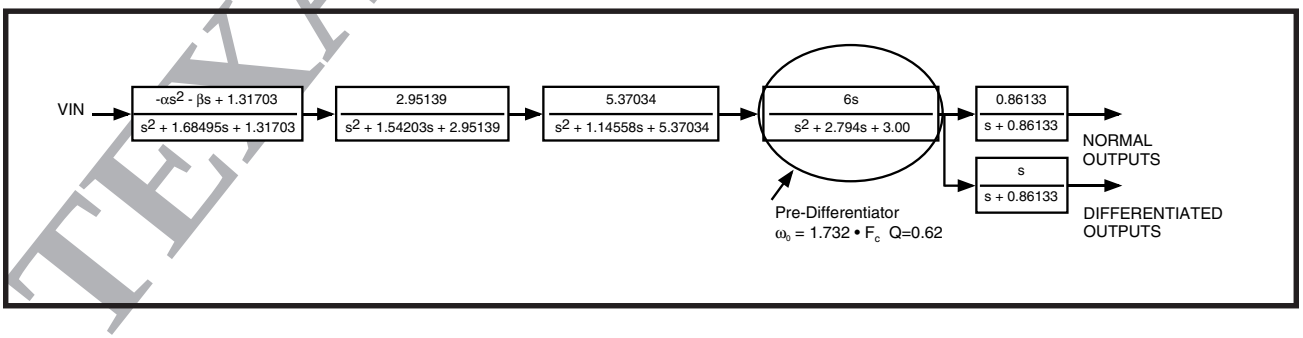


FIGURE 10: Filter Transfer Function

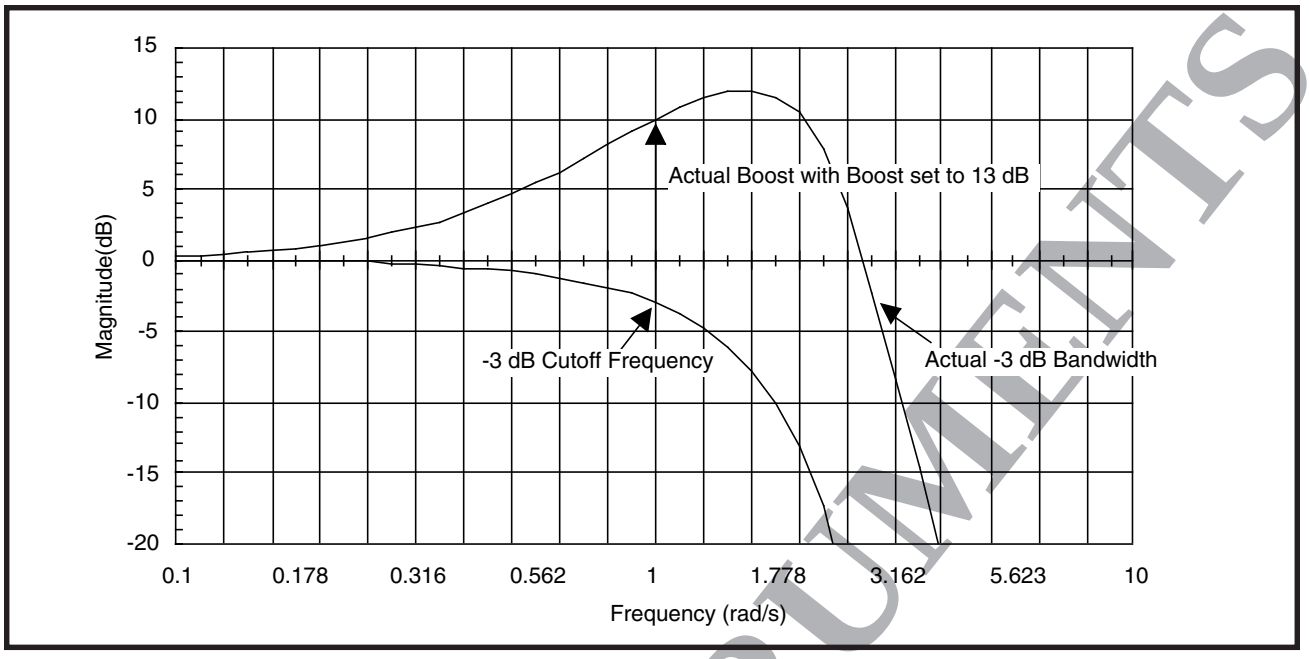


FIGURE 11: Filter Magnitude Response (Δ% = 0)

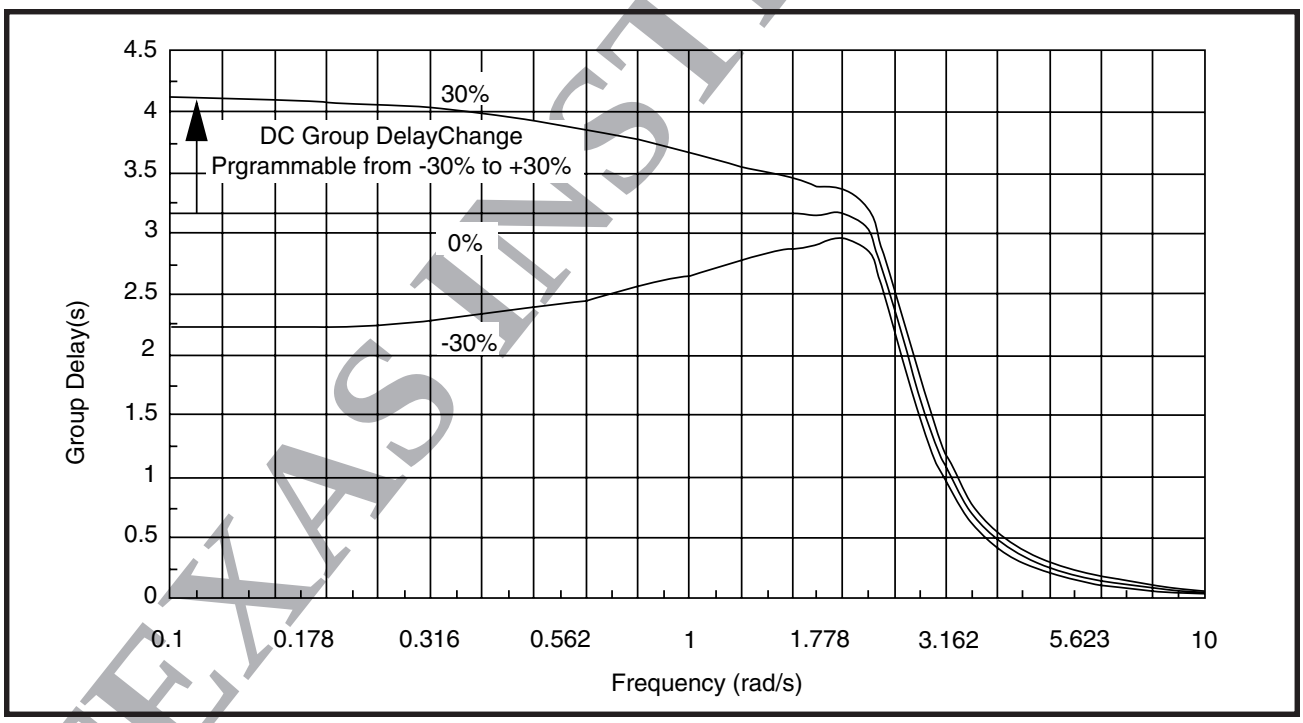


FIGURE 12: Filter Group Delay Response (Boost = 0 dB)

TABLE 1: Filter Magnitude Response

FREQ.	MAG(dB)							
(RAD/S)	BST = 0dB	1dB	3dB	5dB	7dB	9dB	11dB	13dB
0.0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.1	-0.03	-0.02	0.00	0.04	0.08	0.13	0.19	0.26
0.2	-0.13	-0.08	0.02	0.14	0.30	0.48	0.72	1.00
0.3	-0.28	-0.18	0.04	0.31	0.64	1.04	1.52	2.08
0.4	-0.49	-0.32	0.07	0.53	1.09	1.73	2.49	3.35
0.5	-0.75	-0.49	0.10	0.80	1.60	2.51	3.53	4.67
0.6	-1.07	-0.70	0.13	1.08	2.13	3.31	4.59	5.97
0.7	-1.45	-0.95	0.15	1.35	2.67	4.08	5.59	7.17
0.8	-1.90	-1.25	0.13	1.61	3.17	4.80	6.50	8.25
0.9	-2.42	-1.60	0.08	1.82	3.61	5.44	7.30	9.19
1.0	-3.01	-2.01	-0.01	1.99	3.99	5.99	7.99	9.99
2.0	-13.14	-9.68	-4.67	-0.85	2.36	5.22	7.84	10.31
3.0	-35.67	-29.24	-22.21	-17.61	-13.98	-10.88	-8.09	-5.52

TABLE 2: Filter Group Delay Response/Boost = 0 dB

FREQ.	DELAY(SEC)						
(RAD/S)	-30%	-20%	-10%	0%	10%	20%	30%
0	-2.22	-2.54	-2.86	-3.18	-3.49	-3.81	-4.13
0.1	-2.23	-2.54	-2.86	-3.17	-3.49	-3.81	-4.12
0.2	-2.25	-2.54	-2.85	-3.17	-3.48	-3.79	-4.09
0.3	-2.28	-2.55	-2.85	-3.16	-3.48	-3.78	4.04
0.4	-2.33	-2.57	-2.85	-3.16	-3.47	-3.76	-3.99
0.5	-2.39	-2.59	-2.86	-3.17	-3.47	-3.74	-3.94
0.6	-2.45	-2.62	-2.86	-3.17	-3.48	-3.73	-3.89
0.7	-2.52	-2.65	-2.87	-3.18	-3.48	-3.71	-3.84
0.8	-2.57	-2.67	-2.88	-3.18	-3.47	-3.68	-3.78
0.9	-2.62	-2.69	-2.88	-3.17	-3.46	-3.65	-3.72
1	-2.67	-2.71	-2.88	-3.17	-3.45	3.62	-3.66
2	-2.98	-2.94	-2.95	-3.18	-3.41	-3.42	-3.39
3	-1.16	-1.13	-1.1	-1.27	-1.43	-1.41	-1.37

FILTER DESCRIPTION (continued)

the SFGDS bit of the SRV Register.

The normal low pass filter is a seven-pole two-real-zero type. Figure 10 illustrates the transfer function normalized to 1 rad/s. The response can be denormalized to the cutoff frequency of Fc (Hz) by replacing s by $s/2\pi Fc$, while the boost and group delay equalization are controlled by varying the α and β.

With a zero at the origin, the filter also provides a time-differentiated filter output. This is used in time qualification of the servo pulse qualifier. To ease the timing requirement of the qualifier for a signal slightly

FILTER DESCRIPTION (continued)

above the threshold, the time-differentiated output is purposely delayed by 1.2 ns relative to the normal low pass output. The normal low pass output feeds

that data qualifier (DP/DN) and the differentiated output feeds the clock comparator (CP/CN) of the servo qualifier.

Shown also are theoretical magnitude response at no boost and 15 dB boost with $\Delta\% = 0$, and group delay response at $\Delta\% = -30$, 0, and 30 with no boost. To denormalize the response to Fc multiply frequency by $2\pi Fc$, and divide the group delay response by $2\pi Fc$. For example if Fc = 30 MHz, multiply frequency axis by $1.885 \bullet 10^8$ for rad/s conversion or by $30 \bullet 10^6$ for Hz conversion. For the group delay divide the delay numbers by $1.885 \bullet 10^8$. The delay of 3.18 s translates to 16.87 ns

Five definitions are introduced for the filter control discussion:

Cutoff Frequency:

The cutoff frequency is the -3 dB low pass bandwidth with no boost and group delay equalization, i.e., $\alpha = 0$ and $\beta = 0$.

Actual Boost:

The amount of peaking in magnitude response at the cutoff frequency due to $\alpha \neq 0$ and/ or $\beta \neq 0$.

Alpha Boost:

The amount of peaking in magnitude response at the cutoff frequency due to $\alpha \neq 0$ and without group delay equalization. In general, the actual boost with group delay equalization is higher than the alpha boost. However, with 3 dB alpha boost, the difference is minimal. Alpha and the boost in dB are related by:

$$\alpha = 1.3713 \bullet (10^{dB/20} - 1)$$

Group Delay Δ%:

The group delay $\Delta\%$ is the percentage change in absolute group delay at DC with respect to that without equalization applied ($\beta = 0$). Beta and $\Delta\%$ are related by:

$$\beta = 0.04183 \bullet \Delta\%.$$

Group Delay Variation:

The group delay variation is the change in group delay from DC to the cutoff frequency. This can be expressed as a percentage defined as: (change in group delay divided by the absolute group delay with $\beta = 0$) • 100%.

Filter Operation

Direct coupled differential signals from the AGC amplifier output are applied to the filter. The programmable bandwidth and equalization characteristics of the filter are controlled by 3 internal DACs. The registers for these DACs (FC, FB and FGD) are programmed through the serial port. The current reference for the DACs is set using a single external resistor connected from pin RX (15.8 K, 1%) to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. This establishes excellent temperature stability for the filter characteristics.

The cutoff frequency can be set independently in the servo mode and the data mode. In the data mode, the cutoff frequency is controlled by the FC Register. In the servo mode, the cutoff frequency is controlled by the FCS Register.

Cutoff Control (Filter Only)

The programmable cutoff frequency from 5 to 35 MHz is set by the 7 bit linear FC DAC. The filter cutoff is set by the FC Register in non-servo mode and is set by the FCS Register in servo mode. The cutoff frequency is set as:

$$Fc(MHz) = 1.0525 + 0.2753 \bullet FC.$$

The filter cutoff frequency (Fc) is defined as the -3 dB bandwidth with no boost applied. When boost/ equalization is applied, the actual -3 dB point will move up. The ratio of actual -3 dB bandwidth to the programmed cutoff is tabulated in Table 3 as a function of applied boost at the normalized frequency of 1.0 rad/s. Note: Due to the pre-differentiator function now present in the filter signal path, the term Fpk will be used to describe the cutoff frequency of the total system. See the pre-differentiator and total system response section.

TABLE 3: Ratio of Actual -3 dB Bandwidth to Cutoff Frequency

ALPHA BOOST	GROUP DELAY						
	0%	±5%	±10%	±15%	±20%	±25%	±30%
0 (dB)	1.00	1.01	1.06	1.16	1.31	1.47	1.62
1	1.19	1.21	1.28	1.38	1.50	1.62	1.74
2	1.49	1.51	1.56	1.63	1.71	1.79	1.87
3	1.79	1.80	1.83	1.87	1.91	1.96	2.01
4	2.03	2.04	2.05	2.07	2.09	2.11	2.14
5	2.20	2.20	2.21	2.22	2.23	2.24	2.25
6	2.32	2.32	2.33	2.33	2.34	2.34	2.35
7	2.42	2.42	2.42	2.43	2.43	2.44	2.44
8	2.51	2.51	2.51	2.51	2.51	2.52	2.52
9	2.59	2.59	2.59	2.59	2.59	2.59	2.59
10	2.66	2.66	2.66	2.66	2.66	2.66	2.67
11	2.73	2.73	2.73	2.73	2.73	2.73	2.73
12	2.80	2.80	2.80	2.80	2.80	2.80	2.80
13	2.86	2.86	2.86	2.86	2.86	2.87	2.87
14	2.93	2.93	2.93	2.93	2.93	2.93	2.93
15	3.00	3.00	3.00	3.00	3.00	3.00	3.00
16	3.06	3.06	3.06	3.06	3.06	3.06	3.06

PROGRAMMABLE FILTER / PRE-DIFFERENTIATOR CIRCUIT DESCRIPTION
(continued)

Boost Control

The programmable alpha boost from 0 to 16 dB is set by the 7-bit linear FB DAC in data mode or 2-bit linear FBS DAC in servo mode. The alpha boost in data mode is set as:

Boost(dB) = 20 • log[0.000045 • FC • FB + 0.04927 • FC + 1].

In servo mode, the FBS bits in the SRV Register controls the boost as :

Boost(dB) = FBS • 2.0. That is boost in the servo mode can be changed in 2 dB steps from 0 to 6 dB.

The programmed alpha boost is the magnitude gain at the cutoff frequency with no group delay equalization. When finite group delay equalization is applied, the actual boost is higher than programmed alpha boost. However, the difference becomes negligible when the programmed alpha boost is 3 dB. Table 4 below tabulates the actual boost at $\omega = 1.0$ as function of the applied alpha boost & group delay equalization.

TABLE 4: Actual Boost vs. Alpha Boost & Group Delay Change at ω = 1.0 rad/s

ALPHA BOOST	GROUP DELAY						
	0%	±5%	±10%	±15%	±20%	±25%	±30%
0 (dB)	0.00	0.11	0.42	0.89	1.47	2.12	2.81
1	1.00	1.09	1.33	1.72	2.21	2.76	3.36
2	2.00	2.07	2.27	2.58	2.99	3.45	3.97
3	3.00	3.05	3.21	3.47	3.80	4.19	4.63
4	4.00	4.04	4.17	4.38	4.65	4.97	5.34
5	5.00	5.03	5.14	5.30	5.52	5.79	6.10
6	6.00	6.03	6.11	6.24	6.42	6.64	6.89
7	7.00	7.02	7.09	7.19	7.34	7.51	7.72
8	8.00	8.02	8.07	8.15	8.27	8.41	8.58
9	9.00	9.01	9.05	9.12	9.22	9.33	9.47
10	10.0	10.0	10.0	10.1	10.2	10.3	10.4
11	11.0	11.0	11.0	11.1	11.1	11.2	11.3
12	12.0	12.0	12.0	12.1	12.1	12.2	12.2
13	13.0	13.0	13.0	13.1	13.1	13.1	13.2

Group Delay Equalization (Filter Only)

The group delay Δ% can be programmed between -30% to +30% by the 5-bit linear FGD DAC. The FGD register holds the 5-bit FGD DAC control value. The group delay Δ% is set as:

Group Delay Δ% = 0.9677 • (FGD4:0) • 100%
$0 \leq FGD \leq 31$, where FGDS = sign of FGD (0 = neg, 1 = pos)

The group delay Δ% is defined to be the percentage change of the absolute group delay due to equalization from the absolute group delay without equalization at DC. Note that Δ% is not dependent on alpha setting; the group delay variation is. In servo mode the group delay Δ% can be programmed between -15% and +15% in steps of 5% with the SGDE[1:0] register bits located in the SRV Register. The sign of the group delay magnitude is controlled by the SFGDS bit located in the SRV Register.

Pre-Differentiator and Total System Response

The pre-differentiator is a second-order active differentiator whose transfer function is shown along with the filter in Figure 10.

The Pre-Differentiator can be selectively enabled or disabled (bypassed) by the user with the ENDPRE and ENSPRE register bits in the serial port. When ENDPRE (MC2[5]) = 1, the Pre-Differentiator will be enabled in the read and idle modes of operation. When ENDPRE = 0, the Pre-Differentiator is bypassed. Similarly, if ENSPRE (SRV[7]) = 1, the Pre-Differentiator will be enabled in the servo mode, and bypassed otherwise.

The second-order poles of the denominator are described by an $\omega_0 = 1.73 \bullet Fc$, with the Q = 0.62. A single zero is located in the numerator. The ω_0 of the poles as well as the gain at any particular frequency scales with the Fc of the filter, so that the overall gain of the pre-differentiator remains constant as a function of data rate, when the Fc setting is adjusted proportionally. The magnitude and group delay of the pre-differentiator is shown in Figures 13 and 14, respectively, when the filter Fc (excluding the pre-differentiator) is set for 1 rad/s. These figures show the relative bandwidth of the pre-differentiator as compared to the filter's response, as previously shown in Figures 11 and 12. Not shown in Figure 10 is a gain stage (A_V = 2) immediately following the pre-differentiator. This circuit is unconnected at the present date, however, can be connected as a metal-mask option should its use be required for improved channel performance.

The total channel response of the filter and the pre-differentiator is shown in Figures 15 and 16, for the respective magnitude and group delay responses. Again, the Fc is set for 1 rad/s for the filter section. The total channel peak frequency Fpk for the normal outputs is the frequency at which the total channel magnitude is a maximum, when the filter boost is set to zero. Fpk corresponds to, and is closely related to the Fc of the filter without the pre-differentiator. When boost equalization is applied, the actual -3 dB point of the filter will move up along with the magnitude of the

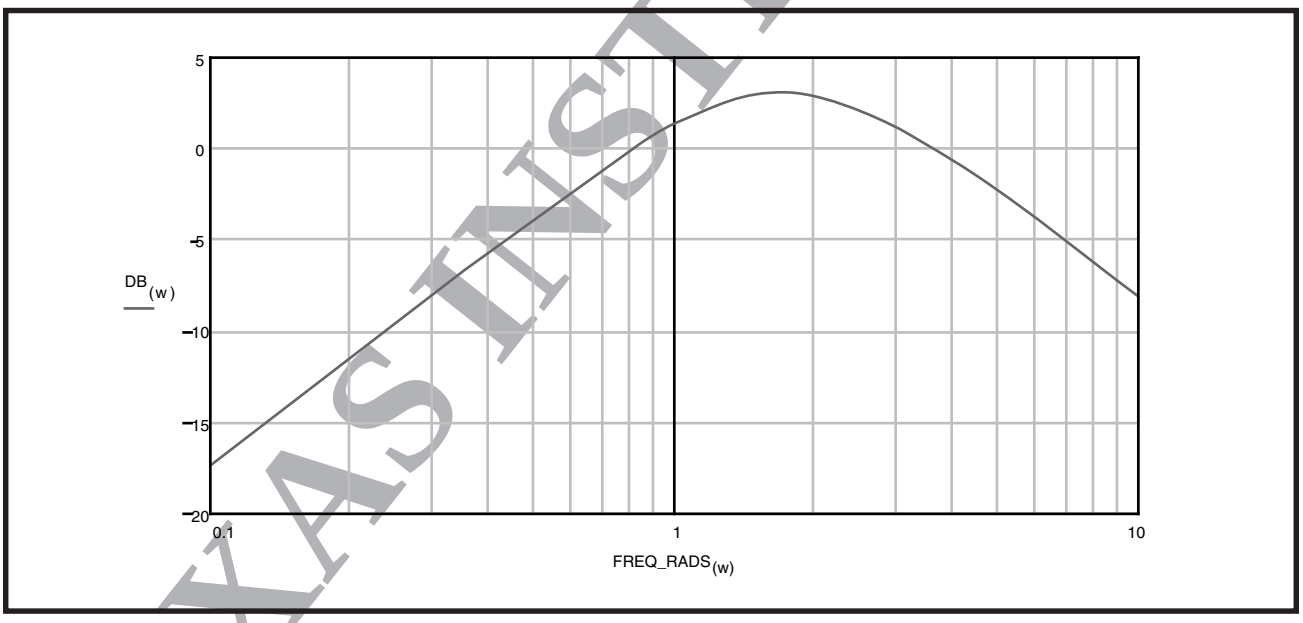


FIGURE 13: Pre-Differentiator Normalized Magnitude

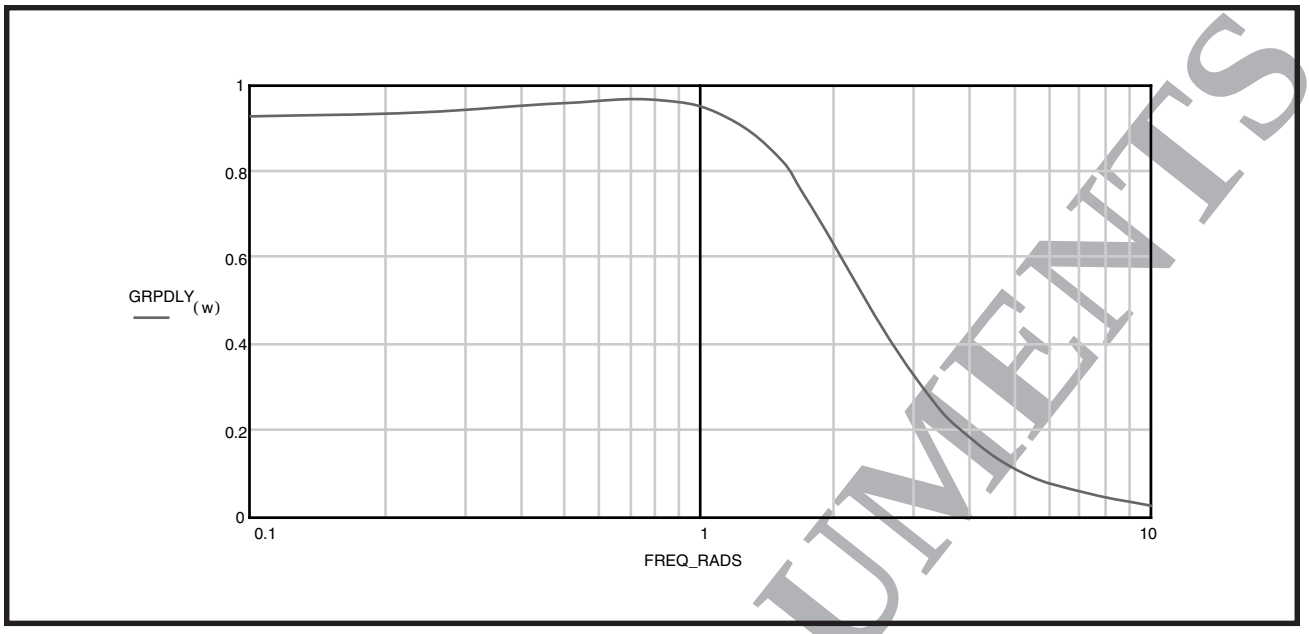


FIGURE 14: Pre-Differentiator Normalized Group Delay

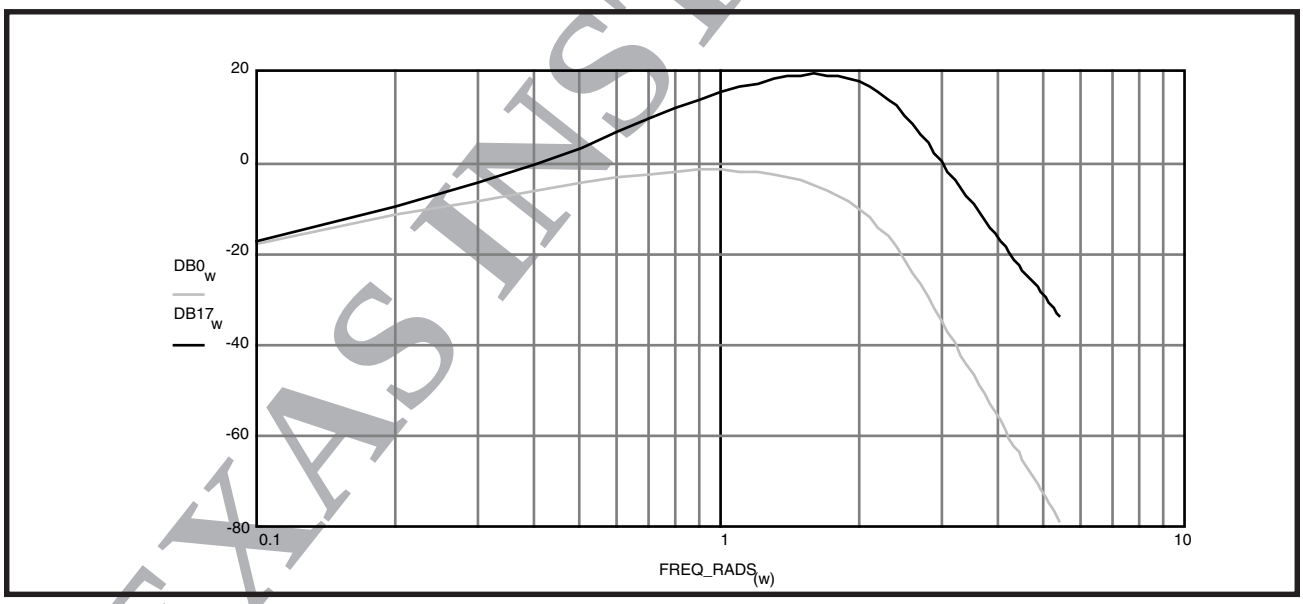


FIGURE 15: Total Channel Normalized Magnitude (0, 17 dB Boost)

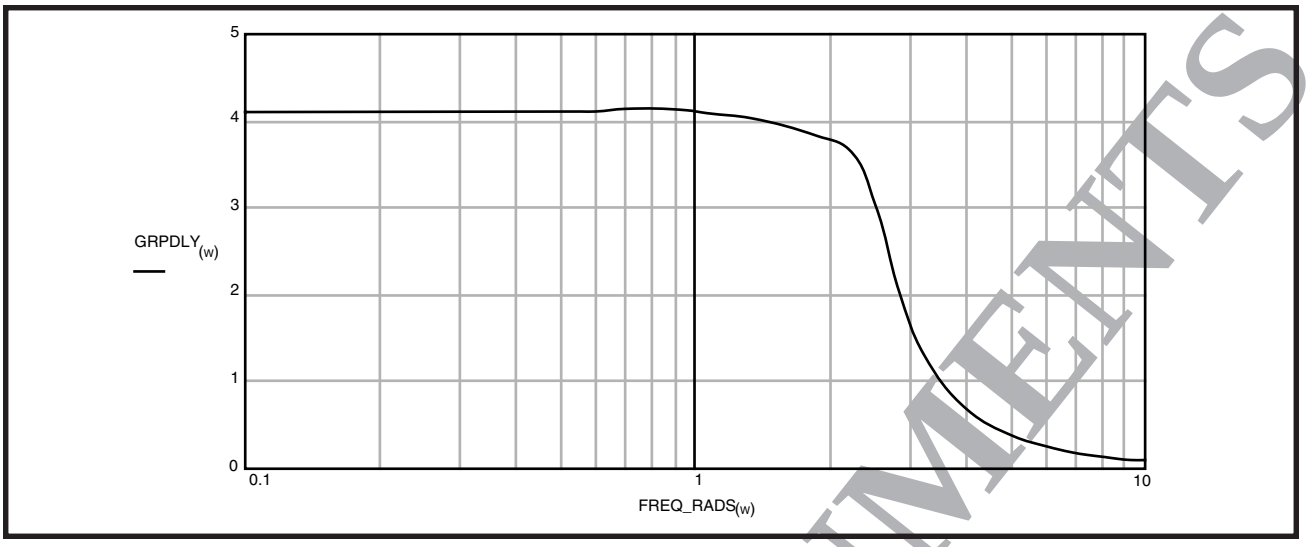


FIGURE 16: Total Channel Normalized Group Delay

PROGRAMMABLE FILTER/PRE-DIFFERENTIATOR CIRCUIT DESCRIPTION

(continued)

total channel response at Fpk by the same amount. Thus, when observing the total channel, the change in magnitude at Fpk as a function of boost is equal to the change in boost of the filter by itself. The individual responses of the pre-differentiator and the filter are specified and tested compositely in the electrical section of this document under the heading: Total Channel Parameters.

Internal AC Coupling

The conventional ac coupling at the filter/qualifier interface is now replaced by a pair of feedback circuits, one for the normal and one for the differentiated filter outputs. The offset of each of the filter outputs are sensed, integrated, and fed back to the filter output

TABLE 5: Filter Group Delay Response (Boost = 13 dB)

FREQ.	DELAY (s)						
(rad/s)	-30%	-20%	-10%	0%	10%	20%	30%
0	-2.22	-2.54	-2.86	-3.18	-3.49	-3.81	-4.13
0.1	-2.32	-2.60	-2.89	-3.17	-3.46	-3.74	-4.03
0.2	-2.55	-2.75	-2.96	-3.17	-3.38	-3.58	-3.78
0.3	-2.80	-2.91	-3.04	-3.16	-3.29	-3.41	-3.53
0.4	-3.00	-3.05	-3.10	-3.16	-3.22	-3.28	-3.33
0.5	-3.13	-3.14	-3.15	-3.17	-3.18	-3.19	-3.20
0.6	-3.21	-3.20	-3.19	-3.17	-3.16	-3.14	-3.13
0.7	-3.26	-3.24	-3.21	-3.18	-3.15	-3.12	-3.09
0.8	-3.28	-3.25	-3.21	-3.18	-3.14	-3.10	-3.07
0.9	-3.28	-3.25	-3.21	-3.17	-3.13	-3.09	-3.06
1	-3.28	-3.24	-3.20	-3.17	-3.13	-3.09	-3.05
2	-3.24	-3.22	-3.20	-3.18	-3.16	-3.14	-3.13
3	-1.30	-1.29	-1.28	-1.27	-1.26	-1.25	-1.24

FUNCTIONAL DESCRIPTION (continued)

stage. The feedback loop forces the filter output offset nominally to zero. To minimize transients, separate coupling capacitors are used for the data and servo modes. In the normal read mode (Low_Z = 0), an AC coupling low cutoff frequency of about 50 kHz or 150 kHz can be selected with the OSNBW bit of the DRC Register (bit 7). When Low_Z is asserted, the cutoff frequency increases to about 550 kHz or 1.2 MHz depending upon the state of the OSNBW bit.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator (TBG) is a PLL based circuit that provides a programmable reference frequency to the data separator for constant density recording applications. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N, and DR Registers. The TBG output frequency, Fout, should be programmed to be ((3/2) • NRZ Data Rate). The time base also supplies the timing reference for write precompensation so that the precompensation tracks the reference time base period.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to reduce the effects of common mode noise.

In read, write and idle modes, the programmable time base generator is used to provide a stable reference frequency for the data separator. In the write and idle modes, the TBG output, when selected by the CT1 register TP bits, can be monitored at the TPB and $\overline{\text{TPB}}$ test pins. In the read mode, the TBG output should not be selected for output on the test pins to minimize the possibility of jitter in the data separator PLL.

The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

F_{TBG} = FREF [(M + 1)/(N + 1)]

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The DR Register must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N Registers only after the DR Register is updated.

The DR Register value directly affects the following parameters:

- center frequency of the time base generator VCO
- center frequency of the data separator VCO
- phase detector gain of the time base generator phase detector
- phase detector gain of the data separator phase detector

The reference current for the DR DAC is set by a fixed external resistor, RR, connected between the RR pin and ground. RR = 13.7 kΩ for up to 120 Mbit/s operation.

DATA SEPARATOR CIRCUIT DESCRIPTION

The Data Separator circuit provides complete

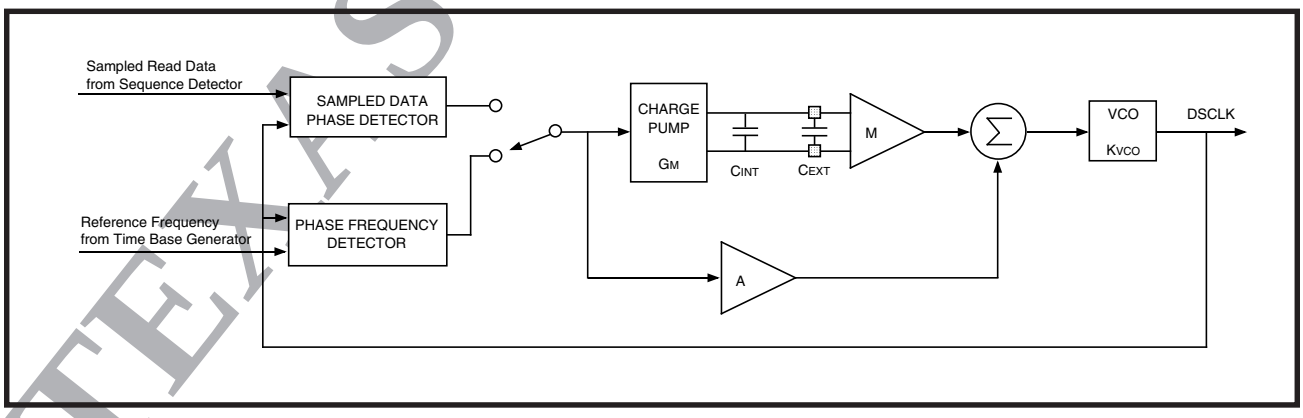


FIGURE 17: Data Separator Phase-Locked Loop Block Diagram

encoding, decoding, and synchronization for 1,7 RLL data. In data read mode, the circuit performs, clock recovery, code word framing (bit synchronization), decoding, sync byte detection, descrambling, and NRZ interface conversion. In the write mode, the circuit generates the VCO sync field, scrambles and converts the NRZ data into 1,7 RLL format, and performs write precompensation.

The circuit consists of five major functional blocks: the data synchronizer, 1,7 ENDEC, NRZ scrambler/descrambler, NRZ interface, and write precompensation.

Data Synchronizer

The data synchronizer uses a fully integrated, fast acquisition, PLL to recover the code rate clock from the incoming read data. To achieve fast acquisition, the data synchronizer PLL uses zero phase restart (when switching to read mode) and two separate phase detectors to drive the loop. A decision-directed phase detector is used in the read mode and phase-frequency detector is used in the idle, servo, and write modes.

A 3T ('001') pattern is written for PLL and bit synchronization. It produces a '3', '3', '0', E²PR4 sample read pattern. After read gate is asserted, the phase detector is switched from the reference clock to the read data. The VCO is then restarted in phase with the detected data and the PLL acquires lock using its timing acquisition algorithm. The switching from acquisition to data mode occurs when the programmable sync field count (SFC) has been reached . The gain of the phase detector is reduced by a factor of 5 after the SFC to reduce the bandwidth of the loop. This increases the immunity of the loop from noise during data.

In the write and idle modes the non-harmonic phase-frequency detector is continuously enabled, thus maintaining both phase and frequency lock to the time base generator's VCO output signal, F_{TBG}. The polarity and width of the detector's output current pulses correspond to the direction and magnitude of the phase error.

The two phase detector outputs are muxed into a single differential charge pump which drives the loop filter directly. The loop filter requires an external capacitor. The loop damping ratio is programmed by bits 6 - 0 in the DRC Register. The programmed damping ratio is independent of data rate.

In write mode, the TBG output is used to clock the encoder and write precompensation circuits producing the write data (WD, $\overline{WD}$) outputs and the precompensated, delayed Code Clock outputs (DLYCCLKP, DLYCCLKN).

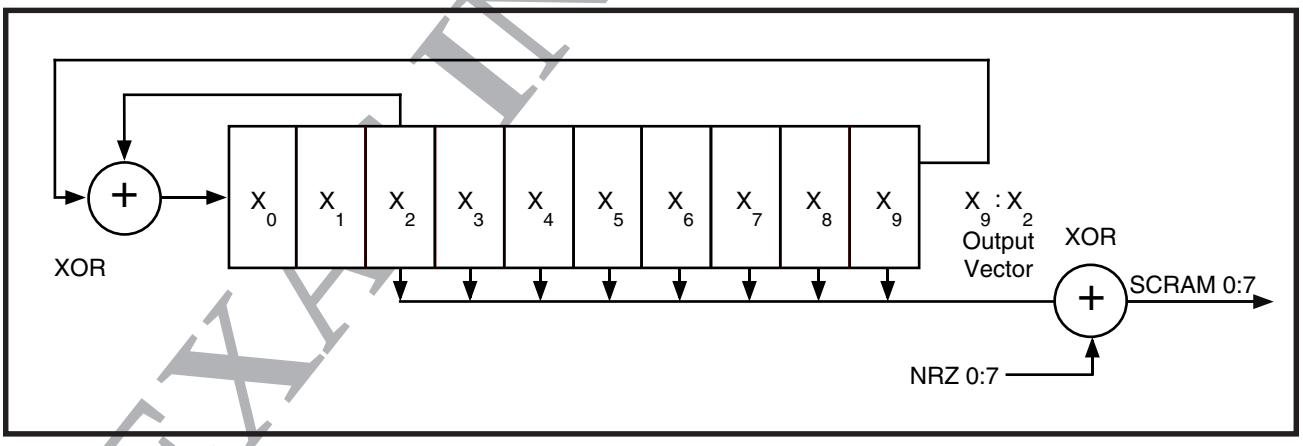


FIGURE 18: Scrambler Block Diagram

TABLE 6: Scrambler Sequence

CLOCK CYCLE	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	SCRAMBLER STATE X9:X0 h	OUTPUT VECTOR X9:X2 h
0	1	1	1	1	1	1	1	1	1	1	3FF	FF
1	1	1	1	1	1	1	1	1	1	0	3FE	FF
2	1	1	1	1	1	1	1	1	0	0	3FC	FF
3	1	1	1	1	1	1	1	0	0	0	3F8	FE
4	1	1	1	1	1	1	0	0	0	1	3F1	FC
5	1	1	1	1	1	0	0	0	1	1	3E3	F8
6	1	1	1	1	0	0	0	1	1	1	3C7	F1
7	1	1	1	0	0	0	1	1	1	0	38E	E3
8	1	1	0	0	0	1	1	1	0	0	31C	C7
9	1	0	0	0	1	1	1	0	0	0	238	8E
10	0	0	0	1	1	1	0	0	0	1	071	1C
11	0	0	1	1	1	0	0	0	1	0	0E2	38
12	0	1	1	1	0	0	0	1	0	0	1C4	71
13	1	1	1	0	0	0	1	0	0	1	389	E2
14	1	1	0	0	0	1	0	1	1	1	313	C4
15	1	0	0	0	1	0	0	1	1	1	227	89
16	0	0	0	1	0	0	1	1	1	0	04E	13

ENDEC

During write operations the encoder portion of the ENDEC converts 2-bit parallel data, scrambled or unscrambled, to 3-bit parallel code words that are then converted to serial format. In data read operation, after the sync byte has been detected in the sequence qualified serial data stream, the data is converted to 3-bit parallel form and the decoder portion of the ENDEC converts the 3-bit code words to 2 bit NRZ format.

Scrambler/Descrambler

The scrambler/descrambler circuit is provided to reduce fixed pattern effects on the channel's performance. It is enabled or disabled using the SD bit in the SC Register. In write mode, if enabled, the circuit scrambles the 2-bit internal NRZ data before passing it to the encoder. Only user data, i.e., the NRZ data following the second sync byte, is scrambled. In data read mode, only the decoded NRZ data after the second sync byte is descrambled. The scrambler polynomial is $H(X) = 1 \text{ xor } X^3 \text{ xor } X^{10}$. The scrambler block diagram is shown in Figure 18. The scrambler is effectively clocked 2 times for each NRZ dibit time, and the X_8X_9 outputs are XOR'd with the NRZ data (X_8 is the LSB, and is XOR'd with NRZ_0).

When the scrambler is enabled, the initial state of the scrambler is 3FFh (all ones), and the X output vector is FFh. At the next NRZ byte, the scrambler has been clocked 8 times, the scrambler state is 31Ch and the X output vector is E3h. Since the scrambler is reset during each resync period (i.e., every 15 bytes) the X output vector repeats every 120 bit times.

When the scrambler is disabled, the flip-flops are preloaded with zeros, and the scrambler state (and the X vector) remains at zero. When this is XOR'd with the data, the data is unchanged.

NRZ Interface

A byte-wide NRZ controller interface is provided. In data write mode, the NRZ write data is latched by the SSI 33P3705 on the rising edge of the WCLK input. The WCLK must be synchronous to RCLK or overflow/underflow will occur. It is recommended that WCLK be connected to or derived from the RCLK to prevent this from occurring.

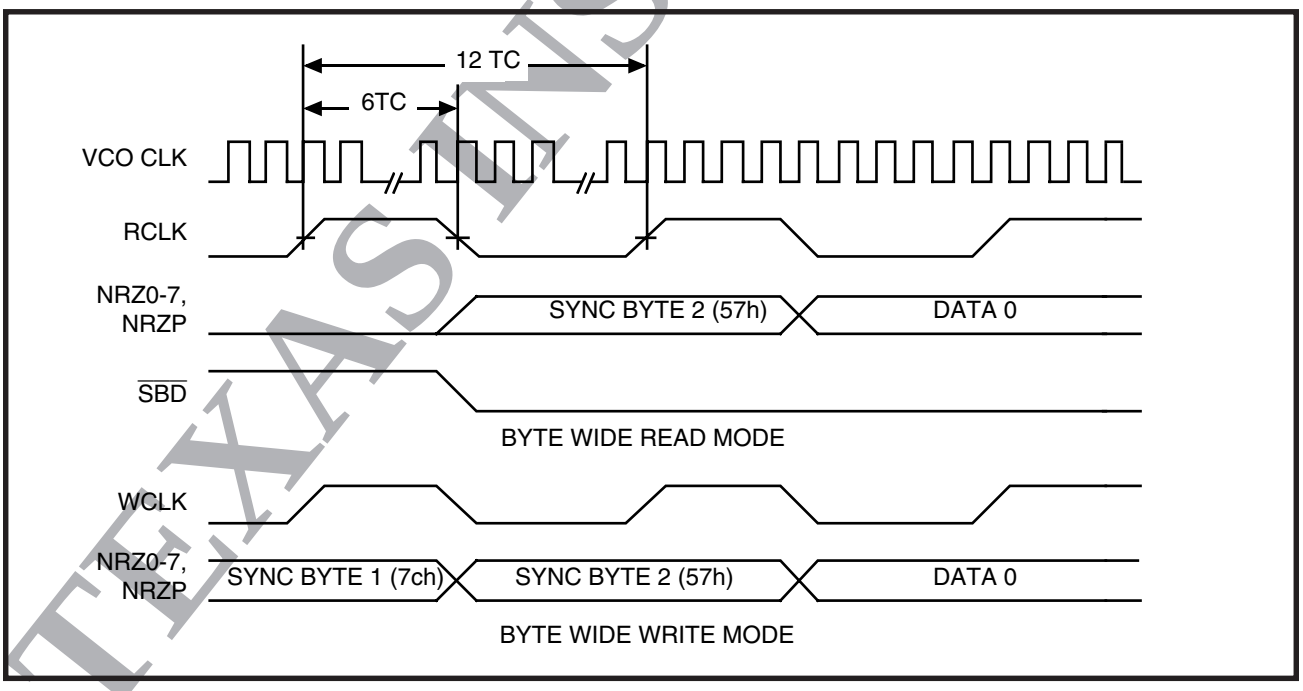


FIGURE 19: RCLK and WCLK vs. NRZ Data

ENDEC (continued)

In data read mode, the NRZ data will be presented to the controller near the falling edge of RCLK so that it can be latched by the controller on the rising edge of RCLK. When RG goes high, the NRZ interface will output low data until the sync byte has been detected. The first non-zero data presented will be the sync byte #2 regardless of which sync byte is detected. The sync byte detect output $\overline{SBD}$ will be asserted low immediately prior to sync byte #2 regardless of which sync byte is detected. The NRZ interface is at a high impedance state when not in data read mode.

Code Clock Write Precompensation and Write Data Output

In write mode, the write data is synchronized to the delayed code clock (DLYCCLKP/DLYCCLKN) and output at the WD/$\overline{WD}$ pins. Write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes specific write data patterns and can adjust the time position of the rising edge of the delayed code clock (DLYCCLKP/DLYCCLKN), used by the external laser driver circuits to counteract the magnetic nonlinearity effect. The write precompensation time shift can be specified as either late or early with the WPPOL bit of the SC Register (SC[3]). The magnitude of the time shift is programmable via the WPC[3:0]

TABLE 7: Write Precompensation Algorithm

Bit			Bit N Compensation
N-2	N-1	N	
0	0	1	None
1	0	1	Late or Early as specified by SC[3] (WPPOL)

TABLE 8: Write Precompensation Time Shift Values

WPC3	WPC2	WPC1	WPC0	WPC Value	Shift
0	0	0	0	0	None
0	0	0	1	1	0.01 T_{TBG}
0	0	1	0	2	0.02 T_{TBG}
0	0	1	1	3	0.03 T_{TBG}
0	1	0	0	4	0.04 T_{TBG}
0	1	0	1	5	0.05 T_{TBG}
0	1	1	0	6	0.06 T_{TBG}
0	1	1	1	7	0.07 T_{TBG}
1	0	0	0	8	0.08 T_{TBG}
1	0	0	1	9	0.09 T_{TBG}
1	0	1	0	10	0.10 T_{TBG}
1	0	1	1	11	0.11 T_{TBG}
1	1	0	0	12	0.12 T_{TBG}
1	1	0	1	13	0.13 T_{TBG}
1	1	1	0	14	0.14 T_{TBG}
1	1	1	1	15	0.15 T_{TBG}

T_{TBG} is the period of the reference frequency provided by the internal time base generator.

Register bits, and is made proportional to the time base generator's VCO period (i.e., data rate). The precomp is adjustable in steps of 1% of the time base generator period to a maximum of 15% under nominal conditions. WPC = 0 disables the precompensation circuitry. The delayed code clock will be precompensated according to the algorithm shown in Table 7 below. Table 8 shows the Write Precompensation Time Shift Values.

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude

Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

Code Clock Variable Delay

The differential code clock outputs (DLYCCLKP/DLYCCLKN) can be delayed with respect to the Write Data outputs (WD/$\overline{WD}$) as specified by the WDLY[3:0] register bits. This delay is programmable up to one full cycle of the code clock with a resolution of 4 bits, or 15 steps. Setting WDLY = 0 disables the code clock delay. The time delay will scale with the user data rate as specified by the equation:

t_d (sec) = WDLY/[15 • (1.4 • DR + 7.4) • 10^6]

where DR and WDLY are the Data Rate and Clock Delay Register values, both in decimal notation.

DATA RESYNC CIRCUIT

Normal Operation

To enable the recovery of data due to media defects, the SSI 33P3705 provides the ability to reframe the user data following a large defect so that the data loss in each sector is minimized. This is achieved with the use of a resync pattern which is inserted into the user data during write mode. The resync pattern is written immediately following every 15 bytes of user data as shown in Figure 20 below, for a total of 39 resyncs in a 512 byte sector. The resync pattern which is one byte, or 12 code bits in length, has the binary value of 010 000 001 010, and is not recognized by the 1,7 encoder/decoder as a valid pattern. The scrambler/descrambler is reset during the resync period so that the resync pattern is not affected.

In read mode, data detection is initialized by the proper detection of the sync byte pattern. The sync byte pattern used by the SSI 33P3705 is a fault-tolerant 7C57h pattern which is not scrambled. When the sync

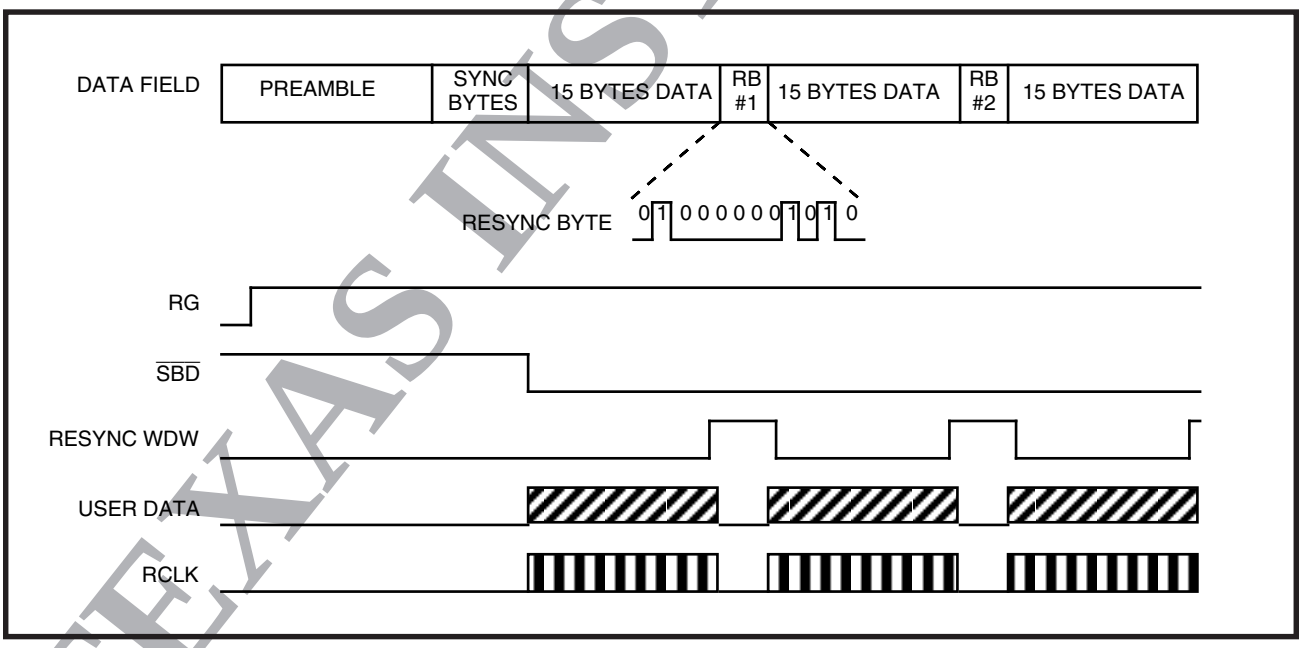


FIGURE 20: Normal Detection of Resync During Sector Read

DATA RESYNC CIRCUIT (continued)

byte is detected, the $\overline{SBD}$ pin is asserted low initializing an internal counter. After every 16 bytes are counted a window is opened to enable the detection of the resync byte. The resync window width is programmable via the RWW[1:0] Register bits, with values of 12 (1 byte), 14, 20, and 26 code bits available. During normal operation, as displayed in Figure 20, the counter is restarted after each resync is properly detected, enabling the detection of each subsequent resync byte in its corresponding window throughout the sector. The NRZ data clock (RCLK) to the controller is disabled during the resync period and contains exactly 15 clock periods between each period.

Defect Recovery In Data Field

Recovery of data in a defect area is made possible by identifying the location of the missing resyncs in the sector. If a resync is not detected in the window where expected, the number of the missing resync is stored in the MRBEG[5:0] Register. Subsequently, the first resync to be detected following the missing resync will be stored in the MREND[5:0] Register. Two or more consecutive missing Resyncs must be present in order for these registers to be loaded. The initial value of both registers will be zero. A single missing resync will not be flagged. These register locations identify the beginning and end points of the defect to facilitate data recovery by the controller.

The number of missing resyncs allowed in a sector is stored in the MRFT[2:0] Register by the controller during a disk format. In a read operation, if the number of missing resyncs equals the threshold value programmed in this register, the MRF signal is asserted high as shown in Figure 21. This signal is provided as a maskable interrupt for the controller (discussed below). The actual number of missing resyncs detected in a sector is stored in the MRFC[3:0] Register and is available through the serial port. In addition, an output is provided to flag each missing resync byte. As displayed in Figure 21, the RMB pin will be asserted high each time the resync byte is not detected in its corresponding window.

To minimize the disturbance which the AGC and PLL may experience during a defect, and thus provide the best opportunity for data recovery, these circuits may be placed in a coast mode by the controller as specified in the CST1 and CST2 Registers. The CST1[5:0] Register bits can be written with the location at which the AGC and PLL are to begin to coast. The endpoint of the coast mode is stored in the CST2[5:0] Register. During normal operation both registers are set to 00h. To enable coast operations in split sector data fields, two register bits are provided to inform the channel if the coast mode is to be initiated after the first, second, or third assertion of RG. Register bits SSPLT[1:0] can be set to decimal values 1, 2, or 3 for this purpose, allowing up to 2 splits in any given sector. The duration of the coast mode can also be observed on the COAST output pin, which will be asserted high during the coast period as shown in Figure 21.

Defect Recovery Due To Sync Byte Loss

In the event that the sync byte is not detected, the SSI 33P3705 provides an alternate method of synchronizing the resync windows which is not dependent upon the initial sync byte. The special retry mode can be enabled by setting the resync recovery mode bit (RRM = 1) along with the sync byte detect mode bit (SBDM = 1). When the SBDM bit is set high, the fault-tolerant detection of the sync byte is disabled requiring an exact match to the 7C57h pattern. Setting the RRM bit high enables the following resynchronization of data to occur due to the corrupted sync byte pattern. During the read retry operation specified by the SSPLT[1:0] Register bits, a 57h pattern will be sent to the controller immediately following the completion of sync field count (SFC). This will be followed by either 15 or 30 NRZ clocks, the actual number specified by the state of the NRZNUM Register bit. The additional NRZ clocks allow for the first resync pattern to also be corrupted along with the sync byte. The additional NRZ clocks will be sent to the controller at the normal NRZ rate specified by the programmed data rate (a function of the M, N, and DR Registers) divided by 8. During the retry mode the resync window is opened continuously until the first resync pattern is detected, after which the data is read as normal. Timing diagrams for both of these conditions are shown in Figure 22.

A dedicated pin is also provided to indicate the mis-detection of the sync byte pattern. The SBDEF pin will be asserted high if the sync byte is not detected within 48 bytes after SFC. The SBDEF pin will remain high until the next positive transition of RG.

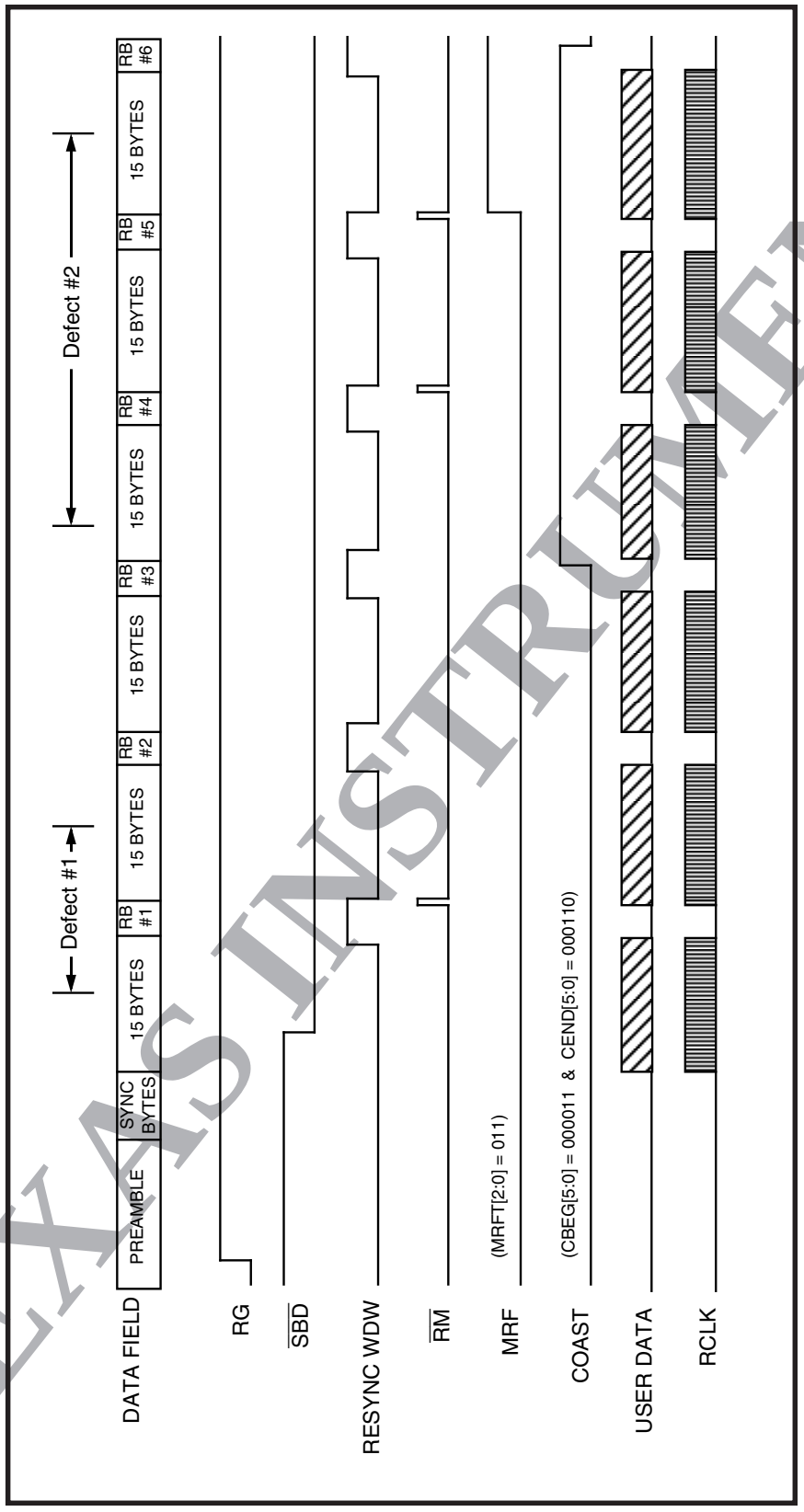


FIGURE 21: Mis-Detection of Resyncs due to Defects

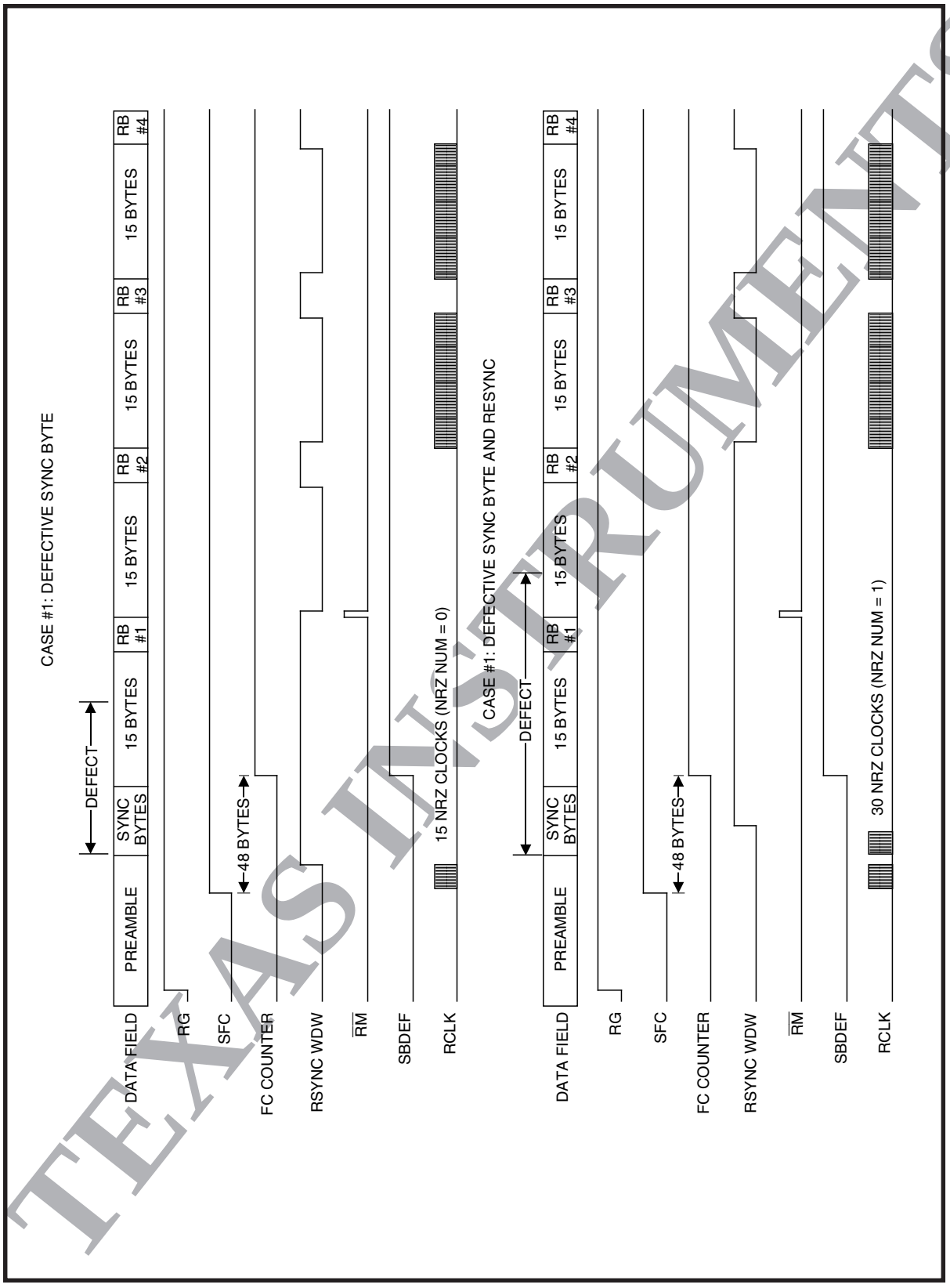


FIGURE 22: Loss of Sync Byte Due to Defects

FUNCTIONAL DESCRIPTION (continued)

Defect Recovery Due to Sync Byte Loss

The 33P3705 also incorporates a timeout feature which can be used to interrupt the controller should the Sync Byte fail to be detected in the specified time period. When register bits RRM = 0 and MIC[3] = 1, then the CONTDEF pin will be asserted if the Sync Byte is not detected within 48 NRZ clocks following the completion of Sync Field Count (SFC). This assumes that the appropriate wedge has occurred as selected by register bits CST1[7:6] and MIC[3] = 1. Again, register bit MIC[1] will also be set high at this time.

Mask Interrupt Control

Mask interrupt capability is provided for the external controller with the CONTDEF output pin. This pin can be used to interrupt an external controller based upon the conditions specified by the MI[1:0] Register bits. These register bits allow any combination of the MRF and/or SBDEF signals to be used as an interrupt. The source of the interrupt can be read from the IS[1:0] Register bits, and can be reset by writing to the same bits. Thus, the CONTDEF pin will be asserted low when the unmasked interrupt source is asserted, and must be reset by writing a zero to IS[1:0]. The polarity of the CONTDEF pin can be inverted to an active high signal by setting register bit INTPOL = 1.

SERIAL PORT CIRCUIT DESCRIPTION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the twenty-two internal registers of the SSI 33P3705. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

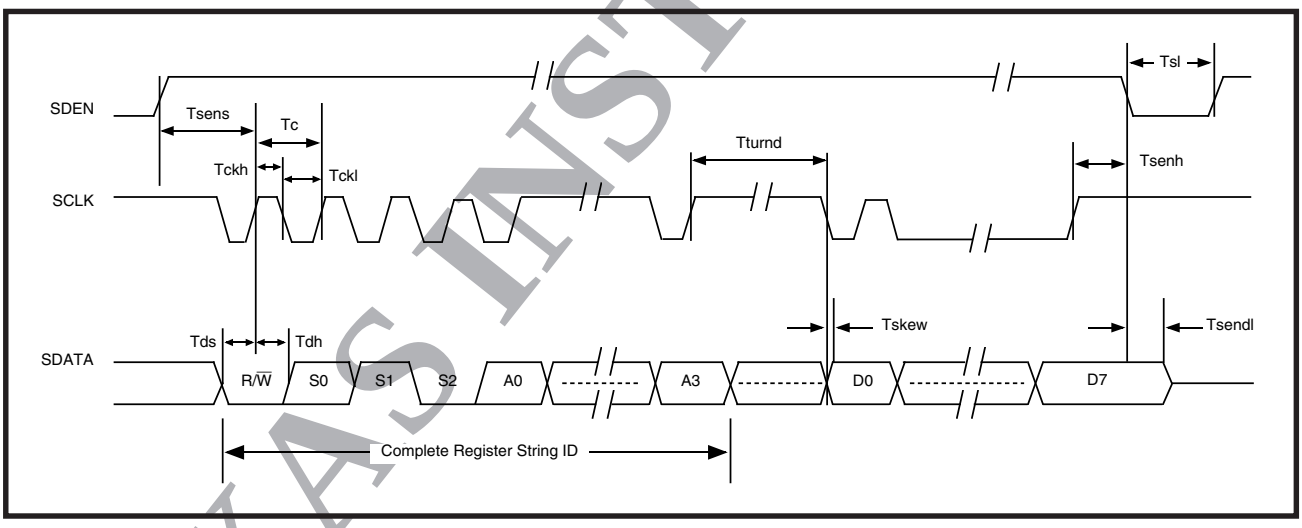


FIGURE 23: Serial Port Interface Timing

FUNCTIONAL DESCRIPTION (continued)

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/$\overline{W}$ bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits contain the three device select bits, S0:S3, and the four address bits, A0:A3, which determine the internal register to be accessed. The entire byte is considered to be the register string ID and is referred to in the following format: A3, A2, A1, A0, S2, S1, S0, R/$\overline{W}$. The address and select bits together are considered to be the register address and are referred to in the following format: A3, A2, A1, A0, S2, S1, S0

The second byte contains the programming data. In read mode (R/$\overline{W}$ = 1) the SSI 33P3705 will output the register contents of the selected address. In write mode (R/$\overline{W}$ = 0) the device will load the selected register with data presented on the SDATA pin.

At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. If the $\overline{POR}$ pin is asserted, however, at initial power-up or at any other time, the contents of the internal registers will be set to their initial values as specified in the Serial Port Register Definitions section. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in the electrical specifications section. Figure 23 shows the serial port interface timing.

DESCRIPTION OF OPERATING MODES

The fundamental operating modes of the SSI 33P3705 are controlled by the servo gate (SG), read gate (RG), and write gate (WG) input pins. The exclusive assertion of any these inputs causes the device to enter that mode. If none of these inputs is asserted, the device is in idle mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The overriding mode takes effect immediately.

RG and SG are asynchronous inputs and may be initiated or terminated at any time. WG is also an asynchronous input, but should not be terminated until the encoder has been flushed of data.

Idle Mode Operation

If SG, RG, and WG are not active, the SSI 33P3705 is in idle mode. In idle mode, the time base generator (TBG) and the data separator PLL are running, and the data separator PLL is phase-frequency locked to the TBG output. The AGC, continuous time filter, and pulse qualifiers are active, but the outputs of the pulse qualifiers are disabled. The continuous time filter uses the programmed values in the data mode registers (FC, FB) for cutoff frequency and boost. The AGC operation is the same as in the VCO preamble portion of a data read.

Servo Mode Operation

If SG is high, the device is in the servo mode. This mode is the same as idle except that the filter cutoff, boost, and asymmetry settings are switched from the data mode registers to the servo mode registers (FCS and SRV), the AGC is switched to servo mode, and the $\overline{RDS}$ and PPOL and outputs are enabled. The assertion of SG causes read mode, write mode, and the power down register settings for the front end to be overridden.

Write Mode Operation

The WG pin operation can be inverted by setting the WGP bit in the MC Register (bit 7). When MC:7 is low, WG is active high. When MC:7 is high, WG is active low. Throughout this specification, WG is referred to as active high. A minimum of one NRZ time period must elapse after RG goes low before WG can be set high. The data separator PLL is phase-frequency locked to the TBG VCO output (FOUT) in this mode.

When WG goes high, the NRZ inputs must be low and must be held low for the duration of the VCO 3T sync field generation. To write the VCO sync field, the NRZ pattern '00', is written. Two Sync Bytes must be written, SB1 (7C hex) and SB2 (57 hex) followed by user data, which is scrambled (if enabled). The data is then encoded into 1,7 RLL formatted data, precompensated, and then fed to the write data toggle flip-flop to be output on the WD/$\overline{WD}$ pins for use by the preamp to store data on the disk. Finally after the last byte of user data has been clocked in, the WG must remain high for a minimum of 5 NRZ bite times to insure that the device is flushed of data. WG can then go low. WD/WD stops toggling a maximum of 2 NRZ bit time periods after WG goes low.

When not in write mode, the write data outputs are placed in high impedance mode to reduce power dissipation of any termination resistors. Since the write

data flip-flops are reset when WG goes low, the WD outputs go to a zero state when WG is low.

Data Read Mode Operation

Data read mode is initiated by setting the read gate (RG) input pin high. This action causes the data synchronizer to begin acquisition of the clock from the incoming VCO sync pattern. To achieve this, the data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the sample clock. This PLL is normally locked to the time base generator output, but when read gate input (RG) goes high, the PLL's reference input is switched to the filtered incoming read signal.

Acquisition of DS VCO Sync and AGC Mode Switch

When RG is asserted, the DS PLL input is switched from the TBG VCO output to the sampled data input. The VCO is then restarted in phase with the detected data and the PLL acquires lock using its timing acquisition algorithm. This is also the point at which an internal counter begins counting DSVCO code clock periods. The counter continues counting until a count value of SFC, programmed with the SFC bits in the SC Register, is reached. When the counter reaches SFC, the data synchronizer PLL is assumed to be locked and settled (VCO lock). At SFC, the PLL is switched from the acquisition to data mode and the phase detector gain is reduced. The AGC is switched early from its continuous time peak detect mode to its sample data mode at count of SFC or SFC/2 as set by the AGC SWITCH bit. To allow for different preamble lengths, SFC can be set to 72, 96, 120, or 144 from the SC Register. These values for SFC are the number of code clock periods in the sync field.

VCO Lock, PD Gain and Code Bit Frame Detector Enable

At SFC, the phase detector gain is reduced by a factor of 5. Also at SFC, the DS VCO is assumed locked to the incoming read samples, and an internal VCO LOCK signal is generated. This signal switches the RCLK generator source from the TBG output (FOUT) to the DS VCO clock. VCO LOCK also enables the code bit frame detection circuitry to detect the 3T boundaries. RCLK may stop toggling for up to a maximum of 2 RCLK time periods during the FOUT to DS VCO switch over. No short duration glitches will occur on RCLK during the switch over. RG should not be disabled within a 1 byte period previous or following the RCLK switch.

Because the 1,7 RLL coding encodes 2 NRZ bits into 3 code bits, the correct decoding frame must be established. When the Code Bit Frame Detector circuitry is activated, it searches for 3 sets of 3T('001') patterns. The leading '0' defines the beginning of the decode frame. The '1' defines the end bit of the decode frame.

During data, the decision-directed timing recovery updates the PLL by comparing amplitudes of adjacent, same polarity '3' samples. With dibits, the '3' and '2' samples are compared with an added correction factor.

Sync Byte Detect and NRZ Output

The SSI 33P3705 uses a dual sync byte scheme to provide more robust sync byte detection. The sync byte detection circuit looks for one of several combinations of correctly decoded NRZ pairs from SB1 = 7C hex and SB2 = 57 hex. The decision logic used is:

$$SBD = ABC + AB(E) + AC(D + E) + BC(D + E) + DE(A) + DEFG,$$

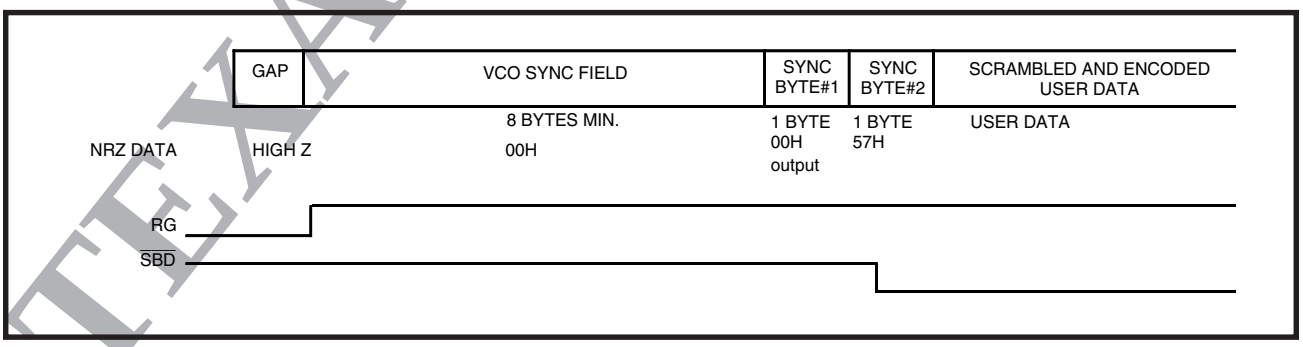


FIGURE 24: Data Read Sequence

TABLE 5: Mode Control

WG	RG	SG	MODE	DESCRIPTION
0	0	0	Idle	DS VCO locked to FTBG. NRZ7-0 tri-stated.
0	1	0	Data Read	DS PLL acquisition, code word boundary search and detect, decode, sync byte detect, and NRZ data output. DS VCO switched from FTBG to data after preamble detect. RCLK gen. input switched from FTBG to DS VCO. RCLK re-synchronized to data at code word boundary detect. NRZ7-0 active.
1	0	0	Data Write	Write mode sync field, sync byte and data write. DS VCO locked to FTBG. RCLK synchronized to FTBG. WD and $\overline{WD}$ active. NRZ7-0 tri-stated.
1	1	0	Read Override	RG overrides WG which causes any write in progress to cease and data read mode to be entered.
X	X	1	Servo	Low-Z and Fast Recovery AGC periods, followed by servo bursts capture.

DESCRIPTION OF OPERATING MODES (continued)

where H, A, B, C, F, D, G, E are true for the correctly decoded NRZ pairs: 01, 11, 11, 00, 01, 01, 01, 11 respectively, in sequence.

If the Mode Control Register bit 4 is set to 1, the sync byte detection circuit will declare sync byte Detect when a 7C57h NRZ data is detected.

The NRZ outputs are held low before the sync byte output. When sync byte is detected, the SB2 (57 hex) is presented at the NRZ interface. After RG is deasserted, the NRZ outputs go to a high impedance state.

Power Down Operation

The power management modes of the SSI 33P3705 are determined by the states of the PD Register bits, the power down mode bit, and the $\overline{PWRDN}$ input. The individual sections of the chip, AGC/filter, pulse detector, data separator, and TBG can be powered down or up using the PD Register. When the power down mode bit = 0, a high level in a PD Register bit disables that section of the circuit when the $\overline{PWRDN}$ pin is asserted. When the power down mode bit = 1, a high level in a PD Register bit disables that section of the circuit regardless of the state of the $\overline{PWRDN}$ pin, and the $\overline{PWRDN}$ pin sets the device in a full sleep mode when asserted, regardless of the states of the PD Register bits.

The serial port is active in all power down modes. When SG = 1 or the RDE bit = 1, and the power down mode bit = 0, the AGC, filter, and pulse detector are automatically enabled regardless of the state of the $\overline{PWRDN}$ pin. The pulse detector is enabled when either SG = 1 or the RDE bit = 1, except when the device is in the full sleep mode. The time to restart from a full power down is dependent on the PLL loop filter and the data rate.

Register Bit Assignment Summary Table

Throughout this document, RR:BB refers to bit BB in register RR. As an example, PD:TB refers to bit TB in register PD.

NOTE: The initial default register values are denoted by <0>...<0000 0000> for each bit, or byte, respectively.

NAME	DESCRIPTION	ADDRESS	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	ID register	0000010 = 02h	ID_SM[7:0] <0001 0010>							
PD	TP Sel/Power Down	0001010 = 0ah	TPC/D [1:0] <00>		ATOEN <0>	PDM <1>	PDA <0>	PDT <0>	PDD <0>	UNUSED
FC	Filter cutoff, data mode	0010010 = 12h	RDPOL <0>	FC [6:0] Filter cutoff frequency, data mode <111 1111>						
FCS	Filter cutoff, servo mode	0011010 = 1Ah	OSNH <0>	FCS [6:0] Filter cutoff frequency, servo mode <001 1110>						
FB	Filter boost, data mode	0100010 = 22h	PQM <0>	FB [6:0] filter boost, data mode <101 1010>						
FGD	Filter asymmetric zero adjust	0101010 = 2Ah	RDATT [1:0] <00>		FGD sign <0>	FGD [4:0] Filter asymmetric zero adjust <0 0000>				
DVT	Detector threshold	0110010 = 32h	BOSP <0>	DVT [6:0]Data detector threshold level <100 1100						
SDVT	Servo Data Threshold	0111010 = 3Ah	AGC [1:0] <11>	DVT [5:0] Servo data threshold <10 0000>						
BLO	Base line offset	1000010 = 42h	Servo base line offset [3:0] <0000>				Data base line offset [3:0] <0000>			
CT1	Control test mode 1	1001010 = 4Ah	SBTM <0>	DTP1 <0>	TP [2:0] Test point control <000>			RDT <0>	PLL Tests <00>	
CT2	Control test mode 2	0010011 = 13h	SSI Test Mode <000>			Bypass TBG <0>	I/O MAP <0>	SSI test mode <0>	threshold test mode <0>	DTPO <0>
N	Time base N counter	1010010 = 52h	ZMD <0>	N [6:0] Time base generator M counter value <001 0011>						
M	Time base M counter	1011010 = 5Ah	M[7:0] Time base generator M counter value <1110 1111>							
DR	Data rate	1100010 = 62h	AGCSW <0>	DR [6:0] Data rate value <111 1111>						

Register Bit Assignment Summary Table (continued)

NAME	DESCRIPTION	ADDRESS	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SC	Sequence Control	1101010 = 6Ah	SFC [1:0] Sync field length <11>		AGC HOLD <0>	ScrDis <0>	WPPOL <0>	MRFC [2:0] Missing Resync Fail Count (Read Only)		
WCP	Write Clock Delay & Precomp	0100011 = 23h	WDLY [3:0] Write Clock Delay <0000>				WPC [3:0] Write Precomp. Magnitude <0000>			
MC1	Mode Control 1	1110010 = 72h	WG Pol <0>	OFND <0>	SBDD <0>	SBD mode <0>	Timed AGC <0>	RD Enable <0>	LTH <0>	DW <0>
MC2	Mode Control 2	1111010 = 7Ah	unused	unused	ENDPRE <1>	DISRDS <0>	INHSG <0>	LZSG <0>	FRCBYPS <0>	LZTCR <0>
DRC	Damping ratio control	0000011 = 03h	OSNBW <0>	DRC [6:0] Damping ratio <001 1001>						
TC	Time Control	0001011 = 0Bh	T_SPC <0>	Low Z Time [2:0] <111>			Fast Recovery Time [2:0] <111>			Read Data Pulse Width <0>
SRV	Servo Control	0011011 = 1Bh	ENSPRE <0>	FBS [1:0] <0>		SFGDS <0>	SGDE [1:0] <00>		SATT [1:0] <00>	
MRL1	Missing Resync Location 1	1000011 = 43h	RWW [1:0] <00>		MRBEG [5:0] Missing Resync Beginning Point (Read Only)					
MRL2	Missing Resync Location 2	1010011 = 53h	ENHADET <0>	FRCHA <0>	MRENDS [5:0] Missing Resync End Point (Read Only)					
CST1	PLL/AGC Coast 1	1100011 = 63h	SSPLT [1:0] <01>		CBEG [5:0] PLL/AGC Coast Mode Beginning Point <00 0000>					
CST2	PLL/AGC Coast 2	1110011 = 73h	RRM <0>	NRZNUM <0>	CEND [5:0] PLL/AGC Coast Mode End Point <00 0000>					
MIC	Mask Interrupt Control	0101011 = 2Bh	MRFT [2:0] Missing Resync Fail Threshold <100>			INTPOL <0>	MI [1:0] Mask Interrupt Control <00>		IS [1:0] Interrupt Source Control <00>	
SQTH	Servo Qualifier Threshold	0111011 = 3Bh	FATH[3:0] Full Amplitude Threshold <1000>				HATH[3:0] Half Amplitude Threshold <1000>			

REGISTER DESCRIPTIONS

SERIAL PORT REGISTER DEFINITIONS

Throughout the specification, the notation RR:BB is used, where RR is the register, and BB is the bit in the register. For example, PD:DS denotes the DS bit in the PD Register. Addresses are shown MSB first and are formatted as: A3, A2, A1, A0, S2, S1, S0.

POWER DOWN CONTROL REGISTER (PD)

Address = 000 1010 = 0Ah

BIT	NAME	DESCRIPTION
7:6	TPC/D[1:0]	Test point C/D/E Control MC[2] = 0 MC[2] = 1 TPC-$\overline{\text{TPC}}$ TPD-$\overline{\text{TPD}}$ TPE TPE 00 = disabled disabled disabled disabled 01 = DP/DN CP/CN as input FDC FOSN 10 = DP/DN CP/CN as output —— HOLD 11 = AGC AGC as output —— UFDecay
5	ATOEN	Output select for ATO test point 0 = ATO disabled (normal mode) 1 = ATO output enabled DAC last written to is selected
4	PDM	Power down mode 1 = $\overline{\text{PWRDN}}$ sets device in full sleep mode 0 = $\overline{\text{PWRDN}}$ sets selected sections in sleep mode
3	PDA	AGC, Filter power down
2	PDT	Time base generator power down
1	PDD	Data separator power down
0	TBD	Unused

Bits 3 - 0: 1 = power down, 0 = power up, as set by PDM bit

DATA FILTER CUTOFF REGISTER (FC)

Address = 001 0010 = 12h

7	RDPOL	$\overline{\text{RDS}}$ pin read data polarity 1 = active low 0 = active high
6:0	FC[6:0]	Filter cutoff frequency in non-servo mode $16 \le FC \le 127_{dec}$

SERVO FILTER CUTOFF REGISTER (FCS)

Address = 001 1010 = 1Ah

7	OSNH	Offset null hold enable 1 = Enable offset null hold during coast mode 0 = Normal operation
6:0	FCS[6:0]	Filter cutoff frequency in servo mode $16 \le FCS \le 127_{dec}$

REGISTER DESCRIPTION (continued)

DATA MODE FILTER BOOST REGISTER (FB)

Address = 010 0010 = 22h

BIT	NAME	DESCRIPTION
7	PQM	Pulse qualifier mode: 1 = Hysteresis (Polarity Check) 0 = Window Qualifier (No Polarity Check)
6:0	FB[6:0]	Filter boost setting in data mode $0 \le FB \le 127_{dec}$

FILTER ASYMMETRIC ZERO REGISTER (FGD)

Address = 010 1010 = 2Ah

7:6	RDATT[1:0]	Input attenuation resistance in data mode RDATT1 RDATT0
		1 1 = 0.8 kΩ 1 0 = 1.4 kΩ 0 1 = 2.1 kΩ 0 0 = Disabled
5	FGDS	Filter group delay equalization sign
4:0	FGD[4:0]	Filter group delay equalization magnitude

DATA DETECTOR THRESHOLD REGISTER (DVT)

Address = 011 0010 = 32h

7	BOSP	Base line offset polarity BOSP = 1: (+) offset, BOSP = 0: (-) offset
6:0	DVT[6:0]	Data detector threshold voltage $0 \le DVT \le 127_{dec}$

SERVO DATA THRESHOLD REGISTER (SDVT)

Address = 011 1010 = 3Ah

7:6	AGC[1:0]	AGC charge pump current in sampled AGC mode = 0.157 • AGC • DR
5:0	SDVT[5:0]	Servo data qualification threshold voltage Lth = 10.42 • SDVT [mV]

BASE LINE OFFSET (BLO)

Address = 100 0010 = 42h

7:4	SBO[3:0]	Servo base line offset [3:0] BOSP controls polarity Differential offset = 4xSBO mV
3:0	DBO [3:0]	Data base line offset [3:0] BOSP controls polarity Differential offset = 4xDBO mV

CONTROL TEST MODE REGISTER 1 (CT1)
Address = 100 1010 = 4Ah

BIT	NAME	DESCRIPTION
7	SBTM	Sync byte test mode 1 = Enable test mode 0 = Normal operation
6	DTP1	DIGTP Test point mux select (DTP0 = CT2:0) **DTP1 DTP0 Function** 0 0 Sampled CP Enable 0 1 Split Sector Cntr Out 1 0 Resync Window Out 1 1 Window Cntr Out
5:3	TP[2:0]	Multiplexed test point selection

TP3	TP2	TP1	Function	TPA, $\overline{TPA}$	TPB, $\overline{TPB}$
0	0	0	Test Points Off	high impedance	high impedance
0	0	1	Delay line A	Phase A In	Phase A out
0	1	0	Delay line B	Phase B In	Phase B out
0	1	1	Delay line out	Phase A out	Phase B out
1	0	0	Comparator Output	Phase A out	Phase B out
1	0	1	Detector Interleave	Detector A out	Detector B out
1	1	0	Detector out	Detector out	Phase Detector
1	1	1	VCO/2 or Fout/2	TBD	DS VCO/2 If RG = 1 TBG Fout/2 if RG = 0

2	RTM	Read test mode 1 = Mux RDT digital input to the data decoder, fix AGC/Filter low frequency gain at 24 dB, (used for testing only) 0 = normal operating mode
1:0	PLLT[1:0]	Phase lock loop/data separator loop filter tests PLLT1 PLLT0 0 0 = No tests (normal mode) 0 1 = TBG phase detector continuous pump down 1 0 = TBG phase detector continuous pump up 1 X = Enable Data charge pump test mode X 1 = Disable gain switching in Data Separator loop filter

REGISTER DESCRIPTION (continued)

CONTROL TEST MODE 2 (CT2)

Address = 001 0011 = 13h

BIT	NAME	DESCRIPTION
7 - 5	Reserved	SSI Test mode
4	BT	By-pass time base generator 1 = data synchronizer reference frequency is FREF input 0 = data synchronizer reference frequency is TBG output
3	I/OMAP	I/O Test enable 1 = Enable, 0 = Disable
2	Reserved	SSI Test mode
1	TTM	Threshold test mode: 1 = Enabled 0 = Disabled
0	DTP0	DIGTP Test point mux select (See CT1:6 Description)

N COUNTER REGISTER (N)

Address = 101 0010 = 52h

7	ZMD	AGC Input impedance 'Z' mode when LOWZ = 1 0 = Low-Z mode 1 = Open-Z mode
6:0	N[6:0]	N Counter $2 \leq N \leq 127$

M COUNTER REGISTER (M)

Address = 101 1010 = 5Ah

7:0	M[7:0]	M Counter $2 \leq M \leq 255$, $F_{TBG} = FREF \bullet (M + 1)/(N + 1)$

DATA RATE REGISTER (DR)

Address = 110 0010 = 62h

7	AGCSW	AGC Switch to sampled mode: 1 = occurs at SFC 0 = occurs at 1/2 SFC
6:0	DR[6:0]	Data rate DAC value. $0 \leq DR \leq 127$, Fvco (MHz) = 3/2 Data Rate

SEQUENCE CONTROL REGISTER (SC)
Address = 110 1010 = 6Ah

BIT	NAME	DESCRIPTION
7:6	SFC[1:0]	Sync field length **SFC2** **SFC1** **Sync field length (Code Periods)** 0 0 72 0 1 96 1 0 120 1 1 144
5	AGCH	AGC Hold over data. When enabled, the AGC is held after SBD 1 = Enable AGC hold 0 = Disabled
4	SD	Scrambler disable 1 = Disable 0 = Enable
3	WPPOL	Write precomp. polarity 1 = Early precomp 0 = Late precomp
2:0	MRFC2:0]	Missing resync fail count (read only)

WRITE CLOCK DELAY & PRECOMP (WCP)
Address = 010 0011 = 23h

7:4	WDLY[3:0]	Write clock delay
3:0	WPC[3:0]	Write precomp magnitude = 1.0% • WPC

REGISTER DESCRIPTION (continued)

MODE CONTROL 1 REGISTER (MC1)

Address = 111 0010 = 72h

BIT	NAME	DESCRIPTION
7	WGP	Write gate polarity 1 = Inverted (WGB); 0 = Noninverted (WG)
6	OFND	Offset null disable 1 = Disable offset null; 0 = Normal operation.
5	SBDD	Sync byte detect disable 1 = Sync byte not required to write. Also if RDT bit = 1, analog filter put into oscillation mode 0 = Normal operation.
4	SBDM	Sync byte detect mode 0 = Detect '7C' or '57' 1 = Detect single '57' NRZ
3	TAM	Timed AGC mode 0 = Disabled ; 1 = Enabled
2	RDE	RD Enable 1 = Enable RD when not in servo mode 0 = Disabled
1	LTH	Qualifier hysteresis select 1 = Hysteresis is 75% of threshold 0 = Normal operation (15%)
0	DW	Direct write 1 = NRZ0 drives the WD pins 0 = Disabled

MODE CONTROL 2 REGISTER (MC2)

Address = 111 1010 = 7Ah

7:6	Unused	
5	ENDPRE	Enable Pre-Differentiator in read and idle modes 1 = Enable Pre-Differentiator 0 = Pre-Differentiator disabled
4	DISRDS	Disable RDSB output 1 = Disable RDSB output 0 = Normal operation
3	INHSG	Inhibit Hold in servo mode 1 = Inhibit Hold when SG = 1 0 = Normal operation
2	LZSG	LowZ time period on SG Transitions 1 = 800 ns (16 FREF periods) 0 = 500 ns (10 FREF periods)
1	FRCBYPS	Force servo AGC gain when SG = 0 1 = Force BYPS voltage to fix servo AGC gain when SG = 0 0 = Normal operation

MODE CONTROL 2 REGISTER (MC2) (continued)
Address = 111 1010 = 7Ah

BIT	NAME	DESCRIPTION
0	LZTCR	Non Low-Z/Low Z Time Constant Ratio 0 = 15:1 8.3 kΩ:0.55 kΩ at VIA/VIAB 1 = 5:1 2.7 kΩ:0.55 kΩ at VIA/VIAB

DAMPING RATIO CONTROL REGISTER (DRC)
Address = 000 0011 = 03h

7	OSNBW	AC-Coupler bandwidth 1 = 150 kHz 0 = 50 kHz
6:0	DRC[6:0]	Damping amplifier gain A = DRC (0.7 / 127) Damping Ratio = A • KVCO • 0.25/(2 • ω_n)

TIME CONTROL REGISTER (TC)
Address = 000 1011 = 0Bh

7	T_SPC	Test points C & D enabled when not in servo mode 1 = Always enabled, 0 = Disabled when SG = 0
6:4	LZT[2:0]	Low-Z Time following WG falling edge LZT2 LZT1 LZT0 FREF periods Time @10 Mhz 0 0 0 2 200 ns 0 0 1 3 300 ns 0 1 0 5 500 ns 0 1 1 7 700 ns 1 0 0 10 1000 ns 1 0 1 13 1300 ns 1 1 0 16 1600 ns 1 1 1 20 2000 ns
3:1	FRT[2:0]	Fast recovery time FRT2 FRT1 FRT0 FREF periods Time @10 MHz 0 0 0 4 400 ns 0 0 1 6 600 ns 0 1 0 10 1000 ns 0 1 1 14 1400 ns 1 0 0 20 2000 ns 1 0 1 26 2600 ns 1 1 0 32 3200 ns 1 1 1 40 4000 ns
0	RDPW	Read data pulse width 1 = 25 ns 0 = 50 ns

REGISTER DESCRIPTION (continued)

SERVO CONTROL REGISTER (SRV)

Address = 001 1011 = 1Bh

BIT	NAME	DESCRIPTION
7	ENSPRE	Enable Pre-Differentiator in servo mode 1 = Enable Pre-Differentiator 0 = Pre-Differentiator disabled
6:5	FBS[1:0]	Filter boost setting in servo mode $0 \le FBS \le 3_{dec}$
4	SFGDS	Filter group delay equalization sign in servo mode
3:2	SGDE[1:0]	Filter group delay equalization magnitude in servo mode
1:0	SATT[1:0]	Input attenuation resistance in servo mode SATT1 SATT0 1 1 = 0.8 kΩ 1 0 = 1.4 kΩ 0 1 = 2.1 kΩ 0 0 = Disabled

MISSING RESYNC LOCATION 1 REGISTER (MRL1)

Address = 1000 011 = 43h

7:6	RWW[1:0]	Resync window width RWW1 RWW0
		1 1 = 26 code bits 1 0 = 20 code bits 0 1 = 14 code bits 0 0 = 12 code bits (1 byte)
5:0	MRBEG[5:0]	Missing resync beginning point (read only) $0 \le MRBEG \le 39$

MRL2 MISSING RESYNC LOCATION 2

Address = 1010 011 = 53h

7	ENHADET	Enable Half-Amplitude Detector 1 = Enable Half-Amplitude Detector 0 = Disabled
6	FRCHA	Force Servo Qualifier Half-Amplitude Threshold 1 = Force V_{HATH} half-amplitude threshold for test purposes 0 = Normal operation
5:0	MREND[5:0]	Missing Resync End Point (Read Only) $0 \le MREND \le 39$

PLL/AGC COAST 1 REGISTER (CST1)
Address = 1100 011 = 63h

BIT	NAME	DESCRIPTION
7:6	SSPLT[1:0]	Sector split number SSPLT1 SSPLT0 1 1 = Coast mode enabled on 3rd RG assertion 1 0 = Coast mode enabled on 2nd RG assertion 0 1 = Coast mode enabled on 1st RG assertion 0 0 = Unused
5:0	CBEG[5:0]	PLL/AGC Coast mode beginning point 0 ≤ CBEG ≤ 39

PLL/AGC COAST 2 REGISTER (CST2)
Address = 1110 011 = 73h

7	RRM	Resync recover mode 1 = Enabled 0 = Disabled
6	NRZNUM	Number of NRZ dummy data bytes to controller 1 = 30 0 = 15
5:0	CEND[5:0]	PLL/AGC Coast mode end point 0 ≤ CEND ≤ 39

MASK INTERRUPT CONTROL REGISTER (MIC)
Address = 0101 011 = 2Bh

7:5	MRFT[2:0]	Missing resync fail threshold
4	INTPOL	CONTDEF pin polarity 1 = Active high 0 = Active low
3:2	MI[1:0]	Mask interrupt control 1x = Inhibit interrupt on Sync Byte Defect x1 = Inhibit interrupt on Missing Resync Flag
1:0	IS[1:0]	Interrupt source control 1x = Sync Byte Defect x1 = Missing Resync Flag

SQTH SERVO QUALIFIER THRESHOLDS
Address = 011 1011 = 3Bh

7:4	FATH[3:0]	Servo Data upper qualification threshold voltage V_{FATH} = 330 + 22.0 • FATH [mV]
3:0	HATH[3:0]	Servo Data lower qualification threshold voltage V_{HATH} = 22.0 • HATH [mV]

PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output

POWER SUPPY PINS

NAME	TYPE	DESCRIPTION
VPA	-	AGC/filter/pulse qualifier analog circuit supply
VPF	-	Time base generator PLL digital circuit supply
VPT	-	Time base generator analog supply
VPP	-	Data separator PLL analog circuit supply
VPD	-	TTL buffer I/O digital supply
VPC	-	Internal ECL, CMOS logic digital supply
VPS (x2)	-	Sampled data processor supply
VNA (x2)	-	AGC/filter/pulse qualifier analog circuit ground
VNF (x2)	-	Time base generator PLL digital circuit ground
VNT	-	Time base generator analog ground
VNP (x2)	-	Data separator PLL analog circuit ground
VND	-	TTL Buffer I/O digital ground
VNC	-	Internal ECL, CMOS logic digital ground
VNS (x2)	-	Sampled data processor ground

ANALOG INPUT PINS

VIA, $\overline{\text{VIA}}$	AI	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins
RUFDC	AI	With an external resistor Rext connected to VPA, additional fast decay current is made available. Iufdc = (VPA - Vbyp)/Rext during fast recovery period if signal <125% of the target.

ANALOG OUTPUT PINS

NAME	TYPE	DESCRIPTION
TPA, $\overline{\text{TPA}}$	AO	TEST PINS: Emitter output test points. Various signals are multiplexed to these test points by the TP bits in the CT1 Register. The signals include the sampled values, comparator outputs and the detector outputs. The test points are provided to show how the signal is being processed. Internal “pull down” resistors to ground are provided. To save power when not in test mode, the TP bits must be set to “0”.
TPB, $\overline{\text{TPB}}$	AO	TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. These pins are used to look at the other phase of the interleaved signal.
TPC, $\overline{\text{TPC}}$	AO	TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. These pins are used to look at the normal outputs of the continuous time filter or AGC output. These pins may also be driven with DP/DN like signals for back end testing.
TPD,$\overline{\text{TPD}}$	AO	TEST PINS: Emitter output test points similar to TPA and $\overline{\text{TPA}}$. These pins are used to look at the differentiated output of the continuous time filter or AGC output. These pins may also be driven with CP/CN like signals for back end testing.
TPE	AO	TEST PIN: Emitter output test points similar to TPA. This pin is used to look at the AGC timing signals.
VRC	AO	VRC Reference Voltage: The ATO reference voltage (VPA - 2.3 V) is output on this pin.
ATO	AO	ANALOG TEST OUT: This test point output provides a monitor of the DAC outputs. When enabled by the ATOEN bit in the PD Register, the last DAC written to by the serial control register is the DAC monitored. Signal at ATO is referenced to VRC/2.

ANALOG CONTROL PINS

BYPD	C	The data AGC integrating capacitor, CBYPD, is connected between BYPD and VPA. This pin is used in non-servo mode (SG = 0).
BYPS	C	The servo AGC integrating capacitor, CBYPS, is connected between BYPS and VPA. This pin is used when in servo read mode (SG = 1).
FLTR1, $\overline{\text{FLTR1}}$	C	TBG PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components.
FLTR2, $\overline{\text{FLTR2}}$	C	DS PLL LOOP FILTER: Differential connection points for the data separator PLL loop filter capacitor.
RR	C	CURRENT REFERENCE RESISTOR INPUT: An external 13.7 kΩ 1% resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and the time base generator DACs.
RX	C	FILTER REFERENCE RESISTOR INPUT: An external 15.8 kΩ 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter DACs.

PIN DESCRIPTION (continued)

DIGITAL INPUT PINS

NAME	TYPE	DESCRIPTION
LOWZ	DI	LOW-Z MODE INPUT: TTL compatible control pin which, when pulled high, the input impedance is reduced to allow rapid recovery of the input coupling capacitors. When pulled low, keeps the AGC amplifier and filter input impedance high. An open pin is a logic low.
FASTREC	DI	FAST RECOVERY: TTL compatible control pin which, when pulled high, puts the AGC charge pump in the fast decay mode. An open pin is a logic low.
$\overline{\text{HOLD}}$	DI	AGC HOLD CONTROL INPUT: TTL compatible control pin which, when pulled low, holds the AGC amplifier gain constant by turning off the AGC charge pump. The AGC loop is active when this pin is high. An open pin is a logic high.
$\overline{\text{PWRDN}}$	DI	POWER DOWN CONTROL: TTL compatible power control pin. When low the selected circuitry in the PD Register is shut down. This pin should be set inactive in normal operating mode. There is no default value for this pin. Must be pulled inactive if not used.
FREF	DI	REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an ac coupled ECL signal. When the BT bit in the CT2 Register is set, FREF replaces the VCO as the input to the data separator.
WCLK	DI	WRITE CLOCK: TTL compatible input that latches in the data at the NRZ interface on the rising edge. Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. There is no default value for this pin.
RG	DI	read gate: TTL compatible input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the read sequence. A low level selects the time base generator output. There is no default value for this pin.
WG	DI	write gate: TTL compatible input that, when pulled high, enables the write mode. There is no default value for this pin.
SG	DI	servo gate: TTL compatible input that, when pulled high, enables the servo read mode. There is no default value for this pin.
RDT	DI	READ DATA: A TTL or ac coupled PECL compatible input to the data separator back end, for testing purposes only. This pin is controlled by the RDT bit in the CT1 Register.

DIGITAL BIDIRECTIONAL PINS

NRZ0-7	DI/O	BYTE WIDE NRZ DATA PORT: TTL compatible bi-directional input/output. Input to the encoder when WG is high. Output from the decoder when RG is high.

DIGITAL OUTPUT PINS

NAME	TYPE	DESCRIPTION
RCLK	DO	READ REFERENCE CLOCK: A multiplexed clock source used by the controller. When RG is low, RCLK is synchronized to the time base generator output, F_{TBG}. When RG goes high, RCLK remains synchronized to F_{TBG} until the SFC is reached. At that time, RCLK is synchronized to the data separator VCO. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. TTL output levels.
$\overline{SBD}$	DO	SYNC BYTE DETECT: Transitions low upon detection of sync byte. This transition is synchronized to the sync byte. Once it transitions low, $\overline{SBD}$ remains low until RG goes low, at which point it returns high. CMOS output.
DLYCCLKP, DLYCCLKN	DO	DELAYED CODE CLOCK: Differential PECL outputs of the code rate write data clock. These outputs are synchronized to the WD/$\overline{WD}$ outputs and can be delayed with respect to the data with the WCP[7:4] register bits. The rising edge of the clock can also be pre-compensated with the WPC[3:0] Register bits.
WD, $\overline{WD}$	DO	WRITE DATA: Write data flip-flop output. The data is automatically re-synchronized (independent of the delay between RCLK and WCLK) to the reference clock FTBG, except in direct write mode. Differential PECL output levels.
$\overline{RDS}$	DO	SERVO READ DATA: Read data pulse output for servo read data. Active low CMOS output. Output active when SG is high, and high when SG is low.
PPOL	DO	SERVO READ DATA POLARITY: Read data pulse polarity output for servo read data. Active high CMOS output. Negative pulse = low, positive pulse = high. Output active when SG is high.
SBDEF	DO	SYNC BYTE DEFECT: Output active when the sync byte pattern is not detected within 48 bytes after SFC. This pin is reset on the next RG rising edge. Active high CMOS output.
RMB	DO	RESYNC MISSING BYTE: Output is asserted high each time the resync pattern is undetected in a resync window. CMOS output.
CONTDEF	DO	CONTROLLER DEFECT: Controller interrupt output. See functional description. Active low CMOS output.
COAST	DO	COAST: Output is high when the PLL and AGC are in coast mode as programmed in the CST1 and CST2 Register locations. CMOS output.
DIGTP	DO	DIGITAL TEST POINT: Internal ENDEC signals can be muxed to this output as a function of the CT1:[6] and CT2:[0] Register bits. CMOS output.

PIN DESCRIPTION (continued)

SERIAL PORT PINS

NAME	TYPE	DESCRIPTION
SCLK	DI	SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. TTL input levels.
SDATA	DI/O	SERIAL DATA: Input pin for serial data; 8 address bits first followed by 8 data bits. The address and data bits are entered LSB first, MSB last. TTL input levels.
SDEN	DI	SERIAL DATA ENABLE: A high level input enables data loading. The data is internally parallel latched when this input goes low. TTL input levels.
$\overline{\text{POR}}$	DI	POWER ON RESET: A low level input resets the Serial Port Registers to their initial values. Internal logic circuits of the part are also intialized. An open pin is a logic high. TTL input levels.

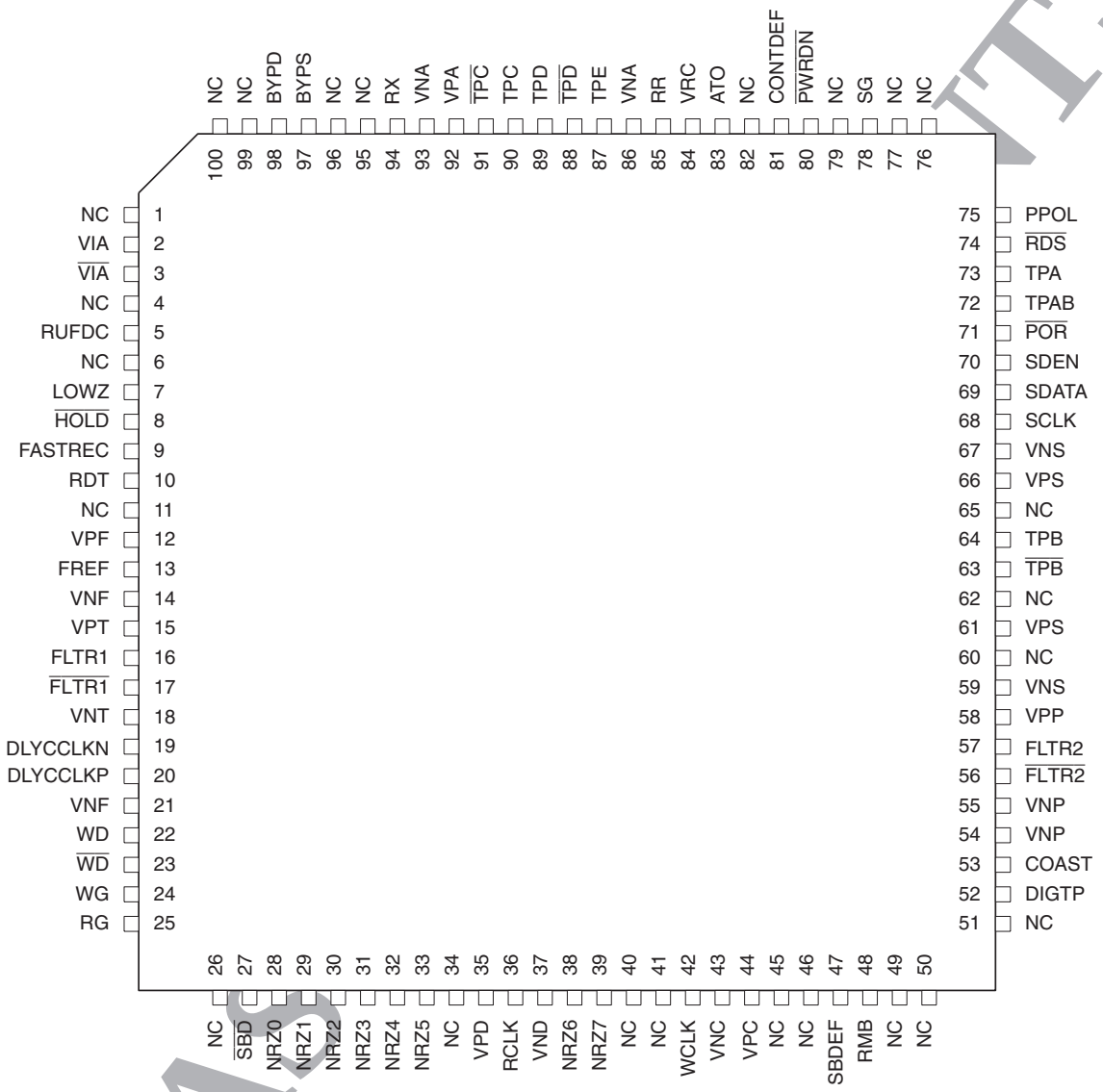
TABLE 10: 1,7 RLL Decode Table

ENCODED BIT DATA							DECODED NRZ DATA	
Previous		Present			Next			
Y	Y	Y	Y	Y	Y	Y	D	D
2	3	1	2	3	1	2	1	2
0	0	0	0	0	X	X	0	1
1	0	0	0	0	X	X	0	0
0	1	0	0	0	X	X	0	1
X	X	1	0	0	X	X	1	1
X	0	0	1	0	0	0	1	1
X	0	0	1	0	1	0	1	0
X	0	0	1	0	0	1	1	0
X	1	0	1	0	0	0	0	1
X	1	0	1	0	1	0	0	0
X	1	0	1	0	0	1	0	0
0	0	0	0	1	X	X	0	1
1	0	0	0	1	X	X	0	0
0	1	0	0	1	X	X	0	0
X	X	1	0	1	X	X	1	0

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

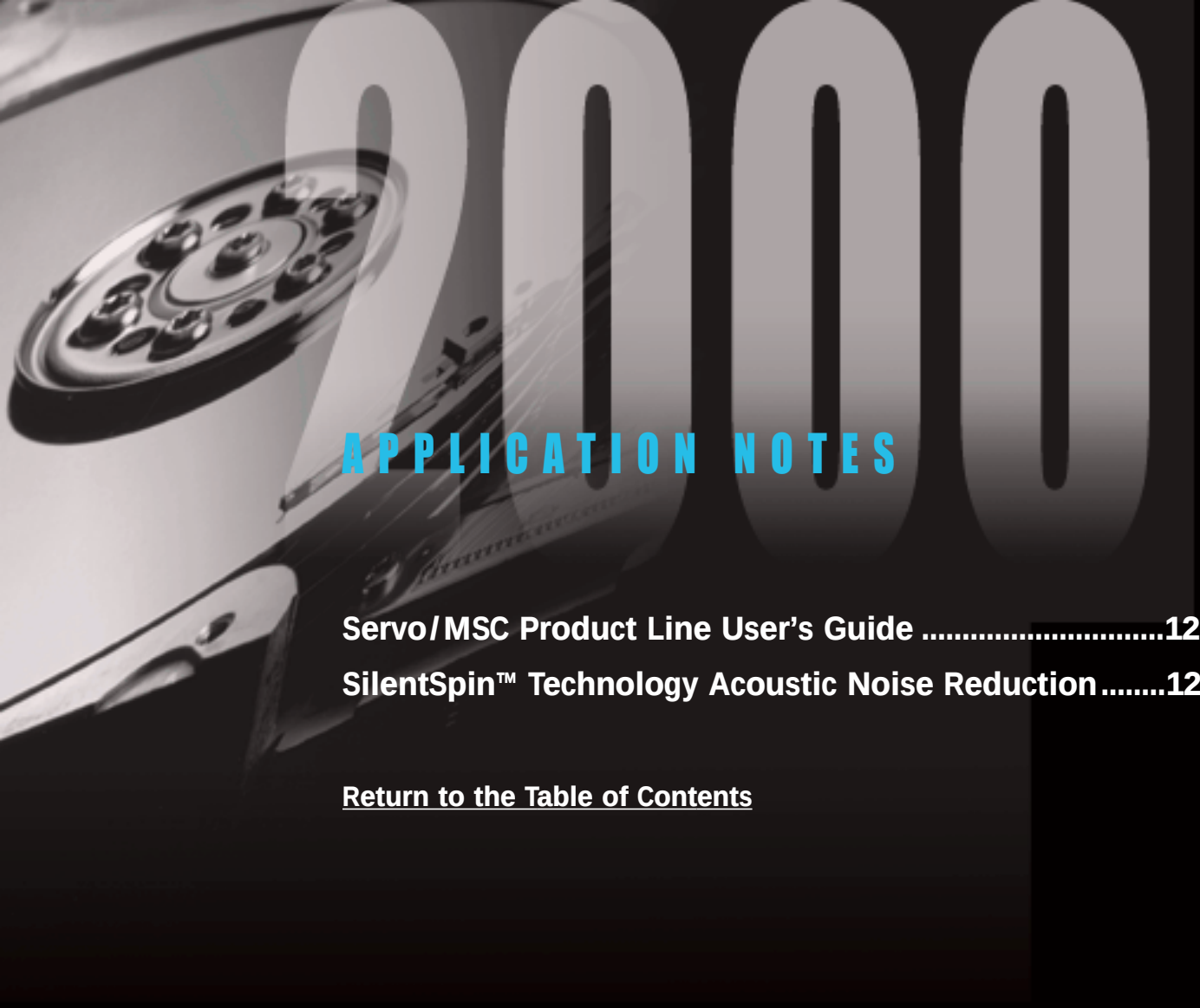


100-Lead Power TQFP

Preproduction: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Sale of the product described above is made subject to the terms and conditions of sale supplied at the time of order acknowledgment, as well as this notice and the notice contained in the front of the Texas Instruments Storage Products Group Data Book. Buyer is advised to obtain the most current information about TI's products before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914



2000

APPLICATION NOTES

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Texas Instruments

Abridged Version

TEXAS INSTRUMENTS

Servo/MSC Product Line User's Guide

August 1997

INTRODUCTION

As a major supplier of Mixed Signal Integrated Circuits (MSICs) to the Hard Disk Drive (HDD) industry, Silicon Systems, Inc. produces a wide range of products that are used to implement many of the functions required to produce a modern disk drive in today's market. Since the functions required are very disparate in nature these products are broken into product lines that specialize in the design and production of an IC that implements a specific set of functions as required by the customer. One such product line is the Servo/Motor Speed Control product line which produces the circuits that control the physical plant of the HDD, those parts that cause motion in the drive for the purposes of spinning the disks of magnetic recording media and positioning the recording and read heads. This document supplies the information necessary for a customer to know to understand the technology that Silicon Systems applies to this product line and the architectures that result in the ICs that result from that technology.

The pin and functional names used in this document can vary from product-to-product. This document is written to be general in nature. Specific implementations may vary substantially and the user must keep this in mind when applying any product from Silicon Systems' Servo/MSC product line.

PRODUCT LINE DEFINITIONS

SERVO DEMODULATORS

Products that provide the circuits necessary to interface to the read channel of the disk drive to digitize the analog servo burst information for use by the digital servo compensator to use in calculating on-track information.

SERVO/SPINDLE CONTROLLER COMBINATIONS

Products that combine Voice Coil Motor (VCM) control and Spindle Motor Speed Control (MSC) functions in a single MSIC. Voice Coil Motor controllers provide the circuits necessary to control the current through the VCM used to position the heads in the disk drive from track-to-track or hold on-track, also called "positioners". Spindle Motor Speed Controllers provide the circuits necessary to control the three-phase, Hall-sensorless, permanent magnet, DC motors used to spin the magnetic recording media disks in a HDD.

In the past it was common for these functions to reside in separate ICs but today Silicon Systems does not produce any products that do not contain both the positioner and MSC functions in a single IC. In fact these products will often contain circuits for other functions not directly related to head positioning and/or spindle motor control in the IC as well. These parts may be drivers (those with internal power devices) or predrivers (those that control external power devices) and are typically for 5 V or 5 V/12 V applications.

HIGH INTEGRATION

Products that provide a higher level of value to the customer by the integration of system functions into a single IC. One example of this is that servo demodulators are typically standalone although many of SSI's read channel products have integrated this function into that product line. One product in particular, the SSI 32H6840, integrates the demodulator with the Servo/Spindle controller combination along with a 'C25 compatible DSP and other ASIC-like functions to implement a complete HDD plant control system on a single IC. This provides the customer with a single chip solution to the servo and spindle control system.

PRODUCT LINE DEFINITIONS (continued)

POWER DRIVER ARRAYS

Products that contain the power FETs used to drive the motor currents in conjunction with a predriver servo/spindle controller. Typically these are used in high performance applications requiring large currents to be controlled. In Class AB positioners the power driver array will contain a “sense FET” used to feedback voltage threshold information to the predriver circuit in order to prevent shoot-through currents while giving optimal performance. Due to the power handling requirements of the power driver array the packaging used is optimized for desirable thermal characteristics.

DISK DRIVE SYSTEMS

The disk drive system contains many systems all acting together to accomplish the goal of getting data written onto the recording media and read off of the recording media. The arrangement of the various blocks that form a complete disk drive system vary from manufacturer-to-manufacturer and drive-to-drive. Figure 1 is meant to show a generic disk drive block diagram system that might be found in any application, the shaded blocks are those that will be covered by this document.

SERVO DEMODULATOR

Disk drives using a VCM (rotary or linear) require a closed-loop position control system to center the data head over the target track. The control system uses position information indicating actual head position and compares this to the desired position so that a compensating VCM error current can be generated. Figure 2 illustrates the elements making up this control system. The position information usually consists of two parts; coarse position giving track number and fine position information relative to each track and used to center the data head.

Position information is placed on the disk surface in servo frames. Demodulators provide the data acquisition portion of the servo positioning system. By using an analog-to-digital converter (ADC) to translate analog servo burst information into a digital format it is possible to implement a digital control system based on information taken from the surface of the recording media. There are two basic types of servo systems implemented in HDD, dedicated and embedded servo. Dedicated servo systems reserve an entire data surface for the position information. Embedded servo systems interleave position information with user data. Servo demodulators decode the fine position information encoded in each servo frame.

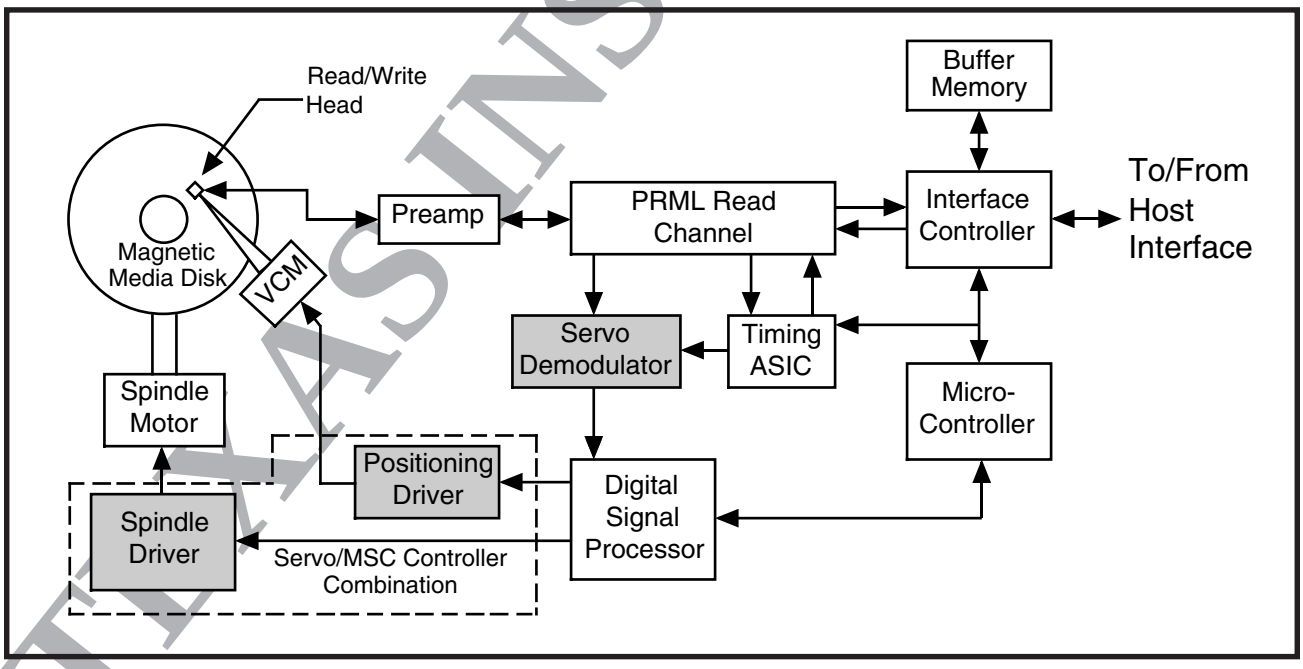


FIGURE 1: Generic Disk Drive System

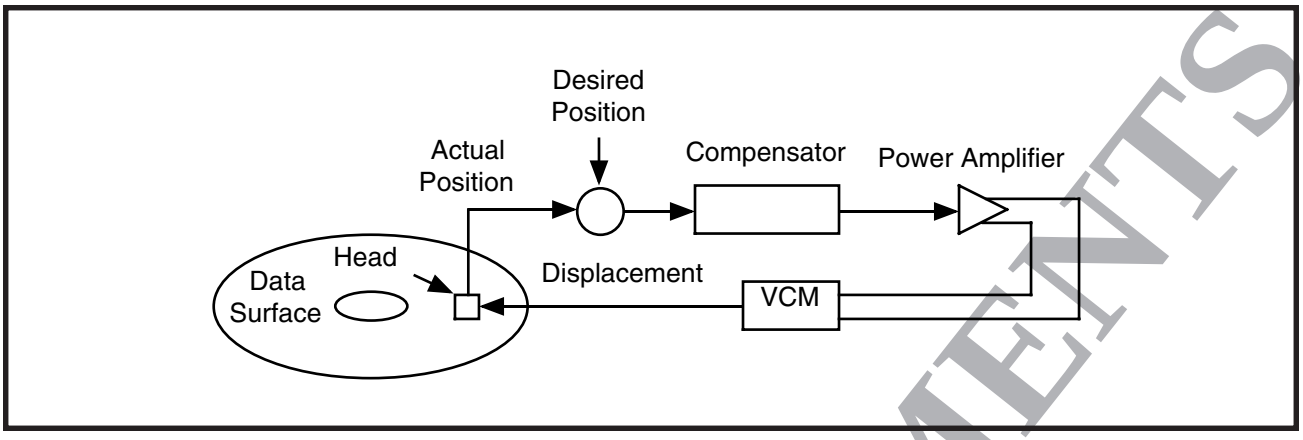


FIGURE 2: Closed-Loop Position Control System

Dedicated servo uses one entire side of a disk to record servo pattern information that is used by the system to make on-track decisions for all other disk surfaces in the drive. The advantage of this technique is that the servo patterns are continuous around an entire revolution of the disk and so an analog, continuous time servo system can be designed that avoids the sample rate and bandwidth limitations of any digitally sampled system. The disadvantages of this system are the consumption of an entire disk surface for only servo data and the mechanical offsets that exist between the heads on the dedicated surface and the data surface that will change with age and temperature causing positioning inaccuracies. In modern HDD systems it is rare to find dedicated servo in actual use.

An embedded servo system places the servo burst information (and other information as well) between sectors of user data on each disk surface and uses the actual data read head as the sensor for the position information in order to provide the feedback to the positioning system. This system only receives position information when a servo wedge is read and so this becomes a digitally sampled system which lends itself well to digital servo system implementation albeit with the sample rate and bandwidth issues inherent in any sampled system. This is the servo system of choice in today's HDD systems.

VCM CONTROL SYSTEM

The VCM control system directs current into and out of the VCM that positions the heads in the application. At its most basic the system must be able to move the heads towards both the inner and outer diameters of the drive. This requires the ability to be able to move the current in two directions through the VCM. This is accomplished by the use of an H-bridge arrangement of power devices as shown in Figure 3. By selectively turning on the power devices in combination the current through the VCM can be controlled as to direction and amount. A requirement for the bridge is that no two devices in the same leg (direct path from positive supply to common) can be energized at the same time to prevent a totem-pole condition from existing that can be destructive to the power devices.

Typically the VCM control system is set up so that a voltage input (from a digital-to-analog converter) is used to control the current through the motor, in an arrangement called a "transconductance amplifier." This is shown in Figure 4 as it might be applied to any typical HDD.

SPINDLE CONTROL SYSTEM

Silicon Systems' motor speed control or MSC circuits are responsible for commutating DC, brushless, three phase motors. In a hard-disk drive, this motor is the spindle motor which is responsible for rotating the platters at a fixed and precise speed. The MSC system provides the circuits necessary to start a motor, commutate the motor drivers to spin the motor smoothly, regulate speed, and drive current through the motor windings. Figure 5 shows a spindle motor control system block diagram.

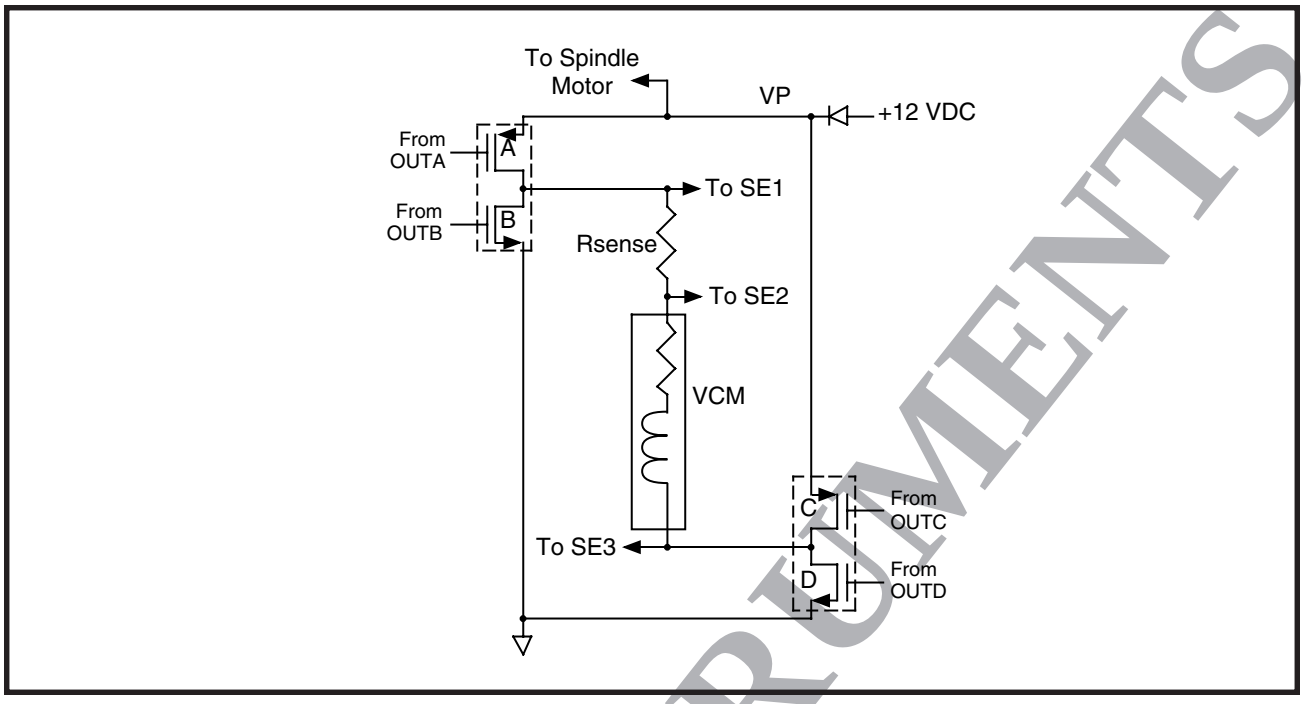


FIGURE 3: H-Bridge Power Amplifier

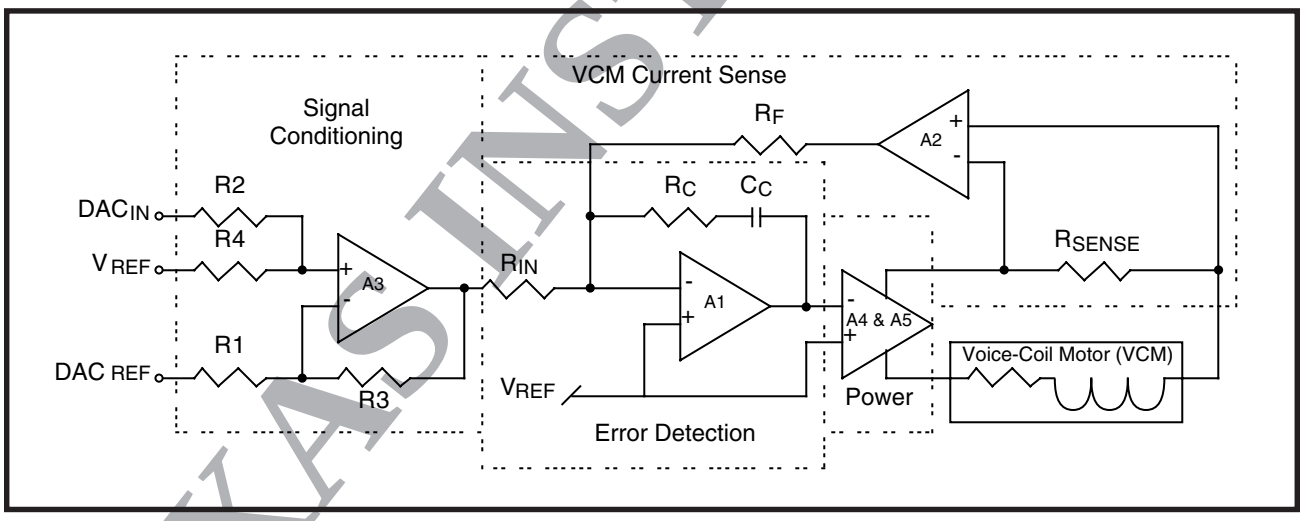


FIGURE 4: Transconductance Amplifier

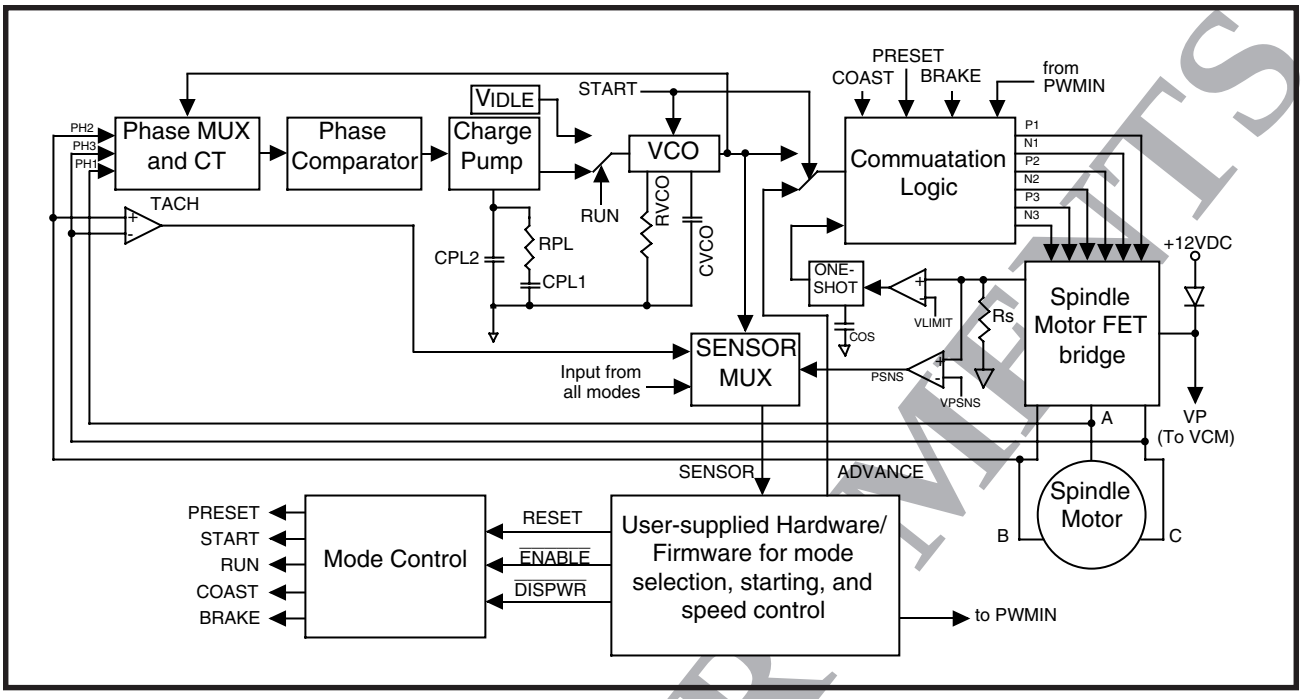


FIGURE 5: Spindle Motor Control System Block Diagram

SPINDLE CONTROL SYSTEM (continued)

Motor commutation is the act of driving current through the motor windings in such a way as to sustain a desired rotational direction. Commutation traditionally has been implemented by placing some kind of sensor on the motor shaft. Hall effect sensors are an ideal device to place in the motor to sense absolute rotor position. For a three phase motor, three Hall sensors may be used to directly decode the next motor commutation state. Hall sensors offer a closed-loop method of absolutely determining the rotor position and to properly commutate the motor under all speed conditions.

Hall sensors burden the motor design, particularly small motors, with the need to place the sensors in the motor and the extra wires for the Hall bias and output. An alternative to Hall effect sensors is to electronically detect the rotor position by examining the back-electromotive-force or bemf generated by a rotating motor. This Hall-sensorless method eliminates the need for Hall sensors to be mounted in the motor and simplifies the motor wiring and has become the technique of choice in today's HDD market.

PREDRIVER VERSUS DRIVERS

A predriver product requires external power MOSFETs. These power MOSFETs directly connect to the motor and deliver current typically in the multiple ampere range. The predriver translates the commutation state and motor current command into signal levels which are connected directly to the gates of the external power MOSFETs. There are three pairs of control output signals used for the spindle predriver, each pair consists of one signal intended for a lower N channel and one for an upper P channel MOSFET and two pair of outputs for the VCM predriver.

An integrated MSC circuit includes power MOSFETs within its package. Such a device has three pins identified as A, B, and C which in turn directly connect to the spindle motor and two pins identified as SE1 and SE3 that directly connect to the VCM. The integrated power devices from Silicon Systems use a stacked NFET arrangement which eliminates the need for a blocking diode when implementing bemf rectification during retraction upon power failure.

SilentSpin™ Technology
Acoustic Noise Reduction

APPLICATION NOTE

March 1997

INTRODUCTION

Two of Silicon Systems' HDD Head Positioning/Motor Control products, the 32H6826 and 32H6840, implement a method of commutating the spindle motor of a HDD that minimizes commutation frequency-related acoustic noise called SilentSpin™. The function of this applications note is to provide the reader with information regarding the theory of the SilentSpin™ technology. It will provide the user some insight into the physical system of the spindle motor with which to develop some understanding of how SilentSpin™ works and why it improves the acoustic performance of the mechanical HDD. Although only two parts have SilentSpin™ currently, it is foreseen that future parts using this technology could be produced with different architectures in which the theory of operation would remain the same but the implementation of SilentSpin™ may appear to be very different.

REFERENCE APPLICATION NOTES

This application note focuses on the theory of SilentSpin™ commutation and only references the current implementation of SilentSpin™ as demonstrated by the 32H6826 and 32H6840 products as required. The techniques of controlling a 3-ø, brushless, DC, permanent magnet, synchronous motor are covered extensively in the applications notes Sensorless Motor Speed Control and 32H682X Sensorless PWM Spindle/Servo Predrivers and it is assumed that the reader is familiar with the material covered in these documents and that they will be available to the reader for referral throughout this document. A further applications note that may have impact for the reader regarding other portions of the 32H6826 and 32H6840 products not referred to in this document is Servo Controllers and Motor Drivers as well as the Product Data Sheets for these two products. Due to the high level of integration of the 32H6840 there are further materials related to the operation of that device that are not referred to in this document but may be of use to the reader in applying that specific product.

HISTORICAL PERSPECTIVE

The HDD industry tends to use 3-ø, brushless, DC, permanent magnet, synchronous motors for the purpose of spinning the recording media disks. These motors are chosen because of the accuracy of the speed of the motor and the small size of assembly as well as attendant cost-related issues. Acoustic noise related to the commutation of such motors has been a continuing problem related to the operation of such motors in the HDD market. This is becoming increasingly important as spin rates increase resulting in more radiated noise as well as with the advent of "green PCs" where reducing the acoustic noise of the entire PC has become a critical concern in the marketing of the product.

Silicon Systems has created a technique for reducing commutation related acoustic noise that results in lowered total radiated noise power and pure tone harmonic specification performance in disk drives. This technique is trademarked as SilentSpin™ and it is the function of this applications note to give the user a basic understanding of the principles that govern spindle motors and the acoustic benefit SilentSpin™ will have on thier behavior. There may or may not be other benefits to the application of SilentSpin™ but this paper will strictly apply to the well documented acoustic benefits of SilentSpin™.

SPINDLE MOTOR THEORY OF OPERATION

The spindle motor is of synchronous type to provide precise speed control in the face of changing inertial and frictional loads. With asynchronous motors the unloaded speed is determined by the frequency of the applied current and the actual speed varies as a function of mechanical load, the difference between the unloaded speed of the motor and the actual speed is called "slip." In order to control the speed of an asynchronous motor in response to a load change it would be necessary to adjust the frequency of the

SPINDLE MOTOR THEORY OF OPERATION (continued)

forcing voltage in closed loop fashion to adjust the speed of the motor. In HDD applications speed control requirements of better than 1% in once-per-mechanical revolution rate are common with 0.1% or better speed regulation accuracy required in high performance drives. Much of the speed regulation accuracy requirements are driven by synchronous read channel technology which allows higher data rate and better arial density as the instantaneous and average speed become more equal and both more accurate. With such stringent requirements for speed control accuracy the use of asynchronous motors in this application is not possible given cost restraints of the market.

Early hard disk drives used Hall-effect sensors to provide feedback to the system indicating the radial position of the spindle motors for purposes of commutation to the next radial state and for speed control applications. This technique added cost and complexity to the system which the HDD manufacturer neither wants nor needs if a better, simpler, and cheaper technique becomes available. Such an improved technique was developed by using the *back electromotive force* (bemf) that the motor generates while spinning to reflect the radial position of the motor and thus provide the commutation advancement and speed control feedback. The transformer action of the spinning permanent magnets and a un-driven winding of the motor's stator make it a useable transducer of radial information from the motor.

Synchronous motors are spun by turning on and off the appropriate FETs of the power bridge in a sequence that provides the correct magnetic field at each radial position to generate maximum torque in order to cause the permanent magnets of the motor rotor to follow the electro-magnetic field as it advances through the motor states. The act of advancing the state of the motor is called *commutation*. The power driver arrangement for synchronous spindle motors is shown in Figure 1 below.

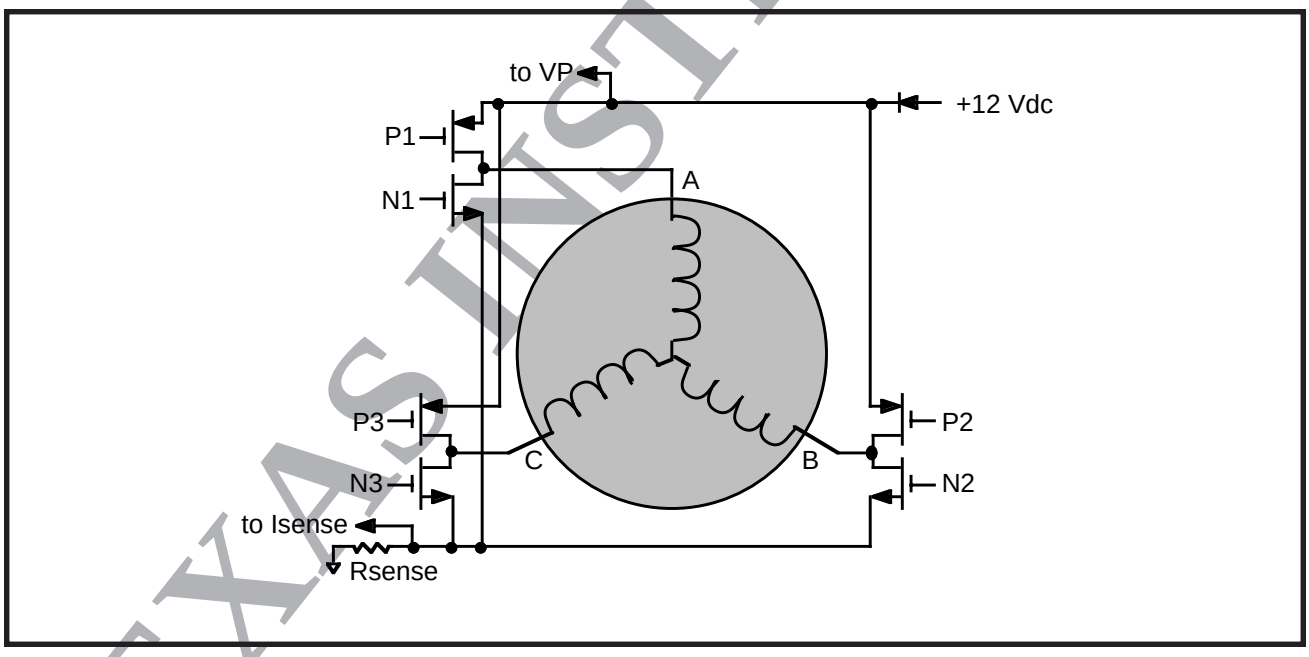


FIGURE 1: Spindle Motor Bridge

At any instant one p-FET and one n-FET are turned on in separate phases resulting in a net magnetic field that is the sum of the fields from the two energized phases (one is sourcing current while the other is sinking current). Both n- and p-FETs are never turned on in the same phase at the same time, this is a condition called *totem-pole* that results in the rapid overheating of the FETs. The remaining phase is un-driven and the voltage at the phase is governed by the bemf generated by the magnetic fields of the rapidly spinning magnets (at run conditions) of the rotor in proximity with the inductors of that phase interacting in classical generator action. It is this bemf that is used to sense rotor position in sensorless systems to provide the angular information necessary for correct commutation of the motor to occur. The switching between states is done as quickly as possible (typically there may be slew rate limiting on the turn-on time of the lower FETs) as there are only three possible conditions for a phase current to be at: +1, 0 (or floating), and -1. The resulting current waveforms (called six-state) related to the commutation of the spindle motor are shown in Figure 2 below.

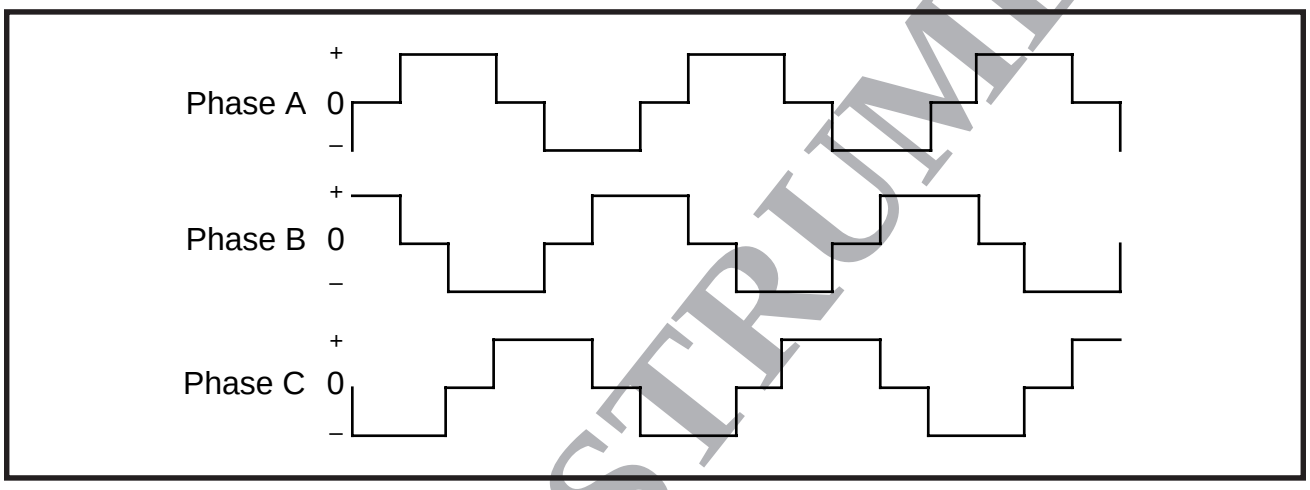


FIGURE 2: Six-State Spindle Motor Current Waveforms

The control of motor speed is implemented by controlling the average amount of current flowing through each leg of the motor (control of the amplitude of the current waveform). The amount of current in an inductor is proportional to the intensity of the magnetic field it generates. This relationship is known as Ampere's Law and is shown in equation form as:

$$H = I \bullet dl$$

Where H - is the magnetic field intensity, I - is the current in the inductor, and *dl* - is length of wire carrying the current. Given a fixed air gap of any motor (area is constant) the flux density is directly proportional to the flux intensity which is in turn directly proportional to the current through the inductance of the coil windings of the motor phase. The force that pushes a magnetic flux through the space of an air gap is called *magnetomotive force* (mmf) and it is this force that the motor will use to generate the torque necessary to cause the mechanical rotation of the rotor around the stator. In a linear system a force applied to a mass will cause a resulting acceleration in a relationship known as Newton's Second Law of Physics which is shown as the familiar equation:

$$F = m \bullet A$$

SPINDLE MOTOR THEORY OF OPERATION (continued)

Where *F* - is the unopposed force applied, *m* is the mass to which the force is applied, and A is the resulting acceleration in the direction of the force. The spindle motor of an HDD is a rotational device and the parameters are defined differently. Torque applied to an inertia causes an angular acceleration:

$$T = j \bullet \alpha$$

Where T - is the torque being applied around the axis of rotation, j is the inertial load of the rotational system, and a is the resulting angular acceleration. The amount of torque per amp of current in the windings of a motor is calculated by:

$$T = K_T \bullet I$$

Where T - is the torque generated, K_T - is the torque constant of the motor whose units are in torque per ampere current (determined by the physical construction of the motor), and I - is the amount of current through the inductor. It is now obvious that the angular acceleration of a motor is governed by the current applied to the motor inductance and that the voltage applied to the motor winding is only important as a forcing function for the current. In order to accelerate the motor apply more voltage to force more current. The control system has a single integration implied by using current to alter acceleration as a method of controlling velocity.

SPECTRAL STUDY OF SIX-STATE WAVEFORMS

The frequency content of standard six-state commutation can be found by deriving a time-domain representation of the signal then applying Fourier analysis to the signal to create a frequency-domain representation as a Taylor-series expansion. The Figure 3 shows the area-under-the-curve to be integrated, setting the equation up to use cosine waves rather than sine waves to allow the use of symmetry to simplify the integration. There are other methods for setting up the calculation that should all result in the same coefficients.

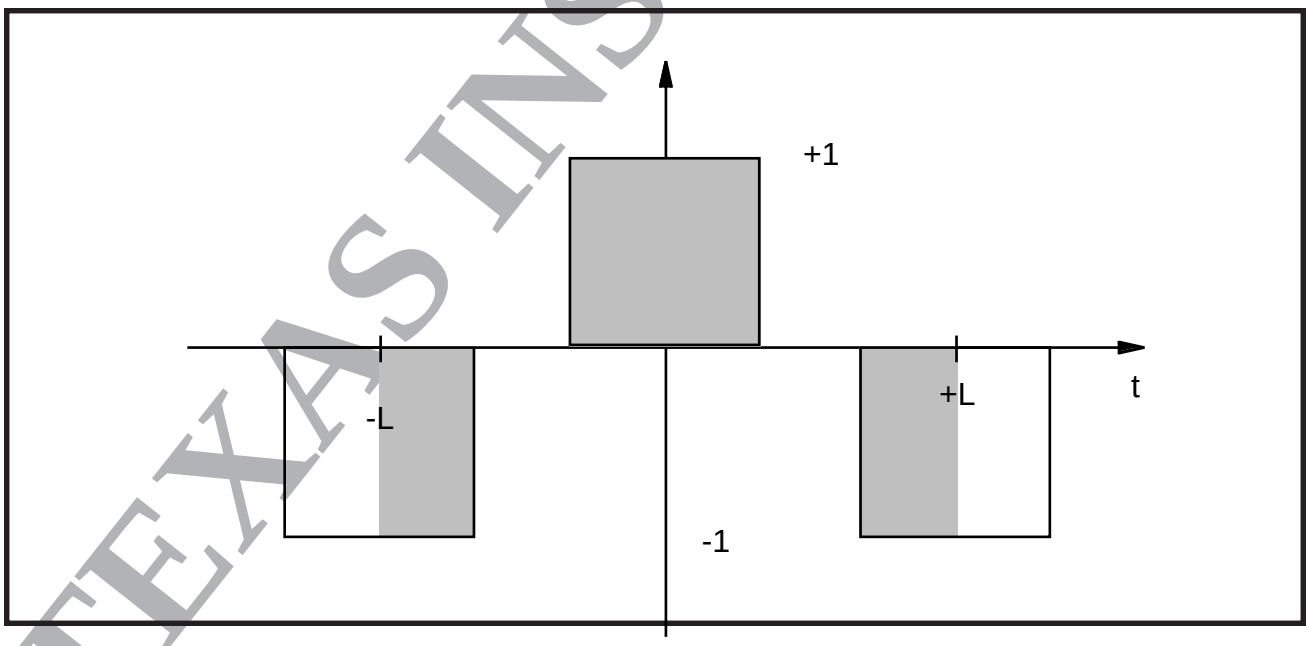


FIGURE 3: Waveform Integration Transformation Setup

Analysis of this setup allows simplification by first canceling out the portions of the waveform from: $-\infty < t \leq -L$ to $L < t < +\infty$ resulting in the following integration for each of the frequency coefficients:

$$Cn = \frac{1}{L}\int_{t=-L}^{L} f(t)\cos\left(\frac{nt\pi}{L}\right)dt \qquad \text{(eq. 1)}$$

Since the area under the full curve is symmetrical around the origin it follows that the total area must equal twice the area from the origin to either integration limit this allows a further simplification to:

$$Cn = \frac{2}{L}\int_{0}^{L} f(t)\cos\left(\frac{nt\pi}{L}\right)dt \qquad \text{(eq. 2)}$$

$$f(t) = \begin{Bmatrix} +1\,for\,0 \leq t < L/3 \\ 0\,for\,L/3 \leq t < 2L/3 \\ -1\,for\,2L/3 \leq t < L \end{Bmatrix}$$

By breaking the integration into its three separate, piece-wise linear parts we can then derive the following equation for the transformation:

$$Cn = \frac{2}{L}\left[\int_{0}^{L/3}(+1)\cos\left(\frac{nt\pi}{L}\right)dt + \int_{L/3}^{2L/3}(0)\cos\left(\frac{nt\pi}{L}\right)d + \int_{2L/3}^{L}(-1)\cos\left(\frac{nt\pi}{L}\right)dx\right] \text{(eq. 3)}$$

By use of a simple u-substitution the equation for the coefficients can be then reduced to:

$$Cn = \frac{2}{n\pi}\left[\sin\left(\frac{4n\pi}{3}\right) + \sin\left(\frac{2n\pi}{3}\right)\right] \qquad \text{(eq. 4)}$$

$$u = \frac{nt\pi}{L}, du = \frac{n\pi}{L}dx, dx = du\frac{L}{n\pi}$$

SPECTRAL STUDY OF SIX-STATE WAVEFORMS (continued)

Figure 4 show a graph of the relative coefficient values as calculated by the results from equation 4 using a 4-pole motor running at 3600 RPM over the range of frequencies from 0 to 10 kHz (a range in the middle of the ability of the human ear to respond to sound. Notice the frequency-rich content spread over the entire range of interest. If a coupling mechanism exists and the HDA structure has a mechanical resonance close to a frequency of a peak then an acoustical “singing” sound will be produced that could represent a significant contribution to the total acoustic output of the drive.

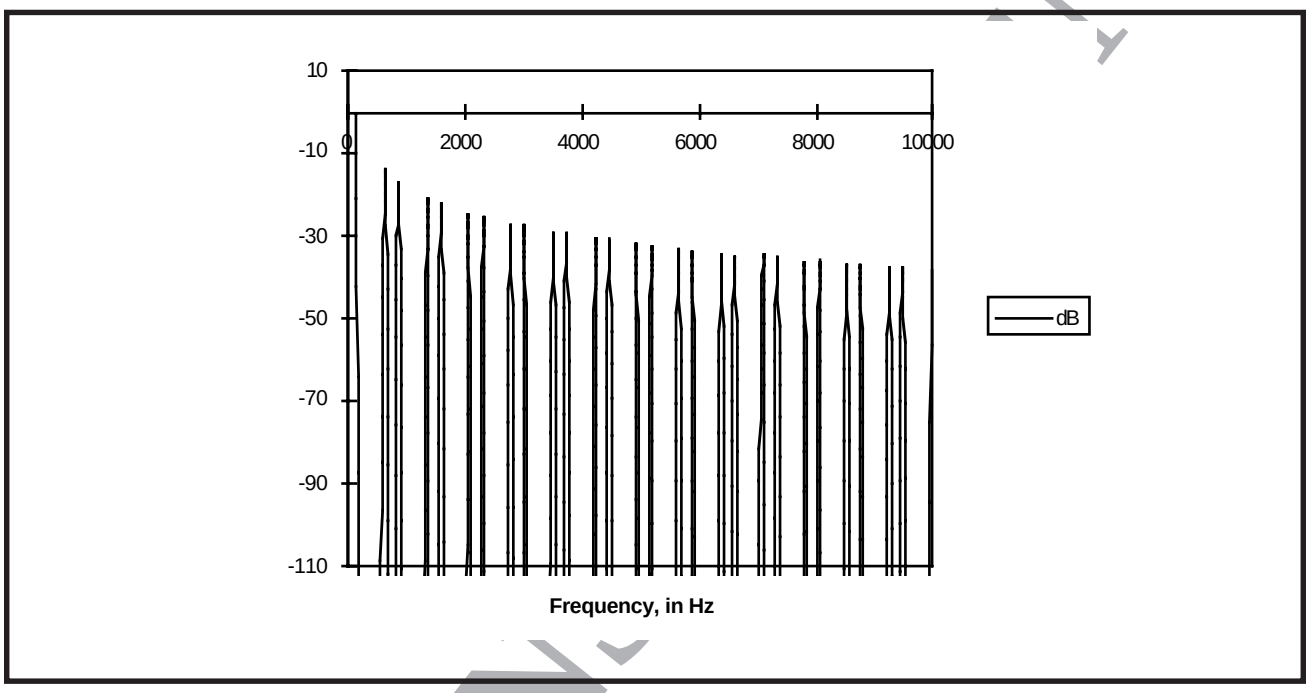


FIGURE 4: Six-State Calculated Current Spectral Analysis

Figure 5 shows the same plot as measured using a current probe around a single motor phase on a 4-pole, 3600 RPM motor in actual operation. Notice that the predicated six-state frequency spectrum closely matches that of the calculated coefficients. All of these frequencies exist in the magnetic flux in the air gap of the motor strictly due to the use of six-state current waveforms in the act of commutating the motor. A wide acoustic spectrum is difficult to minimize using mechanical baffling, cancellation, and absorption techniques for acoustic noise reduction. If the current harmonics are limited to a much narrower range of frequencies that can be mathematically predicted by the mechanical parameters of the motor and its speed then the act of using mechanical means to eliminate acoustic noise is substantially simplified and could be addressed early in the design stage of the mechanical assembly.

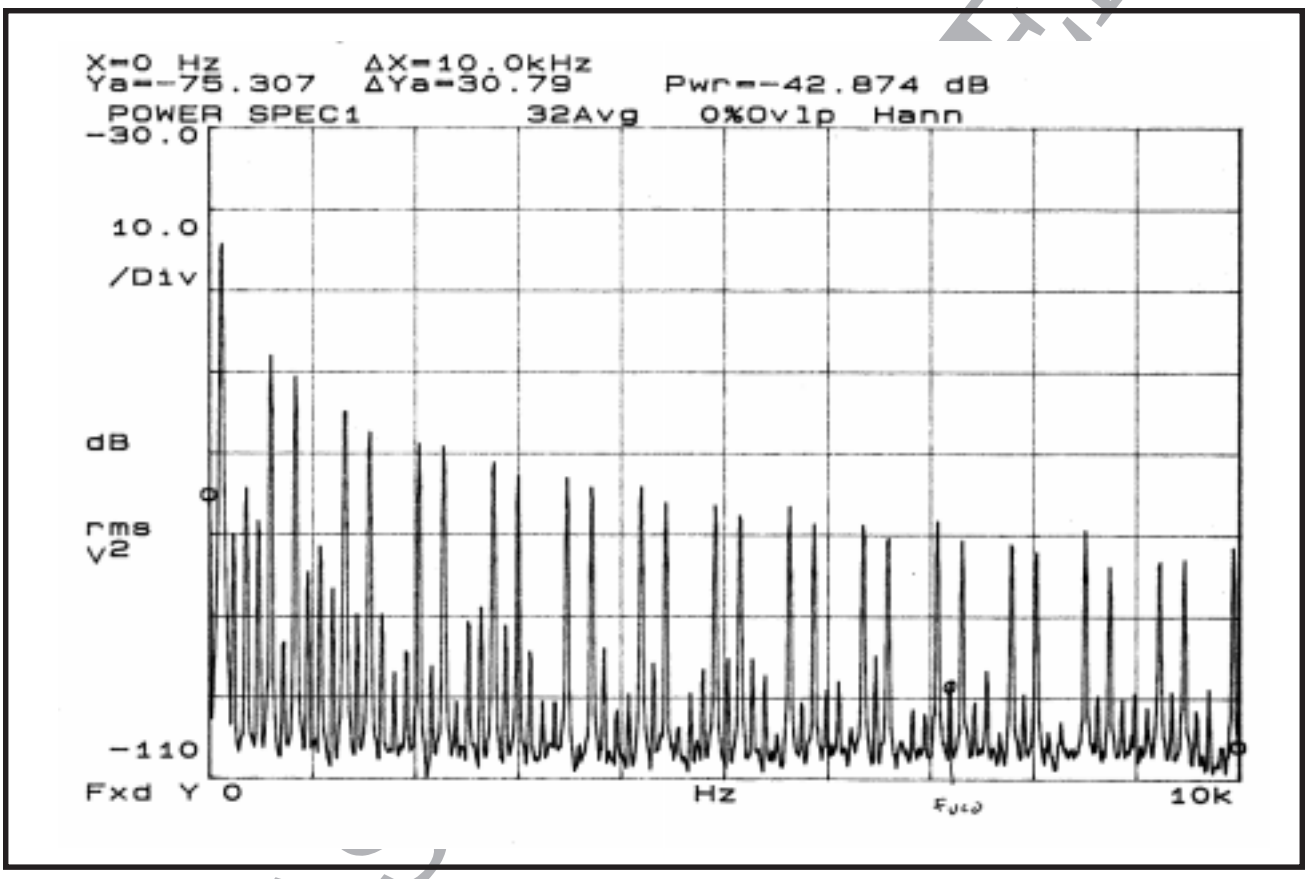


FIGURE 5: Six-State Measured Current Spectral Analysis

SPECTRAL STUDY OF SIX-STATE WAVEFORMS (continued)

Notice that the calculated graph (Figure 4) shows none of the even order harmonics that are shown in the measured spectrum (Figure 5). These come from a variety of sources not included in the simple model of the current waveform shown in Figure 2. In reality there exists a few reasons that the fundamental frequency of the electrical revolution rate is distorted to produce these even order harmonics. If the model was improved to include more of these real world phenomena then the spectrum calculated should more closely match that measured by use of the current probe. It is interesting to note that none of the measured even order harmonics come close to the amplitude of the odd order ones from the commutation of the motor. This implies that these even order harmonics are not significant contributors to acoustic noise specifications for the HDA.

One reason is that the calculated coefficient for the fundamental frequency is greater than 1 (about 1.102). If the power driver is not capable of providing the extra overhead then the fundamental is clipped and this type of distortion produces even order harmonics. Perfectly sharp-edged waveforms of the mathematics do not include real-world slew rate limiting from the FETs, RL effects of the motor, and any slew rate limiting included in the IC.

SILENTSPIN™ ACOUSTIC NOISE REDUCTION EXPLAINED

The implications of Ampere's Law are such that the frequencies of the current through the inductor are present as the frequencies in the magnetic field in the air gap of the motor. If the current waveform of the motor winding thus contains harmonics of the fundamental commutation frequency that content is also represented in the magnetic field. From a text entitled "ELECTRIC MACHINES," (Mulukutla S. Sarma, 1985) the following quote; "Harmonic fluxes, besides causing harmonics in induced emf, produce secondary effects in the energy-conversion process itself, and develop undesirable *parasitic torques* that may become responsible for vibration and noise." Thus the harmonics of the commutation frequency represent energy that is not needed to spin the motor. These torques are parasitic in nature and at any instant the actual torque applied is a combination of the fundamental frequency (necessary for torque generation) and the harmonic content which varies from instant-to-instant in the time domain causing "torque ripple" (which is not necessary for torque generation).

Torque ripple causes the acceleration of the motor to not be constant, widening the deviation of instantaneous angular velocity from the mean, which may have a negative impact in the stability of the speed control system. Further, an axial force can be applied to the rotor by the force generated by the magnetic fields of the air gap containing radial and axial components due to physical misalignments between the magnetic fields of the permanent magnets in the rotor and the electromagnets of the stator coils. This axial force can cause displacement of the disks or, if constrained by a mechanical system of some kind, a stress force can be applied to the mechanical HDA.

If there is a mechanical resonance in the HDA that is close to one of the frequencies contained in the stressing force then an audible noise results that can adversely affect the acoustic noise performance of the drive. In particular this resonance sounds like a high pitched "singing" sound that can show up in the total noise power testing and is particularly evident in the pure tone harmonic testing. In order to eliminate the harmonic content from the magnetic flux it is only necessary to provide a single frequency current waveform. A single or "pure" frequency is defined as a sinusoid and its frequency spectrum is a single impulse in the frequency domain at the electrical revolution rate of the drive. Figure 6 shows the motor current waveform for the 4-pole 3600 RPM drive during run conditions. Notice the roughly sinusoidal shape (PWM and slight phase-to-phase motor imbalances are mostly responsible for the distortion.

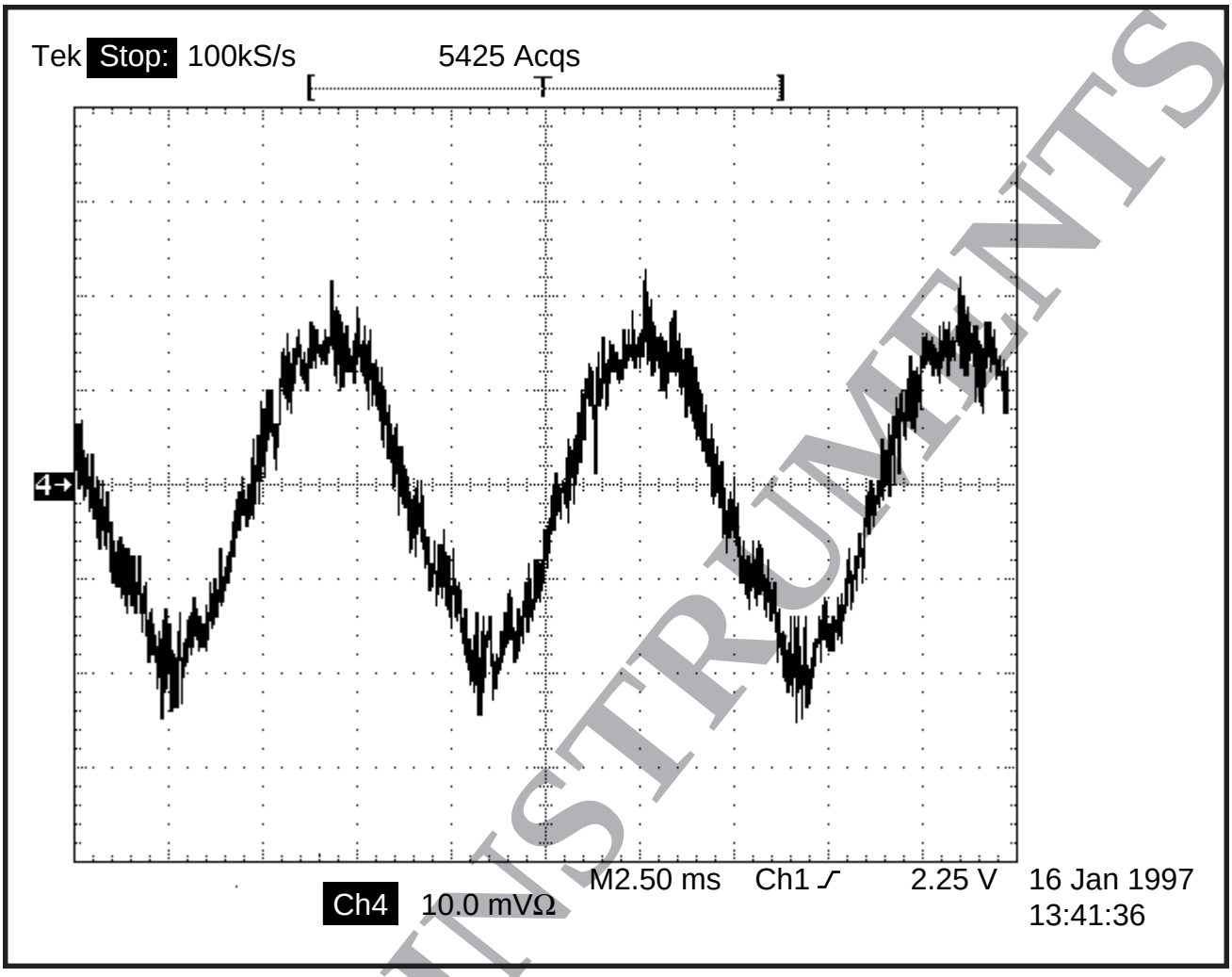


FIGURE 6: SilentSpin™ Single Phase Motor Current

The elimination of the extraneous frequency content of the commutation waveform may have the potential to improve the efficiency of the system a slight amount due to the Conservation of Energy. If the total energy delivered to the system is constant but the odd order harmonics are reduced then the energy contained by the fundamental frequency must be increased. Another way of saying this is that if the fundamental frequency is the one that delivers the energy for commutation (the power delivered by the odd order harmonics is parasitic) then the elimination of the power contained in the odd order harmonics should result in the same performance in spin rate with less total power delivered to the motor.

SILENTSPIN™ ACOUSTIC NOISE REDUCTION EXPLAINED (continued)

Figure 7 shows a measured spectral analysis of the SilentSpin™ current waveform. Note that the odd order harmonics that dominated the six-state spectrum are practically eliminated except two that are related to the digitization rate and step-size of the sine wave generated. This is related to the error function of any digitally synthesized sinusoidal waveform and will exist in the application. It is a much easier mechanical engineering task to delta with this one set of peaks. They are closely spaced, higher in the audible range, and their location will be at the commutation state advance rate separated by the electrical revolution rate of the motor.

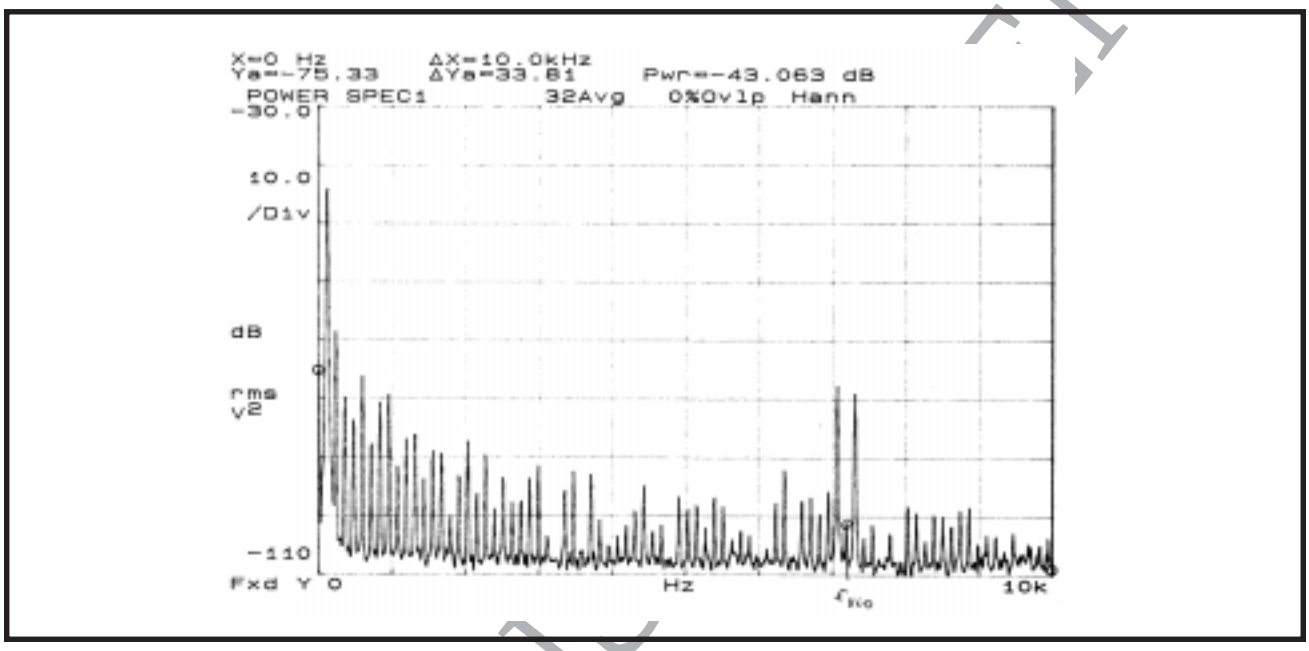
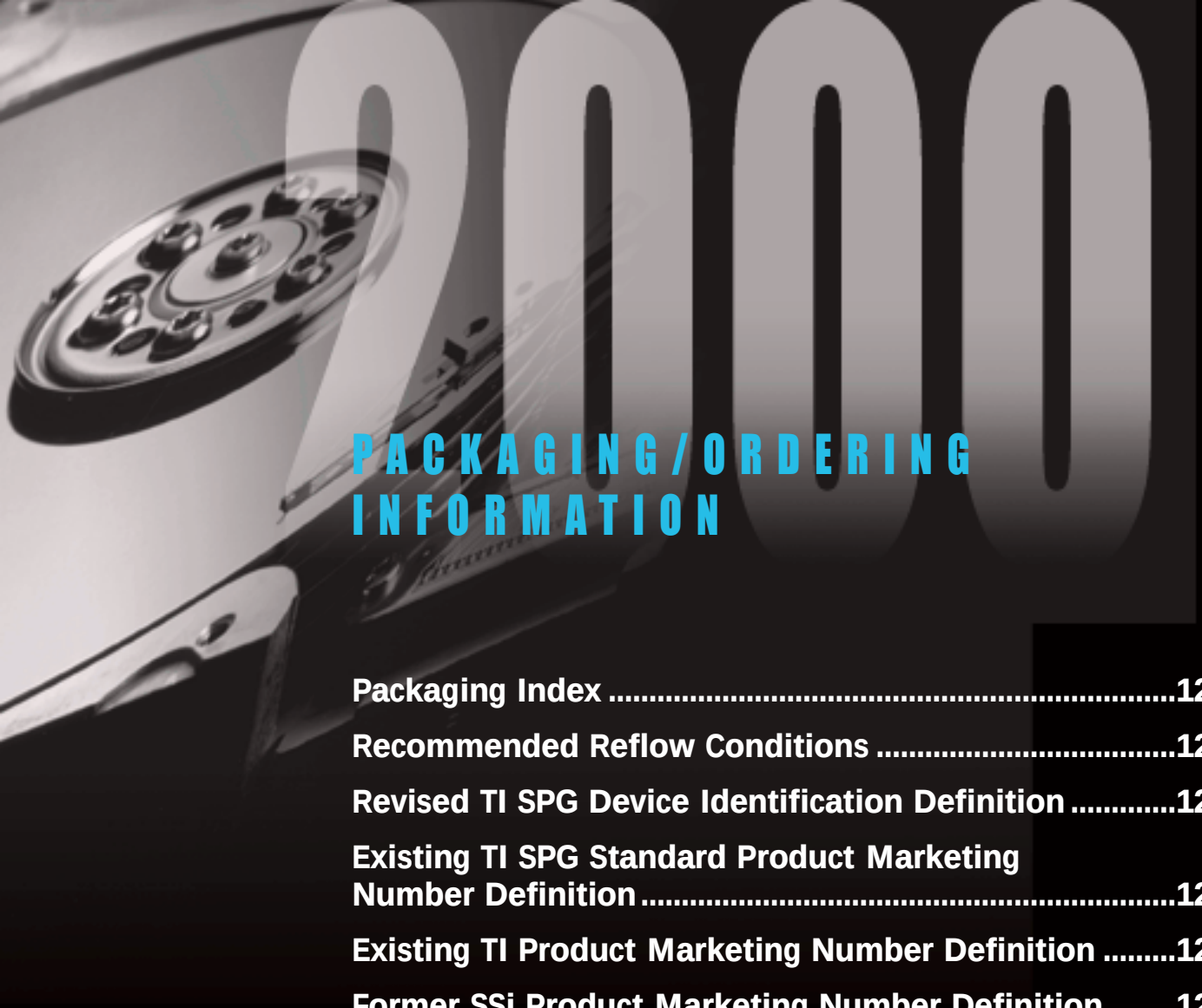


FIGURE 7: SilentSpin™ Measured Current Spectral Analysis

The use of SilentSpin™ eliminates all of the useless odd order commutation frequency harmonics without sacrificing performance. The potential exists to give 0.2 dB to over 6 dB in improvement (as measured in two years of testing HDAs at Silicon Systems) if there are the right mechanical coupling and resonance mechanisms in place. Even acoustically quiet drives can experience a reduction in pure tones of up to 10 dB when utilizing SilentSpin™ to eliminate those harmonics inherent in six-state commutation waveforms.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914



PACKAGING/ORDERING INFORMATION

Return to the Table of Contents

Texas Instruments Storage Products
Packaging Index

Standard Package

Package Type	Package Terminology	TI Package Code
SOP/ SOIC	Small-Outline Package/ Small-Outline Integrated Chip	D, DW,
SSOP	Shrink Small-Outline Package	DB, DBQ, DBY, DL
TSSOP	Thin Shrink Small-Outline Package	DA, DBT, DGG, PW
LQFP	Low Profile Quad Flat Package	VF, PM, PN, PT, PZ, PGF
TQFP	Thin Quad Flat Package	PAG, PFB, PFC, PZT

Power Pad Package

Package Type	Package Terminology	TI Package Code
HTSSOP	Thermally Enhanced Thin Shrink Small-Outline Package	DCA, DCP, PWP
HTQFP	Thermally Enhanced Thin Quad Flat Pack	PAP, PFD, PFP, PHP, PJD, PZP

Texas Instruments Storage Products
SPG Packaging Database

Standard Package

Package Type	Pins	Page No.
SOP/ SOIC	8D, 14D, 16D, 16DW , 20DW 24DW, 28DW	
SSOP	8DB, 14DB, 16DB, 20DB, 24DB, 28DB, 30DB, 38DB, 24DBY, 28DL 48DL, 56DL , 16DBQ, 20DBQ, 24DBQ	
TSSOP	28DBT, 30DBT, 38DBT, 44DBT, 14PW, 16PW, 20PW, 24PW, 28PW, 48DGG, 56DGG,	
LQFP	32VF, 48PT, 64PM, 80PN, 100PZ, 176PGF	
TQFP	48PFB, 64PAG, 80PFC, 100PZT	

Power Pad Package

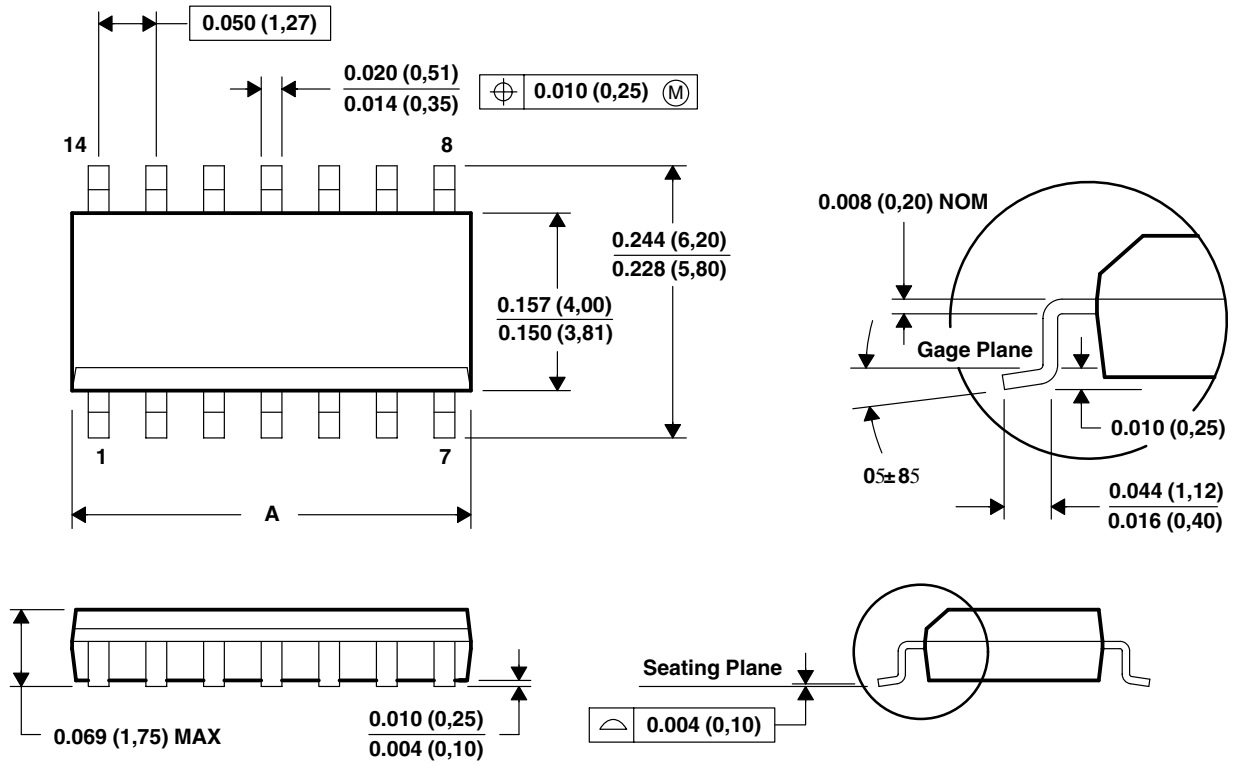
Package Type	Pins	Page No.
HTSSOP	16PWP, 20PWP, 24PWP, 38DCP 56DCA,	
HTQFP	48PHP, 64PAP, 80PFP, 100PZP, 100PFD	

Package Outline Drawing

SOP/SOIC (8D, 14D, 16D)

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

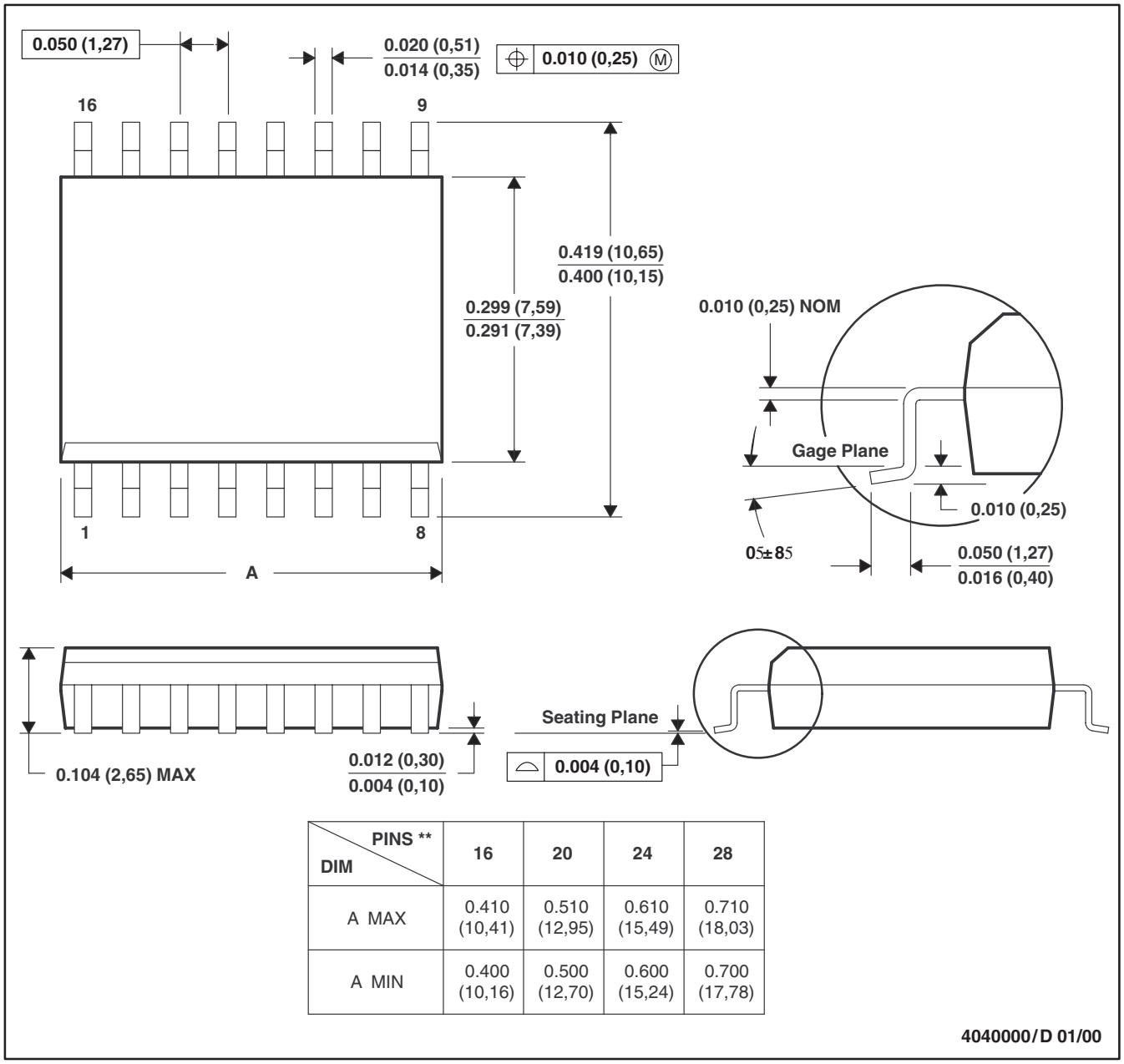
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

Package Outline Drawing

SOP/SOIC (16DW, 20DW, 24DW, 28DW)

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/D 01/00

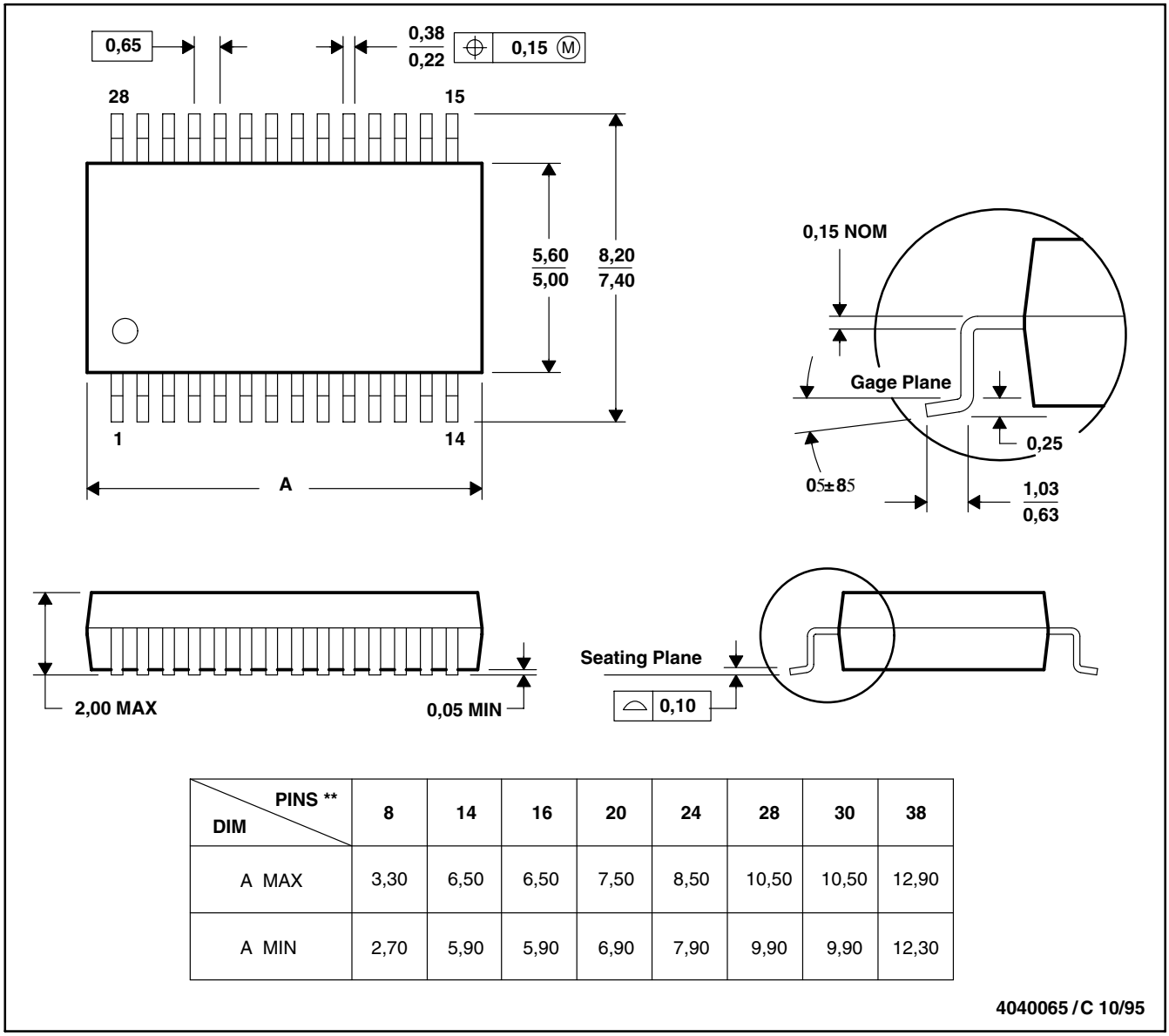
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

Package Outline Drawing

SOP/SOIC (8D, 14D, 16D)

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

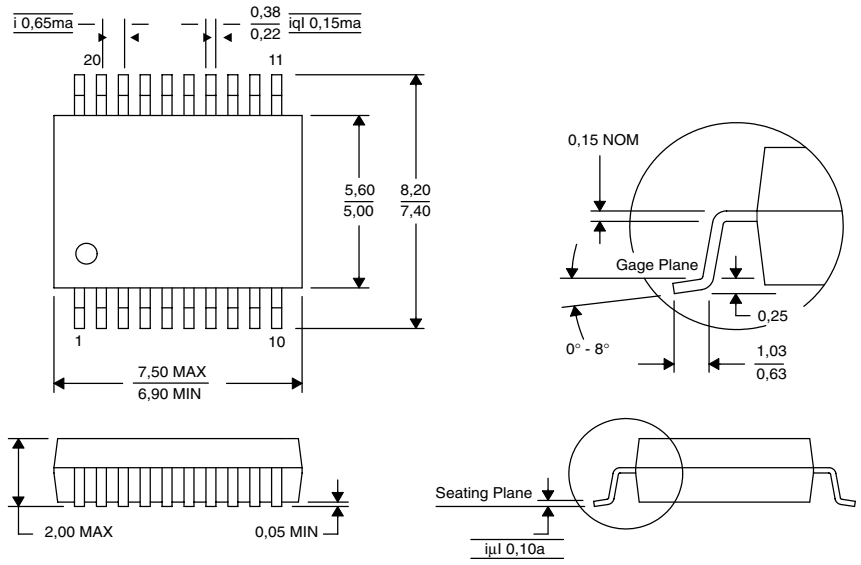
4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

Package Outline Drawing

SSOP (20DB)

NOTE: Controlling dimensions are in mm

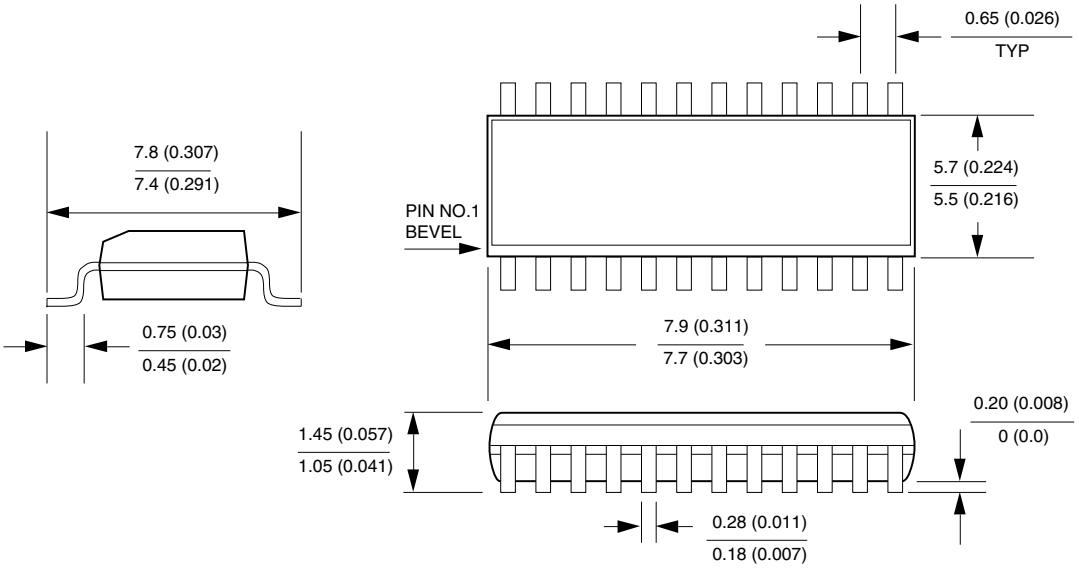


20-Lead VSOP

Package Outline Drawing

SSOP (24DBY)

NOTE: Controlling dimensions are in mm



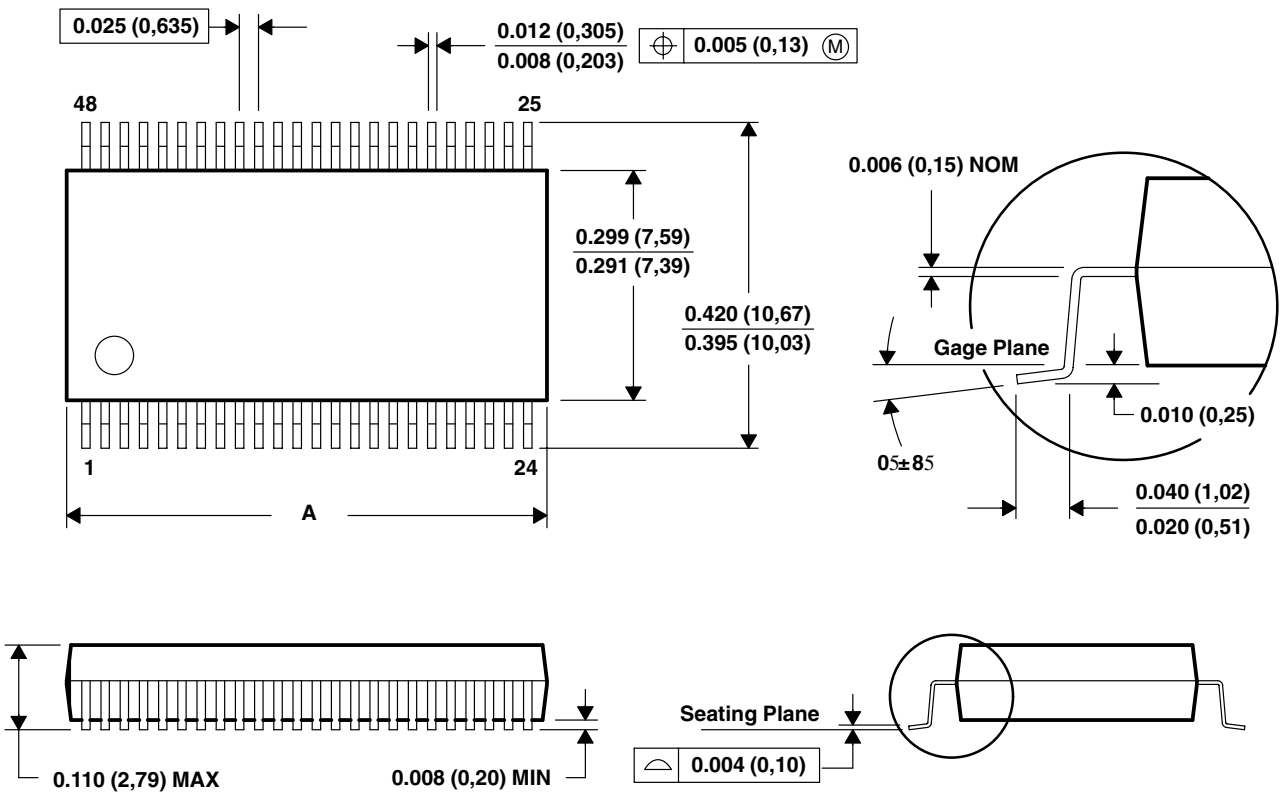
24-Lead VSOP

Package Outline Drawing

SSOP (28DL, 48DL, 56DL)

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/D 08/97

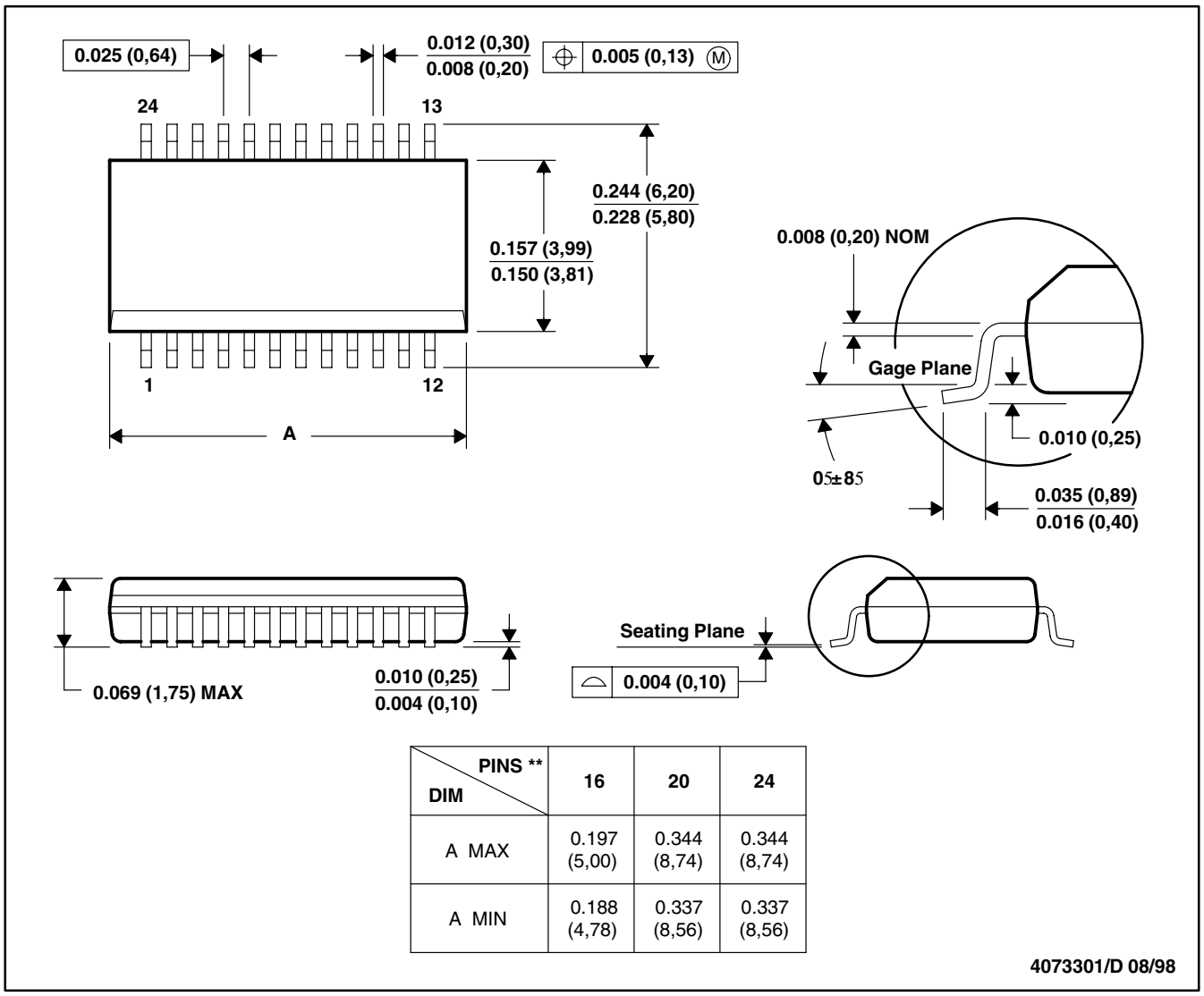
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

Package Outline Drawing

SSOP (16DBQ, 20DBQ, 24DBQ)

DBQ (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

24 PINS SHOWN



DIM \ PINS **	16	20	24
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)
A MIN	0.188 (4,78)	0.337 (8,56)	0.337 (8,56)

4073301/D 08/98

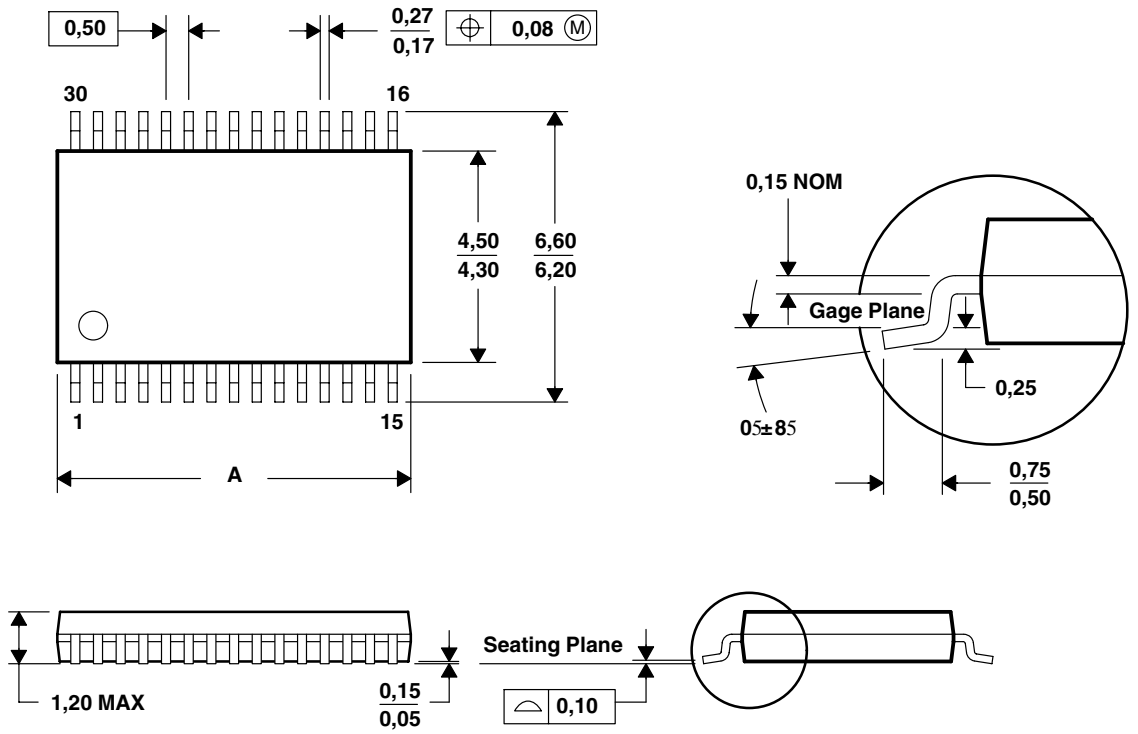
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-137

Package Outline Drawing

TSSOP (28DBT, 30 DBT, 38DBT, 44DBT, 50DBT)

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,10	12,60
A MIN	7,70	7,70	9,60	10,90	12,40

4073252/D 09/97

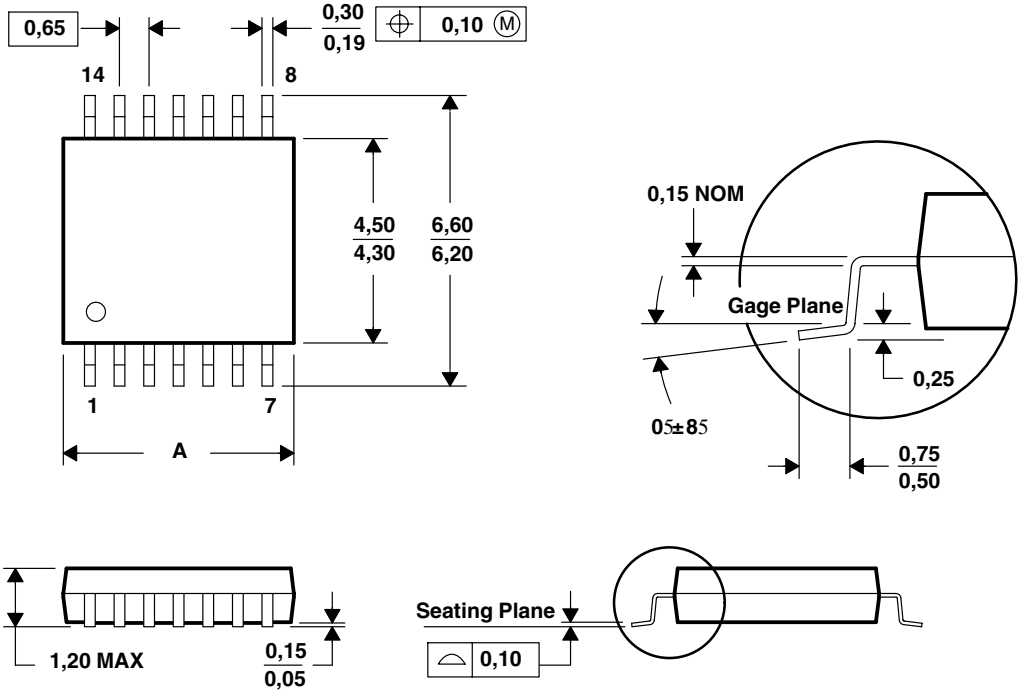
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

Package Outline Drawing

TSSOP (14PW, 16PW, 20PW, 24PW, 28PW)

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

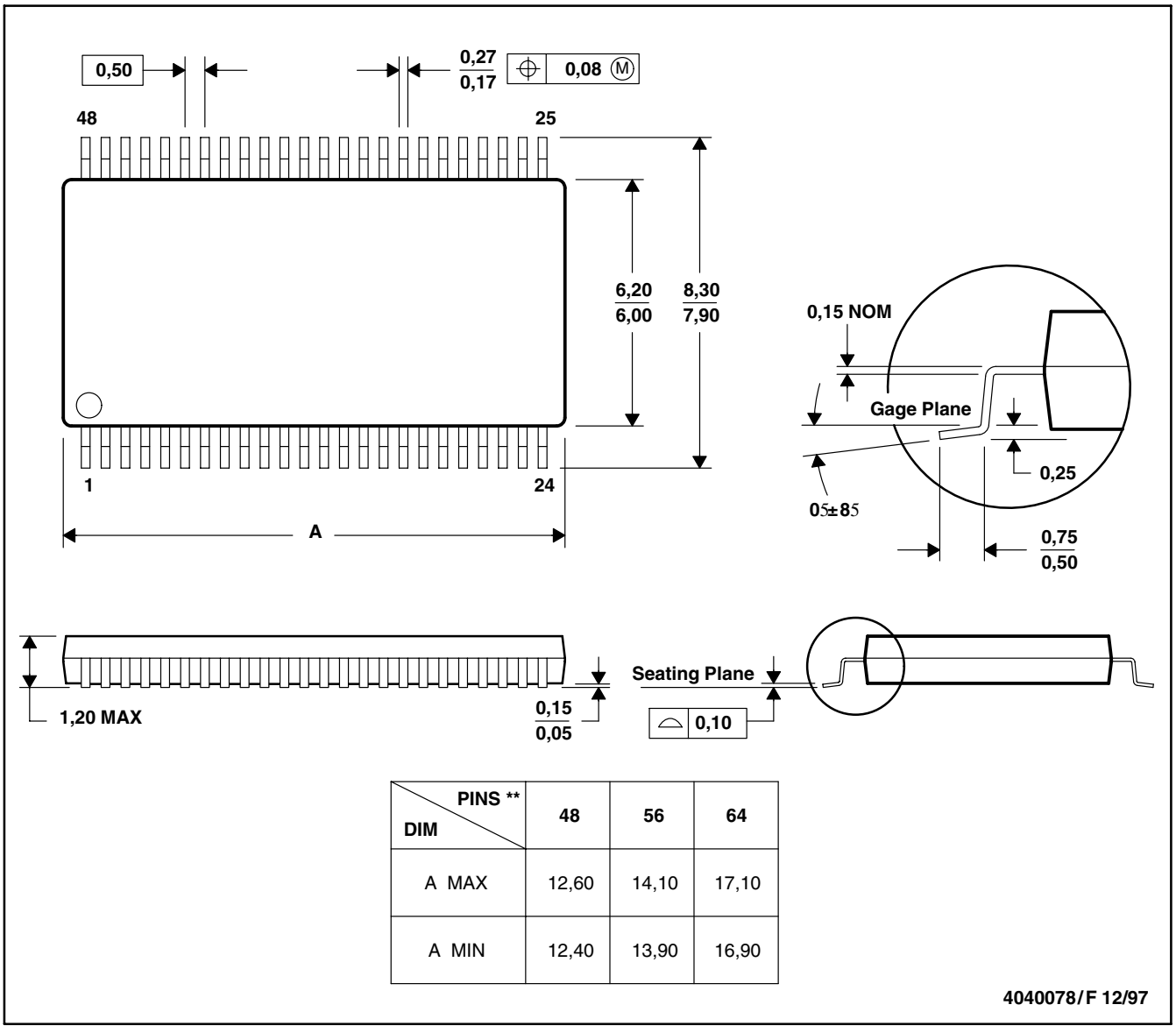
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

Package Outline Drawing

TSSOP (48DGG, 56DGG)

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

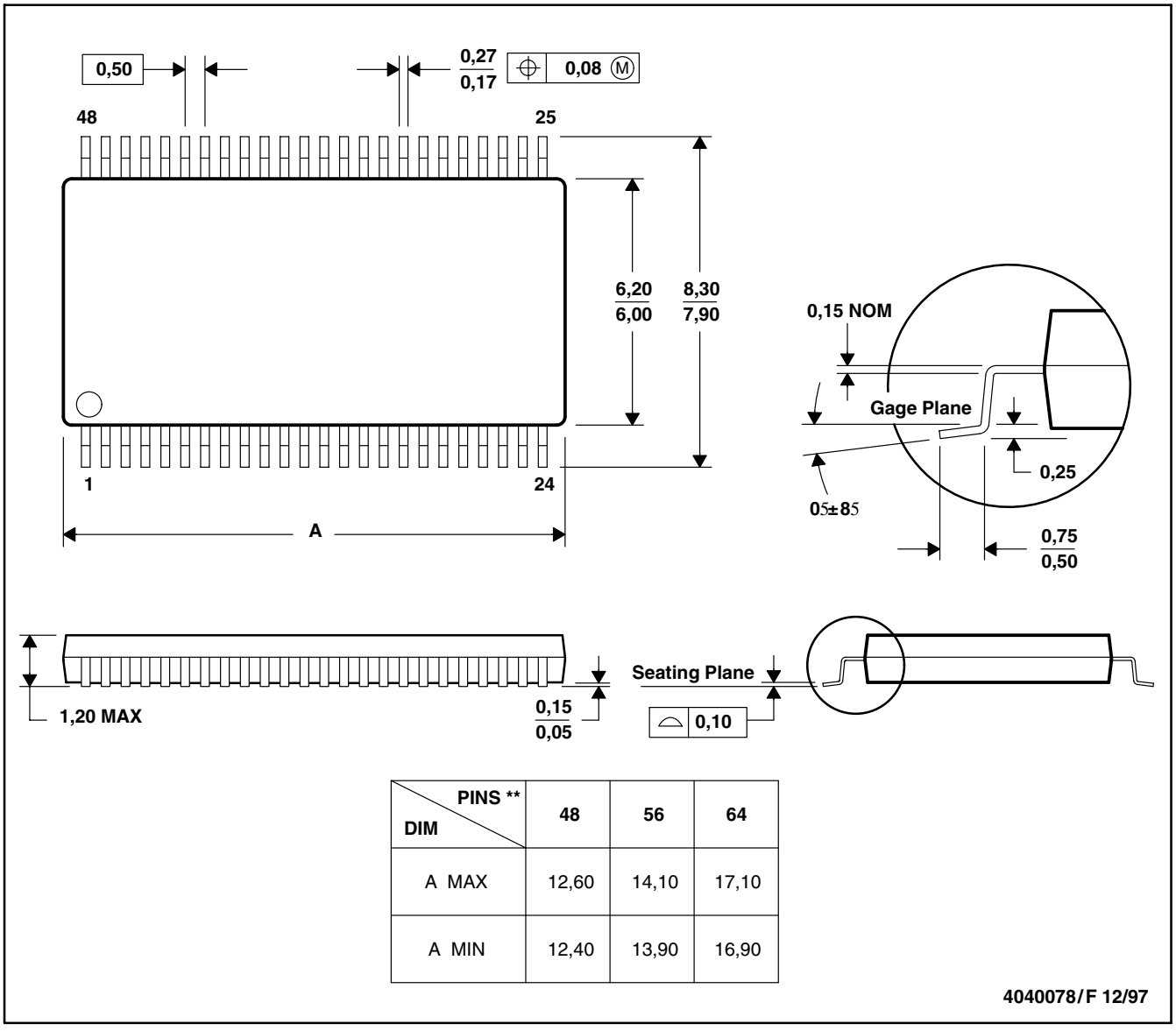
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

Package Outline Drawing

LQFP (32VF)

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

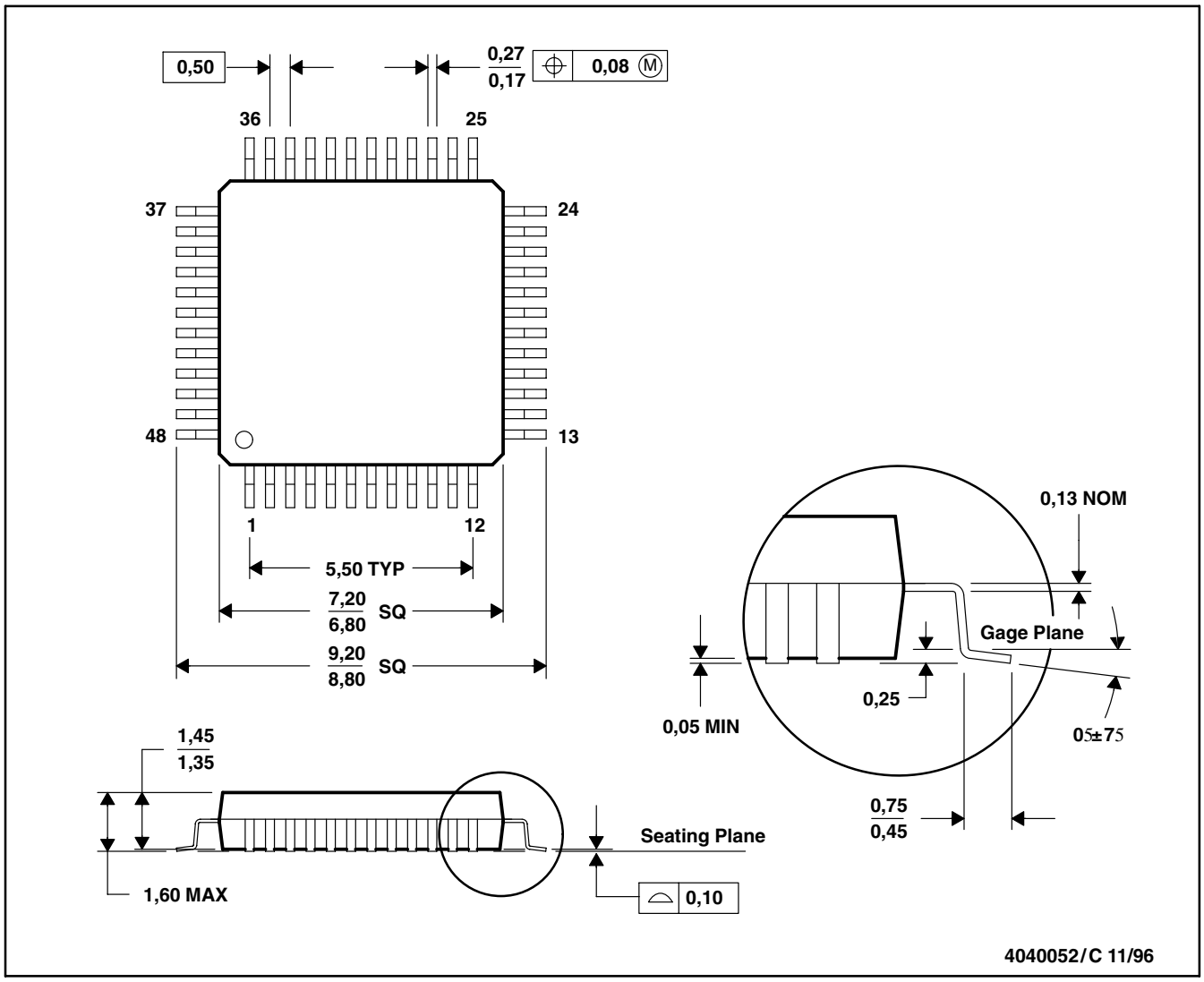
4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

Package Outline Drawing

LQFP (48PT)

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**

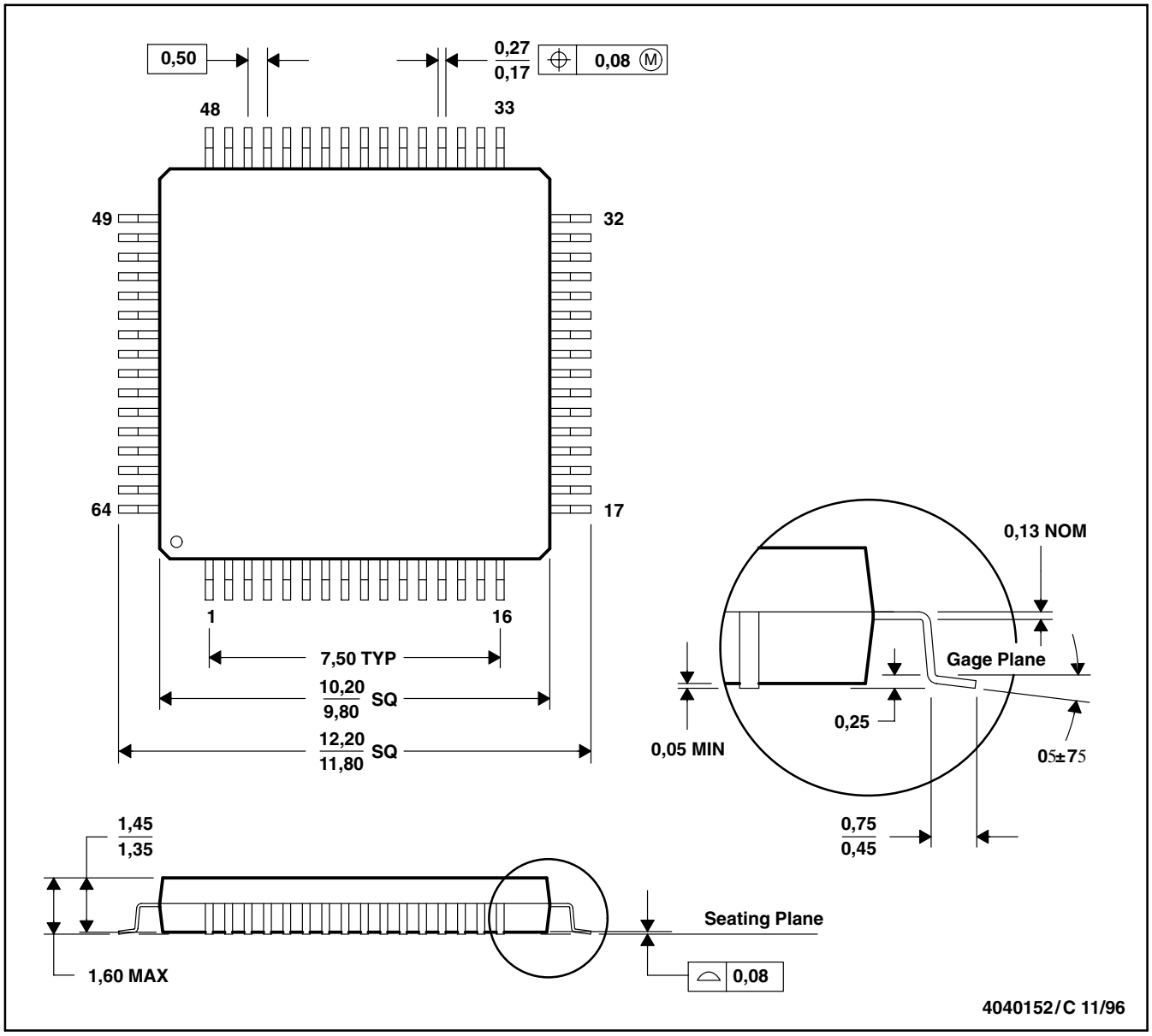


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

Package Outline Drawing

LQFP (64PM)

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**

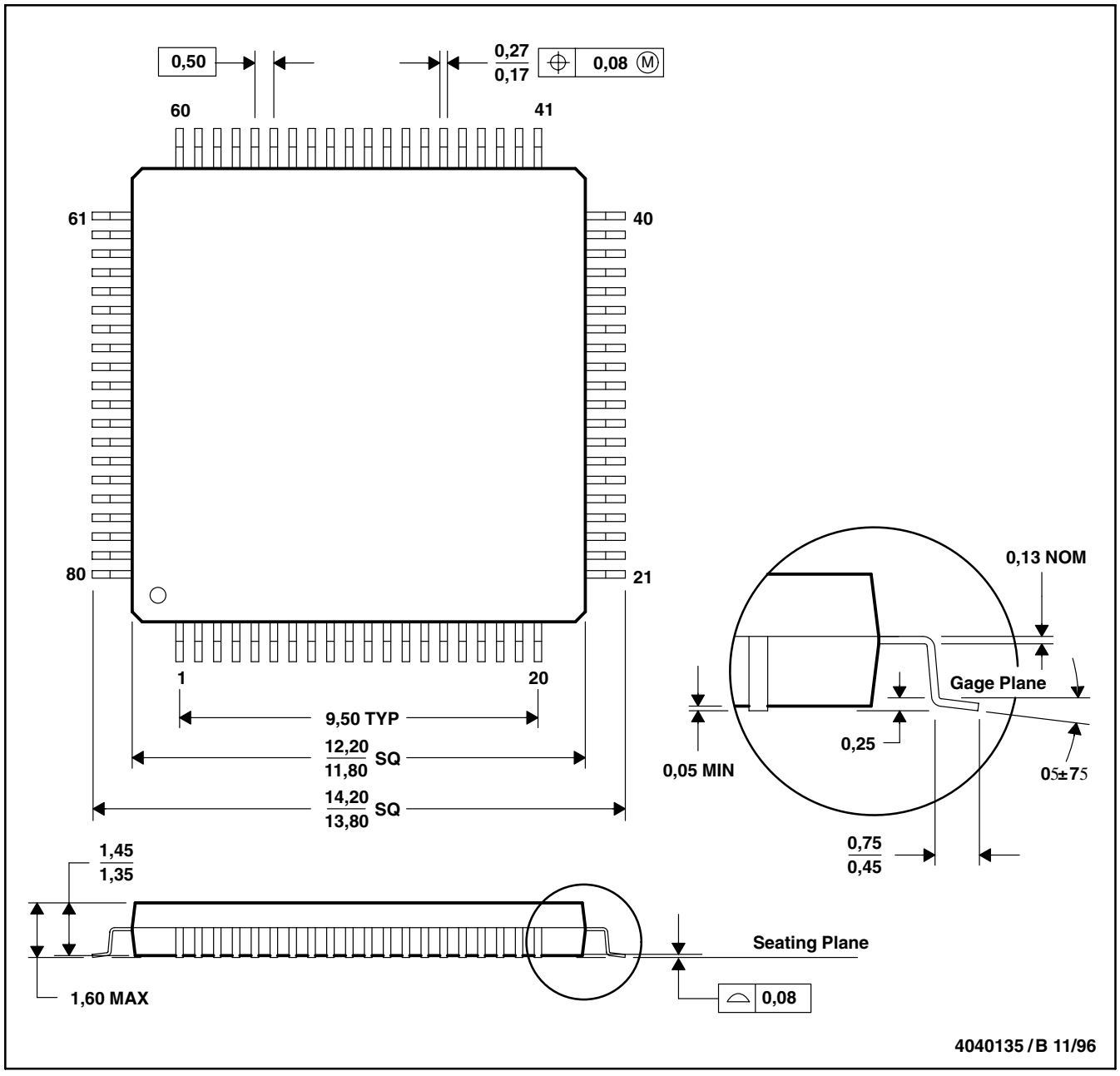


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

Package Outline Drawing

LQFP (80PN)

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**

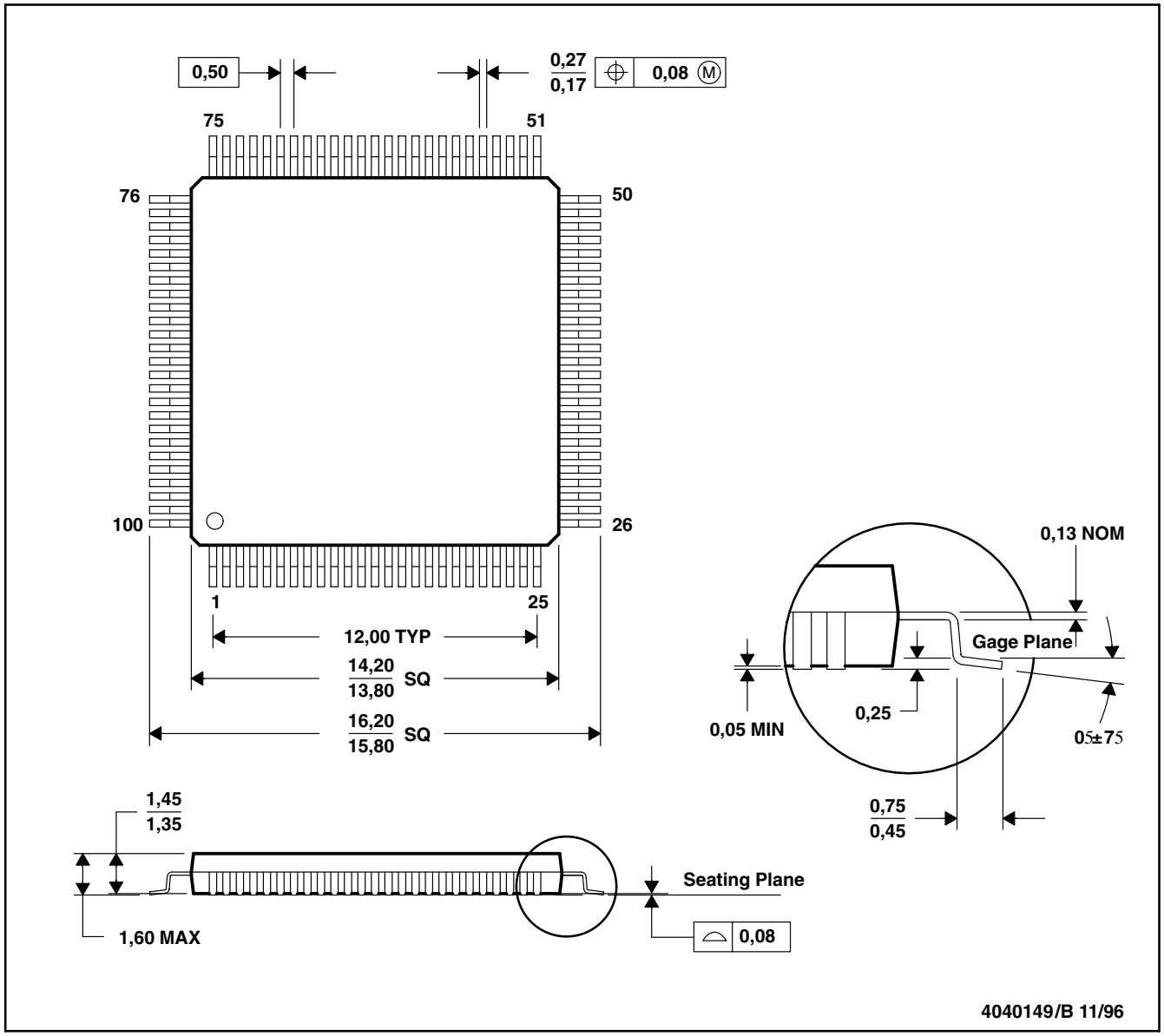


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Package Outline Drawing

LQFP (100PZ)

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**

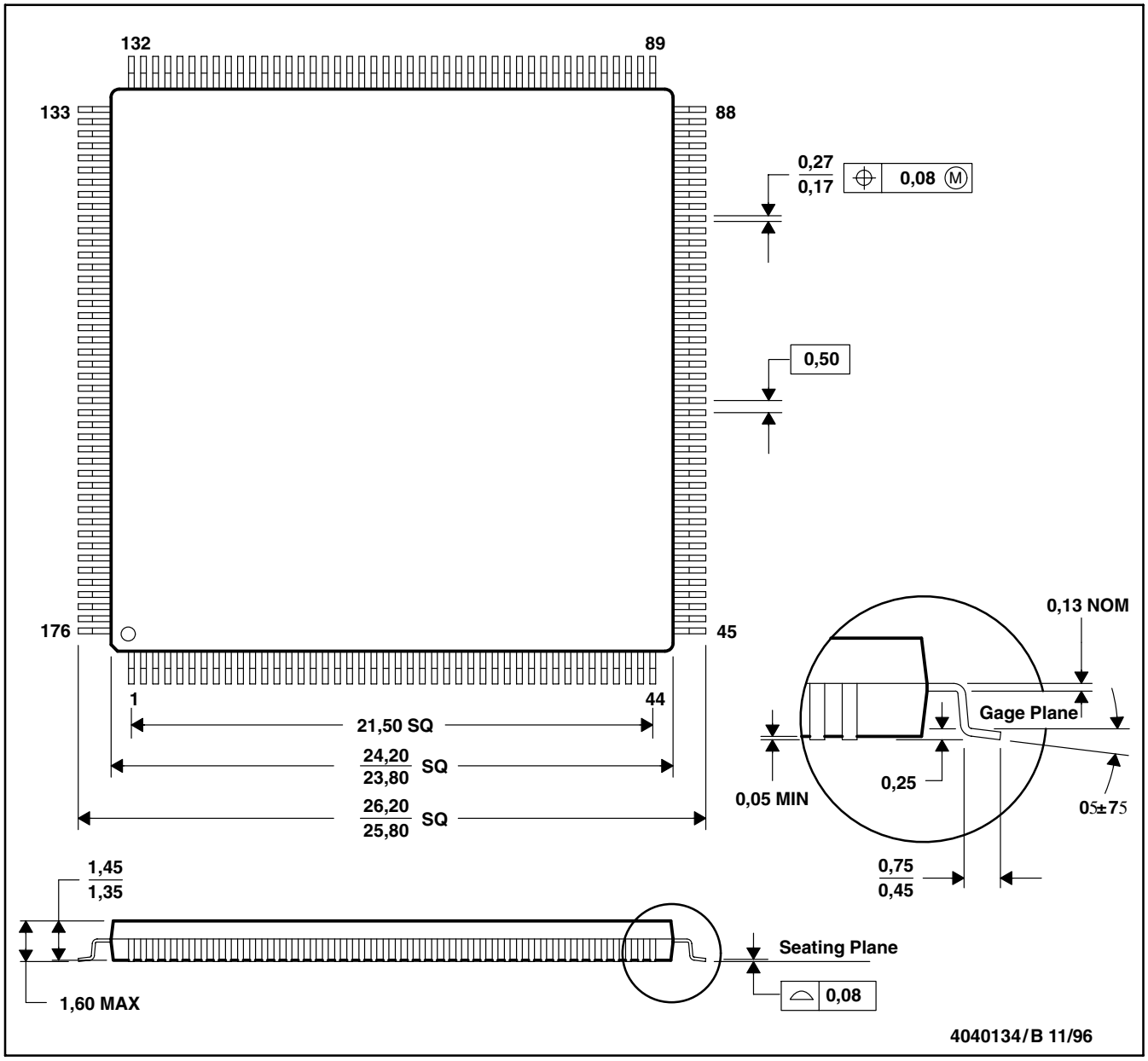


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Package Outline Drawing

LQFP (176PGF)

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**

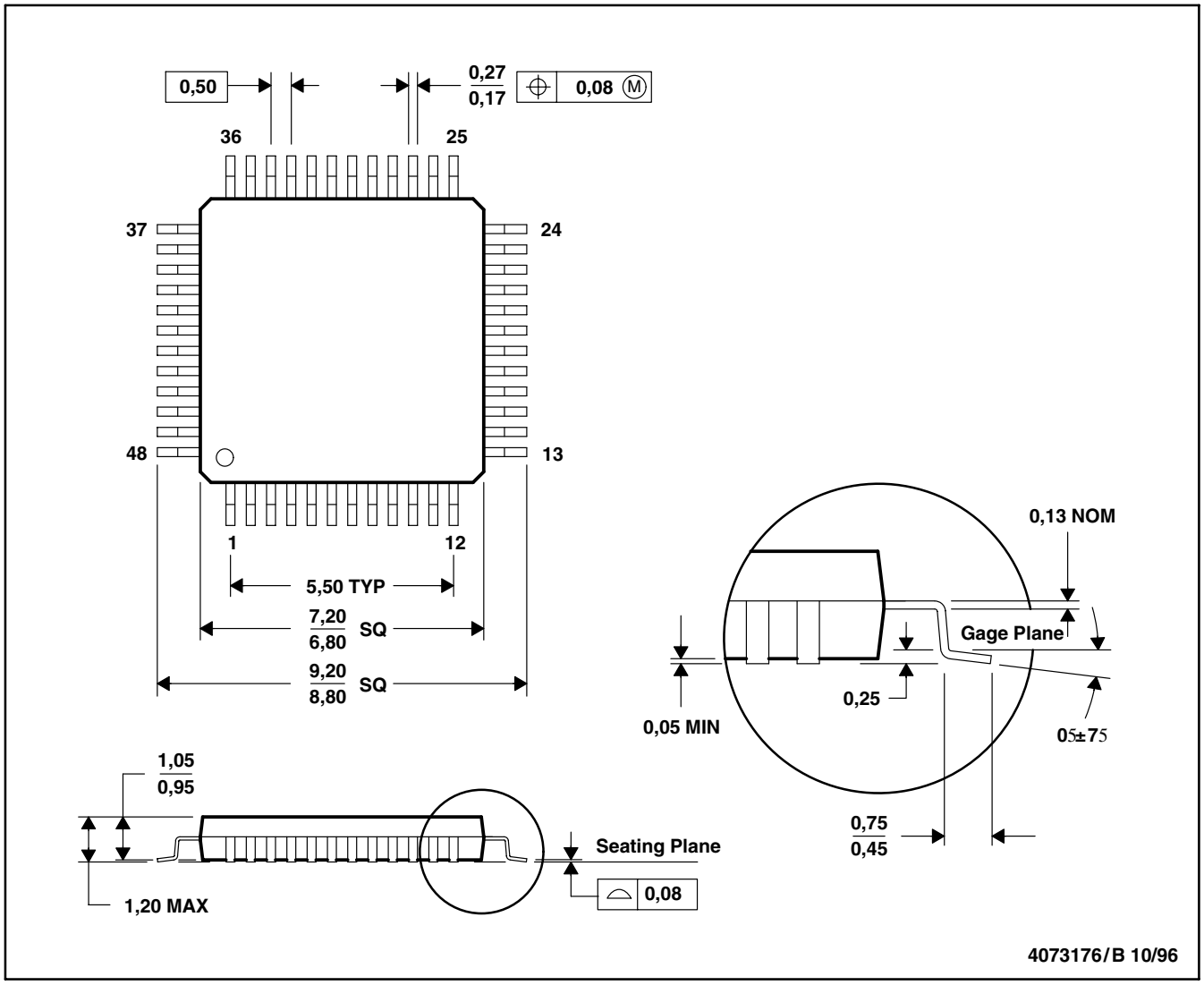


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Package Outline Drawing

TQFP (48PBF)

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**

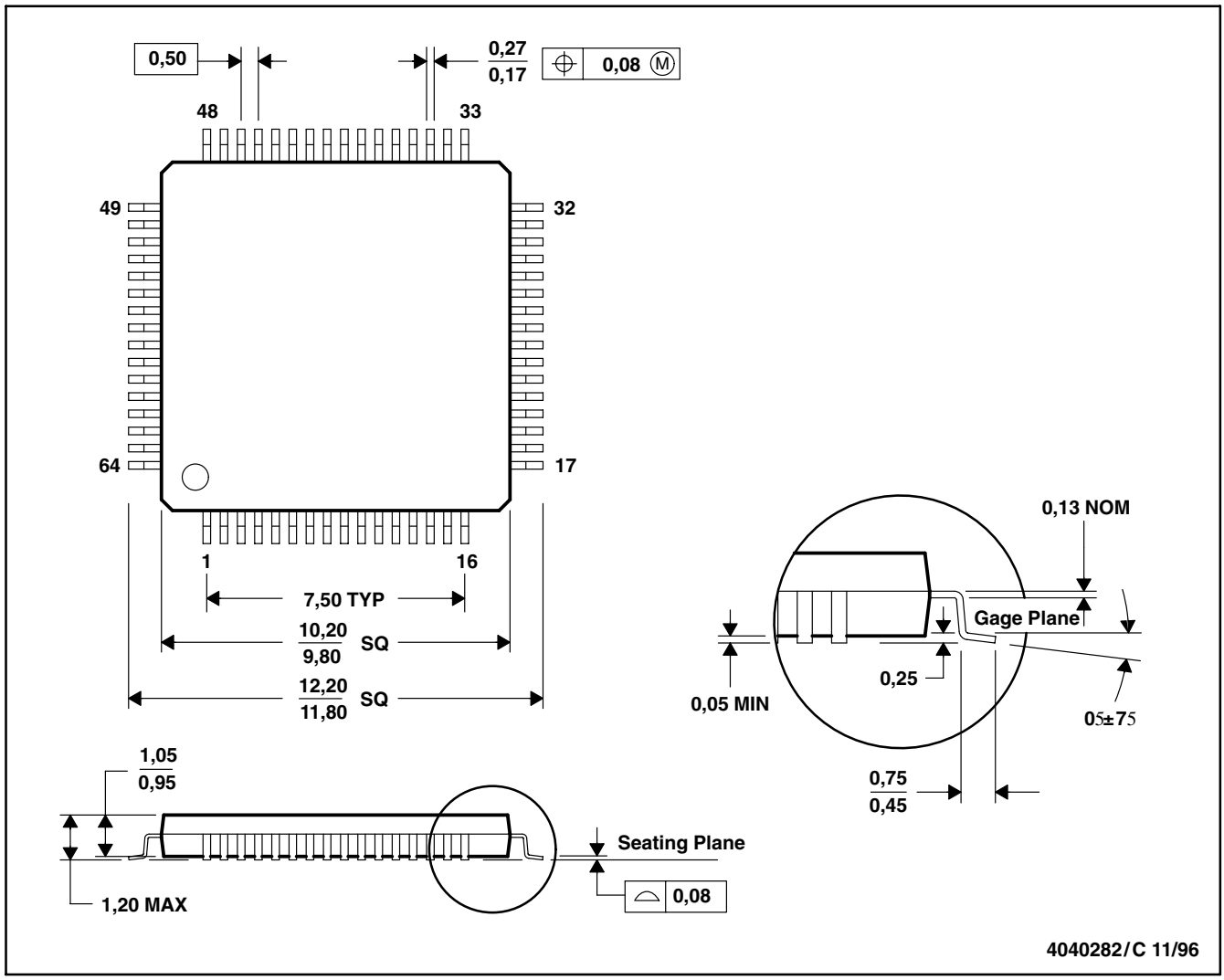


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Package Outline Drawing

TQFP (64PAG)

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**

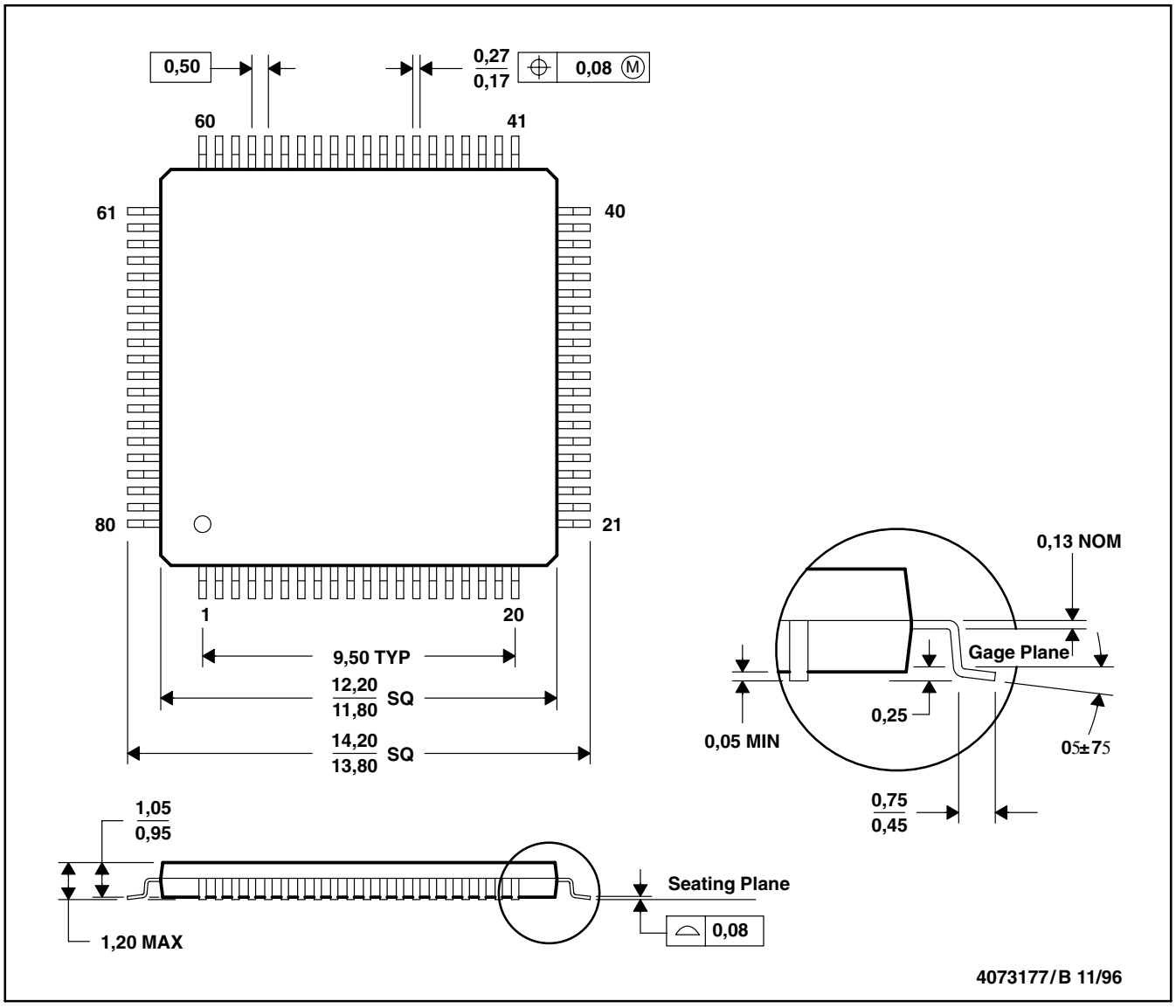


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Package Outline Drawing

TQFP (80PFC)

PFC (S-PQFP-G80) **PLASTIC QUAD FLATPACK**

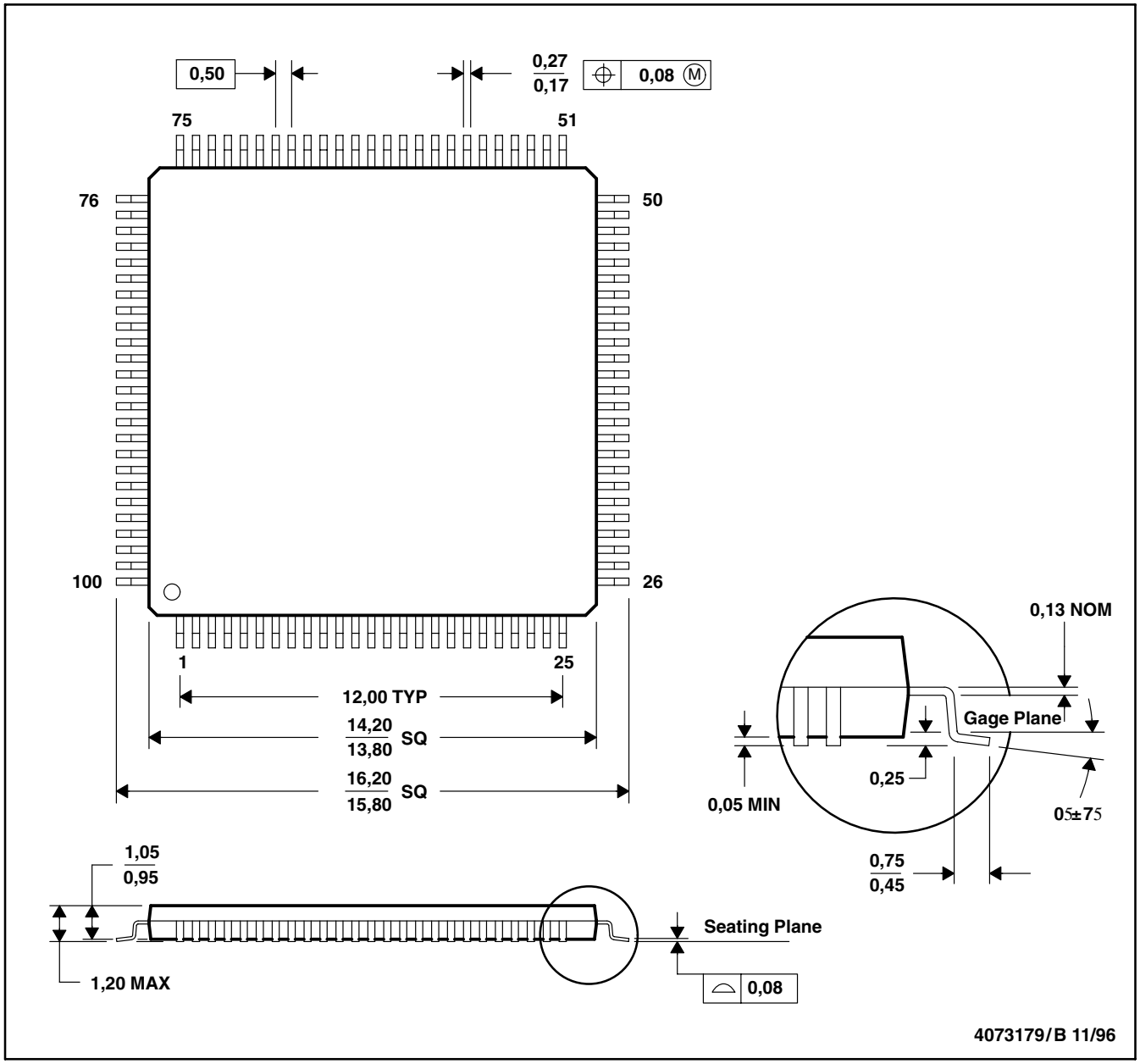


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Package Outline Drawing

TQFP (100PZT)

PZT (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



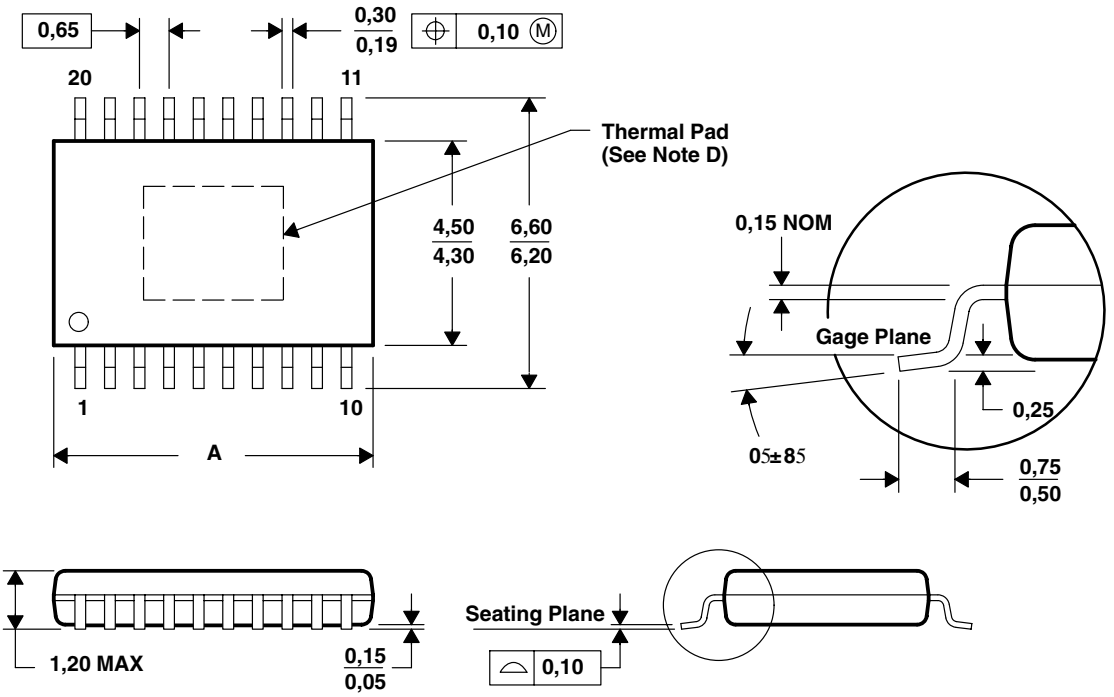
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Package Outline Drawing

HTSSOP (16PWP, 20PWP, 24PWP)

PWP (R-PDSO-G)** **PowerPAD PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

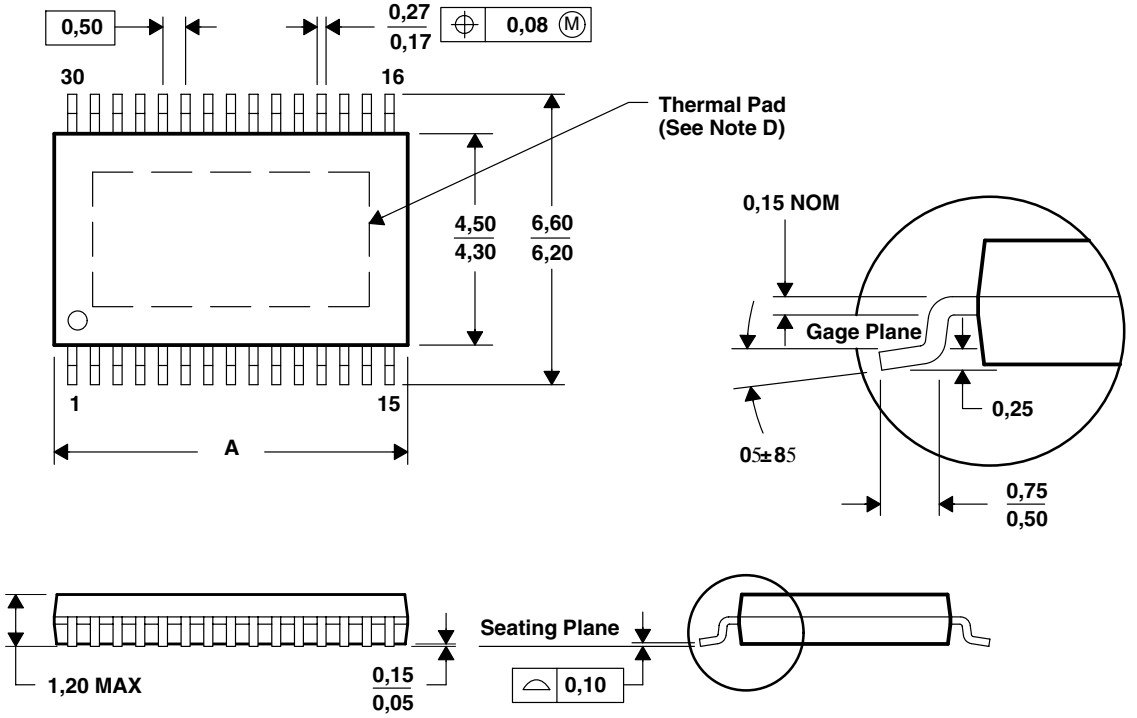
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

Package Outline Drawing

HTSSOP (38DCP)

DCP (R-PDSO-G)** **PowerPAD PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,40	12,60
A MIN	7,70	7,70	9,60	11,20	12,40

4073267/A 02/98

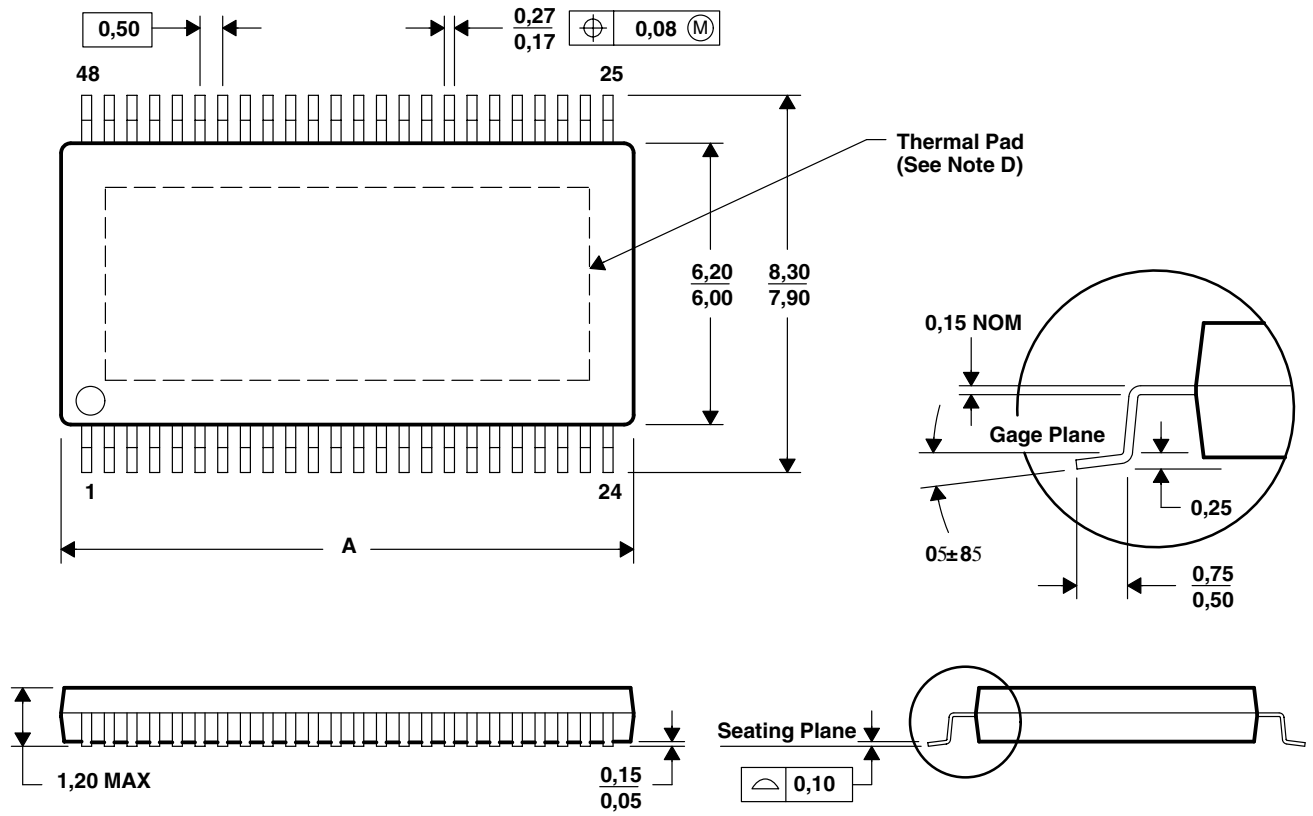
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

Package Outline Drawing

HTSSOP (56DCA)

DCA (R-PDSO-G)** **PowerPAD PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

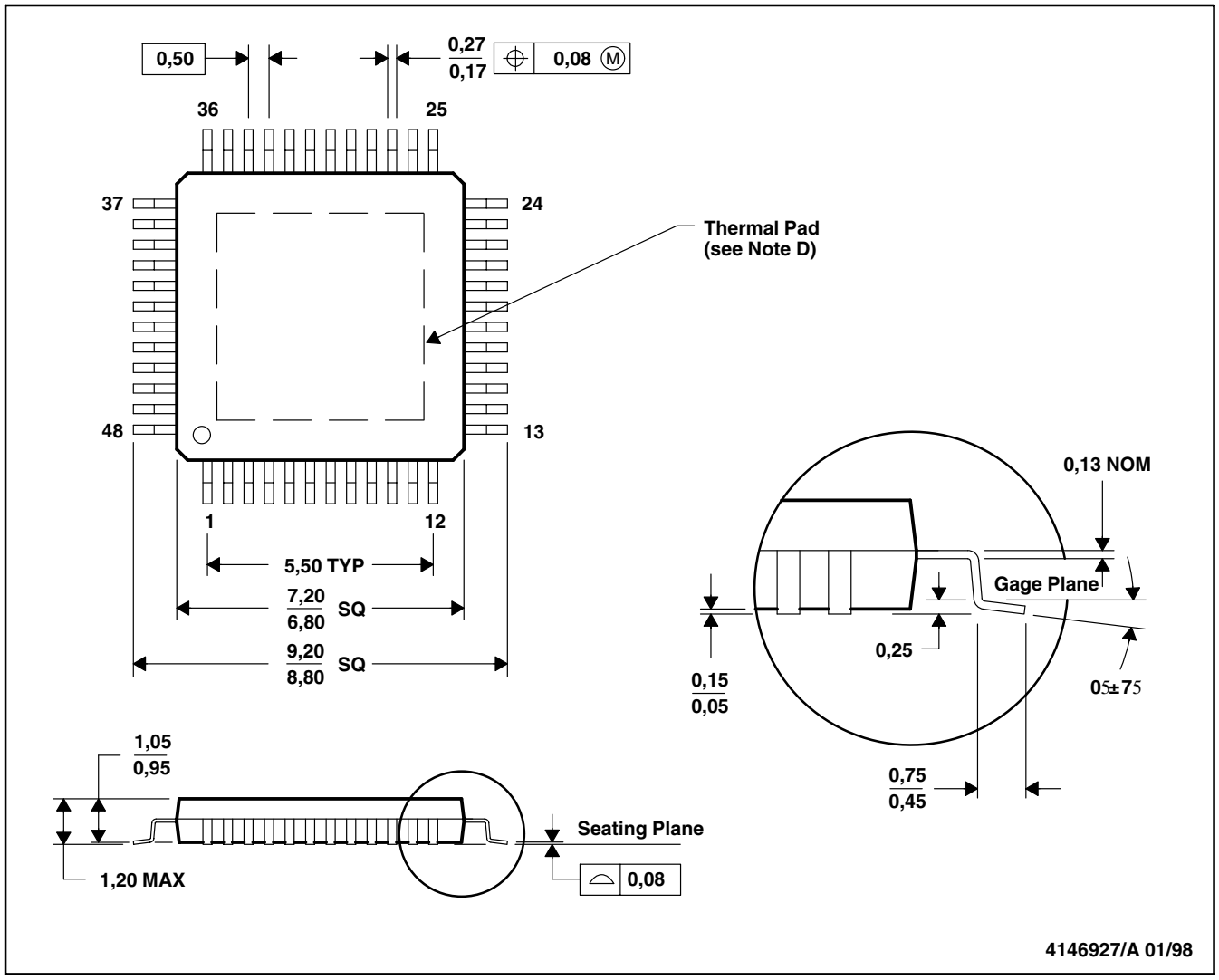
4073259/A 01/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

Package Outline Drawing

HTQFP (48PHP)

PHP (S-PQFP-G48) **PowerPAD PLASTIC QUAD FLATPACK**

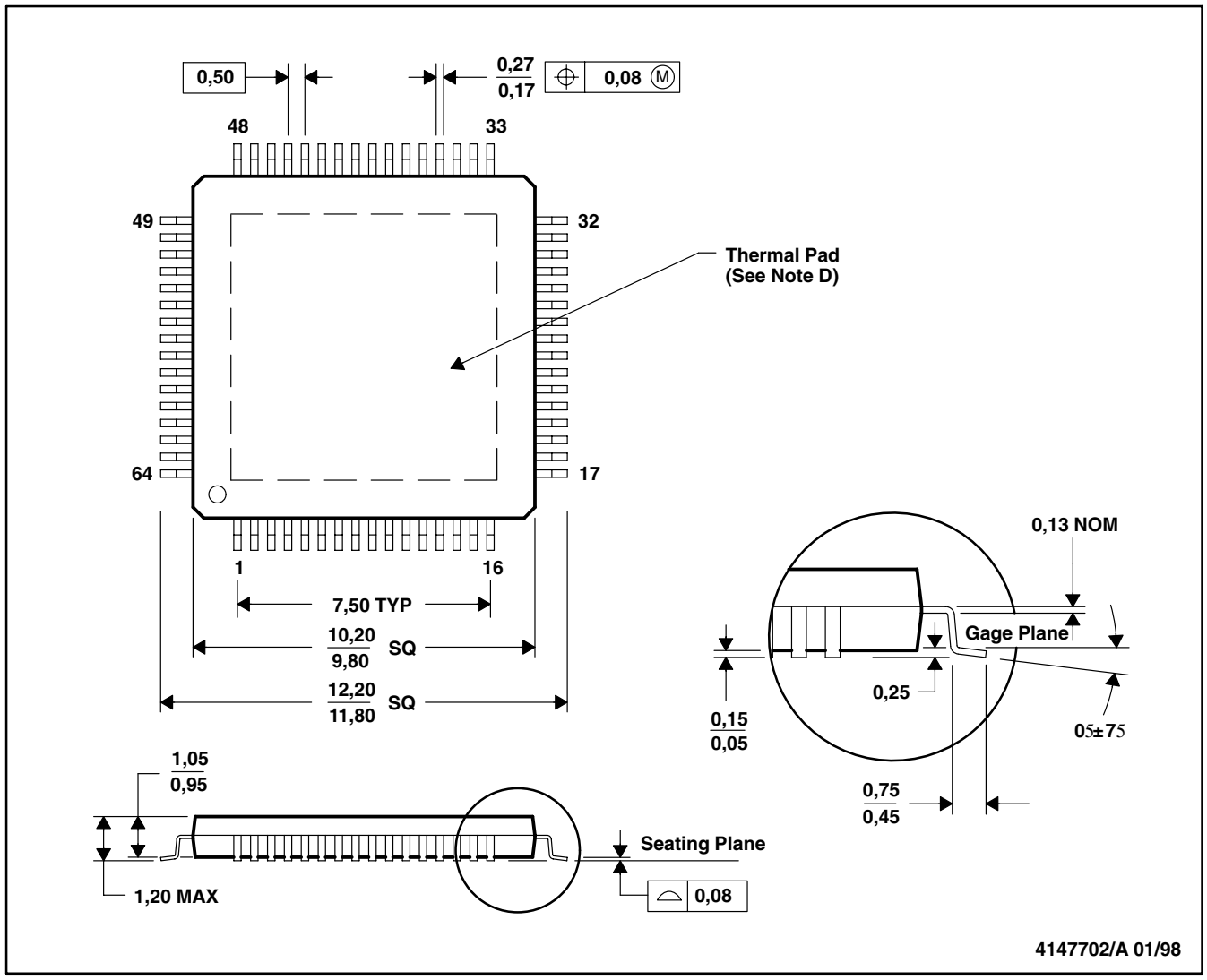


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

Package Outline Drawing

HTQFP (64PAP)

PAP (S-PQFP-G64) **PowerPAD PLASTIC QUAD FLATPACK**

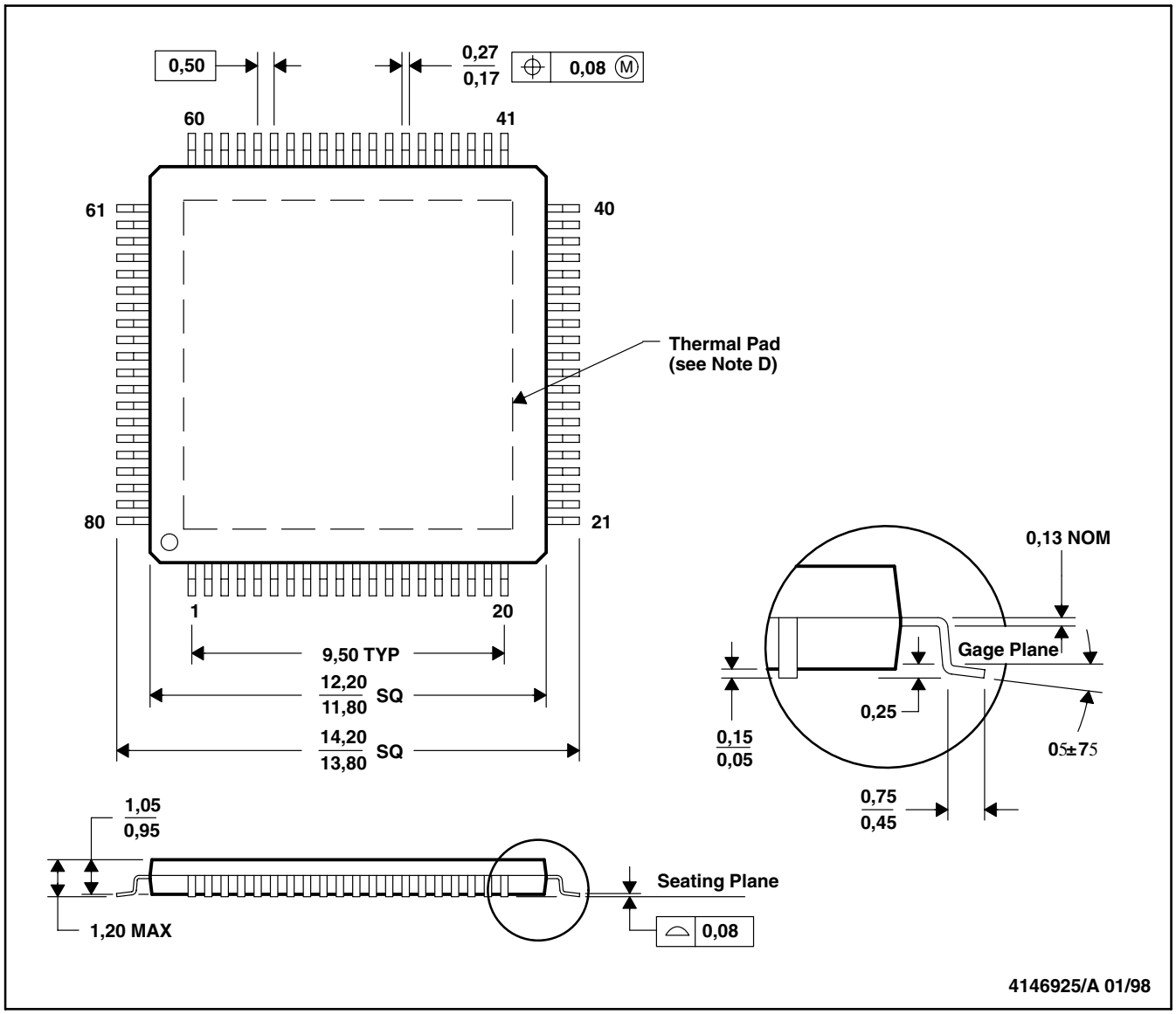


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

Package Outline Drawing

HTQFP (80PFP)

PFP (S-PQFP-G80) **PowerPAD PLASTIC QUAD FLATPACK**

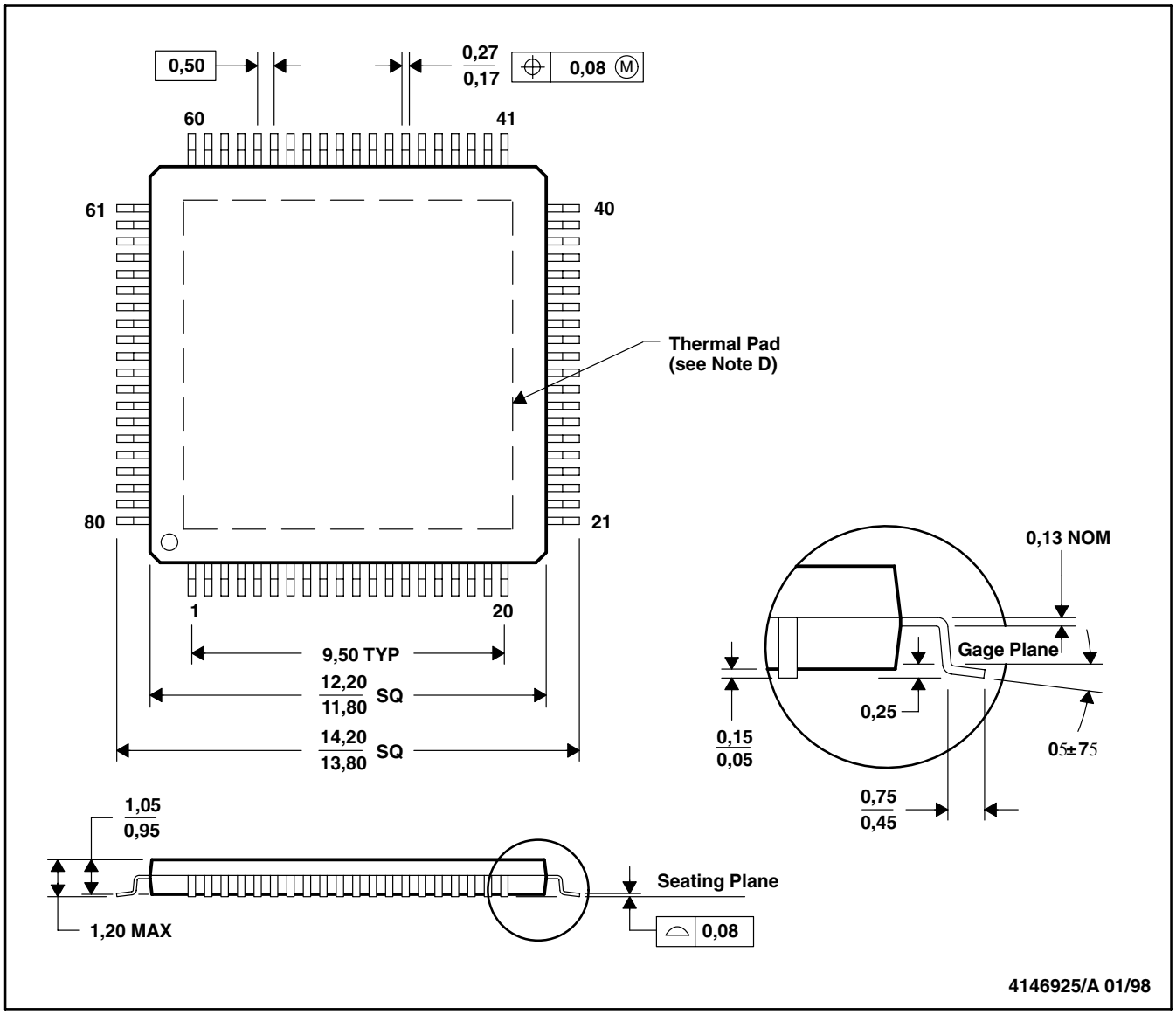


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

Package Outline Drawing

HTQFP (80PFP)

PFP (S-PQFP-G80) **PowerPAD PLASTIC QUAD FLATPACK**

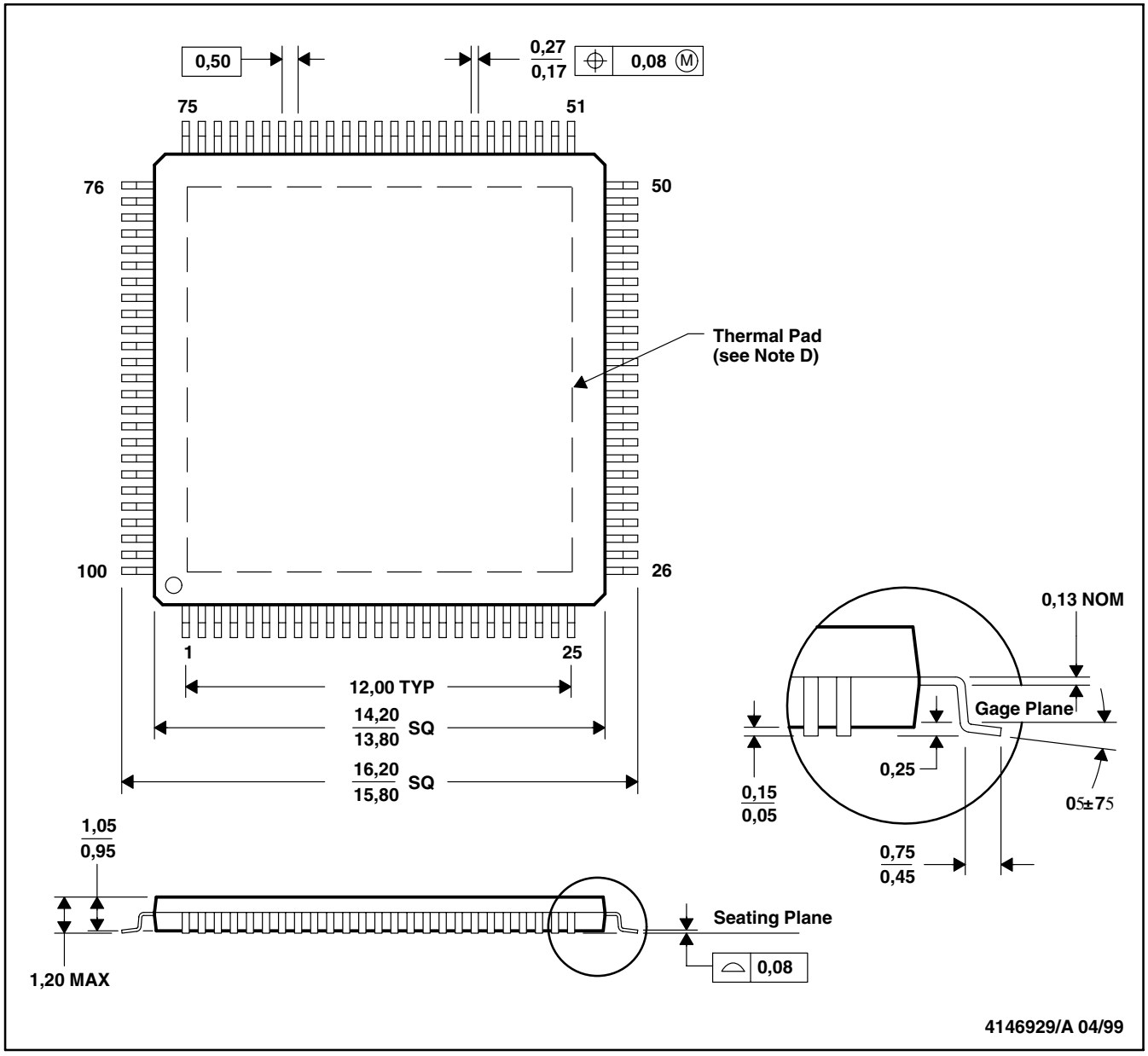


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

Package Outline Drawing

HTQFP (100PZP)

PZP (S-PQFP-G100) **PowerPAD PLASTIC QUAD FLATPACK**

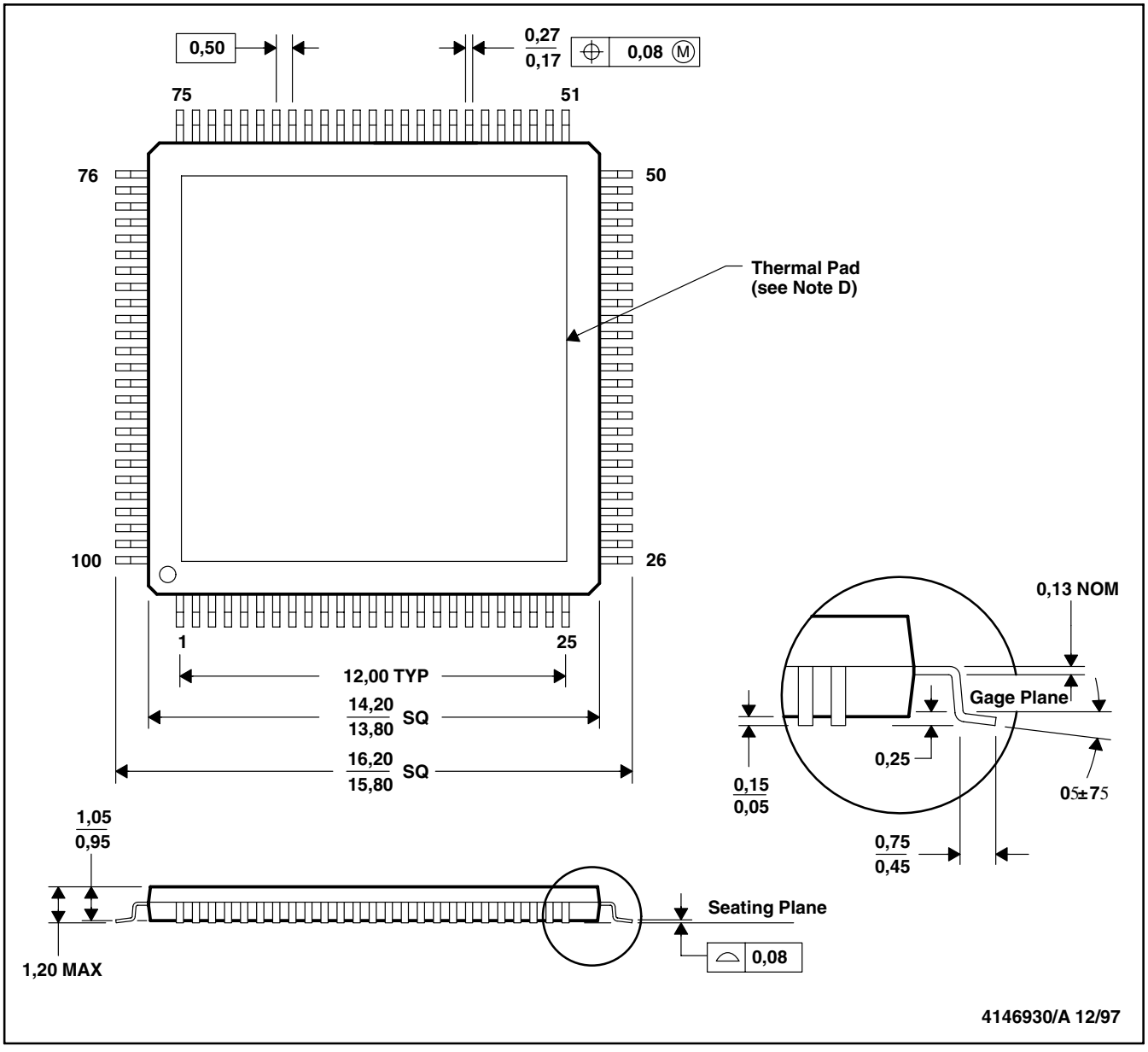


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

Package Outline Drawing

HTQFP (100PFP)

PFD (S-PQFP-G100) **PowerPAD PLASTIC QUAD FLATPACK (DIE DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

Recommended Reflow Conditions

The following figures shown below are the recommended standard soldering conditions for Texas Instruments Storage Products products. Recommended temperature profiles are specified using the upper limits of the surface temperature of the body. Actual soldering conditions should be determened as shown by the dotted line.

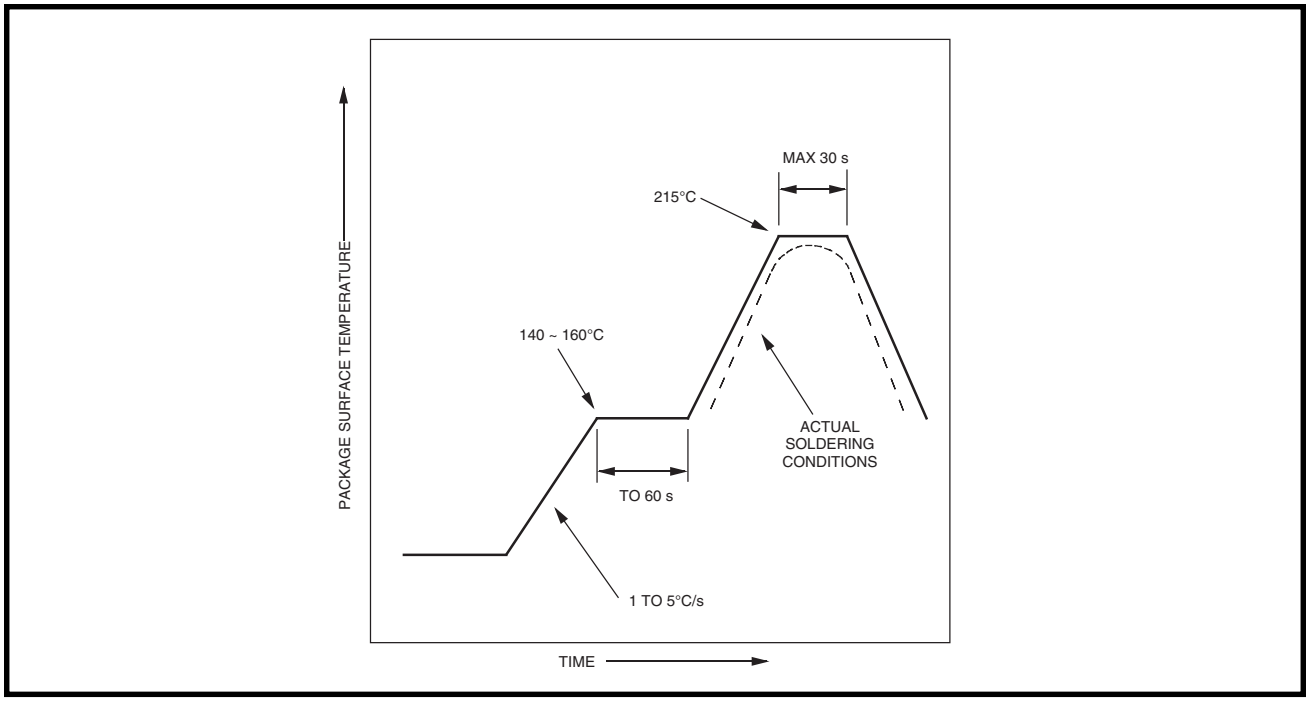


FIGURE A: Temperature Profile for VPS (Vapor Phase Reflow Soldering)

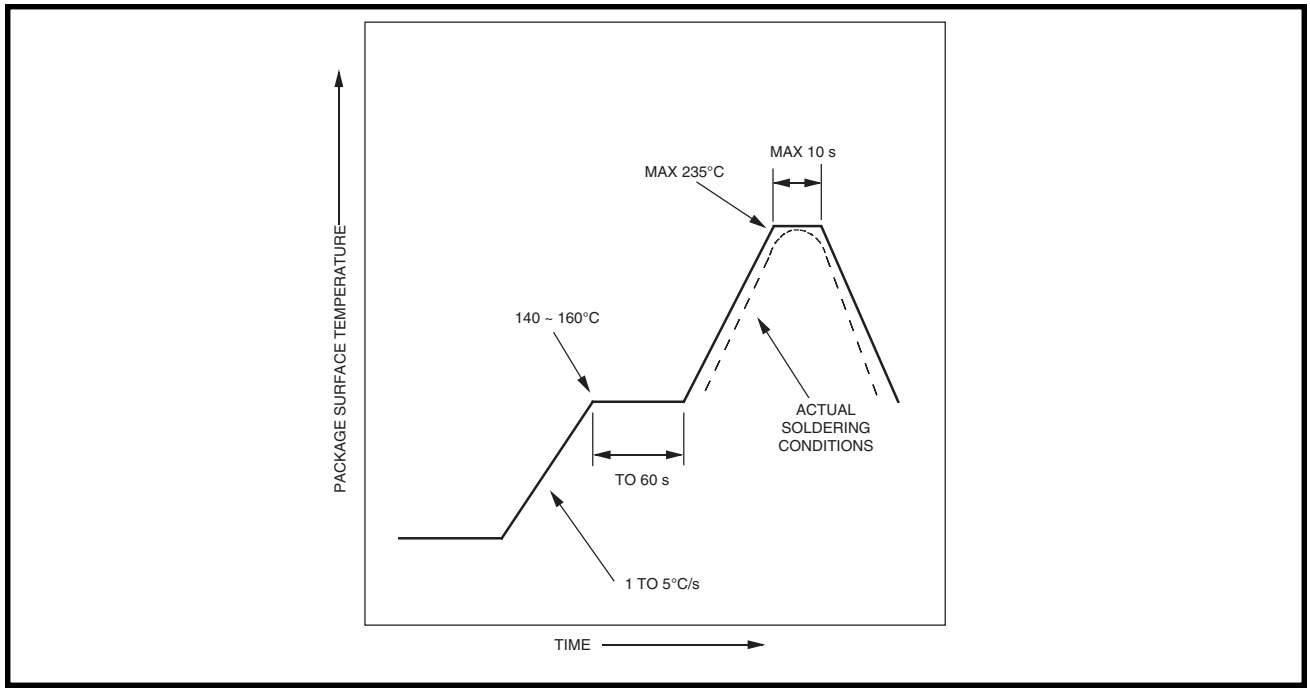
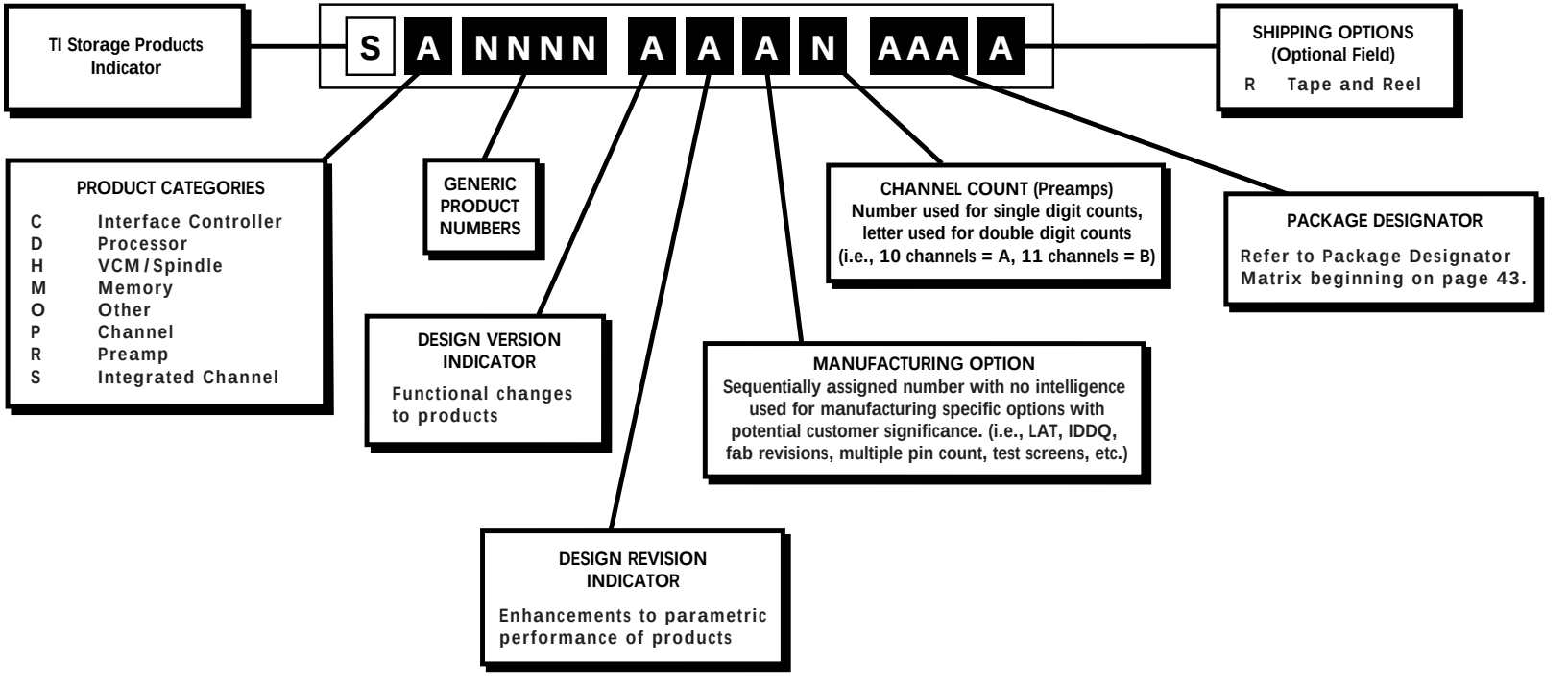


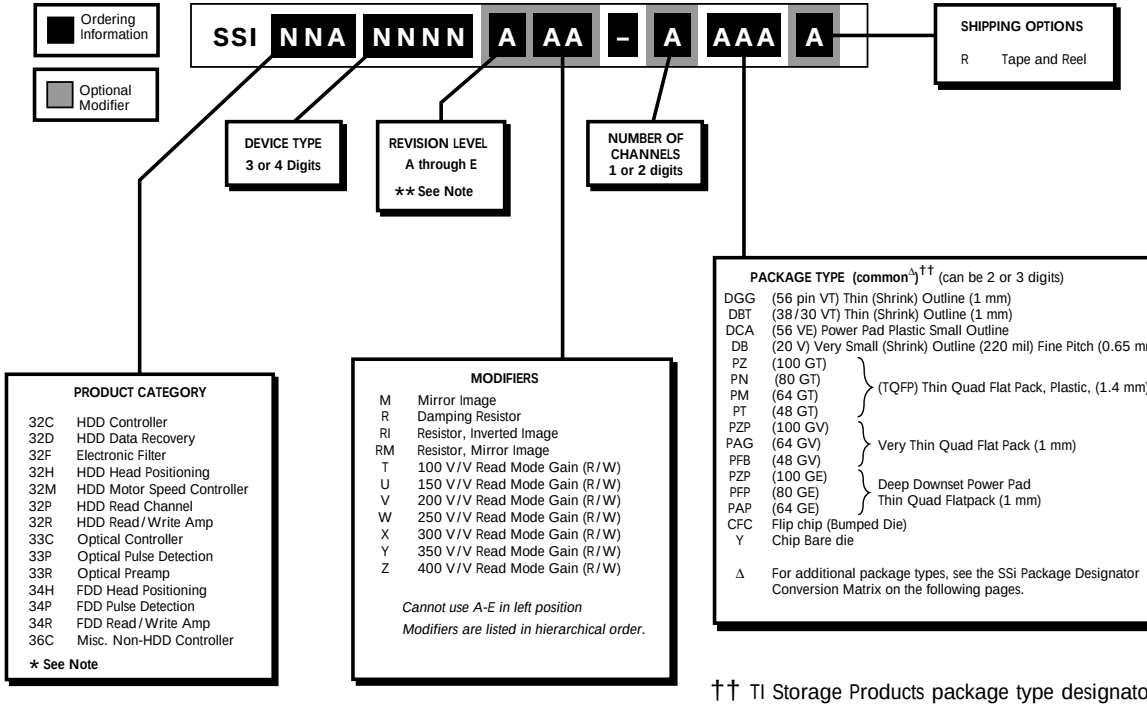
FIGURE B: Temperature Profile for Infrared Reflow Soldering

REVISED‡ TI STORAGE PRODUCTS DEVICE IDENTIFICATION DEFINITION



‡ Refers to all new products beginning July 1, 1998 and any subsequent product revisions

EXISTING$^{\Delta}$ TI STORAGE PRODUCTS STANDARD PRODUCT MARKETING NUMBER DEFINITION



Exception:
Demo Kit Marketing Part Number

Δ Refers to products existing as of November 1, 1997 through July 1, 1998 and any subsequent product revisions

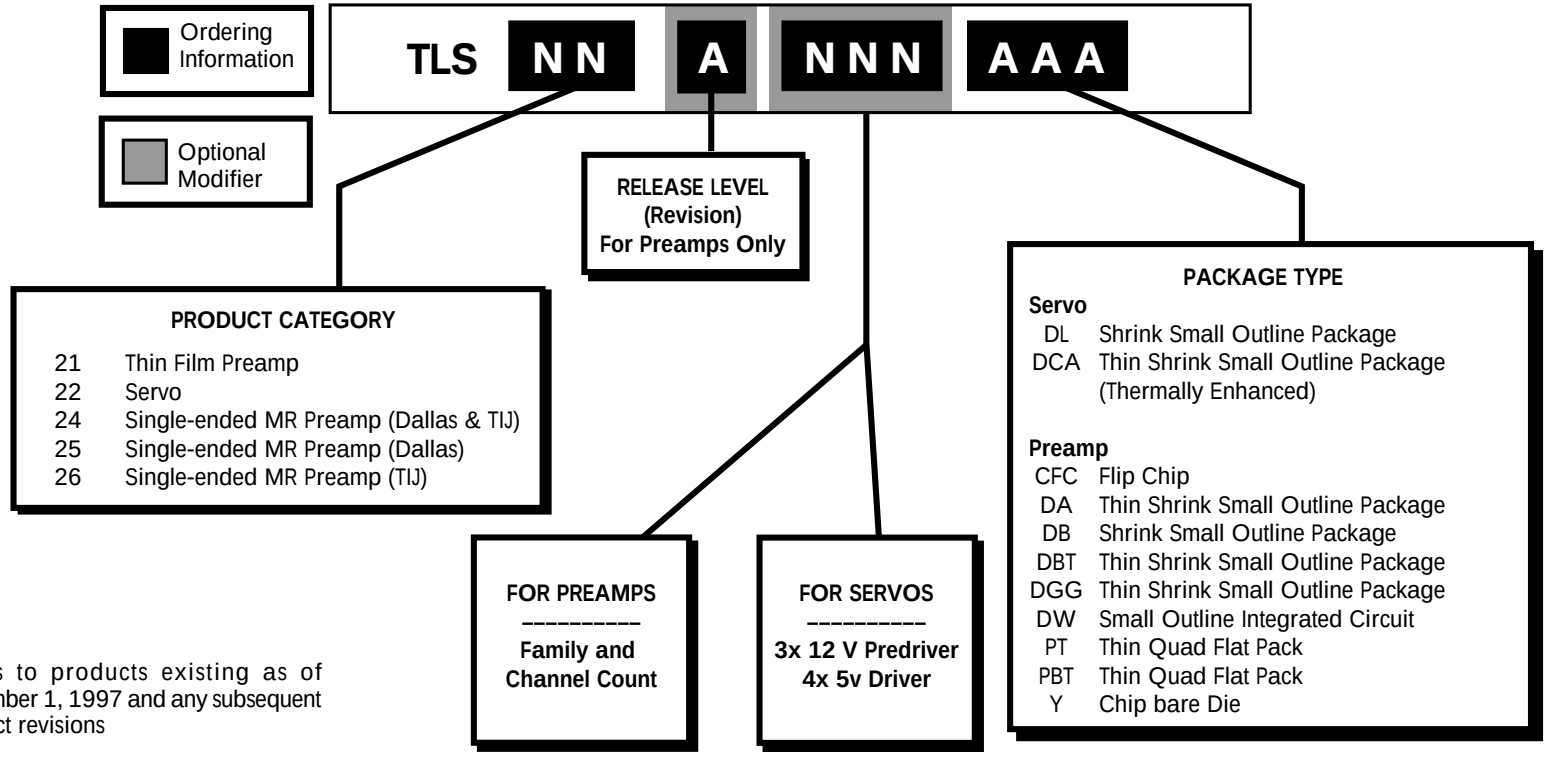
* 30 replacing any 3x prefix refers to custom proprietary product

** Release level should only be used to define enhancement to parametric performance, cannot be used for functional changes. Functional changes to a part should be defined as a new marketing number.

†† TI Storage Products package type designator conforms with TI package type nomenclature (suffix only). All new device types between November 1, 1997 and July 1, 1998 adhere to these Standard Package Designators.

EXISTING$^{\Delta}$ TI PRODUCT MARKETING NUMBER DEFINITION

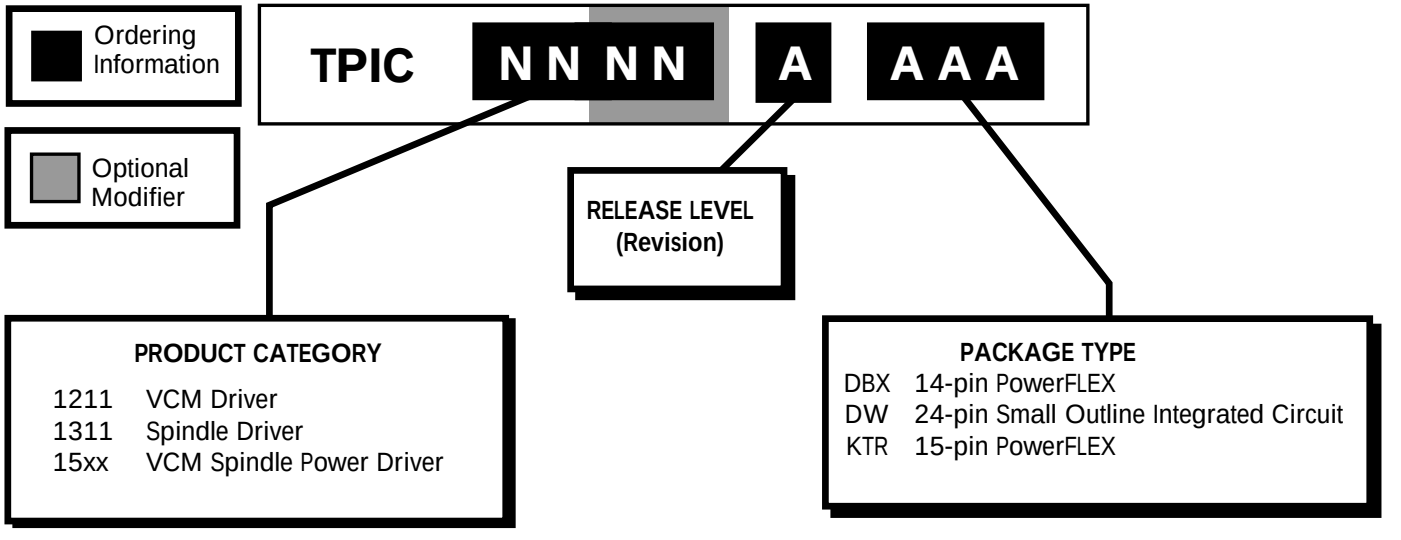
TEXAS INSTRUMENTS LINEAR STORAGE



Δ Refers to products existing as of November 1, 1997 and any subsequent product revisions

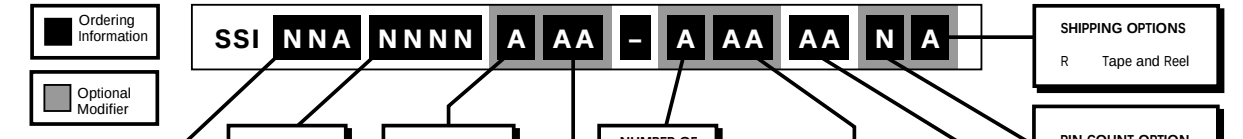
EXISTING$^{\Delta}$ TI PRODUCT MARKETING NUMBER DEFINITION

TEXAS INSTRUMENTS POWER INTEGRATED CIRCUIT



Δ Refers to products existing as of November 1, 1997 and any subsequent product revisions

FORMER$^{\Delta}$ SSi PRODUCT MARKETING NUMBER DEFINITION



SHIPPING OPTIONS

R Tape and Reel

PIN COUNT OPTION
1 or 2 digits

DEVICE TYPE
3 or 4 Digits

REVISION LEVEL
A through E
**** See Note**

NUMBER OF CHANNELS
1 or 2 digits

TEMPERATURE RANGE

C	Commercial (0 °C to +70 °C)
I	Industrial (-40 °C to +85 °C)
J	Burn-In (168 Hours)
K	Burn-In (48 Hours)

Modifiers are listed in hierarchical order.

PRODUCT CATEGORY

32C	HDD Controller
32D	HDD Data Recovery
32F	Electronic Filter
32H	HDD Head Positioning
32M	HDD Motor Speed Controller
32P	HDD Read Channel
32R	HDD Read/Write Amp
33C	Optical Controller
33P	Optical Pulse Detection
33R	Optical Preamp
34H	FDD Head Positioning
34P	FDD Pulse Detection
34R	FDD Read/Write Amp
36C	Misc. Non-HDD Controller

*** See Note**

MODIFIERS

M	Mirror Image
R	Damping Resistor
RI	Resistor, Inverted Image
RM	Resistor, Mirror Image
T	100 V/V Read Mode Gain (R/W)
U	150 V/V Read Mode Gain (R/W)
V	200 V/V Read Mode Gain (R/W)
W	250 V/V Read Mode Gain (R/W)
X	300 V/V Read Mode Gain (R/W)
Y	350 V/V Read Mode Gain (R/W)
Z	400 V/V Read Mode Gain (R/W)

Cannot use A-E in left position

Modifiers are listed in hierarchical order.

PACKAGE TYPE

C	Side-Brazed Ceramic
F	Flatpack
G	QFP, Quad Flatpack, Plastic EIAJ (1.4mm)
GE	Deep Downset Power Pad Thin Quad Flatpack (1 mm)
GF	TQFP, Fused Thin Quad Flatpack (1.4 mm)
GT	TQFP, Thin Quad Flatpack, Plastic (1.4 mm)
GU	Ultra Thin Quad Flatpack, Plastic (0.7 mm)
GV	Very Thin Quad Flatpack, Plastic (1 mm)
H	PLCC, Quad Plastic
IB	Bumped Die Sales (Flip Chip)
IO	Standard Die Sales
L	Small Outline, Large (300 mil.)
M	Small Outline, (300 mil.), Fine Pitch (0.8 mm)
N	Small Outline, Narrow (150 mil.)
P	Plastic Dip
S	Plastic, Narrow Dip
V	Very Small Outline (220 mil.) Fine Pitch (0.65 mm)
VT	Very Thin Small Outline (1 mm)
W	Small Outline, Wide (400 mil.)

Exception:
Demo Kit Marketing Part Number

* 30 replacing any 3x prefix refers to custom proprietary product

** Release level should only be used to define enhancement to parametric performance, cannot be used for functional changes. Functional changes to a part should be defined as a new marketing number.

Δ Refers to products existing as of November 1997 and any subsequent product revisions

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