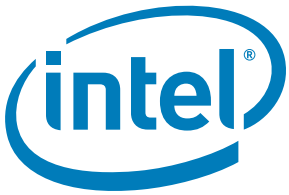

Dual-Core Intel® Xeon® Processor 5100 Series

Datasheet

August 2007

Reference Number: 313355-003

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Contents

Figures

Table

Revision History

Revision	Description	Date
001	Initial release	June 2006
002	Updated Sections 2, 3, and 6 with SKUs for 5148/5138/5128	November 2006
003	Updated Sections 2, 3, and 6 with G-step information.	August 2007

§

1 Introduction

The Dual-Core Intel® Xeon® Processor 5100 Series are 64-bit server/workstation processors utilizing two Intel microarchitecture cores. These processors are based on Intel's 65 nanometer process technology combining high performance with the power efficiencies of a low-power microarchitecture. The Dual-Core Intel® Xeon® Processor 5100 Series maintain the tradition of compatibility with IA-32 software. Some key features include on-die, 32 KB Level 1 instruction and data caches and 4 MB Level 2 cache with Advanced Transfer Cache Architecture. The processors' Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance. The 1333 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 333 MHz system clock making 10.66 GBytes per second data transfer rates possible. Some lower speed SKU's are available which support a 1066 MHz Front Side Bus (FSB). This is a quad-pumped bus running off a 266 MHz system clock making 8.5 GBytes per second data transfer rates possible. The Dual-Core Intel® Xeon® Processor 5160 offers higher clock frequencies than the Dual-Core Intel® Xeon® Processor 5100 Series for platforms that are targeted for the performance optimized segment.

Enhanced thermal and power management capabilities are implemented including Thermal Monitor (TM1), Thermal Monitor 2 (TM2) and Enhanced Intel SpeedStep® Technology. These technologies are targeted for dual processor in enterprise environments. TM1 and TM2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep® Technology provides power management capabilities to servers and workstations.

Dual-Core Intel® Xeon® Processor 5100 Series features include Advanced Dynamic Execution, enhanced floating point and multi-media units, Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE3 instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations.

The Dual-Core Intel® Xeon® Processor 5100 Series support Intel® Extended Memory 64 Technology (Intel® EM64T) as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology. Further details on Intel Extended Memory 64 Technology and its programming model can be found in the *64-bit Extension Technology Software Developer's Guide* at http://developer.intel.com/technology/64bitextensions/.

In addition, the Dual-Core Intel® Xeon® Processor 5100 Series support the Execute Disable Bit functionality. When used in conjunction with a supporting operating system, Execute Disable allows memory to be marked as executable or non executable. This feature can prevent some classes of viruses that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. Further details on Execute Disable can be found at http://www.intel.com/cd/ids/developer/asmo-na/eng/149308.htm.

The Dual-Core Intel® Xeon® Processor 5100 Series support Intel® Virtualization Technology for hardware-assisted virtualization within the processor. Intel Virtualization Technology is a set of hardware enhancements that can improve virtualization solutions. Intel Virtualization Technology is used in conjunction with Virtual Machine

Monitor software enabling multiple, independent software environments inside a single platform. Further details on Intel Virtualization Technology can be found at http://developer.intel.com/technology/vt.

The Dual-Core Intel® Xeon® Processor 5100 Series are intended for high performance server and workstation systems. The Dual-Core Intel® Xeon® Processor 5100 Series support a Dual Independent Bus (DIB) architecture with one processor on each bus, up to two processor sockets in a system. The DIB architecture provides improved performance by allowing increased FSB speeds and bandwidth. The Dual-Core Intel® Xeon® Processor 5100 Series are packaged in an FC-LGA6 Land Grid Array package with 771 lands for improved power delivery. It utilizes a surface mount LGA771 socket that supports Direct Socket Loading (DSL).

Table 1-1. Dual-Core Intel® Xeon® Processor 5100 Series

# of Processor Cores	L1 Cache	L2 Advanced Transfer Cache	Front Side Bus Frequencies	Package
2	32 KB instruction 32 KB data	4 MB shared	1333 MHz 1066 MHz	FC-LGA6 771 Lands

The Dual-Core Intel® Xeon® Processor 5100 Series based platforms implement independent core voltage (V_{CC}) power planes for each processor. FSB termination voltage (V_{TT}) is shared and must connect to all FSB agents. The processor core voltage utilizes power delivery guidelines specified by VRM/EVRD 11.0 and its associated load line (see *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for further details). VRM/EVRD 11.0 will support the power requirements of all frequencies of the Dual-Core Intel® Xeon® Processor 5100 Series. Refer to the appropriate platform design guidelines for implementation details.

The Dual-Core Intel® Xeon® Processor 5100 Series support 1333 MHz Front Side Bus operation. The Dual-Core Intel® Xeon® Processor LV 5138 and Dual-Core Intel® Xeon® Processor LV 5128 support 1066MHz Front Side Bus operation. The FSB utilizes a split-transaction, deferred reply protocol and Source-Synchronous Transfer (SST) of address and data to improve performance. The processor transfers data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a 'double-clocked' or a 2X address bus. In addition, the Request Phase completes in one clock cycle. The FSB is also used to deliver interrupts.

Signals on the FSB use Assisted Gunning Transceiver Logic (AGTL+) level voltages. Section 2.1 contains the electrical specifications of the FSB while implementation details are fully described in the appropriate platform design guidelines (refer to Section 1.3).

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

Commonly used terms are explained here for clarification:

- **Dual-Core Intel® Xeon® Processor 5100 Series** – Intel 64-bit microprocessor intended for dual processor servers and workstations. The Dual-Core Intel® Xeon® Processor 5100 Series are based on Intel's 65 nanometer process, in the FC-LGA6 package with two processor cores. For this document, "processor" is used as the generic term for the Dual-Core Intel® Xeon® Processor 5100 Series.
- **Dual-Core Intel® Xeon® Processor LV 5148, Dual-Core Intel® Xeon® Processor LV 5138 and Dual-Core Intel® Xeon® Processor LV 5128-** Intel 64-bit microprocessor intended for dual processor server blades and embedded servers requiring higher case temperatures. The Dual-Core Intel® Xeon® Processor LV 5148, Dual-Core Intel® Xeon® Processor LV 5138, and Dual-Core Intel® Xeon® Processor LV 5128 are lower voltage, lower power version of the Dual-Core Intel® Xeon® Processor 5100 Series. For this document "Dual-Core Intel® Xeon® Processor LV 5148/5138/5128" is used to call out specifications that are unique to the Dual-Core Intel® Xeon® Processor LV 5148/5138/5128 SKU.
- **Dual-Core Intel® Xeon® Processor 5160**- A performance optimized version of the Dual-Core Intel® Xeon® Processor 5100 Series. For this document "Dual-Core Intel® Xeon® Processor 5160" is used to call out specifications that are unique to the Dual-Core Intel® Xeon® Processor 5160 SKU.
- **FC-LGA6 (Flip Chip Land Grid Array) Package** – The Dual-Core Intel® Xeon® Processor 5100 Series package is a Land Grid Array, consisting of a processor core mounted on a pinless substrate with 771 lands, and includes an integrated heat spreader (IHS).
- **LGA771 socket** – The Dual-Core Intel® Xeon® Processor 5100 Series interfaces to the baseboard through this surface mount, 771 Land socket. See the *LGA771 Socket Design Guidelines* for details regarding this socket.
- **Processor core** – Processor core with integrated L1 cache. L2 cache and system bus interface are shared between the two cores on the die. All AC timing and signal integrity specifications are at the pads of the processor core.
- **FSB (Front Side Bus)** – The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
- **Dual Independent Bus (DIB)** – A front side bus architecture with one processor on each bus, rather than a FSB shared between two processor agents. The DIB architecture provides improved performance by allowing increased FSB speeds and bandwidth.
- **Flexible Motherboard Guidelines (FMB)** – Are estimates of the maximum values the Dual-Core Intel® Xeon® Processor 5100 Series will have over certain time periods. The values are only estimates and actual specifications for future processors may differ.
- **Functional Operation** – Refers to the normal operating conditions in which all processor specifications, including DC, AC, FSB, signal quality, mechanical and thermal are satisfied.
- **Storage Conditions** – Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.

- **Priority Agent** – The priority agent is the host bridge to the processor and is typically known as the chipset.
- **Symmetric Agent** – A symmetric agent is a processor which shares the same I/O subsystem and memory array, and runs the same operating system as another processor in a system. Systems using symmetric agents are known as Symmetric Multiprocessing (SMP) systems.
- **Integrated Heat Spreader (IHS)** – A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Thermal Design Power** – Processor thermal solutions should be designed to meet this target. It is the highest expected sustainable power while running known power intensive real applications. TDP is not the maximum power that the processor can dissipate.
- **Intel® Extended Memory 64 Technology (Intel® EM64T)** – An enhancement to Intel's IA-32 architecture that allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology. Further details on can be found in the 64-bit Extension Technology Software Developer's Guide at http://developer.intel.com/.
- **Enhanced Intel SpeedStep® Technology (EIST)** – Technology that provides power management capabilities to servers and workstations.
- **Platform Environment Control Interface (PECI)** – A proprietary one-wire bus interface that provides a communication channel between Intel processor and chipset components to external thermal monitoring devices, for use in fan speed control. PECI communicates readings from the processor's digital thermal sensor. PECI replaces the thermal diode available in previous processors.
- **Intel® Virtualization Technology** – Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
- **VRM (Voltage Regulator Module)** – DC-DC converter built onto a module that interfaces with a card edge socket and supplies the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **EVRD (Enterprise Voltage Regulator Down)** – DC-DC converter integrated onto the system board that provides the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **V_{CC}** – The processor core power supply.
- **V_{SS}** – The processor ground.
- **V_{TT}** – FSB termination voltage. (Note: In some Intel processor EMTS documents, V_{TT} is instead called V_{CCP}.)

1.2 State of Data

The data contained within this document is the most accurate information available by the publication date of this document. Values are subject to change prior to production.

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document:

2 Electrical Specifications

2.1 Front Side Bus and GTLREF

Most Dual-Core Intel® Xeon® Processor 5100 Series FSB signals uses Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active PMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Platforms implement a termination voltage level for AGTL+ signals defined as V_{TT}. Because platforms implement separate power planes for each processor (and chipset), separate V_{CC} and V_{TT} supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address buses have made signal integrity considerations and platform design methods even more critical than with previous processor families. Design guidelines for the processor FSB are detailed in the appropriate platform design guidelines (refer to Section 1.3).

The AGTL+ inputs require reference voltages (GTLREF_DATA and GTLREF_ADD) which are used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF_DATA is used for the 4X front side bus signaling group and GTLREF_ADD is used for the 2X and common clock front side bus signaling groups. Both GTLREF_DATA and GTLREF_ADD must be generated on the baseboard. Refer to the applicable platform design guidelines for details. Termination resistors (R_{TT}) for AGTL+ signals are provided on the processor silicon and are terminated to V_{TT}. The on-die termination resistors are always enabled on the Dual-Core Intel® Xeon® Processor 5100 Series to control reflections on the transmission line. Intel chipsets also provide on-die termination, thus eliminating the need to terminate the bus on the baseboard for most AGTL+ signals.

Some FSB signals do not include on-die termination (R_{TT}) and must be terminated on the baseboard. See Table 2-9 for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system. Contact your Intel Field Representative to obtain the processor signal integrity models, which includes buffer and package models.

2.2 Power and Ground Lands

For clean on-chip processor core power distribution, the processor has 223 V_{CC} (power) and 273 V_{SS} (ground) inputs. All Vcc lands must be connected to the processor power plane, while all V_{SS} lands must be connected to the system ground plane. The processor V_{CC} lands must be supplied with the voltage determined by the processor **V**oltage **ID**entification (VID) signals. See Table 2-3 for VID definitions.

Twenty two lands are specified as V_{TT}, which provide termination for the FSB and provides power to the I/O buffers. The platform must implement a separate supply for these lands which meets the V_{TT} specifications outlined in Table 2-13.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the Dual-Core Intel® Xeon® Processor 5100 Series are capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-13. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and guidelines, refer to the appropriate platform design guidelines.

2.3.1 V_{CC} Decoupling

Vcc regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR), and the baseboard designer must assure a low interconnect resistance from the regulator (EVRD or VRM pins) to the LGA771 socket. Bulk decoupling must be provided on the baseboard to handle large current swings. The power delivery solution must insure the voltage and current specifications are met (as defined in Table 2-13). For further information regarding power delivery, decoupling and layout guidelines, refer to the appropriate platform design guidelines.

2.3.2 V_{TT} Decoupling

Bulk decoupling must be provided on the baseboard. Decoupling solutions must be sized to meet the expected load. To insure optimal performance, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution consists of a combination of low ESR bulk capacitors and high frequency ceramic capacitors. For further information regarding power delivery, decoupling and layout guidelines, refer to the appropriate platform design guidelines.

2.3.3 Front Side Bus AGTL+ Decoupling

The Dual-Core Intel® Xeon® Processor 5100 Seriesintegrates signal termination on the die, as well as a portion of the required high frequency decoupling capacitance on the processor package. However, additional high frequency capacitance must be added to the baseboard to properly decouple the return currents from the FSB. Bulk decoupling must also be provided by the baseboard for proper AGTL+ bus operation. Decoupling guidelines are described in the appropriate platform design guidelines.

2.4 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous processor generations, the Dual-Core Intel® Xeon® Processor 5100 Series core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier is set during manufacturing. The default setting is for the maximum speed of the processor. It is possible to override this setting using software (see the *Conroe and Woodcrest Processor Family BIOS Writer's Guide*). This permits operation at lower frequencies than the processor's tested frequency.

The processor core frequency is configured during reset by using values stored internally during manufacturing. The stored value sets the highest bus fraction at which the particular processor can operate. If lower speeds are desired, the appropriate ratio can be configured via the CLOCK_FLEX_MAX MSR. For details of operation at core frequencies lower than the maximum rated processor speed, refer to the *Conroe and Woodcrest Processor Family BIOS Writer's Guide.*

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK[1:0] input, with exceptions for spread spectrum clocking. The Dual-Core Intel® Xeon® Processor 5100 Series utilizes differential clocks. Details regarding BCLK[1:0] driver specifications are provided in the *CK410B Clock Synthesizer/Driver Design Guidelines.* Table 2-1 contains processor core frequency to FSB multipliers and their corresponding core frequencies.

Table 2-1. Core Frequency to FSB Multiplier Configuration

Core Frequency to FSB Multiplier	Core Frequency with 266 MHz FSB Clock	Processor	Notes
1/6	1.60 GHz	5110	1, 2, 3, 4
1/7	1.86 GHz	5120/5128	1, 2, 3
1/8	2.13 GHz	5138	1, 2, 3

Core Frequency to FSB Multiplier	Core Frequency with 333 MHz FSB Clock	Processor	Notes
1/6	2.0 GHz	5130	1, 2, 3, 4
1/7	2.33 GHz	5140/5148	1, 2, 3
1/8	2.66 GHz	5150	1, 2, 3
1/9	3.0 GHz	5160	1, 2, 3

Notes:
1. Listed frequencies illustrate clock frequency multipliers and are not necessarily committed production frequencies for 40 W, 65 W or 80 W versions of Dual-Core Intel® Xeon® Processor 5100 Series.
2. Individual processors operate only at or below the frequency marked on the package.
3. For valid processor core frequencies, refer to the *Dual-Core Intel® Xeon® Processor 5100 Series Specification Update*.
4. The lowest bus ratio supported by the Dual-Core Intel® Xeon® Processor 5100 Seriesis 1/6.

2.4.1 Front Side Bus Frequency Select Signals (BSEL[2:0])

Upon power up, the FSB frequency is set to the maximum supported by the individual processor. BSEL[2:0] are CMOS outputs which must be pulled up to V_{TT}, and are used to select the FSB frequency. Please refer to Table 2-16 for DC specifications. Table 2-2 defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), chipset, and clock synthesizer. All FSB agents must operate at the same core and FSB frequency. See the appropriate platform design guidelines for further details.

Table 2-2. BSEL[2:0] Frequency Table (Sheet 1 of 2)

BSEL2	BSEL1	BSEL0	Bus Clock Frequency
0	0	0	266.666 MHz
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	333.333 MHz

2.4.2 PLL Power Supply

An on-die PLL filter solution is implemented on the Dual-Core Intel® Xeon® Processor 5100 Series. The V_{CCPLL} input is used for this configuration in Dual-Core Intel® Xeon® Processor 5100 Series based platforms. Please refer to Table 2-13 for DC specifications. Refer to the appropriate platform design guidelines for decoupling and routing guidelines.

2.5 Voltage Identification (VID)

The Voltage Identification (VID) specification for the Dual-Core Intel® Xeon® Processor 5100 Series is defined by the *Voltage Regulator Module (VRM) and Enterprise Voltage*

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-3. Voltage Identification Definition

VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	V_{CC_MAX}		VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	V_{CC_MAX}
1	1	1	1	0	1	0.8500		0	1	1	1	1	0	1.2375
1	1	1	1	0	0	0.8625		0	1	1	1	0	1	1.2500
1	1	1	0	1	1	0.8750		0	1	1	1	0	0	1.2625
1	1	1	0	1	0	0.8875		0	1	1	0	1	1	1.2750
1	1	1	0	0	1	0.9000		0	1	1	0	1	0	1.2875
1	1	1	0	0	0	0.9125		0	1	1	0	0	1	1.3000
1	1	0	1	1	1	0.9250		0	1	1	0	0	0	1.3125
1	1	0	1	1	0	0.9375		0	1	0	1	1	1	1.3250
1	1	0	1	0	1	0.9500		0	1	0	1	1	0	1.3375
1	1	0	1	0	0	0.9625		0	1	0	1	0	1	1.3500
1	1	0	0	1	1	0.9750		0	1	0	1	0	0	1.3625
1	1	0	0	1	0	0.9875		0	1	0	0	1	1	1.3750
1	1	0	0	0	1	1.0000		0	1	0	0	1	0	1.3875
1	1	0	0	0	0	1.0125		0	1	0	0	0	1	1.4000
1	0	1	1	1	1	1.0250		0	1	0	0	0	0	1.4125
1	0	1	1	1	0	1.0375		0	0	1	1	1	1	1.4250
1	0	1	1	0	1	1.0500		0	0	1	1	1	0	1.4375
1	0	1	1	0	0	1.0625		0	0	1	1	0	1	1.4500
1	0	1	0	1	1	1.0750		0	0	1	1	0	0	1.4625
1	0	1	0	1	0	1.0875		0	0	1	0	1	1	1.4750
1	0	1	0	0	1	1.1000		0	0	1	0	1	0	1.4875
1	0	1	0	0	0	1.1125		0	0	1	0	0	1	1.5000
1	0	0	1	1	1	1.1250		0	0	1	0	0	0	1.5125
1	0	0	1	1	0	1.1375		0	0	0	1	1	1	1.5250
1	0	0	1	0	1	1.1500		0	0	0	1	1	0	1.5375
1	0	0	1	0	0	1.1625		0	0	0	1	0	1	1.5500
1	0	0	0	1	1	1.1750		0	0	0	1	0	0	1.5625
1	0	0	0	1	0	1.1875		0	0	0	0	1	1	1.5750
1	0	0	0	0	1	1.2000		0	0	0	0	1	0	1.5875
1	0	0	0	0	0	1.2125		0	0	0	0	0	1	1.6000
0	1	1	1	1	1	1.2250		0	0	0	0	0	0	OFF

Table 2-4. Voltage Identification Definition

HEX	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	V_{CC_MAX}	HEX	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	V_{CC_MAX}
7A	1	1	1	1	0	1	0.8500	3C	0	1	1	1	1	0	1.2375
78	1	1	1	1	0	0	0.8625	3A	0	1	1	1	0	1	1.2500
76	1	1	1	0	1	1	0.8750	38	0	1	1	1	0	0	1.2625
74	1	1	1	0	1	0	0.8875	36	0	1	1	0	1	1	1.2750
72	1	1	1	0	0	1	0.9000	34	0	1	1	0	1	0	1.2875
70	1	1	1	0	0	0	0.9125	32	0	1	1	0	0	1	1.3000
6E	1	1	0	1	1	1	0.9250	30	0	1	1	0	0	0	1.3125
6C	1	1	0	1	1	0	0.9375	2E	0	1	0	1	1	1	1.3250
6A	1	1	0	1	0	1	0.9500	2C	0	1	0	1	1	0	1.3375
68	1	1	0	1	0	0	0.9625	2A	0	1	0	1	0	1	1.3500
66	1	1	0	0	1	1	0.9750	28	0	1	0	1	0	0	1.3625
64	1	1	0	0	1	0	0.9875	26	0	1	0	0	1	1	1.3750
62	1	1	0	0	0	1	1.0000	24	0	1	0	0	1	0	1.3875
60	1	1	0	0	0	0	1.0125	22	0	1	0	0	0	1	1.4000
5E	1	0	1	1	1	1	1.0250	20	0	1	0	0	0	0	1.4125
5C	1	0	1	1	1	0	1.0375	1E	0	0	1	1	1	1	1.4250
5A	1	0	1	1	0	1	1.0500	1C	0	0	1	1	1	0	1.4375
58	1	0	1	1	0	0	1.0625	1A	0	0	1	1	0	1	1.4500
56	1	0	1	0	1	1	1.0750	18	0	0	1	1	0	0	1.4625
54	1	0	1	0	1	0	1.0875	16	0	0	1	0	1	1	1.4750
52	1	0	1	0	0	1	1.1000	14	0	0	1	0	1	0	1.4875
		0	1	0	0	0	1.1125	12	0	0	1	0	0	1	1.5000
		0	0	1	1	1	1.1250	10	0	0	1	0	0	0	1.5125
		0	0	1	1	0	1.1375	0E	0	0	0	1	1	1	1.5250
		0	0	1	0	1									

1111" VID pattern is observed, the voltage regulator output should be disabled.
tes the expected VID range of the Dual-Core Intel® Xeon® Processor 5100 Series.
e includes VID transitions that may be initiated by thermal events, assertion of the FORCEPR# signal (see
.2), Extended HALT state transitions (see Section 7.2.2), or Enhanced Intel SpeedStep® Technology transitions
7.3). **The Extended HALT state must be enabled for the processor to remain within its specifications.**
M/EVRD is operating after power-up, if either the Output Enable signal is de-asserted or a specific VID off code is
VRM/EVRD must turn off its output (the output should go to high impedance) within 500 ms and latch off until
ed. Refer to *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design*

Table 2-5. Loadline Selection Truth Table for LL_ID[1:0]

LL_ID1	LL_ID0	Description
0	0	Reserved
0	1	Dual-Core Intel® Xeon® Processor 5100 Series
1	0	Reserved
1	1	Reserved

Note: The LL_ID[1:0] signals are used to select the correct loadline slope for the processor.

Table 2-6. Market Segment Selection Truth Table for MS_ID[1:0]

MS_ID1	MS_ID0	Description
0	0	Reserved
0	1	Dual-Core Intel® Xeon® Processor 5100 Series
1	0	Reserved
1	1	Reserved

Note: The MS_ID[1:0] signals are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying.

2.6 Reserved or Unused Signals

All Reserved signals must remain unconnected. Connection of these signals to V_{CC}, V_{TT}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 4 for a land listing of the processor and the location of all Reserved signals.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active high inputs, should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected; however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the baseboard trace for FSB signals, unless otherwise noticed in the appropriate platform design guidelines. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}).

Some TAP, CMOS Asynchronous inputs and CMOS Asynchronous outputs do not include on-die termination. Inputs and utilized outputs must be terminated on the baseboard. Unused outputs may be terminated on the baseboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the appropriate platform design guidelines.

Each of the TESTHI signals must be tied to the processor V_{TT} individually using a matched resistor, where a matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, if the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω is required.

2.7 Front Side Bus Signal Groups

The FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF_DATA and GTLREF_ADD as reference levels. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. AGTL+ asynchronous outputs can become active anytime and include an active PMOS pull-up transistor to assist during the first clock of a low-to-high voltage transition.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals whose timings are specified with respect to rising edge of BCLK0 (ADS#, HIT#, HITM#, and so forth) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, and so forth) and can become active at any time during the clock cycle. Table 2-7 identifies which signals are common clock, source synchronous and asynchronous.

Table 2-7. FSB Signal Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#;
AGTL+ Common Clock Output	Synchronous to BCLK[1:0]	BPM4#, BPM[2:1]#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#, BINIT#[2], BNR#[2], BPM5#, BPM3#, BPM0#, BR[1:0]#, DBSY#, DP[3:0]#, DRDY#, HIT#[2], HITM#[2], LOCK#, MCERR#[2]
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#,A[16:3]#</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes I/O	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Open Drain Output	Asynchronous	FERR#/PBE#, IERR#, PROCHOT#, THERMTRIP#
CMOS Asynchronous Input	Asynchronous	A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, STPCLK#,
CMOS Asynchronous Output	Asynchronous	BSEL[2:0], VID[6:1]
FSB Clock	Clock	BCLK[1:0]
TAP Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output	Synchronous to TCK	TDO
Power/Other	Power/Other	GTLREF_ADD_MID, GTLREF_ADD_END, GTLREF_DATA_MID, GTLREF_DATA_END, LL_ID[1:0], MS_ID[1:0], PECI, RESERVED, SKTOCC#, TESTHI[11:0], TESTIN1, TESTIN2, VCC, VCC_DIE_SENSE, VCC_DIE_SENSE2, VCCPLL, VID_SELECT, VSS_DIE_SENSE, VSS_DIE_SENSE2, VSS, VTT, VTT_OUT, VTT_SEL

Notes:
1. Refer to Section 5 for signal descriptions.
2. These signals may be driven simultaneously by multiple agents (Wired-OR).

Table 2-9 outlines the signals which include on-die termination (R_{TT}). Table 2-9 outlines non AGTL+ signals including open drain signals. Table 2-10 provides signal reference voltages.

Table 2-8. AGTL+ Signal Description Table

AGTL+ signals with R_{TT}	AGTL+ signals with no R_{TT}
A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, LOCK#, MCERR#, REQ[4:0]#, RS[2:0]#, RSP#	BPM[5:0]#, RESET#

Table 2-9. Non AGTL+ Signal Description Table

Signals with R_{TT}	Signals with no R_{TT}
FORCEPR#[1], PROCHOT#[1]	A20M#, BCLK[1:0], BSEL[2:0], FERR#/PBE#, GTLREF_ADD, GTLREF_DATA, IERR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, LL_ID[1:0], MS_ID[1:0], PECI, PWRGOOD, SKTOCC#, SMI#, STPCLK#, TCK, TDI, TDO, TESTHI[11:0], THERMTRIP#, TMS, TRDY#, TRST#, VCC_DIE_SENSE, VCC_DIE_SENSE2, VID[6:1], VID_SELECT, VSS_DIE_SENSE, VSS_DIE_SENSE2, VTT_SEL

Note:
1. Signals that have RTT in the package with 50 Ω pullup to V_{TT}.

Table 2-10. Signal Reference Voltages

GTLREF	CMOS
A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BPRI#, BR[1:0]#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#, HIT#, HITM#, LOCK#, MCERR#, RESET#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#	A20M#, LINT0/INTR, LINT1/NMI, IGNNE#, INIT#, PWRGOOD, SMI#, STPCLK#, TCK, TDI, TMS, TRST#

2.8 CMOS Asynchronous and Open Drain Asynchronous Signals

Legacy input signals such as A20M#, IGNNE#, INIT#, SMI#, and STPCLK# utilize CMOS input buffers. Legacy output signals such as FERR#/PBE#, IERR#, PROCHOT#, and THERMTRIP# utilize open drain output buffers. All of the CMOS and Open Drain signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Chapter 6 for additional timing requirements for entering and leaving the low power states.

2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor(s) be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of

accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TMS, TDO, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

2.10 Platform Environmental Control Interface (PECI) DC Specifications

The release of the Dual-Core Intel® Xeon® Processor 5100 Series marks the transition from thermal diodes to digital thermal sensors for fan speed control. Digital Thermal Sensors (DTS) are on-die, analog-to-digital temperature converters calibrated at the factory for reasonable accuracy to provide a digital representation of relative processor temperature. Data from the DTS are processed and stored in a processor register, which is queried through the Platform Environment Control Interface (PECI). PECI is a proprietary one-wire bus interface that provides a communication channel between Intel processor and chipset components to external thermal monitoring devices. More detailed information may be found in Section 6.3.

2.10.1 DC Characteristics

A PECI device interface operates at a nominal voltage set by V_{TT}. The set of DC electrical specifications shown in Table 2-11 is used with devices normally operating from a V_{TT} interface supply. V_{TT} nominal levels will vary between processor families. All PECI devices will operate at the V_{TT} level determined by the processor installed in the system. For specific nominal V_{TT} levels, refer to the appropriate processor EMTS.

Table 2-11. PECI DC Electrical Limits

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_{in}	Input Voltage Range	-0.150	V_{TT} + 0.150	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{TT}	N/A	V	
V_n	Negative-edge threshold voltage	0.275 * V_{TT}	0.500 * V_{TT}	V	
V_p	Positive-edge threshold voltage	0.550 * V_{TT}	0.725 * V_{TT}	V	
I_{source}	High level output source (V_{OH} = 0.75 * V_{TT})	-6.0	N/A	mA	
I_{sink}	Low level output sink (V_{OL} = 0.25 * V_{TT})	0.5	1.0	mA	
I_{leak+}	High impedance state leakage to V_{TT} (V_{leak} = V_{OL})	N/A	50	µA	2
I_{leak-}	High impedance leakage to GND (V_{leak} = V_{OH})	N/A	10	µA	2
C_{bus}	Bus capacitance	N/A	10	pF	
V_{noise}	Signal noise immunity above 300 MHz	0.1 * V_{TT}	N/A	V_{p-p}	

Note:
1. V_{TT} supplies the PECI interface. PECI behavior does not affect V_{TT} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.

2.10.2 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 2-1 as a guide for input buffer design.

2.11 Mixing Processors

Intel supports and validates dual processor configurations only in which both processors operate with the same FSB frequency, core frequency, power segments, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel. Combining processors from different power segments is also not supported.

Figure 8-2. Boxed Dual-Core Intel® Xeon® Processor 5100 Series 2U Passive Heat Sink

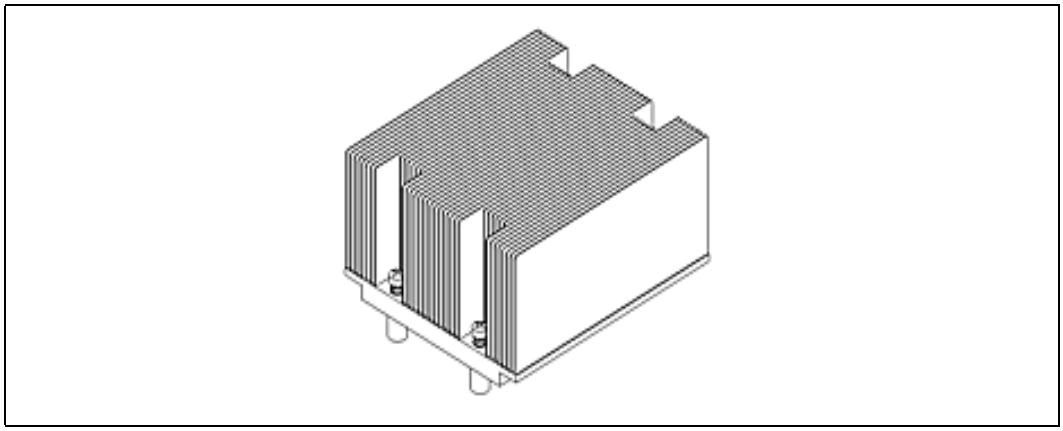
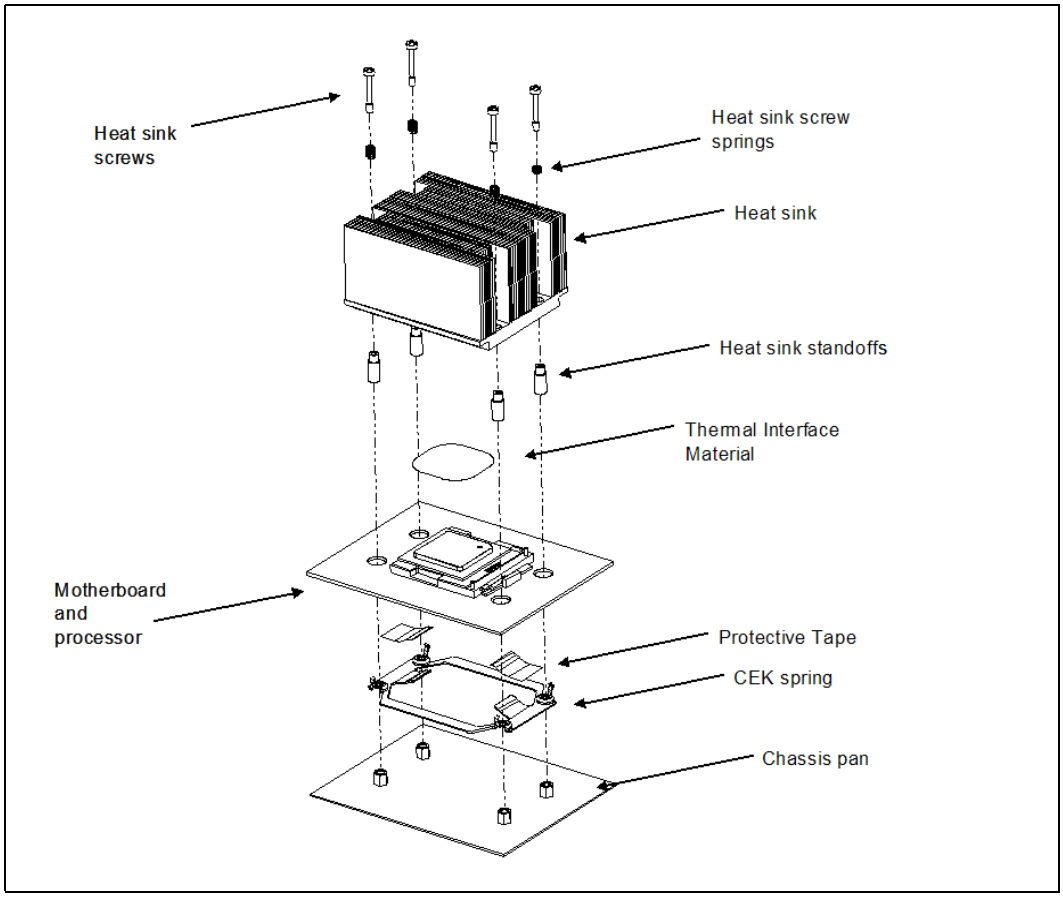


Figure 8-3. 2U Passive Dual-Core Intel® Xeon® Processor 5100 Series Thermal Solution (Exploded View)



Notes:
1. The heat sinks represented in these images are for reference only, and may not represent the final boxed processor heat sinks.
2. The screws, springs, and standoffs will be captive to the heat sink. This image shows all of the components in an exploded view.
3. It is intended that the CEK spring will ship with the base board and be pre-attached prior to shipping.

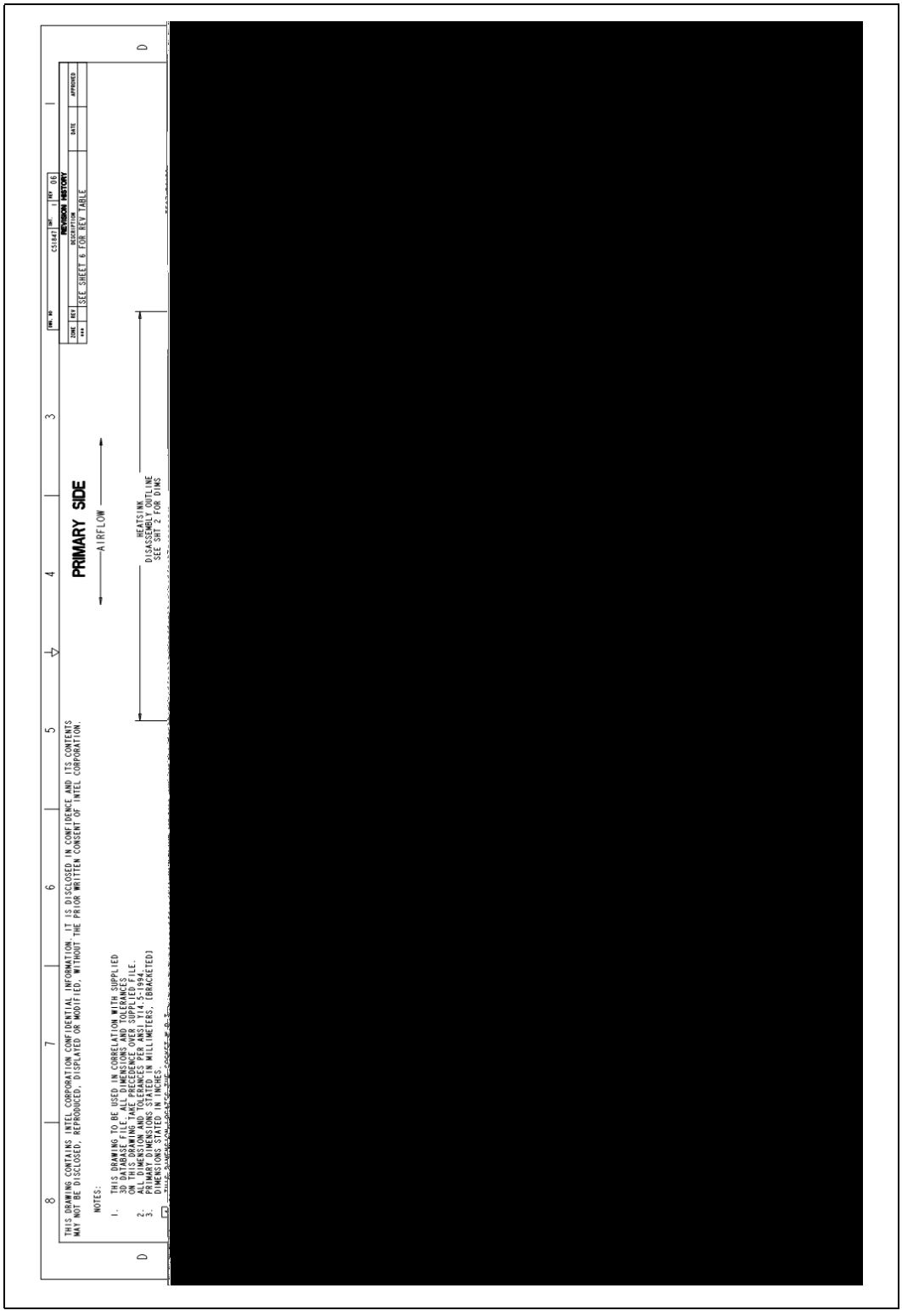
8.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed processor.

8.2.1 Boxed Processor Heat Sink Dimensions (CEK)

The boxed processor will be shipped with an unattached thermal solution. Clearance is required around the thermal solution to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor and assembled heat sink are shown in Figure 8-4 through Figure 8-8. Figure 8-9 through Figure 8-10 are the mechanical drawings for the 4-pin board fan header and 4-pin connector used for the active CEK fan heat sink solution.

Figure 8-4. Top Side Board Keepout Zones (Part 1)



8.2.2 Boxed Processor Heat Sink Weight

8.2.2.1 Thermal Solution Weight

The 1U passive/3U+ active combination heat sink solution and the 2U passive heat sink solution will not exceed a mass of 1050 grams. Note that this is per processor, a dual processor system will have up to 2100 grams total mass in the heat sinks. This large mass will require a minimum chassis stiffness to be met in order to withstand force during shock and vibration.

See Section 3 for details on the processor weight.

8.2.3 Boxed Processor Retention Mechanism and Heat Sink Support (CEK)

Baseboards and chassis designed for use by a system integrator should include holes that are in proper alignment with each other to support the boxed processor. Refer to the Server System Infrastructure Specification (SSI-EEB 3.6, TEB 2.1 or CEB 1.1). These specification can be found at: http://www.ssiforum.org.

Figure 8-3 illustrates the Common Enabling Kit (CEK) retention solution. The CEK is designed to extend air-cooling capability through the use of larger heat sinks with minimal airflow blockage and bypass. CEK retention mechanisms can allow the use of much heavier heat sink masses compared to legacy limits by using a load path directly attached to the chassis pan. The CEK spring on the secondary side of the baseboard provides the necessary compressive load for the thermal interface material. The baseboard is intended to be isolated such that the dynamic loads from the heat sink are transferred to the chassis pan via the stiff screws and standoffs. The retention scheme reduces the risk of package pullout and solder joint failures.

All components of the CEK heat sink solution will be captive to the heat sink and will only require a Phillips screwdriver to attach to the chassis pan. When installing the CEK, the CEK screws should be tightened until they will no longer turn easily. This should represent approximately
6-8 inch-pounds of torque. More than that may damage the retention mechanism components.

8.3 Electrical Requirements

8.3.1 Fan Power Supply (Active CEK)

The 4-pin PWM controlled thermal solution is being offered to help provide better control over pedestal chassis acoustics. This is achieved though more accurate measurement of processor die temperature through the processor's Digital Thermal Sensors. Fan RPM is modulated through the use of an ASIC located on the baseboard, that sends out a PWM control signal to the 4th pin of the connector labeled as Control. This thermal solution requires a constant +12 V supplied to pin 2 of the active thermal solution and does not support variable voltage control or 3-pin PWM control. See Table 8-2 for details on the 4-pin active heat sink solution connectors.

If the 4-pin active fan heat sink solution is connected to an older 3-pin baseboard CPU fan header it will default back to a thermistor controlled mode, allowing compatibility with legacy 3-wire designs. When operating in thermistor controlled mode, fan RPM is automatically varied based on the TINLET temperature measured by a thermistor located at the fan inlet of the heat sink solution.

The fan power header on the baseboard must be positioned to allow the fan heat sink power cable to reach it. The fan power header identification and location must be documented in the suppliers platform documentation, or on the baseboard itself. The baseboard fan power header should be positioned within 177.8 mm [7 in.] from the center of the processor socket.

Table 8-1. PWM Fan Frequency Specifications for 4-Pin Active CEK Thermal Solution

Description	Min Frequency	Nominal Frequency	Max Frequency	Unit
PWM Control Frequency Range	21,000	25,000	28,000	Hz

Table 8-2. Fan Specifications for 4-Pin Active CEK Thermal Solution

Description	Min	Typ Steady	Max Steady	Max Startup	Unit
+12 V: 12 volt fan power supply	10.8	12	12	13.2	V
IC: Fan Current Draw	N/A	1	1.25	1.5	A
SENSE: SENSE frequency	2	2	2	2	Pulses per fan revolution

Figure 8-11. Fan Cable Connector Pin Out for 4-Pin Active CEK Thermal Solution

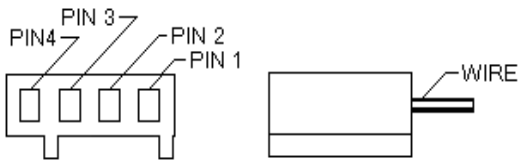


Table 8-3. Fan Cable Connector Pin Out for 4-Pin Active CEK Thermal Solution

Pin Number	Signal	Color
1	Ground	Black
2	**Power:** (+12 V)	Yellow
3	**Sense:** 2 pulses per revolution	Green
4	**Control:** 21 KHz-28 KHz	Blue

8.3.2 Boxed Processor Cooling Requirements

As previously stated the boxed processor will be available in two product configurations. Each configuration will require unique design considerations. Meeting the processor's temperature specifications is also the function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specifications are found in Section 6 of this document.

8.3.2.1 1U Passive / 3U+ Active Combination Heat Sink Solution (1U Rack Passive)

In the 1U configuration it is assumed that a chassis duct will be implemented to provide a minimum airflow of 15 cfm at 0.38 in. H_2O (25.5 m^3/hr at 94.6 Pa) of flow impedance. The duct should be carefully designed to minimize the airflow bypass around the heatsink. It is assumed that a 40°C TLA is met. This requires a superior chassis design to limit the TRISE at or below 5°C with an external ambient temperature of 35°C. Following these guidelines will allow the designer to meet Dual-Core Intel® Xeon® Processor 5100 Series Thermal Profile and conform to the thermal requirements of the processor.

8.3.2.2 1U Passive / 3U+ Active Combination Heat Sink Solution (Pedestal Active)

The active configuration of the combination solution is designed to help pedestal chassis users to meet the thermal processor requirements without the use of chassis ducting. It may be still be necessary to implement some form of chassis air guide or air duct to meet the TLA temperature of 40° C depending on the pedestal chassis layout. Also, while the active thermal solution design will mechanically fit into a 2U volumetric, it may not provide adequate airflow. This is due to the requirement of additional space at the top of the thermal solution to allow sufficient airflow into the heat sink fan. Use of the active configuration in a 2U rackmount chassis is not recommended.

It is recommended that the ambient air temperature outside of the chassis be kept at or below 35°C. The air passing directly over the processor thermal solution should not be preheated by other system components. Meeting the processor's temperature specification is the responsibility of the system integrator.

8.3.2.3 2U Passive Heat Sink Solution (2U+ Rack or Pedestal)

In the 2U+ passive configuration it is assumed that a chassis duct will be implemented to provide a minimum airflow of 27 cfm at 0.182 in. H_2O (45.9 m^3/hr at 45.3 Pa) of flow impedance. The duct should be carefully designed to minimize the airflow bypass around the heatsink. The T_{LA} temperature of 40° C should be met. This may require the use of superior design techniques to keep TRISE at or below 5°C based on an ambient external temperature of 35°C.

8.4 Boxed Processor Contents

A direct chassis attach method must be used to avoid problems related to shock and vibration, due to the weight of the thermal solution required to cool the processor. The board must not bend beyond specification in order to avoid damage. The boxed processor contains the components necessary to solve both issues. The boxed processor will include the following items:

- Dual-Core Intel® Xeon® Processor 5100 Series
- Unattached heat sink solution
- Four screws, four springs, and four heat sink standoffs (all captive to the heat sink)
- Foam air bypass pad and skirt (included with 1U passive/3U+ active solution)
- Thermal interface material (pre-applied on heat sink)
- Installation and warranty manual
- Intel Inside Logo

The other items listed in Figure 8-3 that are required to compete this solution will be shipped with either the chassis or boards. They are as follows:

- CEK Spring (supplied by baseboard vendors)
- Heat sink standoffs (supplied by chassis vendors)

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9 Debug Tools Specifications

Please refer to the *Debug Port Design Guide for UP/DP Systems* and the appropriate platform design guidelines for information regarding debug tool specifications. Section 1.3 provides collateral details.

9.1 Debug Port System Requirements

The Dual-Core Intel® Xeon® Processor 5100 Series debug port is the command and control interface for the In-Target Probe (ITP) debugger. The ITP enables run-time control of the processors for system debug. The debug port, which is connected to the FSB, is a combination of the system, JTAG and execution signals. There are several mechanical, electrical and functional constraints on the debug port that must be followed. The mechanical constraint requires the debug port connector to be installed in the system with adequate physical clearance. Electrical constraints exist due to the mixed high and low speed signals of the debug port for the processor. While the JTAG signals operate at a maximum of 75 MHz, the execution signals operate at the common clock FSB frequency. The functional constraint requires the debug port to use the JTAG system via a handshake and multiplexing scheme.

In general, the information in this chapter may be used as a basis for including all run-control tools in Dual-Core Intel® Xeon® Processor 5100 Series based system designs including tools from vendors other than Intel.

Note: The debug port and JTAG signal chain must be designed into the processor board to utilize the XDP for debug purposes except for interposer solutions.

9.2 Target System Implementation

9.2.1 System Implementation

Specific connectivity and layout guidelines for the Debug Port are provided in the *Debug Port Design Guide for UP/DP Systems* and the appropriate platform design guidelines.

9.3 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Dual-Core Intel® Xeon® Processor 5100 Series systems. Tektronix and Agilent should be contacted to obtain specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Dual-Core Intel® Xeon® Processor 5100 Series based multiprocessor systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing a Dual-Core Intel® Xeon® Processor 5100 Series based system that can make use of an LAI: mechanical and electrical.

9.3.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI plugs into the socket, while the processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include differerent requirements from the space normally occupied by the heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

9.3.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB, therefore it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

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