

Section 1 – Descriptions and Family Characteristics

FACT – Logic

ON Semiconductor FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fan-out capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The sub two-micron silicon gate CMOS process utilized in this family has been proven in the field. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

For direct replacement of LS, ALS and other TTL devices, the 'ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 74ACTXXX devices.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
 - Common Output Structure for Standard and Buffer Drivers
 - Output Sink/Source Current of 24 mA
 - Transmission Line Driving 50 ohm (Commercial) Guaranteed
- Operation from 2–6 Volts Guaranteed
- Temperature Range -40°C to $+85^{\circ}\text{C}$ (Commercial)
- Improved ESD Protection Network
- High Current Latch-Up Immunity

Interfacing

FACT devices have a wide operating voltage range ($V_{CC} = 2$ to 6 Vdc) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

'AC – This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ± 24 mA of I_{OH} and I_{OL} current. Industry standard 'AC nomenclature and pinouts are used.

'ACT – This is a high-speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a

$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ with $V_{OH} = 2.4 \text{ V}$ and $V_{OL} = 0.4 \text{ V}$. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT devices have the same output structures as 'AC devices.

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

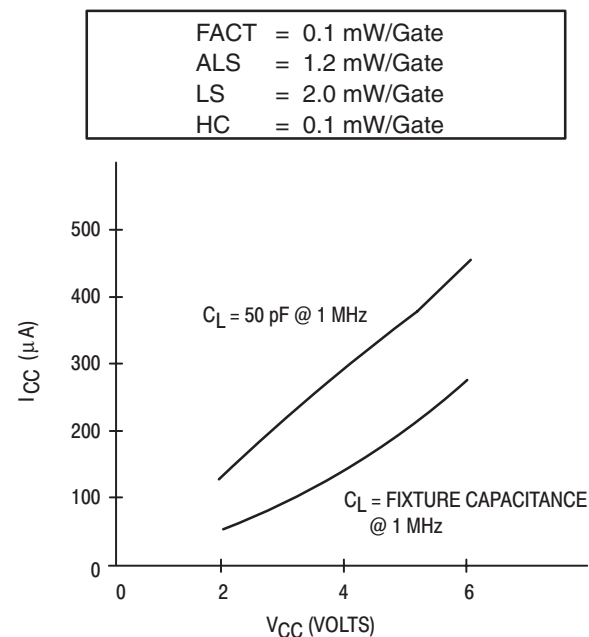


Figure 1-1. I_{CC} versus V_{CC}

Figure 1-1 illustrates the effects of I_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

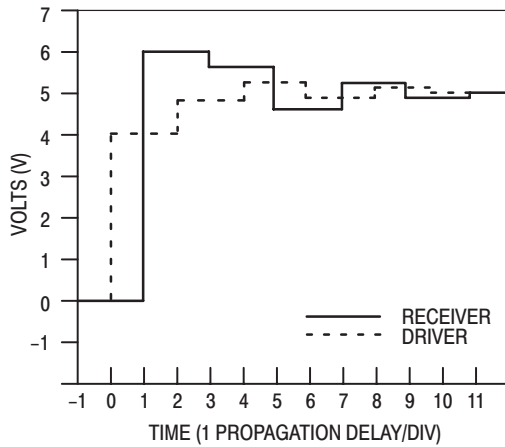


Figure 1-3a. Resultant Waveforms Driving 50 Ohm Line – Theoretical

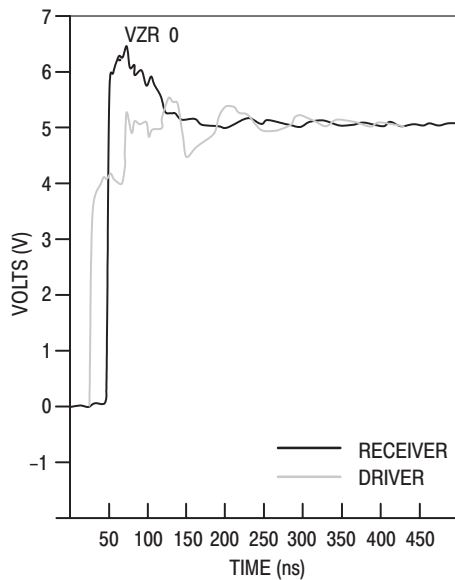


Figure 1-3b. Resultant Waveforms Driving 50 Ohm Line – Actual

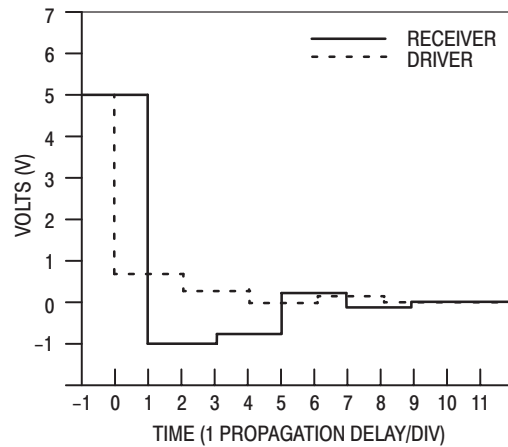


Figure 1-3c. Resultant Waveforms Driving 50 Ohm Line – Theoretical

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figures 1-3a, 1-3b, 1-3c and 1-3d show the resultant wave- forms. Each division on the time scale represents the propagation delay of the transmission line.

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{CC} . The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_0|$ at V_I . For $V_{OQ} = 100$ mV, $V_{IH} = 3.85$ V, $V_{CC} = 5.5$ V and $Z_0 = 50$ ohms, the required I_{OH} at 3.85 V is 75 mA. For the HIGH-to-LOW transition, $V_{OQ} = 5.4$ V, $V_{IL} = 1.35$ V and $Z_0 = 50$ ohms, I_{OL} is 75 mA at 1.65 V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50 ohms, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

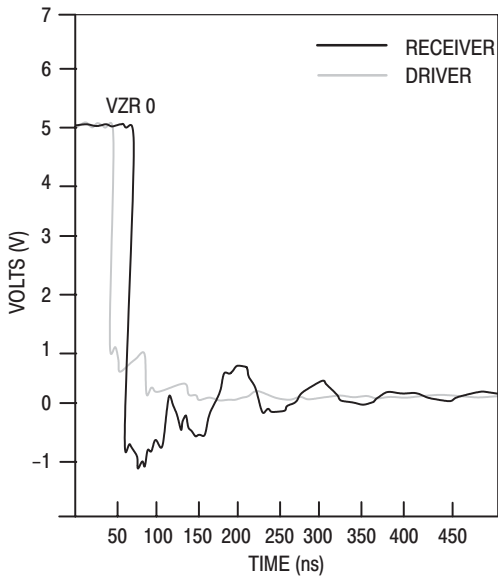


Figure 1-3d. Resultant Waveforms Driving 50 Ohm Line – Actual

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

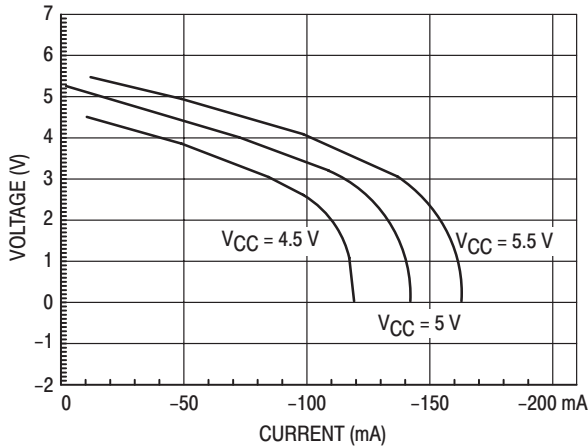


Figure 1-4. Output Characteristics V_{OH}/I_{OH} , MC74AC00

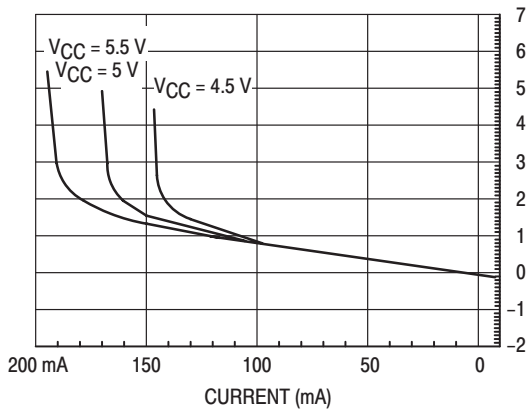


Figure 1-5. Output Characteristics V_{OL}/I_{OL} , MC74AC00

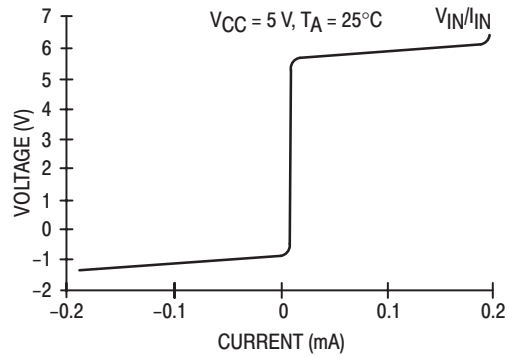


Figure 1-6. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at $3.3 \text{ V} \pm 0.3 \text{ V}$. To this end, ON Semiconductor guarantees all of its devices operational at $3.3 \text{ V} \pm 0.3 \text{ V}$. Note also that AC and DC specifications are guaranteed between 3 and 5.5 V. Operation of FACT logic is also guaranteed from 2 to 6 V on V_{CC} .

Operating Voltage Ranges

FACT	= 2 to 6 V
ALS	= $5 \text{ V} \pm 10\%$
LS	= $5 \text{ V} \pm 5\%$
HC	= 2 to 6 V

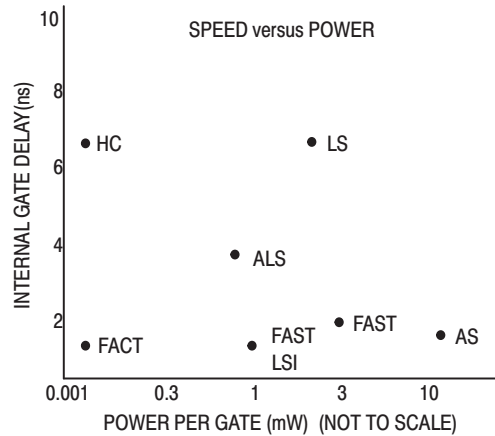


Figure 1-7. Internal Gate Delays

GENERAL CHARACTERISTICS (All Max Ratings)

Symbol	Parameter	LS	ALS	HCMOS	FACT		Unit
					'AC	'ACT	
V _{CC} /EE/DD	Operating Voltage Range	5 ± 5%	5 ± 10%	2 to 6	2 to 6	2 to 6	V
T _A 74 Series	Operating Temperature Range	0 to +70	0 to +70	-40 to +85	-40 to +85	-40 to +85	°C
V _{IH} (min)	Input Voltage (limits)	2	2	3.15	3.15	2	V
V _{IL} (max)		0.8	0.8	0.9	1.35	0.8	V
V _{OH} (min)	Output Voltage (limits)	2.7	2.7	V _{CC} -0.1	V _{CC} -0.1	V _{CC} -0.1	V
V _{OL} (max)		0.5	0.5	0.1	0.1	0.1	V
I _{IH}	Input Current	20	20	+1	+1	+1	μA
I _{IL}		-400	-200	-1	-1	-1	μA
I _{OH}	Output Current at V _O (limit)	-0.4	-0.4	-4 @ V _{CC} -0.8	-24 @ V _{CC} -0.8	-24 @ V _{CC} -0.8	mA
I _{OL}		8	8	4 @ 0.4 V	24 @ 0.4 V	24 @ 0.4 V	mA
DCM	DC Noise Margin LOW/HIGH	0.3/0.7	0.4/0.7	0.8/1.25	1.25/1.25	0.7/2.4	V

Note: All DC parameters are specified over the commercial temperature range.

Figure 1-8. Logic Family Comparisons

FACT Replaces LS, ALS, HCMOS

ON Semiconductor's Advanced CMOS family is specifically designed to outperform the LS, ALS and HCMOS families. Figure 1-7 shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1 μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

SPEED/POWER CHARACTERISTICS (All Typical Ratings)

Symbol	Parameter	LS	ALS	HCMOS	FACT	Unit
I _G	Quiescent Supply Current/Gate	0.4	0.2	0.0005	0.0005	mA
P _G	Power/Gate (Quiescent)	2	1.2	0.0025	0.0025	mW
t _p	Propagation Delay	7	5	8	5	ns
-	Speed Power Product	14	6	0.02	0.01	pJ
f _{max}	Clock Frequency D/FF	33	50	50	160	MHz

PROPAGATION DELAY (Commercial Temperature Range)

	Product		LS	ALS	HCMOS	FACT	Unit
t _{PLH} /t _{PHL}	74XX00	Typ	10	5	8	5	ns
		Max	15	11	23	8.5	ns
t _{PLH} /t _{PHL} (Clock to Q)	74XX74	Typ	25	12	23	8	ns
		Max	40	18	44	10.5	ns
t _{PLH} /t _{PHL} (Clock to Q)	74XX163	Typ	18	10	20	5	ns
		Max	27	17	52	10	ns

Conditions: (LS) V_{CC} = 5 V, C_L = 15 pF, 25°C;

(ALS/HC/FACT) V_{CC} = 5 V, ± 10%, C_L = 50 pF, Typ values at 25°C, Max values at 0 to 70°C for ALS, -40 to +85°C for HC/FACT.

Figure 1-8. Logic Family Comparisons, cont'd