## Section 1 - Descriptions and Family Characteristics

## FACT - Logic

ON Semiconductor FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fan-out capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The sub two-micron silicon gate CMOS process utilized in this family has been proven in the field. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

For direct replacement of LS, ALS and other TTL devices, the 'ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 74ACTXXX devices.

## Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs

Common Output Structure for Standard and Buffer Drivers
Output Sink/Source Current of 24 mA
Transmission Line Driving 50 ohm (Commercial) Guaranteed

- Operation from 2-6 Volts Guaranteed
- Temperature Range $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ (Commercial)
- Improved ESD Protection Network
- High Current Latch-Up Immunity


## Interfacing

FACT devices have a wide operating voltage range ( $\mathrm{V}_{\mathrm{CC}}$ $=2$ to 6 Vdc ) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:
'AC - This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive $\pm 24 \mathrm{~mA}$ of $\mathrm{IOH}_{\mathrm{OH}}$ and IOL current. Industry standard 'AC nomenclature and pinouts are used.
'ACT - This is a high-speed CMOS device with a TTL-toCMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a
$\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}$ with $\mathrm{V}_{\mathrm{OH}}=2.4 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{OL}}=0.4 \mathrm{~V}$. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT devices have the same output structures as ' AC devices.

## Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.


Figure 1-1. ICC versus VCC
Figure 1-1 illustrates the effects of $\mathrm{I}_{\mathrm{CC}}$ versus power supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

## AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high- speed systems.

The example below describes typical values for a 74XX138, 3-to-8 line decoder.

| FACT | $=6.0 \mathrm{~ns} @ \mathrm{CL}_{\mathrm{L}}=50 \mathrm{pF}$ |
| ---: | :--- |
| ALS | $=12.0 \mathrm{~ns} @ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |
| LS | $=22.0 \mathrm{~ns} @ \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| HC | $=17.5 \mathrm{~ns} @ \mathrm{CL}_{\mathrm{L}}=50 \mathrm{pF}$ |

AC performance specifications are guaranteed at $5 \mathrm{~V} \pm$ 0.5 V and $3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$. For worst case design at $2 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ on all device types, the formula below can be used to determine AC performance.

AC performance at $2 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}=1.9 \times \mathrm{AC}$ specification at 3.3 V .

## Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps . This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and $5 \mathrm{~V} \pm$ $10 \% \mathrm{~V}_{\mathrm{CC}}$.

## Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.
The comparisons shown describe the difference between the input threshold of a device and the output voltage, $\left|\mathrm{V}_{\mathrm{IL}}-\mathrm{V}_{\mathrm{OL}}\right| /\left|\mathrm{V}_{\mathrm{IH}}-\mathrm{V}_{\mathrm{OH}}\right|$ at $4.5 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$.

```
FACT = 1.25/1.25 V
ALS = 0.4/0.7 V
LS = 0.3/0.7 V @ 4.75 V VCC
HC = 0.8/1.25 V
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## Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC and 'ACT device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All devices ('AC or 'ACT) are guaranteed to source and sink 24 mA . Commercial devices, 74AC/ACTXXX, are capable of driving 50 ohm transmission lines.

## IOL/IOH Characteristics

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FACT = 24/-24 mA
ALS = 24/-15 mA
LS = 8/-0.4 mA @ 4.75 V VCC
HC = 4/-4 mA
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## Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied 'typical' output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these 'typical' performance values across the operating voltage and temperature limits. Fortunately for the system designers, ON Semiconductor has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50 ohms for the commercial temperature range.

Figure 1-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ( $\mathrm{I}_{\mathrm{out}}>0$ ), are the $\mathrm{V}_{\mathrm{OH}}$ and $\mathrm{I}_{\mathrm{IH}}$ curves for FACT logic while on the left side ( $\mathrm{I}_{\mathrm{Out}}<0$ ), are the curves for VOL and IIL. Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.


Figure 1-2. Gate Driving 50 Ohm Line Reflection Diagram

Begin analysis at the $\mathrm{V}_{\text {OL }}$ (quiescent) point. This is the intersection of the $\mathrm{V}_{\mathrm{OL}} / \mathrm{IOL}$ curve for the output and the $\mathrm{V}_{\mathrm{IN}} / \mathrm{I}_{\text {IN }}$ curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV . Then draw a 50 ohm load line from this intersection to the $\mathrm{VOH}_{\mathrm{OH}} / \mathrm{IOH}$ curve as shown by Line 1 . This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95 V . Then draw a line with a slope of -50 ohms from this first intersection point to the $\mathrm{V}_{\mathrm{IN}} / \mathrm{I}_{\mathrm{IN}}$ curve as shown by Line
2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the $\mathrm{V}_{\mathrm{OH}} / \mathrm{I}_{\mathrm{OH}}$ curve should have positive slopes while lines terminating on the $\mathrm{V}_{\mathrm{IN}} / \mathrm{I}_{\mathrm{IN}}$ curve should have negative slopes.


Figure 1-3a. Resultant Waveforms Driving 50 Ohm Line - Theoretical


Figure 1-3b. Resultant Waveforms Driving 50 Ohm Line - Actual


Figure 1-3c. Resultant Waveforms Driving 50 Ohm Line - Theoretical

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the $\mathrm{VOH} / \mathrm{IOH}$ curve will be waves travelling from the driver to the receiver while intersection points on the $\mathrm{V}_{\mathrm{IN}} / \mathrm{I}_{\text {IN }}$ curve will be waves travelling from the receiver to the driver.
Figures $1-3 \mathrm{a}, 1-3 \mathrm{~b}, 1-3 \mathrm{c}$ and $1-3 \mathrm{~d}$ show the resultant wave- forms. Each division on the time scale represents the propagation delay of the transmission line.
While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either $70 \%$ or $30 \%$ of $\mathrm{VCC}^{2}$. The formula for calculating the current and voltage required is $\left|\left(\mathrm{V}_{\mathrm{OQ}}-\mathrm{V}_{\mathrm{I}}\right) / \mathrm{Z}_{\mathrm{O}}\right|$ at $\mathrm{V}_{\mathrm{I}}$. For $\mathrm{V}_{\mathrm{OQ}}=100 \mathrm{mV}, \mathrm{V}_{\mathrm{IH}}=3.85 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ and $\mathrm{Z}_{\mathrm{O}}=50 \mathrm{ohms}$, the required IOH at 3.85 V is 75 mA . For the HIGH-to-LOW transition, $\mathrm{V}_{\mathrm{OQ}}=5.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=1.35 \mathrm{~V}$ and $\mathrm{Z}_{\mathrm{O}}=50 \mathrm{ohms}, \mathrm{IOL}$ is 75 mA at 1.65 V . FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50 ohms, the current requirements are less and switching is still guaranteed.
It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid $\mathrm{V}_{\text {IN }}$ level.


Figure 1-3d. Resultant Waveforms Driving 50 Ohm Line - Actual
The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.


Figure 1-4. Output Characteristics $\mathrm{V}_{\mathrm{OH}} / \mathrm{IOH}$, MC74AC00


Figure 1-5. Output Characteristics $\mathrm{VOL}_{\mathrm{OL}} \mathrm{IOL}$, MC74AC00


Figure 1-6. Input Characteristics $\mathrm{V}_{\mathrm{IN}} / \mathrm{I}_{\mathrm{IN}}$

## Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3 V $\pm 0.3 \mathrm{~V}$. To this end, ON Semiconductor guarantees all of its devices operational at $3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$. Note also that AC and DC specifications are guaranteed between 3 and 5.5 V . Operation of FACT logic is also guaranteed from 2 to 6 V on $\mathrm{V}_{\mathrm{CC}}$.

## Operating Voltage Ranges

$$
\begin{aligned}
& \mathrm{FACT}=2 \text { to } 6 \mathrm{~V} \\
& \mathrm{ALS}=5 \mathrm{~V} \pm 10 \% \\
& \mathrm{LS}=5 \mathrm{~V} \pm 5 \% \\
& \mathrm{HC}=2 \text { to } 6 \mathrm{~V}
\end{aligned}
$$



Figure 1-7. Internal Gate Delays

GENERAL CHARACTERISTICS (All Max Ratings)

| Symbol | Parameter | LS | ALS | HCMOS | FACT |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | 'AC | 'ACT |  |
| VCC/EE/DD | Operating Voltage Range | $5 \pm 5 \%$ | $5 \pm 10 \%$ | 2 to 6 | 2 to 6 | 2 to 6 | V |
| TA 74 Series | Operating Temperature Range | 0 to +70 | 0 to +70 | -40 to +85 | -40 to +85 | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{IH}}($ min $)$ | Input Voltage (limits) | 2 | 2 | 3.15 | 3.15 | 2 | V |
| $\mathrm{V}_{\text {IL }}$ (max) |  | 0.8 | 0.8 | 0.9 | 1.35 | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}(\mathrm{min})$ | Output Voltage (limits) | 2.7 | 2.7 | $\mathrm{V}_{\mathrm{CC}}-0.1$ | $\mathrm{V}_{\mathrm{CC}}-0.1$ | $\mathrm{V}_{\mathrm{CC}}{ }^{-0.1}$ | V |
| $\mathrm{V}_{\mathrm{OL}}$ (max) |  | 0.5 | 0.5 | 0.1 | 0.1 | 0.1 | V |
| $\mathrm{IIH}^{\text {H }}$ | Input Current | 20 | 20 | +1 | +1 | +1 | $\mu \mathrm{A}$ |
| IIL |  | -400 | -200 | -1 | -1 | -1 | $\mu \mathrm{A}$ |
| ${ }^{\mathrm{I}} \mathrm{OH}$ | Output Current at $\mathrm{V}_{0}$ (limit) | -0.4 | -0.4 | -4@ $\mathrm{V}_{\mathrm{CC}}-0.8$ | -24@ $\mathrm{V}_{\mathrm{CC}}-0.8$ | -24 @ $\mathrm{V}_{\mathrm{CC}}-0.8$ | mA |
| IOL |  | 8 | 8 | 4 @ 0.4 V | 24 @ 0.4 V | 24 @ 0.4 V | mA |
| DCM | DC Noise Margin LOW/HIGH | 0.3/0.7 | 0.4/0.7 | 0.8/1.25 | 1.25/1.25 | 0.7/2.4 | V |

Note: All DC parameters are specified over the commercial temperature range.
Figure 1-8. Logic Family Comparisons

## FACT Replaces LS, ALS, HCMOS

ON Semiconductor's Advanced CMOS family is specifically designed to outperform the LS, ALS and HCMOS families. Figure 1-7 shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming $1 \mu \mathrm{~W}$ of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

SPEED/POWER CHARACTERISTICS (All Typical Ratings)

| Symbol | Parameter | LS | ALS | HCMOS | FACT | Unit |
| :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{G}}$ | Quiescent Supply Current/Gate | 0.4 | 0.2 | 0.0005 | 0.0005 | mA |
| $\mathrm{P}_{\mathrm{G}}$ | Power/Gate (Quiescent) | 2 | 1.2 | 0.0025 | 0.0025 | mW |
| $\mathrm{tP}_{\mathrm{P}}$ | Propagation Delay | 7 | 5 | 8 | 5 | ns |
| - | Speed Power Product | 14 | 6 | 0.02 | 0.01 | pJ |
| $\mathrm{f}_{\max }$ | Clock Frequency D/FF | 33 | 50 | 50 | 160 | MHz |

PROPAGATION DELAY (Commercial Temperature Range)

|  | Product |  | LS | ALS | HCMOS | FACT | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPLH/tPHL | 74XX00 | Typ | 10 | 5 | 8 | 5 | ns |
|  |  | Max | 15 | 11 | 23 | 8.5 | ns |
| tPLH/tPHL (Clock to Q) | 74XX74 | Typ | 25 | 12 | 23 | 8 | ns |
|  |  | Max | 40 | 18 | 44 | 10.5 | ns |
| tPLH/tPHL (Clock to Q) | 74XX163 | Typ | 18 | 10 | 20 | 5 | ns |
|  |  | Max | 27 | 17 | 52 | 10 | ns |

Conditions: (LS) $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{CL}_{\mathrm{L}}=15 \mathrm{pF}, 25^{\circ} \mathrm{C}$;
(ALS/HC/FACT) $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \pm 10 \%, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Typ values at $25^{\circ} \mathrm{C}$, Max values at 0 to $70^{\circ} \mathrm{C}$ for $\mathrm{ALS},-40$ to $+85^{\circ} \mathrm{C}$ for $\mathrm{HC} / \mathrm{FACT}$.
Figure 1-8. Logic Family Comparisons, cont'd

