CPC945 Bridge and Memory Controller Datasheet

Version A15-6009-01

Preliminary

August 15, 2006

Printed in the United States of America August 2006.

Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Note: The IBM CPC945 Bridge and Memory Controller may not be used in personal computer products.

IBM Systems and Technology Group
2070 Route 52, Bldg. 330
Hopewell Junction, NY 12533-6351

The IBM home page can be found at **ibm.com**

The IBM semiconductor solutions home page can be found at **ibm.com/**chips

A15-6009-01 Preliminary
August 15, 2006

Contents

List of Figures

List of Tables

About This Datasheet

This datasheet describes the CPC945 Bridge and Memory Controller, also called the CPC945. It provides a general overview of the device, electrical and physical package information, signal descriptions, timing, and power considerations. The device is the front-side bus controller companion chip to the PowerPC® 970MP RISC microprocessor (PowerPC 970MP). The CPC945 also supports the PowerPC 970FX microprocessor.

Who Should Read This Datasheet

System designers and system architects of PowerPC 970MP or PowerPC 970FX applications should use this document to effectively incorporate the CPC945 into a design. Readers should be familiar with the PowerPC Architecture™ and the general constraints and requirements of developing personal computers.

Related Publications

PowerPC Microprocessor Documentation

The latest version of this manual, errata, and other IBM documents referred to in this manual, including the *CPC945 Bridge and Memory Controller Initialization Considerations Application Note,* can be found at ibm.com/chips/techlib. Other information about the PowerPC 970MP or PowerPC 970FX can be obtained from this website or from an IBM representative.

Architecture and Specifications

- *Double Data Rate 2 (DDR2) SDRAM Specification*, JESD79-2a
  www.jedec.org
- *HyperTransport I/O Link Specification*, revision 1.04
  www.hypertransport.org
- *I^2C-Bus Specification*, version 2.1
  www.semiconductors.philips.com
- May, Cathy, et. al., eds. *The PowerPC Architecture: A Specification for a New Family of RISC Processors*, Second Edition. San Francisco: Morgan-Kaufmann, 1994.
- *PCI Express Base Specification*, version 1.0a
  www.pcisig.com

Conventions Used in This Datasheet

- Hexadecimal values are preceded by a lowercase *x*. For example: x‘0B00’.
- Binary values in text are either spelled out (zero and one) or appear in single quotation marks. For example: ‘10101’.
- Differential pairs of signals are designated by _P for the positive signal and _N for the negative signal. For example: DDR_CK_A_P and DDR_CK_A_N.
- Active-low (non-differential) signals are designated by overbars. For example: $\overline{\text{AGP\_TRDY}}$.

1. General Information

1.1 Features

- Dual PowerPC 970MP processor interface buses with cache coherency and snooping protocols supporting up to four processor cores.
- PCI-Express x1, x4, x8, or x16 interface
- 128/144-bit, 533 Mega Transfers per second (MTps) double data rate 2 (DDR2) synchronous DRAM (SDRAM) controller and interface with ECC
- 800 MHz (1600 MTps DDR) HyperTransport host bridge with 16-bit wide data interface and flash ROM support
- One slave and two master I^2C interfaces
- Interrupt controller
- Point-to-point internal architecture provides high-speed non-blocking performance
- 40-bit physical memory address space
- 1182-pin flip-chip plastic ball grid array (FC-PBGA) single chip implementation
- Processor interface interconnection speed of up to 625 MHz (1250 Mbps double data rate)
- Support for eight outstanding transactions per master
- Support for read pipelining and write combining from the processor interface or PCI bus
- Support for read-around-write on the processor interface with PCI ordering
- Support for eight 64/72-bit double-sided dual inline memory modules (DIMMs) arranged in pairs
- PCI and HyperTransport transactions snooped on the processor interface
- Power management support for the CPC945 North Bridge through clock control
- DMA address relocation table (DART) provides flexible I/O memory space relocation and consolidation

1.2 Description

The CPC945 is a frontside bus controller that is compatible with the PowerPC 970MP and PowerPC 970FX RISC microprocessors.

The CPC945 provides a 5-way interconnection among:

- Two PowerPC 970 family processor interfaces
- A DDR2 SDRAM memory subsystem
- PCI-Express bus
- A HyperTransport host bridge

The boot ROM is connected to an I/O device attached to the system via the HyperTransport bus. The CPC945 includes two master-only I^2C interfaces for configuring the memory subsystem. An I^2C slave interface connects the CPC945 North Bridge to a single-chip microcontroller for power management and processor interface configuration. A multiprocessor-capable interrupt controller collects and distributes system interrupts from the PCI-Express and HyperTransport blocks.

To software, the CPC945 appears as:

- A processor interface to the PCI-Express root complex
- A processor interface to the HyperTransport host bridge
- A memory controller
- An interrupt controller
- A set of control registers

1.3 Revision Register

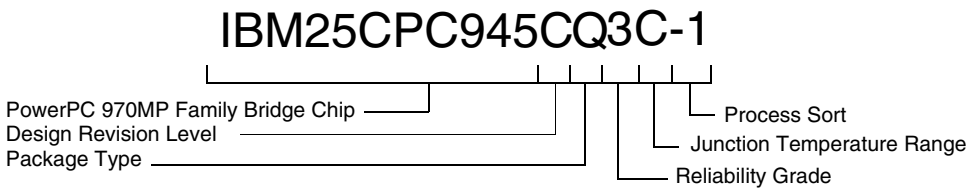
The CPC945 has the following Revision Register values for the respective design revision levels.

Table 1-1. CPC945 Revision Register

Design Revision Level	Revision Register Value
DD1.0	x'0000 0040'
DD1.1	x'0000 0041'
DD1.2	x'0000 0042'

1.4 Part Number Information

Figure 1-1. Part Number Legend



Design Revision Level	B = DD1.1, C = DD1.2
Package Type	Q = Lead free, Flip Chip Plastic Ball Grid Array (FC-PBGA) with 2mm lid.
Reliability Grade	3 = Grade 3
Junction Temperature Range	C = 0–90°C
Process Sort	1 = Standard OEM sort (see *Table 1-2* for details) 2 = Premium OEM sort (available for sample orders only)

Table 1-2. CPC945 Standard OEM Sort Speed Bins

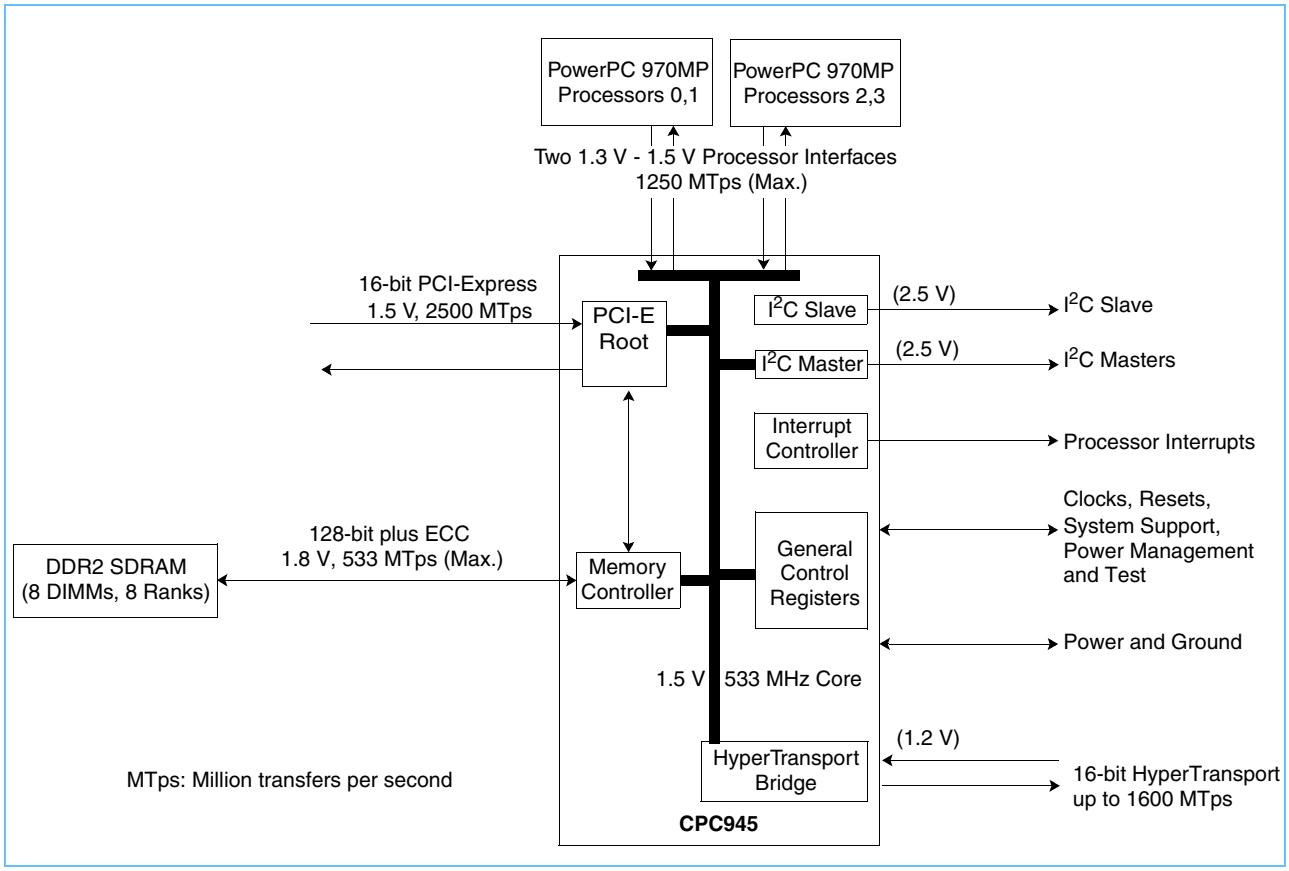
OEM Part Number	IBM Part Number	Speed Classification	PSRO Values[1] (ns)
IBM25CPC945CQ3C-2	41E4198	Fast #3	168-190
IBM25CPC945CQ3C-2	41E4242	Fast #2	191-200
IBM25CPC945CQ3C-2	41E4244	Fast #1	201-210
IBM25CPC945CQ3C-1	41E4246	Nominal Fast	211-220
IBM25CPC945CQ3C-1	41E4248	Nominal	221-230
IBM25CPC945CQ3C-1	41E4250	Nominal Slow	231-240

Note:
1. PSRO - Performance Sort Ring Oscillator. A manufacturing process parameter used to indicate where the part falls in the process distribution range.

2. Overview

2.1 Functional Blocks

Figure 2-1. CPC945 Bridge and Memory Controller Block Diagram



2.1.1 Processor Interfaces

The CPC945 has interfaces for connecting to two dual core PowerPC 970 RISC microprocessors. Each interface consists of two separate point-to-point processor buses, each providing separate inbound and outbound buses. Each interface has the following features:

- 35-bit (logical)/44-bit (physical) multiplexed address/data (AD)
- 1-bit transfer handshake
- 2-bit snoop response bus
- Supports split transactions for reads and writes using a tagged packet-passing protocol
- Transaction reflecting and global snooping ensure memory-to-cache coherency
- Processor bus runs asynchronously from the CPC945 core
- Debug facility generates logic analyzer triggers and stores transaction samples

2.1.2 PCI Express Interface

The CPC945 PCI-Express (PCI-E) interface enables interfacing to other PCI-E devices. The PCI-based interface has the following features:

- PCI-Express root complex
- Configurable single port with selectable lane width of x1, x4, x8, or x16 bit lanes at 2.5 GHz
- Includes the arbiter for the point to point interface
- Includes PCI configuration space

2.1.3 I^2C Interfaces

The CPC945 has three I^2C interfaces for use in configuring the memory subsystem and other CPC945 components.

- Two software-selectable master-only I^2C interfaces for use in configuring the memory subsystem
- One slave I^2C interface for processor interface configuration, power management, debugging, and diagnostic purposes

2.1.4 Interrupt Controller

The interrupt controller collects and distributes system interrupts from the PCI-Express and HyperTransport blocks. The controller has the following features:

- Collects up to 128 interrupt sources (120 available) from the HyperTransport bridge, and delivers them to up to four processors.
- Interrupt controller registers are directly mapped inside the CPC945 register space.
- Interrupt sources internal to the CPC945 are delivered directly to the interrupt controller.

2.1.5 Memory Controller

The memory controller supports the CP945's double data rate 2 (DDR2) SDRAM memory subsystem. It has the following features:

- Supports up to eight 64/72-bit wide double-sided DDR2 registered or unregistered DIMMs arranged in a 128/144-bit wide data bus providing 64 bytes in four data beats, or 128-byte access in two sets of four data beats. **Note:** Achieving maximum memory transfer rate (533 MTps) and driving eight ranks of memory simultaneously is not possible without incorporating use of external components such as data muxes and buffers to redrive the address and data signals.
- Random single error correct and double error detect ECC with x4 chip kill error correction for the main memory array.
- Runs asynchronously from the processor interface at up to 533 MHz.
- Wide data bus provides efficient 128-byte cache line fills.

2.1.6 HyperTransport Bridge

The HyperTransport bridge carries external interrupt information between a HyperTransport South Bridge device and the CPC945. It has the following features:

- 16-bit wide bus; 64-byte memory accesses.
- Bridges to HyperTransport-capable South Bridges and I/O devices.
- Boot ROM is mapped through the HyperTransport bus.
- Carries external interrupt information between a HyperTransport South Bridge and the CPC945.

2.2 General Parameters

Table 2-1 provides a summary of the general parameters of the CPC945.

Table 2-1. General Parameters of the CPC945 Bridge and Memory Controller

Parameter	Description
Die size	95.7 sq. mm
Die dimensions	10.2048 mm × 9.3776 mm
Transistor count	80 million (estimated)
Logic design	Static
Package	1182-pin flip-chip plastic ball grid array (FC-PBGA), 37.5 mm × 37.5 mm (1.0-mm pitch)
Core power supply	1.5 V ±0.05 V
Total power dissipation	22 W (at nominal supply voltages and 533 MHz core frequency)
Maximum heatsink attachment force	4 Kg
Maximum static printed circuit board (PCB) assembly placement force	500 Grams
Maximum spring-loaded heatsink static force	57 Grams

3. Electrical and Thermal Characteristics

3.1 Absolute Maximum Ratings

Note: The absolute maximum ratings shown in *Table 3-1* are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
1.5 V Core logic, PCI-Express supply	V_{DD}	0	2.25	V	1,2
1.8 V DDR I/O supply	V_{DD3}	0	2.8	V	1,2
1.3 V to 1.5 V Processor interface supply	V_{DD2}	0	2.25	V	1,2
1.2 V HyperTransport data interface supply	V_{DD4}	0	1.8	V	1,2
2.5 V I^2C master interface, slave interface, and misc. signals supply	V_{DD5}	0	3.5	V	1,2
1.2 V I/O pin voltage	$V_{IN1.2}$	– 0.60	1.5	V	1,2
1.5 V I/O pin voltage	$V_{IN1.5}$	– 0.60	1.90	V	1,2
1.8 V I/O pin voltage	$V_{IN1.8}$	– 0.60	2.8	V	1,2
2.5 V I/O pin voltage	$V_{IN2.5}$	– 0.60	3.5	V	1,2
Storage temperature	T_{STG}	– 65	150	°C	

Note:

1. Pin voltage limits are stated at nominal I/O supply voltages of 2.5 V, 1.8V, and 1.5 V.
2. The core voltage should be brought up first, followed by the I/O voltages. Note that correct I^2C slave interface operation depends on stable core, processor I/O, and DDR I/O voltages. No voltage should be applied to an I/O pad if the associated power supply is not on.

3.2 Package Thermal Specifications

Table 3-2. Package Thermal Information

Parameter	Package	Symbol	Value
Junction-to-case thermal resistance	FC-PBGA	θ_{JC}	0.383/W

3.3 Capacitance

Table 3-3. Input Capacitance

Parameter	Symbol	Maximum	Units
Input capacitance (1.2 V group)	C_{IN12}	5	pF
Input capacitance (1.3 V - 1.5 V group)	$C_{IN13-15}$	6	pF
Input capacitance (1.5 V group)	C_{IN15}	7	pF
Input capacitance (1.8 V group)	C_{IN18}	7	pF
Input capacitance (2.5 V group)	C_{IN25}	6	pF

Note: These values are not 100% tested or guaranteed. They are provided as guidelines; however, designers are encouraged to model the high speed interfaces to verify that their applications will work at their desired performance level. Models and package impedance information is available for download from the IBM technical library.

3.4 Recommended DC Operating Conditions

Device operation beyond the conditions specified in *Table 3-4* is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Table 3-4. Recommended Functional DC Operating Ratings (Page 1 of 2)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
1.5 V core logic supply voltage	V_{DD}	1.45	1.50	1.55	V	
1.8 V DDR interface supply voltage	V_{DD3}	1.7	1.8	1.9	V	
1.3 V - 1.5 V processor interface supply voltage	V_{DD2}	1.25	1.45	1.6	V	4
2.5 V I^2C, miscellaneous I/O supply voltage	V_{DD5}	2.3	2.5	2.7	V	
1.2 V HyperTransport data interface supply voltage	V_{DD4}	1.14	1.2	1.26	V	

Notes:

1. The PLL analog power supply and ground pins must be filtered with a inductive-capacitive (LC) filter. See *Figure 3-1, Analog VDD Filtering for the Hyper-Transport and PCI-Express Phase-Locked Loops,* on page 20 for details.
2. At 533 MHz core frequency, 533 MTps DDR2, 1250 MTps processor interface, nominal supply voltages, and 70°C junction temperature. Configurations with lower speeds and narrower interfaces (333 MTps 64-bit DDR2, 600 MTps PI, 400 MTps 8-bit HT) will consume less power. Contact IBM applications engineering for more details.
3. The four PLLs consume current from both the V_{DD} and V_{PLL} AVDD, AVDD2, AVDDA, AVDDB supplies. These currents are small relative to the total core current.
4. Processor interface supply voltage VDD2 can vary from 1.3 V to 1.5 V, depending on system or card design requirements and processor I/O voltage specifications. Designers should either perform necessary simulations or provide a variable voltage and determine, experimentally, which voltage best meets their requirements. This voltage must be the same for both processor (OVDD) and bridge (VDD2).

Table 3-4. Recommended Functional DC Operating Ratings (Page 2 of 2)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
HT and PCI-E PLL supply voltage - AVDD2, AVDDA, AVDDB	AVDDx	1.6	1.8-2.5	2.8	V	
DDR and PI PLL supply voltage - AVDD	AVDD	1.4	1.5	1.6	V	1
V_{DD} active current	I_{DD}	—	10.0	—	A	2
V_{DD2} active current	I_{DD2}	—	1.0	—	A	2
V_{DD3} active current	I_{DD3}	—	2.8	—	A	2
V_{DD4} active current	I_{DD4}	—	0.17	—	A	2
V_{DD5} active current	I_{DD5}	—	0.08	—	A	2
V_{PLL} active current - AVDD	I_{PLL}	—	0.1	—	A	2, 3
V_{DD} active power	P_{DD}	—	15.0	—	W	2
V_{DD2} active power	P_{DD2}	—	1.4	—	W	2
V_{DD3} active power	P_{DD3}	—	5.0	—	W	2
V_{DD4} active power	P_{DD4}	—	0.2	—	W	2
V_{DD5} active power	P_{DD5}	—	0.2	—	W	2
AVDD2, AVDDA, AVDDB active power	P_{AVDDx}	—	0.10	—	W	
V_{PLL} active power	P_{PLL}	—	0.10	—	W	2, 3
Total device power	P_T	—	22.0	—	W	2
2.5 V input logic high	V_{IH2}	1.7		2.7	V	
2.5 V input logic low	V_{ILH2}	0		0.7	V	
V_{DD2} Input logic high	V_{IH1}	$0.65 \times V_{DD2}$		1.6	V	4
V_{DD2} Input logic low	V_{IL1}	0		$0.35 \times V_{DD2}$	V	4
2.5 V output high	V_{OH2}	2		2.7	V	
2.5 V output low	V_{OL2}	0		0.4	V	
V_{DD2} Output logic high	V_{OH1}	$0.75 \times V_{DD2}$		1.6	V	4
V_{DD2} Output logic low	V_{OL1}	0		$0.25 \times V_{DD2}$	V	4
Input leakage current	I_L	0	<1	10	µA	
Ambient temperature (startup condition)	T_A	0	—	+70	°C	
Die junction temperature	T_J	0	—	+90	°C	

Notes:

1. The PLL analog power supply and ground pins must be filtered with a inductive-capacitive (LC) filter. See *Figure 3-1, Analog VDD Filtering for the Hyper-Transport and PCI-Express Phase-Locked Loops,* on page 20 for details.
2. At 533 MHz core frequency, 533 MTps DDR2, 1250 MTps processor interface, nominal supply voltages, and 70°C junction temperature. Configurations with lower speeds and narrower interfaces (333 MTps 64-bit DDR2, 600 MTps PI, 400 MTps 8-bit HT) will consume less power. Contact IBM applications engineering for more details.
3. The four PLLs consume current from both the V_{DD} and V_{PLL} AVDD, AVDD2, AVDDA, AVDDB supplies. These currents are small relative to the total core current.
4. Processor interface supply voltage VDD2 can vary from 1.3 V to 1.5 V, depending on system or card design requirements and processor I/O voltage specifications. Designers should either perform necessary simulations or provide a variable voltage and determine, experimentally, which voltage best meets their requirements. This voltage must be the same for both processor (OVDD) and bridge (VDD2).

Figure 3-1. Analog V_{DD} Filtering for the Hyper-Transport and PCI-Express Phase-Locked Loops

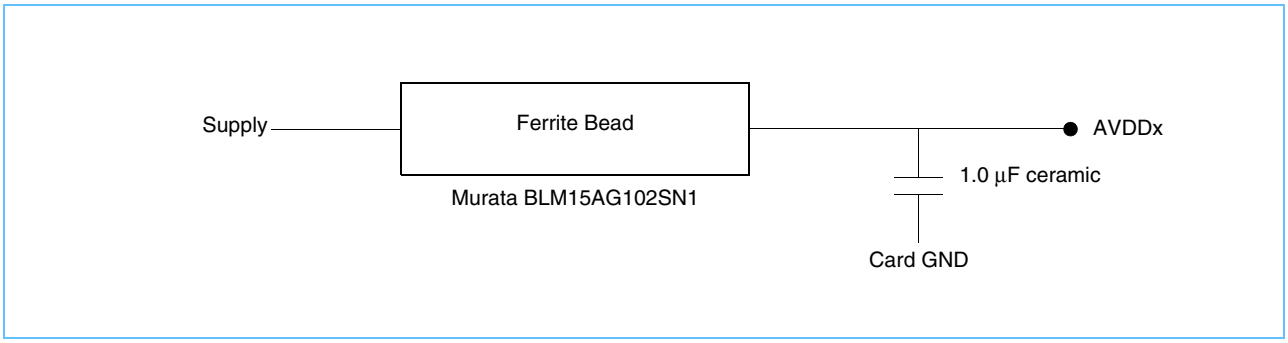
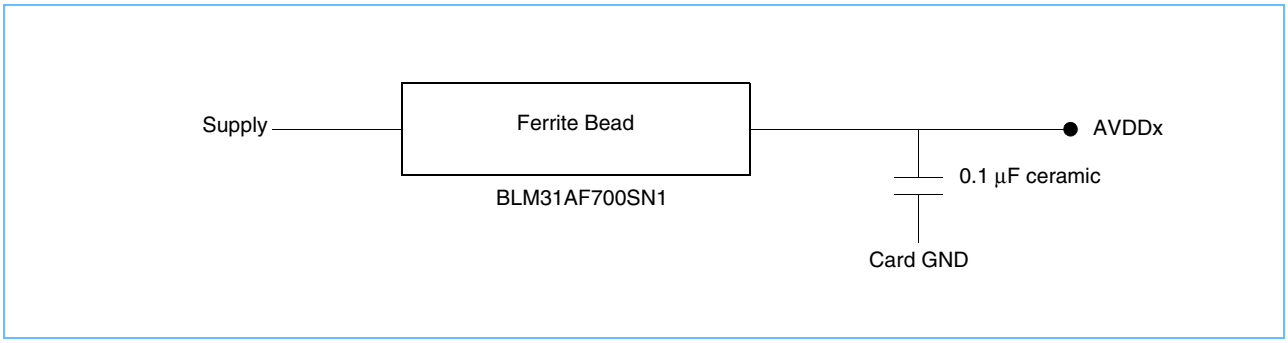


Figure 3-2. Analog V_{DD} Filtering for the PI and DDR2 Interface Phase-Locked Loops



3.4.1 Guidelines for PLL Filtering for HyperTransport and PCI-Express PLLs (AVDD2, AVDDA, AVDDB)

In general, to control jitter at the card level it is important to ensure that the incoming Reference Clock signal has minimal jitter.

- Good design practices with card design and layout should be followed, especially if the Reference Clock is derived from an external crystal.
- On card VDD and GND noise should be minimized through the appropriate use of decoupling capacitors. Use of a voltage regulator as the source of the analog VDD can also help reduce noise.
- Care should be taken to ensure that the AVDD2 and AVDD pins for the PCI-Express and those for the HyperTransport cores are separately connected to the power plane on the card through individual filter networks. Connecting multiple AVDD2 or AVDD pins together and feeding them through a common filter network is not recommended. Modulation between the interface cores may result if a design incorporates such a common filter network.
- Each AVDD2 or AVDD pin should have a filter network (an example of one possible implementation is shown in *Figure 3-1*). All wire lengths should be kept as short as possible to minimize inductive coupling from other noise sources. The recommended capacitor should be of type X5R ceramic construction, of size 0603, and have a 6.3 V rating and should be located adjacent to the device package. The impedance of the ferrite bead should be much greater than that of the capacitor for the noise frequencies. Circuit simulation and experimentation is necessary to determine the optimal filter design.

3.4.2 Guidelines for PLL Filtering for Processor Interface and DDR2 (AVDD)

- In general, to control jitter at the card level it is important to ensure that the incoming Reference Clock signal has minimal jitter. Good design practices with card design and layout should be followed, especially if the Reference Clock is derived from an external crystal.
- On card VDD and GND noise should be minimized through the appropriate use of decoupling capacitors. Use of a voltage regulator as the source of the analog VDD can also help reduce noise.
- Each AVDD pin should have a filter network (an example of one possible implementation is shown in *Figure 3-2*). All wire lengths should be kept as short as possible to minimize inductive coupling from other noise sources. The recommended capacitor should be of type X5R ceramic construction, of size 0603, and have a 6.3 V rating and should be located adjacent to the device package. The impedance of the ferrite bead should be much greater than that of the capacitor for the noise frequencies. Using a resistor in place of a ferrite bead may be preferable in some applications. Designers should note that these filter configurations are only recommendations and should only be used as a starting point. Circuit simulation and experimentation is necessary to determine the optimal filter design.
- The AVDD-AGND compression/expansion due to noise should be less than ±50 mV.

3.5 Clocks

Table 3-5. Reference Clock Input Frequencies

Interface	Signal Name	Frequency	Input Type
Processor Interface	PI_REFCLK	Refer to CPC945 UM, Tables 12-11 and 12-12	Pseudo HSSTL
DDR	DDR_REFCLK	66.67 MHz	LVDS
HyperTransport	HT_REFCLK	66.67 MHz	CMOS/LVDS
PCI-Express	PCIE_REFCLK	100 MHz	CMOS/LVDS
Power Management	PMR_CLK	300 MHz (no PLL)	PECL

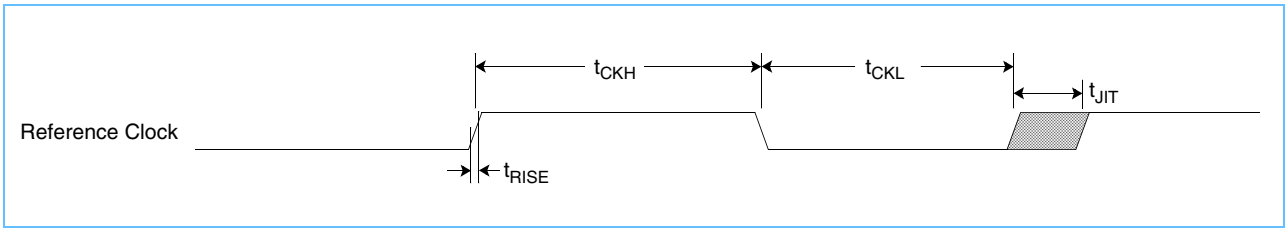
Table 3-6. PI_REFCLK Reference Clock Specifications

Parameter	Symbol	Value		Unit	Notes
		Minimum	Maximum		
Clock Rise and Fall Time	t_{RISE} t_{FALL}		500	ps	
Clock Duty Cycle		45	55	%	
Clock Input Jitter	t_{JIT}		± 100	ps	
PI_REFCLK Input High Voltage	V_{ih}		VDD2 + 0.3	V	
PI_REFCLK Input Low Voltage	V_{il}	- 0.3		V	
PI_REFCLK Input Voltage Range	V_{ih}-V_{il}	0.1		V	

Table 3-7. DDR_REFCLK Reference Clock Specifications

Parameter	Symbol	Value		Unit	Notes
		Minimum	Maximum		
Clock Rise and Fall Time	t_{RISE} t_{FALL}		550	ps	
Clock Duty Cycle		45	55	%	
Clock Input Jitter	t_{JIT}		± 100	ps	
DDR_REFCLK Common Mode Voltage Level	V_{icm}	0	1.8	V	
DDR_REFCLK Input High Voltage	V_{ih}	V_{icm} + 0.05	2.15	V	
DDR_REFCLK Input Low Voltage	V_{il}	- 0.3	V_{icm} + 0.05	V	
DDR_REFCLK Input Voltage Range	V_{ih}-V_{il}	100		mV	

Figure 3-3. PLL Reference Clock Parameters



HT_REFCLK and PCIE-REFCLK PLL inputs can be either LVDS or CMOS. There is no setting required to select between these two types of input. It is determined strictly by the inputs provided by the system design.

Table 3-8. HT_REFCLK and PCIE_REFCLK Reference Clock Input Specifications for LVDS

Parameter	Symbol	Value		Unit	Notes
		Minimum	Maximum		
Clock Rise and Fall Time	t_{RISE} t_{FALL}	0.35	0.55	ns	1
Clock Duty Cycle		45	55	%	
Clock Input Jitter	t_{JIT}		± 100	ps	
SE Peak-to-Peak at PLL Inputs	V_{ih}-V_{il}	250	450	mV	2

Note:
1. LVDS at 20/80%.
2. Single Ended (SE) means that REFCLK_N and REFCLK_P each must see this swing.

Figure 3-4. Typical External Termination for LVDS Input

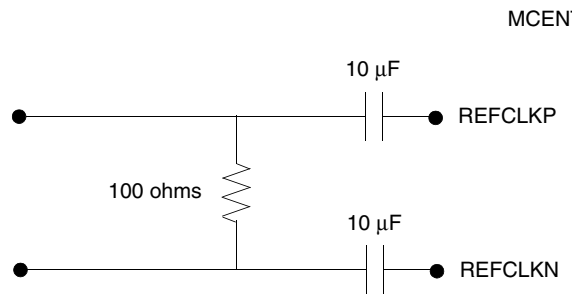
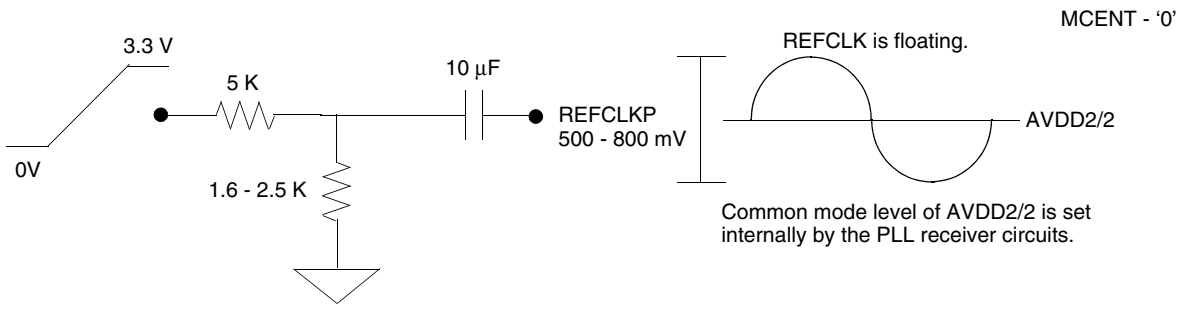


Table 3-9. HT_REFCLK and PCIE_REFCLK Reference Clock Input Specifications for CMOS

Parameter	Symbol	Value		Unit	Notes
		Minimum	Maximum		
Clock Rise and Fall Time	t_{RISE} t_{FALL}		1	ns	
Clock Duty Cycle		45	55	%	
Clock Input Jitter	t_{JIT}		± 100	ps	
Peak-to-Peak at HT_REFCLK Inputs		500	800	mV	
Peak-to-Peak at PCIE_REFCLK Inputs		500	800	mV	

Figure 3-5. Typical External Termination for CMOS Oscillator



3.6 Processor Interface Specifications

The CPC945's dual PowerPC 970 processor interfaces operate at up to 625 MHz in double-data rate mode, providing up to 1250 million transfers per second. The CPC945 uses internal registers, which must be configured at startup to comply with the timing requirements of the IBM PowerPC 970MP Microprocessor. The settings for these registers must be determined by analysis using the card design electrical characteristics, and optimized experimentally. The eye-opening requirement for the CPC945 on the receiving end is the same as for the IBM PowerPC 970MP Microprocessor. The processor link design must be appropriate for the desired bit rate. The operating frequencies for the processor interfaces are generated by PLL1 from the PI_APCLK differential signal pair.

The processor interfaces feature an automatic initialization alignment procedure (IAP) that adjusts the timing skews on all the data lines at the receiving end of the interface. Board wiring flight-time information must be used to ensure that the maximum data skew figures listed in the *IBM PowerPC 970MP RISC Microprocessor Datasheet* are met. Additional requirements for board wiring are contained in that document. Contact your IBM representative for information on obtaining this document.

3.7 PCI-Express Interface Specification

The PCI-Express interface operates at 2.5 GHz and complies with the electrical and timing requirements in the PCI-SIG, "PCI Express Base Specification Revision 1.0a", PCI Express, April 15, 2003.

PCI-SIG, "PCI Express Card Electromechanical Specification Revision 1.0a", PCI Express, April 15, 2003., must be used to correctly design this interface.

3.8 I^2C Interface Specifications

The I^2C slave interface complies with the I^2C-bus specification for standard-mode operation (100 kbps) and fast-mode operation (400 kbps). The I^2C master interfaces support standard-mode and operate at selectable bit rates of 25, 50, and 100 kbps.

Table 3-10. I^2C-Bus Specifications

Parameter	Symbol	Standard Mode		Fast Mode		Units
		Minimum	Maximum	Minimum	Maximum	
SCL clock frequency (slave)	f_{SCL}	0	100	0	400	kHz
SCL clock frequency (master)	f_{SCL}	0	100	N/A	N/A	kHz
Data set-up time	t_{SU}	250	—	100[1]	—	ns
Data hold time	t_{HO}	0[2]	70	0[2]	150	ns
SCL clock high time	t_{CLH}	4.0	—	0.6	—	µs
SCL clock low time	t_{CLL}	4.7	—	1.3	—	µs

3. A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the *low* period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line, t_r max + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C-bus specification), before the SCL line is released.
4. A device must internally provide a data hold time to bridge the undefined period between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

3.9 DDR2 SDRAM Interface Specifications

The double data rate, 128/144-bit-wide SDRAM interface operates in synchronous mode at up to 266 MHz (533 million transfers per second). Registers in the CPC945 are used to meet the timing requirements of the DDR2 DIMM standard. The settings are determined experimentally and must match the timing requirements of the memory DIMMs and the card design. Care must be taken to match the data (DQ) latency between bits within a byte lane. The timing between byte lanes is adjustable by the internal registers.

Note: A thorough and comprehensive tuning process must be followed during board bring-up with several different parts. Tuning should be done with all possible memory configurations planned for the application. For further information on the tuning process, review the application note Memory Signal Delay Tuning. Additionally, parts used for this initial tuning phase should cover the entire manufacturing process window. Contact your IBM sales or marketing representative for information on obtaining samples of parts outside of the production part number PSRO range.

Note: Achieving maximum memory transfer rate of 533 MTps and driving eight ranks of memory simultaneously is not possible without the use of external components to redrive the load.

3.10 HyperTransport Interface Specifications

The HyperTransport interface is a source-synchronous interface that latches data at a clock edge. As the interface can support up to 1600 MTps, careful consideration is necessary to ensure that the clock and signal alignments and flight times are matched in a board design. The CPC945 meets the module requirements and specifications of the *HyperTransport 1.04 Specification*, which should be used to design this interface.

4. Dimensions and Pin Information

4.1 Package Information

The CPC945 device is packaged in a Flip Chip Plastic Ball Grid Array (FC-PBGA) incorporating 1182 populated package pins on a 36 × 36-ball array. This package has Lead Free C4 and BGA attachment and a 2 mm attached heat-spreader lid. Lead Free means IBM's estimate that none of a product's Homogeneous Materials contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls or polybrominated diphenyl ethers in excess of the RoHS directives's maximum concentration values (as those values existed as of March 1, 2006). For further information, refer to the CPC945 Materials Declaration Form.

- *Figure 4-1* on page 28 and *Figure 4-2* on page 29 show the dimensions for the FC-PBGA package.
- *Figure 4-3* on page 30 identifies the pin types used on this device.

Figure 4-1. FC-PBGA Package (Bottom View)

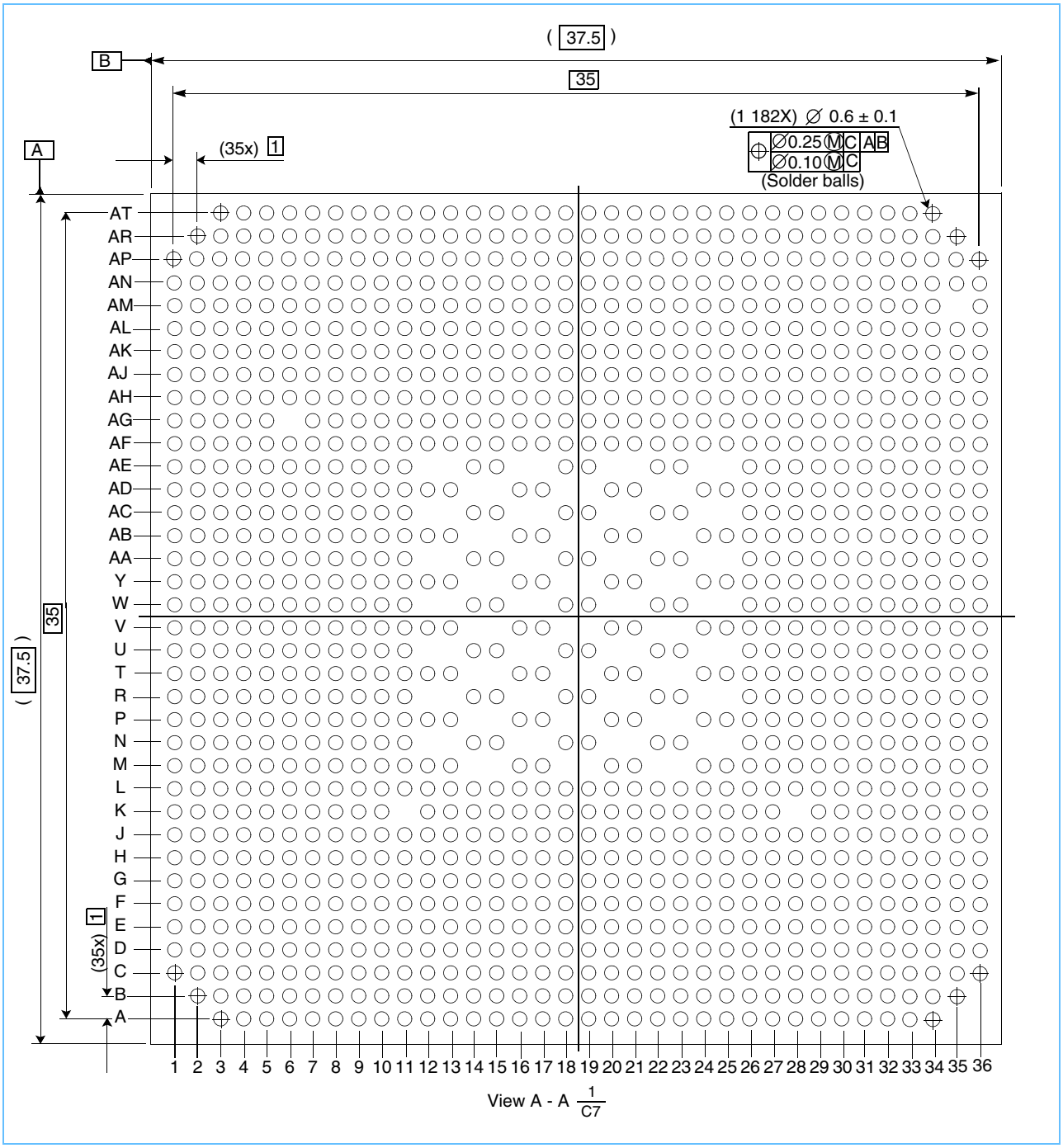
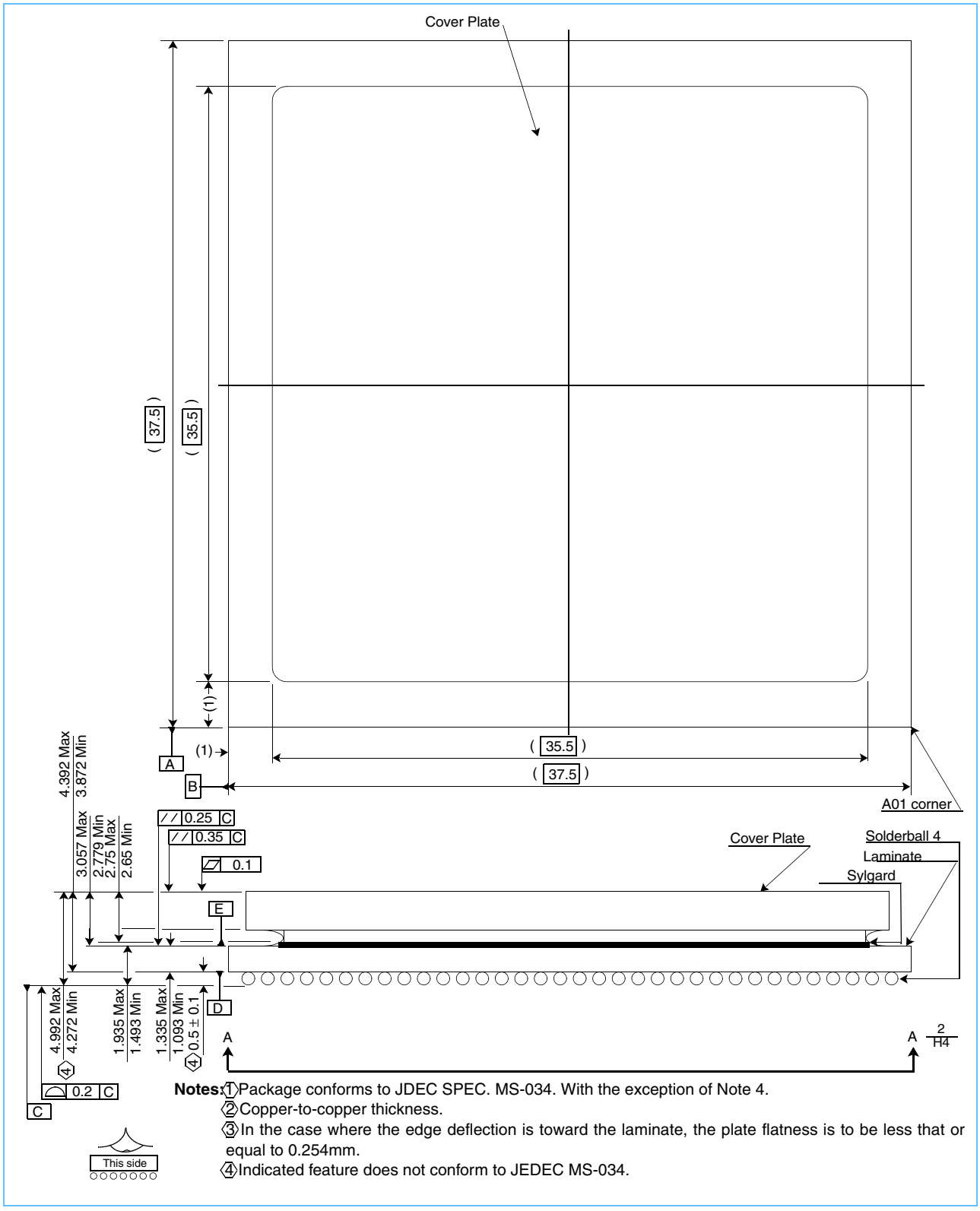
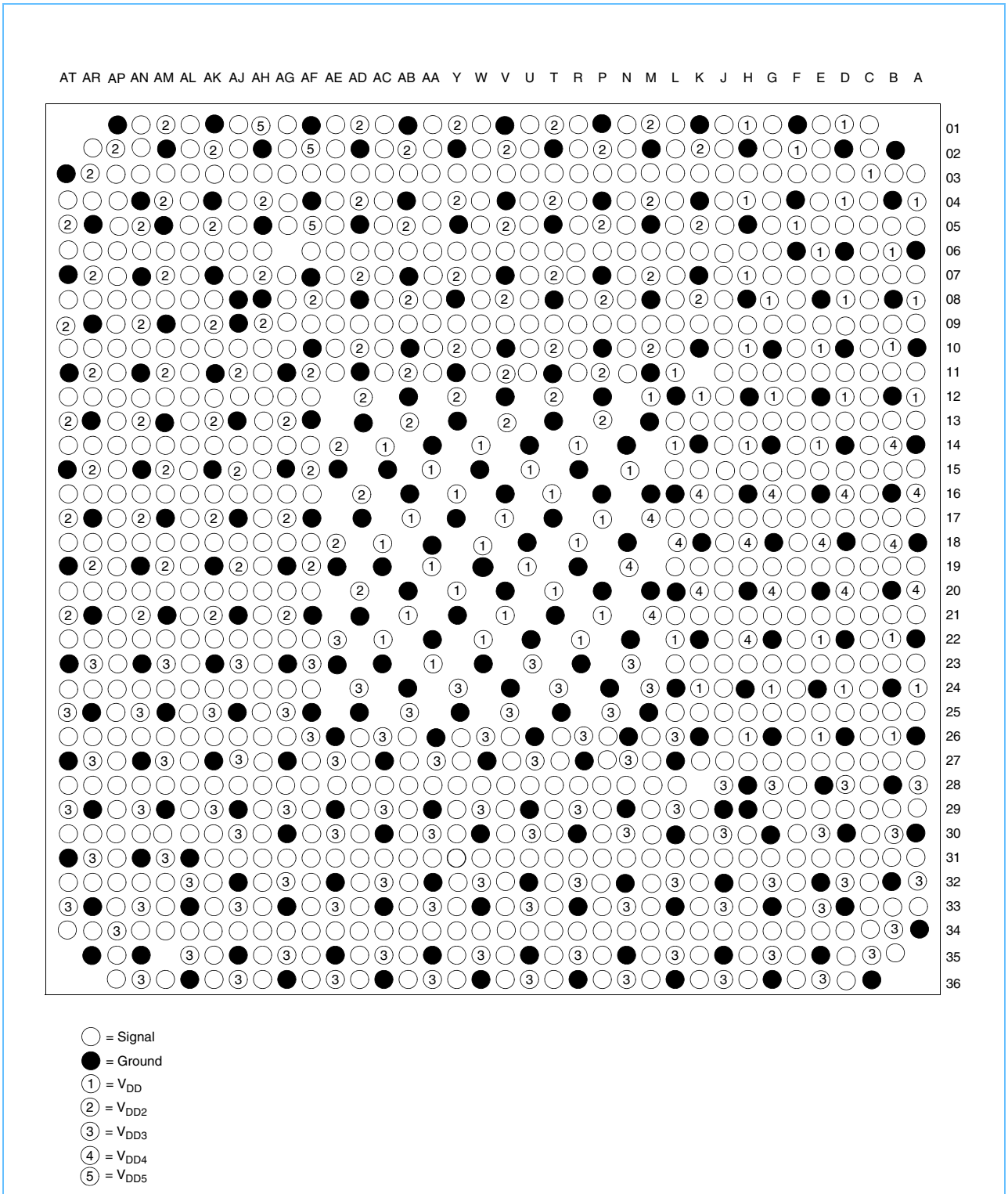


Figure 4-2. FC-PBGA Package (Top and Side Views)



4.2 Pinout

Figure 4-3. CPC945 Bridge and Memory Controller Pinout Drawing (Top View)



4.3 Signal Pins

For information on signal pin locations, see *Table 4-16, CPC945 Bridge and Memory Controller Pin List by Signal Name,* on page 41 and *Table 4-17, CPC945 Bridge and Memory Controller Pin List by Grid Position,* on page 53.

The following table groups the pins by function, lists the number of pins of each type, and points to the location of specific information in this section.

Table 4-1. CPC945 Signal Pin Overview

Pin Type	Total Pins	Reference
PCI Express	73	*Table 4-2, PCIE Signal Pins,* on page 31.
DDR SDRAM	255	*Table 4-3, DDR SDRAM Signal Pins,* on page 32.
HyperTransport	88	*Table 4-4, HyperTransport Signal Pins,* on page 34.
Processor Interface	100	*Table 4-5, Processor Interface 0 Signal Pins,* on page 35.
	100	*Table 4-6, Processor Interface 1 Signal Pins,* on page 35.
	5	*Table 4-7, Processor Interface Support Signal Pins,* on page 36.
	10	*Table 4-8, Processor Interface Power Management Signal Pins,* on page 36.
System Support	5	*Table 4-9, System Support Signal Pins,* on page 37.
I^2C	6	*Table 4-10, I2C Signal Pins,* on page 37.
Clock and PLL	23	*Table 4-11, Clock and PLL Signal Pins,* on page 37.
JTAG and Test	9	*Table 4-12, JTAG and Test Support Signal Pins,* on page 38.
Power Supply (VDDx and GND)	504	*Table 4-13, Power Supply Pins,* on page 39.
Other Pins	1	*Table 4-14, Other Signal Pins,* on page 39.
		Table 4-15, CPC945 128-Bit DIMM Slot Configuration, on page 39.
Pin List by Signal Names		*Table 4-16, CPC945 Bridge and Memory Controller Pin List by Signal Name,* on page 41
Pin List by Grid Position		*Table 4-17, CPC945 Bridge and Memory Controller Pin List by Grid Position,* on page 53

Table 4-2. PCIE Signal Pins (Page 1 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PCIE_HSOP[15:0]	PCI Express Transmit Bus - Positive differential signal.	Output	1.5 V	VDD
PCIE_HSON[15:0]	PCI Express Transmit Bus - Negative differential signal.	Output	1.5 V	VDD
PCIE_HISP[15:0]	PCI Express Receive Bus - Positive differential signal	Input	1.5 V	VDD
PCIE_HISN[15:0]	PCI Express Receive Bus - Negative differential signal.	Input	1.5 V	VDD
PCIE_AV25_0 PCIE_AV25_1 PCIE_AV25_2	PCI Express PHY analog voltage regulator input.	Analog Power	1.65-2.75 V	N/A

Table 4-2. PCIE Signal Pins (Page 2 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PCIE_AVREG_0 PCIE_AVREG_1 PCIE_AVREG_2	PCI Express PHY analog voltage regulator monitor output, test only.	Output	N/A	N/A
PCIE_UCAL_RES0 PCIE_UCAL_RES1	Calibration resistor input.	Reference	N/A	N/A
$\overline{\text{PCIE\_PRESENTN}}$	Slot present, an open drain with external pull up. Low input indicates PCI-E card is present.	Input	2.5 V	VDD5

Table 4-3. DDR SDRAM Signal Pins (Page 1 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
DDR_DQ[0:143]	DDR Ram data bus [0:143], 128 bits of data, 16 bits of ECC.	I/O	1.8 V	VDD3
DDR_DQSP[0:17]	Positive I/O of the Differential Data StrobesDQS[0:17] for DDR_DQ[0:143]: DDR_DQ[0:7] - DDR_DQS[0], DDR_DQ[8:15] - DDR_DQS[1], DDR_DQ[16:23] -DDR_DQS[2], DDR_DQ[24:31] - DDR_DQS[3], DDR_DQ[32:39] - DDR_DQS[4], DDR_DQ[40:47] - DDR_DQS[5], DDR_DQ[48:55] - DDR_DQS[6], DDR_DQ[56:63] - DDR_DQS[7], DDR_DQ[64:71] - DDR_DQS[8], DDR_DQ[72:79] - DDR_DQS[9], DDR_DQ[80:87] - DDR_DQS[10], DDR_DQ[88:95] - DDR_DQS[11], DDR_DQ[96:103] -DDR_DQS[12], DDR_DQ[104:111] - DDR_DQS[13], DDR_DQ[112:119] - DDR_DQS[14], DDR_DQ[120:127] - DDR_DQS[15], DDR DQ[128:135] - DDR_DQS[16], DDR DQ[136:143] - DDR_DQS[17]	I/O	1.8 V	VDD3
DDR_DQSN[0:17]	Negative I/O of the Differential Data Strobes DQS[0:17].	I/O	1.8 V	VDD3
DDR_VREF_0_1	Voltage reference for DDR_DQ[0:15] & DDR_DQS[0:1]. VREF is typically generated using external low value (<1K OHM), 1-percent precision resistors. These voltage references should also be bypassed to ground with a capacitor to track any ground noise. The reference voltages must be stable and low noise. The input current into the VREF pins is negligible.	Reference	0.5 × VDD3	VDD3
DDR_VREF_2_3	Voltage reference for DDR_DQ[16:31] & DDR_DQS[2:3]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3
DDR_VREF_4_16	Voltage reference for DDR_DQ[32:39] &DDR_DQS[4], DDR_DQ[128:135] &DDR_DQS[16]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3
DDR_VREF_5_6	Voltage reference for DDR_DQ[40:55] &DDR_DQS[5:6]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3
DDR_VREF_7_8	Voltage reference for DDR_DQ[56:71] &DDR_DQS[7:8]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3
DDR_VREF_9_10	Voltage reference for DDR_DQ[72:87] &DDR_DQS[9:10]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3
DDR_VREF_11_17	Voltage reference for DDR_DQ[88:95] &DDR_DQS[11], DDR_DQ[136:143] &DDR_DQS[17]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3
DDR_VREF_12_13	Voltage reference for DDR_DQ[112:127] &DDR_DQS[14:15]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3

Table 4-3. DDR SDRAM Signal Pins (Page 2 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
DDR_VREF_14_15	Voltage reference for DDR_DQ[96:111] &DDR_DQS[12:13]. See DDR_VREF_0_1 for implementation details.	Reference	0.5 × VDD3	VDD3
DDR_CK_A	Positive output of the differential clock to bank 0 of the SDRAM.	Output	1.8 V	VDD3
DDR_CK_AN	Negative output of the differential clock to bank 0 of the SDRAM.	Output	1.8 V	VDD3
DDR_CK_B	Positive output of the differential clock to bank 1 of the SDRAM.	Output	1.8 V	VDD3
DDR_CK_BN	Negative output of the differential clock to bank 1 of the SDRAM.	Output	1.8 V	VDD3
DDR_CKE[0:7]	The SDRAM clock enables.	Output	1.8 V	VDD3
DDR_CS[0:15]	SDRAM chip selects.	Output	1.8 V	VDD3
DDR_BA[0:2]	SDRAM bank address.	Output	1.8 V	VDD3
DDR_MAD[0:15]	Address input to SDRAM.	Output	1.8 V	VDD3
DDR_RAS	Memory command, row enables.	Output	1.8 V	VDD3
DDR_CAS	Memory command, column enables.	Output	1.8 V	VDD3
DDR_WE	Memory commands, write enables.	Output	1.8 V	VDD3
DDR_MUXEN[0:7]	Mux selects for data external data mux.	Output	1.8 V	VDD3
DDR_ODT[0:7]	8 bits of the On Die Termination (ODT).	Output	1.8 V	VDD3

Table 4-4. HyperTransport Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
HT_CAD_TXP[0:15]	Differential signal for Command, Address and Data Bus Transmitter (Positive).	Output	1.2 V	VDD4
HT_CAD_TXN[0:15]	Differential signal for Command, Address and Data Bus Transmitter (Negative).	Output	1.2 V	VDD4
HT_CLK_TXN[0:1]	Differential signal for CAD [0:7] clock Transmitter (Positive).	Output	1.2 V	VDD4
HT_CLK_TXP[0:1]	Differential signal for CAD [0:7] clock Transmitter (Negative).	Output	1.2 V	VDD4
HT_CTL_TXP0 HT_CTL_TXP1	Differential signal for Control Transmitter (Positive).	Output	1.2 V	VDD4
HT_CTL_TXN0 HT_CTL_TXN1	Differential signal for Control Transmit (Negative).	Output	1.2 V	VDD4
HT_PWROK	HyperTransport Power OK.	I/O	2.5 V	VDD5
$\overline{\text{HT\_RESET\_L}}$	HyperTransport Reset.	I/O	2.5 V	VDD5
$\overline{\text{HT\_LDTSTOP\_L}}$	HyperTransport Power down request.	I/O	2.5 V	VDD5
$\overline{\text{HT\_LDTREQ\_L}}$	Reenabling link for normal operation.	I/O	2.5 V	VDD5
HT_CAD_RXP[0:15]	Differential signal for Command, Address and Data Bus Receive (Positive).	Input	1.2 V	VDD4
HT_CAD_RXN[0:15]	Differential signal for Command, Address and Data Bus Receive (Negative).	Input	1.2 V	VDD4
HT_CLK_RXP[0:1]	Differential signal for CAD [0:7] clock Receiver (Positive).	Input	1.2 V	VDD4
HT_CLK_RXN[0:1]	Differential signal for CAD [0:7] clock Receiver (Negative).	Input	1.2 V	VDD4
HT_CTL_RXP0 HT_CTL_RXP1	Differential signal for Control Receive (Positive).	Input	1.2 V	VDD4
HT_CTL_RXN0 HT_CTL_RXN1	Differential signal for Control Receive (Negative).	Input	1.2 V	VDD4
HT_PVTREF0 HT_PVTREF1	This I/O requires an external 100 Ohms precision resistor between HT_PVTREF0 and HT_PVTREF1.	Reference	N/A	N/A
HT_PVTREF2 HT_PVTREF3	This I/O requires an external 200 Ohms precision resistor between HT_PVTREF2 and HT_PVTREF3.	Reference	N/A	N/A

Table 4-5. Processor Interface 0 Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PI0_ADO[0:43]	PI Input Data from processor 0 or 1 on bus 0. ADO[0:44] represents the address, data and control information which can be balanced code encoded or 36-bit un-encoded signal plus 8-bit parity bits. When data transmitted unencoded, AD[0:35] = data, AD[36] = transfer handshake and AD[37:43] = parity.	Input	1.3 V - 1.5 V	VDD2
PI0_SROP[0:1]	Snoop coherency response from the processor #0 or 1 to CPC945.	Input	1.3 V - 1.5 V	VDD2
PI0_SRON[0:1]	Complement signals to PI0_SROP[0:1].	Input	1.3 V - 1.5 V	VDD2
PI0_BCLKOP	BCLKI is the differential bus clock input from the transmitting agent used to strobe incoming data by the receiver. PI0_BCLKOP is the positive input from processor #0 or 1 to CPC945.	Input	1.3 V - 1.5 V	VDD2
PI0_BCLKON	Negative input of the differential bus clock PI0_BCLKP.	Input	1.3 V - 1.5 V	VDD2
PI0_ADI[0:43]	PI Output Data to processors 0 or 1 on bus 0. ADI[0:44] represents the address, data and control information which can be balanced code encoded or 36-bit un-encoded signal plus 8-bit parity bits. When data transmitted un-encoded, ADI[0:35] = data, ADI[36] = transfer handshake and ADI[37:43] = parity.	Output	1.3 V - 1.5 V	VDD2
PI0_SRIP[0:1]	The snoop response is the accumulated snoop coherency response output from CPC945 to processors #0, 1.	Output	1.3 V - 1.5 V	VDD2
PI0_SRIN[0:1]	Complementary signals to PI0_SRIP[0:1].	Output	1.3 V - 1.5 V	VDD2
PI0_BCLKIP	BCLKI is the differential bus clock from the transmitting agent used to strobe incoming data by the receiver. PI_BCLKIP is the positive output from CPC945 to processor bus 0.	Output	1.3 V - 1.5 V	VDD2
PI0_BCLKIN	The negative output of PI0_BCLKIP to processor bus 0 from CPC945.	Output	1.3 V - 1.5 V	VDD2

Note: For the PIO, the driver impedance is controllable to 20 Ω and 40 Ω. The receiver has a 90 Ω termination that can be deactivated. Refer to CPC 945 User's Manual for more information.

Table 4-6. Processor Interface 1 Signal Pins (Page 1 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PI1_ADO[0:43]	PI Input Data from processors 2, 3 on bus 1. ADO[0:43] represents the address, data and control information which can be balanced code encoded or 36-bit un-encoded signal plus 8-bit parity bits. When data transmitted un-encoded, ADO[0:35] = data, ADO[36] = transfer handshake and ADO[37:43] = parity.	Input	1.3 V - 1.5 V	VDD2
PI1_SROP[0:1]	Snoop coherency response from processors #2,3 to CPC945.	Input	1.3 V - 1.5 V	VDD2
PI1_SRON[0:1]	Complementary signals to PI1_SROP[0:1].	Input	1.3 V - 1.5 V	VDD2
PI1_BCLKOP	BCLKO is the differential bus clock input from the transmitting agent used to strobe incoming data by the receiver.	Input	1.3 V - 1.5 V	VDD2
PI1_BCLKON	Negative input of the differential bus clock PI1_BCLKP.	Input	1.3 V - 1.5 V	VDD2

Table 4-6. Processor Interface 1 Signal Pins (Page 2 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PI1_ADI[0:43]	PI output Data to processors 2, 3 on bus 1. ADI[0:43] represents the address, data and control information which can be balanced code encoded or 36-bit un-encoded signal plus 8-bit parity bits. When data transmitted un-encoded, ADI[0:35] = data, ADI[36] = transfer hand-shake and ADI[37:43] = parity.	Output	1.3 V - 1.5 V	VDD2
PI1_SRIP[0:1]	The snoop response output is the accumulated snoop coherency response from CPC945 to processor #2,3.	Output	1.3 V - 1.5 V	VDD2
PI1_SRIN[0:1]	Complementary signals to PI1_SRIP[0:1].	Output	1.3 V - 1.5 V	VDD2
PI1_BCLKIP	The positive differential bus clock sent from the CPC945 to the PowerPC 970 processor 1. The clock is used by processor 1 to strobe incoming data. BCLKI is the differential bus clock from the transmitting agent used to strobe incoming data by the receiver. PI_BCLKIP is the positive output from CPC945 to processor bus 1.	Output	1.3 V - 1.5 V	VDD2
PI1_BCLKIN	The negative output of PI0_BCLKIP to processor bus 1 from CPC945.	Output	1.3 V - 1.5 V	VDD2
Note: For the PIO, the driver impedance is controllable to 20 Ω and 40 Ω. The receiver has a 90 Ω termination that can be deactivated. Refer to *CPC 945 User's Manual* for more information.				

Table 4-7. Processor Interface Support Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PI0_APSYNC	PI clocking signal used to provide system-wide synchronization. This pin is an input from a clock chip which generates the appropriate timing for CPC945 and each processor.	Input	1.3 V - 1.5 V	VDD2
PI1_APSYNC	This signal is unused and should be left floating.	Output	1.3 V - 1.5 V	VDD2
$\overline{\text{PI\_CSTP}}$	PI check stop.	I/O	1.3 V - 1.5 V	VDD2
PI0_SE	Logic analyzer trigger 0.	Output	1.3 V - 1.5 V	VDD2
PI1_SE	Logic analyzer trigger 1.	Output	1.3 V - 1.5 V	VDD2

Table 4-8. Processor Interface Power Management Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
$\overline{\text{PI\_QREQ}}$[0:3]	Processor sleep requests. To ensure proper operation, unused inputs should be pulled down.	Input	1.3 V - 1.5 V	VDD2
$\overline{\text{PI\_QACK}}$[0:3]	These signals provide the CPC945 acknowledgment to processor sleep requests.	Output	1.3 V - 1.5 V	VDD2
$\overline{\text{SUSPENDREQ\_L}}$	Suspend request. This active-low signal is sent from the power management unit (under software control) to the CPC945 to request that the device stop all activity and enter the suspend (sleep) state.	Input	2.5 V	VDD5
$\overline{\text{SUSPENDACK\_L}}$	Suspend acknowledgement. The CPC945 asserts this active-low signal back to the power management unit to indicate the suspension request is complete.	Output	2.5 V	VDD5

Table 4-9. System Support Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
IRQ[0:3]	The interrupt outputs from the CPC945 to the PowerPC 970 processors.	Output	1.3 V - 1.5 V	VDD2
NORTH_BRIDGE_RESET_L	Power on reset input to CPC945.	Input	2.5 V	VDD5

Table 4-10. I^2C Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PI_ISCA	I^2C slave only data bus. Used by the power management unit to set up the processor interface and the debug facilities. It is also a portal for diagnostic reads and writes to any system address.	I/O	2.5 V	VDD5
PI_ISCL	Strobe signal for PI_ISCA.	I/O	2.5 V	VDD5
SYS_ISCA0	I^2C master bus 0. Used to configure the system SDRAM.	I/O	2.5 V	VDD5
SYS_ISCL0	Strobe signal for SYS_ISCA0.	I/O	2.5 V	VDD5
SYS_ISCA1	I^2C master bus 1. This can also be used to configure the system SDRAM.	I/O	2.5 V	VDD5
SYS_ISCL1	Strobe signal for SYS_ISCA1.	I/O	2.5 V	VDD5

Table 4-11. Clock and PLL Signal Pins (Page 1 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PI_APCLK_AGND	Analog ground for PLL.	Analog GND		
PI_APCLK_AVDD	Analog Power for PLL.	Analog Power	1.5 V	1.5 V
PI_REFCLK_P PI_REFCLK_N	Differential PI reference clock positive input. This is a 1.3 V -1.5 V signal.	Input	1.3 V-1.5 V	VDD2
HT_REFCLK_P HT_REFCLK_N	HT clock reference input. This is a 2.5 V signal.	Input	2.5 V	VDD5
HT_REFCLK_AGND	Analog ground for PLL.	Analog GND		
HT_REFCLK_AVDD HT_REFCLK_AVDD2	Analog Power for PLL.	Analog Power	1.65 V- 2.75 V	
DDR_REFCLK_P DDR_REFCLK_N	DDR2 reference clk input.	Input	2.5 V	VDD5
DDR_CLK_AGND	Analog ground for PLL.	Analog GND		
DDR_CLK_AVDD	Analog Power for PLL.	Analog Power	1.5 V	1.5 V

Table 4-11. Clock and PLL Signal Pins (Page 2 of 2)

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
PCIE_REFCLK_P PCIE_REFCLK_N	Reference clock input for PCI-Express PLL. This is a 1.5 V signal.	Input	1.5 V	VDD
PCIE_REFCLK_AGNDA PCIE_REFCLK_AGNDB	Analog ground for PLL.	Analog GND		
PCIE_REFCLK_AVDD2 PCIE_REFCLK_AVDDA PCIE_REFCLK_AVDDB	Analog Power for PLL.	Analog Power	1.65 V-2.75 V	
PMR_CLK_P PMR_CLK_N	Reference clock input for power management.	Input	2.5 V	VDD5
PMR_CLK_STOP	External clock stop for power management.	Input	2.5 V	VDD5
Note: AVDDx supplies must have dedicated filters; otherwise, severe degradation can occur when AVDDx supplies are shared between PLLs.				

Table 4-12. JTAG and Test Support Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
CE1_DI1_TMS	JTAG TMS. It should be tied high during normal (non-test) operation.	JTAG	2.5 V	VDD5
CE1_DI2_TRST	JTAG TRST. It should be tied high during normal (non-test) operation	JTAG	2.5 V	VDD5
CE1_LT_TCK	JTAG TCK. It should be tied high during normal (non-test) operation.	JTAG	2.5 V	VDD5
CE0_TEST	IBM test pin. Set this test pin to '0' for normal (non-test) operation.	Test	1.5 V	VDD
SYS_THDIO_D	The anode of a thermal test diode, which can be used to measure the junction temperature of the device. The internal thermal diode does require some precision equipment so it may only be useful for lab analysis. These pins have ESD protection so they can be wired out to test points. If a design is not going to use the diode, this I/O should be grounded. Contact IBM PowerPC applications engineering if additional information is required. Refer to IBM Cu11_IO data sheet, cell name THERMALDIO_A cell.	Reference	N/A	N/A
SYS_THDIO_G	The cathode of a thermal test diode, which can be used to measure the junction temperature of the device. The internal thermal diode does require some precision equipment so it may only be useful for lab analysis. These pins have ESD protection so they can be wired out to test points. If a design is not going to use the diode, this I/O should be grounded. Contact IBM PowerPC applications engineering if additional information is required.	Reference	N/A	N/A
CE1_MC_TDI	JTAG TDI, refer to IEEE 1149 spec. It should be tied high during normal (non-test) operation.	JTAG	2.5 V	VDD5
OBSV	PLL outputs observer / scope trigger. The output of this pin is the PLL frequency divided by 8. For example, the PCIE PLL outputs 625 MHz, so the observable frequency would be 78.125 MHz.	Output	1.8 V	VDD4
TDO	JTAG TDO. This is an output for JTAG. Tying it high in normal (non-test) operation is ok.	JTAG	2.5 V	VDD5
LSSD_RI	Receiver inhibit test pin input. This pin should be tied high in normal (non-test) operation.	Test	2.5 V	VDD5

Table 4-13. Power Supply Pins

Signal Name	Signal Description	Signal Type
VDD	The motherboard supplies 1.5 V to the core logic through these pins.	Supply
VDD2	The motherboard supplies 1.3 V - 1.5 V to the processor interface.	Supply
VDD3	The motherboard supplies 1.8 V to the DDR2 memory controller interface I/O drivers through these pins.	Supply
VDD4	The motherboard supplies 1.2 V to the HyperTransport I/O drivers through these pins.	Supply
VDD5	The motherboard supplies 2.5 V to the I^2C and miscellaneous signals through these pins.	Supply
GND	The motherboard supplies ground to the device through these pins. These grounds are separate from the PLL analog grounds.	Supply

Table 4-14. Other Signal Pins

Signal Name	Signal Description	Signal Type	Signal Levels	I/O Supply Voltage
$\overline{\text{CHP\_FAULT\_N}}$	This active low signal is activated whenever an exception, previously enabled through the APIMASK1 register, occurs. See *CPC945 User's Manual* for details.	Output	1.8 V	VDD3

Table 4-15. CPC945 128-Bit DIMM Slot Configuration

Physical Rank	DDR_DQ[0:63]				DDR_DQ[64:127]			
0	DIMM0	$\overline{\text{DDR\_CS}}$[0]	DDR_CKE[0]	DDR_ODT[0]	DIMM1	$\overline{\text{DDR\_CS}}$[8]	DDR_CKE[0]	DDR_ODT[4]
1		$\overline{\text{DDR\_CS}}$[1]	DDR_CKE[1]	GND		$\overline{\text{DDR\_CS}}$[9]	DDR_CKE[1]	GND
2	DIMM2	$\overline{\text{DDR\_CS}}$[2]	DDR_CKE[2]	DDR_ODT[1]	DIMM3	$\overline{\text{DDR\_CS}}$[10]	DDR_CKE[2]	DDR_ODT[5]
3		$\overline{\text{DDR\_CS}}$[3]	DDR_CKE[3]	GND		$\overline{\text{DDR\_CS}}$[11]	DDR_CKE[3]	GND
4	DIMM4	$\overline{\text{DDR\_CS}}$[4]	DDR_CKE[4]	DDR_ODT[2]	DIMM5	$\overline{\text{DDR\_CS}}$[12]	DDR_CKE[4]	DDR_ODT[6]
5		$\overline{\text{DDR\_CS}}$[5]	DDR_CKE[5]	GND		$\overline{\text{DDR\_CS}}$[13]	DDR_CKE[5]	GND
6	DIMM6	$\overline{\text{DDR\_CS}}$[6]	DDR_CKE[6]	DDR_ODT[3]	DIMM7	$\overline{\text{DDR\_CS}}$[14]	DDR_CKE[6]	DDR_ODT[7]
7		$\overline{\text{DDR\_CS}}$[7]	DDR_CKE[7]	GND		$\overline{\text{DDR\_CS}}$[15]	DDR_CKE[7]	GND

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 1 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
CE0_TEST	AG08	DDR_CS14	G29	DDR_DQ34	AD31
CE1_DI1_TMS	AL02	DDR_CS15	E27	DDR_DQ35	AG28
CE1_DI2_TRST	AK06	DDR_DQ0	AP31	DDR_DQ36	AD34
CE1_LT_TCK	AJ04	DDR_DQ1	AP32	DDR_DQ37	AD35
CE1_MC_TDI	AG07	DDR_DQ2	AN32	DDR_DQ38	AH35
$\overline{\text{CHP\_FAULT\_N}}$	AH22	DDR_DQ3	AM30	DDR_DQ39	AH34
DDR_BA0	AL22	DDR_DQ4	AN30	DDR_DQ40	AB36
DDR_BA1	AP28	DDR_DQ5	AP30	DDR_DQ41	AC34
DDR_BA2	AN28	DDR_DQ6	AR30	DDR_DQ42	AA31
DDR_CAS	AM24	DDR_DQ7	AM32	DDR_DQ43	AD36
DDR_CK_A	AR28	DDR_DQ8	AM36	DDR_DQ44	AB35
DDR_CK_AN	AT28	DDR_DQ9	AK31	DDR_DQ45	AB34
DDR_CK_B	AL26	DDR_DQ10	AL34	DDR_DQ46	AB33
DDR_CK_BN	AK26	DDR_DQ11	AT34	DDR_DQ47	AC31
DDR_CKE0	AJ24	DDR_DQ12	AR34	DDR_DQ48	V32
DDR_CKE1	AH24	DDR_DQ13	AN34	DDR_DQ49	Y32
DDR_CKE2	AL21	DDR_DQ14	AM33	DDR_DQ50	V31
DDR_CKE3	AP21	DDR_DQ15	AM34	DDR_DQ51	Y33
DDR_CKE4	AT22	DDR_DQ16	AH31	DDR_DQ52	V33
DDR_CKE5	AP22	DDR_DQ17	AK34	DDR_DQ53	V34
DDR_CKE6	AN22	DDR_DQ18	AH32	DDR_DQ54	V35
DDR_CKE7	AM22	DDR_DQ19	AK33	DDR_DQ55	Y29
DDR_CS0	AL27	DDR_DQ20	AH30	DDR_DQ56	V30
DDR_CS1	AP33	DDR_DQ21	AH29	DDR_DQ57	Y34
DDR_CS2	AJ31	DDR_DQ22	AJ34	DDR_DQ58	Y35
DDR_CS3	AF31	DDR_DQ23	AK32	DDR_DQ59	U34
DDR_CS4	AH33	DDR_DQ24	AE31	DDR_DQ60	AB28
DDR_CS5	AB32	DDR_DQ25	AG34	DDR_DQ61	AB27
DDR_CS6	V36	DDR_DQ26	AE34	DDR_DQ62	W34
DDR_CS7	W31	DDR_DQ27	AH36	DDR_DQ63	AA28
DDR_CS8	V29	DDR_DQ28	AF36	DDR_DQ64	P32
DDR_CS9	R34	DDR_DQ29	AF35	DDR_DQ65	T36
DDR_CS10	M32	DDR_DQ30	AF34	DDR_DQ66	U31
DDR_CS11	M28	DDR_DQ31	AG31	DDR_DQ67	P31
DDR_CS12	H35	DDR_DQ32	AF29	DDR_DQ68	T30

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 2 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
DDR_CS13	D36	DDR_DQ33	AF30	DDR_DQ69	T29
DDR_DQ70	T28	DDR_DQ107	F34	DDR_DQSN0	AT32
DDR_DQ71	W28	DDR_DQ108	C34	DDR_DQSN1	AP36
DDR_DQ72	P34	DDR_DQ109	D34	DDR_DQSN2	AK36
DDR_DQ73	T34	DDR_DQ110	D35	DDR_DQSN3	AF32
DDR_DQ74	P33	DDR_DQ111	E34	DDR_DQSN4	AD32
DDR_DQ75	T35	DDR_DQ112	D31	DDR_DQSN5	AB31
DDR_DQ76	P35	DDR_DQ113	E31	DDR_DQSN6	Y30
DDR_DQ77	P36	DDR_DQ114	C31	DDR_DQSN7	Y28
DDR_DQ78	R31	DDR_DQ115	F30	DDR_DQSN8	V27
DDR_DQ79	T31	DDR_DQ116	A33	DDR_DQSN9	T32
DDR_DQ80	K36	DDR_DQ117	B33	DDR_DQSN10	M35
DDR_DQ81	M34	DDR_DQ118	C32	DDR_DQSN11	P28
DDR_DQ82	K35	DDR_DQ119	C30	DDR_DQSN12	H32
DDR_DQ83	N31	DDR_DQ120	D27	DDR_DQSN13	F32
DDR_DQ84	L31	DDR_DQ121	F29	DDR_DQSN14	B31
DDR_DQ85	L34	DDR_DQ122	E29	DDR_DQSN15	A27
DDR_DQ86	M31	DDR_DQ123	D29	DDR_DQSN16	AD28
DDR_DQ87	M33	DDR_DQ124	C29	DDR_DQSN17	K33
DDR_DQ88	M27	DDR_DQ125	B29	DDR_DQSP0	AR32
DDR_DQ89	R28	DDR_DQ126	A29	DDR_DQSP1	AP35
DDR_DQ90	U28	DDR_DQ127	C28	DDR_DQSP2	AK35
DDR_DQ91	T27	DDR_DQ128	AB29	DDR_DQSP3	AF33
DDR_DQ92	N28	DDR_DQ129	AC28	DDR_DQSP4	AD33
DDR_DQ93	P29	DDR_DQ130	AF27	DDR_DQSP5	AB30
DDR_DQ94	P30	DDR_DQ131	AE28	DDR_DQSP6	Y31
DDR_DQ95	N34	DDR_DQ132	AD29	DDR_DQSP7	Y27
DDR_DQ96	G34	DDR_DQ133	AD30	DDR_DQSP8	V28
DDR_DQ97	J31	DDR_DQ134	Y36	DDR_DQSP9	T33
DDR_DQ98	G31	DDR_DQ135	AA34	DDR_DQSP10	M36
DDR_DQ99	J34	DDR_DQ136	F36	DDR_DQSP11	P27
DDR_DQ100	H30	DDR_DQ137	K31	DDR_DQSP12	H33
DDR_DQ101	H36	DDR_DQ138	K34	DDR_DQSP13	F33
DDR_DQ102	H31	DDR_DQ139	F35	DDR_DQSP14	A31
DDR_DQ103	H34	DDR_DQ140	M30	DDR_DQSP15	B27
DDR_DQ104	B35	DDR_DQ141	L28	DDR_DQSP16	AD27
DDR_DQ105	F31	DDR_DQ142	K29	DDR_DQSP17	K32

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 3 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
DDR_DQ106	C33	DDR_DQ143	K30	DDR_MAD0	AN26
DDR_MAD1	AP26	DDR_VREF_2_3	AD26	depop	AD18
DDR_MAD2	AR26	DDR_VREF_4_16	AB26	depop	AD19
DDR_MAD3	AT26	DDR_VREF_5_6	Y26	depop	AD22
DDR_MAD4	AM26	DDR_VREF_7_8	V26	depop	AD23
DDR_MAD5	AL25	DDR_VREF_9_10	T26	depop	AE12
DDR_MAD6	AP25	DDR_VREF_11_17	P26	depop	AE13
DDR_MAD7	AH28	DDR_VREF_12_13	M26	depop	AE16
DDR_MAD8	AL30	DDR_VREF_14_15	F28	depop	AE17
DDR_MAD9	AR22	DDR_WE	AP23	depop	AE20
DDR_MAD10	AJ28	depop	A01	depop	AE21
DDR_MAD11	AH27	depop	A02	depop	AE24
DDR_MAD12	AH26	depop	A35	depop	AE25
DDR_MAD13	AH25	depop	A36	depop	AG06
DDR_MAD14	AJ26	depop	AA12	depop	AM35
DDR_MAD15	AK24	depop	AA13	depop	AR01
DDR_MUXEN0	AP27	depop	AA16	depop	AR36
DDR_MUXEN1	AM28	depop	AA17	depop	AT01
DDR_MUXEN2	AL28	depop	AA20	depop	AT02
DDR_MUXEN3	AK28	depop	AA21	depop	AT35
DDR_MUXEN4	AK30	depop	AA24	depop	AT36
DDR_MUXEN5	AT30	depop	AA25	depop	B01
DDR_MUXEN6	AL29	depop	AB14	depop	B36
DDR_MUXEN7	AP29	depop	AB15	depop	K11
DDR_ODT0	AL23	depop	AB18	depop	K28
DDR_ODT1	AT24	depop	AB19	depop	M14
DDR_ODT2	AR24	depop	AB22	depop	M15
DDR_ODT3	AN24	depop	AB23	depop	M18
DDR_ODT4	AP24	depop	AC12	depop	M19
DDR_ODT5	AK22	depop	AC13	depop	M22
DDR_ODT6	AF28	depop	AC16	depop	M23
DDR_ODT7	M29	depop	AC17	depop	N12
DDR_RAS	AL24	depop	AC20	depop	N13
DDR_REFCLK_AGND	AH21	depop	AC21	depop	N16
DDR_REFCLK_AVDD	AH23	depop	AC24	depop	N17
DDR_REFCLK_N	AG24	depop	AC25	depop	N20
DDR_REFCLK_P	AF24	depop	AD14	depop	N21

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 4 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
DDR_VREF_0_1	AG26	depop	AD15	depop	N24
depop	N25	depop	W16	#GND	AC23
depop	P14	depop	W17	#GND	AC27
depop	P15	depop	W20	#GND	AC30
depop	P18	depop	W21	#GND	AC33
depop	P19	depop	W24	#GND	AC36
depop	P22	depop	W25	#GND	AD02
depop	P23	depop	Y14	#GND	AD05
depop	R12	depop	Y15	#GND	AD08
depop	R13	depop	Y18	#GND	AD11
depop	R16	depop	Y19	#GND	AD13
depop	R17	depop	Y22	#GND	AD17
depop	R20	depop	Y23	#GND	AD21
depop	R21	#GND	A06	#GND	AD25
depop	R24	#GND	A10	#GND	AE15
depop	R25	#GND	A14	#GND	AE19
depop	T14	#GND	A18	#GND	AE23
depop	T15	#GND	A22	#GND	AE26
depop	T18	#GND	A26	#GND	AE29
depop	T19	#GND	A30	#GND	AE32
depop	T22	#GND	A34	#GND	AE35
depop	T23	#GND	AA14	#GND	AF01
depop	U12	#GND	AA18	#GND	AF04
depop	U13	#GND	AA22	#GND	AF07
depop	U16	#GND	AA26	#GND	AF10
depop	U17	#GND	AA29	#GND	AF13
depop	U20	#GND	AA32	#GND	AF17
depop	U21	#GND	AA35	#GND	AF21
depop	U24	#GND	AB01	#GND	AF25
depop	U25	#GND	AB04	#GND	AG11
depop	V14	#GND	AB07	#GND	AG15
depop	V15	#GND	AB10	#GND	AG19
depop	V18	#GND	AB12	#GND	AG23
depop	V19	#GND	AB16	#GND	AG27
depop	V22	#GND	AB20	#GND	AG30
depop	V23	#GND	AB24	#GND	AG33
depop	W12	#GND	AC15	#GND	AG36

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 5 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
depop	W13	#GND	AC19	#GND	AH02
#GND	AH05	#GND	AN31	#GND	D30
#GND	AH08	#GND	AN35	#GND	D33
#GND	AJ08	#GND	AP01	#GND	E08
#GND	AJ09	#GND	AR05	#GND	E12
#GND	AJ13	#GND	AR09	#GND	E16
#GND	AJ17	#GND	AR13	#GND	E20
#GND	AJ21	#GND	AR17	#GND	E24
#GND	AJ25	#GND	AR21	#GND	E28
#GND	AJ29	#GND	AR25	#GND	E32
#GND	AJ32	#GND	AR29	#GND	E35
#GND	AJ35	#GND	AR33	#GND	F01
#GND	AK01	#GND	AR35	#GND	F04
#GND	AK04	#GND	AT03	#GND	F06
#GND	AK07	#GND	AT07	#GND	G10
#GND	AK11	#GND	AT11	#GND	G14
#GND	AK15	#GND	AT15	#GND	G18
#GND	AK19	#GND	AT19	#GND	G22
#GND	AK23	#GND	AT23	#GND	G26
#GND	AK27	#GND	AT27	#GND	G30
#GND	AL31	#GND	AT31	#GND	G33
#GND	AL33	#GND	B02	#GND	G36
#GND	AL36	#GND	B04	#GND	H02
#GND	AM02	#GND	B08	#GND	H05
#GND	AM05	#GND	B12	#GND	H08
#GND	AM09	#GND	B16	#GND	H12
#GND	AM13	#GND	B20	#GND	H16
#GND	AM17	#GND	B24	#GND	H20
#GND	AM21	#GND	B28	#GND	H24
#GND	AM25	#GND	B32	#GND	H28
#GND	AM29	#GND	C36	#GND	H29
#GND	AN04	#GND	D02	#GND	J29
#GND	AN07	#GND	D06	#GND	J32
#GND	AN11	#GND	D10	#GND	J35
#GND	AN15	#GND	D14	#GND	K01
#GND	AN19	#GND	D18	#GND	K04
#GND	AN23	#GND	D22	#GND	K07

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 6 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
#GND	AN27	#GND	D26	#GND	K10
#GND	K14	#GND	R23	#GND	Y08
#GND	K18	#GND	R27	#GND	Y11
#GND	K22	#GND	R30	#GND	Y13
#GND	K26	#GND	R33	#GND	Y17
#GND	L12	#GND	R36	#GND	Y21
#GND	L16	#GND	T02	#GND	Y25
#GND	L20	#GND	T05	HT_CAD_RXN0	F26
#GND	L24	#GND	T08	HT_CAD_RXN1	F25
#GND	L27	#GND	T11	HT_CAD_RXN2	A25
#GND	L30	#GND	T13	HT_CAD_RXN3	G25
#GND	L33	#GND	T17	HT_CAD_RXN4	L25
#GND	L36	#GND	T21	HT_CAD_RXN5	G27
#GND	M02	#GND	T25	HT_CAD_RXN6	J25
#GND	M05	#GND	U14	HT_CAD_RXN7	C26
#GND	M08	#GND	U18	HT_CAD_RXN8	E23
#GND	M11	#GND	U22	HT_CAD_RXN9	A23
#GND	M13	#GND	U26	HT_CAD_RXN10	H23
#GND	M16	#GND	U29	HT_CAD_RXN11	C22
#GND	M20	#GND	U32	HT_CAD_RXN12	K23
#GND	M25	#GND	U35	HT_CAD_RXN13	J23
#GND	N14	#GND	V01	HT_CAD_RXN14	A21
#GND	N18	#GND	V04	HT_CAD_RXN15	C24
#GND	N22	#GND	V07	HT_CAD_RXP0	F27
#GND	N26	#GND	V10	HT_CAD_RXP1	F24
#GND	N29	#GND	V12	HT_CAD_RXP2	B25
#GND	N32	#GND	V16	HT_CAD_RXP3	H25
#GND	N35	#GND	V20	HT_CAD_RXP4	K25
#GND	P01	#GND	V24	HT_CAD_RXP5	H27
#GND	P04	#GND	W15	HT_CAD_RXP6	J26
#GND	P07	#GND	W19	HT_CAD_RXP7	C27
#GND	P10	#GND	W23	HT_CAD_RXP8	D23
#GND	P12	#GND	W27	HT_CAD_RXP9	B23
#GND	P16	#GND	W30	HT_CAD_RXP10	G23
#GND	P20	#GND	W33	HT_CAD_RXP11	C23
#GND	P24	#GND	W36	HT_CAD_RXP12	L23
#GND	R15	#GND	Y02	HT_CAD_RXP13	J24

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 7 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
#GND	R19	#GND	Y05	HT_CAD_RXP14	B21
HT_CAD_RXP15	C25	HT_CLK_RXP1	F23	PCIE_AV25_1	J07
HT_CAD_TXN0	F16	HT_CLK_TXN0	J19	PCIE_AV25_2	H11
HT_CAD_TXN1	G17	HT_CLK_TXN1	C16	PCIE_AVREG_0	E04
HT_CAD_TXN2	J18	HT_CLK_TXP0	J20	PCIE_AVREG_1	J08
HT_CAD_TXN3	F18	HT_CLK_TXP1	C17	PCIE_AVREG_2	G11
HT_CAD_TXN4	G19	HT_CTL_RXN0	J27	PCIE_HSIN0	G05
HT_CAD_TXN5	G21	HT_CTL_RXN1	D21	PCIE_HSIN1	G01
HT_CAD_TXN6	F21	HT_CTL_RXP0	K27	PCIE_HSIN2	C04
HT_CAD_TXN7	K21	HT_CTL_RXP1	E21	PCIE_HSIN3	C07
HT_CAD_TXN8	D19	HT_CTL_TXN0	J22	PCIE_HSIN4	E01
HT_CAD_TXN9	D17	HT_CTL_TXN1	D15	PCIE_HSIN5	J05
HT_CAD_TXN10	C19	HT_CTL_TXP0	J21	PCIE_HSIN6	H06
HT_CAD_TXN11	A15	HT_CTL_TXP1	E15	PCIE_HSIN7	E05
HT_CAD_TXN12	A17	$\overline{\text{HT\_LDTREQ\_L}}$	AF09	PCIE_HSIN8	D11
HT_CAD_TXN13	B19	$\overline{\text{HT\_LDTSTOP\_L}}$	AF06	PCIE_HSIN9	F12
HT_CAD_TXN14	C15	HT_PVTREF0	L17	PCIE_HSIN10	H09
HT_CAD_TXN15	C20	HT_PVTREF1	K17	PCIE_HSIN11	F09
HT_CAD_TXP0	F17	HT_PVTREF2	K19	PCIE_HSIN12	G13
HT_CAD_TXP1	H17	HT_PVTREF3	L19	PCIE_HSIN13	C13
HT_CAD_TXP2	J17	HT_PWROK	AF03	PCIE_HSIN14	D07
HT_CAD_TXP3	F19	HT_REFCLK_AGND	L15	PCIE_HSIN15	G07
HT_CAD_TXP4	H19	HT_REFCLK_AVDD	K15	PCIE_HSIP0	G04
HT_CAD_TXP5	H21	HT_REFCLK_AVDD2	H15	PCIE_HSIP1	G02
HT_CAD_TXP6	F20	HT_REFCLK_N	J16	PCIE_HSIP2	C05
HT_CAD_TXP7	L21	HT_REFCLK_P	J15	PCIE_HSIP3	C06
HT_CAD_TXP8	E19	$\overline{\text{HT\_RESET\_L}}$	AE11	PCIE_HSIP4	E02
HT_CAD_TXP9	E17	IRQ0	W11	PCIE_HSIP5	J04
HT_CAD_TXP10	C18	IRQ1	R11	PCIE_HSIP6	G06
HT_CAD_TXP11	B15	IRQ2	N11	PCIE_HSIP7	D05
HT_CAD_TXP12	B17	IRQ3	U11	PCIE_HSIP8	E11
HT_CAD_TXP13	A19	LSSD_RI	AG01	PCIE_HSIP9	F13
HT_CAD_TXP14	C14	NC	AF22	PCIE_HSIP10	G09
HT_CAD_TXP15	C21	NC	AJ22	PCIE_HSIP11	F08
HT_CLK_RXN0	E25	$\overline{\text{NORTH\_BRIDGE\_RESET\_L}}$	AL01	PCIE_HSIP12	H13
HT_CLK_RXN1	F22	OBSV	AG22	PCIE_HSIP13	C12
HT_CLK_RXP0	D25	PCIE_AV25_0	J06	PCIE_HSIP14	E07

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 8 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
PCIE_HSIP15	F07	PCIE_REFCLK_AVDDA	J12	PI0_ADI28	L01
PCIE_HSON0	D03	PCIE_REFCLK_AVDDB	K13	PI0_ADI29	L02
PCIE_HSON1	J01	PCIE_REFCLK_N	J10	PI0_ADI30	L03
PCIE_HSON2	C01	PCIE_REFCLK_P	J11	PI0_ADI31	L09
PCIE_HSON3	A07	PCIE_UCAL_RES0	F14	PI0_ADI32	K06
PCIE_HSON4	F03	PCIE_UCAL_RES1	J14	PI0_ADI33	K09
PCIE_HSON5	H03	PI_CSTP	AD09	PI0_ADI34	L10
PCIE_HSON6	A03	PI_REFCLK_N	AJ06	PI0_ADI35	L08
PCIE_HSON7	A05	PI_REFCLK_P	AJ07	PI0_ADI36	R07
PCIE_HSON8	C11	PI0_ADI0	R01	PI0_ADI37	R06
PCIE_HSON9	B11	PI0_ADI1	R02	PI0_ADI38	L06
PCIE_HSON10	F11	PI0_ADI2	T06	PI0_ADI39	M09
PCIE_HSON11	B09	PI0_ADI3	T03	PI0_ADI40	N10
PCIE_HSON12	D13	PI0_ADI4	U08	PI0_ADI41	N09
PCIE_HSON13	B13	PI0_ADI5	U07	PI0_ADI42	L07
PCIE_HSON14	D09	PI0_ADI6	R03	PI0_ADI43	K03
PCIE_HSON15	C08	PI0_ADI7	R04	PI0_ADO0	AE03
PCIE_HSOP0	E03	PI0_ADI8	R05	PI0_ADO1	AE04
PCIE_HSOP1	J02	PI0_ADI9	T09	PI0_ADO2	AE02
PCIE_HSOP2	C02	PI0_ADI10	R09	PI0_ADO3	AE01
PCIE_HSOP3	B07	PI0_ADI11	R10	PI0_ADO4	AD06
PCIE_HSOP4	G03	PI0_ADI12	P09	PI0_ADO5	AD03
PCIE_HSOP5	J03	PI0_ADI13	U10	PI0_ADO6	AE05
PCIE_HSOP6	B03	PI0_ADI14	P06	PI0_ADO7	AC04
PCIE_HSOP7	B05	PI0_ADI15	P03	PI0_ADO8	AC03
PCIE_HSOP8	C10	PI0_ADI16	N01	PI0_ADO9	AC05
PCIE_HSOP9	A11	PI0_ADI17	N02	PI0_ADO10	AC06
PCIE_HSOP10	F10	PI0_ADI18	N03	PI0_ADO11	AC07
PCIE_HSOP11	A09	PI0_ADI19	N04	PI0_ADO12	AC08
PCIE_HSOP12	E13	PI0_ADI20	R08	PI0_ADO13	AC02
PCIE_HSOP13	A13	PI0_ADI21	U06	PI0_ADO14	AA04
PCIE_HSOP14	E09	PI0_ADI22	M03	PI0_ADO15	AA05
PCIE_HSOP15	C09	PI0_ADI23	M06	PI0_ADO16	AB06
$\overline{\text{PCIE\_PRESENTN}}$	AJ02	PI0_ADI24	N08	PI0_ADO17	AA03
PCIE_REFCLK_AGNDA	J13	PI0_ADI25	N07	PI0_ADO18	AA02
PCIE_REFCLK_AGNDB	L13	PI0_ADI26	N06	PI0_ADO19	AA01
PCIE_REFCLK_AVDD2	J09	PI0_ADI27	N05	PI0_ADO20	AA08

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 9 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
PI0_ADO21	AE06	PI0_BCLKIP	L04	PI1_ADI25	AP07
PI0_ADO22	W06	PI0_BCLKON	AA07	PI1_ADI26	AT06
PI0_ADO23	W05	PI0_BCLKOP	AA06	PI1_ADI27	AR06
PI0_ADO24	W07	PI0_SE	AL07	PI1_ADI28	AP08
PI0_ADO25	W08	PI0_SRIN0	W10	PI1_ADI29	AT04
PI0_ADO26	Y03	PI0_SRIN1	U09	PI1_ADI30	AR04
PI0_ADO27	Y06	PI0_SRIP0	V09	PI1_ADI31	AP05
PI0_ADO28	W04	PI0_SRIP1	W09	PI1_ADI32	AM06
PI0_ADO29	W03	PI0_SRON0	AB03	PI1_ADI33	AN06
PI0_ADO30	W02	PI0_SRON1	AE07	PI1_ADI34	AP06
PI0_ADO31	AB09	PI0_SROP0	AC01	PI1_ADI35	AP04
PI0_ADO32	AC09	PI0_SROP1	AE08	PI1_ADI36	AM03
PI0_ADO33	AA10	PI1_ADI0	AM12	PI1_ADI37	AN01
PI0_ADO34	AA09	PI1_ADI1	AN12	PI1_ADI38	AL06
PI0_ADO35	Y09	PI1_ADI2	AL12	PI1_ADI39	AL05
PI0_ADO36	U02	PI1_ADI3	AK12	PI1_ADI40	AL04
PI0_ADO37	U01	PI1_ADI4	AP11	PI1_ADI41	AL03
PI0_ADO38	U03	PI1_ADI5	AL11	PI1_ADI42	AN02
PI0_ADO39	U04	PI1_ADI6	AP12	PI1_ADI43	AN03
PI0_ADO40	U05	PI1_ADI7	AR12	PI1_ADO0	AP20
PI0_ADO41	V06	PI1_ADI8	AT12	PI1_ADO1	AN20
PI0_ADO42	V03	PI1_ADI9	AH12	PI1_ADO2	AR20
PI0_ADO43	W01	PI1_ADI10	AG12	PI1_ADO3	AT20
PI_ISCA	AG03	PI1_ADI11	AH13	PI1_ADO4	AL19
PI_ISCL	AH03	PI1_ADI12	AJ12	PI1_ADO5	AP19
$\overline{\text{PI\_QACK0}}$	AH10	PI1_ADI13	AG14	PI1_ADO6	AM20
$\overline{\text{PI\_QACK1}}$	AF12	PI1_ADI14	AM10	PI1_ADO7	AM18
$\overline{\text{PI\_QACK2}}$	AF14	PI1_ADI15	AL10	PI1_ADO8	AL18
$\overline{\text{PI\_QACK3}}$	AC11	PI1_ADI16	AN10	PI1_ADO9	AN18
$\overline{\text{PI\_QREQ0}}$	AA11	PI1_ADI17	AP10	PI1_ADO10	AP18
$\overline{\text{PI\_QREQ1}}$	AF18	PI1_ADI18	AR10	PI1_ADO11	AR18
$\overline{\text{PI\_QREQ2}}$	AF16	PI1_ADI19	AT10	PI1_ADO12	AT18
$\overline{\text{PI\_QREQ3}}$	AF20	PI1_ADI20	AK10	PI1_ADO13	AK18
PI_REFCLK_AGND	AG10	PI1_ADI21	AJ10	PI1_ADO14	AP17
PI_REFCLK_AVDD	AG09	PI1_ADI22	AM08	PI1_ADO15	AL17
PI0_APSYNC	AC10	PI1_ADI23	AN08	PI1_ADO16	AH20
PI0_BCLKIN	L05	PI1_ADI24	AL08	PI1_ADO17	AJ20

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 10 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
PI1_ADO18	AK20	PI1_SRON1	AH18	#VDD	E06
PI1_ADO19	AH19	PI1_SROP0	AG18	#VDD	E10
PI1_ADO20	AG20	PI1_SROP1	AJ18	#VDD	E14
PI1_ADO21	AL20	PMR_CLK_N	AE10	#VDD	E22
PI1_ADO22	AM16	PMR_CLK_P	AE09	#VDD	E26
PI1_ADO23	AN16	PMR_CLK_STOP	AG02	#VDD	F02
PI1_ADO24	AL16	$\overline{\text{SUSPENDACK\_L}}$	AJ03	#VDD	F05
PI1_ADO25	AK16	$\overline{\text{SUSPENDREQ\_L}}$	AJ01	#VDD	G08
PI1_ADO26	AP15	SYS_ISCA0	AG04	#VDD	G12
PI1_ADO27	AL15	SYS_ISCA1	AH06	#VDD	G24
PI1_ADO28	AP16	SYS_ISCL0	AK03	#VDD	H01
PI1_ADO29	AM14	SYS_ISCL1	AJ05	#VDD	H04
PI1_ADO30	AL14	SYS_THDIO_D	F15	#VDD	H07
PI1_ADO31	AN14	SYS_THDIO_G	G15	#VDD	H10
PI1_ADO32	AP14	TDO	AG05	#VDD	H14
PI1_ADO33	AR14	#VDD	A04	#VDD	H26
PI1_ADO34	AT14	#VDD	A08	#VDD	K12
PI1_ADO35	AK14	#VDD	A12	#VDD	K24
PI1_ADO36	AP13	#VDD	A24	#VDD	L11
PI1_ADO37	AL13	#VDD	AA15	#VDD	L14
PI1_ADO38	AG16	#VDD	AA19	#VDD	L22
PI1_ADO39	AH15	#VDD	AA23	#VDD	M12
PI1_ADO40	AJ14	#VDD	AB17	#VDD	N15
PI1_ADO41	AH14	#VDD	AB21	#VDD	P17
PI1_ADO42	AH16	#VDD	AC14	#VDD	P21
PI1_ADO43	AH17	#VDD	AC18	#VDD	R14
PI1_APSYNC	AH11	#VDD	AC22	#VDD	R18
PI1_BCLKIN	AR08	#VDD	B06	#VDD	R22
PI1_BCLKIP	AT08	#VDD	B10	#VDD	T16
PI1_BCLKON	AR16	#VDD	B22	#VDD	T20
PI1_BCLKOP	AT16	#VDD	B26	#VDD	U15
PI1_SE	AK08	#VDD	C03	#VDD	U19
PI1_SRIN0	AL09	#VDD	D01	#VDD	V17
PI1_SRIN1	AP03	#VDD	D04	#VDD	V21
PI1_SRIP0	AP09	#VDD	D08	#VDD	W14
PI1_SRIP1	AR02	#VDD	D12	#VDD	W18
PI1_SRON0	AJ16	#VDD	D24	#VDD	W22

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 11 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
#VDD	Y16	#VD2	AG13	#VD2	K05
#VDD	Y20	#VD2	AG17	#VD2	K08
#VD2	P11	#VD2	AG21	#VD2	M01
#VD2	P13	#VD2	AH04	#VD2	M04
#VD2	T01	#VD2	AH07	#VD2	M07
#VD2	T04	#VD2	AH09	#VD2	M10
#VD2	T07	#VD2	AJ11	#VD2	P02
#VD2	T10	#VD2	AJ15	#VD2	P05
#VD2	T12	#VD2	AJ19	#VD2	P08
#VD2	V02	#VD2	AK02	#VD3	A28
#VD2	V05	#VD2	AK05	#VD3	A32
#VD2	V08	#VD2	AK09	#VD3	AA27
#VD2	V11	#VD2	AK13	#VD3	AA30
#VD2	V13	#VD2	AK17	#VD3	AA33
#VD2	Y01	#VD2	AK21	#VD3	AA36
#VD2	Y04	#VD2	AM01	#VD3	AB25
#VD2	Y07	#VD2	AM04	#VD3	AC26
#VD2	Y10	#VD2	AM11	#VD3	AC29
#VD2	Y12	#VD2	AM15	#VD3	AC32
#VD2	AB02	#VD2	AM19	#VD3	AC35
#VD2	AB05	#VD2	AN05	#VD3	AD24
#VD2	AB08	#VD2	AN09	#VD3	AE22
#VD2	AB11	#VD2	AN13	#VD3	AE27
#VD2	AB13	#VD2	AN17	#VD3	AE30
#VD2	AD01	#VD2	AN21	#VD3	AE33
#VD2	AD04	#VD2	AP02	#VD3	AE36
#VD2	AD07	#VD2	AR03	#VD3	AF23
#VD2	AD10	#VD2	AR07	#VD3	AF26
#VD2	AD12	#VD2	AR11	#VD3	AG25
#VD2	AD16	#VD2	AR15	#VD3	AG29
#VD2	AD20	#VD2	AR19	#VD3	AG32
#VD2	AE14	#VD2	AT05	#VD3	AG35
#VD2	AE18	#VD2	AT09	#VD3	AJ23
#VD2	AF08	#VD2	AT13	#VD3	AJ27
#VD2	AF11	#VD2	AT17	#VD3	AJ30
#VD2	AF15	#VD2	AT21	#VD3	AJ33
#VD2	AF19	#VD2	K02	#VD3	AJ36

Table 4-16. CPC945 Bridge and Memory Controller Pin List by Signal Name (Page 12 of 12)

Signal Name	Grid Location	Signal Name	Grid Location	Signal Name	Grid Location
#VD3	AK25	#VD3	M24	#VD4	M17
#VD3	AK29	#VD3	N23	#VD4	M21
#VD3	AL32	#VD3	N27	#VD4	N19
#VD3	AL35	#VD3	N30	#VD5	AF02
#VD3	AM23	#VD3	N33	#VD5	AF05
#VD3	AM27	#VD3	N36	#VD5	AH01
#VD3	AM31	#VD3	P25		
#VD3	AN25	#VD3	R26		
#VD3	AN29	#VD3	R29		
#VD3	AN33	#VD3	R32		
#VD3	AN36	#VD3	R35		
#VD3	AP34	#VD3	T24		
#VD3	AR23	#VD3	U23		
#VD3	AR27	#VD3	U27		
#VD3	AR31	#VD3	U30		
#VD3	AT25	#VD3	U33		
#VD3	AT29	#VD3	U36		
#VD3	AT33	#VD3	V25		
#VD3	B30	#VD3	W26		
#VD3	B34	#VD3	W29		
#VD3	C35	#VD3	W32		
#VD3	D28	#VD3	W35		
#VD3	D32	#VD3	Y24		
#VD3	E30	#VD4	A16		
#VD3	E33	#VD4	A20		
#VD3	E36	#VD4	B14		
#VD3	G28	#VD4	B18		
#VD3	G32	#VD4	D16		
#VD3	G35	#VD4	D20		
#VD3	J28	#VD4	E18		
#VD3	J30	#VD4	G16		
#VD3	J33	#VD4	G20		
#VD3	J36	#VD4	H18		
#VD3	L26	#VD4	H22		
#VD3	L29	#VD4	K16		
#VD3	L32	#VD4	K20		
#VD3	L35	#VD4	L18		

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 1 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
A01	depop	B01	depop	C01	PCIE_HSON2
A02	depop	B02	#GND	C02	PCIE_HSOP2
A03	PCIE_HSON6	B03	PCIE_HSOP6	C03	#VDD
A04	#VDD	B04	#GND	C04	PCIE_HSIN2
A05	PCIE_HSON7	B05	PCIE_HSOP7	C05	PCIE_HSIP2
A06	#GND	B06	#VDD	C06	PCIE_HSIP3
A07	PCIE_HSON3	B07	PCIE_HSOP3	C07	PCIE_HSIN3
A08	#VDD	B08	#GND	C08	PCIE_HSON15
A09	PCIE_HSOP11	B09	PCIE_HSON11	C09	PCIE_HSOP15
A10	#GND	B10	#VDD	C10	PCIE_HSOP8
A11	PCIE_HSOP9	B11	PCIE_HSON9	C11	PCIE_HSON8
A12	#VDD	B12	#GND	C12	PCIE_HSIP13
A13	PCIE_HSOP13	B13	PCIE_HSON13	C13	PCIE_HSIN13
A14	#GND	B14	#VD4	C14	HT_CAD_TXP14
A15	HT_CAD_TXN11	B15	HT_CAD_TXP11	C15	HT_CAD_TXN14
A16	#VD4	B16	#GND	C16	HT_CLK_TXN1
A17	HT_CAD_TXN12	B17	HT_CAD_TXP12	C17	HT_CLK_TXP1
A18	#GND	B18	#VD4	C18	HT_CAD_TXP10
A19	HT_CAD_TXP13	B19	HT_CAD_TXN13	C19	HT_CAD_TXN10
A20	#VD4	B20	#GND	C20	HT_CAD_TXN15
A21	HT_CAD_RXN14	B21	HT_CAD_RXP14	C21	HT_CAD_TXP15
A22	#GND	B22	#VDD	C22	HT_CAD_RXN11
A23	HT_CAD_RXN9	B23	HT_CAD_RXP9	C23	HT_CAD_RXP11
A24	#VDD	B24	#GND	C24	HT_CAD_RXN15
A25	HT_CAD_RXN2	B25	HT_CAD_RXP2	C25	HT_CAD_RXP15
A26	#GND	B26	#VDD	C26	HT_CAD_RXN7
A27	DDR_DQSN15	B27	DDR_DQSP15	C27	HT_CAD_RXP7
A28	#VD3	B28	#GND	C28	DDR_DQ127
A29	DDR_DQ126	B29	DDR_DQ125	C29	DDR_DQ124
A30	#GND	B30	#VD3	C30	DDR_DQ119
A31	DDR_DQSP14	B31	DDR_DQSN14	C31	DDR_DQ114
A32	#VD3	B32	#GND	C32	DDR_DQ118
A33	DDR_DQ116	B33	DDR_DQ117	C33	DDR_DQ106
A34	#GND	B34	#VD3	C34	DDR_DQ108
A35	depop	B35	DDR_DQ104	C35	#VD3
A36	depop	B36	depop	C36	#GND

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 2 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
D01	#VDD	E02	PCIE_HSIP4	F03	PCIE_HSON4
D02	#GND	E03	PCIE_HSOP0	F04	#GND
D03	PCIE_HSON0	E04	PCIE_AVREG_0	F05	#VDD
D04	#VDD	E05	PCIE_HSIN7	F06	#GND
D05	PCIE_HSIP7	E06	#VDD	F07	PCIE_HSIP15
D06	#GND	E07	PCIE_HSIP14	F08	PCIE_HSIP11
D07	PCIE_HSIN14	E08	#GND	F09	PCIE_HSIN11
D08	#VDD	E09	PCIE_HSOP14	F10	PCIE_HSOP10
D09	PCIE_HSON14	E10	#VDD	F11	PCIE_HSON10
D10	#GND	E11	PCIE_HSIP8	F12	PCIE_HSIN9
D11	PCIE_HSIN8	E12	#GND	F13	PCIE_HSIP9
D12	#VDD	E13	PCIE_HSOP12	F14	PCIE_UCAL_RES0
D13	PCIE_HSON12	E14	#VDD	F15	SYS_THDIO_D
D14	#GND	E15	HT_CTL_TXP1	F16	HT_CAD_TXN0
D15	HT_CTL_TXN1	E16	#GND	F17	HT_CAD_TXP0
D16	#VD4	E17	HT_CAD_TXP9	F18	HT_CAD_TXN3
D17	HT_CAD_TXN9	E18	#VD4	F19	HT_CAD_TXP3
D18	#GND	E19	HT_CAD_TXP8	F20	HT_CAD_TXP6
D19	HT_CAD_TXN8	E20	#GND	F21	HT_CAD_TXN6
D20	#VD4	E21	HT_CTL_RXP1	F22	HT_CLK_RXN1
D21	HT_CTL_RXN1	E22	#VDD	F23	HT_CLK_RXP1
D22	#GND	E23	HT_CAD_RXN8	F24	HT_CAD_RXP1
D23	HT_CAD_RXP8	E24	#GND	F25	HT_CAD_RXN1
D24	#VDD	E25	HT_CLK_RXN0	F26	HT_CAD_RXN0
D25	HT_CLK_RXP0	E26	#VDD	F27	HT_CAD_RXP0
D26	#GND	E27	DDR_CS15	F28	DDR_VREF_14_15
D27	DDR_DQ120	E28	#GND	F29	DDR_DQ121
D28	#VD3	E29	DDR_DQ122	F30	DDR_DQ115
D29	DDR_DQ123	E30	#VD3	F31	DDR_DQ105
D30	#GND	E31	DDR_DQ113	F32	DDR_DQSN13
D31	DDR_DQ112	E32	#GND	F33	DDR_DQSP13
D32	#VD3	E33	#VD3	F34	DDR_DQ107
D33	#GND	E34	DDR_DQ111	F35	DDR_DQ139
D34	DDR_DQ109	E35	#GND	F36	DDR_DQ136
D35	DDR_DQ110	E36	#VD3	G01	PCIE_HSIN1
D36	DDR_CS13	F01	#GND	G02	PCIE_HSIP1
E01	PCIE_HSIN4	F02	#VDD	G03	PCIE_HSOP4

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 3 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
G04	PCIE_HSIP0	H05	#GND	J06	PCIE_AV25_0
G05	PCIE_HSIN0	H06	PCIE_HSIN6	J07	PCIE_AV25_1
G06	PCIE_HSIP6	H07	#VDD	J08	PCIE_AVREG_1
G07	PCIE_HSIN15	H08	#GND	J09	PCIE_REFCLK_AVDD2
G08	#VDD	H09	PCIE_HSIN10	J10	PCIE_REFCLK_N
G09	PCIE_HSIP10	H10	#VDD	J11	PCIE_REFCLK_P
G10	#GND	H11	PCIE_AV25_2	J12	PCIE_REFCLK_AVDDA
G11	PCIE_AVREG_2	H12	#GND	J13	PCIE_REFCLK_AGNDA
G12	#VDD	H13	PCIE_HSIP12	J14	PCIE_UCAL_RES1
G13	PCIE_HSIN12	H14	#VDD	J15	HT_REFCLK_P
G14	#GND	H15	HT_REFCLK_AVDD2	J16	HT_REFCLK_N
G15	SYS_THDIO_G	H16	#GND	J17	HT_CAD_TXP2
G16	#VD4	H17	HT_CAD_TXP1	J18	HT_CAD_TXN2
G17	HT_CAD_TXN1	H18	#VD4	J19	HT_CLK_TXN0
G18	#GND	H19	HT_CAD_TXP4	J20	HT_CLK_TXP0
G19	HT_CAD_TXN4	H20	#GND	J21	HT_CTL_TXP0
G20	#VD4	H21	HT_CAD_TXP5	J22	HT_CTL_TXN0
G21	HT_CAD_TXN5	H22	#VD4	J23	HT_CAD_RXN13
G22	#GND	H23	HT_CAD_RXN10	J24	HT_CAD_RXP13
G23	HT_CAD_RXP10	H24	#GND	J25	HT_CAD_RXN6
G24	#VDD	H25	HT_CAD_RXP3	J26	HT_CAD_RXP6
G25	HT_CAD_RXN3	H26	#VDD	J27	HT_CTL_RXN0
G26	#GND	H27	HT_CAD_RXP5	J28	#VD3
G27	HT_CAD_RXN5	H28	#GND	J29	#GND
G28	#VD3	H29	#GND	J30	#VD3
G29	DDR_CS14	H30	DDR_DQ100	J31	DDR_DQ97
G30	#GND	H31	DDR_DQ102	J32	#GND
G31	DDR_DQ98	H32	DDR_DQSN12	J33	#VD3
G32	#VD3	H33	DDR_DQSP12	J34	DDR_DQ99
G33	#GND	H34	DDR_DQ103	J35	#GND
G34	DDR_DQ96	H35	DDR_CS12	J36	#VD3
G35	#VD3	H36	DDR_DQ101	K01	#GND
G36	#GND	J01	PCIE_HSON1	K02	#VD2
H01	#VDD	J02	PCIE_HSOP1	K03	PI0_ADI43
H02	#GND	J03	PCIE_HSOP5	K04	#GND
H03	PCIE_HSON5	J04	PCIE_HSIP5	K05	#VD2
H04	#VDD	J05	PCIE_HSIN5	K06	PI0_ADI32

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 4 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
K07	#GND	L08	PI0_ADI35	M09	PI0_ADI39
K08	#VD2	L09	PI0_ADI31	M10	#VD2
K09	PI0_ADI33	L10	PI0_ADI34	M11	#GND
K10	#GND	L11	#VDD	M12	#VDD
K11	depop	L12	#GND	M13	#GND
K12	#VDD	L13	PCIE_REFCLK_AGNDB	M14	depop
K13	PCIE_REFCLK_AVDDB	L14	#VDD	M15	depop
K14	#GND	L15	HT_REFCLK_AGND	M16	#GND
K15	HT_REFCLK_AVDD	L16	#GND	M17	#VD4
K16	#VD4	L17	HT_PVTREF0	M18	depop
K17	HT_PVTREF1	L18	#VD4	M19	depop
K18	#GND	L19	HT_PVTREF3	M20	#GND
K19	HT_PVTREF2	L20	#GND	M21	#VD4
K20	#VD4	L21	HT_CAD_TXP7	M22	depop
K21	HT_CAD_TXN7	L22	#VDD	M23	depop
K22	#GND	L23	HT_CAD_RXP12	M24	#VD3
K23	HT_CAD_RXN12	L24	#GND	M25	#GND
K24	#VDD	L25	HT_CAD_RXN4	M26	DDR_VREF_12_13
K25	HT_CAD_RXP4	L26	#VD3	M27	DDR_DQ88
K26	#GND	L27	#GND	M28	DDR_CS11
K27	HT_CTL_RXP0	L28	DDR_DQ141	M29	DDR_ODT7
K28	depop	L29	#VD3	M30	DDR_DQ140
K29	DDR_DQ142	L30	#GND	M31	DDR_DQ86
K30	DDR_DQ143	L31	DDR_DQ84	M32	DDR_CS10
K31	DDR_DQ137	L32	#VD3	M33	DDR_DQ87
K32	DDR_DQSP17	L33	#GND	M34	DDR_DQ81
K33	DDR_DQSN17	L34	DDR_DQ85	M35	DDR_DQSN10
K34	DDR_DQ138	L35	#VD3	M36	DDR_DQSP10
K35	DDR_DQ82	L36	#GND	N01	PI0_ADI16
K36	DDR_DQ80	M01	#VD2	N02	PI0_ADI17
L01	PI0_ADI28	M02	#GND	N03	PI0_ADI18
L02	PI0_ADI29	M03	PI0_ADI22	N04	PI0_ADI19
L03	PI0_ADI30	M04	#VD2	N05	PI0_ADI27
L04	PI0_BCLKIP	M05	#GND	N06	PI0_ADI26
L05	PI0_BCLKIN	M06	PI0_ADI23	N07	PI0_ADI25
L06	PI0_ADI38	M07	#VD2	N08	PI0_ADI24
L07	PI0_ADI42	M08	#GND	N09	PI0_ADI41

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 5 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
N10	PI0_ADI40	P11	#VD2	R12	depop
N11	IRQ2	P12	#GND	R13	depop
N12	depop	P13	#VD2	R14	#VDD
N13	depop	P14	depop	R15	#GND
N14	#GND	P15	depop	R16	depop
N15	#VDD	P16	#GND	R17	depop
N16	depop	P17	#VDD	R18	#VDD
N17	depop	P18	depop	R19	#GND
N18	#GND	P19	depop	R20	depop
N19	#VD4	P20	#GND	R21	depop
N20	depop	P21	#VDD	R22	#VDD
N21	depop	P22	depop	R23	#GND
N22	#GND	P23	depop	R24	depop
N23	#VD3	P24	#GND	R25	depop
N24	depop	P25	#VD3	R26	#VD3
N25	depop	P26	DDR_VREF_11_17	R27	#GND
N26	#GND	P27	DDR_DQSP11	R28	DDR_DQ89
N27	#VD3	P28	DDR_DQSN11	R29	#VD3
N28	DDR_DQ92	P29	DDR_DQ93	R30	#GND
N29	#GND	P30	DDR_DQ94	R31	DDR_DQ78
N30	#VD3	P31	DDR_DQ67	R32	#VD3
N31	DDR_DQ83	P32	DDR_DQ64	R33	#GND
N32	#GND	P33	DDR_DQ74	R34	DDR_CS9
N33	#VD3	P34	DDR_DQ72	R35	#VD3
N34	DDR_DQ95	P35	DDR_DQ76	R36	#GND
N35	#GND	P36	DDR_DQ77	T01	#VD2
N36	#VD3	R01	PI0_ADI0	T02	#GND
P01	#GND	R02	PI0_ADI1	T03	PI0_ADI3
P02	#VD2	R03	PI0_ADI6	T04	#VD2
P03	PI0_ADI15	R04	PI0_ADI7	T05	#GND
P04	#GND	R05	PI0_ADI8	T06	PI0_ADI2
P05	#VD2	R06	PI0_ADI37	T07	#VDD2
P06	PI0_ADI14	R07	PI0_ADI36	T08	#GND
P07	#GND	R08	PI0_ADI20	T09	PI0_ADI9
P08	#VD2	R09	PI0_ADI10	T10	#VD2
P09	PI0_ADI12	R10	PI0_ADI11	T11	#GND
P10	#GND	R11	IRQ1	T12	#VD2

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 6 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
T13	#GND	U14	#GND	V15	depop
T14	depop	U15	#VDD	V16	#GND
T15	depop	U16	depop	V17	#VDD
T16	#VDD	U17	depop	V18	depop
T17	#GND	U18	#GND	V19	depop
T18	depop	U19	#VDD	V20	#GND
T19	depop	U20	depop	V21	#VDD
T20	#VDD	U21	depop	V22	depop
T21	#GND	U22	#GND	V23	depop
T22	depop	U23	#VD3	V24	#GND
T23	depop	U24	depop	V25	#VD3
T24	#VD3	U25	depop	V26	DDR_VREF_7_8
T25	#GND	U26	#GND	V27	DDR_DQSN8
T26	DDR_VREF_9_10	U27	#VD3	V28	DDR_DQSP8
T27	DDR_DQ91	U28	DDR_DQ90	V29	DDR_CS8
T28	DDR_DQ70	U29	#GND	V30	DDR_DQ56
T29	DDR_DQ69	U30	#VD3	V31	DDR_DQ50
T30	DDR_DQ68	U31	DDR_DQ66	V32	DDR_DQ48
T31	DDR_DQ79	U32	#GND	V33	DDR_DQ52
T32	DDR_DQSN9	U33	#VD3	V34	DDR_DQ53
T33	DDR_DQSP9	U34	DDR_DQ59	V35	DDR_DQ54
T34	DDR_DQ73	U35	#GND	V36	DDR_CS6
T35	DDR_DQ75	U36	#VD3	W01	PI0_ADO43
T36	DDR_DQ65	V01	#GND	W02	PI0_ADO30
U01	PI0_ADO37	V02	#VD2	W03	PI0_ADO29
U02	PI0_ADO36	V03	PI0_ADO42	W04	PI0_ADO28
U03	PI0_ADO38	V04	#GND	W05	PI0_ADO23
U04	PI0_ADO39	V05	#VD2	W06	PI0_ADO22
U05	PI0_ADO40	V06	PI0_ADO41	W07	PI0_ADO24
U06	PI0_ADI21	V07	#GND	W08	PI0_ADO25
U07	PI0_ADI5	V08	#VD2	W09	PI0_SRIP1
U08	PI0_ADI4	V09	PI0_SRIP0	W10	PI0_SRIN0
U09	PI0_SRIN1	V10	#GND	W11	IRQ0
U10	PI0_ADI13	V11	#VD2	W12	depop
U11	IRQ3	V12	#GND	W13	depop
U12	depop	V13	#VD2	W14	#VDD
U13	depop	V14	depop	W15	#GND

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 7 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
W16	depop	Y17	#GND	AA18	#GND
W17	depop	Y18	depop	AA19	#VDD
W18	#VDD	Y19	depop	AA20	depop
W19	#GND	Y20	#VDD	AA21	depop
W20	depop	Y21	#GND	AA22	#GND
W21	depop	Y22	depop	AA23	#VDD
W22	#VDD	Y23	depop	AA24	depop
W23	#GND	Y24	#VD3	AA25	depop
W24	depop	Y25	#GND	AA26	#GND
W25	depop	Y26	DDR_VREF_5_6	AA27	#VD3
W26	#VD3	Y27	DDR_DQSP7	AA28	DDR_DQ63
W27	#GND	Y28	DDR_DQSN7	AA29	#GND
W28	DDR_DQ71	Y29	DDR_DQ55	AA30	#VD3
W29	#VD3	Y30	DDR_DQSN6	AA31	DDR_DQ42
W30	#GND	Y31	DDR_DQSP6	AA32	#GND
W31	DDR_CS7	Y32	DDR_DQ49	AA33	#VD3
W32	#VD3	Y33	DDR_DQ51	AA34	DDR_DQ135
W33	#GND	Y34	DDR_DQ57	AA35	#GND
W34	DDR_DQ62	Y35	DDR_DQ58	AA36	#VD3
W35	#VD3	Y36	DDR_DQ134	AB01	#GND
W36	#GND	AA01	PI0_ADO19	AB02	#VD2
Y01	#VD2	AA02	PI0_ADO18	AB03	PI0_SRON0
Y02	#GND	AA03	PI0_ADO17	AB04	#GND
Y03	PI0_ADO26	AA04	PI0_ADO14	AB05	#VD2
Y04	#VD2	AA05	PI0_ADO15	AB06	PI0_ADO16
Y05	#GND	AA06	PI0_BCLKOP	AB07	#GND
Y06	PI0_ADO27	AA07	PI0_BCLKON	AB08	#VD2
Y07	#VD2	AA08	PI0_ADO20	AB09	PI0_ADO31
Y08	#GND	AA09	PI0_ADO34	AB10	#GND
Y09	PI0_ADO35	AA10	PI0_ADO33	AB11	#VD2
Y10	#VD2	AA11	$\overline{\text{PI\_QREQ0}}$	AB12	#GND
Y11	#GND	AA12	depop	AB13	#VD2
Y12	#VD2	AA13	depop	AB14	depop
Y13	#GND	AA14	#GND	AB15	depop
Y14	depop	AA15	#VDD	AB16	#GND
Y15	depop	AA16	depop	AB17	#VDD
Y16	#VDD	AA17	depop	AB18	depop

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 8 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
AB19	depop	AC20	depop	AD21	#GND
AB20	#GND	AC21	depop	AD22	depop
AB21	#VDD	AC22	#VDD	AD23	depop
AB22	depop	AC23	#GND	AD24	#VD3
AB23	depop	AC24	depop	AD25	#GND
AB24	#GND	AC25	depop	AD26	DDR_VREF_2_3
AB25	#VD3	AC26	#VD3	AD27	DDR_DQSP16
AB26	DDR_VREF_4_16	AC27	#GND	AD28	DDR_DQSN16
AB27	DDR_DQ61	AC28	DDR_DQ129	AD29	DDR_DQ132
AB28	DDR_DQ60	AC29	#VD3	AD30	DDR_DQ133
AB29	DDR_DQ128	AC30	#GND	AD31	DDR_DQ34
AB30	DDR_DQSP5	AC31	DDR_DQ47	AD32	DDR_DQSN4
AB31	DDR_DQSN5	AC32	#VD3	AD33	DDR_DQSP4
AB32	DDR_CS5	AC33	#GND	AD34	DDR_DQ36
AB33	DDR_DQ46	AC34	DDR_DQ41	AD35	DDR_DQ37
AB34	DDR_DQ45	AC35	#VD3	AD36	DDR_DQ43
AB35	DDR_DQ44	AC36	#GND	AE01	PI0_ADO3
AB36	DDR_DQ40	AD01	#VD2	AE02	PI0_ADO2
AC01	PI0_SROP0	AD02	#GND	AE03	PI0_ADO0
AC02	PI0_ADO13	AD03	PI0_ADO5	AE04	PI0_ADO1
AC03	PI0_ADO8	AD04	#VD2	AE05	PI0_ADO6
AC04	PI0_ADO7	AD05	#GND	AE06	PI0_ADO21
AC05	PI0_ADO9	AD06	PI0_ADO4	AE07	PI0_SRON1
AC06	PI0_ADO10	AD07	#VD2	AE08	PI0_SROP1
AC07	PI0_ADO11	AD08	#GND	AE09	PMR_CLK_P
AC08	PI0_ADO12	AD09	PI_CSTP	AE10	PMR_CLK_N
AC09	PI0_ADO32	AD10	#VD2	AE11	$\overline{\text{HT\_RESET\_L}}$
AC10	PI0_APSYNC	AD11	#GND	AE12	depop
AC11	$\overline{\text{PI\_QACK3}}$	AD12	#VD2	AE13	depop
AC12	depop	AD13	#GND	AE14	#VD2
AC13	depop	AD14	depop	AE15	#GND
AC14	#VDD	AD15	depop	AE16	depop
AC15	#GND	AD16	#VD2	AE17	depop
AC16	depop	AD17	#GND	AE18	#VD2
AC17	depop	AD18	depop	AE19	#GND
AC18	#VDD	AD19	depop	AE20	depop
AC19	#GND	AD20	#VD2	AE21	depop

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 9 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
AE22	#VD3	AF23	#VD3	AG24	DDR_REFCLK_N
AE23	#GND	AF24	DDR_REFCLK_P	AG25	#VD3
AE24	depop	AF25	#GND	AG26	DDR_VREF_0_1
AE25	depop	AF26	#VD3	AG27	#GND
AE26	#GND	AF27	DDR_DQ130	AG28	DDR_DQ35
AE27	#VD3	AF28	DDR_ODT6	AG29	#VD3
AE28	DDR_DQ131	AF29	DDR_DQ32	AG30	#GND
AE29	#GND	AF30	DDR_DQ33	AG31	DDR_DQ31
AE30	#VD3	AF31	DDR_CS3	AG32	#VD3
AE31	DDR_DQ24	AF32	DDR_DQSN3	AG33	#GND
AE32	#GND	AF33	DDR_DQSP3	AG34	DDR_DQ25
AE33	#VD3	AF34	DDR_DQ30	AG35	#VD3
AE34	DDR_DQ26	AF35	DDR_DQ29	AG36	#GND
AE35	#GND	AF36	DDR_DQ28	AH01	#VD5
AE36	#VD3	AG01	LSSD_RI	AH02	#GND
AF01	#GND	AG02	PMR_CLK_STOP	AH03	PI_ISCL
AF02	#VD5	AG03	PI_ISCA	AH04	#VD2
AF03	HT_PWROK	AG04	SYS_ISCA0	AH05	#GND
AF04	#GND	AG05	TDO	AH06	SYS_ISCA1
AF05	#VD5	AG06	depop	AH07	#VD2
AF06	$\overline{\text{HT\_LDTSTOP\_L}}$	AG07	CE1_MC_TDI	AH08	#GND
AF07	#GND	AG08	CE0_TEST	AH09	#VD2
AF08	#VD2	AG09	PI_REFCLK_AVDD	AH10	$\overline{\text{PI\_QACK0}}$
AF09	$\overline{\text{HT\_LDTREQ\_L}}$	AG10	PI_REFCLK_AGND	AH11	PI1_APSYNC
AF10	#GND	AG11	#GND	AH12	PI1_ADI9
AF11	#VD2	AG12	PI1_ADI10	AH13	PI1_ADI11
AF12	$\overline{\text{PI\_QACK1}}$	AG13	#VD2	AH14	PI1_ADO41
AF13	#GND	AG14	PI1_ADI13	AH15	PI1_ADO39
AF14	$\overline{\text{PI\_QACK2}}$	AG15	#GND	AH16	PI1_ADO42
AF15	#VD2	AG16	PI1_ADO38	AH17	PI1_ADO43
AF16	$\overline{\text{PI\_QREQ2}}$	AG17	#VD2	AH18	PI1_SRON1
AF17	#GND	AG18	PI1_SROP0	AH19	PI1_ADO19
AF18	$\overline{\text{PI\_QREQ1}}$	AG19	#GND	AH20	PI1_ADO16
AF19	#VD2	AG20	PI1_ADO20	AH21	DDR_REFCLK_AGND
AF20	$\overline{\text{PI\_QREQ3}}$	AG21	#VD2	AH22	$\overline{\text{CHP\_FAULT\_N}}$
AF21	#GND	AG22	OBSV	AH23	DDR_REFCLK_AVDD
AF22	NC	AG23	#GND	AH24	DDR_CKE1

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 10 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
AH25	DDR_MAD13	AJ26	DDR_MAD14	AK27	#GND
AH26	DDR_MAD12	AJ27	#VD3	AK28	DDR_MUXEN3
AH27	DDR_MAD11	AJ28	DDR_MAD10	AK29	#VD3
AH28	DDR_MAD7	AJ29	#GND	AK30	DDR_MUXEN4
AH29	DDR_DQ21	AJ30	#VD3	AK31	DDR_DQ9
AH30	DDR_DQ20	AJ31	DDR_CS2	AK32	DDR_DQ23
AH31	DDR_DQ16	AJ32	#GND	AK33	DDR_DQ19
AH32	DDR_DQ18	AJ33	#VD3	AK34	DDR_DQ17
AH33	DDR_CS4	AJ34	DDR_DQ22	AK35	DDR_DQSP2
AH34	DDR_DQ39	AJ35	#GND	AK36	DDR_DQSN2
AH35	DDR_DQ38	AJ36	#VD3	AL01	$\overline{\text{NORTH\_BRIDGE\_RESET\_L}}$
AH36	DDR_DQ27	AK01	#GND	AL02	CE1_DI1_TMS
AJ01	$\overline{\text{SUSPENDREQ\_L}}$	AK02	#VD2	AL03	PI1_ADI41
AJ02	$\overline{\text{PCIE\_PRESENTN}}$	AK03	SYS_ISCL0	AL04	PI1_ADI40
AJ03	$\overline{\text{SUSPENDACK\_L}}$	AK04	#GND	AL05	PI1_ADI39
AJ04	CE1_LT_TCK	AK05	#VD2	AL06	PI1_ADI38
AJ05	SYS_ISCL1	AK06	CE1_DI2_TRST	AL07	PI0_SE
AJ06	PI_REFCLK_N	AK07	#GND	AL08	PI1_ADI24
AJ07	PI_REFCLK_P	AK08	PI1_SE	AL09	PI1_SRIN0
AJ08	#GND	AK09	#VD2	AL10	PI1_ADI15
AJ09	#GND	AK10	PI1_ADI20	AL11	PI1_ADI5
AJ10	PI1_ADI21	AK11	#GND	AL12	PI1_ADI2
AJ11	#VD2	AK12	PI1_ADI3	AL13	PI1_ADO37
AJ12	PI1_ADI12	AK13	#VD2	AL14	PI1_ADO30
AJ13	#GND	AK14	PI1_ADO35	AL15	PI1_ADO27
AJ14	PI1_ADO40	AK15	#GND	AL16	PI1_ADO24
AJ15	#VD2	AK16	PI1_ADO25	AL17	PI1_ADO15
AJ16	PI1_SRON0	AK17	#VD2	AL18	PI1_ADO8
AJ17	#GND	AK18	PI1_ADO13	AL19	PI1_ADO4
AJ18	PI1_SROP1	AK19	#GND	AL20	PI1_ADO21
AJ19	#VD2	AK20	PI1_ADO18	AL21	DDR_CKE2
AJ20	PI1_ADO17	AK21	#VD2	AL22	DDR_BA0
AJ21	#GND	AK22	DDR_ODT5	AL23	DDR_ODT0
AJ22	NC	AK23	#GND	AL24	DDR_RAS
AJ23	#VD3	AK24	DDR_MAD15	AL25	DDR_MAD5
AJ24	DDR_CKE0	AK25	#VD3	AL26	DDR_CK_B
AJ25	#GND	AK26	DDR_CK_BN	AL27	DDR_CS0

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 11 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
AL28	DDR_MUXEN2	AM29	#GND	AN30	DDR_DQ4
AL29	DDR_MUXEN6	AM30	DDR_DQ3	AN31	#GND
AL30	DDR_MAD8	AM31	#VD3	AN32	DDR_DQ2
AL31	#GND	AM32	DDR_DQ7	AN33	#VD3
AL32	#VD3	AM33	DDR_DQ14	AN34	DDR_DQ13
AL33	#GND	AM34	DDR_DQ15	AN35	#GND
AL34	DDR_DQ10	AM35	depop	AN36	#VD3
AL35	#VD3	AM36	DDR_DQ8	AP01	#GND
AL36	#GND	AN01	PI1_ADI37	AP02	#VD2
AM01	#VD2	AN02	PI1_ADI42	AP03	PI1_SRIN1
AM02	#GND	AN03	PI1_ADI43	AP04	PI1_ADI35
AM03	PI1_ADI36	AN04	#GND	AP05	PI1_ADI31
AM04	#VD2	AN05	#VD2	AP06	PI1_ADI34
AM05	#GND	AN06	PI1_ADI33	AP07	PI1_ADI25
AM06	PI1_ADI32	AN07	#GND	AP08	PI1_ADI28
AM07	#VD2	AN08	PI1_ADI23	AP09	PI1_SRIP0
AM08	PI1_ADI22	AN09	#VD2	AP10	PI1_ADI17
AM09	#GND	AN10	PI1_ADI16	AP11	PI1_ADI4
AM10	PI1_ADI14	AN11	#GND	AP12	PI1_ADI6
AM11	#VD2	AN12	PI1_ADI1	AP13	PI1_ADO36
AM12	PI1_ADI0	AN13	#VD2	AP14	PI1_ADO32
AM13	#GND	AN14	PI1_ADO31	AP15	PI1_ADO26
AM14	PI1_ADO29	AN15	#GND	AP16	PI1_ADO28
AM15	#VD2	AN16	PI1_ADO23	AP17	PI1_ADO14
AM16	PI1_ADO22	AN17	#VD2	AP18	PI1_ADO10
AM17	#GND	AN18	PI1_ADO9	AP19	PI1_ADO5
AM18	PI1_ADO7	AN19	#GND	AP20	PI1_ADO0
AM19	#VD2	AN20	PI1_ADO1	AP21	DDR_CKE3
AM20	PI1_ADO6	AN21	#VD2	AP22	DDR_CKE5
AM21	#GND	AN22	DDR_CKE6	AP23	DDR_WE
AM22	DDR_CKE7	AN23	#GND	AP24	DDR_ODT4
AM23	#VD3	AN24	DDR_ODT3	AP25	DDR_MAD6
AM24	DDR_CAS	AN25	#VD3	AP26	DDR_MAD1
AM25	#GND	AN26	DDR_MAD0	AP27	DDR_MUXEN0
AM26	DDR_MAD4	AN27	#GND	AP28	DDR_BA1
AM27	#VD3	AN28	DDR_BA2	AP29	DDR_MUXEN7
AM28	DDR_MUXEN1	AN29	#VD3	AP30	DDR_DQ5

Table 4-17. CPC945 Bridge and Memory Controller Pin List by Grid Position (Page 12 of 12)

Grid Position	Signal Name	Grid Position	Signal Name	Grid Position	Signal Name
AP31	DDR_DQ0	AR30	DDR_DQ6	AT29	#VD3
AP32	DDR_DQ1	AR31	#VD3	AT30	DDR_MUXEN5
AP33	DDR_CS1	AR32	DDR_DQSP0	AT31	#GND
AP34	#VD3	AR33	#GND	AT32	DDR_DQSN0
AP35	DDR_DQSP1	AR34	DDR_DQ12	AT33	#VD3
AP36	DDR_DQSN1	AR35	#GND	AT34	DDR_DQ11
AR01	depop	AR36	depop	AT35	depop
AR02	PI1_SRIP1	AT01	depop	AT36	depop
AR03	#VD2	AT02	depop		
AR04	PI1_ADI30	AT03	#GND		
AR05	#GND	AT04	PI1_ADI29		
AR06	PI1_ADI27	AT05	#VD2		
AR07	#VD2	AT06	PI1_ADI26		
AR08	PI1_BCLKIN	AT07	#GND		
AR09	#GND	AT08	PI1_BCLKIP		
AR10	PI1_ADI18	AT09	#VD2		
AR11	#VD2	AT10	PI1_ADI19		
AR12	PI1_ADI7	AT11	#GND		
AR13	#GND	AT12	PI1_ADI8		
AR14	PI1_ADO33	AT13	#VD2		
AR15	#VD2	AT14	PI1_ADO34		
AR16	PI1_BCLKON	AT15	#GND		
AR17	#GND	AT16	PI1_BCLKOP		
AR18	PI1_ADO11	AT17	#VD2		
AR19	#VD2	AT18	PI1_ADO12		
AR20	PI1_ADO2	AT19	#GND		
AR21	#GND	AT20	PI1_ADO3		
AR22	DDR_MAD9	AT21	#VD2		
AR23	#VD3	AT22	DDR_CKE4		
AR24	DDR_ODT2	AT23	#GND		
AR25	#GND	AT24	DDR_ODT1		
AR26	DDR_MAD2	AT25	#VD3		
AR27	#VD3	AT26	DDR_MAD3		
AR28	DDR_CK_A	AT27	#GND		
AR29	#GND	AT28	DDR_CK_AN		

Revision Log

Revision Date	Contents of Modification
August 15, 2006	Revision A15-6009-01. VDD2 operational voltage range changed to 1.3 V-1.5 V range. VDD2 minimum voltage changed from 1.1 V to 1.25 V.