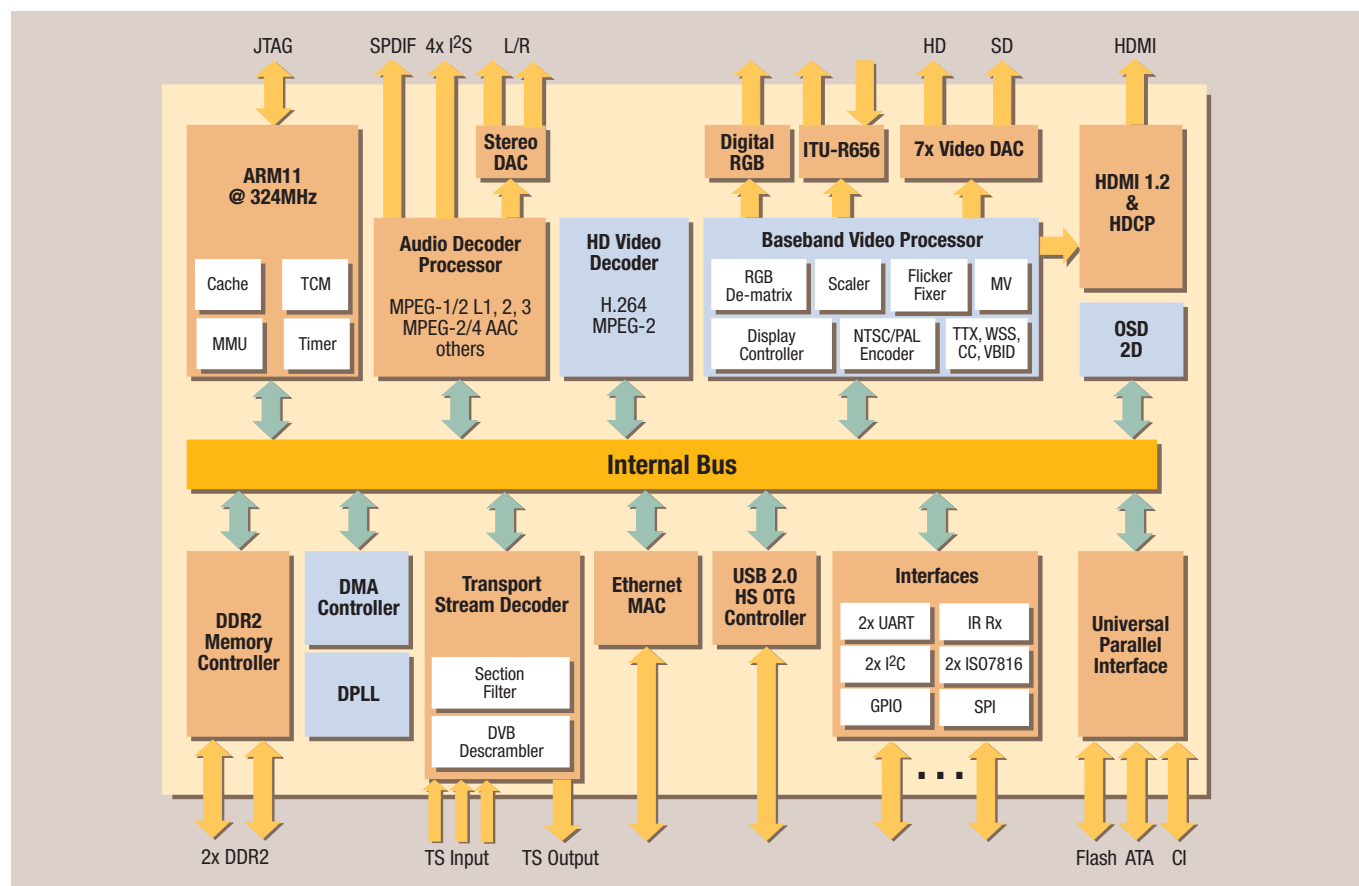


## HD MULTI-STANDARD DECODER

Highly integrated SoC for HDTV receivers



MB86H60 block diagram.

### Description

The MB86H60 is a highly integrated System-on-Chip incorporating all the processing functions required by digital HDTV receivers, including those for digital video, audio and graphics - ideal for IDTV sets and set-top boxes.

The MB86H60 incorporates the high performance ARM processor 1176JZF-S™ featuring an integrated memory management unit (MMU), a floating point co-processor, ARM's Jazelle® technology and Thumb® instruction set extensions for compact code. The ARM11 provides all the processing power needed to enable a whole host of middleware software. Just two 16-bit DDR2 memories are required for operation.

This cost effective, low power, high definition media processor is able to decode both MPEG-2 and H.264/AVC compressed video up to HD resolution (1920 x 1080i). HD video can be provided either via the copy-protected HDMI output or analogue component outputs. Simultaneously the video signal can be scaled down and offered in standard definition (SD) resolution. The picture quality on these SD component outputs may be optimised by using cross-colour and cross-luminance filters. A digital RGB output and an ITU-R 656 input and output are also available.

The integrated audio processor can decode a wide variety of audio standards required by the broadcast market such as MPEG-1/2 Layer 1, 2, 3 and MPEG-2/4 AAC. Furthermore, support for Dolby™ Digital (AC-3) and Dolby™ Digital Plus is planned. Available audio outputs are four I<sup>2</sup>S, SPDIF and stereo analogue outputs.

## FACTSHEET

### MB86H60

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Advanced connectivity is provided by a USB 2.0 high speed On-The-Go (OTG) controller, a 10/100 Base-T Ethernet MAC and a DMA ATA controller. Integrated peripherals include two serial ports, two ISO7816 smart card interfaces, two I<sup>2</sup>C controllers, LED and keypad controller, IR receiver, SPI output, PWM output and 96 GPIO pins. The number of usable GPIOs depends on the system configuration since they are shared among other IO functions.

#### Features

- ARM1176JZF-S™ @ 324MHz with 16K-I/16K-D cache, 16K-I/16K-D TCM, FPU, MMU
- Bootable from NOR or serial flash
- 2x16-bit DDR2 SDRAM interface @ 324MHz
- HD video decoder supporting H.264/AVC Level 4.0 high profile and MPEG-2 HD/SD MP@HL
- Programmable audio processor, audio firmware available or planned for MPEG-1/2 Layer 1, 2 and 3 (MP3), MPEG-2/4 AAC and MPEG-4 HE-AAC, Dolby™ Digital and Dolby™ Digital Plus
- USB 2.0 high speed OTG controller
- Ethernet 10/100 Base-T MAC
- Hardware acceleration unit (DMA): DMA ATA (16MByte/s), TDES, memory copy, etc.
- Universal processor interface supporting NOR flash, common interface and ATA
- 4x transport stream decoder and DVB descrambler (3x external input, 1x output)
- Display controller supporting 5 layers: Video, 2x OSD (YCrCb or RGB), cursor, background
- Teletext, WSS, CC, VBI insertion
- Cross colour and luminance filters
- PAL/NTSC/SECAM digital encoder
- HDMI 1.2 Link and PHY with HDCP
- 3x DAC for analogue HD video output (YPrPb)
- 4x DAC for analogue SD video output
- Digital RGB888 output (HD) and ITU-R 656 I/O (SD)
- 4x I<sup>2</sup>S, SPDIF output, stereo audio DAC
- 2x UART, 2x ISO7816 smart card, 2x I<sup>2</sup>C, PWM, IR RX, SPI
- 96 GPIO (flexible pin assignment, shared with other I/O functions)
- 5 digit 7-segment LED display and keypad controller
- Internal clock recovery (no external VCXO required)
- PBGA 484 package, 27mm x 27mm
- Fujitsu CMOS 90nm technology
- Operating temperature range: 0 to +70°C

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