ZLAN-36

Application of the CESoP Processors MAC-to-MAC Connections

Application Note

Contents

September 2006

1.0 CESoP Processors

Zarlink Semiconductor has three families of Circuit Emulation Service over Packet (CESoP) processors - the ZL50110/11/14 family, the ZL50115/16/17/18/19/20 family and the MT90880/1/2/3 family. These devices have single, dual or triple Fast Ethernet ports and/or single or dual Gigabit Ethernet ports that perform the MAC layer function. The CESoP device would typically interface to off-the-shelf PHYs connecting to a 10/100/1000 Mbit/s Ethernet network. However, any of the MAC interfaces on the CESoP devices may be connected directly to another MAC interface. The ability to connect two MACs directly together would eliminate the need for a PHY. This application note will detail the MAC-to-MAC interface as it applies to the CESoP processors. ZL5011x refers to all ZL50110/11/14/15/16/17/18/19/20 devices.

2.0 MAC-to-MAC Applications

As an example application, a CESoP processor would be configured for MAC-to-MAC operation when there are multiple CESoP application devices connected to a single Ethernet switch. Figure 1, “Gigabit Ethernet Connection - Central Ethernet Switch”, on page 1 shows four ZL5011x devices connected to a Gigabit Ethernet switch, such as the Zarlink MVTX2804 Managed 8-Port 1000 Mbps Ethernet Switch. The four ZL5011x devices have their traffic aggregated inside the Ethernet switch and the traffic is sent out to the Ethernet Network.

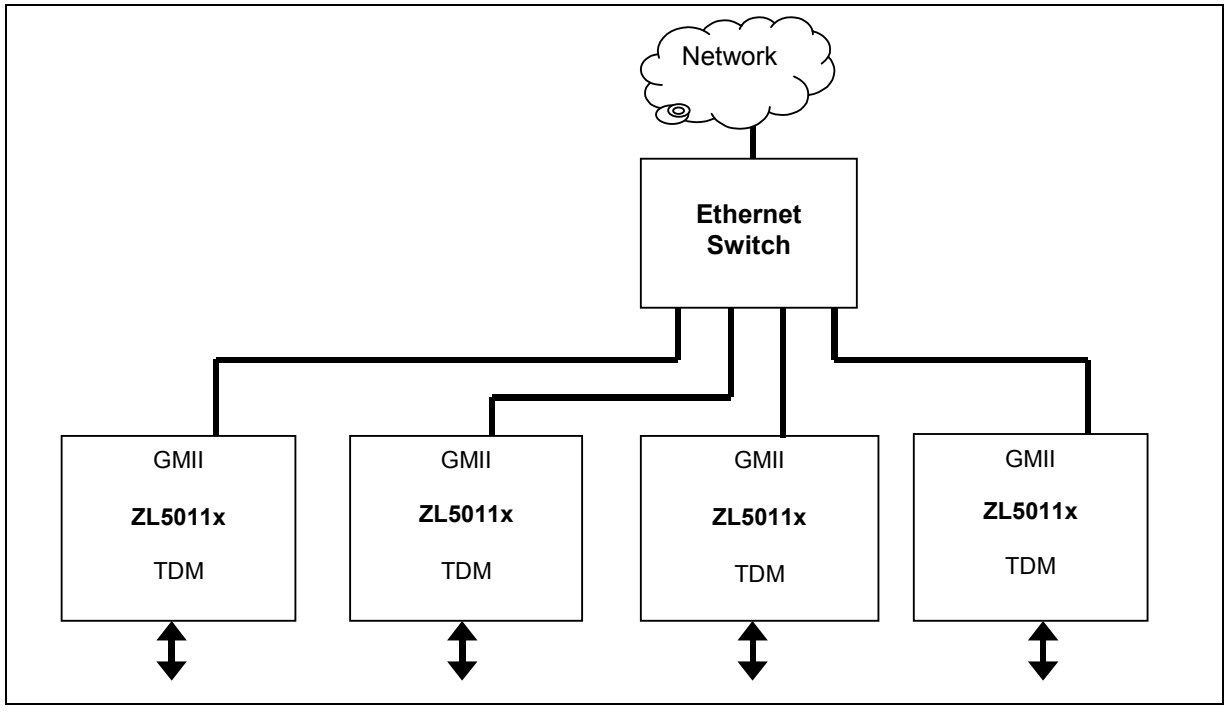

Figure 1 - Gigabit Ethernet Connection - Central Ethernet Switch

3.0 CESoP Families

The MT90880, MT90881, MT90882 and MT90883 form the MT90880/1/2/3 family of CESoP processors. These devices have dual Fast Ethernet ports. Each port is capable of operation in either MII or RMII mode at speeds of 10 Mbit/s or 100 Mbit/s. The ZL50110, ZL50111 and ZL50114 form the ZL50110/11/14 family of CESoP processors. These devices have dual or triple Fast Ethernet ports or dual redundant Gigabit Ethernet ports. The ZL50115, ZL50116, ZL50117, ZL50118, ZL50119 and ZL50120 form the ZL50115/16/17/18/19/20 family of CESoP processors. The ZL50115/16/17 have a single Gigabit Ethernet port. The ZL50118/19/20 have a single Fast Ethernet port and a single Gigabit Ethernet port. For both the ZL50110/11/14 and ZL50115/16/17/18/19/20, the Fast Ethernet ports are capable of operation in MII mode at 100 Mbit/s speed. The Gigabit Ethernet ports are capable of operation in GMII or PCS mode at 1000 Mbit/s speed. Table 1 shows a summary of the various CESoP processors and their MAC interfaces.

Port Interface	Port Speed	MT90880/1/2/3 Family	ZL50110, ZL50114	ZL50111	ZL50118, ZL50119, ZL50120	ZL50115, ZL50116, ZL50117
RMII	10 Mbit/s	√	-	-	-	-
RMII	100 Mbit/s	√	-	-	-	-
MII	10 Mbit/s	√	-	-	-	-
MII	100 Mbit/s	√	√	√	√	√
GMII	1000 Mbit/s	-	√	√	√	√
PCS	1000 Mbit/s	-	√	√	√	√

Table 1 - CESoP Processor MAC Interface Support

4.0 Interface Overview

4.1 RMII Interface

The RMII interface consists of a 2-bit wide data path on both receive and transmit sides. From the MAC point of view, only transmit data (TXD[1:0]) and transmit enable (TXEN) are outputs, the rest of the signals are inputs. This interface is meant to operate at 10 Mbit/s or 100 Mbit/s. The RMII MAC-to-MAC connection should be configured for full duplex mode operation.

RMII Signal Name	MAC Signal Direction	Description
TXD[1:0]	O	Transmit Data Bits [3:0] (driven on rising edge of TXCLK)
TXEN	O	Transmit Data Enable (indicated valid TXD[3:0])
RXD[1:0]	I	Receive Data Bit [3:0] (driven on rising edge of RXCLK)
CRS_DV	I	Carrier Sense and Receive Data Valid (indicated valid RXD[1:0] and/or tx/rx activity)
M_CLK	I	Reference Clock (50 MHz)

Table 2 - RMII Interface Description

4.2 MII Interface

The MII interface consists of a 4-bit wide data path on both receive and transmit sides. From the MAC point of view, only transmit data (TXD[3:0]) and transmit enable (TXEN) are outputs, the rest of the signals are inputs. This interface is meant to operate at 10 Mbit/s or 100 Mbit/s. The MII MAC-to-MAC connection should be configured for full duplex mode operation. For this reason, both CRS and COL are not needed for the MII MAC-to-MAC connection.

MII Signal Name	MAC Signal Direction	Description
TXD[3:0]	O	Transmit Data Bits [3:0] (driven on rising edge of TXCLK)
TXEN	O	Transmit Data Enable (indicated valid TXD[3:0])
TXCLK	I	Transmit Clock (2.5/25 MHz)
RXD[3:0]	I	Receive Data Bit [3:0] (driven on rising edge of RXCLK)
RXDV	I	Receive Data Valid (indicated valid RXD[3:0])
RXCLK	I	Receive Clock (2.5/25 MHz)
CRS	I	Carrier Sense (active during tx/rx activity)
COL	I	Collision Detected (asserted when collision detected in tx/rx path)

Table 3 - MII Interface Description

4.3 GMII Interface

The GMII interface consists of a 8-bit wide data path on both receive and transmit sides. From the MAC point of view, transmit data (TXD[7:0]), transmit enable (TXEN), transmit clock (TXCLK) and transmit error (TXER) are outputs, the rest of the signals are inputs. This interface is meant to operate at 1000 Mbit/s (1 Gbit/s). The GMII MAC-to-MAC connection should be configured as 1000 Mbit/s, full duplex mode operation. For this reason, both CRS and COL are not needed for the GMII MAC-to-MAC connection.

GMII Signal Name	MAC Signal Direction	Description
TXD[7:0]	O	Transmit Data Bits [3:0] (driven on rising edge of TXCLK)
TXEN	O	Transmit Data Enable (indicated valid TXD[7:0])
TXER	O	Transmit error (indicated error during transmission)
TXCLK	O	Transmit Clock (125 MHz)
RXD[7:0]	I	Receive Data Bit [3:0] (driven on rising edge of RXCLK)
RXDV	I	Receive Data Valid (indicated valid RXD[7:0])
RXER	I	Receive error (indicated error during reception)
RXCLK	I	Receive Clock (125 MHz)
CRS	I	Carrier Sense (active during tx/rx activity)
COL	I	Collision Detected (asserted when collision detected in tx/rx path)

Table 4 - GMII Interface Description

5.0 Interface Connections

5.1 RMII Ports

This section describes the MAC-to-MAC connection for the Fast Ethernet ports on the MT90880/1/2/3 when operating in RMII mode at either 10 Mbit/s or 100 Mbit/s. Table 5, “MT90880/1/2/3 RMII Interface Connection” on page 6 details the connection between MT90880/1/2/3 port 0 and a Generic RMII MAC as well as the Zarlink ZL50408 Managed 8-Port 10/100 M + 1 G Ethernet switch. Figure 2, “MT90880/1/2/3 RMII Interface Connection”, on page 6 shows the MAC-to-MAC connection between the MT90880/1/2/3 and a Generic RMII MAC interface.

MT90880/1/2/3 Pin Name	MT90880/1/2/3 Pin Number	RMII MAC Connection	ZL50408 RMII MAC Connection	Notes
ref_clk	AB11	REF_CLK	M_CLK	Connect to 50 MHz clock
m0_txd[1:0]	AE6 [1], AD7 [0]	RXD[3:0]	Mn_RXD[1:0]	
m0_txen	AD6	RXDV	Mn_CRS_DV	
m0_rxd[1:0]	AE9 [1], AD9 [0]	TXD[3:0]	Mn_TXD[1:0]	
m0_rxdv	AF7	TXEN	Mn_TXEN	

Table 5 - MT90880/1/2/3 RMII Interface Connection

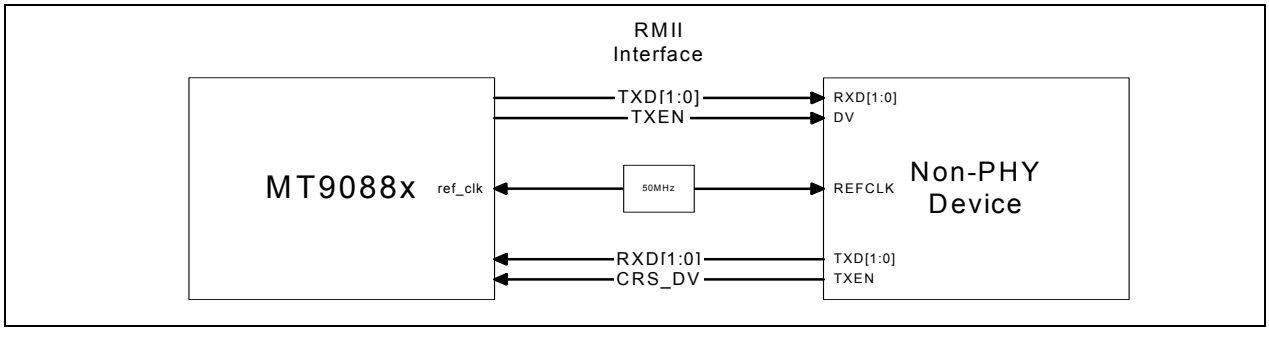

Figure 2 - MT90880/1/2/3 RMII Interface Connection

5.2 MII Ports

This section describes the MAC-to-MAC connection for the Fast Ethernet ports on the MT90880/1/2/3 when operating in MII mode at either 10 Mbit/s or 100 Mbit/s. It also describes the MAC-to-MAC connection for the Fast Ethernet ports on the ZL5011x when operating in MII mode at 100 Mbit/s. Table 6, “MT90880/1/2/3 MII Interface Connection” on page 7 details the connection between MT90880/1/2/3 port 0 and a Generic MII MAC as well as the Zarlink ZL50408 Managed 8-Port 10/100 M + 1G Ethernet switch. The ZL50408 can be programmed to supply TXCLK and RXCLK, thereby eliminating the need for an external per-port clock source as well as reducing the clock routing required.

MT90880/1/2/3 Pin Name	MT90880/1/2/3 Pin Number	MII MAC Connection	ZL50408 MII MAC Connection	Notes
m_mdc	AF9			No connect
m_mdio	AC10			No connect
m_mint0	AF6			No connect
m0_txd[3:0]	AC8 [3], AF5 [2], AE6 [1], AD7 [0]	RXD[3:0]	Mn_RXD[3:0]	
m0_txen	AD6	RXDV	Mn_CRS_DV	
m0_txclk	AB9	RXCLK	Mn_RXCLK	Connect to 2.5 or 25 MHz clock (10 or 100 Mbit/s) OR ZL50408 supplies clock.
m0_rxd[3:0]	AF8 [3], AE8 [2], AE9 [1], AD9 [0]	TXD[3:0]	Mn_TXD[3:0]	
m0_rxdv	AF7	TXEN	Mn_TXEN	
m0_rxclk	AB10	TXCLK	Mn_TXCLK	Connect to 2.5 or 25 MHz clock (10 or 100 Mbit/s) OR ZL50408 supplies clock.
m0_rxer	AD8			No connect
m0_crs	AC9			No connect (full duplex)
m0_col	AE7			No connect (full duplex)

Table 6 - MT90880/1/2/3 MII Interface Connection

Table 7, “ZL5011x MII Interface Connection” on page 8 details the connection between ZL5011x port 0 and a Generic MII MAC as well as the Zarlink ZL50408 Managed 8-Port 10/100M + 1G Ethernet switch. The ZL50408 can be programmed to supply TXCLK and RXCLK, thereby eliminating the need for an external per-port clock source as well as reducing the clock routing required. The Mn_REFCLK pin on the ZL5011x must be connected to the same clock source as the Mn_RXCLK on the ZL5011x for correct operation.

ZL5011x Pin Name	ZL50110/11/14 Pin Number	ZL50115/16/17/ 18/19/20 Pin Number	MII MAC Connection	ZL50408 MII MAC Connection	Notes
M_MDC	H23	H1			No connect
M_MDIO	G26	G1			No connect
M0_LINKUP_LED	G24 or AB23	G3			No connect
M0_ACTIVE_LED	AC26	D17			No connect
M0_REFCLK	AA24	D11			Connect to same clock source as M0_RXCLK.
M0_TXD[3:0]	AA23, W21, Y22, AA22	B13, B14, D13, C13	RXD[3:0]	Mn_RXD[3:0]	
M0_TXEN	V23	A9	RXDV	Mn_CRS_DV	
M0_TXCLK	U24	A3	RXCLK	Mn_RXCLK	Connect to 25 MHz clock (100 Mbit/s) OR ZL50408 supplies clock.
M0_TXER	V22	B10			
M0_RXD[3:0]	W26, U22, Y26, AA26	C8, D10, C9, B7	TXD[3:0]	Mn_TXD[3:0]	
M0_RXDV	V25	C7	TXEN	Mn_TXEN	
M0_RXCLK	AB22	C10	TXCLK	Mn_TXCLK	Connect to 25 MHz clock (100 Mbit/s) OR ZL50408 supplies clock.
M0_RXER	V26	D6			No connect
M0_CRS	U25	B6			No connect (full duplex)
M0_COL	Y25	A7			No connect (full duplex)

Table 7 - ZL5011x MII Interface Connection

Figure 3, “CESoP MII Interface Connections”, on page 9 shows the MAC-to-MAC connection between a Zarlink CESoP processor and a Generic MII MAC interface.

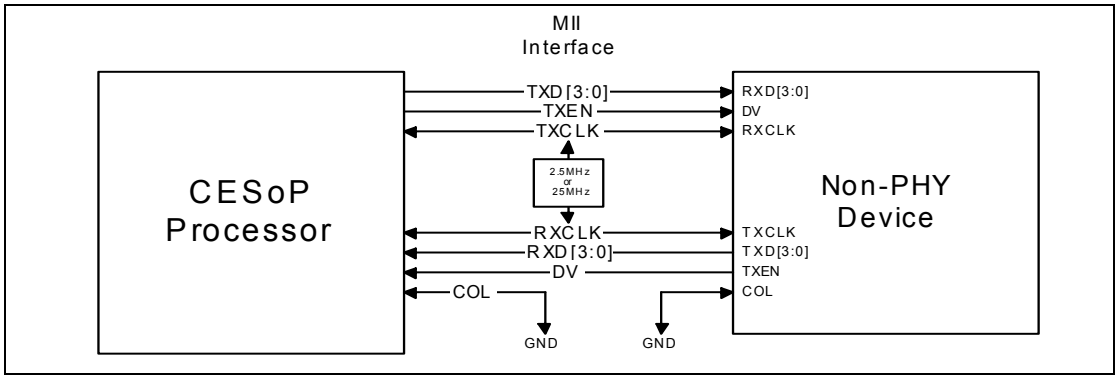

Figure 3 - CESoP MII Interface Connections

5.3 GMII Ports

This section describes the MAC-to-MAC connection for the Gigabit Ethernet ports on the ZL5011x when operating in GMII mode at 1000 Mbit/s. Table 8, “ZL5011x GMII Interface Configuration” on page 9 details the connection between ZL5011x port 0 and a Generic MII MAC as well as the Zarlink MVTX2804 Managed 8-Port 1000 Mbps Ethernet Switch. Figure 4, “ZL5011x GMII Interface Connections”, on page 10 shows the MAC-to-MAC connection between a ZL5011x CESoP processor and a Generic GMII MAC interface.

ZL5011x Pin Name	ZL50110/11/14 Pin Number	ZL50115/16/17/18/ 19/20 Pin Number	GMII MAC Connection	MVTX2804 GMII MAC Connection	Notes
M0_LINKUP_LED	G24 or AB23	G3			No connect
M0_ACTIVE_LED	AC26	D17			No connect
M0_GIGABIT_LED	H22	E2			No connect
M0_REFCLK	AA24	D11		GREF_CLK	Connect to 125 MHz clock.
M0_TXD[7:0]	V21, W23, W22, Y23, A23, W21, Y22, AA22	C11, D12, B12, C12, B13, B14, D13, C13	RXD[7:0]	Gn_RXD[7:0]	
M0_TXEN	V23	A9	RXDV	Gn_RX_DV	
M0_GTXCLK	U21	A8	RXCLK	Gn_RXCLK	
M0_TXER	V22	B10	RXER	Gn_RX_ER	
M0_RXD[7:0]	W25, W24, U23, V24, W26, U22, Y26, AA26	A4, A5, D8, A6, C8, D10, C9, B7	TXD[7:0]	Gn_TXD[7:0]	
M0_RXDV	V25	C7	TXEN	Gn_TX_EN	
M0_RXCLK	AB22	C10	TXCLK	Gn_TXCLK	
M0_RXER	V26	D6	TXER	Gn_TX_ER	
M0_CRS	U25	B6			No connect (full duplex)
M0_COL	Y25	A7			No connect (full duplex)

Table 8 - ZL5011x GMII Interface Configuration

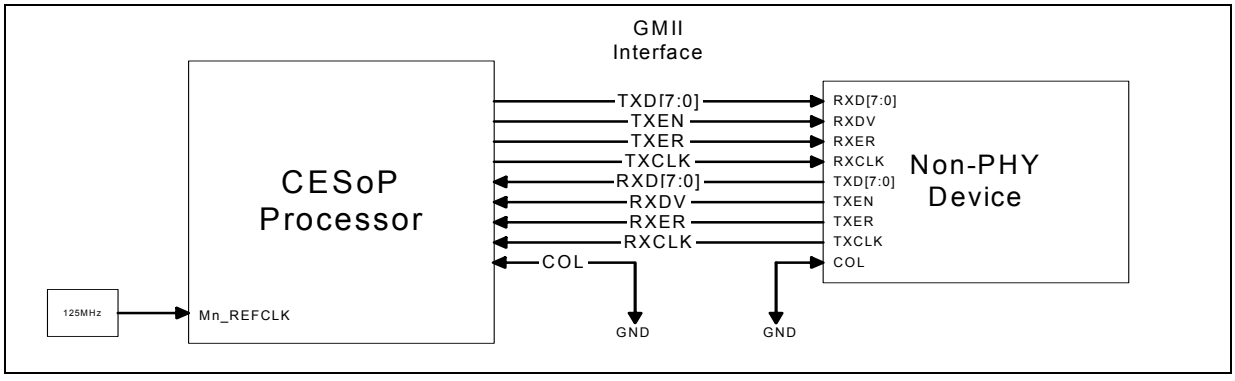

Figure 4 - ZL5011x GMII Interface Connections

6.0 Layout Considerations

An important point about MAC-to-MAC connections is with regard to layout of the board. When a common clock is input to both MAC devices, used to sample data by one MAC and drive data by the other MAC, the propagation delay from the clock source must be the same to both MAC devices. As an example, referring to Figure 2, “MT90880/1/2/3 RMII Interface Connection”, on page 6, a ref_clk reference clock is supplied to both MAC devices. For best operation the trace lengths from ref_clk source to the ref_clk pins on the respective MAC devices should be of equal length. Additionally, it is advantageous to keep the trace lengths as short as possible. When one MAC device drives the clock and data to the other MAC device, as is possible with ZL50408, this issue is of less significance.