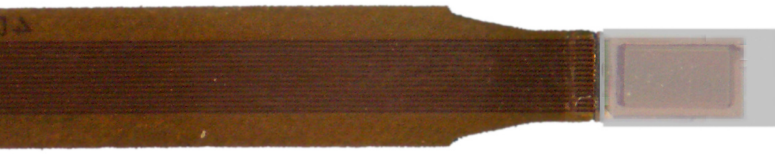
# CyberDisplay® 152K LV

## Ultra-Compact, Wide-Format (16:9) Color AMLCD



***Frameless***
Part No. KCD-QWSF-AA

## 1 GENERAL DESCRIPTION

The CyberDisplay® 152K LV is an active-matrix liquid crystal display with 152k color dot resolution. The CyberDisplay 152K LV utilizes high-performance single-crystal silicon transistors, and is the smallest (0.20" diagonal) transmissive AMLCD for the resolution. The transmissive AMLCD allows the use of simple and thin optics for compact system size.

The CyberDisplay 152K LV features Kopin's patent-pending low-voltage architecture for low power consumption and compatibility with CMOS driver ICs. The input video levels are reduced to half the typical values for other LCDs because the capacitively coupled interface effectively doubles the voltage written to pixels while the integrated switch circuitry restores the DC level. Bidirectional horizontal and vertical scanner circuits are integrated. A sleep mode is provided to simplify system power management.

Figure 1-1 shows the pixel array layout. The active array of 695 × 218 dots is surrounded by opaque dummy pixels, for a total array size of 705 × 222 dots. Alternate rows are shifted horizontally by 1½ dots to produce a delta pixel arrangement.

The CyberDisplay 152K LV is available in a frameless package (KCD-QWSF-AA) for integration into a viewfinder module.

### *1.1 Applications*

The CyberDisplay 152K LV is ideal for camcorder and digital camera viewfinders or entry-level portable consumer and industrial applications that take video in a wide aspect ratio.

### *1.2 Key Specifications*

- 695 × 218 active color dot resolution
- 705 × 222 total color dot resolution
- 6.3 (W) × 11.3 (H) µm pixel pitch
- Ultra-compact (0.20" diagonal)
- Active pixel area (4.38 mm × 2.46 mm)
- Wide 16:9 format with same height as CyberDisplay 113K
- Parallel RGB analog input
- Simple 3.3-volt interface for CMOS compatible drive chip
- Power-saving sleep mode
- Integrated low voltage detect
- Integrated horizontal and vertical scanners
- Bidirectional vertical and horizontal scanning

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## 2 ELECTRICAL SPECIFICATIONS

A block diagram of the CyberDisplay 152K LV is shown in Figure 2-1. External capacitors couple the RGB component signals to the display's six video inputs, with one pair of high and low inputs for each primary color (red, green, and blue). The row inversion drive scheme requires that video polarity be inverted on alternating, with the INV signal selecting the high or low inputs.

Integrated scanners drive the active matrix pixel array. The horizontal and vertical scan directions are mask-programmable, and the display is available in up or down, left or right, scanning configurations.

### *2.1 Interface Signals*

A 15-pin flex cable provides electrical connection to the CyberDisplay 152K LV. The interface signals are listed in Table 2-1.

### *2.2 Inversion*

To preserve DC balance in the liquid crystal, each pixel must be driven with alternating high and low video. The CyberDisplay 152K LV uses row inversion, in which all pixels of each row have the same polarity, but successive rows have alternating polarity. The INV signal indicates the polarity of each row (see timing diagrams of §2.5). The row inversion phases must be inverted with successive fields. For example, if one field is driven with row 0 low, row 1 high, and row 2 low, then the following field must have row 0 high, row 1 low, and row 2 high.

| Pin | Symbol | Description |
|---|---|---|
| 1 | VEE | Supply = 0V |
| 2 | VIDRH | High red video input |
| 3 | VIDGH | High green video input |
| 4 | VIDBH | High blue video input |
| 5 | VIDRL | Low red video input |
| 6 | VIDGL | Low green video input |
| 7 | VIDBL | Low blue video input |
| 8 | HS | Horizontal sync |
| 9 | VS | Vertical sync |
| 10 | INV | Inversion polarity |
| 11 | SLEEP* | Sleep mode |
| 12 | CK0 | Clock |
| 13 | CK1 | Clock |
| 14 | VDD | Supply |
| 15 | VSS | Supply |

* Signal is active low

**Table 2-1:** Supply and Interface Voltage Levels

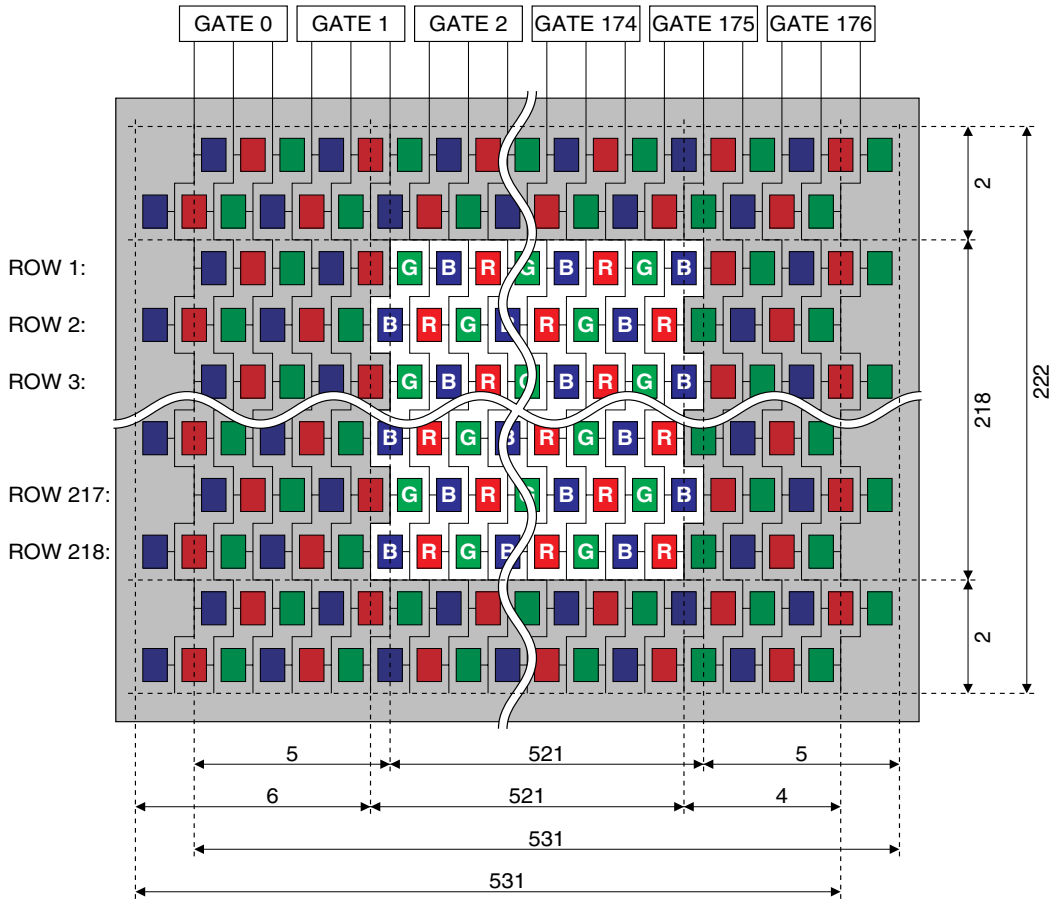


**Figure 1-1:** Pixel Array

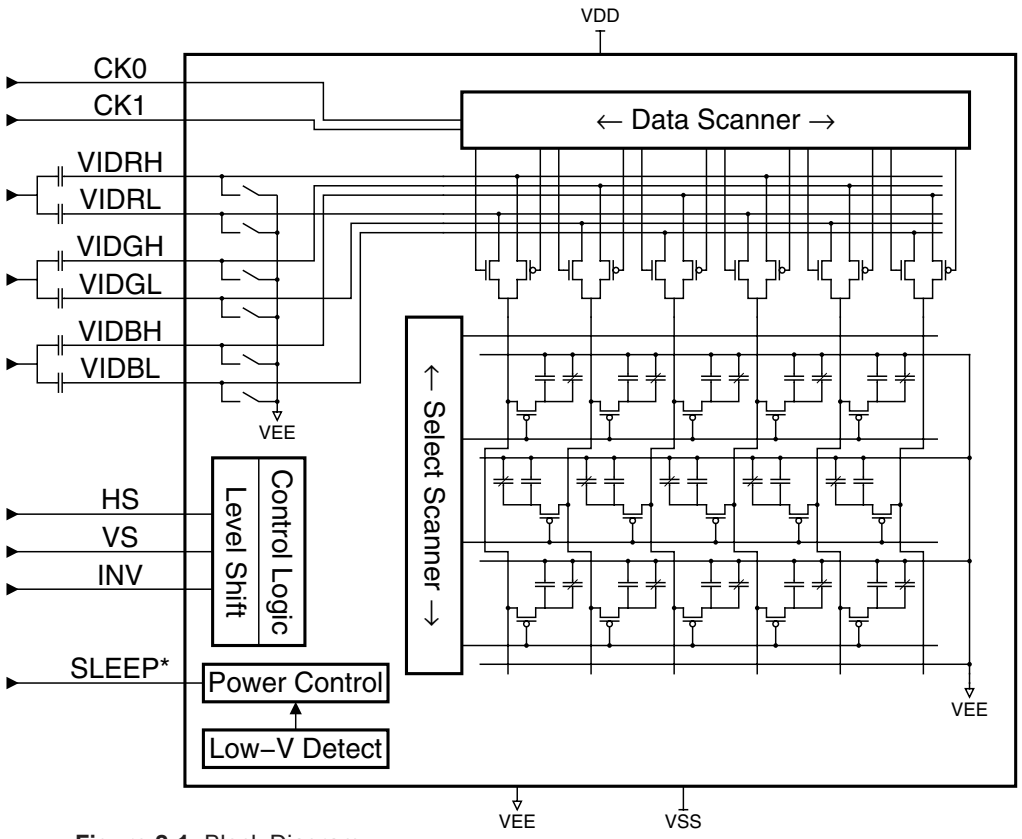


**Figure 2-1:** Block Diagram

### *2.3 Sleep Mode*

The CyberDisplay 152K LV features a sleep mode to simplify system power management. When the SLEEP* pin is driven low, all scanners are disabled and the pixel array is driven to the white state.

The display may remain powered and will draw minimal current while in sleep mode. The backlight may be turned off.

The display will also enter sleep mode when the integrated low voltage detect circuit determines that power has been removed.

### *2.4 Electrical Characteristics*

Permanent damage to the display may result if the Absolute Maximum Ratings in Table 2-2 are exceeded. The Absolute Maximum Ratings are not typical operating conditions.

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply voltage — source | $V_{DD}$ | – 0.5 | 5.0 | V |
| Supply voltage — sink | $V_{SS}$ | – 7.0 | 0.5 | V |
| All inputs | $V_I$ | $V_{SS}$– 0.5 | $V_{DD}$+ 0.5 | V |

Note: All voltages relative to $V_{EE}$=0.

**Table 2-2:** Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply voltage — source | $V_{DD}$ | 3 | 3.5 | 3.6 | V |
| Supply voltage — sink | $V_{SS}$ | – 5.5 | – 5.0 | – 4.5 | V |
| Operating current — source | $I_{DD}$ | | 0.4 | | mA |
| Operating current — sink | $I_{SS}$ | | 0.4 | | mA |
| Operating current | $I_{EE}$ | – 100 | | 100 | µA |
| VID[RGB]H high black level | $V_{HK}$ | | 3.3 | | V |
| VID[RGB]H high white level | $V_{HW}$ | | 0 | | V |
| VID[RGB]L low white level | $V_{LW}$ | | 0 | | V |
| VID[RGB]L low black level | $V_{LK}$ | | – 3.3 | | V |
| Digital input high | $V_{IH}$ | | | | V |
| Digital input low | $V_{IL}$ | | | | V |
| Input current | $I_I$ | – 10 | | 10 | µA |
| Input capacitance: video inputs | $C_{VID}$ | | 21 | 25 | pF |
| Input capacitance: CK0 & CK1 | $C_C$ | | 8 | 12 | pF |
| Input capacitance: other inputs | $C_I$ | | 5 | 10 | pF |

Note: All voltages relative to $V_{EE}$=0.

**Table 2-3:** Electrical Characteristics and Recommended DC Operating Conditions

### *2.5 Timing Specification*

The parameters of Table 2-4 are defined in the timing diagrams of this section.

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Field period | $t_V$ | | 16.7–20.0 | | ms |
| Field rate | $1/t_V$ | | 50–60 | | Hz |
| Line period | $t_H$ | | 64 | | µs |
| Line rate | $1/t_H$ | | 15.6–15.7 | | kHz |
| Clock period | $t_{CP}$ | | 407–410 | | ns |
| HS high pulse width | $t_{HH}$ | 5 | | | µs |
| HS to CK0 pulse 0 delay | $t_{FD}$ | 1 | | | µs |
| CK1 pulse 239 to HS delay | $t_{BD}$ | 1 | | | µs |
| Clock high pulse width | $t_{CH}$ | 120 | | | ns |
| CK0 to CK1 delay | $t_{CD}$ | $(t_{CP}/2)–5$ | $t_{CP}/2$ | $(t_{CP}/2)+5$ | ns |
| CK0 and CK1 non-overlap | $t_{NOL}$ | 0 | 5 | | ns |
| White hold after HS | $t_{WH}$ | 400 | | | ns |
| White setup before HS | $t_{WS}$ | 200 | | | ns |
| Video setup | $t_{VS}$ | 80 | | | ns |
| Video hold | $t_{VH}$ | 50 | | | ns |
| INV setup before HS | $t_{IS}$ | 100 | | | ns |
| INV hold after HS | $t_{IH}$ | 100 | | | ns |
| VS high pulse width | $t_{VSH}$ | 1 | | | µs |
| VS low pulse width | $t_{VSL}$ | 1 | | | µs |
| VS to HS delay | $t_{VHD}$ | 1 | | | µs |
| HS to VS delay | $t_{HVD}$ | 1 | | | µs |

**Table 2-4:** Electrical Characteristics and Recommended AC Operating Conditions

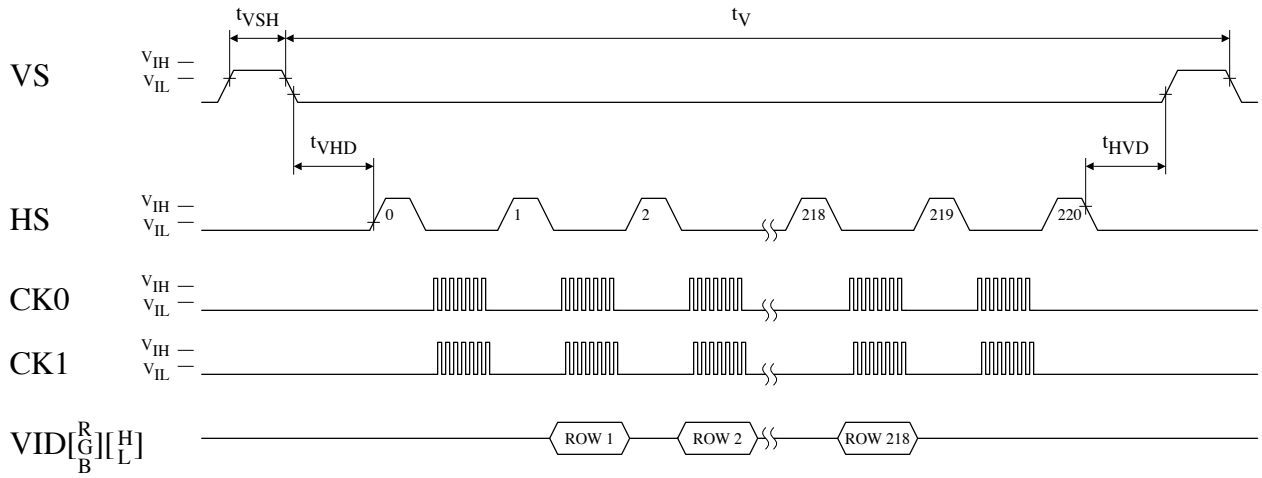


**Figure 2-2:** Vertical Timing, Top-to-Bottom Scan

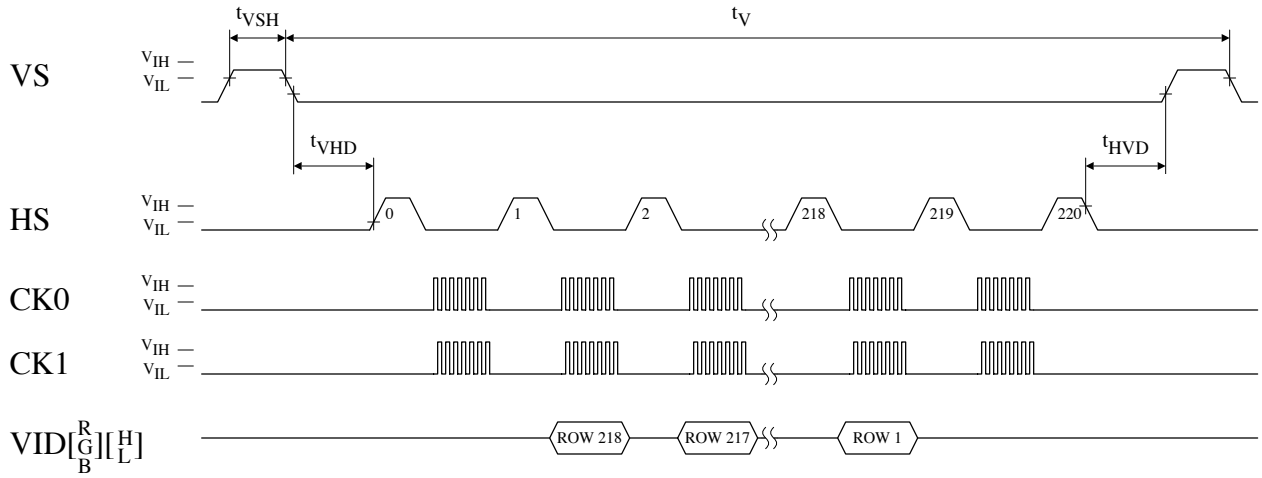


**Figure 2-3:** Vertical Timing, Bottom-to-Top Scan

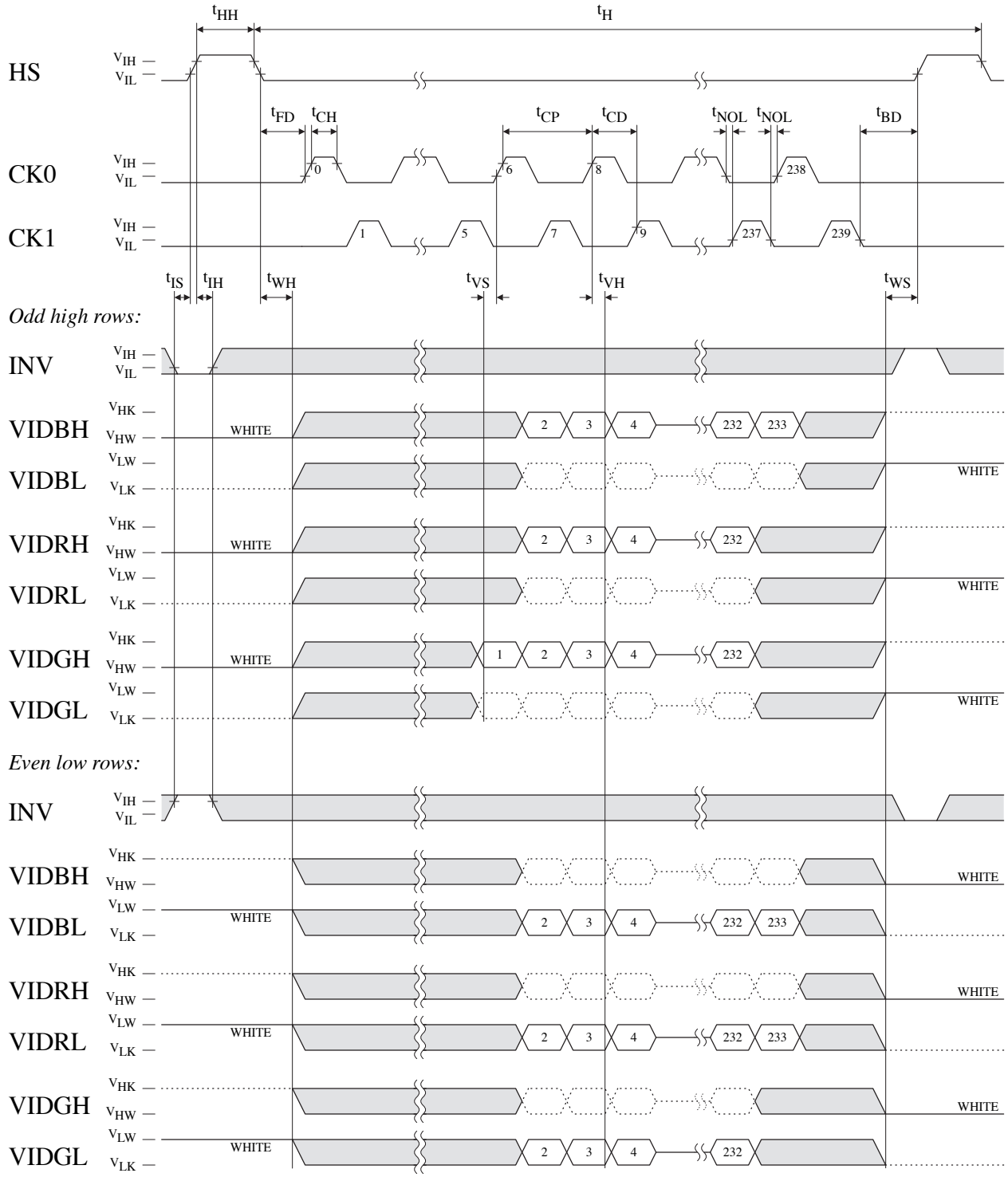


**Figure 2-4:** Horizontal Timing, Left-to-Right Scan, Odd Rows High

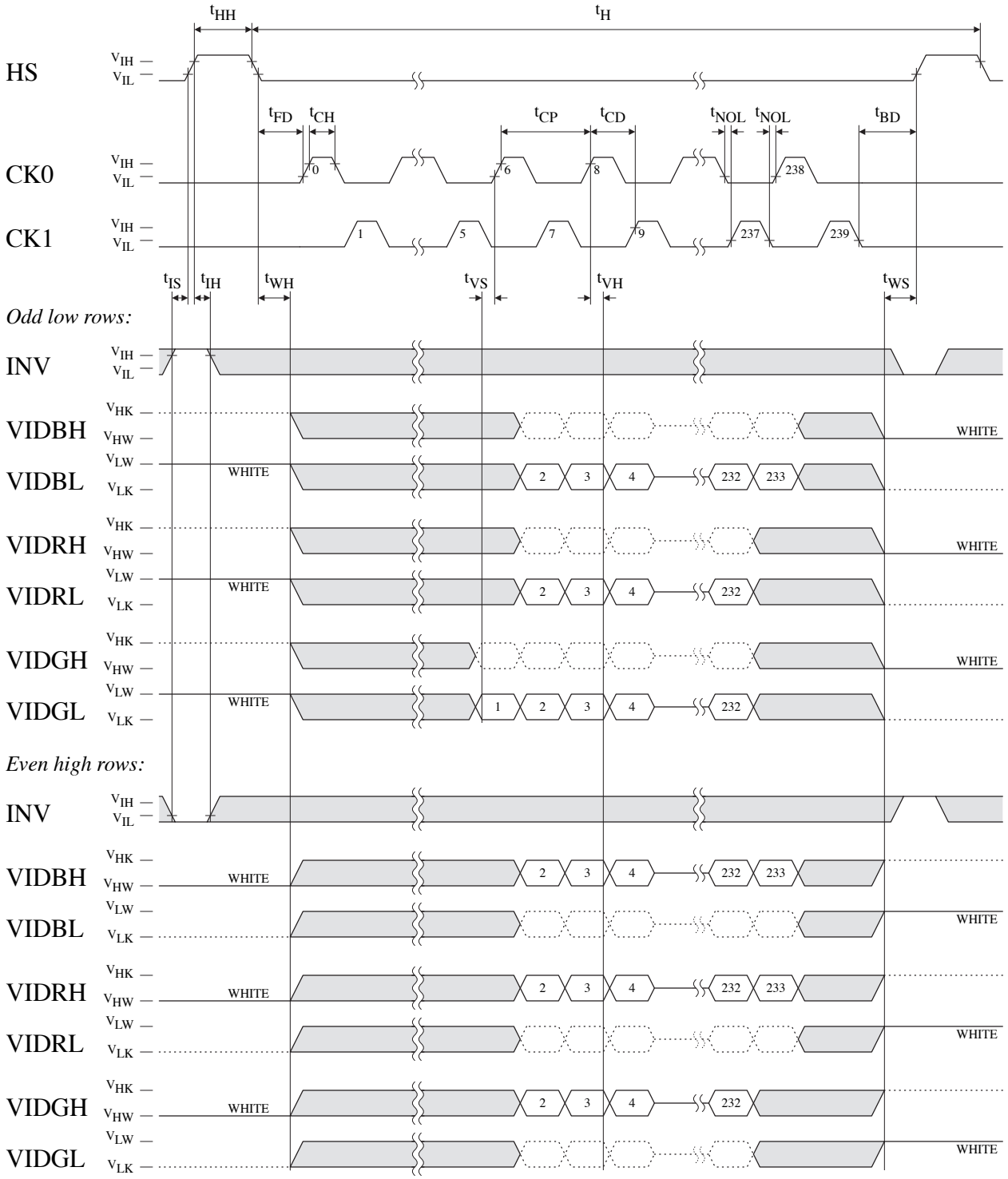


**Figure 2-5:** Horizontal Timing-Left-to-Right Scan, Odd Rows Low

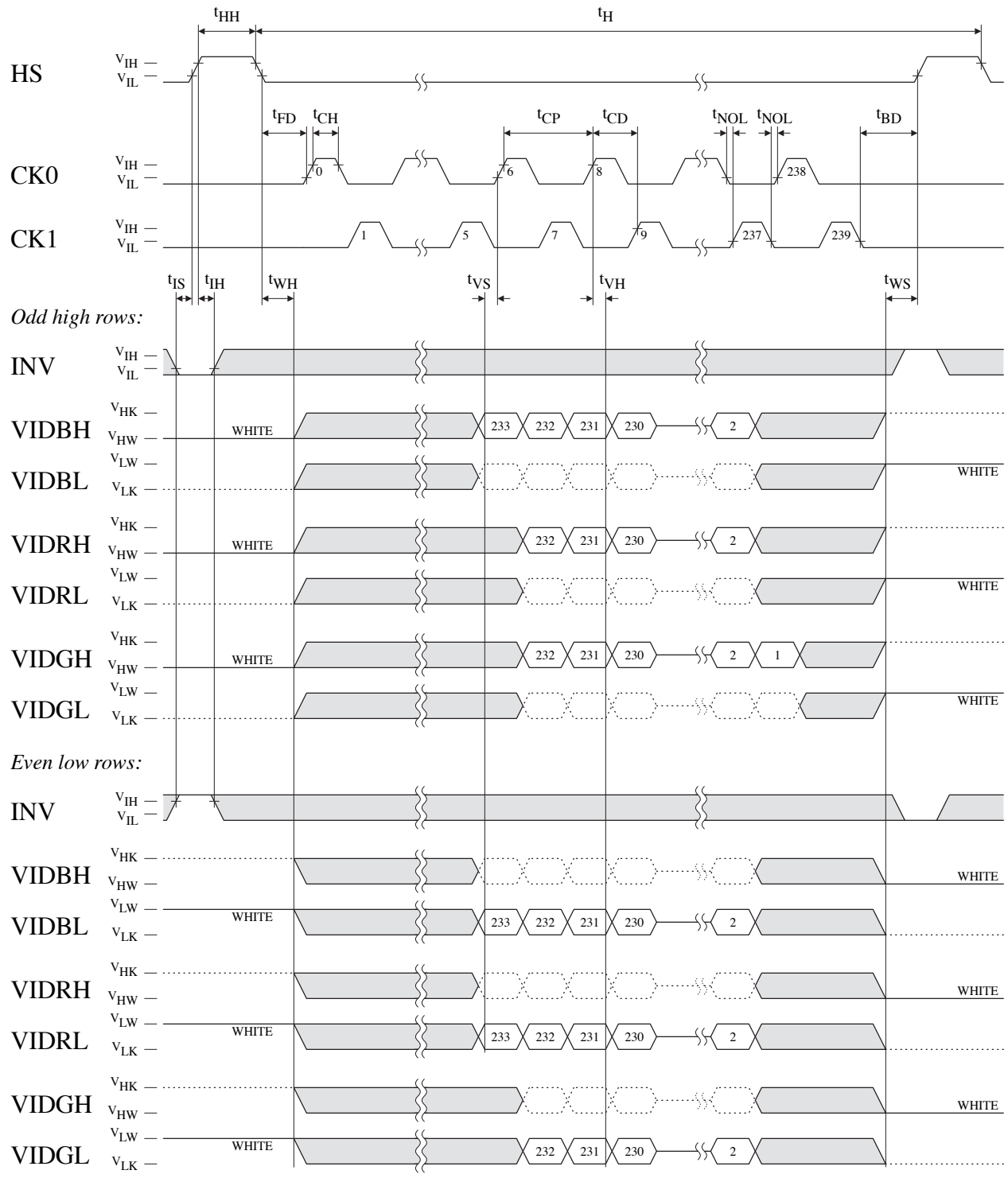


**Figure 2-6:** Horizontal Timing, Right-to-Left Scan, Odd Rows High

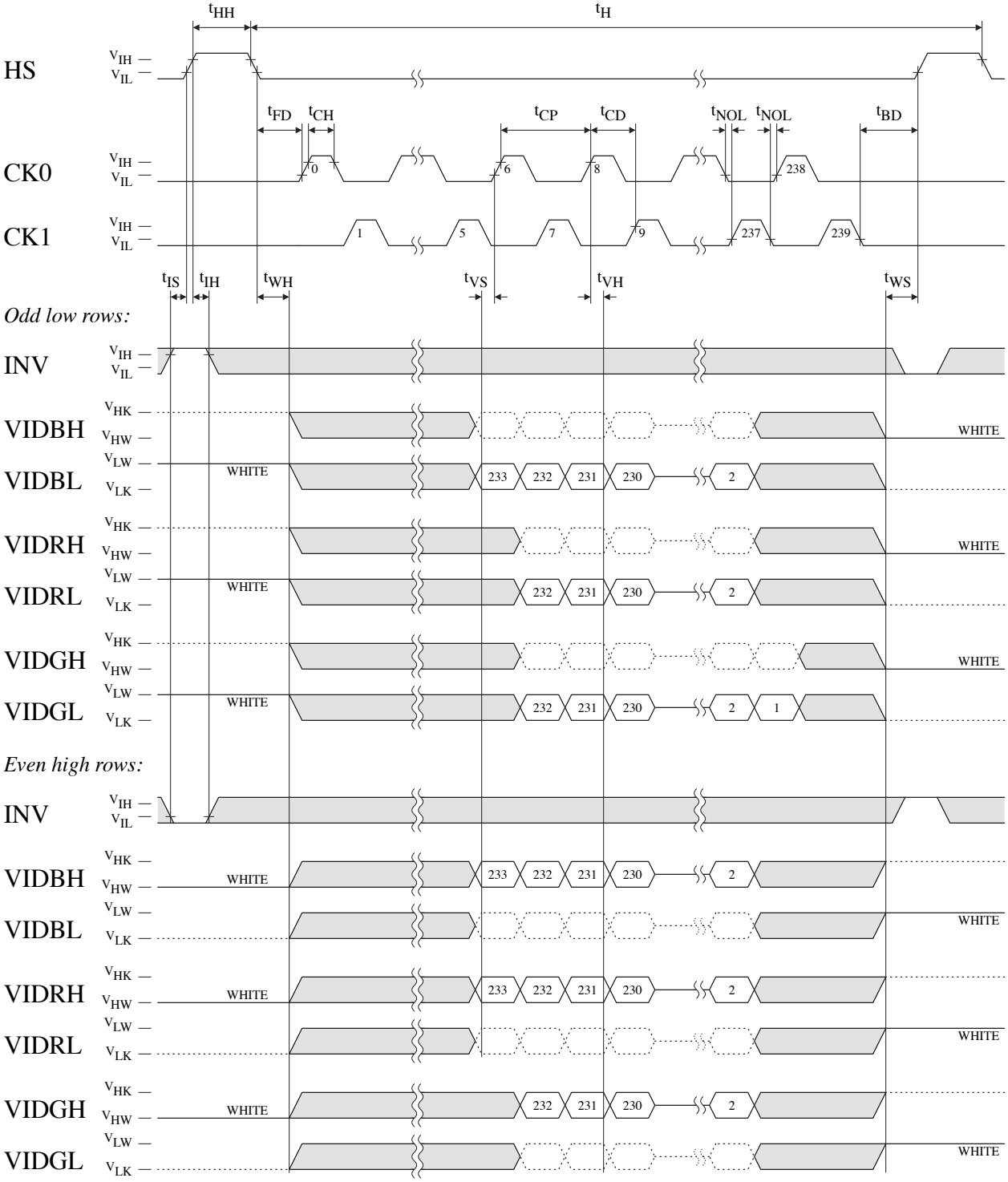


**Figure 2-7:** Horizontal Timing, Right-to-Left Scan, Odd Rows Low

### *2.6 Line Skipping*

Simple vertical scaling may be accomplished by line skipping. For example, to display PAL video with the correct aspect ratio, one of every six lines should be skipped. As illustrated in Figure 2-8, the HS pulse should be extended to remain high during the skipped line. This technique minimizes visible artifacts by preserving the same HS-video timing in the rows before and after the skipped line.

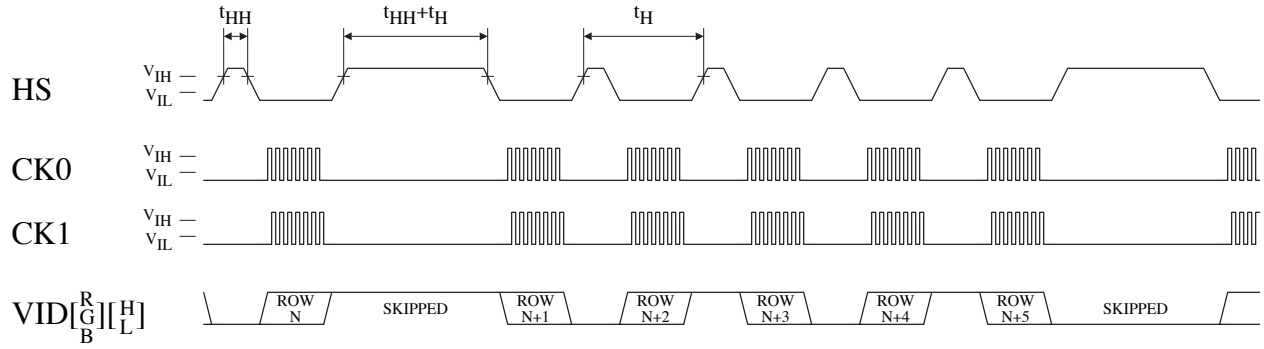


**Figure 2-8:** Line Skipping Timing Diagram

## 3 OPTICAL SPECIFICATIONS

### *3.1 Optical Characteristics*

| Item | | | Symbol | Notes | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Contrast ratio | Vsig = 0 ± 3.3V | | $CR_{3.3}25$ | 1 | 30 | 60 | -- | -- |
| Optical Transmittance | | 25°C | T | 2 | 1.2 | 1.5 | 1.9 | % |
| Chromaticity | W | X | Wx | 3 | 0.26 | 0.30 | 0.34 | CIE standards |
| | | Y | Wy | | 0.27 | 0.31 | 0.35 | |
| | R | X | Rx | | 0.51 | 0.55 | 0.59 | |
| | | Y | Ry | | 0.27 | 0.31 | 0.35 | |
| | G | X | Gx | | 0.25 | 0.28 | 0.32 | |
| | | Y | Gy | | 0.51 | 0.55 | 0.59 | |
| | B | X | Bx | | 0.11 | 0.15 | 0.19 | |
| | | Y | By | | 0.10 | 0.14 | 0.18 | |
| V-T characteristics | $V_{90}$ | 25°C | $V_{90-25}$ | 4 | 0.4 | 0.7 | 1.1 | V |
| | $V_{50}$ | 25°C | $V_{50-25}$ | | 1.0 | 1.3 | 1.7 | |
| | $V_{10}$ | 25°C | $V_{10-25}$ | | 1.7 | 2.0 | 2.6 | |
| Response time | ON time | 25°C | $ton_{25}$ | 5 | -- | 10 | 20 | ms |
| | OFF time | 25°C | $toff_{25}$ | | -- | 30 | 40 | |
| Flicker | | | F | 6 | -- | -- | -40 | dB |

**Table 3-1:** Optical Characteristics (see notes on following page)

Notes On Measurement Conditions:

1. $CR_{3.3}25$ = (Luminance White)/(Luminance Black). System I
2. T = (Luminance White)/(Luminance Backlight). System I
3. CIE Standard 1931. Wight backlight: 7500K. System II
4. V-T is relationship of signal amplitude to transmittance. System I
5. 0% to 90% transmittance. System I + Oscilloscope
6. 20log(AC/DC) @ 50% transmittance. System I + Spectrum Analyzer

# 4 MECHANICAL SPECIFICATIONS

## *4.1 Interconnect*

The flexible PC cable is strain relieved, but tugging forces should be limited to less than 0.5 kg perpendicular to the display and less than 1 kg parallel to the display. The minimum inside bend radius for the cable is .03 inches. Repeated reformings are not recommended.

## *4.2 Mechanical drawings*

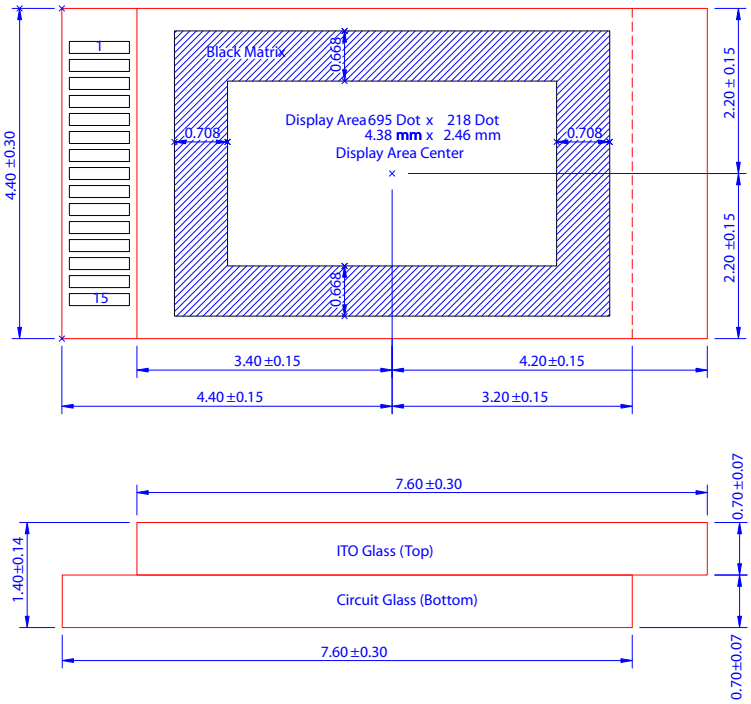


**Figure 4-1:** CyberDisplay 152K LV Display and Pixel Array Area

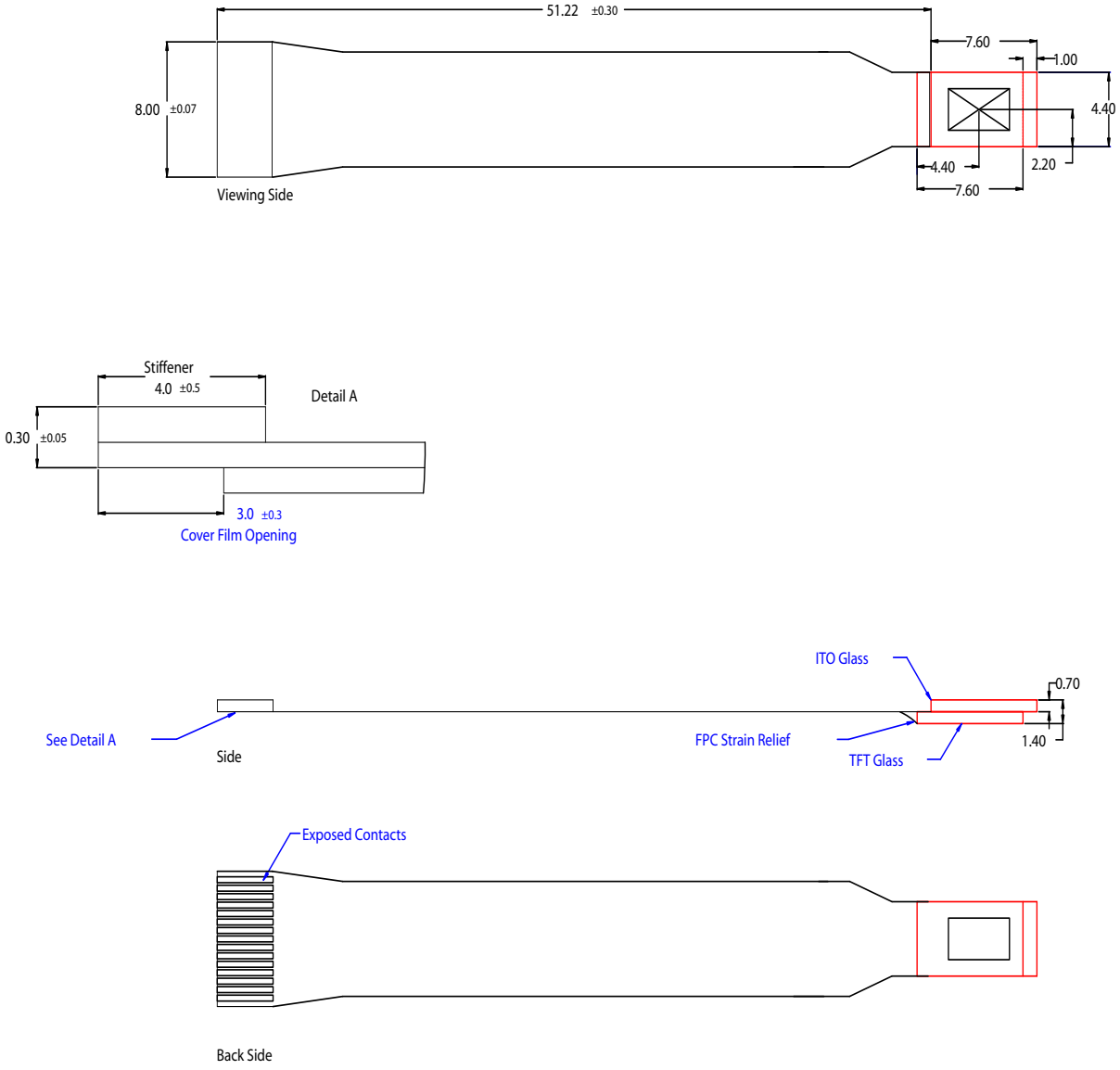


**Figure 4-2:** CyberDisplay 152K LV and FPC Assembly