Link Street® 88E6060 - Unrestricted

Low Power, 6-port, 10/100 Ethernet Switch

Doc. No. MV-S100952-U0, Rev. --
January 3, 2008
Document Classification: Proprietary Information

Document Conventions

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Overview

The Marvell® 88E6060 is a single chip integration of a complete 6-port Fast Ethernet switch with support for a CPU connection. It contains five 10BASE-T/100BASE-TX transceivers (PHYs), two that can be used to support 100BASE-FX; six independent Fast Ethernet media access controllers (MACs), a high-speed non-blocking switch fabric, a high-performance address lookup engine, and a 1/2 megabit frame buffer memory. It is designed for cost-sensitive low port count switch systems and firewall routers.

The PHY transceivers are designed with Marvell Virtual Cable Tester™ (VCT™) technology for advanced cable diagnostics. VCT enables IT managers to easily pinpoint the location of cabling issues down to a meter or less, reducing network installation and support costs.

The Marvell 88E6060 is designed to work in all environments. True Plug-n-Play is supported with Auto Crossover, Auto Polarity and Auto Negotiation in the PHYs, along with bridge loop prevention (using Port States implementing Spanning Tree support).

The shared memory-based switch fabric uses the latest Marvell switch architecture that provides non-blocking switching performance in all traffic environments. Back-pressure and pause-frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The lookup engine allows for up to 1,024 active nodes to be connected with the switch.

The sixth port, ‘always-on’ RMII/MII/SNI interface supports a direct connection to Management or Router CPUs with integrated MACs. It can be configured in either RMII mode, MII-PHY or MII-MAC mode or SNI mode. These interfaces along with BPDU handling, programmable per port VLAN configurations, and Port States, support Spanning Tree and truly isolated WAN vs. LAN firewall applications.

The PHY units in the Marvell 88E6060 are designed with Marvell cutting-edge mixed-signal processing technology for digital implementation of adaptive equalization and clock data recovery. Special power management techniques are used to facilitate low power dissipation and high port count integration. Both the PHY and MAC units in the Marvell 88E6060 comply fully with the applicable sections of IEEE 802.3, IEEE 802.3u, and IEEE 802.3x standards.

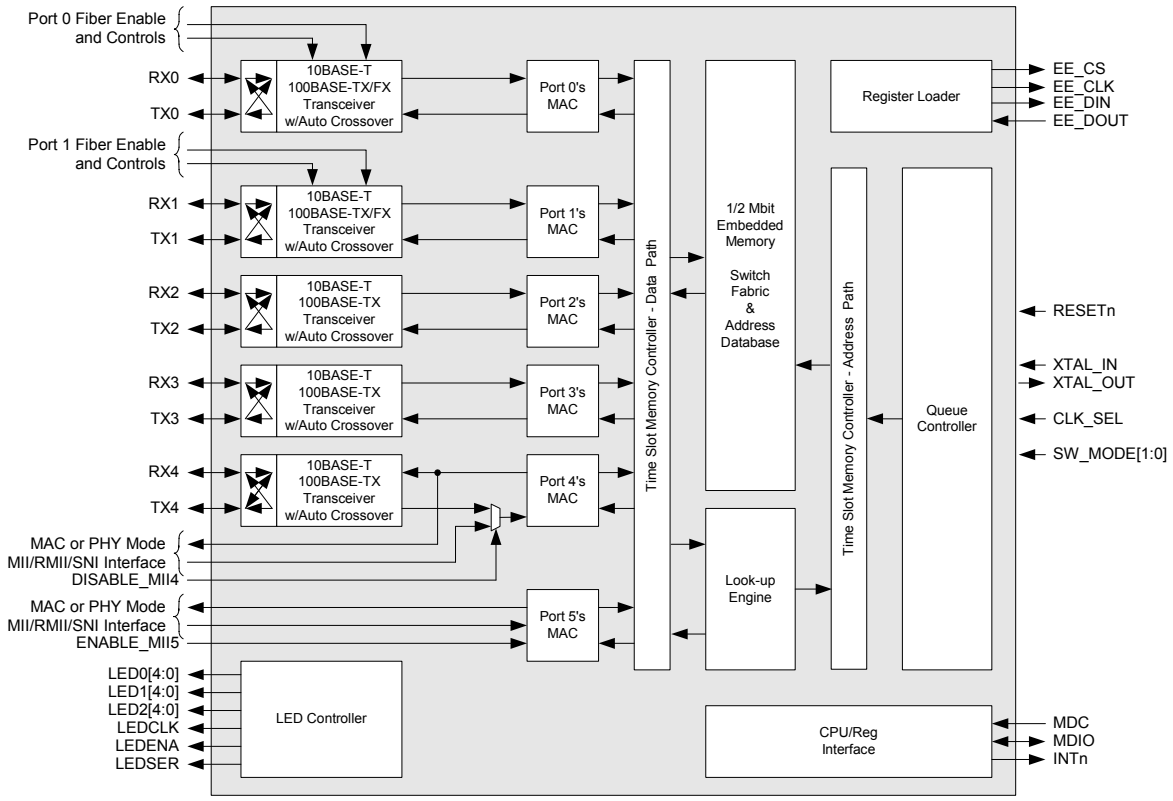
The many operating modes of the Marvell 88E6060 can be configured using SMI (serial management interface - MDC/MDIO) and/or a low cost serial EEPROM (93C46, C56 or C66).

Features

- Single chip integration of a 6-port Fast Ethernet switch in a 14x20 mm 128-pin PQFP package
- Integrates six independent media access controllers fully compliant with the applicable sections of IEEE802.3
- Integrates five independent Fast Ethernet PHY transceivers fully compliant with the applicable sections of IEEE802.3
- Supports 802.1X implementation with Port-based access control
- Port based VLANs supported in any combination
- Supports a CPU header mode for accelerated router performance and wirespeed VLAN control
- Port States & BPDU handling supports Spanning Tree
- Automatic MDI/MDIX crossover for 100BASE-TX and 10BASE-T ports
- Port 0 and Port 1 can be configured as copper (100BASE-TX or 10BASE-T) or fiber (100BASE-FX)
- Port 5 has dedicated, always on, MAC Mode (Forward) or PHY Mode (Reverse) RMII/MII/SNI interface for management and firewall applications
- Port 4 can be either a copper (100BASE-TX or 10BASE-T) or an MII interface with the same interface options as Port 5
- Each port works at 10 Mbps or 100 Mbps, full-duplex or half-duplex mode (forced or auto-negotiated)
- Back-pressure flow control on half-duplex ports & Pause-frame flow control on full-duplex ports
- Shared on-chip memory-based switch fabric with true non-blocking switching performance
- High performance lookup engine with support for up to 1,024 MAC address entries with automatic learning and aging
- Flexible LED support for Link, Speed, Duplex Mode, Collision, and Tx/Rx Activities
- Supports a low cost 25 MHz XTAL clock source or a 25 MHz or 50 MHz OSC.
- Pin compatible with the Marvell® 88E6063, 88E6061, 88E6065, 88E6031, and 88E6035
- Low power dissipation P_{AVE} = Less than 0.6W
- Available with Commercial grade (88E6060 part) or Industrial grade (88E6060-I part) temperature specifications
- Integrates Virtual Circuit Tester™ (VCT™) with each Marvell PHY

Applications

- Firewall Router Switch w/four 10/100BASE-T LAN ports & one 10/100BASE-T WAN port
- Five port Switch with Spanning Tree Support
- Firewall Router Switch supporting a Fiber WAN port
- Fiber to Copper Industrial Temperature media converter
- Four-port LAN switch with two MII connections for WAN PHY and wireless interface



88E6060 Top Level Block Diagram

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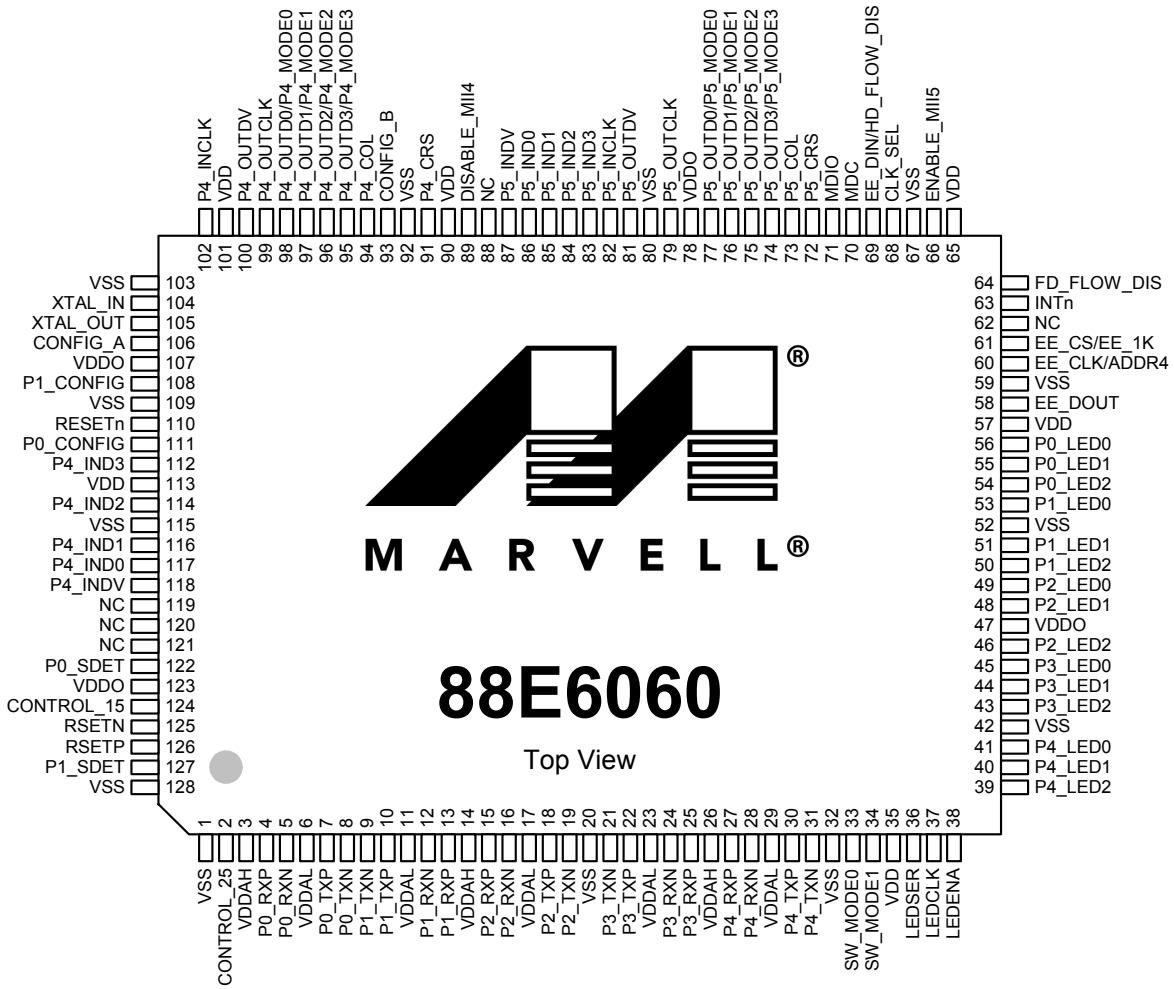
Section 1. Signal Description

1.1 88E6060 128-Pin PQFP Package

Figure 1: 88E6060 128-Pin PQFP Package (Top View)



1.2 Pin Description

Table 1: Pin Type Definitions

Pin Type	Definition
I/O	Input and output
Input	Input only
Output	Output only
Open Drain	Open drain output
Analog	Analog
Typically Input	May be input or output depending upon operating state; usually input
Typically Output	May be output or input depending upon operating state; usually output
Power	Device voltage and current supply
Ground	Device current return
NC	No connection, do not connect anything to these pins

Table 2: Network Interface

128-PQFP Package Pin #	Pin Name	Pin Type	Description
27 25 15 13 4	P[4:0]_RXP	Typically Input Output if in Crossover mode	Receiver input – Positive. P[4:0]_RXP connects directly to the receiver magnetics. If the port is configured for 100BASE-FX mode (ports 0 and 1 only) RXP connects directly to the fiber-optic receiver's positive output. These pins can become outputs if Auto MDI/MDIX Crossover is enabled (see section 4.6). If a PHY port is not used, the RXP pins should be tied to VSS.
28 24 16 12 5	P[4:0]_RXN	Typically Input Output if in Crossover mode	Receiver input – Negative. P[4:0]_RXN connects directly to the receiver magnetics. If the port is configured for 100BASE-FX mode (ports 0 and 1 only) RXN connects directly to the fiber-optic receiver's negative output. These pins can become outputs if Auto MDI/MDIX Crossover is enabled (see section 4.6). If a PHY port is not used, the RXN pins should be tied to VSS.
30 22 18 10 7	P[4:0]_TXP	Typically Output Input if in Crossover mode	Transmitter output – Positive. P[4:0]_TXP connects directly to the transmitter magnetics. If the port is configured for 100BASE-FX mode (ports 0 and 1 only) TXP connects directly to the fiber-optic transmitter's positive input. These pins can become inputs if Auto MDI/MDIX Crossover is enabled (see section 4.6). If a PHY port is not used, the TXP pins should be tied to VSS.
31 21 19 9 8	P[4:0]_TXN	Typically Output Input if in Crossover mode	Transmitter output – Negative. P[4:0]_TXN connects directly to the transmitter magnetics. If the port is configured for 100BASE-FX mode (ports 0 and 1 only) TXN connects directly to the fiber-optic transmitter's negative input. These pins can become inputs if Auto MDI/MDIX Crossover is enabled (see section 4.6). If a PHY port is not used, the TXN pins should be tied to VSS.
127 122	P[1:0]_SDET	Input	Signal Detect input. If port 0 and/or 1 is configured for 100BASE-FX mode SDET indicates whether a signal is detected by the fiber-optic transceiver. A positive level indicates that a signal is detected. If port 0 and/or 1 is configured for 10/100BASE-T mode SDET is not used, but cannot be left floating since these pins do not contain internal resistors. SDET must be tied to VSS or VDDO either directly or through a 4.7 kΩ resistor.

Table 3: PHY Configuration

128-PQFP Package Pin #	Pin Name	Pin Type	Description
108 111	P[1:0]_CONFIG	Input	Port 0 and 1 Configuration. The CONFIG pin is used to set the default configuration for Port 0 and 1 by connecting these pins to other device pins as follows: VSS = Auto-Negotiation enabled - default P0_LED1 = Forced 10BASE-T half-duplex P0_LED2 = Forced 10BASE-T full-duplex P1_LED0 = Forced 100BASE-TX half-duplex P1_LED1 = Forced 100BASE-TX full-duplex P1_LED2 = Forced 100BASE-FX half-duplex VDDO = Forced 100BASE-FX full-duplex Ports 2, 3 and 4's default configuration is Auto-Negotiation enabled. Any port's default configuration can be modified by accessing the PHY registers by a CPU or a serial EEPROM. Fiber vs. copper mode cannot be configured in this way. However, Fiber vs. copper must be selected at reset by using these pins. The CONFIG pins are configured after reset and contain internal pull-down resistors so they can be left floating to select Auto-Negotiation.
106	CONFIG_A	Input	Global Configuration A. This global configuration pin is used to set the default LED mode and Far End Fault Indication (FEFI) mode for 100BASE-FX by connecting these pins to other device pins as follows: VSS = LED Mode 0, FEFI disabled P0_LED0 = LED Mode 0, FEFI enabled P0_LED1 = LED Mode 1, FEFI disabled P0_LED2 = LED Mode 1, FEFI enabled P1_LED0 = LED Mode 2, FEFI disabled P1_LED1 = LED Mode 2, FEFI enabled P1_LED2 = LED Mode 3, FEFI disabled VDDO = LED Mode 3, FEFI enabled - default The LED modes are covered in section 4.7.1 and FEFI is covered in section 4.2.8.3. The CONFIG_A pin is configured after reset and contains an internal pull-up resistor.

Table 3: PHY Configuration (Continued)

128-PQFP Package Pin #	Pin Name	Pin Type	Description
93	CONFIG_B	Input	Global Configuration B. This global configuration pin is used to set the default mode for Auto Crossover, the PHY driver type, and Energy Detect by connecting these pins to other device pins as follows: VSS = No Crossover, Class A[1] drivers, Energy Detect disabled P0_LED0 = No Crossover, Class A drivers, Energy Detect enabled P0_LED1 = No Crossover, Class B[2] drivers, EnergyDetect disabled P0_LED2 = No Crossover, Class B drivers, Energy Detect enabled P1_LED0 = Auto Crossover, Class A drivers, Energy Detect disabled P1_LED1 = Auto Crossover, Class A drivers, Energy Detect enabled P1_LED2 = Auto Crossover, Class B drivers, Energy Detect disabled VDDO = Auto Crossover, Class B drivers, Energy Detect enabled—default Auto crossover is covered in section 4.6, Class B vs. Class A drivers are covered in Table 83 on page 132 and Energy Detect is covered in section Table 71 through Table 74. The CONFIG_B pin is configured after reset and contains an internal pull-up resistor.

1. A Class A driver is available for 100BASE-TX mode only and typically used in backplane or direct connect applications.
2. A Class B driver is typically used in CAT 5 applications.

Table 4: Regulator and Reference

128-PQFP Package Pin #	Pin Name	Pin Type	Description
126	RSETP	Analog	Resistor reference. A 2 kΩ 1% resistor is placed between the RSETP and RSETN. This resistor is used to set an internal bias reference current.
125	RSETN	Analog	Resistor reference. A 2 kΩ 1% resistor is placed between the RSETN and RSETP. This resistor is used to set an internal bias reference current.
124	CONTROL_15	Analog	Voltage control to external 1.5V regulator. This signal controls an external PNP transistor to generate the 1.5V power supply for the VDD and VDDAL pins.
2	CONTROL_25	Analog	Voltage control to external 2.5V regulator. This signal controls an external PNP transistor to generate the 2.5V power supply for the VDDAH pins.

Table 5: System

128-PQFP Package Pin #	Pin Name	Pin Type	Description
104	XTAL_IN	Input	25 MHz or 50 MHz system reference clock input. The frequency of this clock input is selected by the CLK_SEL pin. The clock source can come from a crystal (25 MHz only) or an oscillator (25 or 50 MHz). This is the only clock required as it is used for both the switch and the PHYs.
105	XTAL_OUT	Output	System reference clock output. This output can only be used to drive an external crystal (25 MHz only). It cannot be used to drive external logic. If an oscillator is connected to XTAL_IN this pin should be left unconnected.
68	CLK_SEL	Input	Clock frequency Select. Connect this pin to VSS if XTAL_IN is 25 MHz. Connect this pin to VDDO or leave it unconnected if XTAL_IN is 50 MHz. This pin must be stable before and after reset. CLK_SEL is internally pulled high via a resistor.
110	RESETn	Input	Hardware reset. Active low. The 88E6060 is configured during reset. When RESETn is low all configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or some time after.

Table 6: Register Access Interface

128-PQFP Package Pin #	Pin Name	Pin Type	Description
70	MDC	Input	MDC is the management data clock reference for the serial management interface (SMI). A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz. The SMI is used to access the registers in the PHY and in the Switch if the serial EEPROM is not accessing the registers. It is available in all combinations of SW_MODE[1:0]. MDC is internally pulled high via a resistor.
71	MDIO	I/O	MDIO is the management data Input/Output for the SMI. MDIO is used to transfer management data in and out of the device synchronously with MDC. This pin requires an external pull-up resistor in the range of 4.7 kΩ to 10 kΩ. The 88E6060 device uses 16 of the 32 possible SMI port addresses. The 16 that are used are selectable using the EE_CLK/ADDR4 pin. MDIO is internally pulled high via a resistor.
63	INTn	Open Drain Output	INTn is an active low, open drain pin that is asserted to indicate an unmasked interrupt event occurred. A single external pull-up resistor is required to achieve a logic high when this signal is inactive. The INTn pin is asserted active low if SW_MODE[1:0] (see Table 14) bits are not 0b10 (standalone mode) and the EEPROM data has been completely read into the device. This EEPROM done interrupt indicates to any attached CPU that it may use the MDC/MDIO lines to access the internal registers because the EEPROM has finished using the registers. This pin also goes low when any other unmasked interrupt becomes active inside the device.

Table 7: Serial EEPROM Interface

128-PQFP Package Pin #	Pin Name	Pin Type	Description
61	EE_CS /EE_1K	I/O Input during reset	Serial EEPROM chip select. EE_CS is the serial EEPROM chip select referenced to EE_CLK. It is used to enable the external EEPROM (if present), and to delineate each data transfer. EE_CS is a multi-function pin used to configure the 88E6060 during a hardware reset. When reset is asserted, EE_CS becomes an input and the desired EEPROM type configuration is latched at the rising edge of RESETn as follows: Low = Use 8-bit addresses (for 2K bit 93C56 & 4K bit 93C66) High = Use 6-bit addresses (for 1K bit 93C46) The external EEPROM must be configured in the x16 organization. EE_CS is internally pulled high via a resistor. Use a 4.7 kΩ resistor to VSS for a configuration low.
60	EE_CLK /ADDR4	I/O Output During EEPROM Loading	Serial EEPROM clock. EE_CLK is the serial EEPROM clock reference output by the 88E6060. It is used to shift the external serial EEPROM (if installed) to the next data bit so the default values of the internal registers can be overridden. EE_CLK is a multi-function pin used to configure the 88E6060 during a hardware reset. When reset is asserted, EE_CLK becomes an input and the desired SMI ADDR4 address space configuration (Table 5) is latched at the rising edge of RESETn as follows: Low = Use SMI device addresses 0x00 to 0x0F High = Use SMI device addresses 0x10 to 0x1F EE_CLK is internally pulled high via a resistor. Use a 4.7 kΩ resistor to VSS for a configuration low.

Table 7: Serial EEPROM Interface (Continued)

128-PQFP Package Pin #	Pin Name	Pin Type	Description
69	EE_DIN/ HD_FLOW_DIS	Typically Input Output During EEPROM Loading	Serial EEPROM data into the EEPROM device. EE_DIN is serial EEPROM data referenced to EE_CLK used to transmit the EEPROM command and address to the external serial EEPROM (if present). EE_DIN is a multifunction pin used to configure the 88E6060 during a hardware reset. When reset is asserted, EE_DIN becomes an input and the configured Half-duplex Flow Control disable value is latched at the rising edge of reset as follows: Low = Enable “forced collision” flow control on all half-duplex ports High = Disable flow control on all half-duplex ports EE_DIN is internally pulled high via a resistor. Use a 4.7 kΩ resistor to VSS for a configuration low. FD_FLOW_DIS is used to select flow control on full-duplex ports (see Table 13).
58	EE_DOUT	Input	Serial EEPROM data out from the EEPROM device. EE_DOUT is serial EEPROM data referenced to EE_CLK used to receive the EEPROM configuration data from the external serial EEPROM (if present). EE_DOUT is internally pulled high via a resistor

Table 8: Port 5's Enable

128-PQFP Package Pin #	Pin Name	Pin Type	Description
66	ENABLE_MII5	Input	Enable MII Port 5. This pin is used to enable Port 5. A high enables the Port. A low disables Port 5 (i.e., the drivers are tri-stated). ENABLE_P5 is internally pulled high via a resistor.

Table 9: Port 5's Input MII—If ENABLE_MII5 = High

128-PQFP Package Pin #	Pin Name	Pin Type	Description
82	P5_INCLK	I/O	Input Clock. P5_INCLK is a reference for P5_INDV and P5_IND[3:0]. The direction and speed of P5_INCLK is determined by P5_MODE[3:0] at the end of reset. If the port is in PHY Mode, P5_INCLK is an output. In this mode the frequency of the clock is 25 MHz if the port is in 100BASE-X mode, 2.5 MHz if the port is in 10BASE-T mode and 50 MHz for RMII mode. If the port is in MAC Mode, P5_INCLK is an input. In this mode the frequency of the clock can be anywhere from DC to 25 MHz although it should be 25 MHz for 100BASE-X mode and 2.5 MHz for 10BASE-T mode. P5_INCLK is tri-stated during reset and it is internally pulled high.
83 84 85 86	P5_IND[3:0]	Input	Input Data. P5_IND[3:0] receives the data nibble to be transmitted into the switch in 100BASE-X and 10BASE-T modes. P5_IND[3:0] is synchronous to P5_INCLK. These pins are inputs regardless of the port's mode (i.e., PHY mode or MAC mode). Only P5_IND0 is used when SNI mode is selected. P5_IND[1:0] are used when RMII mode is selected[1]. P5_IND[3:0] are internally pulled high via resistor.
87	P5_INDV	Input	Input Data Valid. When P5_INDV is asserted high, data on P5_IND[3:0] is accepted into the switch. P5_INDV must be synchronous to P5_INCLK for SNI and MII operation. It must be synchronous to P5_OUTCLK or P5_INCLK in RMII operation. P5_INDV is internally pulled low via resistor.

1. When RMII mode is selected P5_IND[1:0] are synchronous to P5_OUTCLK or P5_INCLK which are phase shifted to each other.

Table 10: Port 5's Output MII—If ENABLE_MII5 = High

128-PQFP Package Pin #	Pin Type	Pin Name	Description
79	P5_OUTCLK	I/O	Output Clock. P5_OUTCLK is a reference for P5_OUTDV and P5_OUTD[3:0]. The direction and speed of P5_OUTCLK is determined by P5_MODE[3:0] at the end of reset. If the port is in PHY Mode, P5_OUTCLK is an output. In this mode the frequency of the clock will be 25 MHz if the port is in 100BASE-X mode, and 2.5 MHz if the port is in 10BASE-T mode and 50 MHz for RMII mode. If the port is in MAC Mode, P5_OUTCLK is an input. In this mode the frequency of the clock can be anywhere from DC to 25MHz although it should be 25 MHz for 100BASE-X mode and 2.5 MHz for 10BASE-T mode. P5_OUTCLK is tri-stated during reset and it is internally pulled high.
74 75 76 77	P5_OUTD[3:0] /P5_MODE[3:0]	Normally Output Input only when RESETn is low	Output Data. Data transmitted from the switch is decoded and presented on P5_OUTD[3:0] pins synchronous to P5_OUT_CLK. These pins are outputs regardless of the port's mode (i.e., PHY or MAC mode). Only P5_OUTD0 contains meaningful data when SNI mode is selected. P5_OUTD[1:0] are used when RMII mode[1] is selected. During reset, these internally pulled high pins are tri-stated and used to latch in the required operating mode for the port (see section.3.2.5).
81	P5_OUTDV	Output	Output Data Valid. When P5_OUTDV is asserted high, data transmitted from the switch on P5_OUTD[3:0] is valid. P5_OUTDV is synchronous with P5_OUTCLK in MII mode. When RMII mode is selected, P5_OUTDV can be synchronous to either P5_INCLK or P5_OUTCLK. P5_OUTDV is tri-stated during reset and it is internally pulled high.
72	P5_CRS	I/O	Carrier Sense. After reset, P5_CRS becomes an output if PHY Mode is selected for this port. It remains an input if MAC Mode is selected. P5_CRS asserts (or is expected to be asserted) when the receive data path is non-idle. In half-duplex mode P5_CRS is also asserted (or is expected to be asserted) during transmission. P5_CRS is asynchronous to P5_OUTCLK and P5_INCLK. P5_CRS is tri-stated during reset and it is internally pulled low so the pin can be left unconnected if not used.

1. P5_OUTD[1:0] can be synchronous to either P5_OUTCLK or P5_INCLK, which are phase shifted to each other.

Table 10: Port 5's Output MII—If ENABLE_MII5 = High (Continued)

128-PQFP Package Pin #	Pin Type	Pin Name	Description
73	P5_COL	I/O	Collision. After reset, P5_COL becomes an output if PHY Mode is selected for this port. It remains an input if MAC Mode is selected. In PHY Mode, P5_COL asserts when both the transmit and receive paths are non-idle in both half and full-duplex modes. In half-duplex, MAC mode P5_COL is expected to be asserted when both the transmit and receive paths are non-idle. In full-duplex MAC mode, P5_COL is ignored. P5_COL is asynchronous with P5_OUTCLK and P5_INCLK. P5_COL is tri-stated during reset and it is internally pulled low.

Table 11: Port 4's Enable

128-PQFP Package Pin #	Pin Name	Pin Type	Description
89	DISABLE_MII4	Input	Disable MII Port 4. This pin is used to disable Port 4's MII Interface drivers. A high disables Port 4's MII interface drivers's MII interface (i.e., the drivers are tri-stated) and enables Port 4's PHY interface (its MDI pins). A low enables Port 4's MII Interface and its drivers and disables Port 4's PHY interface. DISABLE_MII4 is internally pulled high via a resistor.

Table 12: Port 4's Input MII—If DISABLE_MII4 = Low

128-PQFP Package Pin #	Pin Name	Pin Type	Description
102	P4_INCLK	I/O	Input Clock. P4_INCLK is a reference for P4_INDV and P4_IND[3:0]. The direction and speed of P4_INCLK is determined by P4_MODE[3:0] at the end of reset. If the port is in PHY Mode, P4_INCLK is an output. In this mode the frequency of the clock will be 25 MHz if the port is in 100BASE-X mode, and 2.5 MHz if the port is in 10BASE-T mode and 50 MHz for RMII mode. If the port is in MAC Mode, P4_INCLK is an input. In this mode the frequency of the clock can be anywhere from DC to 25 MHz although it should be 25 MHz for 100BASE-X mode and 2.5 MHz for 10BASE-T mode. P4_INCLK is tri-stated during reset and it is internally pulled high.
112 114 116 117	P4_IND[3:0]	Input	Input Data. P4_IND[3:0] receives a data nibble to be transmitted into the switch in 100BASE-X and 10BASE-T modes. P4_IND[3:0] is synchronous with P4_INCLK. These pins are inputs regardless of the port's mode (i.e., PHY or MAC mode). Only P4_IND0 is used when SNI mode is selected. P4_IND[1:0] are used when RMII mode is selected[1]. P4_IND[3:0] are internally pulled high via resistor.
118	P4_INDV	Input	Input Data Valid. When P4_INDV is asserted high, data on P4_IND[3:0] is accepted into the switch. P4_INDV must be synchronous to P4_INCLK for SNI and MII operation. It must be synchronous to P4_OUTCLK or P4_INCLK in RMII operation. P4_INDV is internally pulled low via resistor.

1. When RMII mode is selected, P4_IND[1:0] are synchronous to P4_OUTCLK or P4_INCLK, which are phase shifted to each other.

Table 13: Port 4's Output MII—If DISABLE_MII4 = Low

128-PQFP Package Pin #	Pin Name	Pin Type	Description
99	P4_OUTCLK	I/O	Output Clock. P4_OUTCLK is a reference for P4_OUTDV and P4_OUTD[3:0]. The direction and speed of P4_OUTCLK is determined by P4_MODE[3:0] at the end of reset. If the port is in PHY Mode, P4_OUTCLK is an output. In this mode the frequency of the clock will be 25 MHz if the port is in 100BASE-X mode, and 2.5 MHz if the port is in 10BASE-T mode and 50 MHz for RMII mode. If the port is in MAC Mode, P4_OUTCLK is an input. In this mode the frequency of the clock can be anywhere from DC to 25MHz although it should be 25 MHz for 100BASE-X mode and 2.5 MHz for 10BASE-T mode. P4_OUTCLK is tri-stated during reset and it is internally pulled high.
95 96 97 98	P4_OUTD[3:0] /P4_MODE[3:0]	Normally Output Input only when RESETn is low	Output Data. Data transmitted from the switch is decoded and presented on P4_OUTD[3:0] pins synchronous to P4_OUT_CLK. These pins are outputs regardless of the port's mode (i.e., PHY or MAC mode). Only P4_OUTD0 contains data when SNI mode is selected. P4_OUTD[1:0] are used when RMII mode[1] is selected. During reset these internally pulled high pins are tri-stated and used to latch in the desired operating mode for the port (see section 3.2.5).
100	P4_OUTDV	Output	Output Data Valid. When P4_OUTDV is asserted high, data transmitted from the switch on P4_OUTD[3:0] is valid. P4_OUTDV is synchronous with P4_OUTCLK in MII Mode. When RMII mode is selected, P4_OUTDV can be synchronous to either P5_INCLK or P4_OUTCLK. P4_OUTDV is tri-stated during reset and it is internally pulled high.
91	P4_CRS	I/O	Carrier Sense. After reset, P4_CRS becomes an output if PHY Mode is selected for this port. It remains an input if MAC Mode is selected. P4_CRS asserts (or is expected to be asserted) when the receive data path is non-idle. In half-duplex mode P4_CRS is also asserted (or is expected to be asserted) during transmission. P4_CRS is asynchronous to P4_OUTCLK and P4_INCLK. P4_CRS is tri-stated during reset and it is internally pulled low.

1. P4_OUTD[1:0] can be synchronous to either P4_OUTCLK or P4_INCLK, which are phase shifted to each other.

Table 13: Port 4's Output MII—If DISABLE_MII4 = Low (Continued)

128-PQFP Package Pin #	Pin Name	Pin Type	Description
94	P4_COL	I/O	Collision. After reset, P4_COL becomes an output if PHY Mode is selected for this port. It remains an input if MAC Mode is selected. In PHY Mode, P4_COL asserts when both the transmit and receive paths are non-idle in both half and full-duplex modes. In half-duplex, MAC mode P4_COL is expected to be asserted when both the transmit and receive paths are non-idle. In full-duplex MAC mode, P4_COL is ignored. P4_COL is asynchronous to P4_OUTCLK and P4_INCLK. P4_COL is tri-stated during reset and it is internally pulled low.

Table 14: Switch Configuration Interface

128-PQFP Package Pin #	Pin Name	Pin Type	Description
34 33	SW_MODE[1:0]	Input	Switch Mode. These pins are used to configure the 88E6060 after reset. Switch Mode pins work as follows: 1 0 Description 0 0 CPU attached mode – ports come up disabled[1] 0 1 Reserved 1 0 Stand alone mode - ignore EEPROM 1 1 EEPROM attached mode[2] The EEPROM attached mode (when both SW_MODE pins = high) can be used with a CPU. In all but the standalone modes, the INTn pin asserts active low after the EEPROM completes initializing the internal registers (i.e. a halt command has been executed)[3]. SW_MODE[1:0] are not latched on the rising edge of Reset and they must remain static for proper device operation. They are internally pulled high via resistors.
64	FD_FLOW_DIS	Input	Full-duplex Flow Control disable. High = disable flow control on all full-duplex ports Low = enable IEEE 802.3x Pause based flow control on all supported full-duplex ports Full-duplex flow control requires support from the end station. Full-duplex flow control is supported on any full-duplex port that has Auto-Negotiation enabled, advertises that it supports Pause (i.e., FD_FLOW_DIS = Low at reset), and sees that the end station supports Pause as well (from data returned during Auto-Negotiation). If any of these requirements are not met the port does not generate Pause frames and it does not pause when the port receives Pause frames. FD_FLOW_DIS is latched on the rising edge of Reset into all the port's PHY Auto-Negotiation Advertisement registers. It is internally pulled high via a resistor. The EE_DIN/HD_FLOW_DIS multi-function pin is used to select Flow control on half-duplex ports (see Table 7)

1. The ports come up in the Disabled Port State in the CPU mode so the CPU can perform bridge loop detection on link up and/or perform switch initialization/configuration prior to letting packets flow.
2. In EEPROM attached mode the ports come up in the Forwarding Port State unless the Port Control register is overwritten by the EEPROM data.
3. The INTn pin is activated so the CPU can access the registers using the MDC/MDIO pins. The CPU cannot access these registers as long as the EEPROM is still being executed.

Table 15: Port Status LEDs

128-PQFP Package Pin #	Pin Name	Pin Type	Description
39 43 46 50 54	P[4:0]_LED2	Output	Parallel LED outputs – one for each port. This active low LED pin directly drives an LED in Parallel LED mode. It can be configured to display many options. P[4:0]_LED2 are driven active low whenever RESETn is asserted.
40 44 48 51 55	P[4:0]_LED1	Output	Parallel LED outputs – one for each port. This active low LED pin directly drives an LED in Parallel LED mode. It can be configured to display many options. P[4:0]_LED1 are driven active low whenever RESETn is asserted.
41 45 49 53 56	P[4:0]_LED0	Output	Parallel LED outputs – one for each port. This active low LED pin directly drives an LED in Parallel LED mode. It can be configured to display many options. P[4:0]_LED0 are driven active low whenever RESETn is asserted.
36	LEDSER	Output	LEDSER outputs serial status bits that can be shifted into a shift register to be displayed via LEDs. LEDSER is output synchronously to LEDCLK.
38	LEDENA	Output	LEDENA asserts High whenever LEDSER has valid status that is to be stored into the shift register. LEDENA is output synchronously to LEDCLK.
37	LEDCLK	Output	LEDCLK is the reference clock for the serial LED signals.

Table 16: Power and Ground

128-PQFP Package Pin #	Pin Name	Pin Type	Description
47 78 107 123	VDDO	Power	Power to P4 and P5 MIIs, LED, EEPROM, and I/O drivers. VDDO must be connected to 3.3V.
3 14 26	VDDAH	Power	2.5 volt analog power to PHYs
6 11 17 23 29	VDDAL	Power	1.5 volt power to analog core
35 57 65 90 101 113	VDD	Power	1.5 volt power to digital core
1 20 32 42 52 59 67 80 92 103 109 115 128	VSS	Ground	Ground to device
62 88 119 120 121	NC	-	No Connect. These pins must be left unconnected.

1.3 128-Pin LQFP Pin Assignment List—by Signal Name

Table 17: Package Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
68	CLK_SEL
106	CONFIG_A
93	CONFIG_B
124	CONTROL_15
2	CONTROL_25
89	DISABLE_MII4
60	EE_CLK/ADDR4
61	EE_CS/EE_1K
69	EE_DIN/HD_FLOW_DIS
58	EE_DOUT
66	ENABLE_MII5
64	FD_FLOW_DIS
63	INTn
37	LEDCLK
38	LEDENA
36	LEDSER
70	MDC
71	MDIO
62	NC
88	NC
119	NC
120	NC
121	NC
111	P0_CONFIG
56	P0_LED0
55	P0_LED1
54	P0_ LED2
5	P0_RXN
4	P0_RXP
122	P0_SDET
8	P0_TXN
7	P0_TXP

Pin Number	Pin Name
108	P1_CONFIG
53	P1_LED0
51	P1_LED1
50	P1_LED2
12	P1_RXN
13	P1_RXP
127	P1_SDET
9	P1_TXN
10	P1_TXP
49	P2_LED0
48	P2_LED1
46	P2_LED2
16	P2_RXN
15	P2_RXP
19	P2_TXN
18	P2_TXP
45	P3_LED0
44	P3_LED1
43	P3_LED2
24	P3_RXN
25	P3_RXP
21	P3_TXN
22	P3_TXP
41	P4_LED0
40	P4_LED1
39	P4_LED2
28	P4_RXN
27	P4_RXP
31	P4_TXN
30	P4_TXP
73	P5_COL
72	P5_CRS

Pin Number	Pin Name
82	P5_INCLK
86	P5_IND0
85	P5_IND1
84	P5_IND2
83	P5_IND3
87	P5_INDV
79	P5_OUTCLK
77	P5_OUTD0/P5_MODE0
76	P5_OUTD1/P5_MODE1
75	P5_OUTD2/P5_MODE2
74	P5_OUTD3/P5_MODE3
81	P5_OUTDV
94	P4_COL
91	P4_CRS
102	P4_INCLK
117	P4_IND0
116	P4_IND1
114	P4_IND2
112	P4_IND3
118	P4_INDV
99	P4_OUTCLK
98	P4_OUTD0/P4_MODE0
97	P4_OUTD1/P4_MODE1
96	P4_OUTD2/P4_MODE2
95	P4_OUTD3/P4_MODE3
100	P4_OUTDV
110	RESETn
125	RSETN
126	RSETP
33	SW_MODE0
34	SW_MODE1
35	VDD
57	VDD
65	VDD
90	VDD

Pin Number	Pin Name
101	VDD
113	VDD
3	VDDAH
14	VDDAH
26	VDDAH
6	VDDAL
11	VDDAL
17	VDDAL
23	VDDAL
29	VDDAL
47	VDDO
78	VDDO
107	VDDO
123	VDDO
1	VSS
20	VSS
32	VSS
42	VSS
52	VSS
59	VSS
67	VSS
80	VSS
92	VSS
103	VSS
115	VSS
109	VSS
128	VSS
104	XTAL_IN
105	XTAL_OUT

Section 2. Application Examples

The Marvell® 88E6060 device supports many different applications with few additional active components in a small footprint. The 88E6060 contains six ports with five PHYs. This architecture allows all five PHYs to be active and available while at the same time supporting one independent MII interface.

The higher integration, low power, and an extra port saves BOM costs on designs requiring six ports or two MII interfaces. The flexibility of the 88E6060 device comes from its configuration options on Port 0 and Port 1, and its configuration options on its two MII ports (Port 5's MII interface is always on, while Port 4 can be an MII or a PHY). The device also supports an optional EEPROM (93C46 type) to override any of the default settings.

The only active components required to implement a complete 88E6060 10/100 Ethernet switch are:

- 25 MHz crystal clock source or a 25 or 50 MHz oscillator
- Low-cost PNP transistor used to regulate 2.5V down from 3.3V
- Low-cost PNP transistor used to regulate 1.5V down from 3.3V

The 88E6060 is a full system on a chip containing the PHYs, LED drivers, voltage regulator logic, switch logic, and memory. In addition, it is pin compatible with the Marvell® 88E6063 QoS switch.

2.1 Examples with the 88E6060

The 88E6060 has multiple configuration options selectable through four pins: P[1:0]_CONFIG, ENABLE_MII5, and DISABLE_MII4. Table 1 shows Port 0 and Port 1 Copper or Fiber configuration settings, and Port 5 and Port 4 configuration settings. Ports 2, 3, and 4's default configuration is Auto-Negotiation enabled.

Table 18: 88E6060 Port Configuration

P0_CONFIG	P1_CONFIG	ENABLE_MII5	DISABLE_MII4	Port Mode
Low	X	X	X	Port 0 = Copper Auto-Negotiation
High	X	X	X	Port 0 = Fiber Mode
X	Low	X	X	Port 1 = Copper Auto-Negotiation
X	High	X	X	Port 1 = Fiber Mode
X	X	Low	X	Port 5 = Disabled
X	X	High	X	Port 5 = RMII/MII/SNI Mode
X	X	X	Low	Port 4 = RMII/MII/SNI Mode
X	X	X	High	Port 4 = Copper Auto-Negotiation

Each of the following modes are described in detail below:

- Firewall Router Switch w/four 10/100BASE-T LAN ports & one 10/100BASE-T WAN port
- Firewall Router Switch supporting a Fiber WAN port (using port 0 or port 1)
- Firewall Router Switch with four 10/100BASE-T LAN ports & an MII port for a WAN PHY (using port 4)

For the firewall router examples, Port 5 is configured in PHY Mode, and Ports 0 to 4 support 100BASE-TX and/or 10BASE-T operation. Port 0 could be 100BASE-FX if desired as a fiber interface from the WAN (see Figure 3). The CPU's SMI is used to access all the PHY and Switch registers inside the 88E6060.

In Figure 2, Port 0 is used as a WAN interface in the LAN. To make this work, the WAN port needs to be isolated from the LAN ports, and vice versa. LAN frames cannot go directly to the WAN, and WAN frames cannot go directly to the LAN. The CPU's port needs to be the bridge by transmitting, receiving, and translating frames from both the WAN and to and from the LAN. The 88E6060 supports port based VLANs in any programmable configuration that support this requirement and a Marvell header mode supports dynamic VLANs on the CPU's port.

Bringing the 802.3 WAN PHY into the 88E6060's Port 0 not only reduces BOM costs, but it also adds the feature of a 10/100 Mbps interface with Auto Crossover cable support (supported on all copper ports).

Figure 2: 88E6060 Firewall Router Example

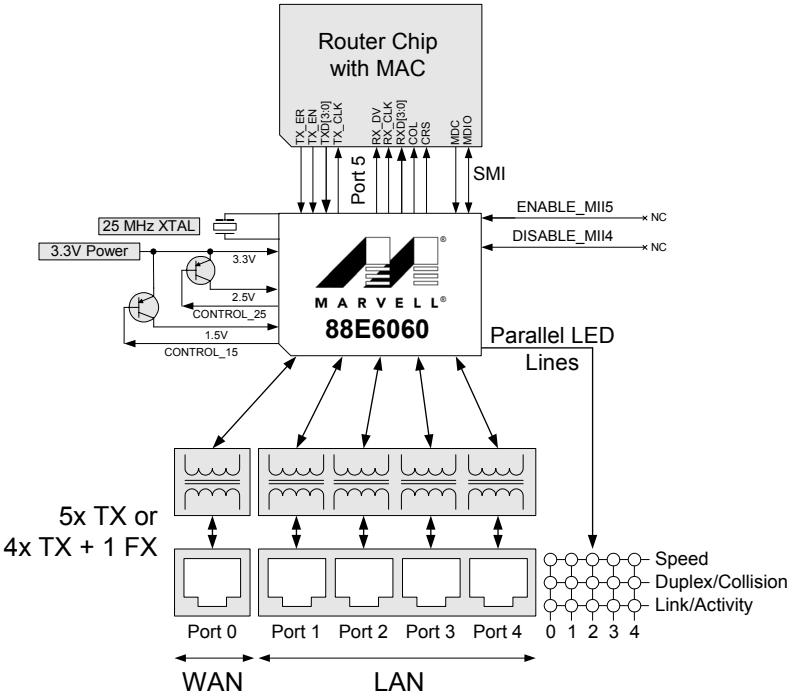


Figure 3: Firewall Router Switch supporting a Fiber WAN port

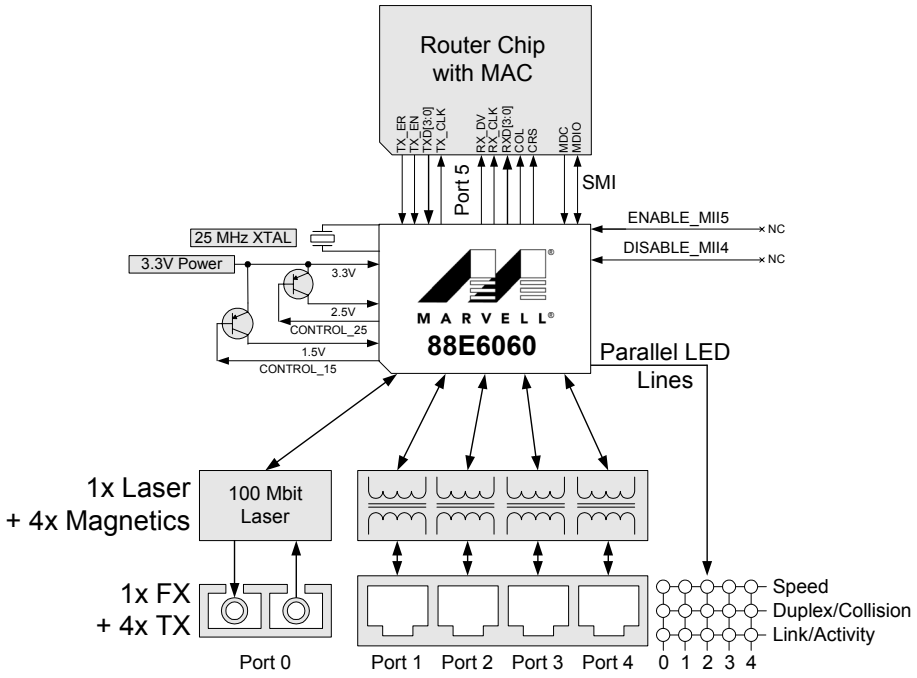
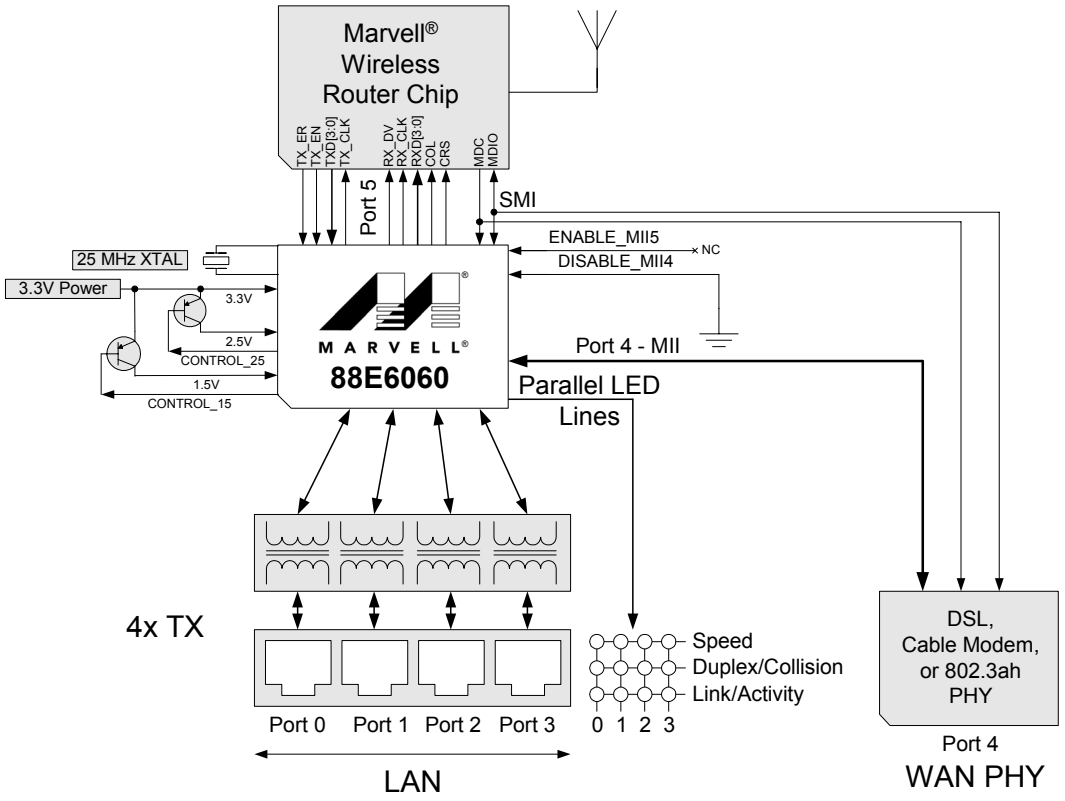


Figure 4: Firewall Router Switch with LAN Ports and WAN PHY



2.2 Routing with the Marvell® Header

The detailed information regarding this feature requires an NDA with Marvell Semiconductor. Please contact your local Marvell Sales Representative for more information.

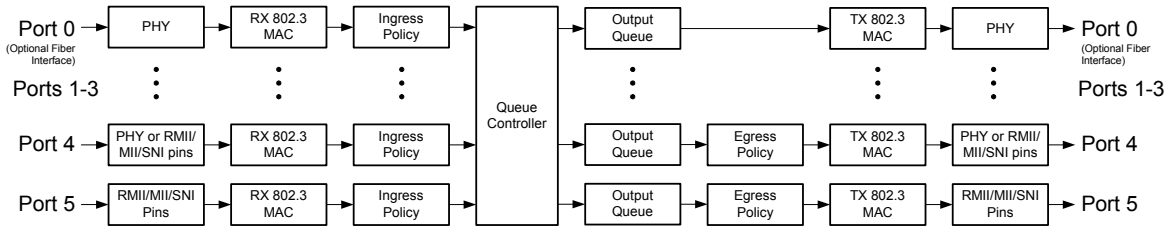
Section 3. Functional Description

This section describes the wire-speed, non-blocking 6-port 10/100-Mbps Fast Ethernet switch core that is integrated into the 88E6060 device. The six ports include PHY, RMII/MII/SNI, and internal MII ports, as described below.

3.1 Switch Data Flow

The 88E6060 device accepts IEEE 802.3 frames and either discards them or transmits them out of one or more of the switchports. The decision on what to do with each frame is one of the many jobs handled inside the switch. Figure 5 shows the data path inside the switch along with the major functional blocks that process the frame as it travels through the 88E6060 device.

Figure 5: 88E6060 Device Switch Data Flow



The PHY, or physical layer interface, is used to receive and transmit frames over CAT 5 twisted pair cable or fiber-optic cables (only Port 0 and Port 1 support a fiber option). The 88E6060 device contains five PHYs connected to Port 0 to Port 4. The PHY block is covered in detail in Section 4.

Port 5 does not contain PHYs. Instead, a short distance industry standard digital interface is supported and generically called the port's Media Independent Interface (MII see "MII/SNI/RMII" on page 41). Many interface modes and timings are supported so that a large number of external device types can be used.

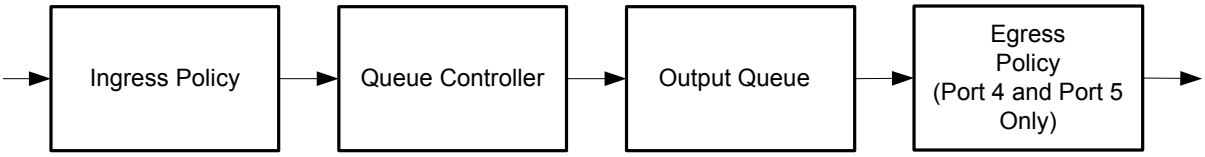
The two MIIs (Port 4 can be MII or PHY) on the 88E6060 support four major modes of operation and each Media Independent Interface (MII) can be configured independently.

The 88E6060 contains six independent MACs (Section 3.3) that perform all of the functions in the 802.3 protocol:

- Frame formatting
- CRC checking
- CSMA/CD enforcement
- Collision handling

The switch portion of the 88E6060 receives good packets from the MACs, processes them, and forwards them to the appropriate MACs for transmission. Processing frames is the key activity, and it involves the Ingress Policy, the Queue Controller, the Output Queues, and the Egress Policy blocks shown in Figure 6. The Egress Policy block is only applicable to the MII ports (Port 4 and Port 5). These blocks modify the normal or default packet flow through the switch and are discussed in section 3.5 to section 3.7.

Figure 6: Switch Operation



3.2 MII/SNI/RMII

The Media Independent Interface (MII) supports four major modes of operation:

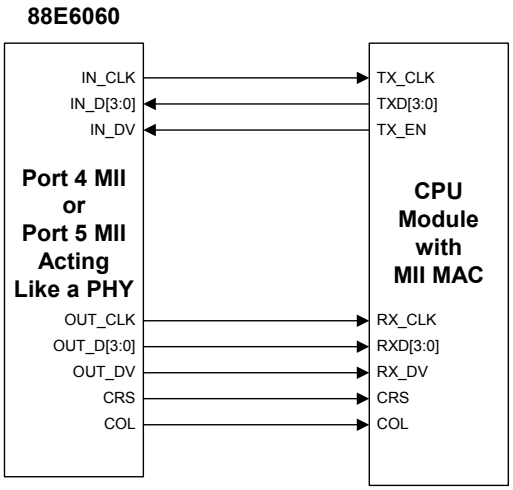
- MII PHY Mode (The 88E6060 device drives the interface clocks - see Section 3.2.1 for details.)
- MII MAC Mode (The external device drives the interface clocks - see Section 3.2.2 for details.)
- SNI PHY Mode
- RMII PHY Mode

The two MII ports can be configured differently from each other.

3.2.1 MII PHY Mode

The MII PHY Mode (Reverse MII) configures the selected MAC inside the 88E6060 device to emulate a PHY. This enables the 88E6060 device to be directly connected to an external MAC (for example, one inside a Router CPU). In this mode, the 88E6060 device drives the interface clocks (Px_INCLK and Px_OUTCLK); therefore, the required frequency needs to be selected. Both full-duplex and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII PHY interface is compliant with the IEEE 802.3u clause 22.

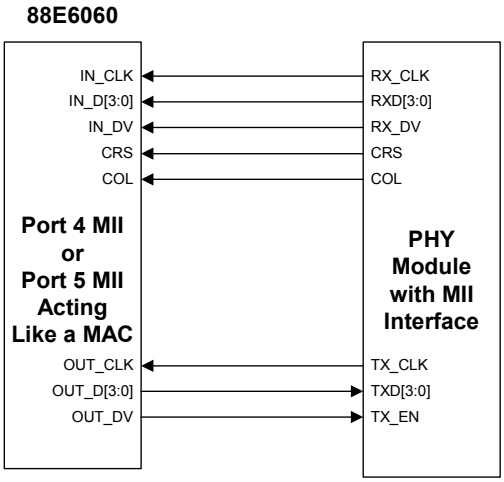
Figure 7: MII PHY Interface Pins



3.2.2 MII MAC Mode

The MII MAC Mode (Forward MII) configures the desired MAC inside the 88E6060 device to act as a MAC so that it can be directly connected to an external PHY. In this mode, the 88E6060 device receives the interface clocks (Px_INCLK and Px_OUTCLK) and works at any frequency from DC to 25 MHz. The two clocks can be asynchronous with respect to each other. Both full-duplex and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII MAC interface is compliant to the IEEE 802.3u clause 22.

Figure 8: MII MAC Interface Pins

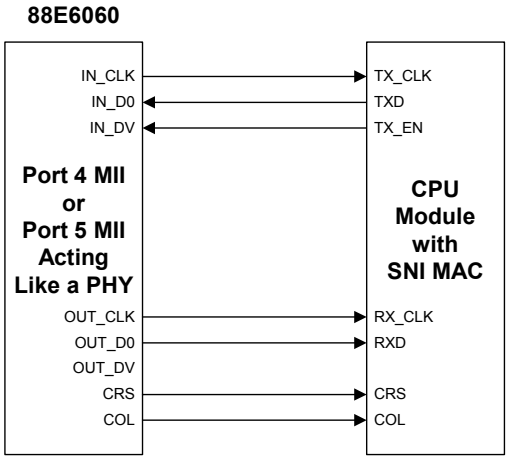


3.2.3 SNI PHY Mode

The SNI PHY Mode (7-Wire interface) configures the selected MAC inside the 88E6060 device to act as a 10 Mbps PHY, enabling it to be directly connected to an external 10 Mbps-only MAC (such as one inside a Router CPU). In this mode, only one data bit is used on each of input and output (Px_IND0 and Px_OUTD0). The interface clocks, Px_INCLK and Px_OUTCLK, are driven by the 88E6060 device. Since SNI was never standardized, the 88E6060 device supports various SNI modes. The active edge of the clock (either rising or falling) and the active level on the collision signal (either active high or low) can be selected.

In SNI mode, the output data from the switch is indicated to be valid by the CRS signal. CRS is not synchronous with OUT_CLK, however. So the receiving MAC needs to detect the beginning of the frame by looking for the Preamble and then the Start of Frame Delimiter (SFD). CRS will be deasserted asynchronously at the end of the frame so the receiving MAC needs to tolerate the presence of these extra 'dribble' bits

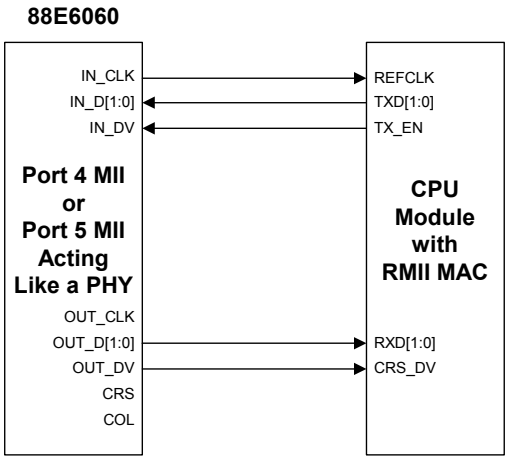
Figure 9: SNI PHY Interface Pins



3.2.4 RMII PHY Mode

RMII PHY Mode (Reduced MII) configures the selected MAC inside the 88E6060 device to act as a 100 Mbps PHY with a Reduced Media Independent Interface (RMII) enabling it to be directly connected to an external 100 Mbps RMII MAC (for example, one inside an ASIC or FPGA). In this mode, only two data bits are used on each of input and output (Px_IND[1:0] and Px_OUTD[1:0]). The interface clock (Px_INCLK) is driven by the 88E6060 device at the RMII constant frequency of 50 MHz.

Figure 10: RMII PHY Interface Pins using INCLK



3.2.5 RMII/MII/SNI Configuration

MII/SNI/RMII interfaces in the 88E6060 device are configured at the rising edges of RESETn. During reset the Px_OUTD[3:0]/Px_MODE[3:0] pins become tri-stated, and the values found on these pins become the interface's mode as defined in Table 19.

Table 19: RMII/MII/SNI Configuration Options

Px_ MODE[3:0] (at Reset)	PHY/ MAC Mode	Duplex	MII/SNI Mode	Description
0 0 0 0	PHY	Half-Duplex	SNI 10 Mbps	Rising edge clock with collision active low
0 0 0 1	PHY	Half-Duplex	SNI 10 Mbps	Rising edge clock with collision active high
0 0 1 0	PHY	Full-Duplex	SNI 10 Mbps	Rising edge clock (collision is don't care)
0 0 1 1	MAC	Full-Duplex	Reserved	Reserved for future use
0 1 0 0	PHY	Half-Duplex	SNI 10 Mbps	Falling edge clock with collision active low
0 1 0 1	PHY	Half-Duplex	SNI 10 Mbps	Falling edge clock with collision active high
0 1 1 0	PHY	Full-Duplex	SNI 10 Mbps	Falling edge clock (collision is don't care)
0 1 1 1	PHY	Full-Duplex	Reserved	Reserved for future use.
1 0 0 0	MAC	Half-Duplex	MII 0 -100 Mbps	DC to 25 MHz MII input clock mode
1 0 0 1	PHY	Half-Duplex	RMII 100 Mbps	50 MHz Reduced MII output clock mode
1 0 1 0	MAC	Full-Duplex	MII 0 -100 Mbps	DC to 25 MHz MII input clock mode
1 0 1 1	PHY	Full-Duplex	RMII 100 Mbps	50 MHz Reduced MII output clock mode
1 1 0 0	PHY	Half-Duplex	MII 10 Mbps	2.5 MHz MII output clock mode
1 1 0 1	PHY	Half-Duplex	MII 100 Mbps	25 MHz MII output clock mode
1 1 1 0	PHY	Full-Duplex	MII 10 Mbps	2.5 MHz MII output clock mode
1 1 1 1	PHY	Full-Duplex	MII 100 Mbps	25 MHz MII output clock mode

3.2.6 Enabling the RMII/MII/SNI Interfaces

Port 5 (the 6th port) is enabled when ENABLE_MII5 is tied high to VDDO. Port 4's MII is enabled when DISABLE_MII4 is tied to VSS.

3.2.7 Port Status Registers

Each switch port of the 88E6060 device has a status register that reports information about that port's PHY or RMII/MII/SNI interface. See Section 6.2.1 "Switch Core Register Map" for more information.

3.3 Media Access Controllers (MAC)

The 88E6060 device contains six independent MACs that perform all of the functions in the 802.3 protocol that include, among others, frame formatting, frame stripping, FCS checking, CSMA/CD enforcement, and collision handling.

Each MAC receive block checks incoming packets and discards packets with CRC errors, alignment errors, short packets (less than 64 bytes), or long packets (more than 1522 bytes)[1]. Each MAC constantly monitors its receive lines waiting for preamble bytes followed by the Start of Frame Delimiter (SFD). The first six bytes after the SFD are used as the packet's Destination Address (DA), and the next six bytes are used as the packet's Source Address (SA). These two addresses are fundamental to the operation of the switch (see section 3.4). The last four bytes of the packet contain the packet's Frame Check Sequence (FCS). The packet is discarded if the FCS does not meet the IEEE 802.3 CRC-32 requirements.

Before a packet can be sent out, the transmit block must check whether the line is available for transmission. The transmit line is available all the time when the port is in full-duplex mode, but the line could be busy receiving a packet when the port is in half-duplex mode. In this case, the transmitter defers its transmission until the line becomes available, when it ensures that a minimum interpacket gap of at least 96 bits occurs before transmitting a 56-bit preamble and an 8-bit Start of Frame Delimiter (SFD) ahead of the basic frame. Transmission of the frame begins immediately after the SFD.

For the half-duplex mode, the 88E6060 device also monitors the collision signal while it is transmitting. When a collision is detected (i.e., both transmitter and receiver of a half-duplex MAC are active at the same time), the MAC transmits a JAM pattern and then delays the retransmission for a random time period determined by the IEEE 802.3 backoff algorithm. In full-duplex mode, the collision signal and backoff algorithm are ignored.

3.3.1 Backoff

In half-duplex mode, the 88E6060 device's MACs implement the truncated binary exponential backoff algorithm defined in the IEEE 802.3 standard. This algorithm starts with a randomly-selected small backoff time and follows by generating progressively longer random backoff times. The random times prevent two or more MACs from always attempting re-transmission at the same time. The progressively longer backoff times give a wider random range at the expense of a longer delay, giving congested links a better chance of finding a winning transmitter. Each MAC in the 88E6060 device resets the progressively longer backoff time circuit after 16 consecutive retransmit trials. Each MAC then restarts the backoff algorithm with the shortest random backoff time and continues to retry and retransmit the frame. A packet that successively collides with a retransmit signal is re-transmitted until transmission is successful. This algorithm prevents packet loss in highly-congested environments. The MACs in the switch can be configured to meet the IEEE 802.3 specification and discard a frame after 16 consecutive collisions instead of restarting the backoff algorithm. To discard a frame after 16 consecutive collisions, set the DiscardExcessive bit to a one in the Global Control register—see Table 53.

3.3.2 Half-Duplex Flow Control

Half-duplex flow control is used to throttle the end station to avoid dropping packets during network congestion. It is enabled on all half-duplex ports when the EE_DIN/HD_FLOW_DIS pin is low at the rising edge of RESETn. The 88E6060 device uses a collision-based scheme to perform half-duplex flow control. When the free buffer space is almost exhausted, the MAC forces a collision in the input port when the 88E6060 device senses an incoming packet. Only those ports that are involved in the congestion are flow controlled. When the half-duplex flow control mode is not set and no packet buffer space is available, the incoming packet is discarded.

1. A maximum frame size of 1536 bytes is supported by setting the MaxFrameSize bit in the Global Control register (section 6.2.3).

3.3.3 Full-Duplex Flow Control

The purpose of full-duplex flow control is the same as that of flow control in the half-duplex case—to avoid dropping packets during congestion. Full-duplex flow control is enabled on all full-duplex ports when:

- FD_FLOW_DIS pin is low at the rising edge of RESETn, and
- Auto-Negotiation is enabled on the port (see section 4.2.13), and
- The link partner 'advertises' that it supports pause during Auto-Negotiation[1]

Full-duplex flow control is not automatically supported on Ports 0–1 when configured for 100BASE-FX operation, nor for Port 5 and Port 4 when it is in MII mode. This is because Auto-Negotiation is not defined for 100BASE-FX or MII. Therefore, the link partners cannot advertise that they support Pause. It can be forced, however—see section 3.3.4. When the full-duplex flow control mode is not set and no packet buffer space is available, the incoming packet is discarded.

In full-duplex mode, the 88E6060 MACs support the standard flow control defined in the IEEE 802.3x specification. This flow control enables stopping and restoring the transmission from the remote node. The basic mechanism for performing full-duplex flow control is by means of a Pause frame. The format of the Pause frame is shown in Table 20.

Table 20: Pause Frame Format

Destination Address (6 Bytes)	Source Address (6 Bytes)	Type (2 Bytes)	Op Code (2 Bytes)	Pause Time (2 Bytes)	Padding (42 Bytes)	FCS (4 Bytes)
01-80-C2-00-00-01	See text	88-08	00-01	See text	All zeros	Computed

Full-duplex flow control functions as follows. When the free buffer space is almost exhausted, the 88E6060 device sends out a Pause frame with the maximum Pause time (a value of all ones—0xFFFF) to stop the remote node from sending more frames into the switch. Only the node that is involved in the congestion is Paused. When the event that invoked flow control disappears, the 88E6060 device sends out a Pause frame with the Pause time equal to zero, indicating that the remote node can resume transmission. The 88E6060 device also responds to the Pause command in the MAC receiving block. When the Pause command is detected, the MAC responds within one slot time (512 bit times) to stop transmission of the new data frame for the amount of time defined in the pause time field of the Pause command packet.

The Source Address of received Pause frames is not learned (see Address Learning in section 3.4.3) since it may not represent the Source Address of the transmitting port. This is generally the case if the link partner is an unmanaged switch. The 88E6060 device can be configured to transmit a unique Source Address on Pause frames (the default is all zeros). Global Switch MAC Address registers 1, 2, and 3 (see Table 50, Table 51, and Table 52) can be set to the Source Address to use. A single fixed Source Address can be used for all ports, or a unique Source Address per port can be selected by changing the value of the DiffAddr bit in Table 50.

The MACs always discard all IEEE 802.3x Pause frames that they receive, even when full-duplex flow control is disabled or even when the port is in half-duplex mode.

1. Full-duplex flow control is not automatically supported on ports configured for 100BASE-FX operation since Auto-Negotiation is not defined for 100BASE-FX, and hence, the link partners cannot advertise that they support Pause. It can be forced, however – see section 3.3.4.

3.3.4 Forcing Flow Control

When flow control is enabled using the 88E6060 device's pins, it is enabled for all ports of the same type (i.e., on all half-duplex ports or on all full-duplex ports that have a flow-controllable link partner). It may be required to have flow control enabled on only one or two ports and have all the other ports disabled. In this case, flow control should be disabled using the appropriate device pins. Refer to the FD_FLOW_DIS and HD_FLOW_DIS pin descriptions for disabling flow control then use the port's ForceFlowControl bit in the Port Control Register for enabling flow control on individual ports. (see section 6.2.2).

3.3.5 Statistics Counters

Sometimes it is necessary to debug network occurrences. For example, a technician may want to view the network remotely to solve a customer problem or a software programmer may want to trace transmitted frames. In these situations, two basic types of data are important:

- Number of good frames entering and leaving each port of the switch
- Quality of network segment performance

Frame size and the distribution of frames between multicast and unicast types are less important in this kind of debugging for an edge switch.

The 88E6060 Statistics Counters support basic debugging needs. Each port can capture two kinds of statistics:

- A count of the number of good frames received with the number of frames transmitted, or
- A count of the number of bad frames received with the number of collisions encountered

The first statistic answers the question "Where did all the frames go?", while the second statistic answers the question "Does the network segment have any performance problems?". These counters are described in Table 47, and in Table 48. The counters can be cleared, and their mode chosen by the CtrMode bit in the Switch Global Control register (section 6.2.3).

3.4 Address Management

The primary function of the switch portion of the 88E6060 device is to receive good packets from the MACs, processes them, and forward them to the appropriate MACs for transmission. This frame processing involves the Ingress Policy, Queue Controller, Output Queues, and Egress Policy blocks shown in Figure 6. These blocks modify the normal or default packet flow through the switch and are discussed following section 3.5. The normal packet flow and processing is discussed first.

The normal packet flow involves learning how to switch packets only to the correct MACs. The switch learns which port an end station is connected to by remembering each packet's Source Address along with the port number on which the packet arrived.

When a packet is directed to a new, currently unlearned MAC address, the packet is transmitted out of all of the ports[1] except for the one on which it arrived[2]. Once a MAC address/port number mapping is learned, all future packets directed to that end station's MAC address (as defined in a frame's Destination Address field) are directed to the learned port number only. This ensures that the packet is received by the correct end station (if it exists), and when the end station responds, its address is learned by the switch for the next series of packets.

Owing to the limitation of physical memory, switches learn only the currently "active" MAC addresses—a small subset of the 2^{48} possible MAC addresses. When an end station is moved from one port to another, a new MAC address/port number association must be learned, and the old one replaced. These issues are handled by the 'Aging' and 'Station Move Handling' functions. A MAC address/port number association is allowed to be "active" for only a limited time. This time limit is typically set to five minutes.

3.4.1 Address Translation Unit

The 88E6060 device's Lookup Engine or Address Translation Unit (ATU) gets the DA and SA from each frame received from each port. It performs all address searching, address learning, and address aging functions for all ports at wire speed rates. For example, a DA and an SA lookup/learn function can be performed for all ports in less time than it takes to receive a 64-byte frame on all ports.

The address database uses a hashing technique for quick storage and retrieval. Hashing a 48-bit address into fewer bits results in some MAC addresses having the same hash address. This situation is called a hash collision and is solved in the 88E6060 device by using a four entry bin per hash location that can store up to four different MAC addresses at each hash location. The four-entry bin is twice as deep as that of many competing switching devices and allows for a reduced size of the address database while still holding the same number of active random value MAC addresses.

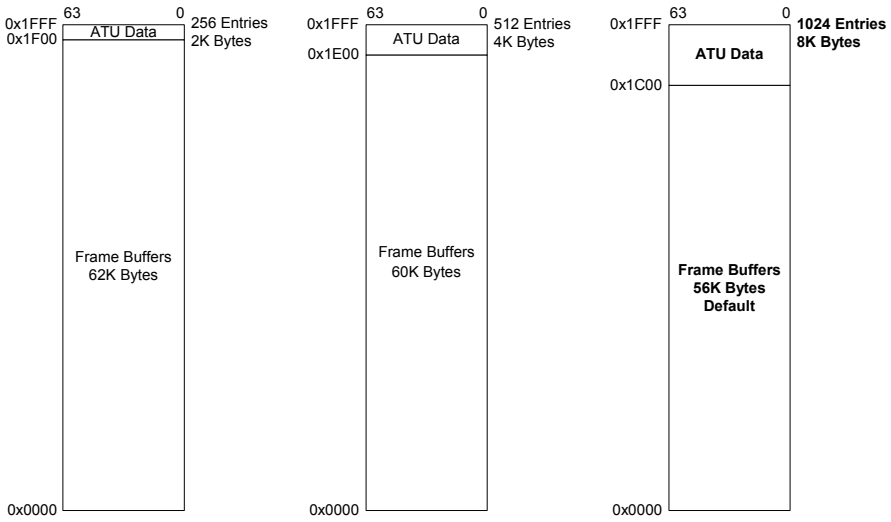
The address database is stored in the embedded SRAM and has a default size of 1024 entries with a default aging time of about 300 seconds or 5 minutes. The size of the address database can be modified to a maximum of 256, 512, or 1024 entries. Decreasing the size of the address database increases the number of buffers available for frames (see Figure 11). The age time can be modified in 16 second increments from 0 seconds (aging disabled) to 4080 seconds (or 68 minutes). These options are set in the ATU Control register (Table 54).

Note

Changing the ATU size will result in ATU reset and SWReset. SWReset will reset the MAC, and the Port State bits will be set back to their configuration reset value. The ATU Reset will reset the entire ATU database. See ATUSize and SWReset register descriptions in Table 54.

1. Port-based VLANs modify this operation (section 3.5.1).
2. The 88E6060 device can be configured to transmit frames out the same port that they came in on—see Table 45.

Figure 11: ATU Size Tradeoffs



3.4.2 Address Searching or Translation

The address search engine searches the address database to get the output port number(s), called the Destination Port Vector (DPV), for each frame's Destination Address (DA). When an address is found, it can switch the frame instead of flooding it. If the destination address is not found, then the packet is flooded. Flooding refers to the action of sending frames out to all the ports of the switch that have link up with PortState not "Disabled", except for the port the frame came in on. The switch arbitrates destination address lookup requests from the ports and grants one lookup at a time. The MAC address is hashed, and then data is read from the SRAM table and compared to the MAC address for a match. Four different addresses can be stored at each hash location. When a match is found, the Address Translation Unit (ATU) returns the DPV to the Ingress Policy block where it may get modified before the packet is queued to the output port(s). The DPV returned from the ATU may get modified by the VLANTable data. When no MAC address match is found, the Ingress Policy block uses a unique default DPV for each Ingress port, which typically floods the frame. The default DPV for each port is the Port's VLANTable data – see Table 45. When the destination address in the frame is a multicast address or broadcast address, the address is searched in the same way as a unicast address, and the frame is processed identically. Multicast addresses cannot be learned, so they appear in the address database only when they are loaded into it by a CPU or the EEPROM – see section 3.4.5.3. This feature is used for multicast filtering and Bridge Protocol Data Unit (BPDU) handling. BPDU frames are special frames used for Spanning Tree or bridge loop detection.

Multiple separate address databases are supported in the 88E6060 device. The database that is searched is controlled by the port's default database number (DBNum - Table 45). MAC addresses that are not members of the port's DBNum cannot be found.

3.4.3 Address Learning

The address learning engine learns source addresses of incoming frames. Up to 1024 MAC address/port number mappings can be stored in the address database. See section 3.4.1. When the source address from an input frame cannot be found in the address database, the ATU enters the self-learning mode, places the new MAC address/port number mapping into the database, and refreshes its Age time. The Age time on a MAC Address entry is refreshed by setting its Entry_State field to 0xE. When the MAC address is already in the database, the port number[1] and Age associated with the entry is updated and/or refreshed. The port number is updated in case the end station has moved, and the port number needs to be corrected. The entry's Age is refreshed since the MAC address is still "active". This refreshing prevents the MAC address/port number mapping from being prematurely removed as being "inactive".

When an address is added into the database it is hashed and then stored in the 1st empty bin found at the hashed location. When all four address bins are full, a "least recently used" algorithm is used to scan each entry's Age time in the Entry_State field. The Entry_State field is described in section 3.4.5.1. When all four address bins have the same Age time, then the 1st unlocked bin is used (see section 3.4.5.1 for more information about locked or static addresses). If all four bins are locked then the address is not learned and an ATUFull interrupt is generated. See the Switch Global Status register – Table 49.

Multiple separate address databases are supported in the 88E6060 device. The port's database number (DBNum - Table 45) determines the MAC address database into which the learned address is stored. The same MAC address can be learned multiple times with different port mappings if different DBNum values are used.

Learning can be disabled for all ports by setting the LearnDis bit to a one in the ATU Control register (Table 54). Learning is disabled on any port that has a PortState of Disabled or Blocking/Listening (see the Port Control register—Table 44) or whose Port Association Vector (PAV bit — Table 46) is cleared to a zero.

3.4.4 Address Aging

Address aging makes room for new active addresses by ensuring that when a node is disconnected from the network segment or when it becomes inactive, its entry is removed from the address database. An address is removed from the database after a predetermined interval from the time it last appeared as an Ingress frame's source address (SA). This interval is programmable in the 88E6060 device. The default Aging interval is about 5 minutes (282 to 304 seconds), but it can be set from 0 seconds (i.e., aging is disabled) to 4,080 seconds in 16 second increments. See AgeTime in ATU Control register—see Table 54.

The 88E6060 device runs the address aging process continuously unless disabled by clearing the AgeTime field in the ATU Control register to zero. Aging is accomplished by a periodic sweeping of the address database. The speed of these sweeps is determined by the AgeTime field. On each aging sweep of the database, the ATU reads each valid entry and updates its Age time by decrementing its Entry_State field as long as the entry is not locked. The Entry_State field is described in section 3.4.5.1. When the Entry_State field reaches zero, the entry is considered invalid and purged from the database.

The time taken to age out any entry in the MAC address database is a function of the AgeTime value in the ATU Control register and the value in the Entry_State field. A new or just-refreshed unicast MAC address has an Entry_State value of 0xE. See section 3.4.2. A purged or invalid entry has an Entry_State value of 0x0. The values from 0xD to 0x1 indicate the Age time on a valid unicast MAC address with 0x1 being the oldest. This scheme provides 14 possible age values in the Entry_State field which increases precision in the age of entries in the MAC address database. This precision is relayed to the "least recently used" algorithm that is employed by the address

1. The port's Port Association Vector (PAV - Table 46) is used as the port's port vector when an address is auto learned or updated.

learning process. An address is purged from the database within 1/14th of the programmed AgeTime value in the ATU Control register.

3.4.5 Address Translation Unit Operations

The ATU in the 88E6060 device supports user commands to access and modify the contents of the MAC address database.

All ATU operations have the same user interface and protocol. Five Global registers are used and are shown in Table 21 on page 52. The protocol for an ATU operation is as follows:

1. Ensuring the ATU is available by checking the ATUBusy bit in the ATU Operation register. The ATU can only perform one user command at a time.
2. Loading the ATU Data and ATU MAC registers, if required by the operation.
3. Starting the ATU operation by defining the DBNum, ATUOp, and setting the ATUBusy bit to a one in the ATU Operation register. The DBNum, ATUOp and the ATUBusy bits setting can be done at the same time.
4. Waiting for the ATU operation to complete. Completion can be verified by polling the ATUBusy bit in the ATU Operation register or by receiving an ATUDone interrupt. See Switch Global Control register Table 53 and Switch Global Status register, Table 49.
5. Reading the results, if appropriate.

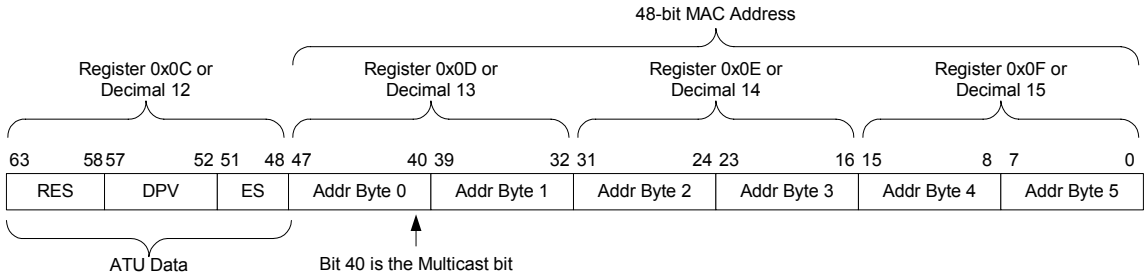
Table 21: ATU Operations Registers

Register	Offset	Section	Before the Operation Starts	After the Operation Completes
ATU Operation	0x0B or Decimal 11	Table 55	Used to define the required operation (including which database to search, i.e., the DBNum field) and start it.	Used to indicate the ATU's Busy status.
ATU Data	0x0C or Decimal 12	Table 56	Used further to define the required operation and used as the required ATU Data that is to be associated with the MAC address below.	Returns the ATU Data that is associated with the resulting MAC address below.
ATU MAC (3 registers)	0x0D to 0x0F or Decimal 13 to 15	Table 57	Used to define the required MAC address upon which to operate	Returns the resulting MAC address from the required operation.

3.4.5.1 Format of the ATU Database

Each MAC address entry in the ATU database is 64 bits in size. The lower 48 bits contain the 48-bit MAC address, and the upper 16 bits contain information about the entry as shown in Figure 12. The database is accessed 16 bits at a time via the Switch Global registers shown in the figure. For more information about these registers, see ATU MAC Switch Address registers, Table 57 through Table 59.

Figure 12: Format of an ATU Entry



The upper 16 bits of the ATU entry are called the ATU Data which are separated into three fields—see ATU Data Fields,Table 22 and ATU DATA register, Table 56.

Table 22: ATU Data Fields

Field	Bits	Description
Entry_State	51:48	The Entry_State field, together with the entry's Multicast bit (bit 40) is used to determine the entry's age or its type as follows: For unicast MAC addresses (bit 40 = 0): 0x0 = Invalid, empty, or purged entry. 0x1 to 0xE = Valid entry where the Entry_State = the entry's age, and the DPV indicates the port or ports mapped to this MAC address. 0xF = Valid entry that is locked and does not age. The DPV indicates the port or ports mapped to this MAC address. For multicast MAC addresses (bit 40 = 1): 0x0 = Invalid, empty, or purged entry. 0x7 = Valid entry that is locked does not age. The DPV indicates the port or ports mapped to this MAC address. Used for multicast filtering. 0xE = Valid entry that is locked and does not age. The DPV indicates the port or ports mapped to this MAC address. Frames with a MAC address that return this Entry_State are considered MGMT (management) frames and are allowed to tunnel through blocked ports (see section 3.5). Used for BPDU handling.
DPV	57:52	The Destination Port Vector. These bits indicate which port or ports are associated with this MAC address (i.e., where frames should be switch to) when they are set to a one. A DPV of all zeros indicates frames with this DA should be discarded. Bit 52 is assigned to physical Port 0, 53 to Port 1, 54 to Port 2, 55 to Port 3, and so on.
Reserved	63:58	Reserved for future use.

3.4.5.2 Reading the Address Database - the Get Next Operation

The contents of the address database can be dumped or searched. The Get Next operation returns the active contents of the address database in ascending network byte order. A search operation can also be done using the Get Next operation. If multiple address databases are being used, the Get Next function returns all unique MAC addresses from the selected database.

The Get Next operation starts with the MAC address contained in the ATU MAC registers and returns the next higher active MAC address currently active in the address database. Use an ATU MAC address of all ones to get the first or lowest active MAC address. The returned MAC address and its data is accessible in the ATU MAC and the ATU Data registers. To get the next higher active MAC address, the Get Next operation can be started again without setting the ATU MAC registers since they already contain the 'last' address. A returned ATU MAC address of all ones indicates that the end of the database has been reached[1]. A summary of how the Get Next operation uses the ATU's registers is shown in Table 23.

Table 23: ATU Get Next Operation Register Usage

Register	Offset	Section	Before the Operation Starts	After the Operation Completes
ATU Operation	0x0B or Decimal 11	Table 55	Used to define the required operation (including which database to search, i.e., the DBNum field) and start it.	Used to indicate the ATU's Busy status.
ATU Data	0x0C or Decimal 12	Table 56	Ignored.	Returns the ATU Data that is associated with the resulting MAC address below. If Entry_State = 0x0 the returned data is not a valid entry.
ATU MAC (3 registers)	0x0D to 0x0F or Decimal 13 to 15	Table 57 through Table 59	Used to define the starting MAC address to search. Use an address of all zeros to find the first or lowest MAC address. Use the last address to find the next address. There is no need to write to this register in this case.	Returns the next higher active MAC address if found, or all ones are returned indicating the end of the table has been reached.

To search for a particular MAC address, start the Get Next operation with a MAC address numerically one less than the particular MAC address using the DBNum of the selected database to search. When the searched MAC address is found, it is returned in the ATU MAC registers along with its associated data in the ATU Data register. When the searched MAC address is not found active, then the ATU MAC registers will not equal the required searched address.

3.4.5.3 Loading and Purging an Entry in the Address Database

Any MAC address (unicast or multicast) can be loaded into, or removed from, the address database by using the Load operation. An address is loaded into the database if the Entry_State in the ATU Data register (Table 56) is non-zero. A value of zero indicates the required ATU operation is a purge.

1. When the returned MAC address is all ones, it always indicates that the end of the table has been reached. If the returned Entry_State bits are non-zero, it also indicates that the MAC address of all ones is active in the database.

The load operation searches the address database indicated by the database number, DBNum (in the ATU Operation register), for the MAC address contained in the ATU MAC registers. When the address is found, it is updated by the information found in the ATU Data register.

Note

A load operation becomes a purge operation when the ATU Data's Entry_State equals zero. Also, locked addresses can be modified without their needing to be purged first.

If the address is not found and if the ATU Data's Entry_State does not equal zero, the address is loaded into the address database using the same protocol as is used by automatic Address Learning. See section 3.4.3. The 16 bits of the ATU Data register are written into bits 63:48 of the ATU entry. See section 3.4.5.1.

A summary of how the Load operation uses the ATU's registers is shown in Table 24.

Table 24: ATU Load/Purge Operation Register Usage

Register	Offset	Section	Before the Operation Starts	After the Operation Completes
ATU Operation	0x0B or Decimal 11	Table 55	Used to define the required operation (including which database to load or purge, i.e., the DBNum field) and start it.	Used to indicate the ATU's Busy status.
ATU Data	0x0C or Decimal 12	Table 56	Used to define the associated data that is loaded with the MAC address below. When Entry_State = 0, the load becomes a purge.	No change.
ATU MAC (3 registers)	0x0D to 0x0F or Decimal 13 to 15	Table 57 through Table 59	Used to define the MAC address to load or purge.	No change.

3.4.5.4 Flushing Entries

All MAC addresses, or just the unlocked MAC addresses, can be purged from the entire set of address databases or from just a particular address database using single ATU operations. These ATU operations are:

- Flush all Entries
- Flush all Unlocked Entries
- Flush All Entries in a particular DBNum Database
- Flush all Unlocked Entries in a particular DBNum Database

The ATU Data and ATU MAC Address registers are not used for these operations and they are left unmodified.

The DBNum field of the ATU Operation register is used for the Flush operations that require a database number to be defined.

3.5 Ingress Policy

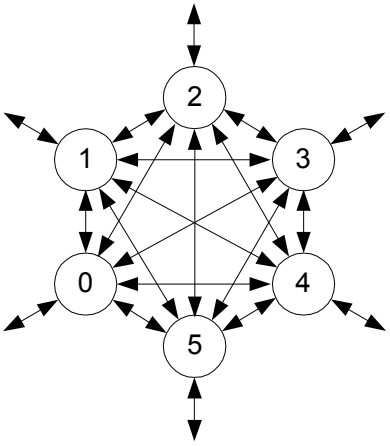
The Ingress Policy block modifies the normal packet flow through the switch. Frames are prevented from going out of certain ports by the use of port-based VLANs, and frames are prevented from entering the switch by the use of switch management Port States.

3.5.1 Port-based VLANs

The 88E6060 device supports a very flexible port-based VLAN feature.

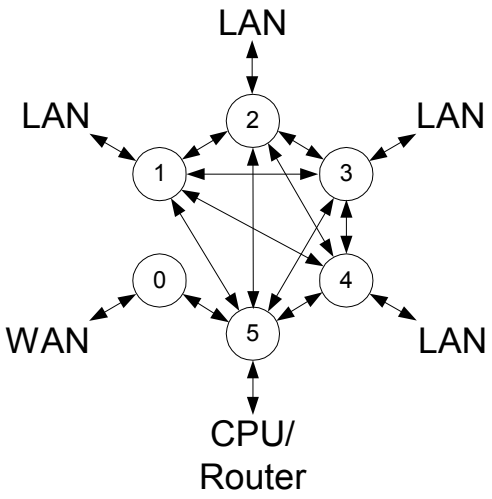
Each Ingress port is associated with the VLANTable field of the Port-based VLAN Map register that restricts which egress ports its frames may use. (Table 45 on page 96). When bit 0 of a port's VLANTable field is set to a one, that port is allowed to send frames to Port 0. When bit 1 of this field is set to a one, that port is allowed to send frames to Port 1. If bit 2 equals 1, Port 2 may receive frames, If bit 3 equals 1, Port 3 may receive frames, and so on. At reset the VLANTable value for each port is set to all ones, except for each port's own bit, which is cleared to a zero. This prevents frames from going back out of the port at which they arrived. This default VLAN configuration allows all of the ports to send frames to all of the other ports as shown in Figure 13.

Figure 13: Switch Operation with VLANs Disabled



One reason for VLAN support in the 88E6060 device is to isolate a port for firewall router applications. Figure 14 shows a typical VLAN configuration for a firewall router. Port 0 is the WAN port. The frames arriving at this port must not go out to any of the LAN ports, but they must be able to go to the router CPU. All the LAN ports are able to send frames directly to each other without the need for CPU intervention but they cannot send frames directly to the WAN port. To accomplish routing, the CPU is able to send frames to all of the ports. The use of the Marvell header (section 3.5.4) enables a CPU to define dynamically to which port or ports a frame is allowed to go. This feature is useful for purposes of WAN and LAN isolation on multicast or flooded traffic generated by the CPU.

Figure 14: Switch Operation with a Typical Router VLAN Configuration



This specific VLAN configuration is accomplished by setting the port's VLANTable registers as follows:

Table 25: VLANTable Settings for Figure 14

Port #	Port Type	VLANTable Setting
0	WAN	0x20
1	LAN	0x3C
2	LAN	0x3A
3	LAN	0x36
4	LAN	0x2E
5	CPU	0x1F

3.5.1.1 Tunneling Frames Through Port-Based VLANS

Normally frames cannot pass through the port based VLAN barriers. However, some frames can be made to pass through the VLAN barriers on the 88E6060 device. Before a frame can tunnel through a port based VLAN barrier, its destination address (DA) must be locked into the address database (section 3.4.5.1), and the VLANTunnel bit on the frame's Ingress port must be set to a one (Table 44 on page 94). When both of these conditions are met, the frame is sent out of the port or ports indicated in the locked address's DPV field for the DA entry in the address database. The VLANTable data is ignored in this case. This feature is enabled only on those ports that have their VLANTunnel bit set to a one.

3.5.2 Switching Frames Back to their Source Port

The 88E6060 device supports the ability to return frames to the port at which they arrived. While this is not a standard way to handle Ethernet frames, some applications may require this ability on some ports. This feature can be enabled on a port-by-port basis by setting the port's own bit in its VLANTable register to a one. See section 3.5.1 and Table 45.

3.5.3 Port States

The 88E6060 device supports four Port States per port as shown in Table 26. The Port States are used by the Queue Controller (section 3.6) in the 88E6060 device to adjust buffer allocation. They are used by the Ingress Policy blocks to control which frame types are allowed to enter and leave the switch, so that Spanning Tree or other bridge loop detection software can be supported. The PortState bits in the Port Control register (Table 44) determine each port's Port State, and they can be modified at any time.

Table 26 below lists the Port States and their function. Two of the Port States require the detection of MGMT frames. A MGMT frame in the 88E6060 device is any multicast frame whose DA address is locked into the address database with an Entry_State value of 0xE (section 3.4.5.1). MGMT frames can tunnel through blocked ports. MGMT frames always ignore VLANs (i.e., they always go to the port indicated by the DA's DPV). These MGMT frames are typically used for 802.1D Spanning Tree Bridge Protocol Data Units (BPDUs), but any multicast address can be used supporting new and/or proprietary protocols.

Table 26: Port State Options

Port State	Description
Disabled	Frames are not allowed to enter (ingress) or leave (egress) a disabled port. Learning does not take place on disabled ports.
Blocking/ Listening	Only MGMT frames are allowed to enter or leave a blocked port. All other frame types are discarded. Learning is disabled on blocked ports.
Learning	Only MGMT frames are allowed to enter or leave a learning port. All other frame types are discarded, but learning takes place on all good frames even if they are not MGMT frames.
Forwarding	Normal operation. All frames are allowed to enter and leave a forwarding port. Learning takes place on all good frames.

The default Port State for all the ports in the switch can be either Disabled or Forwarding depending upon the value of the SW_MODE pins (see Pin Description in Part 1 of this datasheet). The ports come up in the Forwarding Port State unless the SW_MODE is for CPU-attached mode. This enables the CPU to bring up the ports slowly after port-based VLANs are configured (for router WAN to LAN isolation) and so a Spanning tree protocol can be run (if required).

3.5.4 Switch's Ingress Header (Port 4 and Port 5 only)

The detailed information regarding this feature requires an NDA with Marvell® Semiconductor. Please contact your local Marvell Sales Representative for more information.

3.5.5 Switch's Ingress Trailer (Port 4 and Port 5 only)

When a CPU needs to perform Spanning Tree or bridge loop detection or when it needs to be able to send frames out any port or ports, then the CPU's port needs to be configured for Ingress Trailer mode. Any MII port (Port 4 and Port 5) can be configured this way by setting the IngressMode bits in the port's Port Control register (Table 44 on page 94), but only the CPU's port should be configured this way.

When the Ingress Trailer mode is enabled on a port, the last four bytes of the data portion of the frame are used to configure the switch—see Figure 15. The Ingress Policy block removes the Trailer from the frame and overwrites it with a new CRC, causing the frame to be four bytes smaller in size. This adjustment makes the frame 'normal' for the rest of the network since the Trailer's data is intended for the switch only. Frame size checking is performed on the adjusted frame size. This means the CPU must always add four bytes of data to the end of every frame it sends into the switch when the Trailer mode is enabled.

The Ingress Trailer gives the CPU the ability to override normal switch operation on the frame that it just transmitted but this override may not always be necessary. When the CPU requires the switch to process the frame with the switch's current ingress policy, the CPU sets the Trailer data in the frame to all zeros by inserting a four-byte pad. This zero padding clears the Override bit in the Trailer causing the switch to ignore the Trailer's data and process the frame normally after removing the Trailer from the frame.

When the CPU needs to override all of the switch's Ingress policy including Port Based VLANs, it sets the fields in the Trailer as shown in Figure 15 and defined in Table 27.

The ingress trailer is used to force a frame to egress out certain ports and it is the only way for the CPU to tunnel a frame through blocked ports.(by using the MGMT bit). When the CPU uses the trailer it must "know" where it wants the frame to go.

Figure 15: Ingress Trailer Format

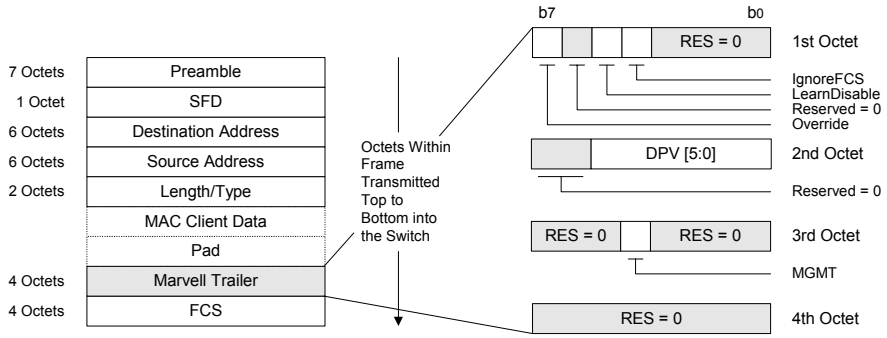


Table 27: Ingress Trailer Fields

Port State	Description
Override	When this bit is set to a one, the Trailer data is used to override the switch's operation. When this bit is cleared to a zero, the Trailer's DPV and MGMT bits are ignored.
LearnDisable	When this bit is set to a one (with or without the Override bit being set) the Source Address contained in this frame will not be learned in the address database.
IgnoreFCS	When this bit is set to a one (with or without the Override bit being set) the frame's FCS is ignored (i.e., the FCS is not checked to see if the frame should be discarded due to a CRC error). The FCS is still a required part of the frame, however, its value is not verified if this bit is set in the Trailer. A new, correct CRC is written to the last four bytes of the frame and the frame is processed by the switch with the good CRC.
DPV[5:0]	The Destination Port Vector. These bits indicate which port or ports the frame is to be sent to if the Override bit is set to a one. A DPV of all zeros discards the frame. Bit 0 is assigned to physical Port 0 and must be set to a one for this frame to egress from that port, bit 1 for Port 1, bit 2 for Port 2, bit 3 for Port 3, and so on.
MGMT	The frame's management bit. When this bit is set to a one (along with the Override bit) indicates the frame is a MGMT frame and is allowed to Ingress and Egress through Blocked ports (section 3.5.3). Must be set on BPDU frames.
RES = 0	These fields are reserved for future use and must be set to zeros.

3.6 Queue Controller

The 88E6060 queue controller uses an advanced non-blocking, output port queue architecture with Resource Reservation. As a result, the 88E6060 supports definable frame latencies without head-of-line blocking problems or non-blocked flow disturbances in any congested environment.

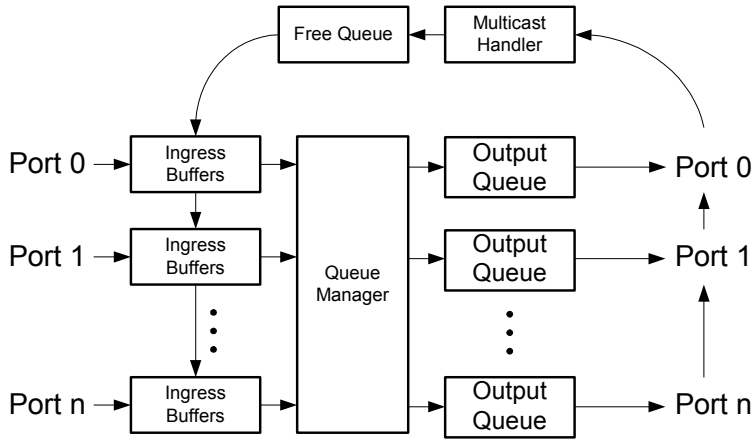
3.6.1 No Head-of-Line Blocking

An output port that is slow or congested never affects the transmission of frames to ports that are not congested. The 88E6060 device is designed to ensure that all flows that are not congested traverse the switch without degradation regardless of the congestion elsewhere in the switch.

3.6.2 The Queues

The queues in the 88E6060 device are shown in Figure 16.

Figure 16: Switch Queues



3.6.3 Queue Manager

At reset[1], the Queue Manager initializes the Free Queue by setting all of the buffer pointers to point into it and ensuring that all of the other queues are empty. The Queue Manager then takes the first available free buffer pointers from the Free Queue and assigns them to any Ingress port that is not disabled[2] and whose link[3] is up. When these conditions are met, the switch is ready to accept and switch packets. Whenever any port's link goes down or the port is set to the Disabled Port State, the port's Ingress buffers and Output Queue buffers are immediately returned to the Free Queue. This feature prevents "stale buffers" or "lost buffers" conditions and maximizes the size of the Free Queue so that of momentary congestion can be handled. When an enabled port's link comes back up, the port gets its Ingress Buffers back and it can start receiving frames again.

1. The Queue Manager is reset either by toggling the hardware RESETn pin, a software reset by the SWReset bit, or by an ATUSize change (both in the ATU Control register–Table 54).
2. When a port is in the Disabled Port State (section 3.5.3), its Ingress buffers are left in the Free Queue for other ports to use.
3. PHY based ports need to get a Link Up signal from the PHY. MII based ports have a link up state if they are enabled.

When a MAC receives a packet, it places it into the embedded memory at the address indicated by the input pointers that the MAC received from the Queue Manager. When packet reception is complete, the MAC transfers the pointers to the Queue Manager and requests new buffers from the Free Queue. When the Free Queue is empty, the MAC is not allocated any pointers until they become available. If the MAC starts to receive a packet when it has no pointers allocated, the packet is dropped. If flow control is enabled, it prevents this condition from occurring.

The Queue Manager uses the data returned from the Lookup Engine (section 3.4.1) and the Ingress Policy (section 3.5) to determine which Output Queue or Queues the packet's pointer(s) should go to. At this point, the Queue Manager modifies the desired mapping of the frame, depending upon the mode of the switch and its level of congestion.

Two modes are supported, with and without Flow Control. Both modes are handled at the same time and can be different per port. One port can have Flow Control enabled, while another has it disabled.

When Flow Control is enabled on an ingress port, the frame is switched to the required output queue without modification. This operation is done so that frames are not dropped. The Queue Manager monitors which output queues are congested and enables or disables flow control on the ingress ports that are causing the congestion. This approach allows flows that are not congested to progress through the switch without degradation.

When Flow Control is disabled on an ingress port, the frame can be discarded instead of being switched to the required Output Queue. If a frame is destined for more than one output queue, it can be switched to some queues and not to others. The decisions are quite complex because the Queue Manager takes many pieces of information into account before the decision is made.

The Queue Manager monitors the current level of congestion in the Output Queues to which the frame is being switched, and the current number of free buffers in the Free Queue. As a result, flows that are not congested traverse the switch unimpeded.

3.6.4 Output Queues

The Output Queues receive and transmit packets in the order received. This is very important for some forms of Ethernet traffic. The Output Queues are emptied as fast as possible, but they can empty at different rates, possibly owing to a port's being configured for a slower or faster speed, or because of network congestion (collisions or Flow Control).

After a packet has been completely transmitted to the MAC, the Output Queue passes the transmitted packet's pointers to the Multicast Handler for processing, after which the MAC begins transmitting the next packet.

3.6.5 Multicast Handler

The Multicast Handler receives the pointers from all of the packets that are transmitted. It looks up each pointer to determine whether each packet were directed to more than one output queue. If not, the pointer is returned to the Free Queue where it can be used again. When the frame is switched to multiple output queues, the Multicast Handler ensures that the frame has exited all of the ports to which it was switched before returning the pointers to the Free Queue.

3.7 Egress Policy (Port 4 and Port 5 only)

The Egress Policy block is used to modify frames, if directed to, as they exit the switch. Specific switch information can be added to the frame for the switch's CPU.

3.7.1 Switch's Egress Header

The detailed information regarding this feature requires an NDA with Marvell Semiconductor. Please contact your local Marvell Sales Representative for more information.

3.7.2 Switch's Egress Trailer

If a CPU needs to perform Spanning Tree or bridge loop detection, the CPU must have information about the originating physical source ports of its received frames, since those frames' SA information cannot be relied upon. To get this physical source port data, the CPU's port needs to be configured for Egress Trailer mode (or egress header mode—section 3.7.1). Any MII port (Port 4 and Port 5) can be configured this way by setting the TrailerMode bit in the port's Port Control register (Table 44 on page 94), but only the CPU's port should be configured this way.

When the Egress Trailer mode is enabled on a port, four extra bytes are added to the end of the frame before the frame's CRC or FCS, and a new CRC is appended to the end of the frame. When the frame is received by the CPU, the Trailer occupies the last four bytes of the frame. The CPU's software can examine portions of the frame to determine if it needs the frame's source port information. Generally it is needed only on MGMT/Spanning Tree frames. If the information is not needed, the CPU reduces the frame size variable by four and passes the frame to the appropriate routines for processing. Removing the Trailer from a frame essentially a subtraction operation without the need to move any data. Consequently CPU overhead is kept to a minimum.

The format of the Egress Trailer is shown in Figure 17 and its fields are defined in Table 28.

Figure 17: Egress Trailer Format

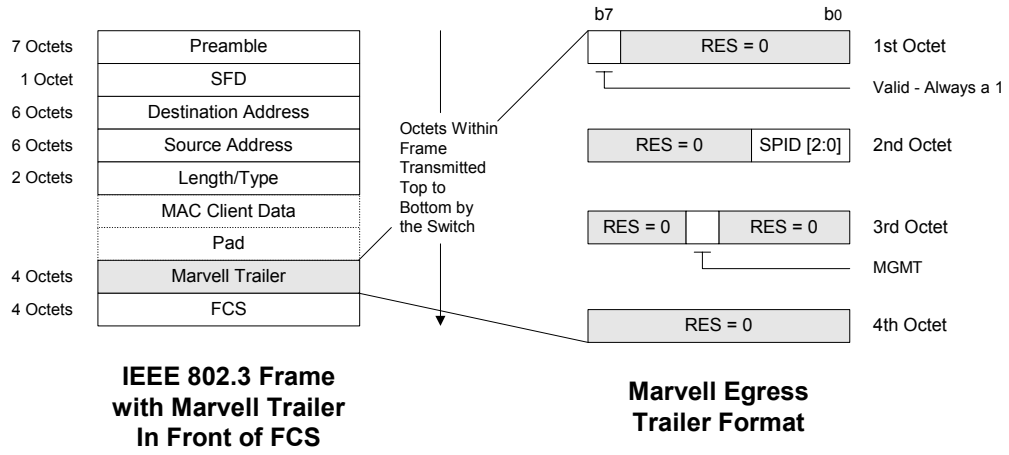


Table 28: Egress Trailer Fields

Field	Description
Valid	When this bit is set to a one, it indicates the Trailer data is present. This bit is always a one.
SPID[2:0]	The Source Port ID. These bits indicate which physical port the frame entered the switch from. An SPID of all zeros indicates Port 0. An SPID of 0x1 indicates Port 1, 0x2 indicates Port 2, 0x3 indicates Port 3, and so on.
MGMT	The frame management bit. When this bit is set to a one, it indicates the frame is a MGMT frame and is allowed to ingress and egress through blocked ports (section 3.5.3). Should be set on BPDU frames.

3.8 Spanning Tree Support

IEEE 802.1D Spanning Tree is supported in the 88E6060 device with the help of an external CPU that runs the Spanning Tree algorithm. The 88E6060 device supports Spanning Tree by:

- Detection of Bridge Protocol Data Unit (BPDU) frames. These frames are called MGMT (management) frames in the 88E6060 device. They are detected by loading the BPDU's multicast address (01:80:C2:00:00:00) into the address database with a MGMT Entry_State indicator (see section 3.4.5.1).
- Tunnelling of BPDU frames through Blocked ports. Blocked ports are controlled by the Port's PortState bits (section 3.5.3). When a port is in the Blocked state, all frames are discarded except for multicast frames with a DA that is contained in the address database with a MGMT indicator (see above).
- Redirection of BPDU frames. BPDU frames need to go to the CPU only, even though they are multicast frames. This is handled in the detection of BPDU frames above by mapping the BPDU's multicast address to the CPU port. (The value of the DPV bits when the address is loaded).
- Source Port information. The CPU needs information of the physical source port of origin of the BPDU frame. The source port is supplied in the frame's Egress Trailer that is sent to the CPU (section 3.7.2).
- CPU transmission of BPDU frames. The CPU needs to be able to transmit BPDU frames out of any physical port of the switch. This is supported only in the Ingress Trailer data that is supplied by the CPU (section 3.5.5). The ingress header cannot be used for this since it cannot force MGMT frames to go out a particular port.

The 88E6060 device can support 802.1D Spanning Tree, or it can be used to perform simpler bridge loop detection on new link up. These different options are accommodated by running appropriate software on the attached CPU.

Any vendor's proprietary protocol units can be handled with the same mechanism.

3.9 Embedded Memory

The 88E6060 device contains an embedded 512Kb (8Kx64) Synchronous SRAM (SSRAM). The SSRAM is running at 50 MHz, and the data bus is 64 bits wide. The memory interface provides up to 3.2 Gbps bandwidth for packet reception/transmission and address mapping data accesses. This memory bandwidth is enough for all the ports running at full wire speed in full-duplex mode with minimum size frames of 64 bytes.

3.10 Interrupt Controller

The 88E6060 device contains a switch Interrupt Controller that is used to merge various interrupts on to the CPU's interrupt signal. Each switch interrupt can be individually masked by an enable bit contained in the Switch Global Control register (Table 53). When an unmasked interrupt occurs and the interrupt pin goes active low, the CPU needs to read the Switch Global Status register (Table 49) to determine the source of the interrupt. When the interrupt comes from the switch core (from ATUFull, ATUDone or EEInt), the switch's interrupt pin goes inactive after the Switch Global Status register is read. The interrupt status bits are cleared on read. If the interrupt comes from the PHY (PHYInt), then the switch's interrupt pin goes inactive only after the PHY's interrupt is cleared by reading the appropriate registers in the PHY. See Table 60 for details.

3.11 Port Monitoring Support

Port monitoring is supported by the 88E6060 device with Egress only monitoring or Egress and Ingress monitoring. Egress monitoring duplicates egress frames from a particular port to a selected monitor port. Ingress monitoring duplicates any good ingress frames for a particular port to a selected monitor port (such frames are processed normally through the switch). Port monitoring is enabled by modifying the Port Association Vector (Table 46) for the particular port that is to be monitored.

3.12 Port Trunking Support

Port Trunking is supported by the 88E6060 device with any combinations of ports. The ports that are to be associated with the trunk need to have all the port member's bits set in each of their Port Association Vectors (Table 46). Port based VLANs are then used to prevent loops and to load balance the trunk.

Section 4. Physical Interface (PHY) Functional Description

The 88E6060 device contains five IEEE 802.3 100BASE-TX and 10BASE-T compliant media-dependent interfaces for support of Ethernet over unshielded twisted pair (UTP) copper cable. DSP-based advanced mixed signal processing technology supports attachment of up 150 meters of CAT 5 cable to each of these interfaces. An optional, per port, automatic MDI/MDIX crossover detection function gives true “plug and play” capability without the need for confusing crossover cables or crossover ports.

The port 0 and port 1 interface can be configured to support IEEE 802.3 100BASE-FX by utilizing a pseudo-ECL (PECL) interface for fiber-optics.

Figure 18: 88E6060 Device Transmit Block Diagram

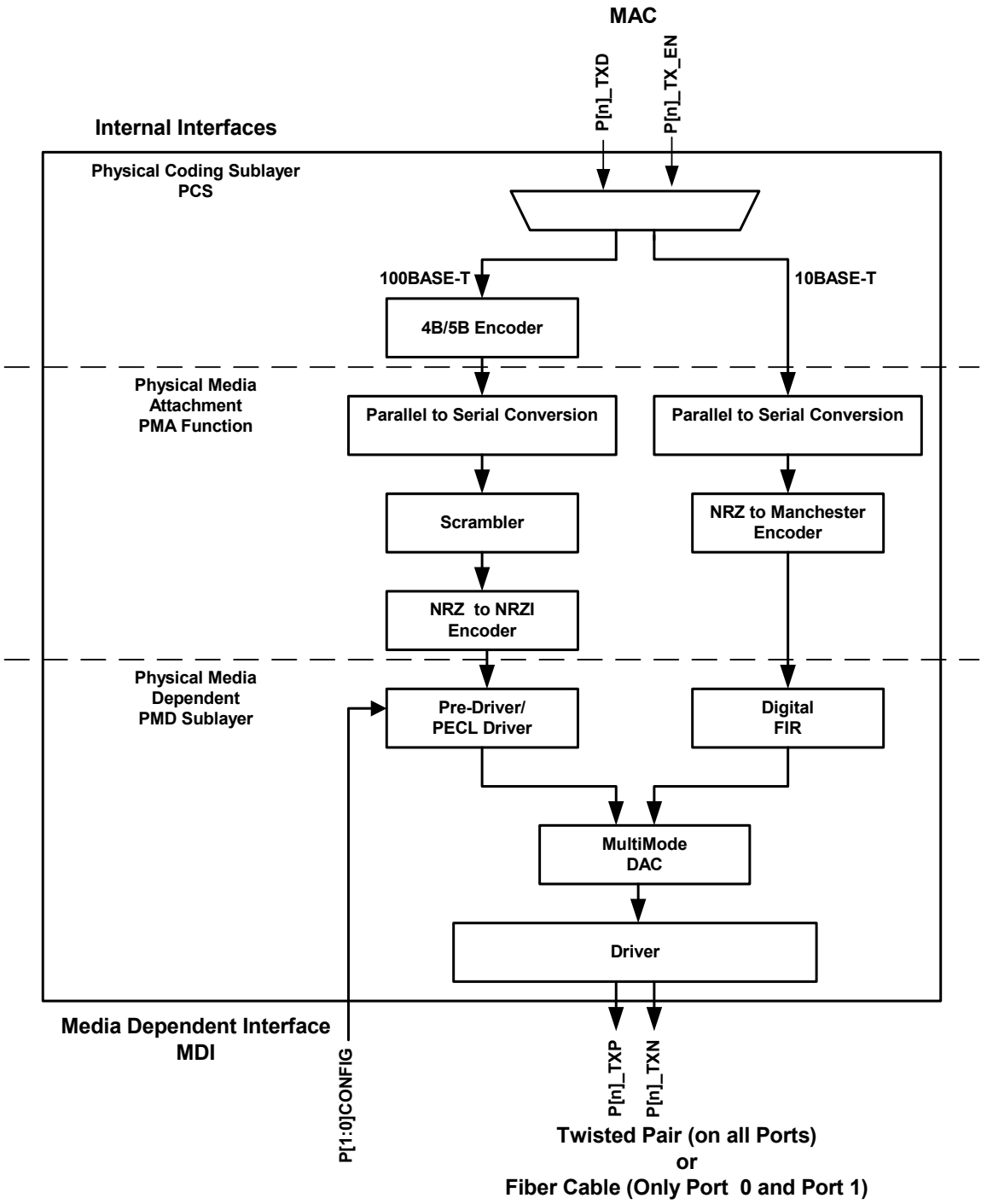
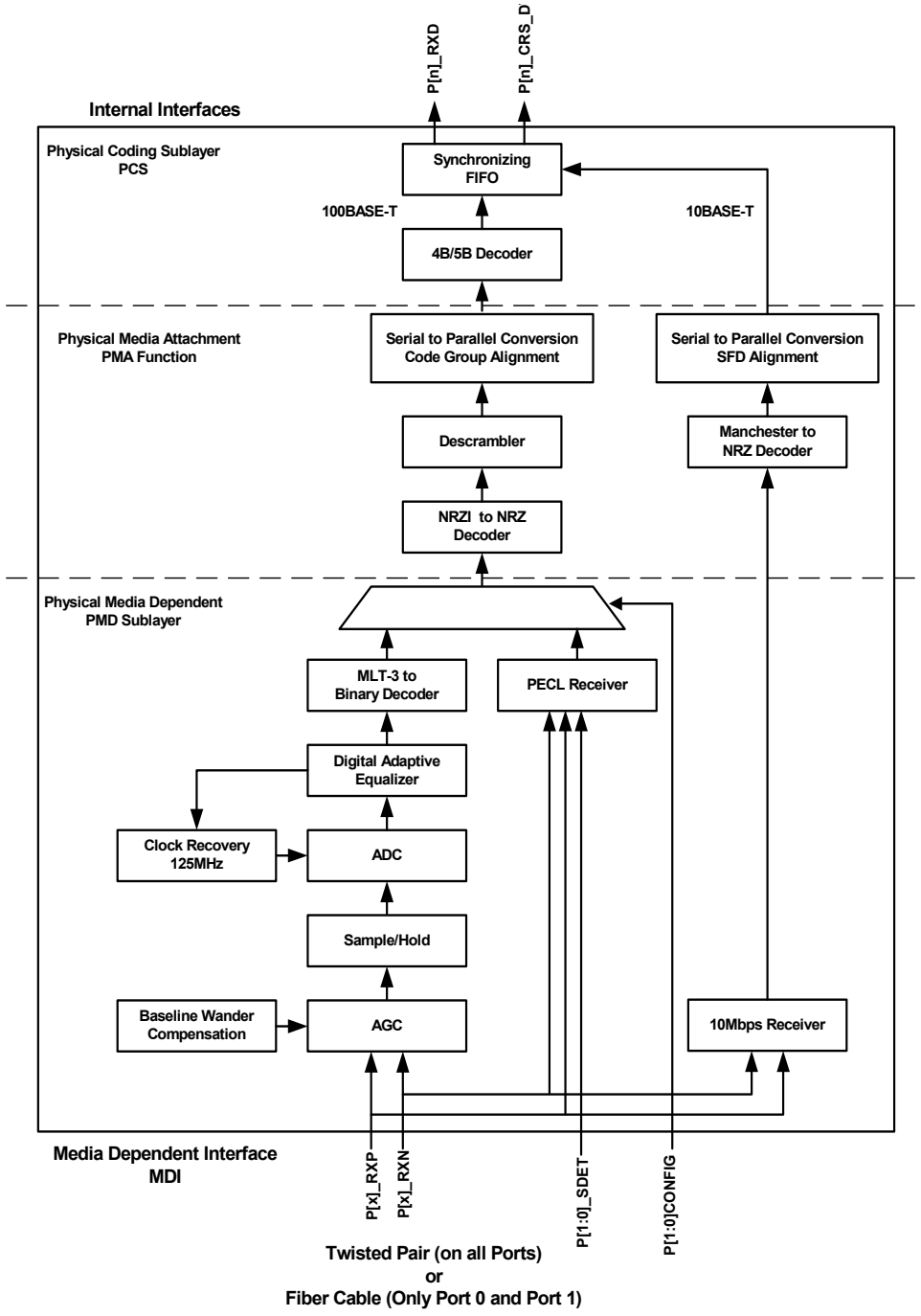


Figure 19: 88E6060 Device Receive Block Diagram



4.1 Transmit PCS and PMA

4.1.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks that convert synchronous 4-bit nibble data to a scrambled MLT-3 125 Mbps serial data stream.

4.1.2 4B/5B Encoding

For 100BASE-TX mode, the 4-bit nibble is converted to a 5-bit symbol with /J/K/ start-of-stream delimiters and /T/R/ end-of-stream delimiters inserted as needed. The 5-bit symbol is then serialized and scrambled.

4.1.3 Scrambler

In 100BASE-TX mode, the transmit data stream is scrambled in order to reduce radiated emissions on the twisted pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit repeating pseudo-random sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

Note

The enabling and disabling of the scrambler and the far end fault generator are controlled in the same way as for the descrambler detection and far end fault detection on the receive side.

4.1.4 NRZ to NRZI Conversion

The data stream is converted from NRZ to NRZI.

4.1.5 Pre-Driver and Transmit Clock

The 88E6060 device uses an all-digital clock generator circuit to create the various receive and transmit clocks necessary for 100BASE-TX, 100BASE-FX, and 10BASE-T modes of operation.

For 100BASE-TX mode, the transmit data is converted to MLT-3-coded symbols. The digital time base generator (TBG) produces the locked 125 MHz transmit clock.

For 100BASE-FX mode, NRZI data is presented directly to the multimode DAC.

For 10BASE-T mode, the transmit data is converted to Manchester encoding. The digital time base generator (TBG) produces the 10 MHz transmit reference clock as well as the over-sampling clock for 10BASE-T waveshaping.

4.1.6 Multimode Transmit DAC

The multimode transmit digital to analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode, NRZI symbols in 100BASE-FX mode, and Manchester-coded symbols in 10BASE-T mode. The transmit DAC utilizes a direct-drive current driver which is well balanced to produce very low common mode transmit noise.

In 100BASE-TX mode, the multimode transmit DAC performs slew control to minimize high frequency EMI.

In 100BASE-FX mode, the pseudo ECL level is generated through external resistive terminations.

In 10BASE-T mode, the multimode transmit DAC generates the needed pre-equalization waveform. This pre-equalization is achieved by using a digital FIR filter.

4.2 Receive PCS and PMA

4.2.1 10-BASE-T/100BASE-TX Receiver

The differential RXP and RXN pins are shared by the 100BASE-TX, 100BASE-FX (supported on Port 0 and Port 1) and 10BASE-T receivers.

The 100BASE-TX receiver consists of several functional blocks that convert the scrambled MLT-3 125 Mbps serial data stream to the synchronous 4-bit nibble data presented to the MAC interfaces.

4.2.2 AGC and Baseline Wander

In 100BASE-TX mode, after input to the AGC block, the signal is compensated for baseline wander by means of a digitally controlled Digital to Analog converter (DAC). It automatically removes the DC offset from the received signal before it reaches the input to the sample and hold stage of the ADC.

4.2.3 ADC and Digital Adaptive Equalizer

In 100BASE-T mode, an analog to digital converter (ADC) samples and quantizes the input analog signal and sends the result into the digital adaptive equalizer. This equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from the ADC output and uses a combination of feed-forward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

4.2.4 Digital Phased Locked Loop (DPLL)

In 100BASE-TX mode, the receive clock is locked to the incoming data stream and extracts a 125 MHz reference clock. The input data stream is quantized by the recovered clock and sent through to the digital adaptive equalizer from each port.

Digital interpolator clock recovery circuits are optimized for MLT-3, NRZI, and Manchester modes. A digital approach makes the 88E6060 receiver path robust in the presence of variations in process, temperature, on-chip noise, and supply voltage.

4.2.5 NRZI to NRZ Conversion

In 100BASE-TX mode, the recovered 100BASE-TX NRZI signal from the receiver is converted to NRZ data, descrambled, aligned, parallelized, and 5B/4B decoded.

4.2.6 Descrambler

The descrambler is initially enabled upon hardware reset if 100BASE-TX is selected. The scrambler can be enabled or disabled via software by setting the descrambler bit (Table 71).

The descrambler “locks” to the descrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization.

The receiver descrambles the incoming data stream by exclusive ORing it with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence.

The descrambler is always forced into the “unlocked” state when a link failure condition is detected or when insufficient idle symbols are detected.

4.2.7 Serial-to-Parallel Conversion and 5B/4B Code-Group Alignment

The Serial-to-Parallel /Symbol Alignment block performs serial to parallel conversion and aligns 5B code-groups to a nibble boundary.

4.2.8 5B/4B Decoder

The 5B/4B decoder translates 5B code-groups into 4B nibbles to be presented to the MAC interfaces. The 5B/4B code mapping is shown in Table 29.

4.2.8.1 FIFO

The 100BASE-X or 10BASE-T packet is placed into the FIFO in order to correct for any clock mismatch between the recovered clock and the reference clock REFCLK.

4.2.8.2 100BASE-FX Receiver

In 100BASE-FX mode, a pseudo-ECL (PECL) receiver is used to decode the incoming NRZI signal passed to the NRZI-NRZ decoder. The NRZI signal from the receiver is converted to NRZ data, aligned, parallelized, and 5B/4B decoded as in the 100BASE-TX mode.

4.2.8.3 Far End Fault Indication (FEFI)

When 100BASE-FX is selected and Bit 0 of CONFIG_A is low at hardware reset, the far end fault detect (FEFD) circuit is enabled. The FEFD enable state can be overridden by programming the FEFI bit (Table 71).

Note

The FEFI function is always disabled if 100BASE-TX is selected.

4.2.8.4 10BASE-T Receiver

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ and then aligned. The alignment is necessary to ensure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

In 10BASE-T mode, a receiver is used to decode the differential voltage offset of the Manchester data. Carrier sense is decoded by measuring the magnitude of the voltage offset.

In this mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ data. The data stream is converted from serial to parallel format and aligned. The alignment is necessary to ensure that the start of frame delimiter (SFD) is aligned to a byte or nibble boundary. For cable lengths greater than 100 meters, the incoming signal has more attenuation. Hence, the receive voltage threshold should be lowered via the ExtendedDistance bit in the PHY Specific Control Register (Table 71).

Table 29: 5B/4B Code Mapping

PCS Code-Group [4:0] 4 3 2 1 0	Name	TXD/RXD <3:0> 3 2 1 0	Interpretation
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 1 1 0	6	0 1 1 0	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data A
1 0 1 1 1	B	1 0 1 1	Data B
1 1 0 1 0	C	1 1 0 0	Data C
1 1 0 1 1	D	1 1 0 1	Data D
1 1 1 0 0	E	1 1 1 0	Data E
1 1 1 0 1	F	1 1 1 1	Data F
1 1 1 1 1	I	Undefined	IDLE; used as inter-stream fill code
1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
0 1 1 0 1	T	Undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
0 0 1 1 1	R	Undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
0 0 0 0 0	V	Undefined	Invalid code
0 0 0 0 1	V	Undefined	Invalid code
0 0 0 1 0	V	Undefined	Invalid code
0 0 0 1 1	V	Undefined	Invalid code
0 0 1 0 1	V	Undefined	Invalid code
0 0 1 1 0	V	Undefined	Invalid code
0 1 0 0 0	V	Undefined	Invalid code
0 1 1 0 0	V	Undefined	Invalid code
1 0 0 0 0	V	Undefined	Invalid code
1 1 0 0 1	V	Undefined	Invalid code

4.2.9 Setting Cable Characteristics

Since cable characteristics differ between unshielded twisted pair and shielded twisted pair cable, optimal receiver performance can be obtained in 100BASE-TX and 10BASE-T modes by setting the TPSelect bit in the PHY Specific Control Register (Table 71) for cable type.

4.2.10 Scrambler/Descrambler

The scrambler block is initially enabled upon hardware reset if 100BASE-TX is selected. If 100BASE-FX or 10BASE-T is selected, the scrambler is disabled by default. The scrambler is controlled by programming the DisScrambler bit in the PHY Specific Control Register (Table 71).

The scrambler setting is also controlled by hardware configuration at the end of hardware reset. Table 30 shows the effect of various configuration settings on the scrambler.

Table 30: Scrambler Settings

P[1:0]_CONFIG (If FX is selected)	DisScrambler Bit ()	Scrambler/ Descrambler
High	HW reset to 1	Disabled
Low	HW reset to 0	Enabled
X	User set to 1	Disabled
X	User set to 0	Enabled

4.2.11 Digital Clock Recovery/Generator

The 88E6060 device uses an all-digital clock recovery and generator circuit to create all of the needed receive and transmit clocks. The digital time base generator (TBG) takes the 25 MHz or 50 MHz reference input clock (XTAL_IN) and produces the locked 25 MHz transmit clock for the MAC in 100BASE-TX mode. It produces a 2.5 MHz transmit clock for the MAC in 10BASE-T mode as well as producing the over-sample clock for 10BASE-T waveshaping.

4.2.12 Link Monitor

The link monitor is responsible for determining whether link is established with a link partner.

In 10BASE-T mode, link monitor function is performed by detecting the presence of the valid link pulses on the RXP/N pins.

In 100BASE-TX mode, the link is established by scrambled idles.

In 100BASE-FX mode, the external fiber-optic receiver performs the signal detection function and communicates this information with the 88E6060 device through SDET pin for Port 0 and Port 1.

If Force Link Good is asserted (ForceLink bit is set high - PHY Specific Control Register, Table 71), the link is forced to be good, and the link monitor is bypassed. Pulse checking is disabled if Auto-Negotiation is disabled, and DisNLPCheck (PHY Specific Control Register, Table 71) is set high. If Auto-Negotiation is disabled and DisNLPGen (PHY Specific Control Register, Table 71) is set high, then the link pulse transmission is disabled.

4.2.13 Auto-Negotiation

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset (SWReset bit—PHY Control Register, Table 61)
- Restart Auto-Negotiation (RestartAneg bit—PHY Control Register, Table 61)
- Transition from power down to power up (PwrDwn bit—PHY Control Register, Table 61)
- Change from the linkfail state to the link-up state

If Auto-Negotiation is enabled, the 88E6060 device negotiates with its link partner to determine the speed and duplex mode at which to operate. If the link partner is unable to Auto-Negotiate, the 88E6060 device goes into the parallel detect mode to determine the speed of the link partner. Under parallel detect mode, the duplex mode is fixed at half-duplex.

After hardware reset, Auto-Negotiation can be enabled and disabled via the AnegEn bit (PHY Control Register - Table 61). When Auto-Negotiation is disabled, the speed and duplex can be changed via the SpeedLSB and Duplex bits (PHY Control Register - Table 61), respectively. The abilities that are advertised can be changed via the Auto-Negotiation Advertisement Register (Table 65).

4.2.14 Register Update

Changes to the AnegEn, SpeedLSB, and Duplex bits (Table 65) do not take effect unless one of the following takes place:

- Software reset (SWReset bit - Table 61)
- Restart Auto-Negotiation (RestartAneg bit - Table 61)
- Transition from power down to power up (PwrDwn bit - Table 61)
- Loss of the link

The Auto-Negotiation Advertisement register (Table 65) is internally latched once every time Auto-Negotiation enters the ability detect state in the arbitration state machine. Hence, a write into the Auto-Negotiation Advertisement Register has no effect once the 88E6060 device begins to transmit Fast Link Pulses (FLPs). This guarantees that a sequence of FLPs transmitted is consistent with one another.

The Next Page Transmit register (Table 69) is internally latched once every time Auto-Negotiation enters the next page exchange state in the arbitration state machine.

4.2.15 Next Page Support

The 88E6060 device supports the use of next page during Auto-Negotiation. By default, the received base page and next page are stored in the Link Partner Ability register - Base Page (Table 66). The 88E6060 device has an option to write the received next page into the Link Partner Next Page register - Table 70 - (similar to the description provided in the IEEE 802.3ab standard) by programming the Reg8NxtPg bit (PHY Specific Control Register - Table 71).

4.2.16 Status Registers

Once the 88E6060 device completes Auto-Negotiation it updates the various status in the PHY Status (Table 72), Link Partner Ability (Next Page) (Table 67), and Auto-Negotiation Expansion (Table 68) registers. Speed, duplex, page received, and Auto-Negotiation completed status are also available in the PHY Specific Status (Table 72) and PHY Interrupt Status registers (Table 74).

4.3 Power Management

The 88E6060 supports advanced power management modes that conserve power.

4.3.1 Low Power Modes

Two low power modes are supported in the 88E6060.

- IEEE 802.3 Clause 22.2.4.1.5 compliant power down
- Energy Detect+™

IEEE 802.3 Clause 22.2.4.1.5 power-down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect+™ allows the 88E6060 to wake up when energy is detected on the wire with the additional capability to wake up a link partner. The 10BASE-T link pulses are sent once every second while listening for energy on the line.

4.3.2 MAC Interface and PHY Configuration for Low Power Modes

The 88E6060 has one CONFIG bit (in CONFIG_B - Table 3) dedicated to support the low power modes.

Low power modes are also register programmable. The EDet bit (Table 71) enables the user to turn on Energy Detect+™. When the low power mode is not selected, the PwrDwn bit (Table 61) can be used. If during the energy detect mode, the PHY wakes up and starts operating in normal mode, the EDet bit settings are retained. When the link is lost and energy is no longer detected, the 88E6060 returns to the mode stored in the EDet bit.

Table 31 shows how these modes are entered

.

Table 31: Operating Mode Power Consumption

Power Mode	Est. Power	How to Activate Mode
IEEE Power down	See Section 9.	PwrDwn bit write (Table 61)
Energy Detect+™	Same as IEEE Power down mode—see Section 9.	Configuration option & register EDet bit write (Table 71)

4.3.3 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting the PwrDwn (Table 61 on page 107) bit equal to one. In this mode, the PHY does not respond to any MAC interface signals except the MDC/MDIO. It also does not respond to any activity on the CAT 5 cable.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the CAT 5 cable. It can only wake up by clearing the PwrDwn bit to 0.

4.3.3.1 Energy Detect +™

In this mode, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every second. If the 88E6060 is in Energy Detect+™ mode, it can wake a connected device and it wakes upon the detection of a connected device. When ENA_EDET is 1, the mode of operation is Energy Detect+™.

4.4 Far End Fault Indication (FEFI)

Far-end fault indication provides a mechanism for transferring information from the local station to the link partner that a remote fault has occurred in 100BASE-FX mode (Port 0 and Port 1 only).

A remote fault is an error in the link that one station can detect while the other one cannot. An example of this is a disconnected fiber at a station's transmitter. This station is receiving valid data and detects that the link is good via the link monitor, but is not able to detect that its transmission is not propagating to the other station.

A 100BASE-FX station that detects this remote fault modifies its transmitted idle stream pattern from all ones to a group of 84 ones followed by one zero. This is referred to as the FEFI idle pattern.

The FEFI function is controlled by CONFIG_A connection and the DisFEFI bit (Table 71).

Table 32 shows the various configuration settings affecting the FEFI function on hardware reset.

Table 32: FEFI Select

Pn_CONFIG[1]	EN_FEFI (CONFIG_A)	FEFI	DisFEFI Bit (Table 71)
Auto-Negotiation	X	Disabled	HW set to 1
10BASE-T	X	Disabled	HW set to 1
100BASE-TX	X	Disabled	HW set to 1
100BASE-FX	0	Disabled	HW set to 1
100BASE-FX	1	Enabled	HW reset to 0

1. "n" in Pn_CONFIG may only take the values "0" or "1"

4.5 Virtual Cable Tester™

The 88E6060 PHY Virtual Cable Tester™ feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatches, bad connectors, termination mismatches, and bad magnetics.

The 88E6060 Switch Core conducts a cable diagnostic test by transmitting a signal of known amplitude (+1V) sequentially along each of the TX and RX pairs of an attached cable. The transmitted signal continues along the cable until it is reflected from a cable imperfection. The magnitude of this echo signal and its return time are shown in the VCT registers (Table 81 and Table 82) on the AmpRfln and DistRfln bits respectively.

Using the information from these registers, the VCT registers (Table 81 and Table 82), the distance to the problem location and the type of problem can be determined. For example, the echo time can be converted to distance using Table 81 and Figure 26 . The polarity and magnitude of the reflection together with the distance indicates the type of discontinuity. For example, a +1V reflection indicates an open close to the PHY and a -1V reflection indicates a short close to the PHY.

When the cable diagnostic feature is activated by setting the ENVCT bit to one (Table 81), a pre-determined amount of time elapses before a test pulse is transmitted. This is to ensure that the link partner loses link, so that it stops sending100BASE-TX idles or 10 Mbit data packets. This is necessary to be able to perform the TDR test. The TDR test can be performed either when there is no link partner or when the link partner is Auto-Negotiating or sending 10 Mbit idle link pulses. If the 88E6060 device receives a continuous signal for 125 ms, it declares a test

failure because it cannot start the TDR test. In the test failure case, the received data is not valid. The results of the test are also summarized in the VCTTst bits (Table 81 and Table 82).

- 11 = Test fail (The TDR test could not be run for reasons explained above)
- 00 = valid test, normal cable (no short or open in cable)
- 10 = valid test, open in cable (Impedance > 333 ohms)
- 01 = valid test, short in cable (Impedance < 33 ohms)

The definition for shorts and opens is arbitrary and can be user-defined using the information in the VCT registers The impedance mismatch at the location of the discontinuity can also be calculated knowing the magnitude of the echo signal. Refer to the Application Note “Virtual Cable Tester -- How to Use TDR results” for details.

4.6 Auto MDI/MDIX Crossover

The 88E6060 device automatically determines whether or not it needs to interchange cable sense between pairs so that an external crossover cable is not required. If the 88E6060 device interoperates with a device that cannot automatically correct for crossover, the 88E6060 PHY makes the necessary adjustment prior to commencing Auto-Negotiation. If the 88E6060 device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 section 40.4.4 determines which device performs the crossover.

When the 88E6060 device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, it follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the 88E6060 device uses signal detection to determine whether to implement crossover.

The Auto MDI/MDIX crossover function can be disabled via the AutoMDI[X] bits (Table 71).

The 88E6060 device is set to normal mode by default if auto MDI/MDIX crossover is disabled at hardware reset.

The pin mapping in normal and crossed modes is specified in Table 33.

Table 33: MDI/MDIX Pin Functions

Physical Pin	Normal		Crossed	
	100BASE-TX	10BASE-T	100BASE-TX	10BASE-T
TXP/TXN	Transmit	Transmit	Receive	Receive
RXP/RXN	Receive	Receive	Transmit	Transmit

4.7 LED Interface

The LED interface pins can either be controlled by a port's PHY or controlled directly, independently of the state of the PHY. Four display options are available and both interfaces (PHY or direct control) can be used together to provide even more LED combinations.

The LEDs can be controlled through a parallel interface or via a serial interface that supports up to seven LEDs per port.

Direct control of the parallel LEDs is achieved by writing to the PHY Manual LED Override register (Table 80). Any of the parallel LEDs can be turned on, off, or made to blink at variable rates independent of the state of the PHY.

When the parallel LEDs are controlled by a port's PHY, their activity is determined by the PHY's state. Each LED can be programmed to indicate various PHY states, with variable blink rate.

Some port PHY events configured to drive LED pins are too short to result in an observable change in LED state. For these events, pulse stretching is provided to translate a short PHY event into an observable LED response. The duration of a pulse stretch can be programmed via the PulseStretch bits (Table 79). The default pulse stretch duration is set to 170 to 340 ms. The pulse stretch duration applies to all applicable LED interface pins.

Some of the status indicators signal multiple events by toggling LED interface pins resulting in a blinking LED. The blink period can be programmed via the BlinkRate bits (Table 79). The default blink period is set to 84 ms. The blink rate information is true for all applicable LEDs.

4.7.1 Parallel LED Interface

These LED interface pins can be used to display port status information. The LED interface has three different status indicators for each port with four different default display options, using the Px_LED2, Px_LED1, and Px_LED0 pins.The LED Parallel Select Register (Table 77) specifies which single LED mode status to display on the LED interface pins. The default display for each mode is shown in Table 34 and the default mode that applies depends upon the hardware configuration established using the CONFIG_A pin—see Table 3.

Table 34: Parallel LED Hardware Defaults

LED Mode —set by CONFIG_A at reset	P[4:0]_LED2	P[4:0]_LED1	P[4:0]_LED0
0	LINK	RX	TX
1	LINK	ACT	SPEED
2	LINK/RX	TX	SPEED
3	LINK/ACT	DUPLEX/COLX	SPEED

Table 77 shows additional display modes that can be set up by software after startup. Table 35 defines all the possible Parallel LED Display modes.

Table 35: Parallel LED Display Interpretation

Status	Description
COLX	Low = Collision activity High = No collision activity This status is pulse stretched to 170 ms.
ERROR	Low = Jabber, received error, false carrier, or FIFO over/underflow occurred High = None of the above occurred This status is pulse stretched to 170 ms.
DUPLEX	Low = Full-duplex High = Half-duplex
DUPLEX/COLX	Low = Full-duplex High = Half-duplex Blink = Collision activity (blink rate is 84ms active then 84 ms inactive) The collision activity is pulse stretched to 84 ms.
SPEED	Low = Speed is 100 Mbps High = Speed is 10 Mbps
LINK	Low = Link up High = Link down
TX	Low = Transmit activity High = No transmit activity This status is pulse stretched to 170 ms.
RX	Low = Receive activity High = No receive activity This status is pulse stretched to 170 ms.
ACT	Low = Transmit or received activity High = No transmit or receive activity This status is pulse stretched to 170 ms.
LINK/RX	Low = Link up High = Link down Blink = receive activity (blink rate is 84 ms active then 84ms inactive) The receive activity is pulse stretched to 84 ms.
ACT (blink mode)	High = No transmit or receive activity Blink = Transmit or receive activity (blink rate is 84ms active then 84 ms inactive) The transmit and receive activity is pulse stretched to 84 ms.

4.7.2 Serial LED Interface

The LEDSER, LEDENA, and LEDCLK pins are used for the serial interface. The CONFIG_A pin (see Table 3) is used to select one of four possible default LED modes which are numerically the same as those set up by the CONFIG_A pin in the parallel case.

However, the default displays in this case are different. The serial LED interface can display a variety of different status indications in 100BASE-TX and 10BASE-T modes (see Table 37 and Table 38). Status to display, pulse stretching, and blink speed can be programmed via the LED Stream Select for Serial LEDs register (Table 78)

4.7.2.1 Single and Dual LED Modes

Single LED mode is initiated at power up according to the CONFIG_A pin settings. Dual LED mode can be entered (or single mode can be reentered) by setting the appropriate register fields according to Table 78. These registers enable LED functions to be programmed individually in dual LED or single LED mode. The data states are sent out on the LEDSER data stream and may be extracted using the LEDCLK and LEDENA signals as shown in the example of Figure 20.

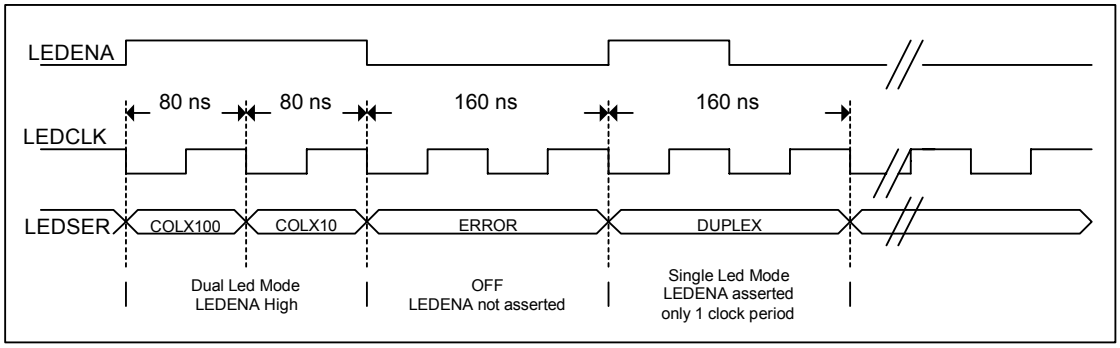
4.7.2.2 Single LED Modes

In the single LED display mode, the same status is driven on both status 100 and status 10 positions in the bit stream. However, the LEDENA signal asserts only over the status that is set and de-asserts over the other position that is turned off in the bit stream. For example, DUPLEX shows the same status for DUPLEX100 and DUPLEX10. However, the LEDENA signal is high over Duplex100 position only for one clock period. Refer to Figure 20 for more details.

4.7.2.3 Dual LED Display Mode

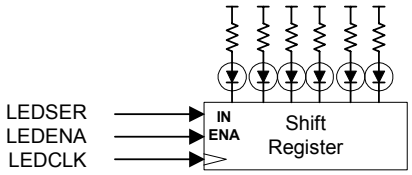
In the dual LED display mode, two LEDs are used: one for 10 Mbps, and one for 100 Mbps activity. A different status is driven on status 100 and status 10 positions in the bit stream. In this case, the LEDENA signal asserts over both 100 and 10 positions in this stream. For example, the LEDENA signal asserts over COLX100 and COLX10 in Figure 20. and remains high for two clock periods. If one of these status bits (shown in Table 38) is turned off, LEDENA is not asserted in both positions.

Figure 20: Serial LEDENA High Clocking with COLX in Dual Mode, Error Off, and DUPLEX in Single Mode



The bit stream on LEDSER can be clocked into a shift register with LEDENA as the shift enable signal as shown in Figure 21. The rate of update of the serial LED interface is controlled by programming register 24.8:6. The default value is set to 42 ms.

Figure 21: Serial LED Conversion



After the LED data is shifted into the correct position, the shift sequence is suspended to allow the appropriate LEDs to light or extinguish depending on status. The LED implementation used in the 88E6060 device is self-synchronizing. The default display options are given in Table 36.

Table 36: Serial LED Display Options (A = Active)

LED Mode	COLX	ERROR	DUPLEX	DUPLEX /COLX	SPEED	LINK	TX	RX	ACT	LINK /RX	LINK /ACT
0	-	A	-	A	A	-	-	-	-	-	A
1	A	A	A	-	A	-	A	-	-	A	-
2	A	A	A	-	A	A	-	-	A	-	-
3	A	A	A	-	A	A	A	A	-	-	-

The LED status bits are output in the order shown on the LEDSER pin synchronously with LEDCLK. All status signals for Port 5 are sent out first followed by those for Ports 4 through 0. Each bit in the stream occupies a period of 80 ns.

Figure 22: Serial LED Display Order—(if all are selected)

<COLX100> → <COLX10> → <ERROR100> → <ERROR10> → <DUPLEX100> → <DUPLEX10>→ <DUPLEX/COLX100> → <DUPLEX/COLX10> → <SPEED100> → <SPEED10> → <LINK100>→ <LINK10> → <TX100> → <TX10> → <RX100> → <RX10> → <ACT100> → <ACT10> → <LINK/RX100>→ <LINK/RX10> → <LINK/ACT100> → <LINK/ACT10>

Table 37 and Table 38 show the status events that can be displayed by programming the 88E6060 device in single and dual LED display modes.

4.7.2.4 Single LED Display Mode

Table 37: Single LED Display Mode

Status	Description
COLX	Low = Collision activity High = No collision activity This status has a default pulse stretch duration of 170 ms.
ERROR	Low = Jabber, received error, false carrier, or FIFO over/underflow occurred High = None of the above occurred This status has a default pulse stretch duration of 170 ms.
DUPLEX	Low = Full-duplex High = Half-duplex
DUPLEX/COLX	Low = Full-duplex High = Half-duplex Blink = Collision activity (blink rate is 84 ms active then 84 ms inactive) The collision activity is pulse stretched to 84 ms.
SPEED	Low = Speed is 100 Mbps High = Speed is 10 Mbps
LINK	Low = Link up High = Link down
TX	Low = Transmit activity High = No transmit activity This status is pulse stretched to 170 ms.
RX	Low = Receive activity High = No receive activity This status is pulse stretched to 170 ms.
ACT	Low = Transmit or received activity High = No transmit or receive activity This status is pulse stretched to 170 ms.
LINK/RX	Low = Link up High = Link down Blink = Receive activity (blink rate is 84 ms active then 84 ms inactive) The receive activity is pulse stretched to 84 ms.
LINK/ACT	Low = Link up High = Link down Blink = Transmit or receive activity (blink rate is 84ms active then 84 ms inactive) The transmit and receive activity is pulse stretched to 170 ms.

4.7.2.5 Dual LED Display Mode

Table 38: Dual LED Display Mode

Event	Description
COLX100	0 = 100 Mbps collision activity 1 = No 100 Mbps collision activity This status can be pulse stretched.
COLX10	0 = 10 Mbps collision activity 1 = No 10 Mbps collision activity This status can be pulse stretched.
ERROR100	0 = Received error, false carrier, or 100 Mbps FIFO over/underflow occurred. 1 = None of the above occurred This status can be pulse stretched.
ERROR10	0 = Jabber or 10 Mbps FIFO over/underflow occurred 1 = None of the above occurred This status can be pulse stretched.
DUPLEX100	0 = 100 Mbps full-duplex 1 = 100 Mbps half-duplex
DUPLEX10	0 = 10 Mbps full-duplex 1 = 10 Mbps half-duplex
DUPLEX/COLX100	0 = 100 Mbps full-duplex 1 = Half-duplex Blink = 100 Mbps collision activity The collision activity can be pulse stretched. The blink rate can be programmed.
DUPLEX/COLX10	0 = 10 Mbps full-duplex 1 = 10 Mbps half-duplex Blink = 10 Mbps collision activity The collision activity can be pulse stretched. The blink rate can be programmed.
SPEED100	0 = Speed is 100 Mbps 1 = Speed is 10 Mbps
SPEED10	0 = Speed is 10 Mbps 1 = Speed is 100 Mbps
LINK100	0 = 100 Mbps link up 1 = 100 Mbps link down
LINK10	0 = 10 Mbps link up 1 = 10 Mbps link down
TX100	0 = 100 Mbps transmit activity 1 = No 100 Mbps transmit activity This status can be pulse stretched.
TX10	0 = 10 Mbps transmit activity 1 = No 10 Mbps transmit activity This status can be pulse stretched.
RX100	0 = 100 Mbps receive activity 1 = No 100 Mbps receive activity This status can be pulse stretched.

Table 38: Dual LED Display Mode (Continued)

Event	Description
RX10	0 = 10 Mbps receive activity 1 = No 10 Mbps receive activity This status can be pulse stretched.
ACT100	0 = 100 Mbps transmit or 100 Mbps receive activity 1 = No 100 Mbps transmit or 100 Mbps receive activity This status can be pulse stretched.
ACT10	0 = 10 Mbps transmit or 10 Mbps receive activity 1 = No 10 Mbps transmit or 10 Mbps receive activity This status can be pulse stretched.
LINK/RX100	0 = 100 Mbps link up 1 = 100 Mbps link down Blink = 100 Mbps receive activity The receive activity can be pulse stretched. The blink rate can be programmed.
LINK/RX10	0 = 10 Mbps link up 1 = 10 Mbps link down Blink = 10 Mbps receive activity The receive activity is can be pulse stretched The blink rate can be programmed.
LINK/ACT100	0 = 100 Mbps link up 1 = 100 Mbps link down Blink = 100 Mbps transmit or 100 Mbps receive activity The transmit and receive activity can be pulse stretched. The blink rate can be programmed.
LINK/ACT10	0 = 10 Mbps link up 1 = 10 Mbps link down Blink = 10 Mbps transmit or 10 Mbps receive activity The transmit and receive activity can be pulse stretched. The blink rate can be programmed.

Section 5. Serial Management Interface (SMI)

The 88E6060 serial management interface provides access to the internal registers via the MDC and MDIO signals and is compliant with IEEE 802.3u clause 22. MDC is the management data clock input whose frequency can run from DC to a maximum rate of 8.3 MHz. MDIO is the management data input/output which carries a bidirectional signal that runs synchronously with the MDC. The MDIO pin requires a pull-up resistor to pull the MDIO high during idle and turnaround times.

5.1 MDC/MDIO Read and Write Operations

All of the relevant serial management registers, as well as several optional registers, are implemented in the 88E6060 Switch Core. A description of these registers can be found in Section 6. "Switch Register Description" .

Note

Access to the 88E6060 device's Switch and PHY registers is not possible when the Serial EEPROM is still loading the registers. A CPU can monitor the 88E6060 device INTn pin, which will go active (low) when the Serial EEPROM has been fully processed (i.e., a Halt instruction has been reached - see section 8).

Figure 23: Typical MDC/MDIO Read Operation

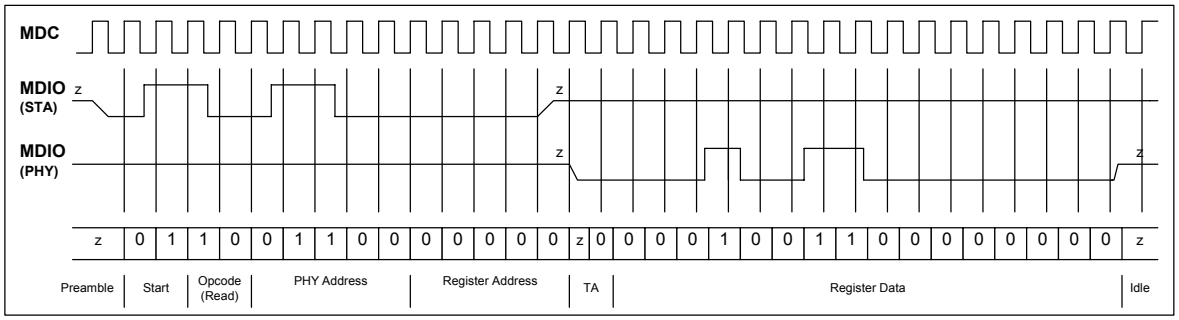


Figure 24: Typical MDC/MDIO Write Operation

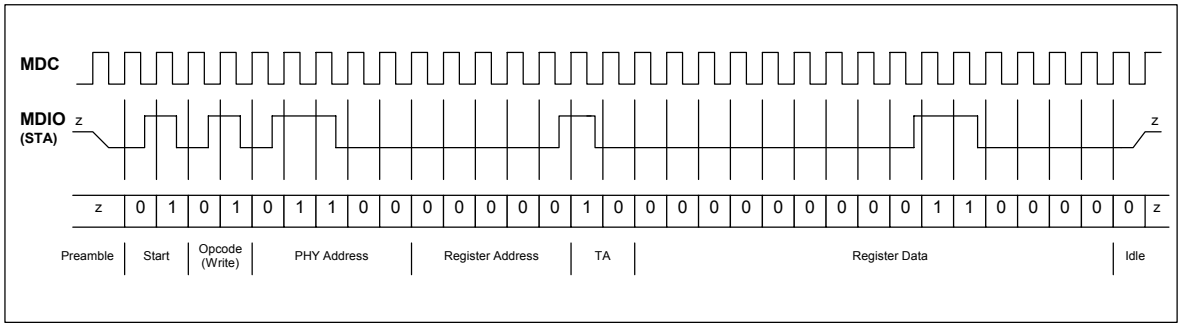


Table 39 shows an example of a read operation of PHY address 04, register 0, with data of 04C0.

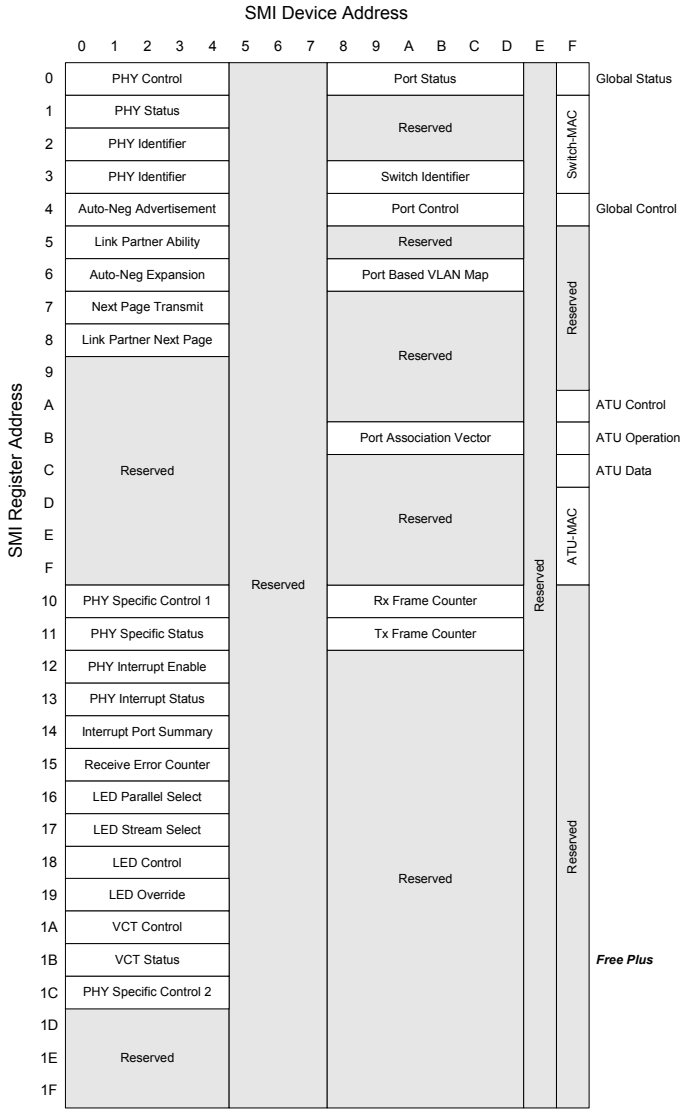
Table 39: Serial Management Interface Protocol Example

32-Bit Preamble	Start of Frame	Opcode Read = 10 Write = 01	5-Bit Phy Device Address	5-Bit Phy Register Address	2-Bit Turnaround Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	00100	00000	z0	0000010011000000	11111111

Section 6. Switch Register Description

All of the 88E6060 registers are accessible using the IEEE Serial Management Interface (SMI) used for PHY devices (see MDC/MDIO pin description in Section 1 and Section 5 of this datasheet). The 88E6060 device uses 16 of the 32 possible Device Addresses. The16 Device Addresses are configurable at reset by use of the EE_CLK/ADDR4 pin (see Signal Description in part 1 of this datasheet). Figure 25 shows the register map assuming the lower 16 SMI Device Addresses are being used.

Figure 25: 88E6060 Register Map



6.1 Register Types

The registers in the 88E6060 device are made up of one or more fields. The way in which each of these fields operate is defined by the field's Type. The function of each Type is described in Table 40.

Table 40: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to a one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or until a reset occurs.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
R/W	Read and write with no definable initial value
RWR	Read/Write reset. All bits are readable and writable. After reset the register field is cleared to zero.
RWS	Read/Write set. All bits are readable and writable. After reset the register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the required function to be immediately executed, then the register field is cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until a soft reset is executed.
Retain	Value written to the register field D0
WO	Write only. Reads to this type of register field return undefined data.

6.2 Switch Core Registers

Switch Core Registers are of two types:

- Switch Port Registers—are separately configured for each port comprised in the switch. Each port has a unique associated SMI device address and this address is used to access that port's switch register set.
- Switch Global Registers—are configured using a single SMI device address. A global register's setting affects all ports of the switch.

The 88E6060 contains six ports (MACS). The supported ports are accessible using SMI device addresses 0x08 to 0x0D, or 0x18 to 0x1D depending upon the value of the EE_CLK/ADDR4 pin at reset (Section 1). The MACs are fully IEEE802.3 compliant. Since there is no IEEE standard covering required MAC registers, these registers are 88E6060 device specific.

The switch contains many global registers that are used to control features and functions that are common to all ports in the switch. The global registers are accessible using SMI device address 0x0F (or 0x1F) depending upon the value of the EE_CLK/ADDR4 pin at reset.

6.2.1 Switch Core Register Map

Table 41: Switch Core Register Map

Description	Offset Hex	Offset Decimal	Page Number
Switch Port Registers (SMI Device Address)			
Port Status Register	0x00	0	page 92
Reserved Registers	0x01 - 0x02	1 - 2	page 93
Switch Identifier Register	0x03	3	page 93
Port Control Register	0x04	4	page 94
Reserved Registers	0x05	5	page 95
Port Based VLAN Map	0x06	6	page 96
Reserved Registers	0x07 - 0x0A	7 - 10	page 96
Port Association Vector	0x0B	11	page 97
Reserved Registers	0x0C - 0x0F	12 - 15	page 97
Rx Counter	0x10	16	page 98
Tx Counter	0x11	17	page 98
Reserved Registers	0x12 - 0x1F	18 - 31	page 98
Switch Global Registers			
Switch Global Status Register	0x00	0	page 99
Switch MAC Address Register Bytes 0 & 1	0x01	1	page 100
Switch MAC Address Register Bytes 2 & 3	0x02	2	page 100
Switch MAC Address Register Bytes 4 & 5	0x03	3	page 100
Switch Global Control Register	0x04	4	page 101
Reserved Registers	0x05 - 0x09	5 - 9	page 101
ATU Control Register	0x0A	10	page 102
ATU Operation Register	0x0B	11	page 103
ATU Data Register	0x0C	12	page 104
ATU MAC Address Register Bytes 0 & 1	0x0D	13	page 104
ATU Switch MAC Address Register Bytes 2 & 3	0x0E	14	page 104
ATU Switch MAC Address Register Bytes 4 & 5	0x0F	15	page 105
Reserved Registers	0x10 - 0x1F	16 - 31	page 105

6.2.2 Switch Port Registers

Table 42: Port Status Register
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Type	Description
15	LinkPause	RO	Link Partner's Pause bit, returned from the link partner through Auto-Negotiation. This bit is valid for Ports with PHYs and when the Resolved bit is set to a one. 0 = MAC Pause not implemented in the link partner 1 = MAC Pause is implemented in the link partner
14	MyPause	RO	My Pause bit, sent to the link partner during Auto-Negotiation. This bit is valid for Ports with PHYs. It is set high if FD_FLOW_DIS (Section 1) is low during reset. 0 = MAC Pause not implemented in the local MAC 1 = MAC Pause is implemented in the local MAC
13	Resolved	RO	Link Mode is resolved. 0 = Link is undergoing Auto-Negotiation or the port is disabled 1 = Link has determined its Speed, Duplex and LinkPause settings
12	Link	RO	Link Status in real time (i.e., it is not latched). 0 = Link is down 1 = Link is up
11	PortMode	RO	Port mode. The value of this bit is always a one for Ports 0 thru 4 and it comes from Px_MODE3 during configuration for Port 5 and Port 4. 0 = SNI mode is enabled 1 = MII 10/100 or RMII 100 Mbps mode is enabled
10	PHYMode	RO	PHY mode. This bit is valid for all ports but it is meaningful for Port 5 and Port 4 only and only when the PortMode (bit 11 above) indicates an MII mode of operation (i.e., PortMode is a one). This bit may be either value for SNI configured ports – but all SNI port configurations are PHY mode. The value of this bit is always zero for Ports 0 to 3 (and Port 4 if Port 4's MII is disabled) and it comes from Px_MODE2 during configuration for Port 5 and Port 4 (if Port 4's MII is enabled). 0 = Pins are in MII MAC Mode (i.e., INCLK and OUTCLK are inputs) or the pins are in RMII PHY Mode (all RMII Modes are PHY mode where INCLK and OUTCLK are outputs). 1 = Pins are in MII PHY Mode (i.e., INCLK and OUTCLK are output)
9	Duplex	RO R/W on Port 4 & 5 Only	Duplex mode. This bit is valid when the Resolved bit is set to a one. 0 = Half-duplex 1 = Full-duplex This bit can be written to on Port 5 and Port 4 only so that the Port's duplex can be modified after Reset occurs. Care must be taken to ensure this Port's duplex matches the duplex of its link partner.

Table 42: Port Status Register (Continued)
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Type	Description
8	Speed	RO	Speed mode. This bit is valid when the Resolved bit is set to a one and the PortMode (bit 11 above) is also a one. If the PortMode bit is a zero then the port's speed is 10 Mbps regardless of the value of this bit. When the port is configured in MII MAC mode, the Speed bit is undefined. 0 = 10 Mbps 1 = 100 Mbps
7:0	Reserved	RES	Reserved for future use.

The PortMode, PHYMode, Duplex, and Speed bits for Port 5 and Port 4 come from the Px_MODE[3:0] pins at reset (if Port 4 is in MII mode). When the PortMode is a one, the PHYMode, Duplex, and Speed bits map the same as the other 10/100 ports that contain PHYs. When the PortMode is a zero the mapping is easier to see by looking at "RMII/MII/SNI Configuration" Table 19:.

Note

Registers 0x01 and 0x02 (Hex), or 1 and 2 (Decimal) are reserved.

Table 43: Switch Identifier Register
Offset: 0x03 (Hex), or 3 (Decimal)

Bits	Field	Type	Description
15:4	DeviceID	RO	Device Identifier. The 88E6060 is identified by the value 0x060.
3:0	RevID	RO	Revision Identifier. The initial version of the 88E6060 has a RevID of 0x0. This RevID field may change at any time. Contact a Marvell FAE for current information on the device revision identifier.

Table 44: Port Control Register
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Type	Description
15	ForceFlow Control	RWR	Force Flow Control. This bit is used to enable full-duplex flow control or half-duplex back pressure on this port depending upon the port's current duplex. This bit can only be changed when the port is in the Disabled Port state (bits 1:0 below). 0 = Use configuration pin settings for flow control/back pressure 1 = Force flow control/back pressure to be enabled on this port
14	Trailer	RWR	Egress Trailer Mode (Port 4 and 5 only). 0 = Normal mode – frames are transmitted unmodified 1 = Add a Trailer to all frames transmitted out of the port. Egress Trailer mode is intended for management CPU ports for source port information on BPDU frame.
13:12	Reserved	RES	Reserved for future use.
11	Header	RWR	The detailed information regarding this feature requires an NDA with Marvell® Semiconductor. Please contact your local Marvell Sales Representative for more information.
10:9	Reserved	RES	Reserved for future use.
8	Ingress Mode	RWR	Ingress Mode (Port 4 and 5 only). 0 = Normal mode – frames are received unmodified 1 = CPU Port with Ingress Trailer mode – frames must be received with a Trailer and the Trailer is checked, potentially used and then removed from the frame. Trailer mode is intended for Ingress data control from a management CPU port so that BPDU frames can be directed.
7	VLAN Tunnel	RWR	VLAN Tunnel. When this bit is cleared to a zero, the VLANs defined in the VLANTable (Table 45, on page 96) are enforced for ALL frames. When this bit is set to a one, the VLANTable masking is bypassed for any frame entering this port with a DA that is currently 'locked' in the ATU. This includes unicast as well as multicast frames.
6:2	Reserved	RES	Reserved for future use.

Table 44: Port Control Register (Continued)
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Type	Description
1:0	PortState	RWR Or RWS to 0b11	Port State. These bits are used to manage a port to determine what kind of frames, if any, are allowed to enter or leave a port for simple bridge loop detection or 802.1D Spanning Tree. The state of these bits can be changed at any time without disrupting frames currently in transit. The Port States are: 00 = Disabled. The switch port is completely disabled and it will not receive or transmit any frames. The QC will return any pre-allocated ingress queue buffers when the port is in this mode. 01 = Blocking/Listening. The switch will examine all frames without learning any SA addresses, and discard all but MGMT frames. MGMT (management) frames are the only kind of frame that can be tunneled through Blocked ports. A MGMT frame is any frame whose multicast DA address appears in the ATU Database with the MGMT Entry State. It will allow MGMT frames only to exit the port. This mode is used for BPDU handling for bridge loop detection and Spanning Tree support. 10 = Learning. The switch will examine all frames, learning all SA addresses, and still discard all but MGMT frames. It will allow MGMT frames only to exit the port. 11 = Forwarding. The switch will examine all frames, learning all SA addresses, and receive and transmit all frames like a normal switch. The PortState bits for all ports come up in the Forwarding state unless the SW_MODE[1:0] pins are set to 0b00, the CPU attached mode. Software Reset, (SWReset - Table 54 on page 102) causes the PortState bits to revert back to their reset state (i.e., either Disabled or Forwarding).

Note

Register 0x05 (Hex), or 5 (Decimal) is reserved.

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Table 45: Port Based VLAN Map
Offset: 0x06 (Hex), or 6 (Decimal)

Bits	Field	Type/ Reset Value	Description
15:12	DBNum	RWR	Port's Default DataBase VLAN Number. This field can be used with VLANs to keep each VLAN's MAC address mapping database separate from the other VLANs. This allows the same MAC address to appear multiple times in the address database (at most one time per VLAN) with a different port mapping per entry. This field should be zero if not being used. It needs to be a unique number for each independent VLAN if used.
11:6	Reserved	RES	Reserved for future use.
5:0	VLANTable	RWS to all ones except for this port's bit	Port based VLAN Table. The bits in this table are used to restrict which output ports this input port can send frames to. These bits restrict where a port can send frames to (unless a VLANTunnel frame is being received - see Port Control register, Table 44). To send frames to Port 0, bit 0 of this register must be a one. To send frames to Port 1, bit 1 of this register must be a one, etc. After reset, all ports are accessible since all the other port number bits are set to a one. This Port's bit will always be zero at reset. This prevents frames exiting the port on which they arrived. This port's bit can be set to a one in the 88E6060 Switch Core enabling frames to be returned on their ingress port; consequently care should be taken in writing code to control these bits. This register is reset to 0x3E for Port 0 (SMI Device Address 0x8), and it resets to 0x3D for Port 1 (Addr 0x9) and to 0x3B for Port 2 (Addr 0xA), etc.

Note

Registers 0x07 - 0x0A (Hex), or 7 - 10 (Decimal) are reserved.

Table 46: Port Association Vector
Offset: 0x0B (Hex), or 11 (Decimal)

Bits	Field	Type	Description
15	Ingress Monitor	RWR	Ingress Monitor enable. When this bit is set to a one ingress port monitoring is enabled on the same ports upon which egress port monitoring is enabled, as defined by the PAV bits below. This is the recommended operation mode for port monitoring.
14:6	Reserved	RES	Reserved for future use.
5:0	PAV	RWS to all zeros except for this port's bit	Port Association Vector for ATU learning. The value of these bits is used as the port's DPV on automatic ATU Learning or Entry_State refresh whenever these bits contain a non-zero value. When these bits are all zero automatic Learning and Entry_State refresh is disabled on this port. For normal switch operation this port's bit should be the only bit set in the vector. These bits must only be changed when frames are not entering the port (see PortState bits in Port Control – Table 44, on page 94). The PAV bits can be used to set up an egress port monitor. To configure Port 0 to receive a copy of the frames that exit Port 1, set bit 0 in Port 1's PAV register (along with Port 1's bit). To configure Port 0 to get a copy of the frames that exit Port 2, set bit 0 in Port 2's PAV register, etc. The PAV bits can be used to set up an ingress port monitor along with an egress port monitor. To configure Port 0 to receive a copy of the frames that enter Port 1 as well as exit Port 1, set bit 0 in Port 1's PAV register (along with Port 1's bit—bit 1) and set the IngressMonitor bit above. The PAV bits can be used to set up port trunking (along with the VLANTable bits (Table 45 on page 96). For the two ports that form a trunk, set both of the port's bits in both port's PAV registers. Then use the VLANTable to isolate the two ports from each other and to steer the traffic from the other ports down the required trunk line of the pair.

Note

Registers 0x0C - 0x0F (Hex), or 12 - 15 (Decimal) are reserved.

Table 47: Rx Counter
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Type/ Reset Value	Description
15:0	RxCtr	RO	Received Counter. When CtrMode is cleared to a zero (Global Control – Table 53, on page 101) this counter increments each time a good frame enters this port. It does not matter if the frame is switched or discarded by the switch. When CtrMode is set to a one this counter increments each time an error frame enters this port. An error frame is one that is 64 bytes or greater with a bad CRC (including alignment errors but not dribbles). Fragments and properly formed frames are not counted. The counter wraps back to zero. The only time this counter does not increment is when this port is Disabled (see PortState, Table 44, on page 94). This register can be cleared by changing the state of the CtrMode bit in the Switch Global Control register (Table 53 on page 101).

Table 48: Tx Counter
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Type/ Reset Value	Description
15:0	TxCtr	RO	Transmit Counter. When CtrMode is cleared to a zero (see Global Control – Table 53 on page 101) this counter increments each time a frame successfully exits this port. When CtrMode is set to a one this counter increments each time a collision occurs during an attempted transmission. It no longer counts all transmitted frames – but only those transmission attempts that resulted in a collision. The counter wraps back to zero. The only time this counter does not increment is when this port is Disabled (see PortState field of Port Control Register (Table 44, on page 94). This register can be cleared by changing the state of the CtrMode bit in Global Control (Table 53 on page 101).

Note

Registers 0x12 - 0x1F (Hex), or 18 - 31 (Decimal) are reserved.

6.2.3 Switch Global Registers

Table 49: Switch Global Status Register
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Type	Description
15:14	Reserved	RES	Reserved for future use.
13:12	SW_Mode	RO	Switch Mode. These bits return the value of the SW_MODE[1:0] pins.
11	InitReady	RO	Switch Ready. This bit is set to a one when all the blocks inside the device have finished their initialization and are ready to accept frames.
10:4	Reserved	RES	Reserved for future use.
3	ATUFull	LH	ATU Full Interrupt. This bit is set to a one if the ATU cannot load or learn a new mapping owing to all of the available locations for an address being locked. It is automatically cleared when read. This bit's being high causes the 88E6060 INTn pin to go low if the ATUFullIntEn bit in GlobalControl (Table 53, on page 101) is set to a one.
2	ATUDone	LH	ATU Done Interrupt. This bit is set to a one whenever the ATUBusy bit (Table 55, on page 103) changes from a one to a zero. It is automatically cleared when read. This bit's being high causes the 88E6060 INTn pin to go low if the ATUDoneIntEn bit in Global Control (Table 53, on page 101) is set to a one.
1	PHYInt	RO	PHY Interrupt. This bit is set to a one when the PHYs interrupt logic has at least one active interrupt. This bit's being high causes the 88E6060 INTn pin to go low if the PHYIntEn bit in Global Control (Table 53, on page 101) is set to a one.
0	EEInt	LH	EEPROM Done Interrupt. This bit is set to a one after the EEPROM finishes loading registers, and it is automatically cleared when read. This bit's being high causes the 88E6060 INTn pin to go low when the EEIntEn bit in Global Control (Table 53 on page 101) is set to a one.

Table 50: Switch MAC Address Register Bytes 0 & 1
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Type	Description
15:9	MACByte0	RWR	MAC Address Byte 0 (bits 47:41) is used as the switch's source address (SA) in transmitted full-duplex Pause frames. Since bit 0 of byte 0 (bit 40) is the multicast bit (it is the 1st bit down the wire) it is always transmitted as a zero, and its value cannot be changed.
8	DiffAddr	RWR	Different MAC addresses per Port. This bit is used to have all ports transmit the same or different source addresses in full-duplex Pause frames. 0 = All ports transmit the same SA 1 = Each port uses a different SA where bits 47:3 of the MAC address are the same, but bits 2:0 are the port number (Port 0 = 0, Port 1 = 1, and so on.)
7:0	MACByte1	RWR	MAC Address Byte 1 (bits 39:32) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.

Table 51: Switch MAC Address Register Bytes 2 & 3
Offset: 0x02 (Hex), or 2 (Decimal)

Bits	Field	Type	Description
15:8	MACByte2	RWR	MAC Address Byte 2 (bits 31:24) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.
7:0	MACByte3	RWR	MAC Address Byte 3 (bits 23:16) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.

Table 52: Switch MAC Address Register Bytes 4 & 5
Offset: 0x03 (Hex), or 3 (Decimal)

Bits	Field	Type	Description
15:8	MACByte4	RWR	MAC Address Byte 4 (bits 15:8) is used as the switch's source address (SA) in transmitted full-duplex Pause frames.
7:0	MACByte5	RWR	MAC Address Byte 5 (bits 7:0) is used as the switch's source address (SA) in transmitted full-duplex Pause frames. Note: Bits 2:0 of this register are ignored when DiffAddr is set to a one.

Table 53: Switch Global Control Register
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Type	Description
15:14	Reserved	RES	Reserved for future use.
13	Discard Excessive	RWR	Discard frames with Excessive Collisions. When this bit is set to a one frames that encounter 16 consecutive collisions are discarded. When this bit is cleared to a zero Egress frames are never discarded and the backoff range is reset after 16 consecutive collisions on a single frame.
12:11	Reserved	RES	Reserved for future use.
10	MaxFrame Size	RWR	Maximum Frame Size allowed. The Ingress block discards all frames that are less than 64 bytes in size. It also discards all frames that are greater than a certain size as follows: 0 = Max size is 1522 if IEEE 802.3ac tagged, or 1518 if not tagged 1 = Max size is 1536
9	ReLoad	SC	Reload the registers using the EEPROM. When this bit is set to a one the contents of the external EEPROM are used to load the registers just as if a reset had occurred. When the reload operation is done, this bit is cleared to a zero automatically, and the EEInt interrupt is set.
8	CtrMode	RWR	Counter Mode. When this bit is set to a one, the Rx counters for all ports (Table 47, on page 98) count Rx errors and the Tx counters for all ports (Table 48, on page 98) count Tx collisions. When this bit is cleared to a zero, the Rx counters for all ports count Rx frames and the Tx counters for all ports count Tx frames. The Rx counters and the Tx counters for all ports are cleared to a zero whenever this bit changes state (i.e., it transitions from a one to a zero or from a zero to a one).
7:4	Reserved	RES	Reserved for future use.
3	ATUFull IntEn	RWR	ATU Full Interrupt Enable. This bit must be set to a one to allow the ATU Full interrupt to drive the 88E6060 INTn pin low.
2	ATUDone IntEn	RWR	ATU Done Interrupt Enable. This bit must be set to a one to allow the ATU Done interrupt to drive the 88E6060 INTn pin low.
1	PHYIntEn	RWR	PHY Interrupt Enable. This bit must be set to a one to allow active interrupts enabled in PHY registers 0x12 to drive the 88E6060 INTn pin low.
0	EEIntEn	RWS	EEPROM Done Interrupt Enable. This bit must be set to a one to allow the EEPROM Done interrupt to drive the 88E6060 INTn pin low.

Note

Registers 0x05 - 0x09 (Hex), or 5 - 9 (Decimal) are reserved.

Table 54: ATU Control Register
Offset: 0x0A (Hex), or 10 (Decimal)

Bits	Field	Type	Description
15	SWReset	SC	Switch Software Reset. Writing a one to this bit causes the QC and the MAC state machines in the switch to be reset. Register values are not modified, except for the PortState bits (Table 44 on page 94) and the EEPROM is not re-read. The PHYs and ATU are not affected by this bit. When the reset operation finishes, this bit is cleared to a zero automatically. The reset occurs immediately. To prevent transmission of CRC frames, set all of the ports to the Disabled state (Table 44 on page 94) and wait for 2 ms (i.e., the time for a maximum frame to be transmitted at 10 Mbps) before setting the SWReset bit to a one.
14	LearnDis	RWR	ATU Learn Disable. 0 = Normal operation, learning is determined by the PortState (Table 44, on page 94) 1 = Automatic learning is disabled on all ports – CPU ATU loads still work
13:12	ATUSize	RWS to 0x2	Address Translation Unit Table Size. The initial size of the ATU database is 1024 entries. The size of the ATU database can be modified at any time, but an ATU reset and a Switch Software Reset (bit 15 above) occurs automatically if the new ATUSize is different from the old ATUSize. 00 = 256 Entry Address Database 01 = 512 Entry Address Database 10 = 1024 Entry Address Database = default 11 = Reserved
11:4	AgeTime	RWS to 0x13	ATU Age Time. These bits determine the time that each ATU Entry remains valid in the database, since its last access as a Source Address, before being purged. The value in this register times 16 is the age time in seconds. For example: The default value of 0x13 is 19 decimal. 19 x 16 = 304 seconds or just over 5 minutes. The minimum age time is 0x1 or 16 seconds. The maximum age time is 0xFF or 4080 seconds or 68 minutes. When the AgeTime is set to 0x0 the Aging function is disabled, and all learned addresses will remain in the database forever.
3:0	Reserved	RES	Reserved for future use.

Table 55: ATU Operation Register
Offset: 0x0B (Hex), or 11 (Decimal)

Bits	Field	Type/ Reset Value	Description
15	ATUBusy	SC	Address Translation Unit Busy. This bit must be set to a one to start an ATU operation (see ATUOp below). Since only one ATU operation can be executing at one time, this bit must be zero before setting it to a one. When the requested ATU operation completes, this bit is automatically cleared to a zero. The transition of this bit from a one to a zero can be used to generate an interrupt (Table 49, on page 99).
14:12	ATUOp	RWR	Address Translation Unit Table Opcode. The 88E6060 device supports the following ATU operations. All of these operations can be executed while frames are transiting through the switch: 000 = No Operation 001 = Flush All Entries[1] 010 = Flush all Unlocked Entries[2] 011 = Load or Purge an Entry[3] in a particular DBNum Database 100 = Get Next from a particular DBNum Database[4] 101 = Flush All Entries in a particular DBNum Database 110 = Flush All Unlocked Entries in a particular DBNum Database 111 = Reserved
11:4	Reserved	RES	Reserved for future use.
3:0	DBNum	RWR	ATU MAC Address Database Number. If multiple address databases are not being used, these bits must remain zero. If multiple address databases are being used these bits are used to set the required address database number that is to be used on the Database supported commands (ATUOps 0x3, 0x4, 0x5, and 0x6 above).

1. All frames flood until new addresses are learned.
2. An Unlocked entry is any unicast address with an EntryState less than 0xF.
3. An Entry is Loaded if the EntryState (Table 56, on page 104) is non-zero. An Entry is Purged if it exists and if the EntryState is zero.
4. A Get Next operation finds the next higher MAC address currently in a particular ATU database (defined by the DBNum field). The ATUByte[5:0] values (Table 57, on page 104) are used as the address to start from. To find the lowest MAC address set ATUByte[5:0] to ones. When the operation is done ATUByte[5:0] contains the next higher MAC address found. To find the next address simply issue the Get Next opcode again. If ATUByte[5:0] is returned set to all ones, no higher MAC address was found (if EntryState = 0) or the Broadcast Address was found (if EntryState ≠ 0) In either case, the end of the table was reached. To Search for a particular address, perform a Get Next operation using a MAC address with a value one less than the one being searched for.

Table 56: ATU Data Register
Offset: 0x0C (Hex), or 12 (Decimal)

Bits	Field	Type	Description
15:10	Reserved	RES	Reserved for future use.
9:4	PortVec	RWR	Port Vector. These bits are used as the input Port Vector for ATU load operation. It is the resulting Port Vector from the ATU Get Next operation.
3:0	EntryState	RWR	ATU Entry State. These bits are used as the input Entry State for ATU Load or purge operations. It is the resulting Entry State from the ATU Get Next operation. (See Table 22 for a description of this function.)

Table 57: ATU Switch MAC Address Register Bytes 0 & 1
Offset: 0x0D (Hex), or 13 (Decimal)

Bits	Field	Type	Description
15:8	ATUByte0	RWR	ATU MAC Address Byte 0 (bits 47:40) is used as the input MAC address for ATU load, purge, or Get Next operations. It is the resulting MAC address from ATU Get Next operation. Bit 0 of byte 0 (bit 40) is the multicast bit (it is the 1st bit down the wire). Any MAC address with the multicast bit set to a one is considered locked by the ATU.
7:0	ATUByte1	RWR	ATU MAC Address Byte 1 (bits 39:32) is used as the input MAC address for ATU load, purge, or Get Next operations. It is the resulting MAC address from the ATU Get Next operation.

Table 58: ATU Switch MAC Address Register Bytes 2 & 3
Offset: 0x0E (Hex), or 14 (Decimal)

Bits	Field	Type	Description
15:8	ATUByte2	RWR	ATU MAC Address Byte 2 (bits 31:24) is used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.
7:0	ATUByte3	RWR	ATU MAC Address Byte 3 (bits 23:16) that are used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.

Table 59: ATU Switch MAC Address Register Bytes 4 & 5
Offset: 0x0F (Hex), or 15 (Decimal)

Bits	Field	Type	Description
15:8	ATUByte4	RWR	ATU MAC Address Byte 4 (bits 15:8) is used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.
7:0	ATUByte5	RWR	ATU MAC Address Byte 5 (bits 7:0) is used as the input MAC address for ATU load, purge or Get Next operations. It is the resulting MAC address from ATU Get Next operations.

Note

Registers 0x10 - 0x1F (Hex), or 16 - 31 (Decimal) are reserved.

Section 7. PHY Registers

The 88E6060 device contains five physical layer devices (PHYs). These devices are accessible using SMI device addresses 0x00 to 0x04 (or 0x10 to 0x14) depending upon the value of the EE_CLK/ADDR4 pin at reset. The PHYs are fully IEEE 802.3 compliant including their register interface.

The PHYs in the 88E6060 device are identical to those in the Marvell® 88E3082 Octal Transceiver except that there are five transceivers (transceivers 5 to 7 do not exist and are not accessible).

Table 60: PHY Register Map

Description	Offset Hex	Offset Decimal	Page Number
PHY Control Register	0x00	0	page 107
PHY Status Register	0x01	1	page 109
PHY Identifier	0x02	2	page 110
PHY Identifier	0x03	3	page 110
Auto-Negotiation Advertisement Register	0x04	4	page 111
Link Partner Ability Register (Base Page)	0x05	5	page 113
Link Partner Ability Register (Next Page)	0x05	5	page 113
Auto-Negotiation Expansion Register	0x06	6	page 114
Next Page Transmit Register	0x07	7	page 115
Link Partner Next Page Register	0x08	8	page 115
Reserved Registers	0x09-0x0F	9 - 15	page 116
PHY Specific Control Register I	0x10	16	page 116
PHY Specific Status Register	0x11	17	page 119
PHY Interrupt Enable	0x12	18	page 121
PHY Interrupt Status	0x13	19	page 122
PHY Interrupt Port Summary (Common register to all ports)	0x14	20	page 123
PHY Receive Error Counter	0x15	21	page 124
LED Parallel Select Register	0x16	22	page 125
LED Stream Select Register	0x17	23	page 126
PHY LED Control Register	0x18	24	page 128
PHY Manual LED Override Register	0x19	25	page 129
VCT™ Control Register	0x1A	26	page 130
VCT™ Status Register	0x1B	27	page 131
PHY Specific Control Register II	0x1C	28	page 132
Reserved Registers	0x1D to 0x1F	29 - 31	page 132

Table 61: PHY Control Register
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SWReset	SC	0x0	Self Clear	PHY Software Reset Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	Retain	0	Enable Loopback Mode When loopback mode is activated, the transmitter data presented on TXD is looped back to RXD internally. The PHY has to be in forced 10 or 100 Mbps mode. Auto-Negotiation must be disabled. 1 = Enable loopback 0 = Disable loopback
13	SpeedLSB	R/W	ANEG [2:0]	Update	Speed Selection (LSB) When a speed change occurs, the PHY drops link and tries to determine speed when Auto-Negotiation is on. Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to these registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15) or Power down (bit 11) transitions from power down to normal operation. 1 = 100 Mbps 0 = 10 Mbps
12	AnegEn	R/W	ANEG [2:0]	Update	Auto-Negotiation Enable Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to these registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15, above), Power down (bit 11, below), or transitions from power down to normal operation. If the AnegEn bit is set to 0, the speed and duplex bits of the PHY Control Register (Offset 0x00) take effect. If the AnegEn bit is set to 1, speed and duplex advertisement is found in the Auto-Negotiation Advertisement Register (Offset 0x04). 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process

Table 61: PHY Control Register (Continued)
Offset: 0x00 (Hex), or 0 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
11	PwrDwn	R/W	0x0	0x0	Power Down Mode When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (bit 15, above) and Restart Auto-Negotiation (bit 9, below) are not set by the user. 1 = Power down 0 = Normal operation
10	Isolate	RO	Always 0	Always 0	Isolate Mode Will always be 0. The Isolate function is not available, since full MII is not implemented. 0 = Normal operation
9	RestartAneg	SC	0x0	Self Clear	Restart Auto-Negotiation Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex	R/W	ANEG [2:0]	Update	Duplex Mode Selection Speed, Auto-Negotiation enable, and duplex enable take on the values set by ANEG[2:0] on hardware reset. A write to these registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15), Power down (bit 11), or transitions from power down to normal operation. 1 = Full-duplex 0 = Half-duplex
7	ColTest	RO	Always 0	Always 0	Collision Test Mode Will always be 0. The Collision test is not available, since full MII is not implemented. 0 = Disable COL signal test
6	SpeedMSB	RO	Always 0	Always 0	Speed Selection Mode (MSB) Will always be 0. 0 = 100 Mbps or 10 Mbps
5:0	Reserved	RO	Always 0	Always 0	Will always be 0.

Table 62: PHY Status Register
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100T4	RO	Always 0	Always 0	100BASE-T4 This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100FDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X full-duplex 1 = PHY able to perform full-duplex
13	100HDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X half-duplex 1 = PHY able to perform half-duplex
12	10FDX	RO	Always 1	Always 1	10BASE-T full-duplex 1 = PHY able to perform full-duplex
11	10HPX	RO	Always 1	Always 1	10BASE-T half-duplex 1 = PHY able to perform half-duplex
10	100T2FDX	RO	Always 0	Always 0	100BASE-T2 full-duplex. This protocol is not available. 0 = PHY not able to perform full-duplex
9	100T2HDX	RO	Always 0	Always 0	100BASE-T2 half-duplex This protocol is not available. 0 = PHY not able to perform half-duplex
8	ExtdStatus	RO	Always 0	Always 0	Extended Status 0 = No extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MFPreSup	RO	Always 1	Always 1	MF Preamble Suppression Mode Must be always 1. 1 = PHY accepts management frames with preamble suppressed
5	AnegDone	RO	0x0	0	Auto-Negotiation Complete 1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed
4	RemoteFault	RO, LH	0x0	0	Remote Fault Mode 1 = Remote fault condition detected 0 = Remote fault condition not detected
3	AnegAble	RO	Always 1	Always 1	Auto-Negotiation Ability Mode 1 = PHY able to perform Auto-Negotiation

Table 62: PHY Status Register (Continued)
Offset: 0x01 (Hex), or 1 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Link	RO, LL	0x0	0	Link Status Mode This register indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read RTLink in Table 72 on page 119. 1 = Link is up 0 = Link is down
1	JabberDet	RO, LH	0x0	0	Jabber Detect 1 = Jabber condition detected 0 = Jabber condition not detected
0	ExtdReg	RO	Always 1	Always 1	Extended capability mode. 1 = Extended register capabilities

Table 63: PHY Identifier
Offset: 0x02 (Hex), or 2 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	OUI MSb	RO	0x0141	0x0141	Organizationally Unique Identifier bits 3:18 0000000101000001 Marvell® OUI is 0x005043

Table 64: PHY Identifier
Offset: 0x03 (Hex), or 3 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits19:24
9:4	ModelNum	RO	Varies	Varies	Model Number = 001000
3:0	RevNum	RO	Varies	Varies	Revision Number Contact Marvell® FAEs for information on the device revision number.

Table 65: Auto-Negotiation Advertisement Register
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	AnegAd NxtPage	R/W	0x0	Retain	Next Page 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.
14	Ack	RO	Always 0	Always 0	Must be 0.
13	AnegAd ReFault	R/W	0x0	Retain	Remote Fault Mode 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.
12:11	Reserved	R/W	0x0	Retain	Must be 00. Reserved bits are R/W to allow for forward compatibility with future IEEE standards. Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.
10	AnegAd Pause	R/W	0x0	Retain	Pause Mode 1 = MAC Pause implemented 0 = MAC Pause not implemented Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.
9	AnegAd 100T4	RO	Always 0	Always 0	100BASE-T4 mode 0 = Not capable of 100BASE-T4
8	AnegAd 100FDX	R/W	0x1	Retain	100BASE-TX full-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.

Table 65: Auto-Negotiation Advertisement Register (Continued)
Offset: 0x04 (Hex), or 4 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
7	AnegAd 100HDX	R/W	0X1	Retain	100BASE-TX half-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.
6	AnegAd 10FDX	R/W	0X1	Retain	10BASE-TX full-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.
5	AnegAd 10HDX	R/W	0X1	Retain	10BASE-TX half-duplex Mode 1 = Advertise 0 = Not advertised Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg - Table 61 on page 107) or link goes down.
4:0	AnegAd Selector	RO	Always 0x01	Always 0x01	Selector Field Mode 00001 = 802.3

Table 66: Link Partner Ability Register (Base Page)
Offset: 0x05 (Hex), or 5 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxt Page	RO	0x0	0	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (Table 71 on page 116) is disabled. When Reg8NxtPg (Table 71 on page 116) is enabled, then next page is stored in the Link Partner Next Page register (Table 70 on page 115), and the Link Partner Ability Register (Table 66 on page 113) holds the base page. Received Code Word Bit 15
14	LPAck	RO	0x0	0	Acknowledge Received Code Word Bit 14
13	LPRemote Fault	RO	0x0	0	Remote Fault Received Code Word Bit 13
12:5	LPTechAble	RO	0x00	0x00	Technology Ability Field Received Code Word Bit 12:5
4:0	LPSelector	RO	00000	00000	Selector Field Received Code Word Bit 4:0

Table 67: Link Partner Ability Register (Next Page)
Offset: 0x05 (Hex), or 5 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxtPage	RO	--	--	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (Table 71 on page 116) is disabled. When Reg8NxtPg (Table 71 on page 116) is enabled, then next page is stored in the Link Partner Next Page register (Table 70 on page 115), and Link Partner Ability Register (Table 66 on page 113) holds the base page. Received Code Word Bit 15
14	LPAck	RO	--	--	Acknowledge Received Code Word Bit 14
13	LPMessage	RO	--	--	Message Page Received Code Word Bit 13
12	LPack2	RO	--	--	Acknowledge 2 Received Code Word Bit 12
11	LPToggle	RO	--	--	Toggle Received Code Word Bit 11

Table 67: Link Partner Ability Register (Next Page) (Continued)
Offset: 0x05 (Hex), or 5 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
10:0	LPData	RO	--	--	Message/Unformatted Field Received Code Word Bit 10:0

Table 68: Auto-Negotiation Expansion Register
Offset: 0x06 (Hex), or 6 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	Always 0x000	Always 0x000	Reserved. Must be 00000000000. The Auto-Negotiation Expansion Register is not valid until the AnegDone (Table 62 on page 109) indicates completed.
4	ParFaultDet	RO	0x0	0x0	Parallel Detection Level 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	LPNxtPg Able	RO	0x0	0x0	Link Partner Next Page Able 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	LocalNxtPg Able	RO	Always 0x1	Always 0x1	Local Next Page Able This bit is equivalent to AnegAble (Table 62 on page 109). 1 = Local Device is Next Page able
1	RxNewPage	RO/LH	0x0	0x0	Page Received 1 = A New Page has been received 0 = A New Page has not been received
0	LPAnegAble	RO	0x0	0x0	Link Partner Auto-Negotiation Able 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 69: Next Page Transmit Register
Offset: 0x07 (Hex), or 7 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TxNxtPage	R/W	0x0	0x0	Next Page A write to the Next Page Transmit Register implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Reserved Transmit Code Word Bit 14
13	TxMessage	R/W	0x1	0x1	Message Page Mode Transmit Code Word Bit 13
12	TxAck2	R/W	0x0	0x0	Acknowledge2 Transmit Code Word Bit 12
11	TxToggle	RO	0x0	0x0	Toggle Transmit Code Word Bit 11
10:0	TxData	R/W	0x001	0x001	Message/Unformatted Field Transmit Code Word Bit 10:0

Table 70: Link Partner Next Page Register
Offset: 0x08 (Hex), or 8 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RxNxtPage	RO	0x0	0x0	Next Page If Reg8NxtPg (Table 71 on page 116) is enabled, then next page is stored in the Link Partner Next Page register (Table 70 on page 115); otherwise, theLink Partner Next Page register (Table 70 on page 115) is cleared to all 0's. Received Code Word Bit 15
14	RxAck	RO	0x0	0x0	Acknowledge Received Code Word Bit 14
13	RxMessage	RO	0x0	0x0	Message Page Received Code Word Bit 13
12	RxAck2	RO	0x0	0x0	Acknowledge 2 Received Code Word Bit 12
11	RxToggle	RO	0x0	0x0	Toggle Received Code Word Bit 11
10:0	RxData	RO	0x001	0x000	Message/Unformatted Field Received Code Word Bit 10:0

Note

Registers 0x09 through 0x0F (hexadecimal (9 through 15 decimal) are reserved. Do not read or write to these registers.

Table 71: PHY Specific Control Register
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--	--	Reserved.
14	EDet	R/W	ENA_ EDET	Retain	Energy Detect 1 = Enable with sense and pulse 0 = Disable Enable with sense only is not supported Enable Energy Detect takes on the appropriate value defined by the CONFIG9 pin at hardware reset.
13	DisNLP Check	R/W	0x0	0x0	Disable Normal Linkpulse Check Linkpulse check and generation disable have no effect, if Auto-Negotiation is enabled locally. 1 = Disable linkpulse check 0 = Enable linkpulse check
12	Reg8NxtPg	R/W	0x0	0x0	Enable the Link Partner Next Page register (Table 67 on page 113) to store Next Page. If set to store next page in the Link Partner Next Page register (Table 67 on page 113), then 802.3u is violated to emulate 802.3ab. 1 = Store next page in the Link Partner Next Page register (Table 67 on page 113) 0 = Store next page in the Link Partner Ability Register (Base Page) register (Table 66 on page 113).
11	DisNLPGen	R/W	0x0	0x0	Disable Linkpulse Generation. Linkpulse check and generation disable have no effect, when Auto-Negotiation is enabled locally. 1 = Disable linkpulse generation 0 = Enable linkpulse generation
10	ForceLink	R/W	0x0	0x0	Force Link Good When link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	DisScrambler	R/W	ANEG [2:0]	Retain	Disable Scrambler If fiber mode is selected then the scrambler is disabled at hardware reset. 1 = Disable scrambler 0 = Enable scrambler

Table 71: PHY Specific Control Register (Continued)
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
8	DisFEFI	R/W	DIS_ FEFI ANEG [2:0]	Retain	Disable FEFI In 100BASE-FX mode, Disable FEFI takes on the appropriate value defined by the CONFIG8 pin at hardware reset. FEFI is automatically disabled regardless of the state of this bit if copper mode is selected. 1 = Disable FEFI 0 = Enable FEFI For the 88E3083 device, this bit applies to Port 7 only.
7	ExtdDistance	R/W	0x0	0x0	Enable Extended Distance When using cable exceeding 100 meters, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 1 = Lower 10BASE-T receive threshold 0 = Normal 10BASE-T receive threshold
6	TPSelect	R/W	ANEG [2:0]	Update	(Un)Shielded Twisted Pair This setting can be changed by writing to this bit followed by software reset. 1 = Shielded Twisted Pair 0 = Unshielded Twisted Pair - default
5:4	AutoMDI[X]	R/W	ENA_ XC,1	Update	MDI/MDIX Crossover This setting can be changed by writing to these bits followed by software reset. If ENA_XC is 1 at hardware reset then bits 5:4 = 11 00 = Transmit on pins RXP/RXN, Receive on pins TXP/TXN 01 = Transmit on pins TXP/TXN, Receive on pins RXP/RXN 1x = Enable Automatic Crossover
3:2	RxFIFO Depth	R/W	0x0	0x0	Receive FIFO Depth 00 = 4 Bytes 01 = 6 Bytes 10 = 8 Bytes 11 = Reserved
1	AutoPol	R/W	0x0	00	Polarity Reversal If polarity is disabled, then the polarity is forced to be normal in 10BASE-T mode. Polarity reversal has no effect in 100BASE-TX mode. 1 = Disable automatic polarity reversal 0 = Enable automatic polarity reversal

Table 71: PHY Specific Control Register (Continued)
Offset: 0x10 (Hex), or 16 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
0	DisJabber	R/W	0x0	00	Disable Jabber Jabber has no effect in full-duplex or in 100BASE-X mode. 1 = Disable jabber function 0 = Enable jabber function

Table 72: PHY Specific Status Register
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--	--	Reserved
14	ResSpeed	RO	ANEG [2:0]	Retain	Resolved Speed Speed and duplex takes on the values set by ANEG[2:0] pins on hardware reset only. The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. 1 = 100 Mbps 0 = 10 Mbps
13	ResDuplex	RO	ANEG [2:0]	Retain	Resolved Duplex Mode Speed and duplex takes on the values set by ANEG[2:0] pins on hardware reset only. The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. This bit is valid only after the resolved bit 11 is set. 1 = Full-duplex 0 = Half-duplex
12	RcvPage	RO, LH	0x0	0x0	Page Receive Mode 1 = Page received 0 = Page not received
11	Resolved	RO	0x0	0x0	Speed and Duplex Resolved. Speed and duplex bits (14 and 13) are valid only after the Resolved bit is set. The Resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Resolved 0 = Not resolved
10	RTLink	RO	0x0	0x0	Link (real time) 1 = Link up 0 = Link down
9:7	Reserved	RES	0x0	0x0	Must be 000.
6	MDI/MDIX	RO	0x1	0x1	MDI/MDIX Crossover Status 1 = Transmit on pins RXP/RXN, Receive on pins TXP/TXN 0 = Transmit on pins TXP/TXN, Receive on pins RXP/RXN
5	Reserved	RES	0x4	0x4	Must be 0.
4	Sleep	RO	0	0x0	Energy Detect Status 1 = Chip is in sleep mode (No wire activity) 0 = Chip is not in sleep mode (Active)
3:2	Reserved	RES	0x0	0x0	Must be 00.

Table 72: PHY Specific Status Register (Continued)
Offset: 0x11 (Hex), or 17 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
1	RTPolarity	RO	0x0	0x0	Polarity (real time) 1 = Reversed 0 = Normal
0	RTJabber	RO	Retain	0x0	Jabber (real time) 1 = Jabber 0 = No Jabber

Table 73: PHY Interrupt Enable
Offset: 0x12 (Hex), or 18 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--	--	Reserved
14	SpeedIntEn	R/W	0x0	Retain	Speed Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
13	DuplexIntEn	R/W	0x0	Retain	Duplex Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
12	RcvPageIntEn	R/W	0x0	Retain	Page Received Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
11	AnegDone IntEn	R/W	0x0	Retain	Auto-Negotiation Completed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
10	LinkIntEn	R/W	0x0	Retain	Link Status Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
9	SymErrIntEn	R/W	0x0	Retain	Symbol Error Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
8	FlsCrsIntEn	R/W	0x0	Retain	False Carrier Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
7	FIFOErrInt	R/W	0x0	Retain	FIFO Over/Underflow Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
6	MDI[x]IntEn	R/W	0x0	0x0	MDI/MDIX Crossover Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
5	Reserved	RES	0x0	Retain	Must be 0.
4	EDetIntEn	R/W	0x0	Retain	Energy Detect Interrupt Enable 1 = Enable 0 = Disable
3:2	Reserved	RES	0x0	Retain	Must be 00.
1	PolarityIntEn	R/W	0x0	Retain	Polarity Changed Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable
0	JabberIntEn	R/W	0x0	Retain	Jabber Interrupt Enable 1 = Interrupt enable 0 = Interrupt disable

Table 74: PHY Interrupt Status
Offset: 0x13 (Hex), or 19 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RES	--	--	Reserved
14	SpeedInt	RO, LH	0x0	0x0	Speed Changed 1 = Speed changed 0 = Speed not changed
13	DuplexInt	RO, LH	0x0	0x0	Duplex Changed 1 = Duplex changed 0 = Duplex not changed
12	RxPageInt	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	AnegDoneInt	RO, LH	0x0	0x0	Auto-Negotiation Completed 1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	LinkInt	RO, LH	0x0	0x0	Link Status Changed 1 = Link status changed 0 = Link status not changed
9	SymErrInt	RO, LH	0x0	0x0	Symbol Error 1 = Symbol error 0 = No symbol error
8	FlsCrsInt	RO, LH	0x0	0x0	False Carrier 1 = False carrier 0 = No false carrier
7	FIFOErrInt	RO, LH	0x0	0x0	FIFO Over /Underflow Error 1 = Over/underflow error 0 = No over/underflow error
6	MDIMDIXInt	RO, LH	0x0	0x0	MDI/MDIX Crossover Changed 1 = MDI/MDIX crossover changed 0 = MDI/MDIX crossover not changed
5	Reserved	RO	Always 0	Always 0	Must be 0
4	EDetChg	RO, LH	0x0	0x0	Energy Detect Changed 1 = Changed 0 = No Change
3:2	Reserved	RO	0x0	0x0	Must be 00
1	PolarityInt	RO	0x0	0x0	Polarity Changed 1 = Polarity changed 0 = Polarity not changed
0	JabberInt	RO, LH	0x0	0x0	Jabber Mode 1 = Jabber 0 = No Jabber

Table 75: PHY Interrupt Port Summary (Global[1])
Offset: 0x14 (Hex), or 20 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x0	0x0	Must be 00000000000.
4	Port4Int Active	RO	0x0	0x0	Port 4 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt
3	Port3Int Active	RO	0x0	0x0	Port 3 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt
2	Port2Int Active	RO	0x0	0x0	Port 2 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt
1	Port1Int Active	RO	0x0	0x0	Port 1 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt
0	Port0Int Active	RO	0x0	0x0	Port 0 Interrupt Active Bit is set high, if any enabled interrupt is active for the port. Bit is cleared only when all bits in register 19 are cleared. 1 = Port has active interrupt 0 = Port does not have active interrupt

1. This global register is accessible for writing or reading from any PHY port (i.e., only one physical register exists for all the PHY Ports).

Table 76: Receive Error Counter
Offset: 0x15 (Hex), or 21 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RxErrCnt	RO	0x0000	0x0000	Receive Error Count This register counts receive errors on the media interface. When the maximum receive error count reaches 0xFFFF, the counter will not roll over.

Table 77: LED Parallel Select Register (Global)[1] [2]
Offset: 0x16 (Hex), or 22 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RES	0000	Retain	Must be 0000
11:8	LED2	R/W	LED[1:0] 00 = LINK 01 = LINK 10 = LINK/RX 11= LINK ACT	Retain	LED2 Control The parallel LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1011 = ACT (BLINK mode), 1100 to 1111 = Force to 1
7:4	LED1	R/W	LED[1:0] 00 = RX 01 = ACT 10 = TX 11= DUPLEX /COLX	Retain	LED1 Control The parallel LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1011 = ACT (BLINK mode), 1100 to 1111 = Force to 1
3:0	LED0	R/W	LED[1:0] 00 = TX 01 = SPEED 10 = SPEED 11= SPEED	Retain	LED0 Control The parallel LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 0000 = COLX, 0001 = ERROR, 0010 = DUPLEX, 0011 = DUPLEX/COLX, 0100 = SPEED, 0101 = LINK, 0110 = TX, 0111 = RX, 1000 = ACT, 1001 = LINK/RX, 1011 = ACT (BLINK mode), 1100 to 1111 = Force to 1

1. See Table 34 on page 80 and Table 35 on page 81 for parallel LED display modes that can be selected by hardware pin configuration at reset.
2. This global register is accessible for writing or reading from any PHY port (i.e., only one physical register exists for all the PHY Ports).

Table 78: LED Stream Select for Serial LEDs
Offset: 0x17 (Hex), or 23 (Decimal)

Bits	Function	Mode	HW Rst	SW Rst	Description
15:14	LEDLnkActy	R/W	LED[1:0]	Retain	LED Link Activity The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
13:12	LEDRcvLnk	R/W	LED[1:0]	Retain	LED Receive Link The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
11:10	LEDActy	R/W	LED[1:0]	Retain	LED Activity The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
9:8	LEDRcv	R/W	LED[1:0]	Retain	LED Receive The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
7:6	LEDTx	R/W	LED[1:0]	Retain	Transmit The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
5:4	LEDLnk	R/W	LED[1:0]	Retain	Link The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single

Table 78: LED Stream Select for Serial LEDs (Continued)
Offset: 0x17 (Hex), or 23 (Decimal)

Bits	Function	Mode	HW Rst	SW Rst	Description
3:2	LEDSpd	R/W	LED[1:0]	Retain	Speed The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single
1:0	LEDDx/ COLX	R/W	LED[1:0]	Retain	LED Duplex/ COLX The serial LED settings take on the appropriate value defined by the CONFIG_A pin at hardware reset. 00 = Off 01 = Reserved 10 = Dual 11 = Single

Table 79: PHY LED Control Register (Global[1])
Offset: 0X18 (Hex), 0r 24 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Must be 0.
14:12	PulseStretch	R/W	0x4	Retain	Pulse stretch duration. Default Value = 100. 000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11:9	BlinkRate	R/W	0x1	Retain	Blink Rate. This is a global setting. Default Value = 001 000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
8:6	SrStrUpdate	R/W	0x2	Retain	Serial Stream Update 000 = 10 ms 001 = 21 ms 010 = 42 ms 011 = 84 ms 100 = 170 ms 101 = 340 ms 110 to 111 = Reserved
5:4	Duplex	R/W	LED[1:0] 00 = Off 01 = Single 10 = Single 11 = Single	Retain	00 = Off 01 = Reserved 10 = Dual 11 = Single
3:2	Error	R/W	11	Retain	00 = Off 01 = Reserved 10 = Dual 11 = Single
1:0	COLX	R/W	LED[1:0] 00 = Off 01 = Single 10 = Single 11 = Single	Retain	00 = Off 01 = Reserved 10 = Dual 11 = Single

1. This global register is accessible for writing or reading from any PHY port (i.e., only one physical register exists for all the PHY Ports).

Table 80: PHY Manual LED Override
Offset: 0x19 (Hex), or 25 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	R/W	0x0	Retain	0000000000
5:4	LED2	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On
3:2	LED1	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On
1:0	LED0	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On

Table 81: VCT™ Register for TXP/N Pins
Offset: 0x1A[1] (Hex), or 26 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EnVCT	R/W, SC	0x0	0x0	Enable VCT The 88E6060 device must be in forced 100 Mbps mode before enabling this bit. 1 = Run VCT 0 = VCT completed After running VCT once, bit 15 = 0 indicates VCT completed. The cable status is reported in the VCTTst bits in registers 26 and 27. Refer to the “Virtual Cable Tester™” feature in section 4.5.
14:13	VCTTst	RO	0x0	Retain	VCT Test Status These VCT test status bits are valid after completion of VCT. 11 = Test fail 00 = valid test, normal cable (no short or open in cable) 10 = valid test, open in cable (Impedance > 333 ohm) 01 = valid test, short in cable (Impedance < 33 ohm)
12:8	AmpRfln	RO	0x0	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bits 14:13) have not indicated test failure.
7:0	DistRfln	RO	0x0	Retain	Distance of Reflection These bits refer to the approximate distance (±1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs). See Figure 26. These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bit 14:13) have not indicated test failure.

1. The results stored in this register apply to the TX pin pair.

Table 82: VCT™ Register for RXP/N pins
Offset: 0x1B[1] (Hex), or 27 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Reserved
14:13	VCTTst	RO	0	Retain	VCT Test Status The VCT test status bits are valid after completion of VCT. 11 = Test fail 00 = valid test, normal cable (no short or open in cable) 10 = valid test, open in cable (Impedance > 333 ohm) 01 = valid test, short in cable (Impedance < 33 ohm)
12:8	AmpRfln	RO	0	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bit 14:13) have not indicated test failure.
7:0	DistRfln	RO	0	Retain	Distance of Reflection These bits refer to the approximate distance (±1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs). See Figure 26. These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bits 14:13) have not indicated test failure.

1. The results stored in this register apply to the RX pin pair.

Figure 26: Cable Fault Distance Trend Line

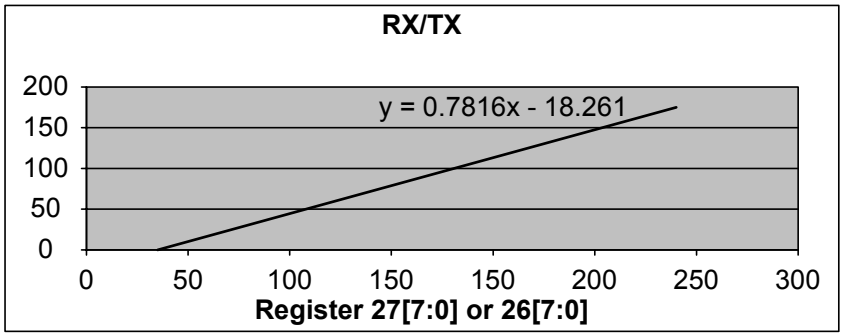


Table 83: PHY Specific Control Register II
Offset: 0x1C (Hex), or 28 (Decimal)

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0	0x0	Must be 000000000000000
0	SelClsA	R/W	SEL_ CLASS A	Update	1 = Select Class A driver; available for 100BASE-TX mode only —typically used in backplane or direct connect applications 0 = Select Class B driver—typically used in CAT 5 applications

Note

Registers 0x1D through 0x1F (hexadecimal (29 through 31 decimal) are reserved. Do not read or write to these registers.

Section 8. EEPROM Programming Format

8.1 EEPROM Programming Details

The 88E6060 device supports an optional external serial EEPROM device for programing its internal registers. The EEPROM data is read in once after RESETn is deasserted if the stand alone Switch Mode is not selected (see Table 14 on page 29).

The 88E6060 supports 1K bit (93C46), 2K bit (93C56), or 4K bit (93C66) EEPROM devices. The size of the device is selected by the EE_DIN/EE_1K pin at reset—see Table 7 on page 21. The external EEPROM device must be configured in x16 data organization mode.

Regardless of which particular device is attached, the EEPROM is read and processed in the same way:

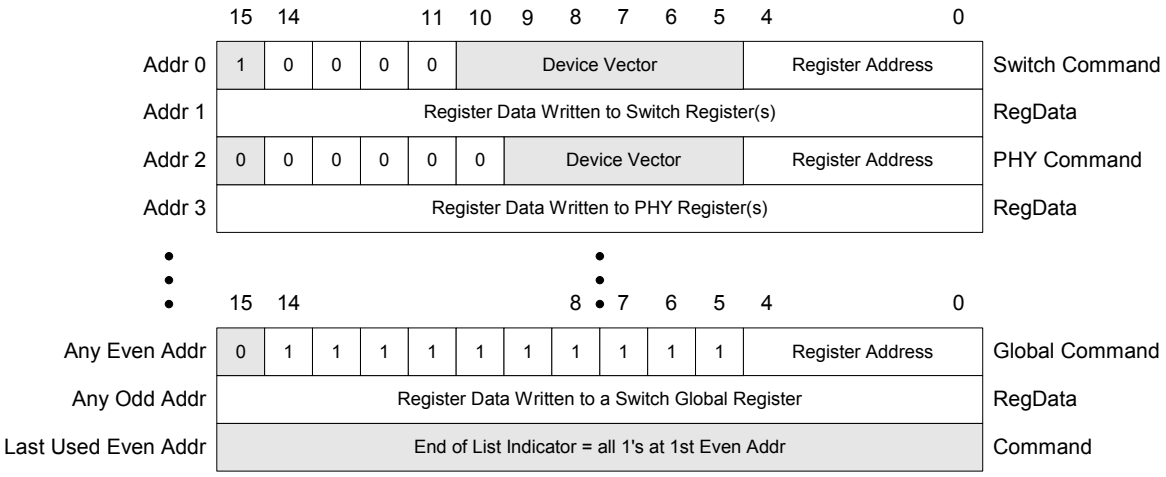
1. Start at EEPROM address 0x00.
2. Read in the 16 bits of data from the even address. This step is called the Command.
3. If the just read in Command is all ones, terminate the serial EEPROM reading process and go to step 8.
4. Increment the address by 1—to the next address.
5. Read in the 16 bits of data from that address—This is called the RegData.
6. Write RegData to the locations defined by the previous Command.
7. Go to step 2.
8. Set the EEInt bit in Global Status to a one (Table 49, on page 99) generating an Interrupt (if enabled).
9. Done.

The 16-bit Command determines which register or registers inside the 88E6060 are updated as follows. Refer to Figure 27 below.

- Bit 15 determines which set of registers can be written.
  If bit 15 = 0 the PHY registers can be written (SMI Device Addresses 0x00 to 0x04) or the Switch Global registers can be written (SMI Device Address 0x7).
  If bit 15 = 1 the Switch registers can be written (SMI Device Addresses 0x08 to 0x0D). See section 6 and Figure 25 for more information on the registers and their addresses.
- Bits 10:5 (or 9:5), the Device Vector, determines which Device Addresses are written. Each bit of the Device Vector that is set to a one causes one Device Address to be written. Bit 5 controls writes for Port 0 (either PHY address 0x00 or Switch address 0x08).
- Bit 6 controls writes for Port 1 (either PHY address 0x01 or Switch address 0x09).
- Bit 7 controls writes for Port 2, etc.
- The Switch Global registers (Switch address 0x0F) are written when bit 15 is a zero and bits 14:5 are ones. Care is needed to ensure that Reserved registers are not written.
- Bits 4:0, the Register Address, determine which SMI Register Address is written.

The format of the EEPROM Commands supports writing the same RegData to all the PHYs or all the Switch's MACs with one Command/RegData pair. The Command/RegData list can be as short or as long as needed. This makes optimum use of the limited number of Command/RegData pairs that can fit in a given size EEPROM[1]. The maximum number of Command/RegData pairs is one fewer than might be expected from a simple calculation because the last entry must be the End of List or Halt Indicator of all ones.

Figure 27: EEPROM Data Format



1. 31 in the 93C46, 63 in the 93C56, and 127 in the 93C66 EEPROM.

Section 9. Electrical Specifications

9.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 84: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on V_{DDO} with respect to V_{SS}	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on V_{DDAH} with respect to V_{SS}	-0.5	2.5	+3.6 or $V_{DD(3.3)}$ +0.5[1] whichever is less	V
$V_{DD(1.5)}$	Power Supply Voltage on V_{DD}, or V_{DDAL} with respect to V_{SS}	-0.5	1.5	+3.6 or $V_{DD(2.5)}$ +0.5[2] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to V_{SS}	-0.5		+3.6 or V_{DDO} +0.5[3] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[4]	°C

1. VDD(2.5) must never be more than 0.5V greater than VDD(3.3) or damage will result. This implies that power must be applied to VDD(3.3) before or at the same time as VDD(2.5).
2. VDD(1.5) must never be more than 0.5V greater than VDD(2.5) or damage will result. This implies that power must be applied to VDD(2.5) before or at the same time as VDD(1.5).
3. VPIN must never be more than 0.5V greater than VDDO or damage will result.
4. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

9.2 Recommended Operating Conditions

Table 85: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For pins V_{DDO}	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For pins V_{DDAH}	2.375	2.5	2.625	V
$V_{DD(1.5)}$	1.5V power supply	For pins V_{DD}, V_{DDAL}	1.425	1.5	1.575	V
T_A	Ambient operating temperature	Commercial Parts	0		70	°C
		Industrial Parts[1]	-40		85	°C
T_J	Maximum junction temperature				125[2]	°C
RSET	Internal bias reference	Resistor value placed between RSET- and RSET+ pins	1980	2000	2020	Ω

1. Industrial part numbers have an “I” following the commercial part numbers. See “Ordering Information” on page 162.
2. Refer to white paper on TJ Thermal Calculations for more Information.

9.3 Package Thermal Information

9.3.1 Thermal Conditions for 128-pin PQFP Package

Table 86: Thermal Conditions for 128-pin PQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 88E6060 device 128-Pin PQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		33.1		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		30.3		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		29.1		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		28.3		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 88E6060 device 128-Pin PQFP package $\psi_{JT} = (T_J - T_c)/P.$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		2.3		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E6060 device 128-Pin PQFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package Thermal resistance[1] - junction to board of the 88E6060 device 128-Pin PQFP package	JEDEC with no air flow		16.7		°C/W
θ_{JB}	$\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		25.7		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

9.4 DC Electrical Characteristics

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 87: DC Electrical Characteristics

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
$I_{DD(3.3)}$	3.3 volt Power to outputs	V_{DDO}	No link on any port		15		mA
			All ports 10 Mbps		17		mA
			All ports 100 Mbps		22		mA
			Power Down Mode		18		mA
			Sleep Mode		18		mA
$I_{DD(2.5)}$	2.5 volt[2] Power to analog core	VDDAH	No link on any port		40		mA
			All ports 10 Mbps and active		126		mA
			All ports 100 Mbps		111		mA
			Power Down Mode		32		mA
			Sleep Mode		36		mA
	2.5 volt[3] Power to Center Tap	External Magnetics Center Tap Pin	No link on any port		10		mA
			All ports 10 Mbps and active		301		mA
			All ports 100 Mbps		103		mA
			Power Down Mode		0		mA
			Sleep Mode		0		mA
$I_{DD(1.5)}$	1.5 volt Power to analog core	V_{DDAL}	No link on any port		0		mA
			All ports 10 Mbps and active		1		mA
			All ports 100 Mbps		29		mA
			Power Down Mode		1		mA
			Sleep Mode		0		mA
	1.5 volt Power to digital core	V_{DD}	No link on any port		40		mA
			All ports 10 Mbps and active		54		mA
			All ports 100 Mbps and active		119		mA
			Power Down Mode		39		mA
			Sleep Mode		36		mA

1. The values listed are typical values with LED mode 3, 3 LEDs per port, and Auto-Negotiation on.
2. The 2.5V power source must supply an additional 100 mA (Typical) current from the center tap on the magnetics. (This number is not included in this table.)
3. The 2.5V power source must supply an additional 100 mA (Typical) current from the center tap on the magnetics. (This number is not included in this table.)

9.4.1 Digital Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 88: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	All pins		2.0		V_{DDO} +0.5	V
		XTAL_IN		1.4			V
V_{IL}	Low level input voltage	All pins		-0.5		0.8	V
		XTAL_IN				0.6	V
V_{OH}	High level output voltage	LED pins[1]	I_{OH} = -8 mA V_{DDO} = Min	2.4			V
		XTAL_OUT	I_{OH} = -1 mA		$V_{IH(XTAL\_IN)}$ +0.2		V
		All others	I_{OH} = -4 mA V_{DDO} = Min	2.4			V
V_{OL}	Low level output voltage	LED pins[1]	I_{OL}= 8 mA			0.4	V
		XTAL_OUT	I_{OL} = 1 mA		$V_{IL(XTAL\_IN)}$ -0.2		V
		INTn pin[2]	I_{OL}= 8 mA				V
		All others	I_{OL}= 4 mA			0.4	V
I_{ILK}	Input leakage current	With pull-up resistor (typ. 120 kΩ)	$0<V_{IN}<V_{DDO}$			+ 10 - 50	µA
		With pull-down resistor (typ. 120 kΩ)	$0<V_{IN}<V_{DDO}$			+ 50 - 10	µA
		All others	$0<V_{IN}<V_{DDO}$			±10	µA
C_{IN}	Input capacitance	All pins				5	pF

1. The LED pins are as follows: P4_LED2[2:0], P3_LED1[2:0], P2_LED2[2:0], P1_LED1[2:0], P0_LED1[2:0]

Table 89: Internal Resistor Description

Pin #	Pin Name	Resistor	Pin #	Pin Name	Resistor
34, 33	SW_MODE[1:0]	Internal pull-up	82	P5_INCLK	Internal pull-up
36	LEDSER	Internal pull-up	83, 84, 85, 86	P5_IND[3:0]	Internal pull-up
37	LEDCLK	Internal pull-up	87	P5_INDV	Internal pull-down
38	LEDENA	Internal pull-up	89	DISABLE_MII4	Internal pull-up
58	EE_DOUT	Internal pull-up	91	P4_CRS	Internal pull-down
60	EE_CLK/ ADDR4	Internal pull-up	93	CONFIG_B	Internal pull-up
61	EE_CS/ EE_1K	Internal pull-up	94	P4_COL	Internal pull-down
64	FD_FLOW_DIS	Internal pull-up	95, 96, 97, 98	P4_OUTD[3:0]/ P4_MODE[3:0]	Internal pull-up
66	ENABLE_MII5	Internal pull-up	99	P4_OUTCLK	Internal pull-up
68	CLK_SEL	Internal pull-up	102	P4_INCLK	Internal pull-up
69	EE_DIN/ HD_FLOW_DIS	Internal pull-up	106	CONFIG_A	Internal pull-up
70	MDC	Internal pull-up	108	P1_CONFIG	Internal pull-down
71	MDIO	Internal pull-up	110	RESETn	None
72	P5_CRS	Internal pull-down	111	P0_CONFIG	Internal pull-down
73	P5_COL	Internal pull-down	112, 114, 116, 117	P4_IND[3:0]	Internal pull-up
74, 75, 76, 77	P5_OUTD[3:0]/ P5_MODE[3:0]	Internal pull-up	118	P4_INDV	Internal pull-down
79	P5_OUTCLK	Internal pull-up	122	P0_SDET	None
81	P5_OUTDV/ WD_DIS	Internal pull-up	127	P1_SDET	None

9.4.2 IEEE DC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14
-100BASE-TX ANSI X3.263-1995
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 90: IEEE DC Transceiver Parameters

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	TXP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		TXP/N[1:0]	10BASE-T cable model	585[1]			mV
		TXP/N[0]	100BASE-FX mode	0.4	0.8	1.2	V
		TXP/N[1:0]	100BASE-TX mode	0.950	1.0	1.05	V
	Overshoot[2]	TXP/N[4:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/ negative)	TXP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage accept level	RXP/N[1:0]	10BASE-T mode	585[3]			mV
		RXP/N[0] P[1:0]_SDET P/N	100BASE-FX mode	200			mV
	Signal Detect Assertion	RXP/N[1:0]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	RXP/N[1:0]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. ANSI X3.263-1995 Figure 9-1.
3. The input test is actually a template test. IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The 88E6060 will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should be de-assert signal detect (internal signal in 100BASE-TX mode). The 88E6060 will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

9.5 AC Electrical Specifications

9.5.1 Reset and Configuration Timing

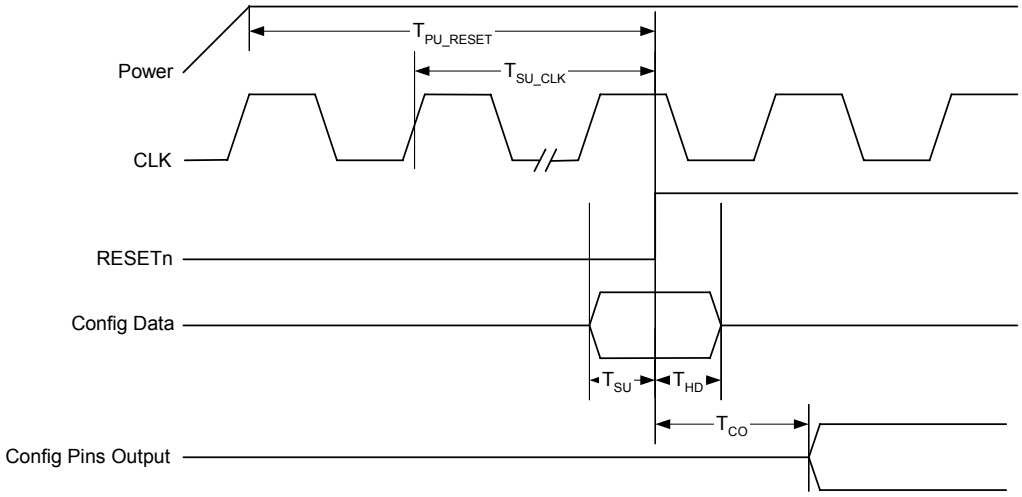
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Table 91: Reset and Configuration Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{PU_RESET}	Valid power to RESETn de-asserted or RESETn assertion time	At power up or subsequent resets after power up	10			ms	
T_{SU_CLK}	Number of valid XTAL_IN cycles prior to RESETn de-asserted		10			Cycles	
T_{SU}	Configuration data valid prior to RESETn de-asserted		200			ns	1
T_{HD}	Configuration data valid after RESETn de-asserted		0			ns	
T_{CO}	Configuration output driven after RESETn de-asserted		40			ns	2

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn.
2. P[x]_OUTD[3:0]/P[x]_MODE[3:0] are normally outputs that are also used to configure the 88E6060 device during hardware reset. When reset is asserted, these pins become inputs and the required LED configuration is latched at the rising edge of RESETn.

Figure 28: Reset and Configuration Timing



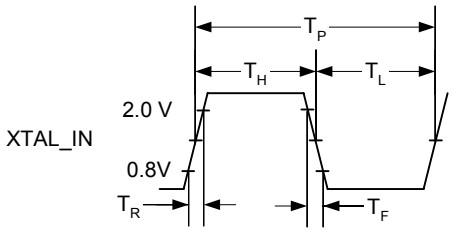
9.5.2 Clock Timing when using a 25 MHz Oscillator

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Table 92: Clock Timing with a 25 MHz Oscillator

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns	25 MHz
T_H	XTAL_IN high time		16			ns	
T_L	XTAL_IN low time		16			ns	
T_R	XTAL_IN rise				3	ns	
T_F	XTAL_IN fall				3	ns	

Figure 29: Oscillator Clock Timing



9.5.3 MII Receive Timing—PHY Mode

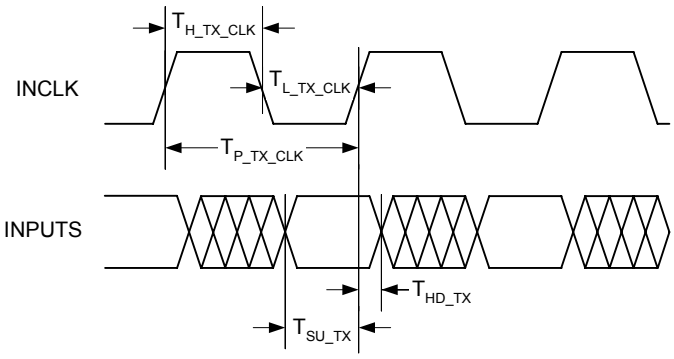
In PHY mode, the P[x]_INCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 93: MII Receive Timing—PHY Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_TX\_CLK}$	P[x]_INCLK period	10BASE mode		400		ns	1
		100BASE mode		40		ns	1
$T_{H\_TX\_CLK}$	P[x]_INCLK high	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
$T_{L\_TX\_CLK}$	P[x]_INCLK low	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		15			ns	
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high.		0			ns	

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 30: PHY Mode MII Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

9.5.4 MII Transmit Timing—PHY Mode

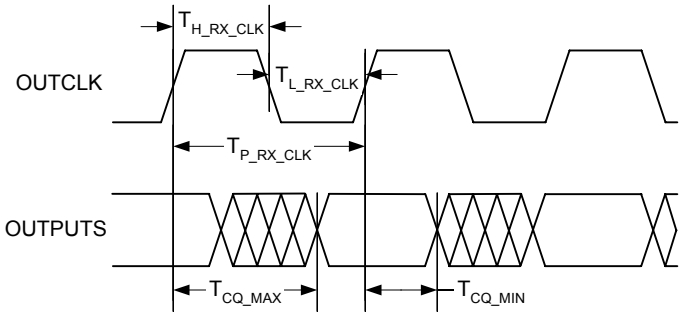
In PHY mode, the P[x]_OUTCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 94: MII Transmit Timing—PHY Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RX\_CLK}$	P[x]_OUTCLK period	10BASE mode		400		ns	1
		100BASE mode		40		ns	1
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	10BASE mode	160	200	240	ns	
		100BASE mode	16	20	24	ns	
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV) valid				25	ns	
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTDV) invalid		10			ns	

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 31: PHY Mode MII Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an output in this mode.

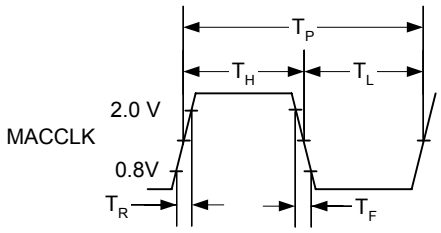
9.5.5 MAC Mode Clock Timing

In MAC mode, INCLK and OUTCLK are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 95: MAC Mode Clock Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MACCLK_IN period		0	4 or 40	40 +50 ppm	ns	DC to 25 MHz
T_H	MACCLK_IN high time		16			ns	
T_L	MACCLK_IN low time		16			ns	
T_R	MACCLK_IN rise				3	ns	
T_F	MACCLK_IN fall				3	ns	

Figure 32: MAC Clock Timing



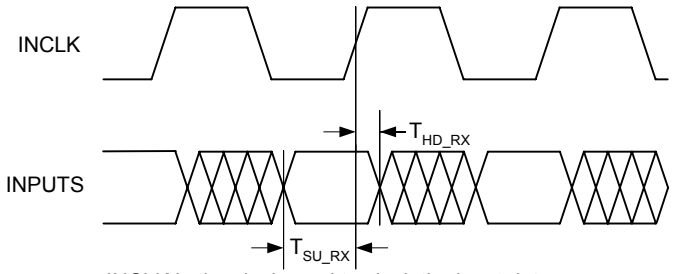
9.5.6 MII Receive Timing—MAC Mode

In MAC mode, the P[x]_INCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 96: MII Receive Timing—MAC Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	10			ns	
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	10			ns	

Figure 33: MAC Mode MII Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an input in this mode.

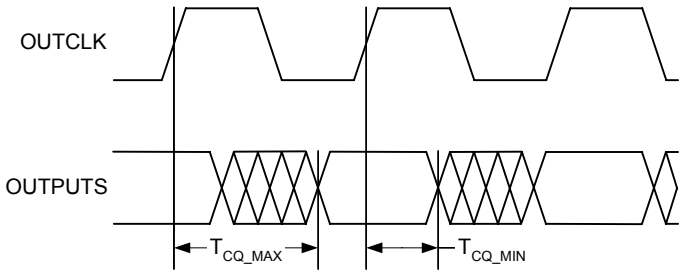
9.5.7 MII Transmit Timing—MAC Mode

In MAC mode, the P[x]_OUTCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 97: MII Transmit Timing—MAC Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV) valid	With 10 pF load			25	ns	
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV) invalid	With 10 pF load	0			ns	

Figure 34: MAC Mode MII Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data. It is an input in this mode.

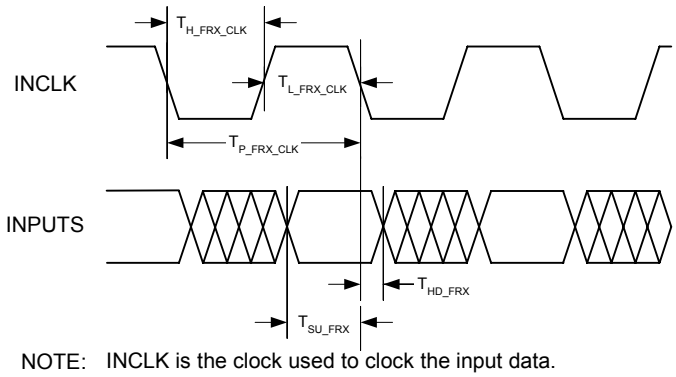
9.5.8 SNI Falling Edge Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 98: SNI Falling Edge Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_FRX\_CLK}$	SNI falling edge INCLK period	10BASE-T Mode		100		ns	
$T_{H\_FRX\_CLK}$	SNI falling edge INCLK high		35	50	65	ns	
$T_{L\_FRX\_CLK}$	SNI falling edge INCLK low		35	50	65	ns	
T_{SU_FRX}	SNI receive data valid prior to INCLK going low		20			ns	
T_{HD_FRX}	SNI receive data valid after INCLK going low		10			ns	

Figure 35: SNI Falling Edge Receive Timing



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

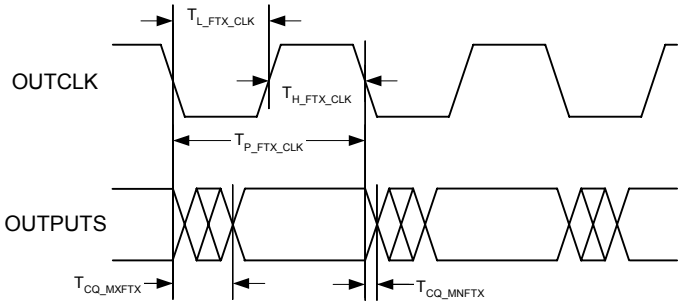
9.5.9 SNI Falling Edge Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 99: SNI Falling Edge Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_FTX\_CLK}$	SNI falling edge OUTCLK period	10BASE-T Mode		100		ns	
$T_{H\_FTX\_CLK}$	SNI falling edge OUTCLK high		35	50	65	ns	
$T_{L\_FTX\_CLK}$	SNI falling edge OUTCLK low		35	50	65	ns	
T_{CQ_MXFTX}	SNI falling edge OUTCLK to output valid				65	ns	
T_{CQ_MNFTX}	SNI falling edge OUTCLK to output invalid		35			ns	

Figure 36: SNI Falling Edge Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

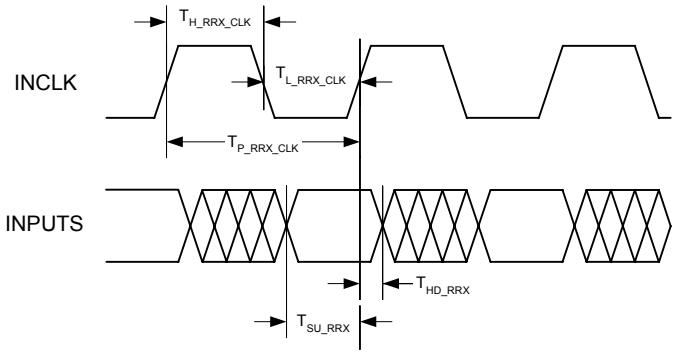
9.5.10 SNI Rising Edge Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 100: SNI Rising Edge Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RRX\_CLK}$	SNI rising edge INCLK period	10BASE-T Mode		100		ns	
$T_{H\_RRX\_CLK}$	SNI rising edge INCLK high		35	50	65	ns	
$T_{L\_RRX\_CLK}$	SNI rising edge INCLK low		35	50	65	ns	
T_{SU_RRX}	SNI receive data valid prior to INCLK going high		20			ns	
T_{HD_RRX}	SNI receive data valid after INCLK going high		10			ns	

Figure 37: SNI Rising Edge Receive Timing



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

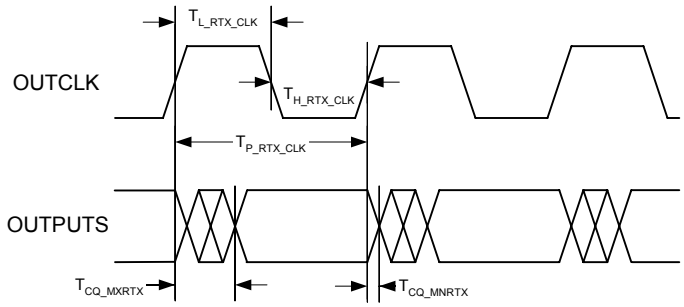
9.5.11 SNI Rising Edge Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 101: SNI Rising Edge Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RTX\_CLK}$	SNI rising edge OUTCLK period	10BASE-T Mode		100		ns	
$T_{H\_RTX\_CLK}$	SNI rising edge OUTCLK high		35	50	65	ns	
$T_{L\_RTX\_CLK}$	SNI rising edge OUTCLK low		35	50	65	ns	
T_{CQ_MXRTX}	OUTCLK to output valid				65	ns	
T_{CQ_MNRTX}	OUTCLK to output invalid		35			ns	

Figure 38: SNI Rising Edge Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

9.5.12 RMII Receive Timing using INCLK

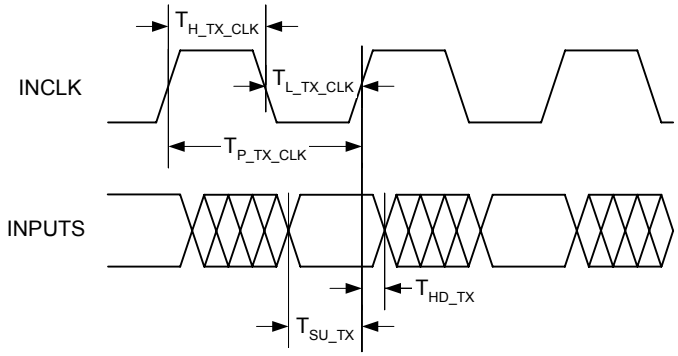
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 102: RMII Receive Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_TX\_CLK}$	P[x]_INCLK period	100BASE mode		20		ns	1
$T_{H\_TX\_CLK}$	P[x]_INCLK high	100BASE mode	8	10	12	ns	
$T_{L\_TX\_CLK}$	P[x]_INCLK low	100BASE mode	8	10	12	ns	
T_{SU_TX}	MII inputs (P[x]_IND[1:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		9.5			ns	
T_{HD_TX}	MII inputs (P[x]_IND[1:0], P[x]_INDV) valid after P[x]_INCLK going high.		0			ns	

1. 50 MHz for 100 Mbps.

Figure 39: PHY Mode RMII Receive Timing using INCLK



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

9.5.13 RMII Transmit Timing using INCLK

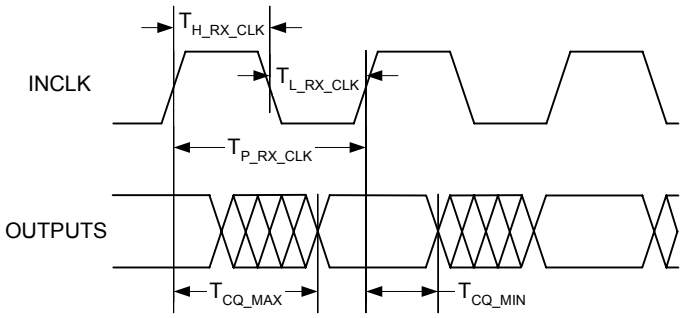
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 103: RMII Transmit Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
$T_{P\_RX\_CLK}$	P[x]_INCLK period	100BASE mode		20		ns	1
$T_{H\_RX\_CLK}$	P[x]_INCLK high	100BASE mode	8	10	12	ns	
$T_{L\_RX\_CLK}$	P[x]_INCLK low	100BASE mode	8	10	12	ns	
T_{CQ_MAX}	P[x]_INCLK to outputs (P[x]_OUTD[1:0], P[x]_OUTDV) valid				8.0	ns	
T_{CQ_MIN}	P[x]_INCLK to outputs P[x]_OUTD[1:0], P[x]_OUTDV) invalid		0			ns	

1. 50 MHz for 100 Mbps.

Figure 40: PHY Mode RMII Transmit Timing using INCLK



NOTE: INCLK is the clock used to clock the output data.
It is an output in this mode.

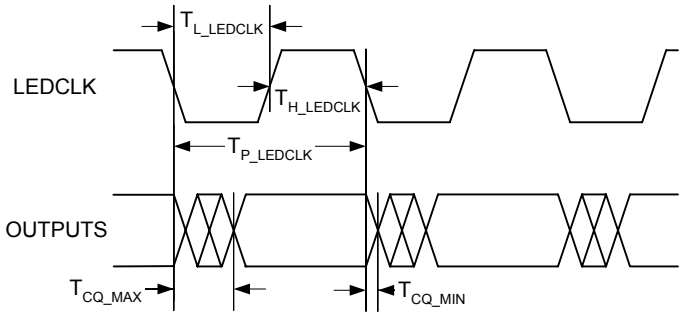
9.5.14 Serial LED Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 104: Serial LED Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{P_LEDCLK}	LEDCLK period			80		ns	
T_{H_LEDCLK}	LEDCLK high		32	40	48	ns	
T_{L_LEDCLK}	LEDCLK low		32	40	48	ns	
T_{CQ_MAX}	LEDCLK falling edge to link outputs (LEDSER, LEDENA) valid	With 10 pF load			20	ns	
T_{CQ_MIN}	LEDCLK falling edge to link outputs (LEDSER, LEDENA) invalid	With 10 pF load	0			ns	

Figure 41: Serial LED Timing



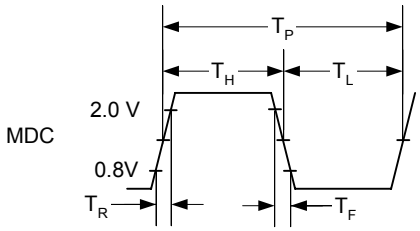
9.5.15 Serial Management Interface Clock Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 105: Serial Management Interface Clock Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDCCLK_IN period		120			ns	8.33 MHz
T_H	MDCCLK_IN high time		48			ns	
T_L	MDCCLK_IN low time		48			ns	
T_R	MDCCLK_IN rise				6	ns	
T_F	MDCCLK_IN fall				6	ns	

Figure 42: Serial Management Interface Clock Timing



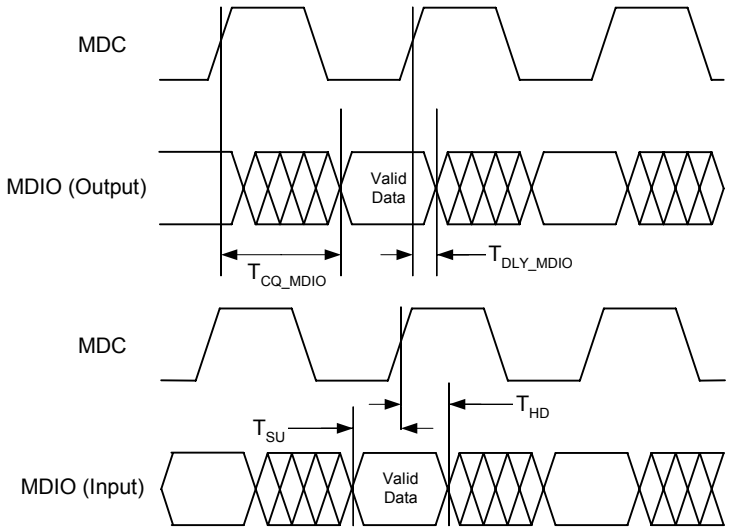
9.5.16 Serial Management Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 106: Serial Management Interface Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{CQ_MDIO}	MDC to MDIO (Output) data valid time				20	ns	
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0			ns	
T_{SU}	MDIO (Input) to MDC setup time		10			ns	
T_{HD}	MDIO (Input) to MDC hold time		10			ns	

Figure 43: Serial Management Interface Timing



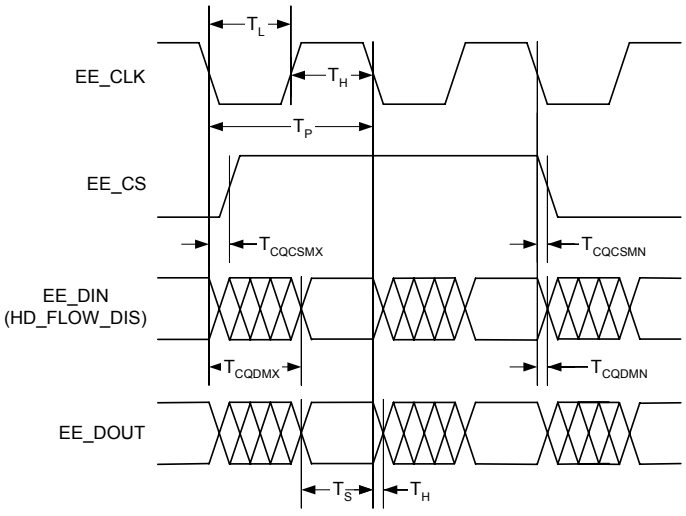
9.5.17 EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 107: EEPROM Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	EE_CLK period			5120		ns	
T_H	EE_CLK high time			2560		ns	
T_L	EE_CLK low time			2560		ns	
T_{CQCSMX}	Serial EEPROM chip select valid	Referenced to EE_CLK			5	ns	
T_{CQCSMN}	Serial EEPROM chip select invalid				5	ns	
T_{CQDMX}	Serial EEPROM data transmitted to EEPROM valid				10	ns	
T_{CQDMN}	Serial EEPROM data transmitted to EEPROM invalid		3			ns	
T_S	Setup time for data received from EEPROM		10			ns	
T_H	Hold time for data received from EEPROM		10			ns	

Figure 44: EEPROM Timing



9.5.18 IEEE AC Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:

- 10BASE-T IEEE 802.3 Clause 14-2000
- 100BASE-TX ANSI X3.263-1995
- 1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

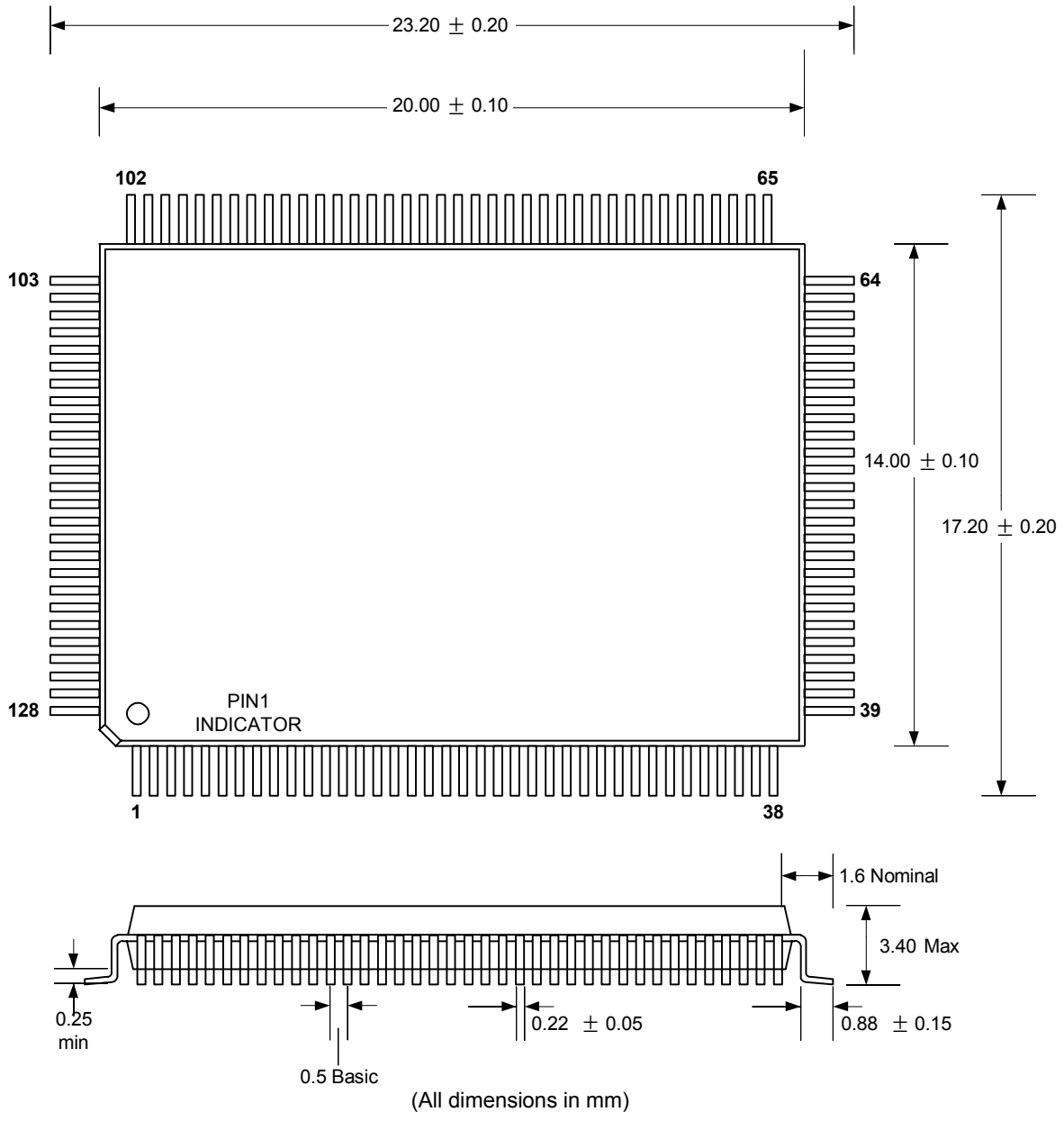
Table 108: IEEE AC Parameters

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	TXP/N[4:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall time	TXP/N[4:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/ T_{FALL} Symmetry		TXP/N[4:0]	100BASE-TX	0		0.5	ns
DCD	Duty cycle distortion	TXP/N[4:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		TXP/N[4:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3.

Section 10. Mechanical Drawings

10.1 128-Pin PQFP Package



(All dimensions in mm)

Section 11. Ordering Information

11.1 Ordering Part Numbers

Figure 45 shows the ordering part numbering scheme for the devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 45: Sample Part Number

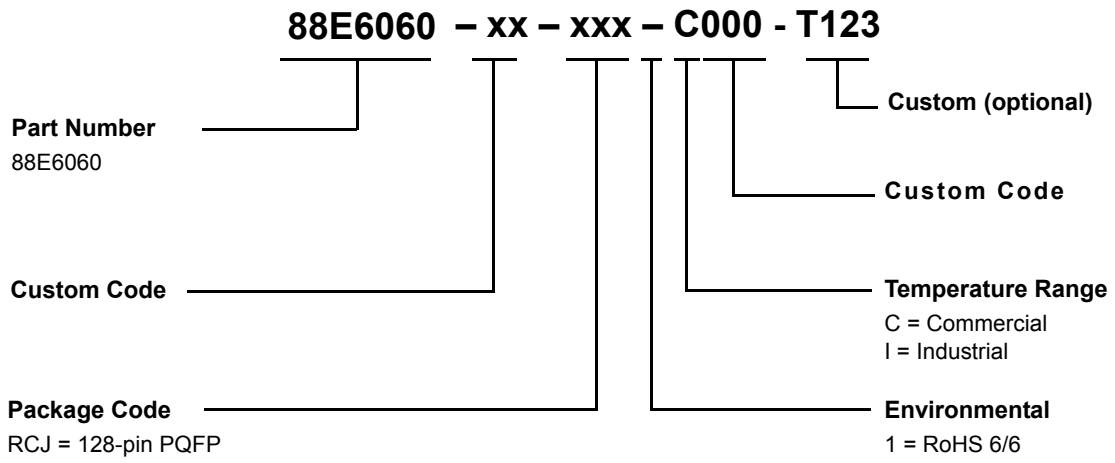


Table 109: Part Order Option - Commercial

Package Type	Part Order Number
88E6060 128-pin PQFP - Commercial - RoHS 6/6	88E6060-xx-RCJ1C000

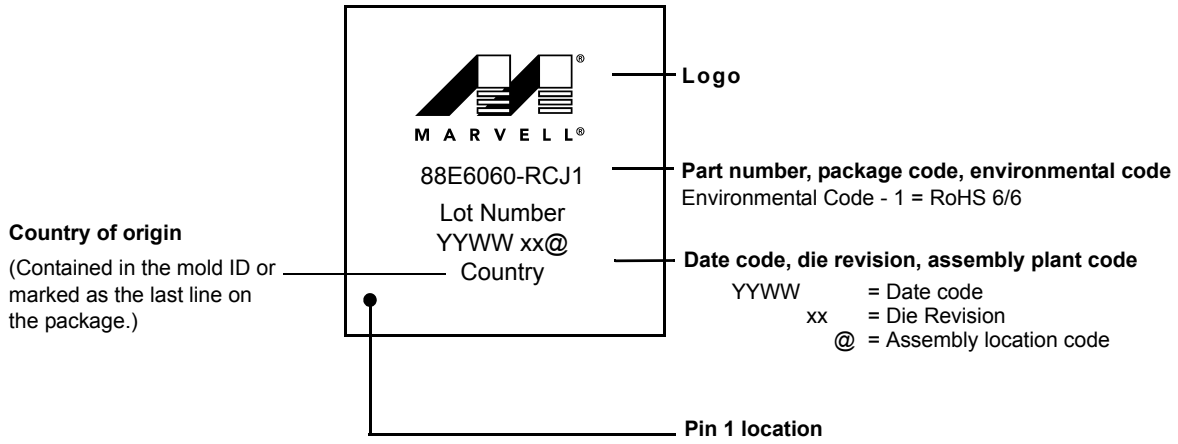
Table 110: Part Order Option - Industrial

Package Type	Part Order Number
88E6060 128-pin PQFP - Industrial - RoHS 6/6	88E6060-xx-RCJ1I000

11.2 Package Markings

Figure 46 is an example of the package marking and pin 1 location for the 88E6060 Device 128-pin PQFP Commercial RoHS 6/6 package.

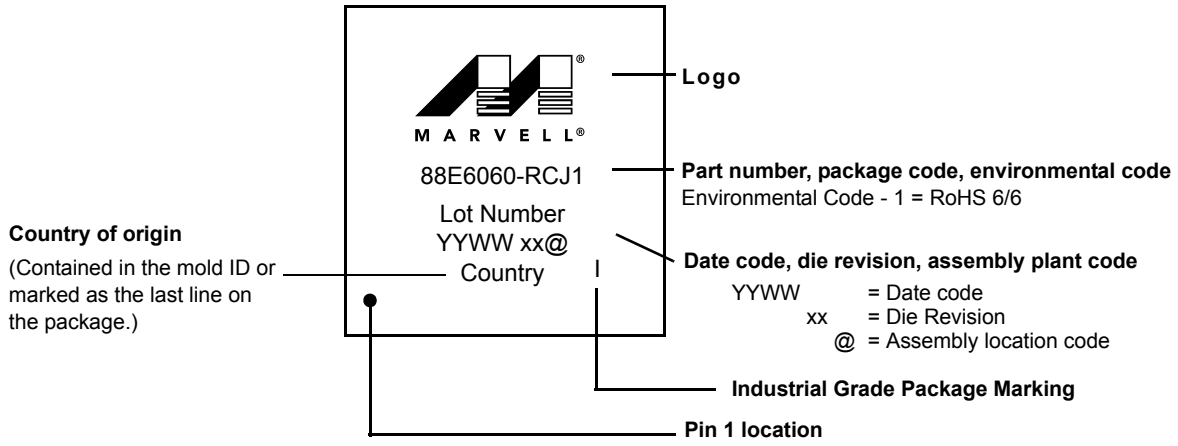
Figure 46: 88E6060 128-pin PQFP Commercial RoHS 6/6 Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 47 is an example of the package marking and pin 1 location for the 88E6060 Device 128-pin PQFP Industrial RoHS 6/6 package.

Figure 47: 88E6060 128-pin PQFP Industrial RoHS 6/6 Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

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