Application
Brief #3

Introduction

In 1990 IEEE adopted a method of testing deeply integrated circuits and complete boards. This resolution, IEEE 1149.1-1990 was brought about by industry looking for a method of testing and debugging that improved on old techniques, such as bed-of-nails, logic probes, and test modules stuck in between devices and their sockets.

With JTAG debugging techniques, a device designer, from microprocessors to ASICs will add to the device itself debugging units that are able to gather information on the operations of the device and route it to a test port on the boundary of the circuit board. This Test Access Port, or TAP, is connected to external JTAG hardware to show what is taking place. But, the test port works both ways. Designers/testers can send information to the chip to configure its initial power-on settings prior to leaving the assembly line and arriving at the customer. JTAG capable FLASH ROMs are programmable once on the board in this manner. This two-way debugging/programming is done with a software language called BSDL or Boundary-Scan Definition Language used to describe how the individual JTAG-capable devices on the board work.

Scan path verification is the first test that is ever executed at the system level. This test verifies that the devices on a scan path are communicating correctly and that there are no “stuck bits.” Scan path verification can be accomplished by flushing data through the path using data or instruction scans. Proper communication with every scannable device is mandatory in order to prevent signal clashes and damaged devices.

Component testing is performed to verify the internal operation of any JTAG device. This is one of the key reasons that boundary scan is incorporated into complex ASICs and CPUs. Test files are used to stimulate internal operations and investigate the results. This eliminates mounting bad parts on a board as well as verifies that the parts were not damaged during the assembly process.

Interconnection testing will verify that signal nets are connected properly. Every signal net running between two JTAG devices can be tested. Signal nets can be checked for both opens and shorts by driving data patterns out of one device using EXTEST and reading the patterns from a destination device using SAMPLE. Interconnection testing inherently checks for cold solder joints and blown output drivers that arise during board assembly.

Finally, system application testing can utilize boundary scan as an elaborate diagnostic tool. Boundary scan can initialize breakpoints and proceed to check preliminary results throughout the circuit (similar to having emulator capability). The power of this feature is priceless for those software designers that have programmed around complicated processors and system architectures. JTAG capability will reduce system debug time with the ability to access data anywhere in a circuit. The end result is a decrease in program cost.

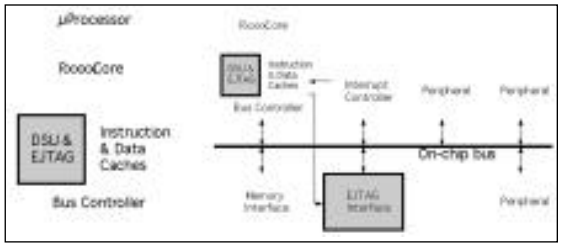
Design Challenges

The Enhanced JTAG (EJTAG) initiative came about when boards and devices were getting more dense and internally complicated requiring additional debugging capabilities. Designers also saw other debugging techniques that could add to JTAG's usefulness. All of the competing EJTAG standards build on traditional JTAG by overlaying the debugging capabilities on top of JTAG pins and adding more pins for runtime trace and control.

There are a couple of competing enhanced JTAG standards. The first is the MIPS consortium-based standard called EJTAG. This standard is rooted in the original IEEE work. Another standard is N-Wire, which is used in the newer processors by NEC. Finally, there is movement in the IBM PowerPC arena with RISCWatch and Motorola PowerPC with Common On-Chip Processor (COP).

Since EJTAG has remained in the public domain and not been adopted by IEEE, it has been easier for the MIPS licensees to modify the proposal, and thus, has gone through many revisions since its introduction in 1997. EJTAG allows greater simulation because there are more 'probes' inside the components to record each pin and the other operations taking place within the component. EJTAG requires significantly more forward-thinking chip designs than JTAG due to complexity, speed, and intended function. *Unlike JTAG, EJTAG is not an easy retrofit into older designs.*

EJTAG provides the designer/programmer the ability to set software and hardware breakpoints. This sets points where the system will stop and debugging information can be read to determine the internal operation. More thorough evaluation and improved error conditions help speed debugging of increasingly advanced systems.



JTAG is the basic functionality of boundary scan. Only when all devices on the board support JTAG can its benefits be truly seen. EJTAG gives the added benefit of more thorough In-Circuit Emulation (ICE) capabilities. When EJTAG is designed-in, a Decoding Support Unit (DSU) is required to do all the communications for the external debugging module. This way, the on-chip logic is sending signals to all supported pins to test their operability and conversely gathering the values of all pins to return real-time status back to the on-board logic and eventually routed to EJTAG test equipment for the designer to evaluate.

In the past, all processors were designed with the ability to interface with external hardware to make up In-Circuit Emulation (ICE) for the designers. As the processors got more complicated, ICE became less cost-effective. EJTAG was then implemented as a new standard for IDT processors for additional debugging and testability. With the latest IDT offering, the RC64600, enhanced JTAG capabilities were needed to further help the customers quickly test and debug the processors and overall systems. IDT chose to use the N-Wire version of EJTAG to make that possible.

Additionally, more IDT products are implementing JTAG, to include System Controllers such as RC32134 and RC64145, FIFOs, and SARs.

The vast majority of the competition's offerings have included a JTAG Test Access Port (TAP). Recently, products have be arriving with more enhanced capabilities, such as N-Wire/N-Trace from NEC, RISCWatch from IBM, and COP from Motorola. These versions of Enhanced JTAG perform relatively the same functions and use the traditional JTAG TAP with a couple additional pins for greater control.

Device Summary, Features and Benefits

Using traditional test and debug methods, it took system designers much time and money to ensure their products were working. JTAG came along to help speed this process up. As processors increased in complexity, Enhanced JTAG versions popped up to help designers even further. IDT has been including JTAG in processors for awhile now, and other product lines are beginning to incorporate the functionality. Competitor products are also using JTAG and Enhanced JTAG to help speed your products to market.

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