Standard Features

- Low-voltage and standard-voltage operation
  - V_{CC} = 1.7V to 5.5V
- Internally organized as 512 x 8 (4K), or 1024 x 8 (8K)
- I^2C-compatible (two-wire) serial interface
- Schmitt Trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 1MHz (5V), 400kHz (1.7V, 2.5V, 2.7V) compatibility
- Write protect pin for hardware data protection
- 16-byte page write mode
  - Partial page writes allowed
- Self-timed write cycle (5ms max)
- High-reliability
  - Endurance: 1 million write cycles
  - Data retention: 100 years
- Green package options (Pb/Halide-free/RoHS compliant)
  - 8-lead SOIC, TSSOP, UDFN, 8-ball VFBGA, 5-lead SOT23
- Die options: wafer form and tape and reel

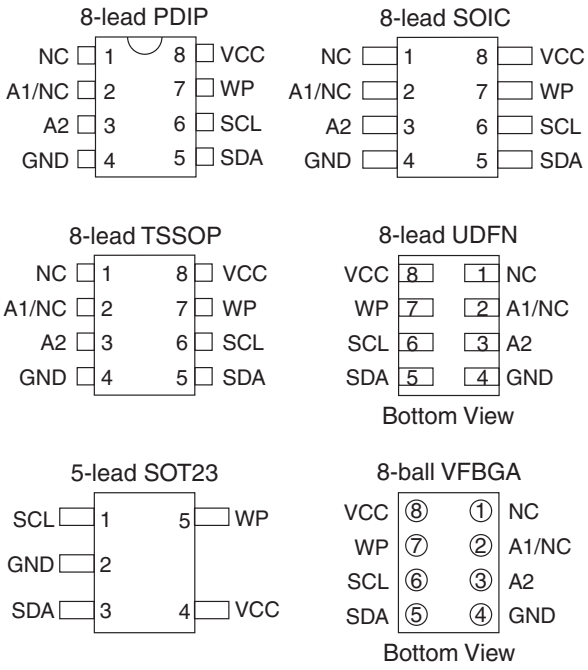
Description

The Atmel® AT24C04C and AT24C08C provides 4096/8192-bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 512/1024-words of 8-bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C04C/C08C is available in space-saving 8-lead PDIP, 8-lead TSSOP, 8-lead JEDEC SOIC, 8-lead UDFN, 5-lead SOT23 and 8-ball VFBGA packages and is accessed via a two-wire serial interface.

Figure 0-1. Pin Configuration

Pin Name	Function
NC	No Connect
A1	Address input (4K only)
A2	Address input
SDA	Serial data
SCL	Serial clock input
WP	Write protect
GND	Ground
VCC	Power supply

Note: For use of 5-lead SOT23, the software A2 and A1 bits in the device address word must be set to zero to properly communicate



I^2C-Compatible (2-wire) Serial EEPROM

4Kbit (512 x 8)

8Kbit (1024 x 8)

Atmel AT24C04C
Atmel AT24C08C

Preliminary

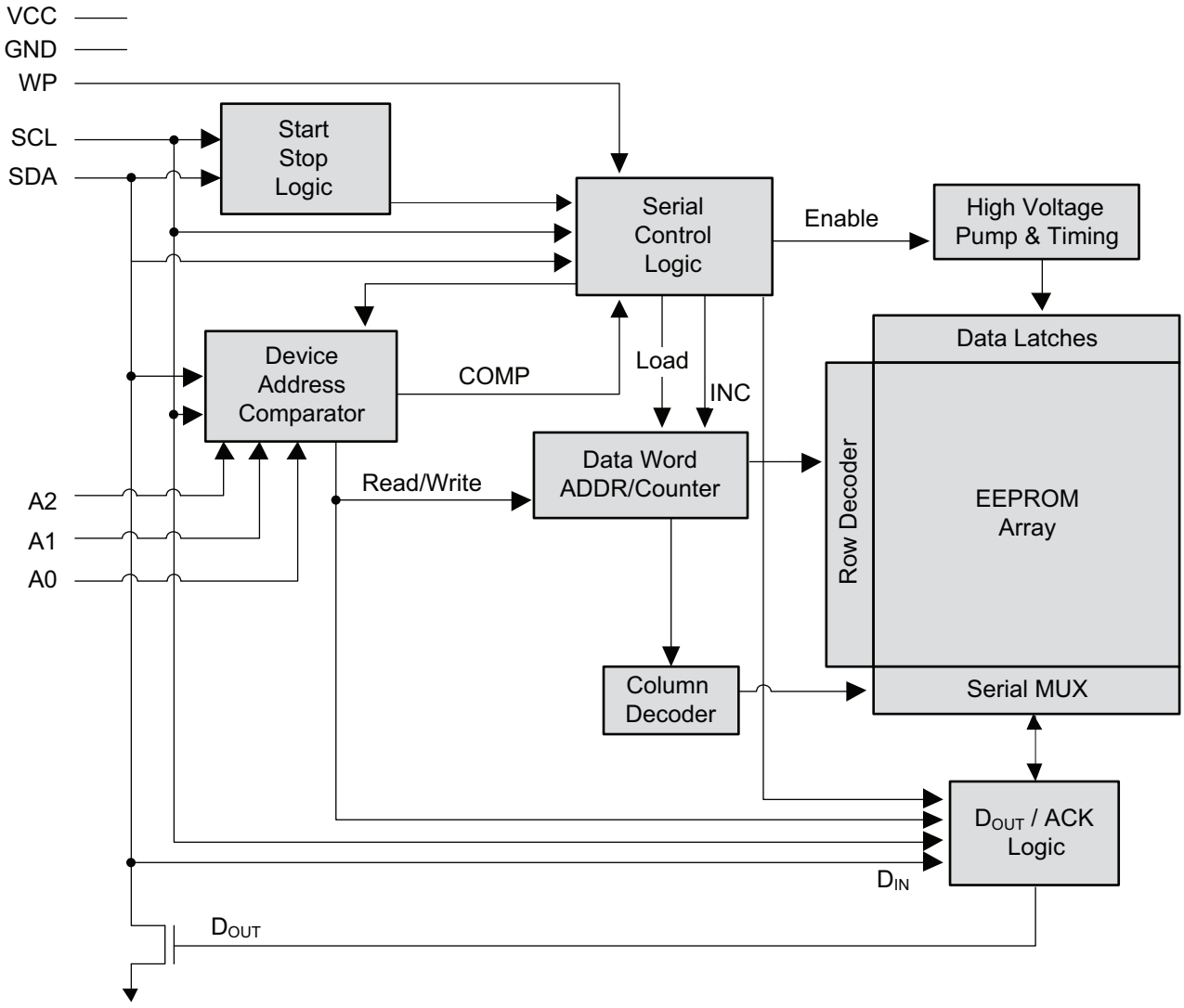
8787A–SEEPR–10/11

Absolute Maximum Ratings

Operating temperature	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on any pin with respect to ground	–1.0V to +7.0V
Maximum operating voltage	6.25V
DC output current	5.0mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram



1. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2 and A1): The AT24C04C uses the A2 and A1 inputs for hard wire addressing allowing a total of four 4K devices to be addressed on a single bus system. The A0 pin is a no connect and can be connected to ground (see Section 6. “Device Addressing” on page 9). The AT24C08C only uses the A2 input for hardware addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects and can be connected to ground (see Section 6. “Device Addressing” on page 9).

WRITE PROTECT (WP): AT24C04C/08C has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when connected to ground (GND). When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in Table 1-1.

Table 1-1. Write Protect

WP Pin Status	Part of the Array Protected
	Atmel AT24C04C/08C
At V_{CC}	Full array
At GND	Normal read/write operations

2. Memory Organization

Atmel AT24C04C, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing

Atmel AT24C08C, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

Table 2-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +1.7V to +5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested

Table 2-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.7		5.5	V
V_{CC2}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	Read at 100kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	Write at 100kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested

Table 2-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.7V to +5.5V, CL = 1TTL Gate and 100pF (unless otherwise noted)

Symbol	Parameter	1.7V, 2.5V, 2.7V		5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time		50		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Setup Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Setup Time	0.6		.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	5.0V, +25°C, Byte Mode	1 Million				Write Cycles

Note: 1. This parameter is ensured by characterization only

3. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 5-2 on page 8). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 5-3 on page 8).

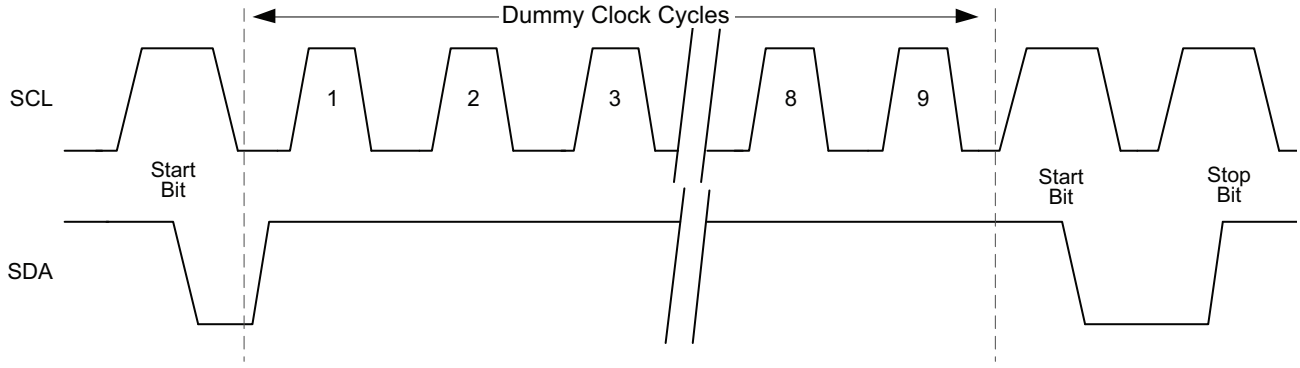
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5-3 on page 8).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The Atmel AT24C04/08C features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

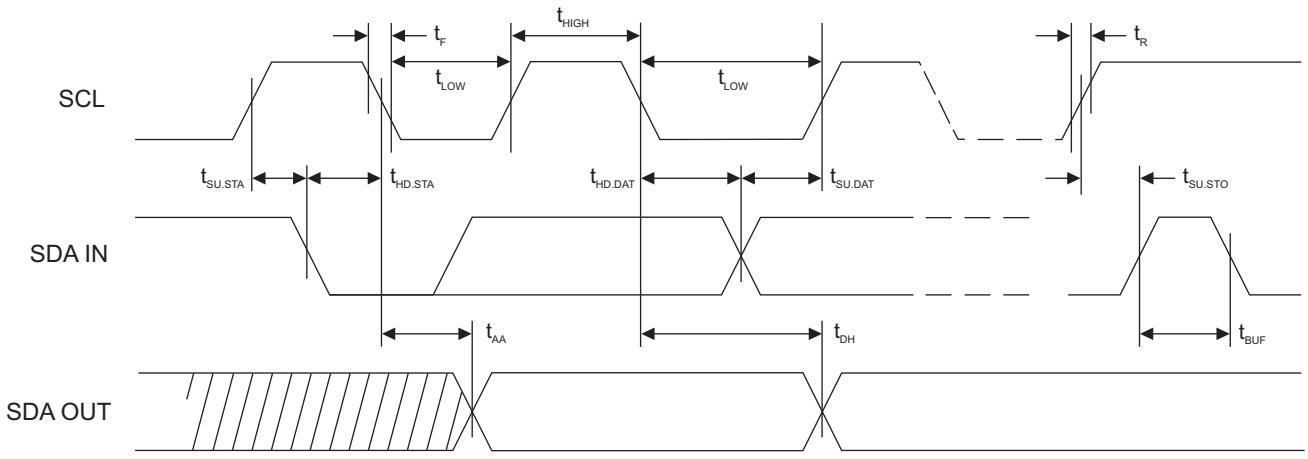
2-WIRE SOFTWARE RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps: (a) Create a start bit condition, (b) clock nine cycles, (c) create another start bit followed by stop bit condition as shown below. The device is ready for next communication after above steps have been completed.

Figure 3-1. Software reset



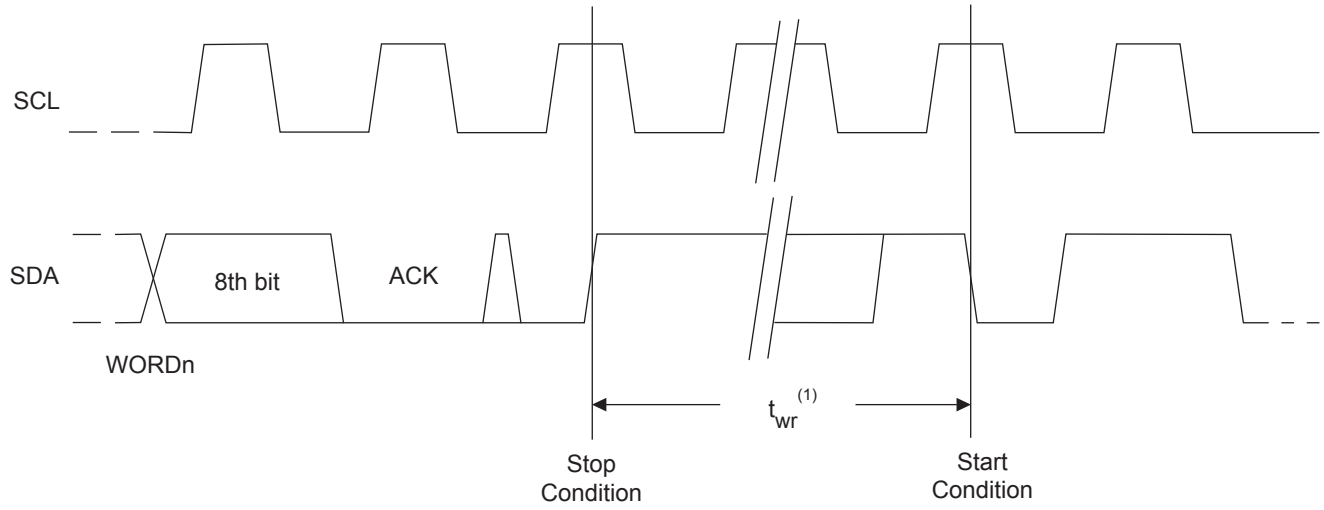
4. Bus Timing

Figure 4-1. SCL: Serial Clock, SDA: Serial Data I/O



5. Write Cycle Timing

Figure 5-1. SCL: Serial Clock, SDA: Serial Data I/O



Notes: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle

Figure 5-2. Data Validity

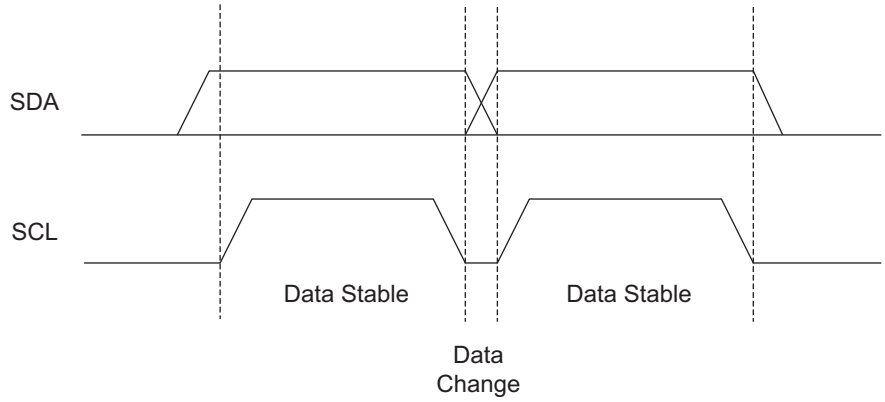


Figure 5-3. Start and Stop Definition

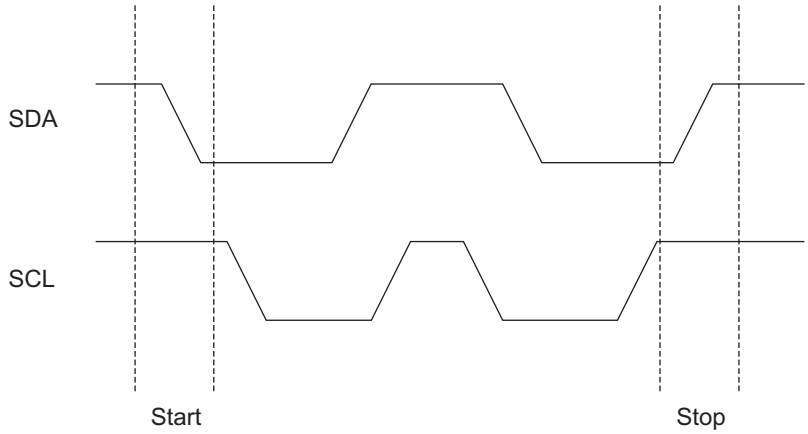
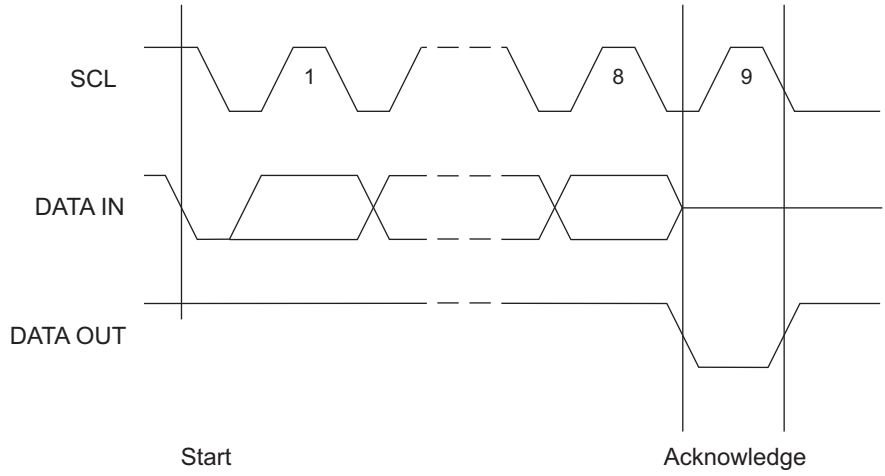


Figure 5-4. Output Acknowledge



6. Device Addressing

STANDARD EEPROM ACCESS: The 4K and 8K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consists of a mandatory '1010' (0xA) sequence for the first four most significant bits as shownin Figure 8-1 on page 10. This is common to all the EEPROM devices.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next two bits being for memory page addressing. The A2 must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

For the SOT23 package offering, the 4K EEPROM software A2 and A1 bits in the device address word must be set to zero to properly communicate. The 8K EEPROM software A2 bit in the device address word must be set to zero to properly communicate.

7. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8-2 on page 10).

PAGE WRITE: The 4K and 8K EEPROM is capable of a 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 8-3 on page 11).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

8. Read Operations

Read operations are initiated in the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are four read operations: current address read, random address read, sequential read, and serial number read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 8-4 on page 11).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8-5 on page 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8-6 on page 11).

Figure 8-1. Device Address

Density	Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4K	EEPROM	1	0	1	0	A_2	A_1	P_0	R/$\overline{W}$
8K	EEPROM	1	0	1	0	A_2	P_1	P_0	R/$\overline{W}$
		MSB							LSB

Figure 8-2. Byte Write

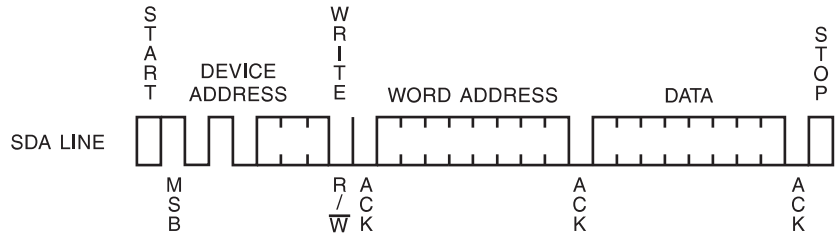


Figure 8-3. Page Write

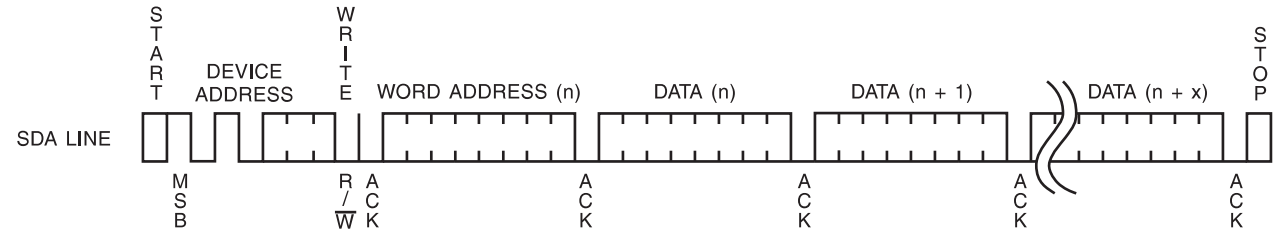


Figure 8-4. Current Address Read

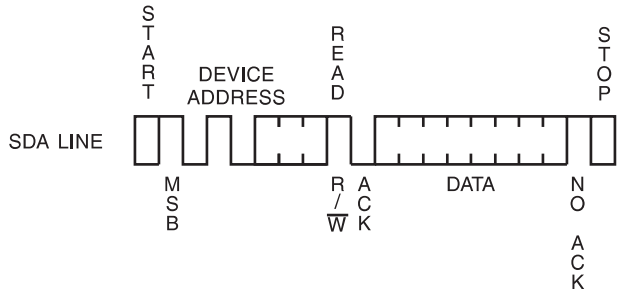


Figure 8-5. Random Read

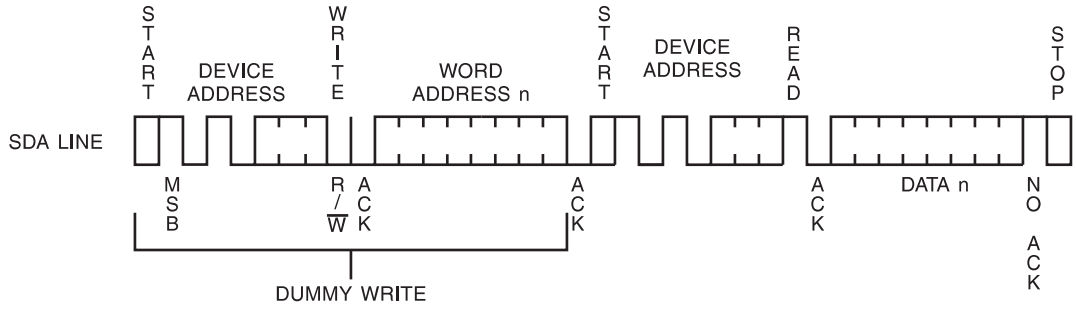
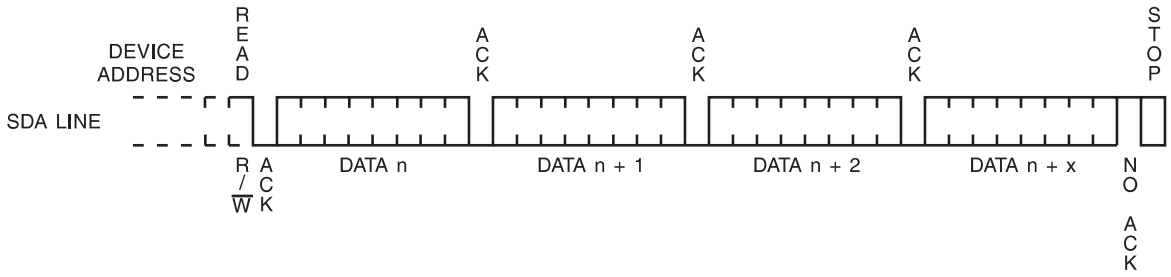
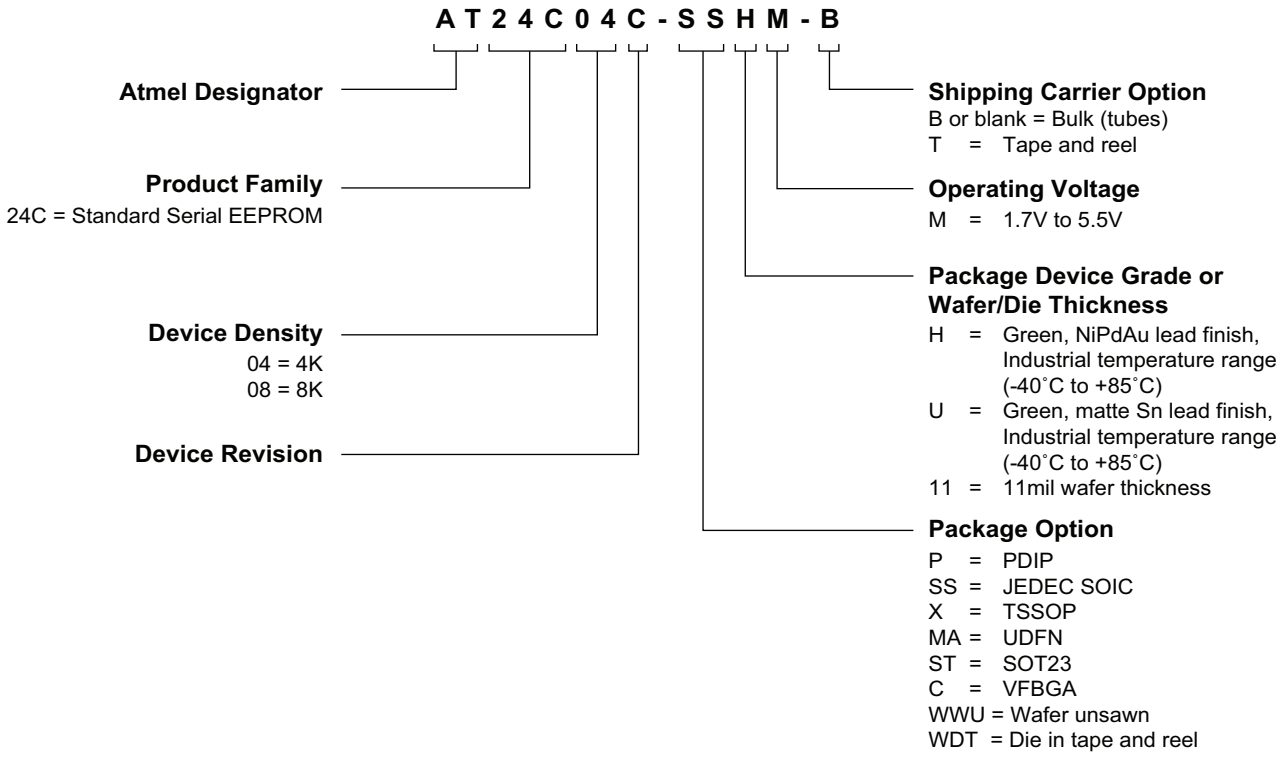


Figure 8-6. Sequential Read

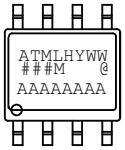


9. Ordering Code Detail



10. Part Markings

8 lead SOIC
3 Rows of 8 Characters



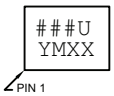
8 lead TSSOP
3 Rows
2 of 6 and 1 of 7 Characters

5 lead SOT-23
2 Rows
1 of 5 and 1 of 4 Characters

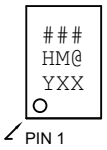
Top Mark

Bottom Mark

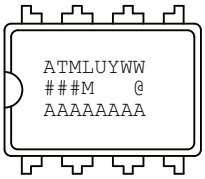
8-ball VFBGA - 1.5x2.0mm
2 Rows of 4 Characters



8 lead UDFN - 2.0x3.0mm
3 Rows of 3 Characters



8 lead PDIP
3 Rows of 8 Characters



Catalog Number: AT24C04C
Catalog Number: AT24C08C

Catalog Truncation: ### = 04C
Catalog Truncation: ### = 08C

Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	M: 1.7V min
0: 2010 4: 2014 1: 2011 5: 2015 2: 2012 6: 2016 3: 2013 7: 2017	A: January B: February “ ” “ L: December	02: Week 2 04: Week 4 ” “ ” 52: Week 52	
Trace Code			**Grade/Lead Finish Material**
XX = Trace Code (ATMEL Lot Numbers to Correspond to Code) (e.g. XX: AA, AB...YZ, ZZ)			U: Industrial/Matt Tin H: Industrial/NiPdAu
Lot Number			
AAAAAAA = ATMEL Wafer Lot Number			
Location of Assembly			**ATMEL Truncation**
@ = Location of Assembly			AT: ATMEL ATM: ATMEL ATML: ATMEL

10/10/11

	TITLE	DRAWING NO.	REV.
Package Mark Contact: DL-CSO-Assy_eng@atmel.com	24C-C-04-08CSM, Standard Marking Information for Package Offering	24C-C-04-08CSM	A

11. Ordering Codes

Atmel AT24C04C Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24C04C-PUM (Bulk form only)	1.7V to 5.5V	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT24C04C-SSHM-B[1] (NiPdAu lead finish)	1.7V to 5.5V	8S1	
AT24C04C-SSHM-T[2] (NiPdAu lead finish)	1.7V to 5.5V	8S1	
AT24C04C-XHM-B[1] (NiPdAu lead finish)	1.7V to 5.5V	8X	
AT24C04C-XHM-T[2] (NiPdAu lead finish)	1.7V to 5.5V	8X	
AT24C04C-MAHM-T[2] (NiPdAu lead finish)	1.7V to 5.5V	8MA2	
AT24C04C-STUM-T[2]	1.7V to 5.5V	5TS1	
AT24C04C-CUM-T[2]	1.7V to 5.5V	8U3-1	
AT24C04C-WWU11[3]	1.7V to 5.5V	Die Sale	Industrial Temperature (–40°C to 85°C)

Notes: 1. “-B” denotes bulk
2. “-T” denotes tape and reel
SOIC = 4K per reel
TSSOP, UDFN, SOT23, and VFBGA = 5K per reel
3. For Wafer sales, please contact Atmel Sales

Package Type	
8P3	8-lead, 0.300" wide, Plastic Dual Inline (PDIP)
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)
8MA2	8-lead, 2.00mm x 3.00mm body, 0.50mm pitch, Dual No Lead (UDFN)
5TS1	5-lead, 2.90mm x 1.60mm body, Plastic Thin Shrink Small Outline (SOT23)
8U3-1	8-ball, die Ball Grid Array (VFBGA)

Atmel AT24C08C Ordering Information

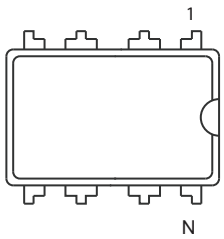
Ordering Code	Voltage	Package	Operation Range
AT24C08C-PUM (Bulk form only)	1.7V to 5.5V	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT24C08C-SSHM-B[1] (NiPdAu Lead Finish)	1.7V to 5.5V	8S1	
AT24C08C-SSHM-T[2] (NiPdAu Lead Finish)	1.7V to 5.5V	8S1	
AT24C08C-XHM-B[1] (NiPdAu Lead Finish)	1.7V to 5.5V	8X	
AT24C08C-XHM-T[2] (NiPdAu Lead Finish)	1.7V to 5.5V	8X	
AT24C08C-MAHM-T[2] (NiPdAu Lead Finish)	1.7V to 5.5V	8MA2	
AT24C08C-STUM-T[2]	1.7V to 5.5V	5TS1	
AT24C08C-CUM-T[2]	1.7V to 5.5V	8U3-1	
AT24C08C-WWU11[3]	1.7V to 5.5V	Die Sale	Industrial Temperature (–40°C to 85°C)

Notes: 1. “-B” denotes bulk
2. “-T” denotes tape and reel
SOIC = 4K per reel
TSSOP, UDFN, SOT23, and VFBGA = 5K per reel
3. For Wafer sales, please contact Atmel Sales

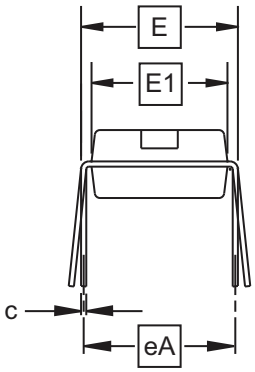
Package Type	
8P3	8-lead, 0.300" wide, Plastic Dual Inline (PDIP)
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)
8MA2	8-lead, 2.00mm x 3.00mm body, 0.50mm pitch, Dual No Lead (UDFN)
5TS1	5-lead, 2.90mm x 1.60mm body, Plastic Thin Shrink Small Outline (SOT23)
8U3-1	8-ball, die Ball Grid Array (VFBGA)

12. Packaging Information

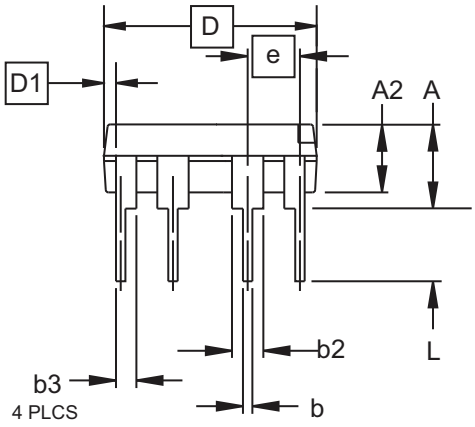
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

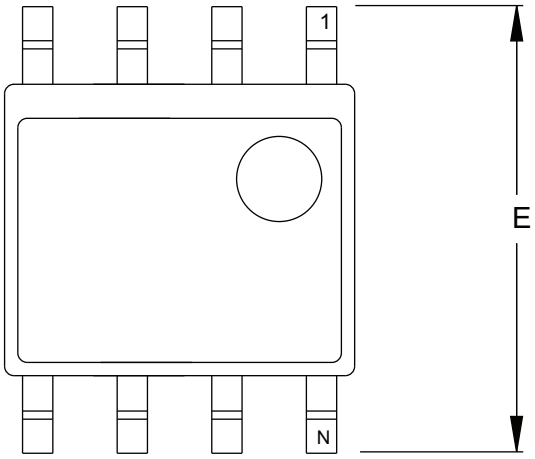
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

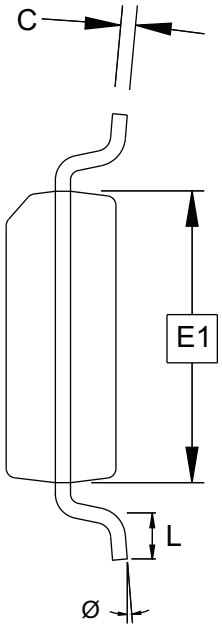
06/21/11

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8P3, 8-lead, 0.300” Wide Body, Plastic Dual In-line Package (PDIP)	PTC	8P3	D

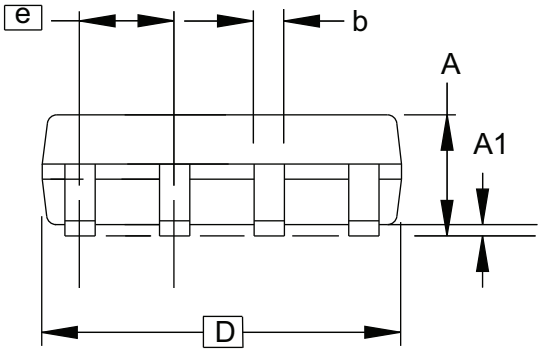
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

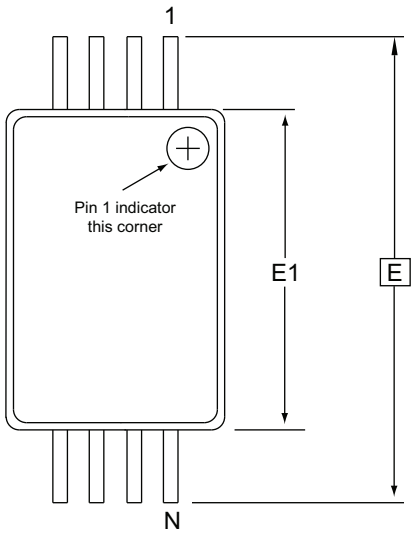
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

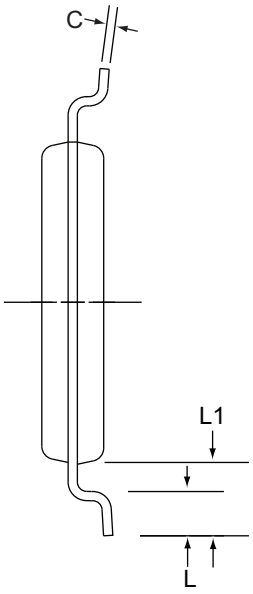
6/22/11

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	SWB	8S1	G

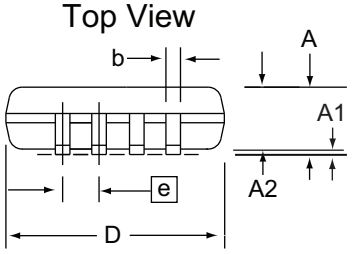
8X – TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

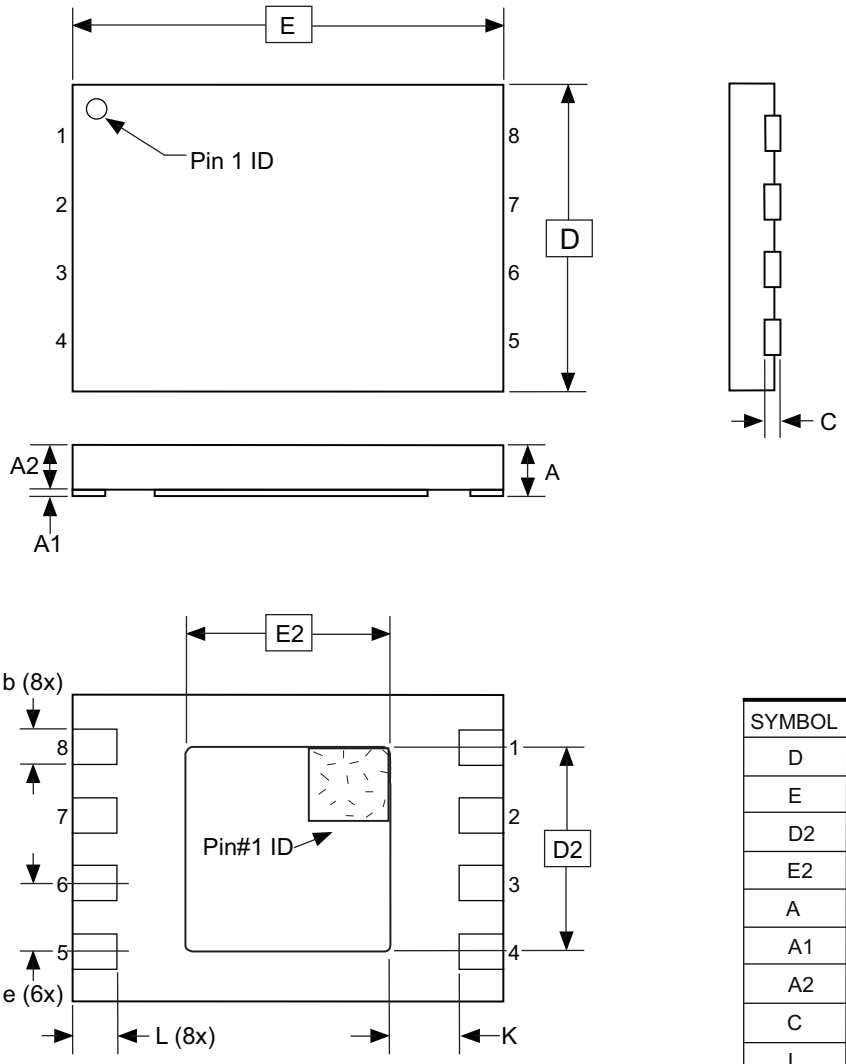
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C		0.09	-	0.20

6/22/11

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	TNR	8X	D

8MA2 - UDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

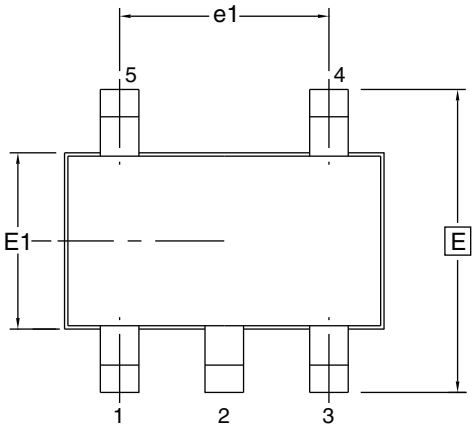
SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	1.20	1.30	1.40	
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	–	–	0.55	
C		0.152 REF		
L	0.30	0.35	0.40	
e		0.50 BSC		
b	0.18	0.25	0.30	3
K	0.20	–	–	

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The terminal #1 ID is a laser-marked feature.
3. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

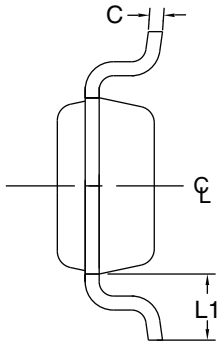
7/15/11

Package Drawing Contact: packagedrawings@atmel.com	TITLE 8MA2, 8-pad, 2 x 3 x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	GPC YNZ	DRAWING NO. 8MA2	REV. B

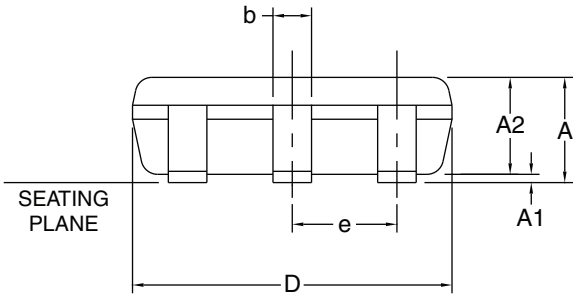
5TS1 – SOT23



Top View



End View



Side View

Notes:
1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.15mm per end. Dimensions E1 does not include interlead flash or protrusion. Interlead flasg or protrusion shall not exceed 0.15mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are deteremined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.80mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07mm.
5. This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

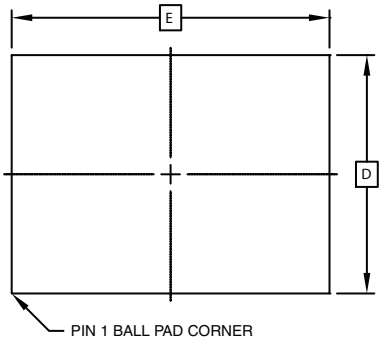
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.10	
A1	0.00	–	0.10	
A2	0.70	0.90	1.00	
c	0.08	–	0.20	3
D	2.90 BSC			1, 2
E	2.80 BSC			1, 2
E1	1.60 BSC			1, 2
L1	0.60 REF			
e	0.95 BSC			
e1	1.90 BSC			
b	0.30	–	0.50	3, 4

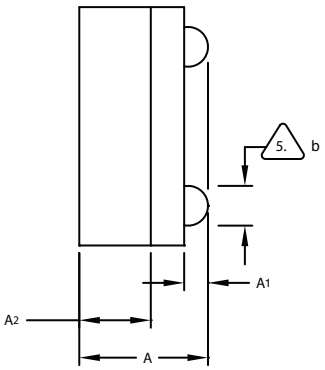
11/05/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	5TS1, 5-lead, 1.60mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	TSZ	5TS1	B

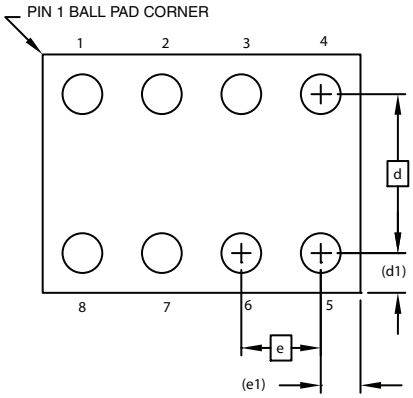
8U3-1 – VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW

8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D		1.50 BSC		
E		2.0 BSC		
e		0.50 BSC		
e1		0.25 REF		
d		1.00 BSC		
d1		0.25 REF		

07/14/10

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**8U3-1, 8-ball, 1.50 x 2.00 mm Body,** 0.50 pitch, VFBGA Package (dBGA2)	GXU	8U3-1	D

13. Revision History

Doc. Rev.	Date	Comments
8787A	10/2011	Initial document release

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