Intel® 440BX AGPset
82443BX Host Bridge/Controller
Specification Update

July 1998

Order Number: 290639-002

The Intel® 82443BX AGPset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

INTEL 82443BX AGPSET

Date of Revision	Version	Description
May 1998	-001	Initial Release
July 1998	-002	Added Specification Changes #2 and #3.

PREFACE

This document is an update to the specifications contained in the Intel® 440BX AGPset Datasheet, Revision 1.0, Order number 290633, and contains issues affecting all designs using the Intel 82443BX Host Bridge/Controller.

This document is intended for hardware system manufactures and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel 82443BX AGPset's, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 82443BX AGPset stepping can be identified by the following register contents:

82443BX Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B-1	8086h	7190h/7192h	02h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space. The default value is 7190h. When AGP is disabled, the value is 7192h.
3. The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Specification Update for
Intel 82443BX Host Bridge/Controller

GENERAL INFORMATION

This section covers the Intel 82443BX AGPset.

INTEL 82443BX COMPONENT MARKING INFORMATION

Stepping	S-Spec	Top Marking	Notes
B-1		FW82443BX Q628ES	Engineering Sample, FM Test
B-1		FW82443BX Q629ES	Engineering Sample, FM Test
B-1		FW82443BX Q630ES	Engineering Sample, T03 Test with Burn-In Full Production Flow
B-1	SL2T5	FW82443BX SL2T5	440BX B-1 Production ASSY

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel 82443BX Stepping. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	B1	Plans	SPECIFICATION CHANGES
1	X	Doc	Abort Disable Test Mode Configuration Bits
2	X	Doc	Selective Auto Precharge
3	X	Doc	Memory Data Buffer Strength Programming
NO.	**B1**	**Plans**	**ERRATA**
1	X	Doc	Hard Reset Collision with Refresh
2	X	Doc	IPDLT Bit Setting
3	X	Fix	SDRAM Suspend Refresh
4	X	Fix	Refresh Collision with SUS_STAT# assertion (EDO Memory)
NO.	**B1**	**Plans**	**SPECIFICATION CLARIFICATIONS**
			There are currently no known 82443BX Specification Clarifications.
NO.	**B1**	**Plans**	**DOCUMENTATION CHANGES**
			There are currently no known 82443BX Documentation Changes.

INTEL 82443BX SPECIFICATION CHANGES

1. Abort Disable Test Mode Configuration Bits

Intel Reserved Register bits at offset F4h, bits 29 and 30 should be set to 1 for normal operation.

2. Selective Auto Precharge

Due to inconsistent behavior of the selective auto precharge feature with different SDRAM components, this feature will be removed from further revisions of the 82443BX External Design Specification. Bit 4 of the Paging Policy register, Offset 78-79h should be set to 0 (default). Bit 4 at Offset 78h will become an Intel Reserved bit location.

3. Memory Data Buffer Strength Programming

Characterization of the MD buffers has shown that the actual buffers are stronger than the simulated buffer strengths. As a result, new buffer strength settings are recommended in order to improve system noise margin. The new settings are described in the BIOS Specification Update, Rev 2.1 or later.

INTEL 82443BX ERRATA

1. Hard Reset Collision with Refresh

PROBLEM: During a software generated hard reset, if a DRAM refresh cycle coincides with the activation of PCIRST#, the system will hang.

IMPLICATION: The system will hang.

WORKAROUND: The system BIOS must disable refresh before generating the reset sequence. Refer to the 82443BX BIOS Specification Update for more details.

RESOLUTION: This erratum will **not** be fixed in the B-1 stepping of the 82443BX.

2. IPDLT Bit Setting

PROBLEM: System validation has uncovered a marginal internal timing path.

IMPLICATION: An incorrect address may be driven on the DRAM bus, resulting in memory data being fetched from the wrong location.

WORKAROUND: The IPDLT bits (register offset 76h, bits 8 and 9) should be set to 01 (i.e. set bit 8 to 1).

RESOLUTION: BIOS workaround (configuration register change).

3. SDRAM Suspend Refresh

PROBLEM: This erratum may occur in Intel 440BX chipset platforms that implement suspend or Stop Clock (C3) states. Platforms that are affected include mobile SDRAM platforms using module MM-config mode (single CKE) and 4 DIMM desktop platforms using GCKE.

These platforms require the 440BX memory controller to stop the normal refresh and place the SDRAM in a self-refresh mode before the system transitions to one of these states. If the self-refresh trigger (SUSTAT1# signal asserted) occurs at the same time as an internally generated normal refresh request, the 440BX generates an incorrect CKE# and CS# signal sequence to the SDRAM. The SDRAM is not placed in self-refresh mode and memory contents may be lost.

Mobile SDRAM platforms using normal mode (not MM-config) and 3 DIMM desktop platforms are not affected. 4 DIMM desktop platforms that do not use GCKE are also not affected.

IMPLICATION: The observed effect of the erratum is a system hang, although data loss or corruption is theoretically possible.

WORKAROUND: APM BIOS workaround:

POS, POSCCL, POSCL, STR and C3 states

The workaround disables normal refresh prior to entering these states and before the 443BX automatically generates the SDRAM self-refresh command. BIOS will re-enabling normal refresh on exit from these states.

ACPI BIOS workaround (TBD):

RESOLUTION: Implement BIOS workaround. This erratum will also be fixed in the next stepping of the 82443BX.

INTEL 82443BX ERRATA (Continued)

4. Refresh Collision with SUS_STAT# assertion (EDO Memory)

PROBLEM: On entry to STR or POSCL in a system with EDO memory, if SUSSTAT1# is asserted at the same time a DRAM refresh cycle occurs the normal refresh state machine is left in an improper state. Refresh control is transferred to the suspend refresh state machine which is not affected. When the system resumes from STR, refresh control is returned to the normal refresh state machine which is in an improper state.

IMPLICATION: The system will hang, typically with RAS# stuck high and CAS stuck low. During the execution of the resume code, operation will continue until the BIOS sets the NREF_EN bit to a 1 (443BX, Device#0, Register Offset 7Ah, bit4).

WORKAROUND: A BIOS workaround consisting of aligning the occurrence of the 443BX north bridge refresh cycles away from the transitions of PIIX4 south bridge SUSCLK# (which controls the assertion of SUSSTAT#) is available.

RESOLUTION: Implement BIOS workaround. This erratum will also be fixed in the next stepping of the 82443BX.

INTEL 82443BX SPECIFICATION CLARIFICATIONS

There are currently no known 82443BX Specifications Clarifications.

INTEL 82443BX DOCUMENTATION CHANGES

There are currently no known 82443BX Documentation Changes.