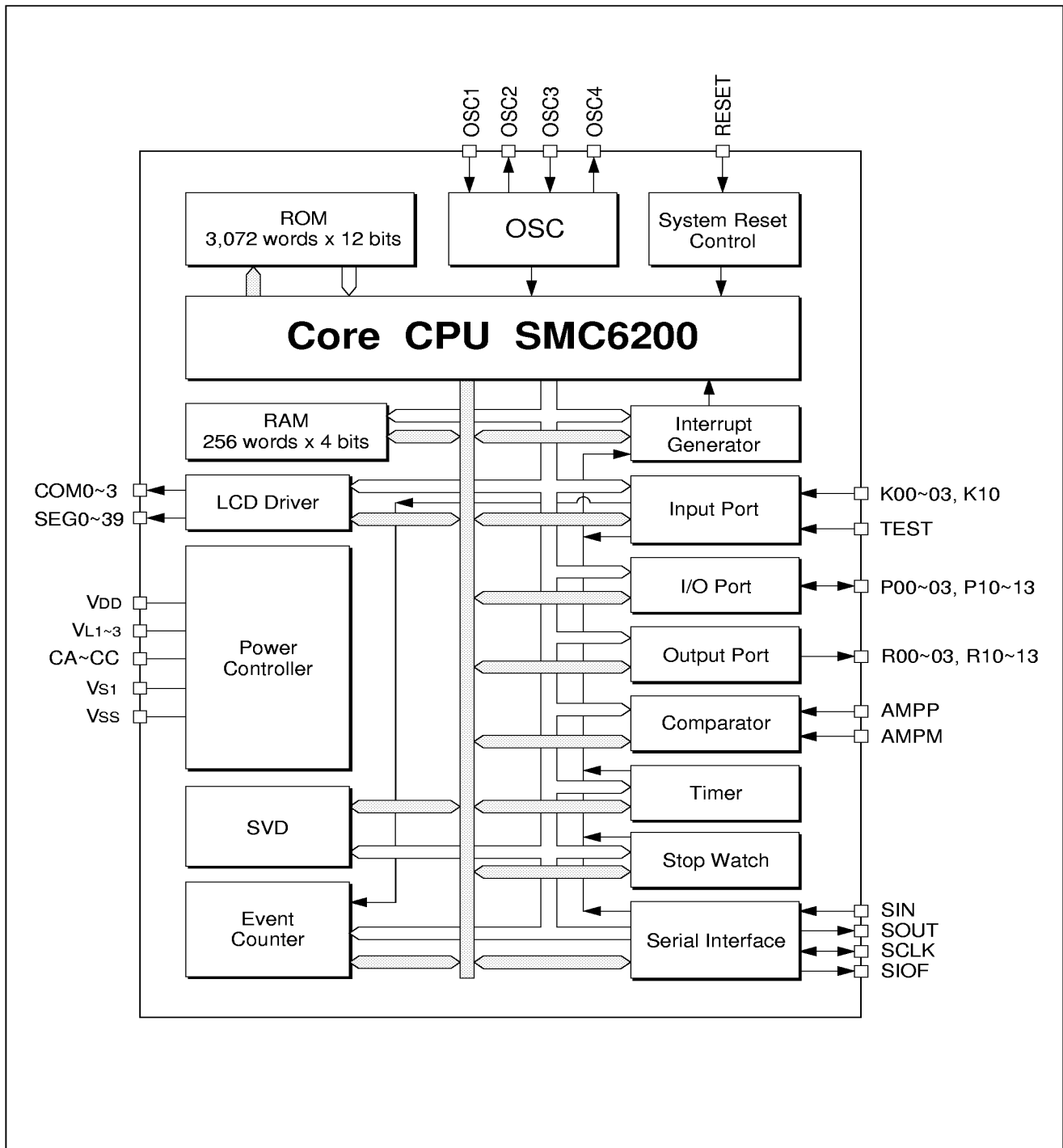
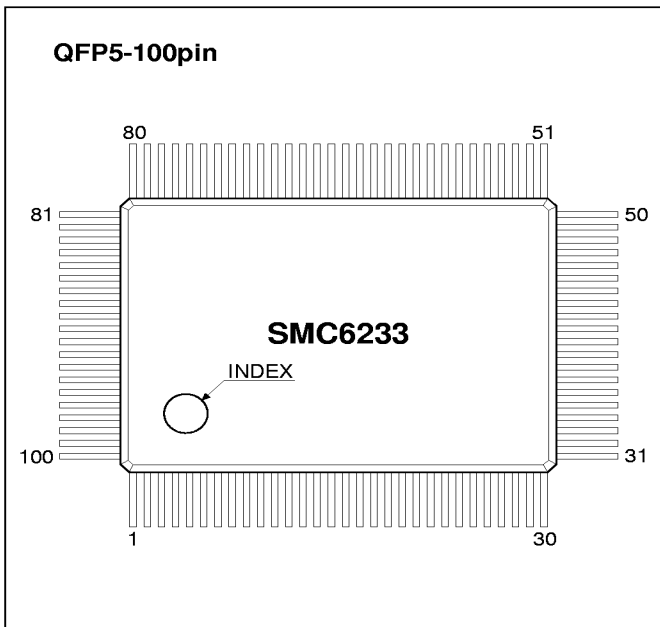


■ BLOCK DIAGRAM



PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	26	SEG38	51	N.C.	76	SIOF
2	N.C.	27	SEG39	52	N.C.	77	SCLK
3	TEST	28	N.C.	53	N.C.	78	N.C.
4	N.C.	29	AMPP	54	N.C.	79	N.C.
5	N.C.	30	N.C.	55	R11	80	N.C.
6	SEG18	31	AMPM	56	R10	81	SOUT
7	SEG19	32	K10	57	R13	82	SIN
8	SEG20	33	K03	58	V _{SS}	83	SEG0
9	SEG21	34	K02	59	RESET	84	SEG1
10	SEG22	35	K01	60	OSC4	85	SEG2
11	SEG23	36	K00	61	OSC3	86	SEG3
12	SEG24	37	P03	62	V _{S1}	87	SEG4
13	SEG25	38	P02	63	OSC2	88	SEG5
14	SEG26	39	P01	64	OSC1	89	SEG6
15	SEG27	40	P00	65	V _{DD}	90	SEG7
16	SEG28	41	P13	66	V _{L3}	91	SEG8
17	SEG29	42	P12	67	V _{L2}	92	SEG9
18	SEG30	43	P11	68	V _{L1}	93	SEG10
19	SEG31	44	P10	69	CC	94	SEG11
20	SEG32	45	R03	70	CB	95	SEG12
21	SEG33	46	R02	71	CA	96	SEG13
22	SEG34	47	N.C.	72	COM3	97	SEG14
23	SEG35	48	R01	73	COM2	98	SEG15
24	SEG36	49	R00	74	COM1	99	SEG16
25	SEG37	50	R12	75	COM0	100	SEG17

N.C. = No Connection

PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V _{DD}	65	I	Power source (+) terminal
V _{SS}	58	I	Power source (-) terminal
V _{S1}	62	O	Oscillation and internal logic system regulated voltage output terminal
V _{L1}	68	O	LCD system regulated voltage output terminal (approx. -1.05 V)
V _{L2}	67	O	LCD system booster output terminal (V _{L1} x 2)
V _{L3}	66	O	LCD system booster output terminal (V _{L1} x 3)
CA-CC	69-71	-	Booster capacitor connecting terminal
OSC1	64	I	Crystal oscillation input terminal
OSC2	63	O	Crystal oscillation output terminal
OSC3	61	I	Ceramic or CR oscillation input terminal (Switchable by mask option, 62A33 only)
OSC4	60	O	Ceramic or CR oscillation output terminal (Switchable by mask option, 62A33 only)
K00-K03, K10	32-36	I	Input terminal
P00-P03, P10-P13	37-44	I/O	I/O terminal
R00-R03	45, 46, 48, 49	O	Output terminal
R10	56	O	Output terminal (DC or BZ output may be selected by mask option)
R13	57	O	Output terminal (DC or BZ output may be selected by mask option)
R11	55	O	Output terminal
R12	50	O	Output terminal (DC or FOUT output may be selected by mask option)
AMPP	29	I	Analog comparator non-inverted input terminal
AMPM	31	I	Analog comparator inverted input terminal
SEG0-39	6-27, 83-100	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0-3	72-75	O	LCD common output terminal
SIN	82	I	Serial interface input terminal
SOUT	81	O	Serial interface output terminal
SCLK	77	I/O	Serial interface clock input/output terminal
SIOF	76	O	Serial interface status output terminal
RESET	59	I	Initial reset input terminal
TEST	3	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

SMC6233/62A33

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-5.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _I OSC	V _{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI _{VSS}	10	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *2	P _D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*2: In case of plastic package (QFP5-100pin).

SMC62L33

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-2.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _I OSC	V _{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI _{VSS}	10	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *2	P _D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*2: In case of plastic package (QFP5-100pin).

● Recommended Operating Conditions

SMC6233

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f _{OSC1}		—	32.768	—	kHz

SMC62L33

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-1.7	-1.5	-1.1	V
		V _{DD} =0V, With software control *1	-1.7	-1.5	-0.9 *2	V
		V _{DD} =0V, When the analog comparator is used	-1.7	-1.5	-1.2	V
Oscillation frequency	f _{OSC1}		—	32.768	—	kHz

*1: When switching to heavy load protection mode. Note, however, that the ON time for SVD in the heavy load protection must be limited to 10 msec per second of operation time.

*2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

SMC62A33

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	f _{OSC1}		—	32.768	—	kHz
Oscillation frequency (2)	f _{OSC3}	duty 50±5%	50	500	600	kHz

● DC Characteristics

SMC6233/62A33

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC1}=32.768kHz$, $T_a=25^{\circ}C$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	K00-03, K10, P00-03, P10-13 SIN, SCLK	$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	V_{IH2}	RESET, TEST	$0.1 \cdot V_{SS}$		0	V
Low level input voltage (1)	V_{IL1}	K00-03, K10, P00-03, P10-13 SIN, SCLK	V_{SS}		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	V_{IL2}	RESET, TEST	V_{SS}		$0.9 \cdot V_{SS}$	V
High level input current (1)	I_{IH1}	$V_{IH1}=0V$ No pull down resistor	0		0.5	μA
High level input current (2)	I_{IH2}	$V_{IH2}=0V$ With pull down resistor	4		16	μA
High level input current (3)	I_{IH3}	$V_{IH3}=0V$ With pull down resistor	25		100	μA
Low level input current	I_{IL}	$V_{IL}=V_{SS}$	-0.5		0	μA
High level output current (1)	I_{OH1}	$V_{OH1}=0.1 \cdot V_{SS}$			-1.8	mA
High level output current (2)	I_{OH2}	$V_{OH2}=0.1 \cdot V_{SS}$			-0.9	mA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.9 \cdot V_{SS}$	6.0			mA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.9 \cdot V_{SS}$	3.0			mA
Common output current	I_{OH3}	$V_{OH3}=-0.05V$			-3	μA
	I_{OL3}	$V_{OL3}=V_{L3}+0.05V$	3			μA
Segment output current (during LCD output)	I_{OH4}	$V_{OH4}=-0.05V$			-3	μA
	I_{OL4}	$V_{OL4}=V_{L3}+0.05V$	3			μA
Segment output current (during DC output)	I_{OH5}	$V_{OH5}=0.1 \cdot V_{SS}$			-200	μA
	I_{OL5}	$V_{OL5}=0.9 \cdot V_{SS}$	200			μA

SMC62L33

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{OSC1}=32.768kHz$, $T_a=25^{\circ}C$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	K00-03, K10, P00-03, P10-13 SIN, SCLK	$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	V_{IH2}	RESET, TEST	$0.1 \cdot V_{SS}$		0	V
Low level input voltage (1)	V_{IL1}	K00-03, K10, P00-03, P10-13 SIN, SCLK	V_{SS}		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	V_{IL2}	RESET, TEST	V_{SS}		$0.9 \cdot V_{SS}$	V
High level input current (1)	I_{IH1}	$V_{IH1}=0V$ No pull down resistor	0		0.5	μA
High level input current (2)	I_{IH2}	$V_{IH2}=0V$ With pull down resistor	2		10	μA
High level input current (3)	I_{IH3}	$V_{IH3}=0V$ With pull down resistor	12		60	μA
Low level input current	I_{IL}	$V_{IL}=V_{SS}$	-0.5		0	μA
High level output current (1)	I_{OH1}	$V_{OH1}=0.1 \cdot V_{SS}$			-300	μA
High level output current (2)	I_{OH2}	$V_{OH2}=0.1 \cdot V_{SS}$			-150	μA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.9 \cdot V_{SS}$	1,400			μA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.9 \cdot V_{SS}$	700			μA
Common output current	I_{OH3}	$V_{OH3}=-0.05V$			-3	μA
	I_{OL3}	$V_{OL3}=V_{L3}+0.05V$	3			μA
Segment output current (during LCD output)	I_{OH4}	$V_{OH4}=-0.05V$			-3	μA
	I_{OL4}	$V_{OL4}=V_{L3}+0.05V$	3			μA
Segment output current (during DC output)	I_{OH5}	$V_{OH5}=0.1 \cdot V_{SS}$			-100	μA
	I_{OL5}	$V_{OL5}=0.9 \cdot V_{SS}$	100			μA

● Analog Circuit Characteristics and Current Consumption

SMC6233 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, T_a=25°C, C_G=25pF, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load)	2•V _{L1} -0.1		2•V _{L1} ×0.9	V
	V _{L3}	Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load)	3•V _{L1} -0.1		3•V _{L1} ×0.9	V
SVD voltage	V _{SVD}		-2.55	-2.40	-2.25	V
SVD circuit response time	t _{SVD}				100	μS
Analog comparator input voltage	V _{IP}	Noninverted input (AMPP)	V _{SS} +0.3		V _{DD} -0.9	V
	V _{IM}	Inverted input (AMPM)				
Analog comparator offset voltage	V _{OF}				10	mV
Analog comparator response time	t _{AMP}	V _{IP} =-1.5V, V _{IM} =V _{IP} ±15mV			3	mS
Current consumption	I _{OP}	During HALT		1.5	4.0	μA
		During operation *1	Without panel load	6.0	10.0	μA

*1: The SVD circuit and analog comparator are in the OFF status.

SMC6233 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, T_a=25°C, C_G=25pF, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load)	2•V _{L1} -0.1		2•V _{L1} ×0.9	V
	V _{L3}	Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load)	3•V _{L1} -0.1		3•V _{L1} ×0.9	V
SVD voltage	V _{SVD}		-2.55	-2.40	-2.25	V
SVD circuit response time	t _{SVD}				100	μS
Analog comparator input voltage	V _{IP}	Noninverted input (AMPP)	V _{SS} +0.3		V _{DD} -0.9	V
	V _{IM}	Inverted input (AMPM)				
Analog comparator offset voltage	V _{OF}				10	mV
Analog comparator response time	t _{AMP}	V _{IP} =-1.5V, V _{IM} =V _{IP} ±15mV			3	mS
Current consumption	I _{OP}	During HALT		11.2	34.0	μA
		During operation *1	Without panel load	14.5	40.0	μA

*1: The SVD circuit is in the ON status (HVLD="1", SVDON="0"). The analog comparator is in the OFF status.

SMC62L33 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, T_a=25°C, C_G=25pF, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load)	2•V _{L1} -0.1		2•V _{L1} ×0.9	V
	V _{L3}	Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load)	3•V _{L1} -0.1		3•V _{L1} ×0.9	V
SVD voltage	V _{SVD}		-1.30	-1.20	-1.10	V
SVD circuit response time	t _{SVD}				100	μS
Analog comparator input voltage	V _{IP}	Noninverted input (AMPP)	V _{SS} +0.3		V _{DD} -0.9	V
	V _{IM}	Inverted input (AMPM)				
Analog comparator offset voltage	V _{OF}				20	mV
Analog comparator response time	t _{AMP}	V _{IP} =-1.1V, V _{IM} =V _{IP} ±30mV			3	mS
Current consumption	I _{OP}	During HALT		1.0	3.0	μA
		During operation *1	Without panel load	3.0	8.0	μA

*1: The SVD circuit and analog comparator are in the OFF status.

SMC62L33 (Heavy Load Protection Mode)

(Unless otherwise specified: VDD=0V, VSS=-1.5V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, Vs1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.85	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.85	V
SVD voltage	VSVD		-1.30	-1.20	-1.10	V
SVD circuit response time	tSVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (AMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (AMPM)				
Analog comparator offset voltage	VOF				20	mV
Analog comparator response time	tAMP	VIP=-1.1V, VIM=VIP±30mV			3	mS
Current consumption	IOP	During HALT *1		2.0	7.0	μA
		During operation *1	Without panel load	8.0	18.0	μA

*1: The SVD circuit is in the ON status (HVLD="1", SVDON="0"). The analog comparator is in the OFF status.

SMC62A33 (Normal Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, Vs1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.9	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
SVD voltage	VSVD		-2.55	-2.40	-2.25	V
SVD circuit response time	tSVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (AMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (AMPM)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tAMP	VIP=-1.5V, VIM=VIP±15mV			3	mS
Current consumption	IOP	During HALT	Without panel load	2.0	5.0	μA
		During operation at 32kHz *1	OSCC="0"	8.0	15.0	μA
		During operation at 500kHz *1	Without panel load	135	300	μA

*1: The SVD circuit and analog comparator are in the OFF status.

SMC62A33 (Heavy Load Protection Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, Vs1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.9	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
SVD voltage	VSVD		-2.55	-2.40	-2.25	V
SVD circuit response time	tSVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (AMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (AMPM)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tAMP	VIP=-1.5V, VIM=VIP±15mV			3	mS
Current consumption	IOP	During HALT	Without panel load	11.5	35.0	μA
		During operation at 32kHz *1	OSCC="0"	16.0	45.0	μA
		During operation at 500kHz *1	Without panel load	130	330	μA

*1: The SVD circuit is in the ON status (HVLD="1", SVDON="0"). The analog comparator is in the OFF status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

SMC6233 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤5sec (V _{SS})	-1.8			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-1.8			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		18		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-3.5	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

SMC62L33 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤5sec (V _{SS})	-1.1			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		18		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-1.1 to -1.7V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-1.7	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

*1: Items enclosed in parentheses () are those used when operating at heavy load protection mode.

Note, however, that the ON time for SVD must be limited to 10 msec per second of operation time.

SMC62A33 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤5sec (V _{SS})	-2.2			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-2.2			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		18		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-2.2 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-3.5	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

SMC62A33 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, T_a=25°C)

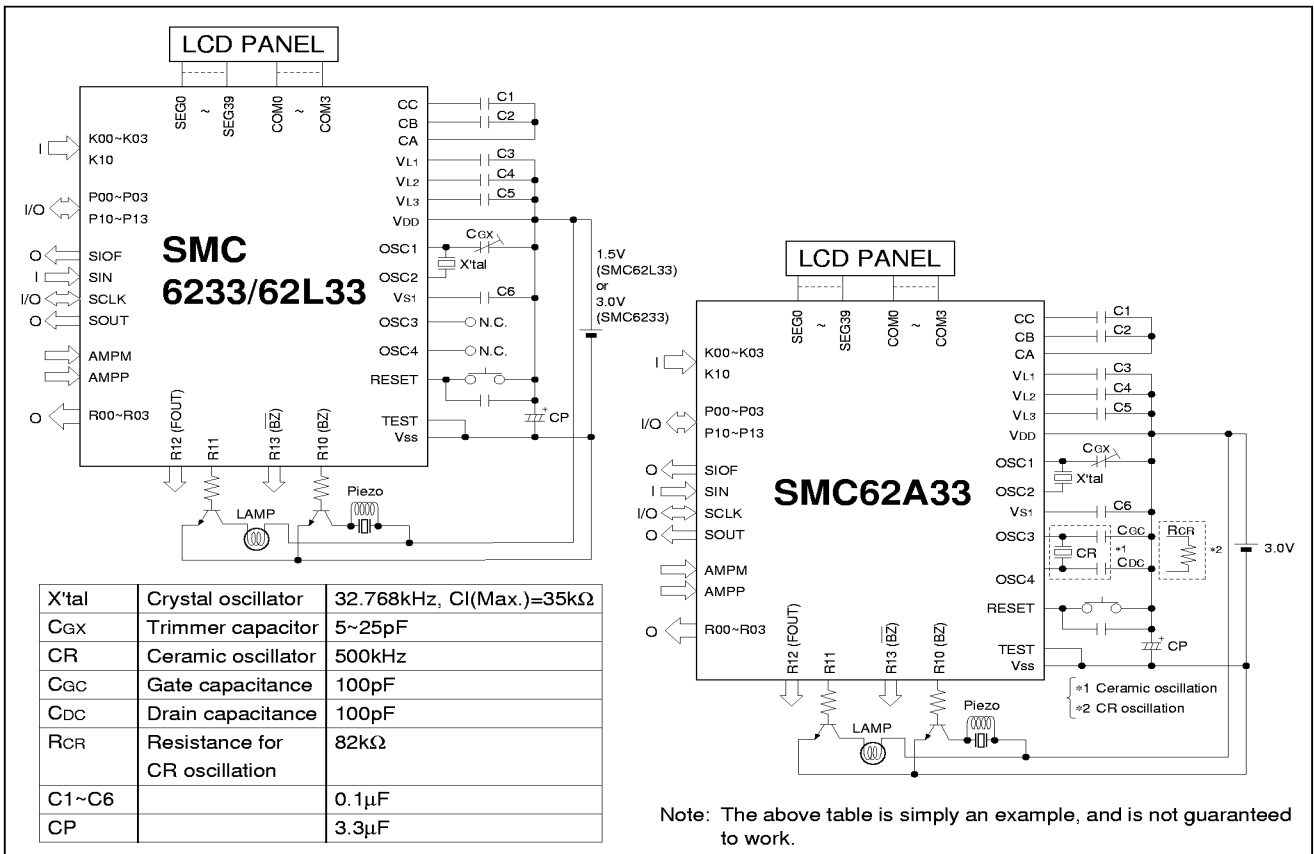
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f _{osc3}		-30	430kHz	30	%
Oscillation start voltage	V _{sta}	(V _{SS})	-2.2			V
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -3.5V			3	mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-2.2			V

SMC62A33 (Ceramic oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 500kHz, C_{Gc}=C_{Dc}=100pF, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	(V _{SS})	-2.2			V
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -3.5V			5	mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM



■ PACKAGE DIMENSIONS

