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NEW PRODUCT RELEASE

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TITLE

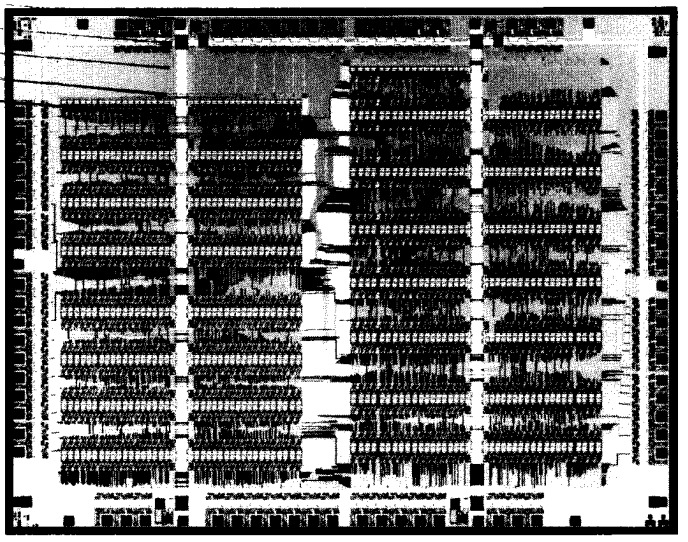
ULA* 'DS' SERIES

ORIG

see pages for Generics

FEATURES

- System Speeds to 100MHz
- Complexities to 10,000 gates
- Average gate power 165μW at 100MHz
- 48mA bus drivers
- Digital and Linear Macros
- Complete CAD Support
- Silicon Compilers



DESCRIPTION

The need to manipulate increasingly large amounts of data means that digital systems are developing an insatiable appetite for speed.

To meet these demands for higher speeds, plus the need for increased system complexity and performance, an ASIC approach is essential. Assessing the ability of a particular VLSI technology to meet a required system speed can however be difficult.

Gate delay is the basic speed parameter normally specified, and since this can be affected significantly by such system criteria as fan-out, supply voltage, clock frequency, capacitive loading, system complexity and temperature, it is often difficult to quantify the speed capability of the technology being considered.

The 'DS' series of ULAs* has been developed specifically to provide a low power ASIC solution for systems with speed requirements to over 100MHz and complexities from 500 to 10,000 gates.

'DS' Series of ULAs for 100 MHz Digital ASIC Systems

The series features gate delays, to below 1ns, which are virtually independent of fan-out, supply voltage and clock frequency, and flip-flops with clock to output delays of 1.5ns. The I/O cells are designed to allow the integration of special digital and linear functions which would normally require external components. Each cell contains a high current transistor to provide 48mA for direct bus drive.

Utilising 'Differential Logic' Macros, the 1.5 micron, double metal Ferranti Advanced Bipolar process – FAB 3, fully supported by the powerful ULACAD software system including silicon compilers for chip implementation, makes the 'DS' series of ULAs one of the most advanced performance, high speed, ASIC product ranges available.

*Silicon Design System is a trademark of Ferranti plc.
*ULA is a registered trademark of Ferranti plc for semiconductor devices.
*VAX is a trademark of the Digital Equipment Corporation.

FERRANTI INTERDESIGN, INC.

FEATURES

- SYSTEM COMPLEXITY
  500 to 10,000 gates

- OUTSTANDING SPEED PERFORMANCE
  True system performance: 100MHz
  'Differential Logic' flip-flop:
  clock to output delay 1.5ns
  clock frequency 250MHz
  Gate delay: 1ns
  virtually independent of fan-out, supply voltage and clock frequency

- LOW POWER PERFORMANCE
  'Differential Logic' Flip-Flop

at 250MHz:	750μW (at 5V)
	375μW (at 2.5V)
at 140MHz:	380μW (at 5V)
	190μW (at 2.5V)
at 50MHz:	137μW (at 5V)
	69μW (at 2.5V)

  Average Gate Power

at 100MHz:	330μW (at 5V)
	165μW (at 2.5V)
at 60MHz:	165μW (at 5V)
	83μW (at 2.5V)
at 25MHz:	55μW (at 5V)
	28μW (at 2.5V)

- COMPLETE CAD SUPPORT
  ULACAD Software covers Design, Simulation and Implementation
  Flexible Customer Interface
  Design Support for Commercial Workstations
  Silicon Compilers for 100% Autorouting and Optimisation
  Transportable Software for VAX* Based Systems
  Extensive Range of Fully Characterised Macros
  User Defined Macro Facility

- OUTSTANDING I/O CAPABILITY
  High Current Bus Drivers: 48mA at 0.5V
  Low Output Delays Driving High Capacitance Loads
  Wide range of Digital and Linear I/O Macros

- WIDE RANGE OF PACKAGE STYLES AND PIN COUNTS

FERRANTI ADVANCED BIPOLAR PROCESS – FAB 3

Key to the performance is a new 1.5 micron advanced bipolar process with double layer metal featuring 6 micron grid pitch on both layers. It offers high and predictable speeds, low power levels and high current drive without chip area penalty.

It also provides the important bipolar performance advantages of excellent linear capability. This capability is particularly beneficial since it allows more of the system to be integrated. This offers the opportunity to further improve cost effectiveness and reduce overall system power requirements.

'DIFFERENTIAL LOGIC'

'Differential Logic' is a radical approach to logic function design. It provides an order of magnitude improvement in speed-power product, ensuring that system power levels are kept to a minimum. It achieves a two to four times improvement in speed, with the added advantage that the flip-flop clock to output delay is less than two equivalent gate delays.

'Differential Logic' is based on steering current through a logic tree by means of differential pairs of transistors stacked across the supply rail (Fig. 1). Many complex and elegant logic functions can be implemented using this technique which is unique to bipolar technology. Unlike ECL, differential logic eliminates the need to generate and distribute accurate temperature compensated voltage references. Its inherent common mode rejection removes problems associated with noise, crosstalk, supply voltage distribution drops and variations in temperature.

A differential pair of transistors also has an extremely linear and sharp transfer characteristic. This enables differential gates to operate with logic swings as low as 100mV whilst retaining the same discrimination between logic levels as single ended circuits which have logic swings of 400mV or greater. Since power dissipation is directly proportional to logic swing, a power saving of 4:1 can be achieved with no compromise in speed.

In addition, differential logic has two further significant advantages illustrated by the 2 level D-type flip-flop (Fig. 2) employed in the DS series.

1. Only two current sources are required to support the basic Master-Slave flip-flop function compared to six for a D-type flip-flop based on conventional gates.
2. The propagation delay from the active clock edge to both outputs is only marginally greater than for a single gate compared with two or three gates for conventional D-types.

'Differential Logic' automatically provides the true and inverse of every input and output removing the need for inverters. Hence an AND gate can become an OR, NOR or NAND simply by changing the order in which the connections are made. The significance of eliminating inverters is that the overall system speed can be increased for a given gate delay.

'Differential Logic' therefore provides a substantial increase in speed while greatly reducing the power. Moreover it is ideally suited to a hierarchical design approach, using the 'Differential Logic' macros available within the ULACAD software for VAX based systems.

FIGURE 1. DIFFERENTIAL LOGIC

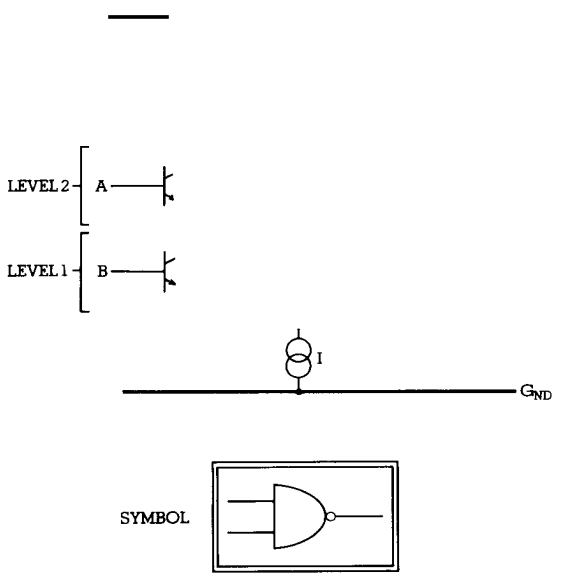
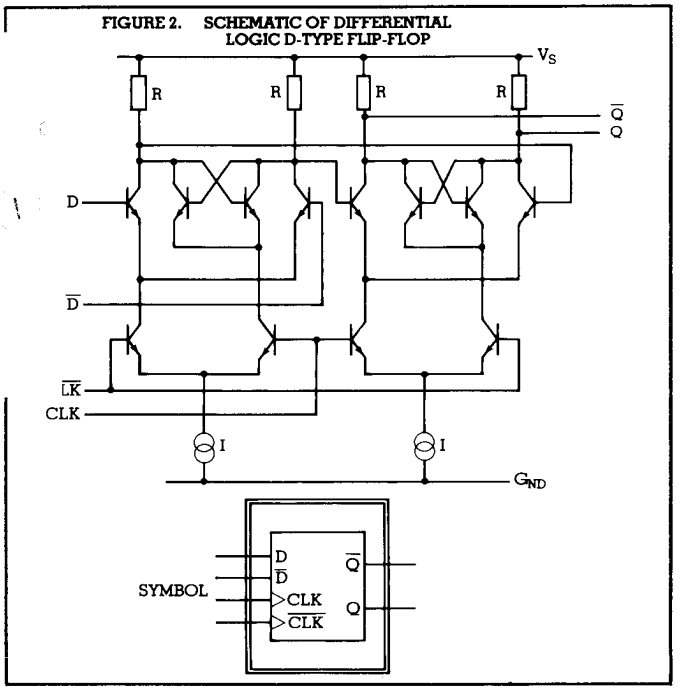


FIGURE 2. SCHEMATIC OF DIFFERENTIAL LOGIC D-TYPE FLIP-FLOP



SYSTEM SPEED

The fundamental factors determining system speeds are toggle rates of bistables and propagation delays through random logic, and the effect of loading on these parameters.

The outstanding performance of 'Differential Logic' functions is complemented by the high speed basic gate featured in the 'DS' Series of ULAs. The propagation delay of this gate, which can be less than 1ns, is virtually independent of fan-out, supply voltage and clock frequency. Fig. 3 shows the effect of fan-out on gate delay and compares a DSA Series gate with the degradation experienced by a typical CMOS gate. The inverter driver gate also features this virtual independence of fan-out loading, as seen in Fig 4.

This excellent perfomance under high load conditions is further enhanced by the clock driver gate. This gate has been designed to directly drive the very high fan-outs experienced on clock lines, avoiding partitioning into tree structures with its associated clock skew problems. The performance of this gate is shown in Fig. 5.

The effect of loading is equally important with the logic macro functions. Fig. 6 shows a similar improvement in performance using the Differential Logic D-Type Flip Flop.

The ULACAD design software allows full advantage to be taken of these features during system design.

FIGURE 3.
INTERNAL LOGIC GATE
PROPAGATION DELAYS

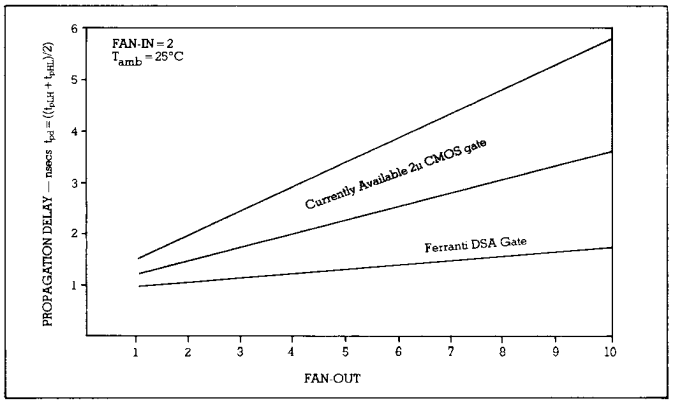


FIGURE 4.
INVERTER DRIVER GATE
PROPAGATION DELAYS

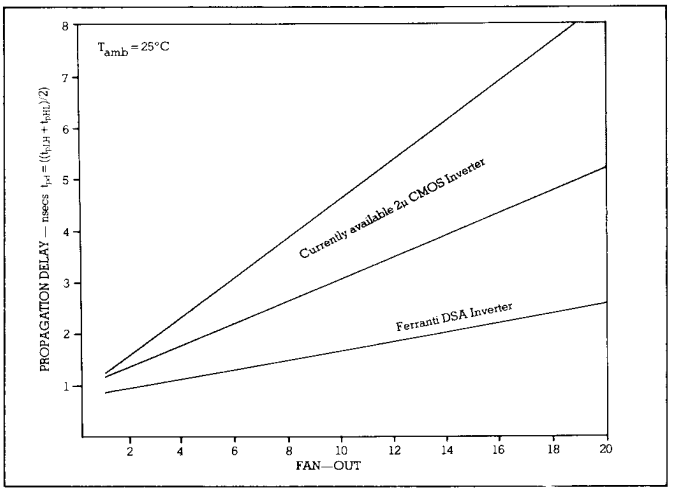


FIGURE 5.
PROPAGATION DELAYS FOR
HIGH FAN-OUT

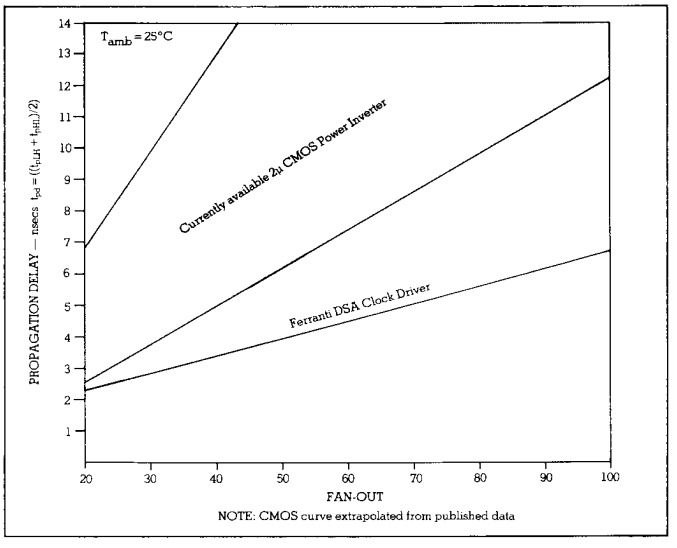
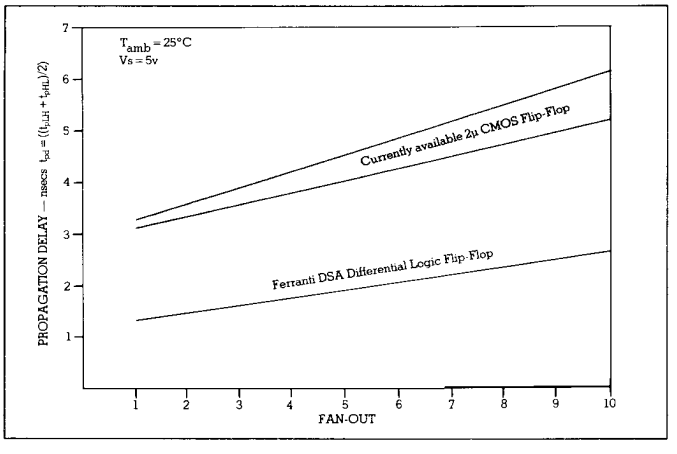


FIGURE 6.
D-TYPE FLIP-FLOP
PROPAGATION DELAYS



THE 'DS' SERIES

ULA TYPE	ULA 6DS	ULA 12DS	ULA 19DS	ULA 25DS	ULA 32DS	ULA 38DS	ULA 47DS	ULA 60DS	ULA 80DS	ULA 100DS
Total Matrix Cells	252	484	748	1020	1292	1596	1944	2484	3168	4000
Equivalent Gates*	630	1210	1870	2550	3230	3990	4860	6210	7920	10000
Peripheral I/O Cells	32	44	64	74	82	90	104	122	138	138
Bond Pads	40	52	72	82	92	100	114	132	150	150

*A gate is defined as one 2 input - 2 output RNOR gate.

SPEED/POWER OPTIONS

A range of speed/power options are available for each of the 'DS' ULA types.

GATE PARAMETER	ARRAY T DSA	DSB
For system speeds up to	100	60
RNOR gate delay — t_{pd}*	1.0	1.6
RNOR gate delay — t_{pd}	1.4	2.4
Average gate current — I_g	66	33

Typical figures at T_{amb} = 25°C
*With selective use of additional matrix cell components

NOTES: 1. $t_{pd} = (t_{pLH} + t_{pHL})/2$
2. Figures are for 2 input gate, FAN-OUT = 2, with typical interconnect metal.
3. Gate current at 60% duty cycle.

GENERIC =
ULA 6DS
TECH = BIPOLAR
SIGN NAME = # GATE ARRAY
ULA 100DS

'DIFFERENTIAL LOGIC'

The use of 'Differential Logic' Macros provides an order of magnitude improvement in speed/power product.

DIFFERENTIAL LOGIC D-TYPE FLIP-FLOP	ARRAY TYPE DSA	DSB	DSC	UNIT
Toggle frequency	250	150	75	MHz
Clock to Output delay	1.5	2.7	7.5	ns
Current	150	76	27.4	μA

Typical figures at T_{amb} = 25°C.

NOTE: 'Differential Logic' currently only available for VAX based system designs

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RANGE	UNIT
V_{CC}	Supply Voltage	−0.5 min +7.0 max	V
V_{IN}	Input Voltage	−0.5 min +5.5 max	V
T_{amb}	Operating Temperature	−55 min +125 max	°C
T_{stg}	Storage Temperature	−65 min +150 max	°C

NOTE: Operation at absolute maximum ratings is not implied. Exposure to stresses greater than those listed may affect reliability and could cause permanent damage to the device.

D.C. CHARACTERISTICS

At nominal V_{CC} = 5V over temperature range T_{amb} = 0 to 70°C

SYMBOL	PARAMETER	CONDITIONS	ARRAY TYPE	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		ALL	4.5	5.0	5.5	V
V_{IH}	High Level Input Voltage	TTL Input	ALL	2.0		5.5	V
V_{IL}	Low Level Input Voltage	TTL Input	ALL	0		0.8	V
I_{IH}	High Level Input Current	TTL Input $V_{IH} = V_{CC}$	ALL	0		10	μA
I_{IL}	Low Level Input Current	TTL Input V_{IL} = 0.4V	DSA	0		−0.6	mA
			DSB	0		−0.4	mA
			DSC	0		−100	μA
V_{OH}	High Level Output Voltage	Totem Pole Output, Tristate Output $I_O = I_{OH}$	ALL	2.4	3.4		V
V_{OL}	Low Level Output Voltage	Totem Pole Output, Tristate Output $I_O = I_{OL}$	ALL			0.5	V
I_{OH}	High Level Output Current	Totem Pole Output, Tristate Output	ALL			−400	μA
I_{OL}	Low Level Output Current	Totem Pole Output, Tristate Output, Open Collector Output V_{OL} = 0.5V	DSA			16	mA
			DSB			8	mA
			DSC			1.6	mA
		High Current Output Driver V_{OL} = 0.5V	All			48	mA

DIGITAL AND LINEAR MACROS

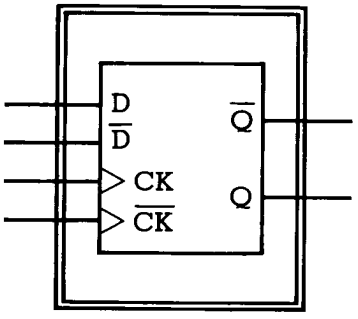
A wide range of fully characterised elements, from logic gates and functions to MSI, LSI and I/O Macros, are available for system specification and design. The elements also include 'Differential Logic' Macros.

The Macro Library, which is continually being expanded, contains well in excess of 100 different design elements which have been fully simulated and characterised. In addition, the designer can create user defined variants of these Macros.

Shown below are some typical examples of design elements.

DIFFERENTIAL LOGIC D-TYPE FLIP-FLOP

SYMBOL

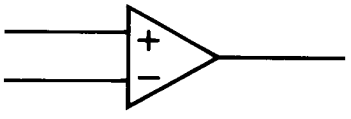


PARAMETER	ARRAY TYPE DSA	DSB	DSC	UNIT
Toggle Frequency	250	140	50	MHz
Clock to Output Delay	1.5	2.7	7.5	ns
Data Set Up Time	1	1.5	4.2	ns
Data Hold Time	0.5	0.9	2.5	ns
Cell Count	4	4	4	
Current	150	76	27.4	μA

Typical figures at T_{amb} = 25°C

VOLTAGE COMPARATOR

SYMBOL

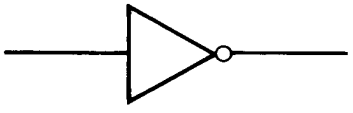


PARAMETER	ARRAY TYPE DSA	DSB	DSC	UNIT
Voltage Gain	45	45	45	dB
Offset Voltage	±10	±10	±10	mV
Bias Current	2	2	1.5	μA
CM Range	1-3	1-3	1-3	V
Bandwidth	6	6	4	MHz
I_{CC} Average	2.4	2.4	1.8	mA

Typical figures at T_{amb} = 25°C

48mA OUTPUT DRIVER

SYMBOL



PARAMETER	ARRAY TYPE DSA	DSB	DSC	UNIT
V_{OL} (max)	0.5	0.5	0.5	V
I_{OL} (max)	48	48	48	mA
I_{OFF} (max)	20	20	20	μA
T_{ON}	15	15	25	ns
T_{OFF}	15	15	25	ns
I_{CC} (for input = 1)	1.8	1.8	1.8	mA
I_{CC} (for input = 0)	2.2	2.2	2.2	mA
I_{CC} Average	2	2	2	mA

NOTE: Load C_L = 15pF

Typical figures at T_{amb} = 25°C

DESIGN CENTRES

There is a network of ULA Design Centres. Each Design Centre is staffed by a team of fully qualified and experienced ULA system design engineers supported by the Ferranti Silicon Design System*. The Silicon Design System is built around the powerful VAX range of computers with the complete suite of ULACAD software.

ULACAD SYSTEM SOFTWARE

The ULACAD software system was developed in parallel with the DS series to ensure complete compatibility between the software system and chip hardware. It covers the complete cycle of design, simulation and chip implementation for ULA based custom LSI.

SILICON COMPILERS

An important feature of the software system is the use of Silicon Compilers. The Silicon Compiler software, which includes the interconnect compiler and the optimising compiler, ensures that the physical layout is automatic without the need for manual intervention.

The interconnect compiler automatically produces the required interconnect routing that is needed to customise the selected array. This route gives the fastest turn around since it utilises uncommitted array wafers that are kept in stock awaiting metalisation.

The optimising compiler is even more powerful and automatically defines all the base layers plus the interconnect routing to produce a full custom chip size which precisely matches the system complexity. In this way all component redundancy is removed and the routing channels are optimised for the necessary tracking. This facility is used for large volume requirements where the benefits of full custom economics are needed.

DESIGN ROUTE

The overall ULA design takes place in the two software environments, the Design Environment and the Physical Environment.

The Design Environment enables the engineer to design, simulate and verify his system and its test schedule. The tools provide complete interactive design simulation including timing verification, test program generation and test schedule verification.

When the design stage has been completed, the verified data is transferred to the Physical Environment for chip implementation.

The Physical Environment, including the silicon compilers, handles all aspects of chip design up to the verified masks from which engineering check samples are produced.

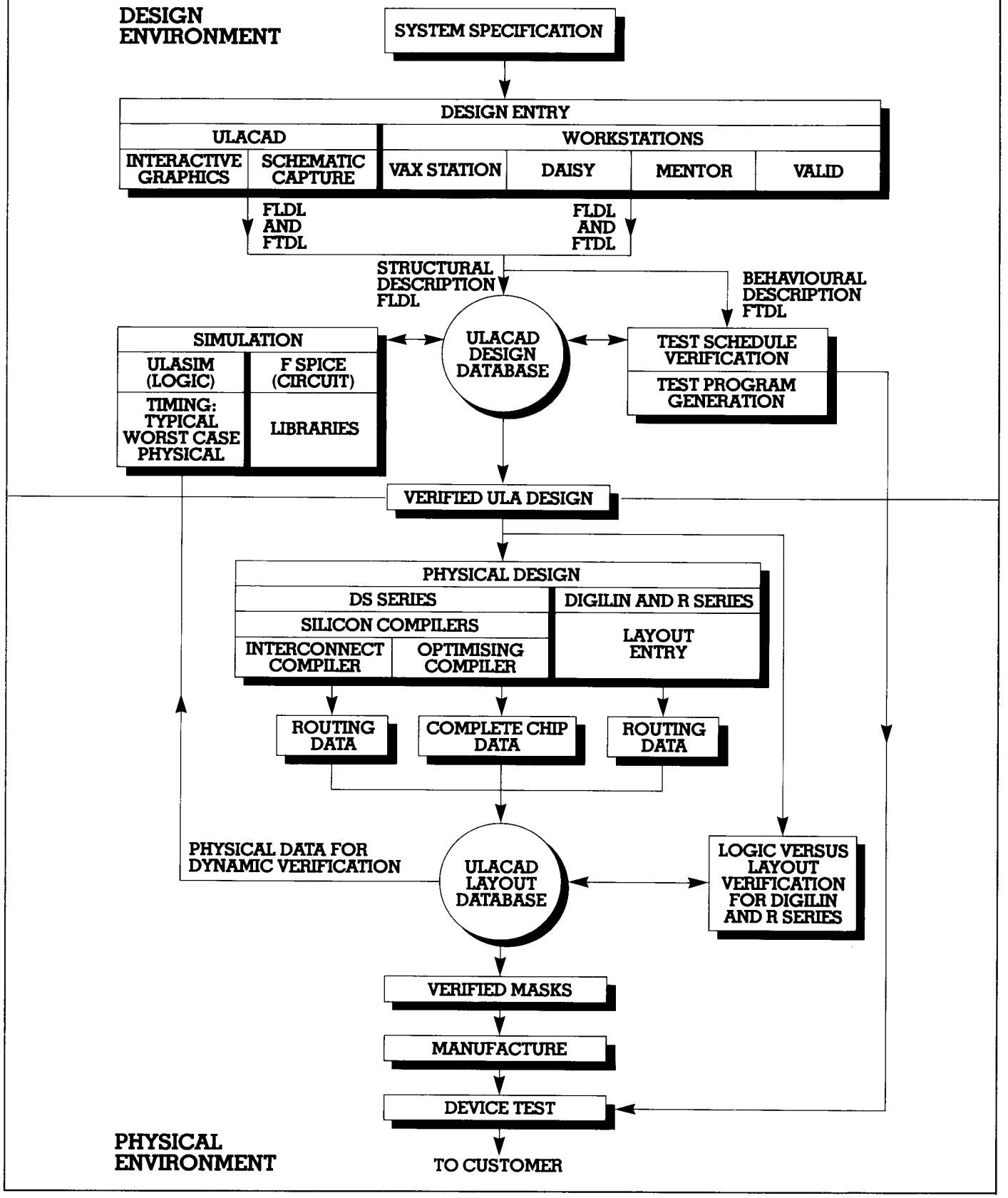
CUSTOMER INTERFACE

There are several customer entry levels into the design route. The choice of entry level depends on the CAE tools available to the customer and the extent to which he wishes to become involved in the detailed design. They provide for a range of customer skills from breadboarding to the production of completely verified designs on customer workstations or mainframe systems.

WORKSTATIONS

The full ULACAD software, including 'Differential Logic' and the interconnect compiler, is portable onto any customer's VAX mainframe. The ULACAD software, covering design prior to interconnect routing, is available for use on VAX Station, Daisy, Mentor and Valid workstations. 'Differential Logic' is currently available for use on VAX based systems only.

DESIGN ROUTE FLOW CHART



NOTE: FLDL is the high level FERRANTI LOGIC DESCRIPTION LANGUAGE in which the structural aspect of the design is produced.

FTDL is the high level FERRANTI TEST DESCRIPTION LANGUAGE used to produce the Behavioural Description of the design.

DESIGN AND CAD SUPPORT DOCUMENTATION

DESIGN DOCUMENTS:

Ref. No.	Title	Contents
ED850	Preferred TTL List	Recommended TTL types for ease of logic conversion to ULA format
ED860	Test Pattern Preparation	Guide to the generation of test information and vectors
A/F 111	Ferranti Logic Macro Function Library	Set of commonly used logic functions and MSI and LSI Macros
DS/100	DS Design Manual	Information necessary for system designer to create integrations using DS arrays
DS/110	VALID Workstation Manual	DS Design Manual for use with Valid workstations
DS/120	MENTOR Workstation Manual	DS Design Manual for use with Mentor workstations
DS/130	DAISY Workstation Manual	DS Design Manual for use with Daisy workstations
DS/200	DS Physical Design Manual	User guide to DS Physical Parameters and CAD autolayout system

CAD DOCUMENTS:

Ref. No.	Title	Contents
Language Documents		
A/F 803	Ferranti Logic Description Language (FLDL II)	User guide to ULA description language for logic
A/F 806	Ferranti Test Description Language (FTDL)	User guide to ULA description for test
A/F 805	ERICA II User Manual	Command set and modelling technique for logic investigation
System Documents		
A/F 900	CAD System Overview	Descriptive overview of the ULACAD system
A/F 901	ULA SYSTEM Manual	User guide to CAD system — operation of CAD and main menus
A/F 902	ULA LAYOUT Manual	User guide to ULA layout — editing, digitising, management
A/F 903	ULALOGIC Manual	User guide to the Logic Database
A/F 904	ULATEST Manual	User guide to the ULACAD System Test area
A/F 905	ULASIM Manual	User guide to the ULACAD Simulation area
A/F 906	ULACHECK Manual	User guide to the ULACAD Layout check area
A/F 910	ULASPICE Manual	User guide to the SPICE system and modelling parameters

PACKAGING

Various package styles are available including dual-in-line, flat packs, ceramic and plastic chip carriers and pin grid.

The selection of a suitable package for a given application is determined by a number of factors:

- number of input and output nodes
- number of V_{CC} and ground connections
- application environment and temperature range
- array die size relative to package island size
- power dissipation
- method of mounting package to substrate and substrate material