

## VIDEO CONTROL COMBINATION

The TDA3501 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).

The required input signals are: luminance and colour difference  $-(R-Y)$  and  $-(B-Y)$ , while linear RGB signals can be inserted from an external source.

RGB signals are provided at the output to drive the video output stages.

The TDA3501 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 2 d.c. gain controls for the green and blue output signals (white point adjustment)
- beam current limiting possibility

### QUICK REFERENCE DATA

Supply voltage	V <sub>6-24</sub>	typ.	12 V
Supply current	I <sub>6</sub>	typ.	100 mA
Luminance input signal (peak-to-peak value)	V <sub>15-24(p-p)</sub>	typ.	0,45 V
Luminance input resistance	R <sub>15-24</sub>	typ.	12 kΩ
Colour difference input signals (peak-to-peak values)			
$-(B-Y)$	V <sub>18-24(p-p)</sub>	typ.	1,33 V
$-(R-Y)$	V <sub>17-24(p-p)</sub>	typ.	1,05 V
Inserted RGB signals (peak-to-peak values)	V <sub>12,13,14-24(p-p)</sub>	typ.	1 V
Three-level sandcastle pulse detector	V <sub>10-24</sub>	typ.	2,5/4,5/8,0 V
Control voltage ranges			
brightness	V <sub>20-24</sub>		1 to 3 V
contrast	V <sub>19-24</sub>		2 to 4 V
saturation	V <sub>16-24</sub>		2,1 to 4 V

### PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

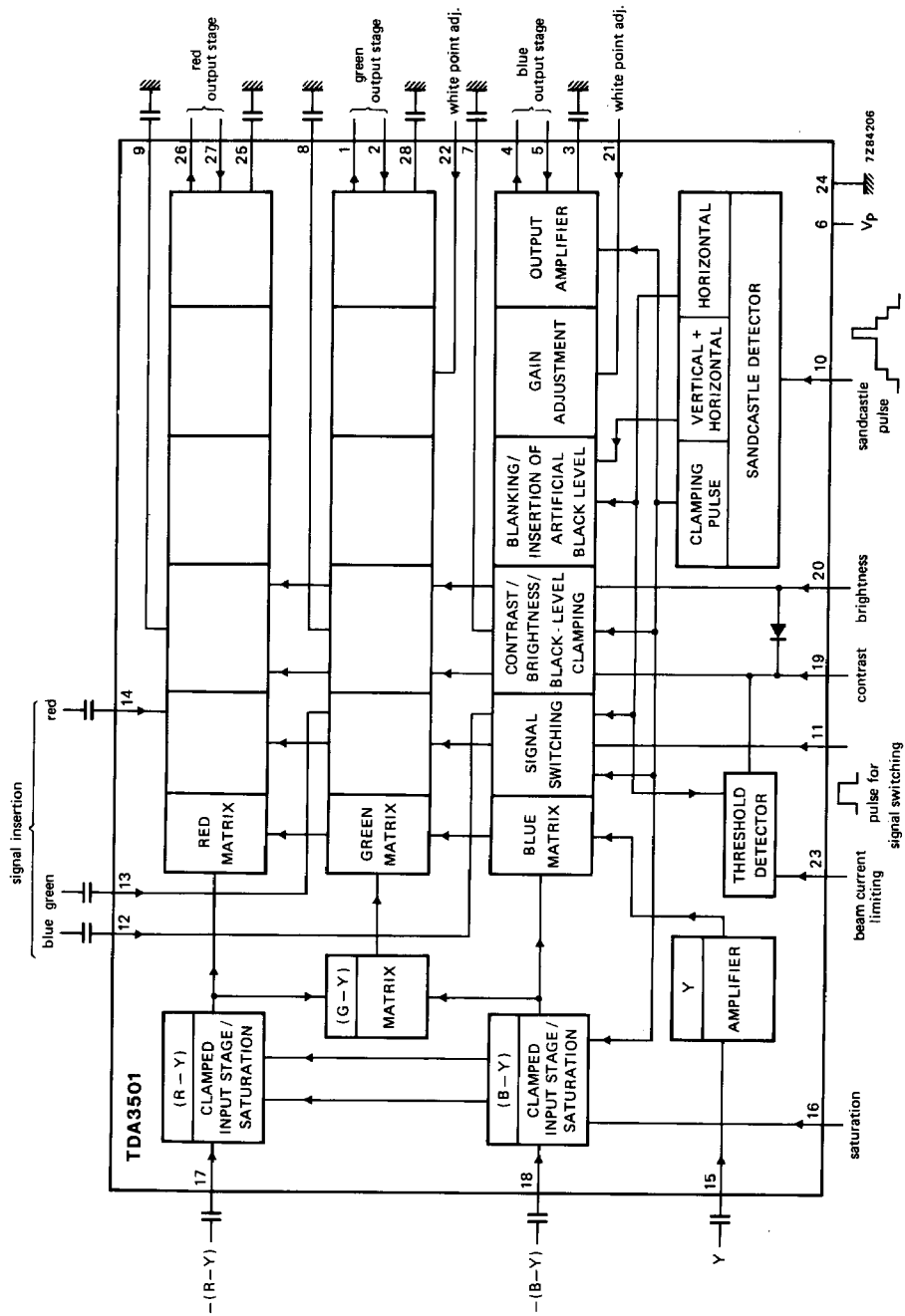


Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	max.	
Supply voltage	$V_P = V_{6-24}$	—	13,2	V
Voltages with respect to pin 24				
pins 1,4,26	$V_{1,4,26-24}$	$\frac{1}{2}V_P$	$V_P + 1$	V
pins 2,5,27	$V_{2,5,27-24}$	0	$V_P$	V
pin 10	$V_{10-24}$	0	$V_P$	V
pin 11	$V_{11-24}$	-0,5	3	V
pins 16,19,20	$V_{16,19,20-24}$	0	$\frac{1}{2}V_P$	V
pins 21,22	$V_{21,22-24}$	0	$V_P$	V
pin 23	$V_{23-24}$	0	$V_P$	V
pins 3,25,28; 7,8,9; 12,13,14; 15,17,18	no external d.c. voltage			
Current at pin 20	$I_{20}$	max.	5	mA
Total power dissipation	$P_{tot}$	max.	1,7	W
Storage temperature	$T_{stg}$		-25 to + 125	°C
Operating ambient temperature	$T_{amb}$		0 to + 70	°C

## CHARACTERISTICS

Supply voltage range	$V_P$		10,8 to 13,2	V
The following characteristics are measured in Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C; $V_{18-24(p-p)} = 1,33$ V; $V_{17-24(p-p)} = 1,05$ V; $V_{15-24(p-p)} = 0,45$ V; $V_{12,13,14-24(p-p)} = 1$ V; unless otherwise specified				
Current consumption	$I_6$	typ.	100	mA
<b>Colour difference inputs</b>				
—(B-Y) input signal (peak-to-peak value)*	$V_{18-24(p-p)}$		1,33	V
—(R-Y) input signal (peak-to-peak value)*	$V_{17-24(p-p)}$		1,05	V
Internal resistance of colour difference sources		<	200	Ω
Input resistance	$R_{17,18-24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18-24}$	typ.	4,2	V
<b>Saturation control</b>				
control voltage range for a change of saturation from -20 dB to + 6 dB	$V_{16-24}$		2,1 to 4	V
control voltage for attenuation > 40 dB	$V_{16-24}$	<	1,8	V
nominal saturation (6 dB below max.)	$V_{16-24}$	typ.	3	V
input current	$I_{16}$	<	20	μA

\* For saturated colour bar with 75% of maximum amplitude.

## CHARACTERISTICS (continued)

## (G-Y) matrix

Matrixed according the equation

$$V_{(G-Y)} = -0,51 V_{(R-Y)} - 0,19 V_{(B-Y)}$$

## Luminance amplifier

Input signal (peak-to-peak)	$V_{15-24(p-p)}$		0,45 V
Input resistance	$R_{15-24}$	typ.	12 k $\Omega$
Internal d.c. voltage	$V_{15-24}$	typ.	2,7 V

## RGB channels

Signal switching input voltage for insertion			
on level	$V_{11-24}$		0,9 to 1,5 V
off level	$V_{11-24}$		-0,5 to +0,3 V
Input current	$I_{11}$		-100 to +200 $\mu$ A
Signal insertion			
external RGB input signal (peak-to-peak value)*	$V_{12,13,14-24(p-p)}$		1 V
internal d.c. voltage due to clamping	$V_{12,13,14-24}$	typ.	3,5 V
input current	$I_{12,13,14}$	<	5 $\mu$ A
Contrast control			
control voltage range for a change of contrast from -17 dB to +3 dB	$V_{19-24}$		2 to 4 V
nominal contrast (3 dB below max.)	$V_{19-24}$	typ.	3,4 V
control voltage for -6 dB	$V_{19-24}$	typ.	2,7 V
input current at $V_{23-24} \geq 6$ V	$I_{19}$	<	2,5 $\mu$ A
Beam current limiting			
internal d.c. voltage	$V_{23-24}$	typ.	6 V
input resistance	$R_{23-24}$	typ.	10 k $\Omega$
input current contrast control			
$V_{23-24} = 5,8$ V	$I_{19}$	typ.	0,7 mA
$V_{23-24} = 5,7$ V	$I_{19}$	typ.	10 mA
$V_{23-24} = 5,6$ V	$I_{19}$	typ.	16 mA
Brightness control			
control voltage range	$V_{20-24}$		1 to 3 V
nominal brightness voltage	$V_{20-24}$		2 V
input current	$I_{20}$	<	10 $\mu$ A
control voltage for nominal black level which equals the inserted artificial black level	$V_{20-24}$	typ.	2 V
change of black level in the control range related to the nominal luminance signal (black-white)		typ.	$\pm 50$ %

\* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200  $\Omega$ .

## Internal signal limiting\*

signal limiting for nominal luminance  
(black to white = 100%)  
black  
white

typ. -25 %  
typ. 125 %

## White point adjustment

A.C. voltage gain \*\*

at  $V_{21,22-24} = 6 \text{ V}$ at  $V_{21,22-24} = 0 \text{ V}$ at  $V_{21,22-24} = 12 \text{ V}$ 

100 %  
< 60 %  
> 140 %

Input resistance

 $R_{21,22-24}$ typ. 20 k $\Omega$ 

## Differential output amplifier

Feedback inputs (pins 2,5,27)  
d.c. voltage during clamping

 $V_{2,5,27-24}$ 

5,79 to 5,95 V

voltage difference between  
the feedback inputs

 $\Delta V$ 

&lt; 80 mV

input resistance

 $R_{2,5,27-24}$ > 100 k $\Omega$ 

Output amplifiers (pins 1,4,26)  
transconductance

$$\frac{\Delta I_1}{\Delta V_{2-24}} = \frac{\Delta I_4}{\Delta V_{5-24}} = \frac{\Delta I_{26}}{\Delta V_{27-24}}$$

typ. 20 mA/V

integrated load resistance

 $R_{1,4,26-24}$ typ. 610  $\Omega$ 

output current (peak value)

at  $V_{1,4,26-24} = 8,2 \text{ V}$  $\pm I_{1,4,26 \text{ m}}$ 

typ. 5 mA

## Gain data

At nominal contrast, saturation and  
white point adjustment

Voltage gain between Y-input (pin 15) and  
feedback inputs (pins 2,5,27)

 $G_{2,5,27-15}$ 

typ. 10 dB

Frequency response (0 to 5 MHz)

 $d_{2,5,27-15}$ 

&lt; 3 dB

Voltage gain between colour difference  
inputs (pins 17 and 18) and feedback  
inputs (pin 5 and 27)

 $G_{5-18} = G_{27-17}$ 

typ. 0 dB

Frequency response (0 to 2 MHz)

 $d_{5-18} = d_{27-17}$ 

&lt; 3 dB

Voltage gain between signal display inputs  
(pins 12,13,14) and feedback inputs  
(pins 2,5,27)

 $G_{2-13} = G_{5-12} = G_{27-14}$ 

typ. 0 dB

Frequency response (0 to 5 MHz)

 $d_{2-13} = d_{5-12} = d_{27-14}$ 

&lt; 3 dB

\* Brightness, contrast and saturation control in nominal position.

\*\* With input pins 21 and 22 not connected an internal bias voltage of 6 V is supplied.

**CHARACTERISTICS** (continued)**Sandcastle detector**

There are 3 internal thresholds (proportional to  $V_p$ )  
the following amplitudes are required for  
separating the various pulses:

horizontal and vertical blanking pulses (note 1)	$V_{10-24}$	>	2 V
		<	3 V
horizontal pulse (note 2)	$V_{10-24}$	>	4 V
		<	5 V
clamping pulse (note 3)	$V_{10-24}$	>	7,5 V
d.c. voltage for artificial black level (note 4) (scan and flyback)	$V_{10-24}$	>	7,5 V
no keying	$V_{10-24}$	<	1 V
Input current	$-I_{10}$	<	100 $\mu A$

**Notes**

1. Blanking to ultra-black ( $-20\%$ ).
2. Insertion of artificial black level.
3. Pulse duration  $> 3,5 \mu s$ .
4. This function will also be obtained by leaving pin 10 open.

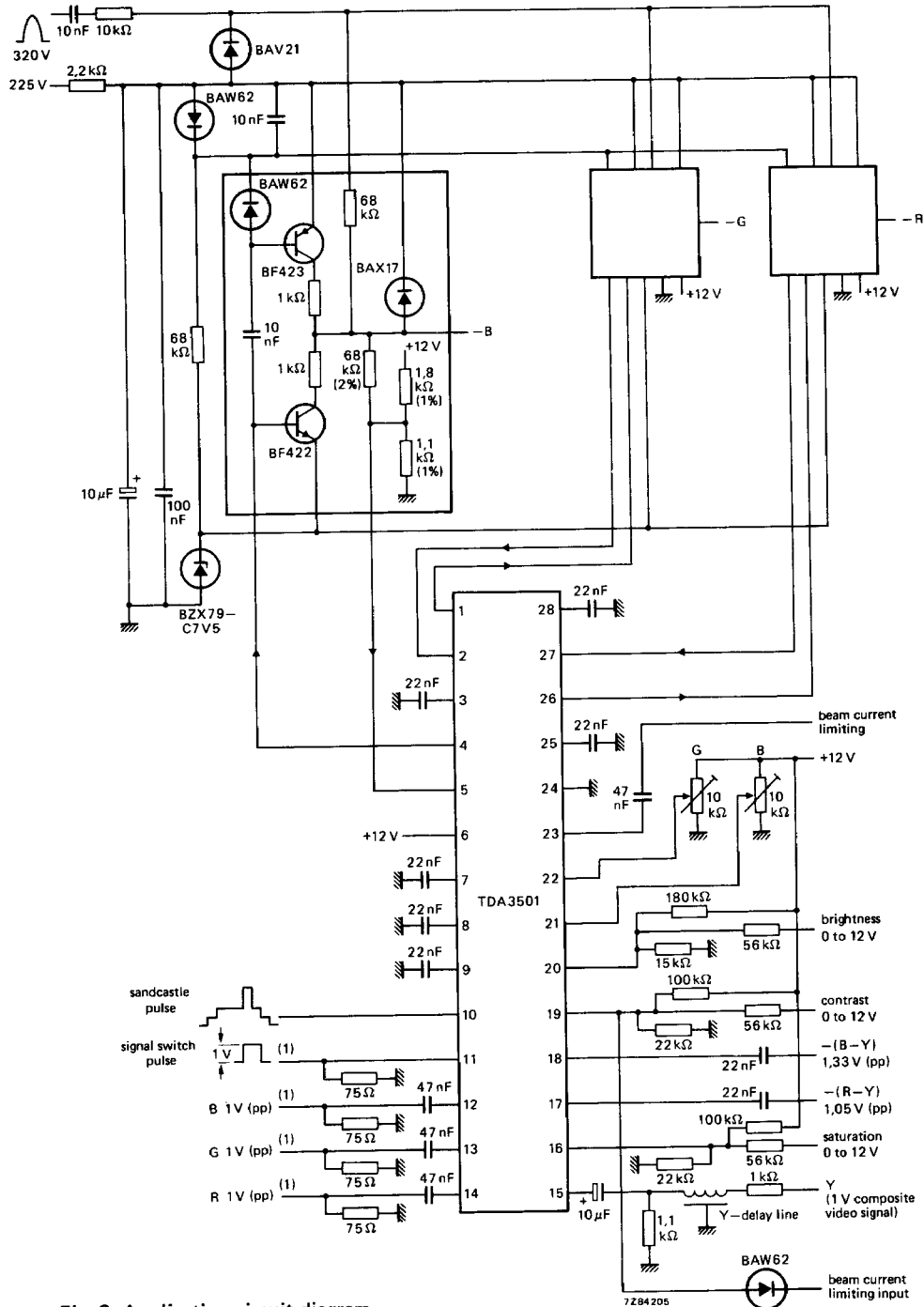


Fig. 2 Application circuit diagram.