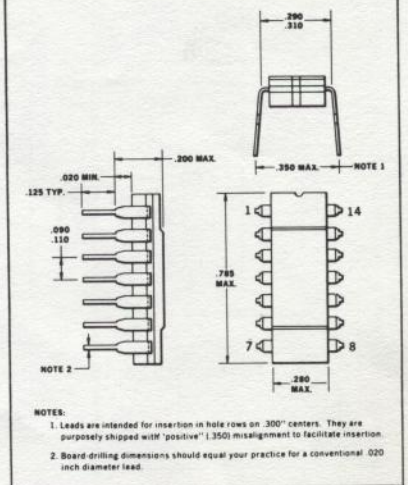
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

INDUSTRIAL MICROCIRCUITS-COMPOSITE DATA SHEET

0°C TO 75°C TEMPERATURE RANGE

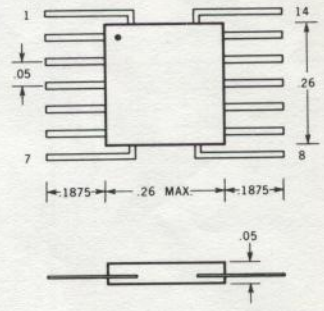
GENERAL DESCRIPTION - Fairchild Diode Transistor Micrologic® (DTμL) Integrated Circuits family uses diode-transistor logic and is designed specifically for integrated circuit technology. The design of these circuits offers distinctly superior performance. Some of the advantages follow:

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

TYPICAL FLAT PACKAGE
TOP VIEW



FEATURES

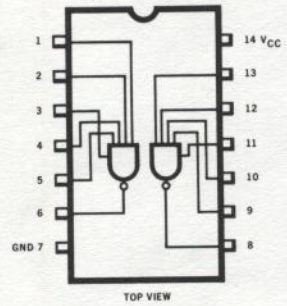
- High performance with a single power supply --- 5.0 V
- High noise immunity --- 1.0 V
- High fan-out capability --- 8-25
- Gates with 6 k or 2 k pull-up resistors for optimum speed
- Fan-out and noise immunity trade-off
- Low power dissipation --- 8.5 mW/Gate
- Gate outputs can be tied together for the "wired OR" function

ORDER INFORMATION

To order Diode Transistor Micrologic elements specify U3I9XXX59X for Flat package and U6A9XXX59X for Dual In-Line package where XXX is 930, 932 etc.

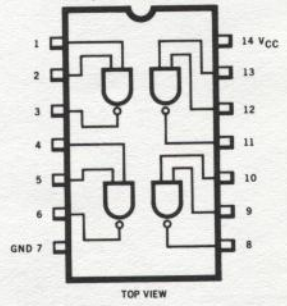
PIN CONFIGURATION: IDENTICAL FOR DUAL-IN-LINE AND FLAT PACKAGES

DTμL 930 / DTμL 961
DTμL 932 / DTμL 944



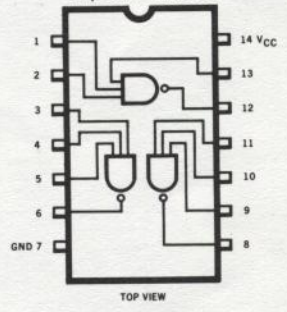
TOP VIEW

DTμL 946 / DTμL 949



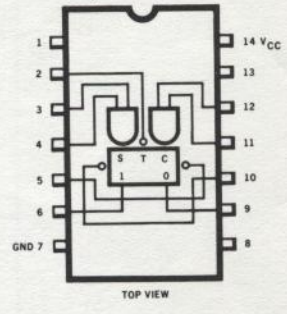
TOP VIEW

DTμL 962 / DTμL 963



TOP VIEW

DTμL 945 / DTμL 948



TOP VIEW

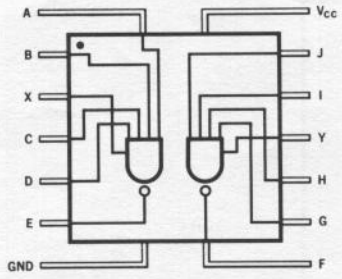
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

DTμL GATES

All DTμL gates are positive logic NAND gates or negative logic NOR gates. A variety of gate combinations is available which provides the system designer the utmost in logic flexibility and reduces package requirements to a minimum. Gate outputs may be paralleled to perform OR (collector) logic. In addition, gates may be cross-connected to form flip-flops, exclusive OR, etc. Gates with 2 kΩ pull-up resistors offer improved propagation delay times.

LOGIC DIAGRAM



POSITIVE (NAND) LOGIC

$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

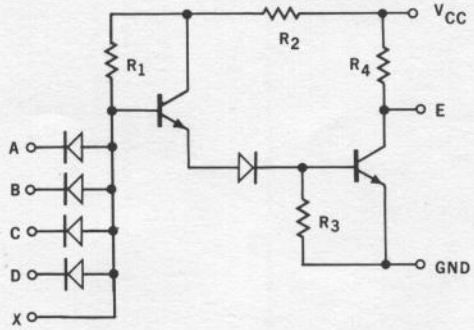
$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

SCHEMATIC DIAGRAM — ONE GATE ONLY

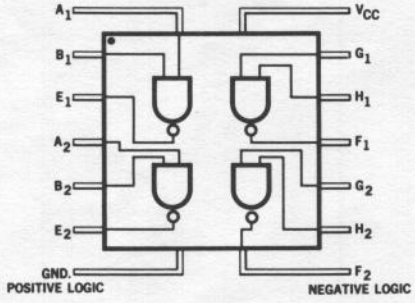
DTμL 930 / DTμL 961

TYPICAL RESISTOR VALUES

R_1 = 2.00k Ω
R_2 = 1.75k Ω
R_3 = 5.00k Ω
R_4 = 6.00k Ω (930)
R_4 = 2.00k Ω (961)



LOGIC DIAGRAM



POSITIVE (NAND) LOGIC

$E = \overline{A \cdot B}$

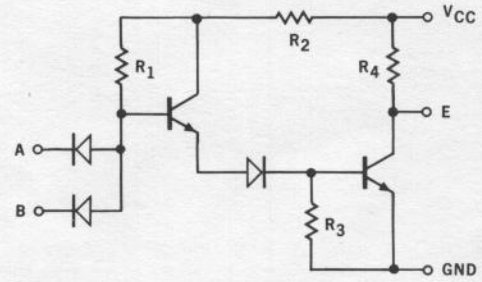
$F = \overline{G \cdot H}$

SCHEMATIC DIAGRAM — ONE GATE ONLY

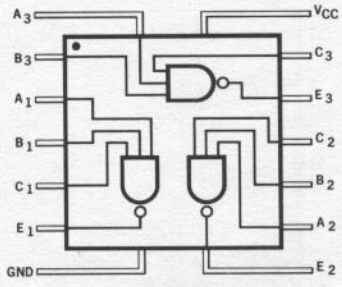
DTμL 946 / DTμL 949

TYPICAL RESISTOR VALUES

R_1 = 2.00kΩ
R_2 = 1.75kΩ
R_3 = 5.00kΩ
R_4 = 6.00kΩ (946)
R_4 = 2.00kΩ (949)



LOGIC DIAGRAM



POSITIVE (NAND) LOGIC

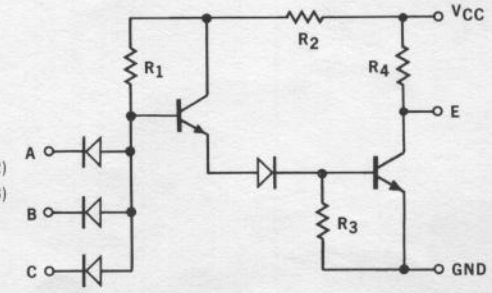
$E = \overline{A \cdot B \cdot C}$

SCHEMATIC DIAGRAM — ONE GATE ONLY

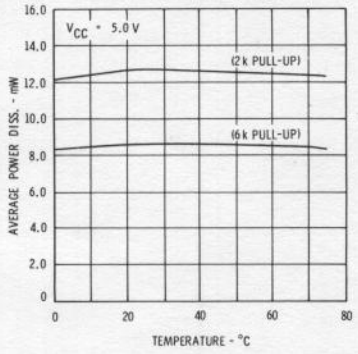
DTμL 962 / DTμL 963

TYPICAL RESISTOR VALUES

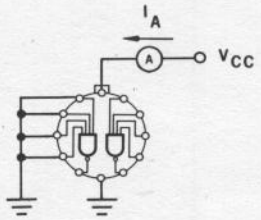
R_1 = 2.00kΩ
R_2 = 1.75kΩ
R_3 = 5.00kΩ
R_4 = 6.00kΩ (962)
R_4 = 2.00kΩ (963)



AVERAGE POWER DISSIPATION VERSUS TEMPERATURE (TYPICAL EACH GATE)

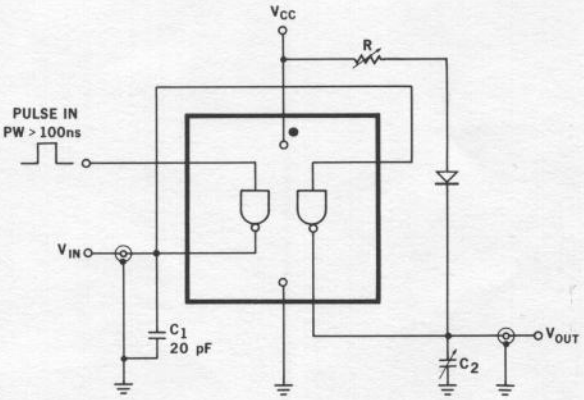


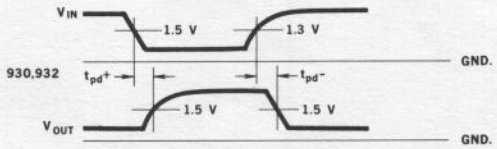
TEST CONDITIONS



$$\text{AV. POWER DRAIN} = \frac{V_{CC}\ I_A}{2}$$

TYPICAL Tpd TEST CIRCUIT DTμL GATES





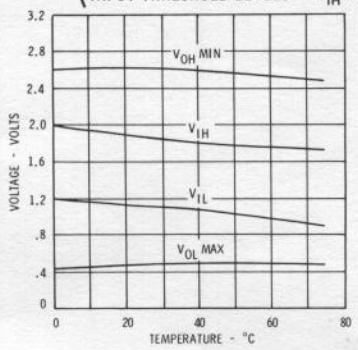
T_{pd} - will be read from input at 1.3 V.

(V_{CC} = 5 V, T = 25°C)

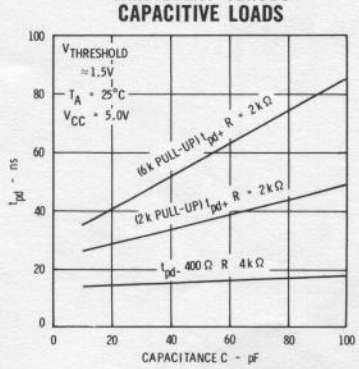
		R	C_2	Min.	Max.
(6 k Pull-up)	t_{pd+}	3.9 kΩ	30 pF	25 ns	80 ns
(6 k & 2 k Pull-up)	t_{pd-}	400 Ω	50 pF	10 ns	30 ns
(2 k Pull-up)	t_{pd+}	3.9 kΩ	30 pF	15 ns	50 ns

OPERATING VOLTAGE CHARACTERISTICS

WORST CASE (OUTPUT LOGIC LEVEL — V_{OH} AND V_{OL} / INPUT THRESHOLD LEVELS — V_{IH} AND V_{IL})



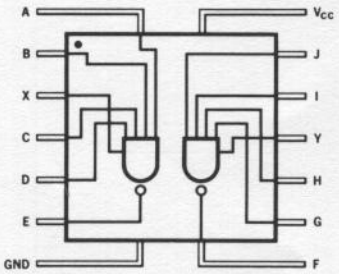
TIME DELAY VERSUS CAPACITIVE LOADS



DTμL 932 BUFFER ELEMENT
DTμL 944 POWER GATE

The DTμL 932 is a dual 4-input inverting driver. It features an emitter-follower pull-up which provides a high fan-out device with superior capacitance-driving capability. The DTμL 944 has an output with no internal pull-up. This provides a high fan-out device whose outputs may be tied together to perform the "wired OR" function. The 944 is useful as an interface driver or as a low-power lamp driver. The fan-in of either element may be extended with the use of the DTμL 933.

LOGIC DIAGRAM

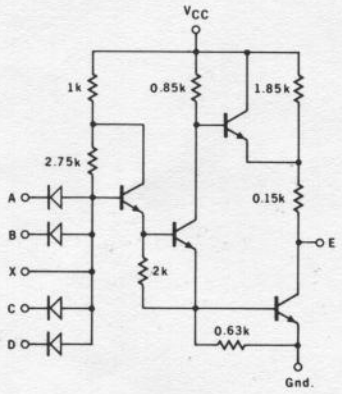


POSITIVE (NAND) LOGIC

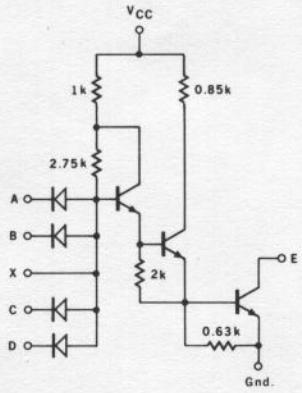
$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

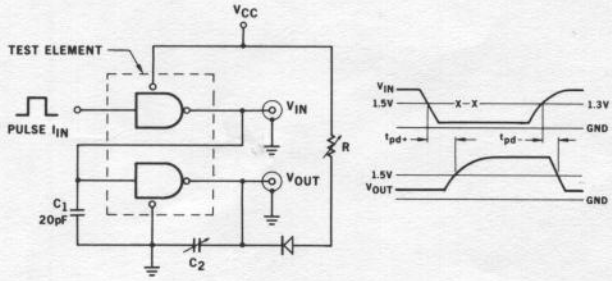
SCHEMATIC DIAGRAM OF THE DTμL 932 ELEMENT (ONE SIDE ONLY)



SCHEMATIC DIAGRAM OF THE DTμL 944 ELEMENT (ONE SIDE ONLY)



tpd TEST CIRCUIT FOR DTμL 932 ELEMENT

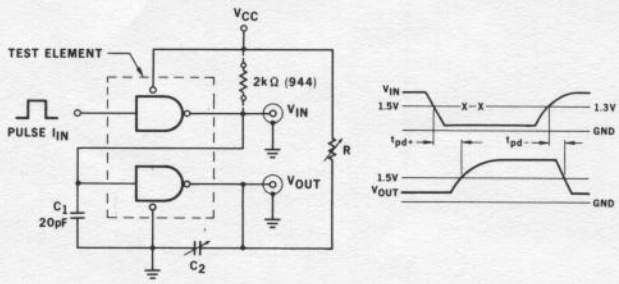


All Diodes are FD600 or Equivalent at 25°C
C_1 and C_2 includes Probe and Jig Capacitance

(V_{CC} = 5.0V, T_A = 25°C)

		R	C	Min.	Max.
t_{pd+}	932	510 Ω	500 pF	25 ns	80 ns
t_{pd-}	932	150 Ω	500 pF	15 ns	40 ns

tpd TEST CIRCUIT FOR DTμL 944 ELEMENT

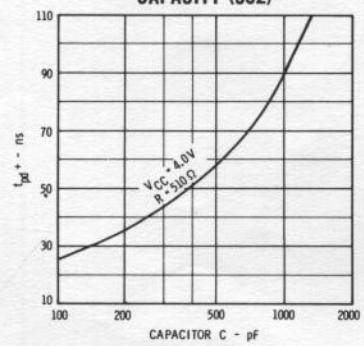


C_1 and C_2 includes Probe and Jig Capacitance

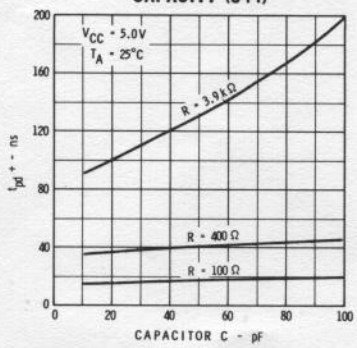
(V_{CC} = 5.0V, T_A = 25°C)

		R	C	Min.	Max.
t_{pd+}	944	510 Ω	20 pF	15 ns	50 ns
t_{pd-}	944	150 Ω	100 pF	10 ns	35 ns

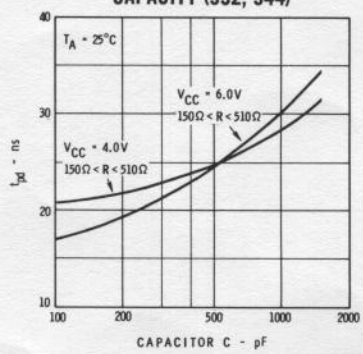
TYPICAL tpd+ VERSUS CAPACITY (932)



TYPICAL tpd+ VERSUS CAPACITY (944)



TYPICAL tpd− VERSUS CAPACITY (932, 944)



9.05 9.05

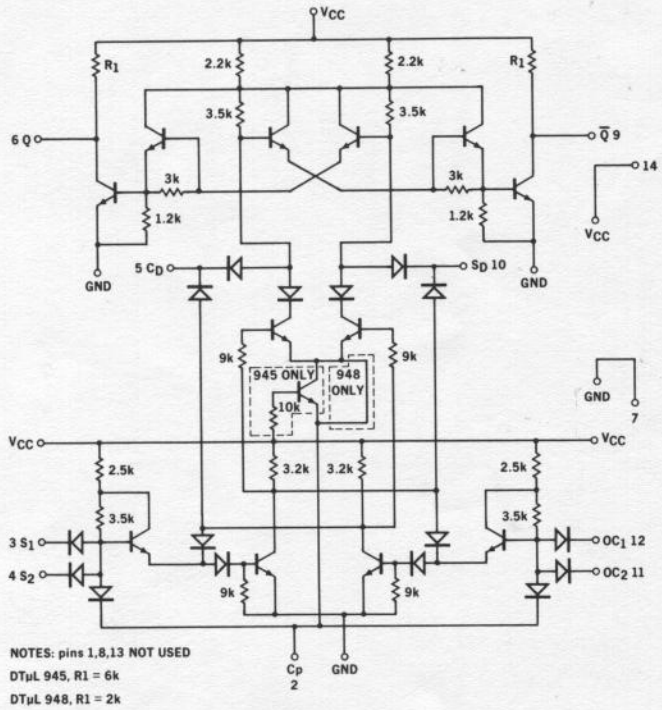
DTμL 945 • DTμL 948 - CLOCKED FLIP - FLOP

The DTμL 945 and DTμL 948 Clocked Flip-Flops are directly-coupled units operating on the "master-slave" principle. Information enters the "master" while the Trigger input voltage is high and transfers to the "slave" when the Trigger input voltage goes low. Since operation depends only on voltage levels, any sort of waveshape having the proper voltage levels may be used as a trigger signal. Rise and fall times are irrelevant.

The DTμL 945 and DTμL 948 have an improved direct Set and Clear design which allows unhampered asynchronous entry irrespective of signals applied to any other inputs. The direct inputs always take precedence, thus simplifying the design of arbitrarily preset ripple-counters and other minimum hardware applications.

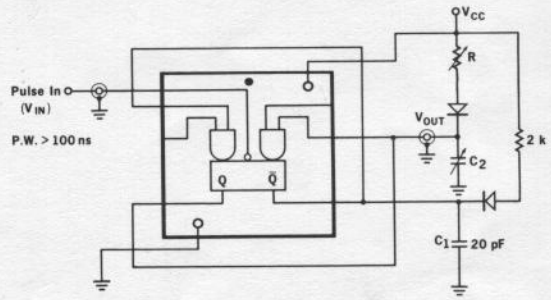
Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise. The DTμL 945 incorporates the standard 6 k-ohm output pull-up resistor, while the DTμL 948 features a 2 k-ohm output pull-up resistor for improved rise times, and matched delay between rising and falling outputs for capacitive loading up to 100 pF.

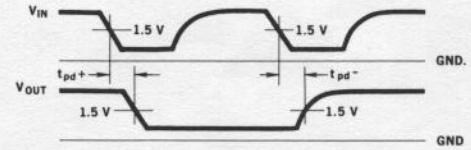
SCHEMATIC DIAGRAM



NOTES: pins 1,8,13 NOT USED
DTμL 945, R1 = 6k
DTμL 948, R1 = 2k

tpd TEST CIRCUIT



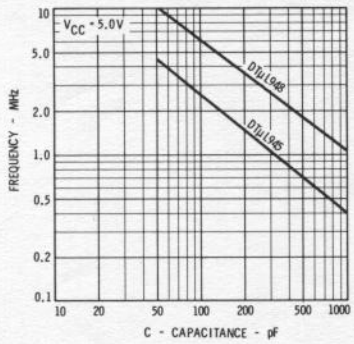


C_1 and C_2 includes Probe and Jig Capacitance

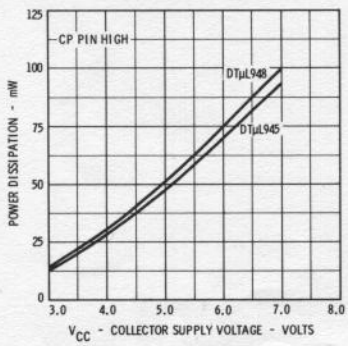
(V_{CC} = 5 V, T = 25°C)

		R	C_2	Min.	Max.
t_{pd+}	945	2.00 k	30 pF	35 ns	75 ns
t_{pd-}	945	330 Ω	30 pF	35 ns	75 ns
t_{pd+}	948	2.00 k	30 pF	20 ns	65 ns
t_{pd-}	948	330 Ω	30 pF	30 ns	75 ns

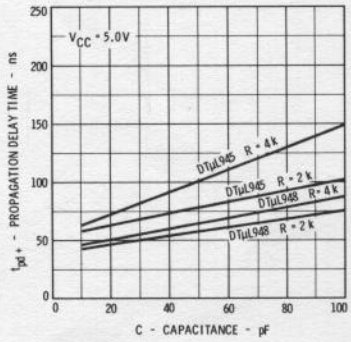
TYPICAL MAXIMUM BINARY COUNTING RATE VERSUS CAPACITY



TYPICAL POWER DISSIPATION VERSUS V_{CC}



TYPICAL tpd VERSUS CAPACITANCE

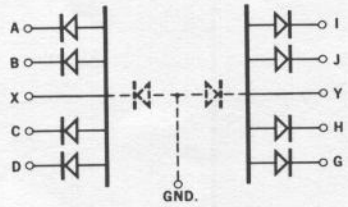


DTμL 933 EXTENDER

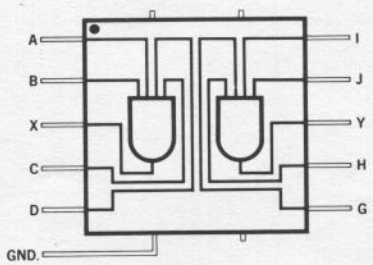
The DTμL 933 is a Dual Input-Extender consisting of two independent diode arrays identical in every respect to the input diodes of the DTμL Gate and Buffer elements. Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance.

Typical input capacitance of DTμL 933 is 2 pF, output capacitance is 5 pF.

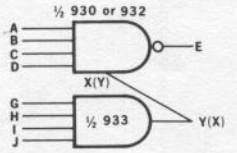
SCHEMATIC DIAGRAM



FLAT PACKAGE LAYOUT



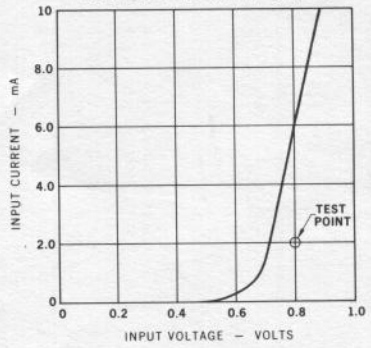
LOGIC EXAMPLE



POSITIVE LOGIC $E = \overline{A\,B\,C\,D\,G\,H\,I\,J}$

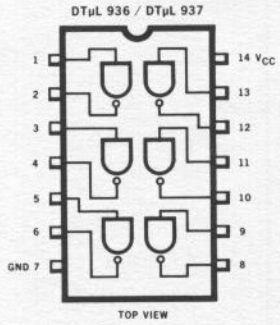
NEGATIVE LOGIC $E = A + B + C + D + G + H + I + J$

FORWARD VOLTAGE VERSUS FORWARD CURRENT +25°C



DTμL 936 • DTuL 937 - HEX INVERTER

The DTμL 936 hex inverter has input-output characteristics identical to the other DTμL gates. Inverters can be cross-connected to form flip-flops or the outputs can be paralleled to perform the "wired OR" function.

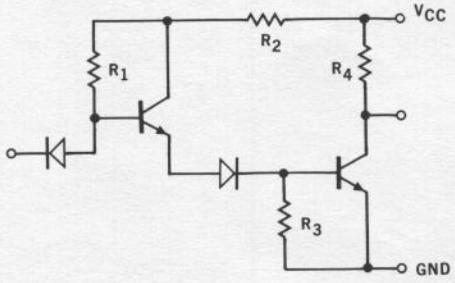


SCHEMATIC DIAGRAM — ONE INVERTER ONLY

DTuL 936 / DTuL 937

TYPICAL RESISTOR VALUES

R_1 = 2.00kΩ
R_2 = 1.75kΩ
R_3 = 5.00kΩ
R_4 = 6.00kΩ (936)
R_4 = 2.00kΩ (937)



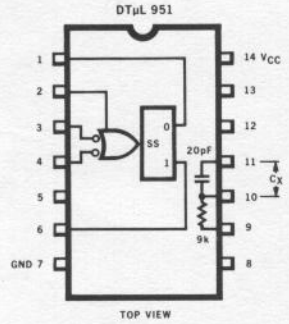
DTμL 951 - MONOSTABLE MULTIVIBRATOR

The DTμL951 is an integrated monostable multivibrator designed for use with other members of the DTμL family. It provides complementary output pulses which are typically 100 ns wide. This pulse width is adjustable by the addition of external components.

ABSOLUTE MAXIMUM RATINGS

(above which useful life may be impaired)

Supply Voltage (V_{CC}), -55°C to +125°C, continuous:	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1 second:	+12 Volts
Output Current, into outputs:	50 mA
Current into Pin 10	5.0 mA
Input Forward Current	-10 mA
Input Reverse Current	1.0 mA

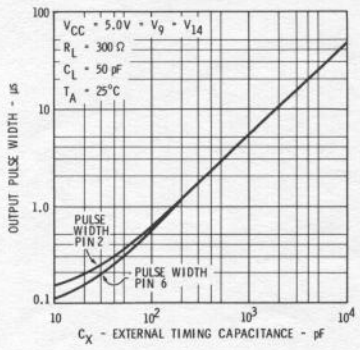


INPUT-OUTPUT LOAD FACTORS TO DTμL FAMILY

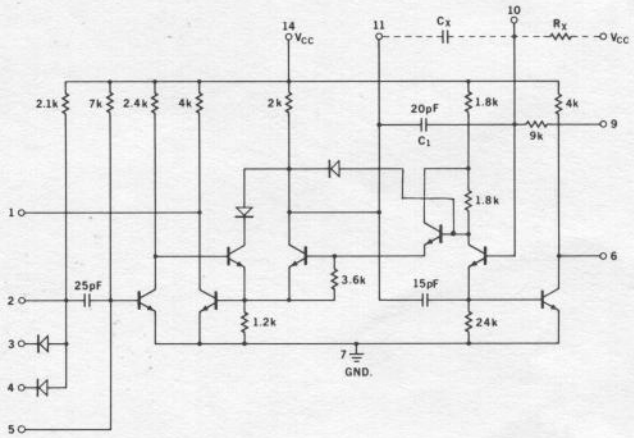
Each DTμL951 input should be rated at 2 loads.

Each DTμL951 output may drive 10 DTμL loads.

OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



SCHEMATIC DIAGRAM



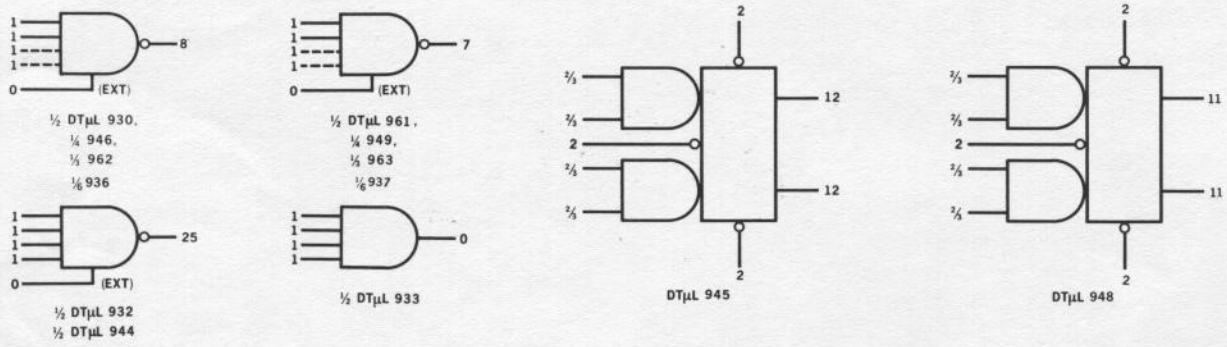
RULES FOR USE OF DTμL 951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_x), the output pulse width is approximately 100 ns.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_x) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_x + 20)$ with C_x in pF and T in ns.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_x) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5\ R_x\ (C_x + 20)$ with R_x in kΩ, C_x in pF and T in ns.
4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2-kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 ns for a 1.0-volt swing. 50 ns for a 2.0-volt swing; 100 ns for a 4.0-volt swing.
6. The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7. The minimum pulse width at output Pin 1 is approximately 100 ns. This pulse width may be decreased to 50 ns by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

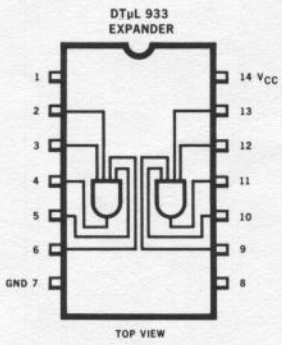
Supply Voltage (V_{CC}), -55°C to +125°C, continuous	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1 second	+12 Volts
Output Current, into outputs	
DTμL 932 & 944	100 mA
DTμL, except 932 & 944	30 mA
Input Forward Current	-10 mA
Input Reverse Current	1.0 mA
Operating Temperature	0°C to +75°C
Storage Temperature	-65°C to +150°C

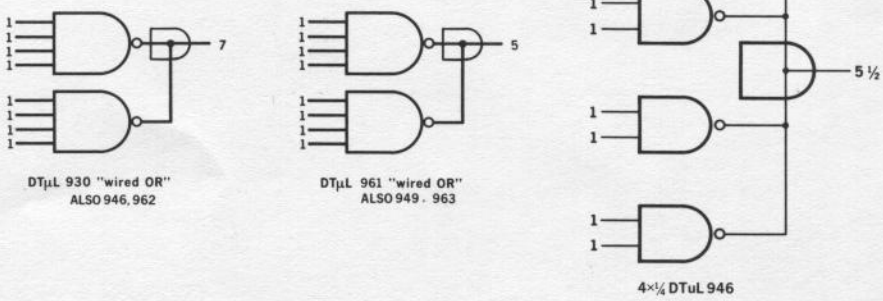
INPUT-OUTPUT LOADING FACTORS

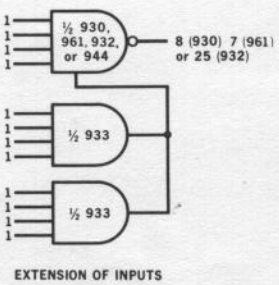


The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability.

RULES FOR INPUT EXPANSION AND "WIRED OR" CONNECTION







RULES

1. Outputs of DTμL gates with 6 kΩ pull-up resistors, 930, 946, and 962 may be tied together for the "wired OR" function. Subtract 1 unit fan-out for each added gate. Subtract 5 fan-outs for 6 added gates.
2. Outputs of DTμL gates with 2 kΩ pull-up resistors, 949, 961, and 963 may be tied together for the "wired OR" function. Subtract 2 units of fan-out for each added gate.
3. Outputs of DTμL 932 may not be tied together for the "wired OR" function.