

July 1993

**CMOS LSI  
PLL FREQUENCY SYNTHESIZER**

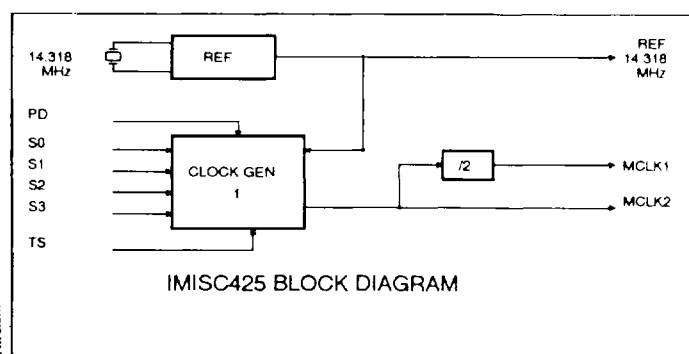
## PRODUCT FEATURES

- Generates CPU Clock Signals for the Motherboards
- 4V to 7V Operating Supply Range
- Supports 80286, 80386 and 80486 Based Designs
- Wide Range of Selectable Output Frequencies Including 80, 66.6, 50, 40, 33.3, 32, 25, 24, 20, 16, and 12 MHz
- 1 NS Maximum Skew Between MCLK1 and MCLK2 CPU Clock Outputs
- Single, Low Cost Crystal (14.318 MHz) Used as Reference Frequency
- Glitch-Free Switching
- 50% Duty Cycle
- Power Down Mode for Low Power Consumption
- TTL or CMOS Compatible Outputs with 12 mA Drive Capability
- Low, Short and Long Term Jitter
- 14 PDIP and 16 Pin SOIC (300 Mil Body) Package Options

## PRODUCT DESCRIPTION

The IMISC425 is a clock chip for Motherboards. The IMISC425 uses a single 14.318 MHz external crystal to generate all essential clock signals. The IMISC425 is designed to generate CPU clock options of 80 MHz, 66.6 MHz, 50 MHz, 40 MHz, 33.3 MHz, 32 MHz, 25 MHz, 24 MHz, 20 MHz, 16 MHz, and 12 MHz, as well as the resultant frequencies from dividing these frequencies by 2, giving flexibility to the user. The user can select the variable frequencies using S0-S3 pins for the CPU clock.

The VCO can be turned off in the standby mode, reducing the current consumption to a few microamperes. In the standby mode, all outputs except 14.318 MHz output are low and both phase detectors are tri-stated.



## APPLICATIONS

IMISC425 eliminates the need for oscillators and generates the CPU clock signals for Personal Computer Motherboards. Supports 8086, 80286, 80386SX, 80386DX and 80486 based designs. IMISC425 can be used with laptop or notebook computers to save power by running the system slower than normal CPU speeds or completely disabling the clocks in standby mode.

**PIN DESCRIPTION**

**X<sub>in</sub>, X<sub>out</sub>** - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.31818 MHz). X<sub>in</sub> may also serve as input for an externally generated reference signal.

**S0, S1, S2, and S3** - Frequency select inputs. These inputs control the MCLK2 frequency selection. All these inputs have internal pull-ups.

Table 1 shows the output frequency selection conditions.

**TS** - Tri-state input pin. When high, all outputs are Tri-States. When low outputs are enabled. This pin has an internal pull-down.

**MCLK2** - Master clock output. Programmable output frequencies can be selected using S0-S3 inputs shown in Table 1.

**MCLK1** - MCLK2 divided by two output.

**REF** - 14.31818 MHz output. Buffered output of on-chip reference oscillator or externally provided reference.

**PD** - This is the phase detector output for the clock generator. It is a single-ended, tri-state output for use

as loop error signal. A 0.1uF capacitor to ground should be connected from this pin to form the loop filter.

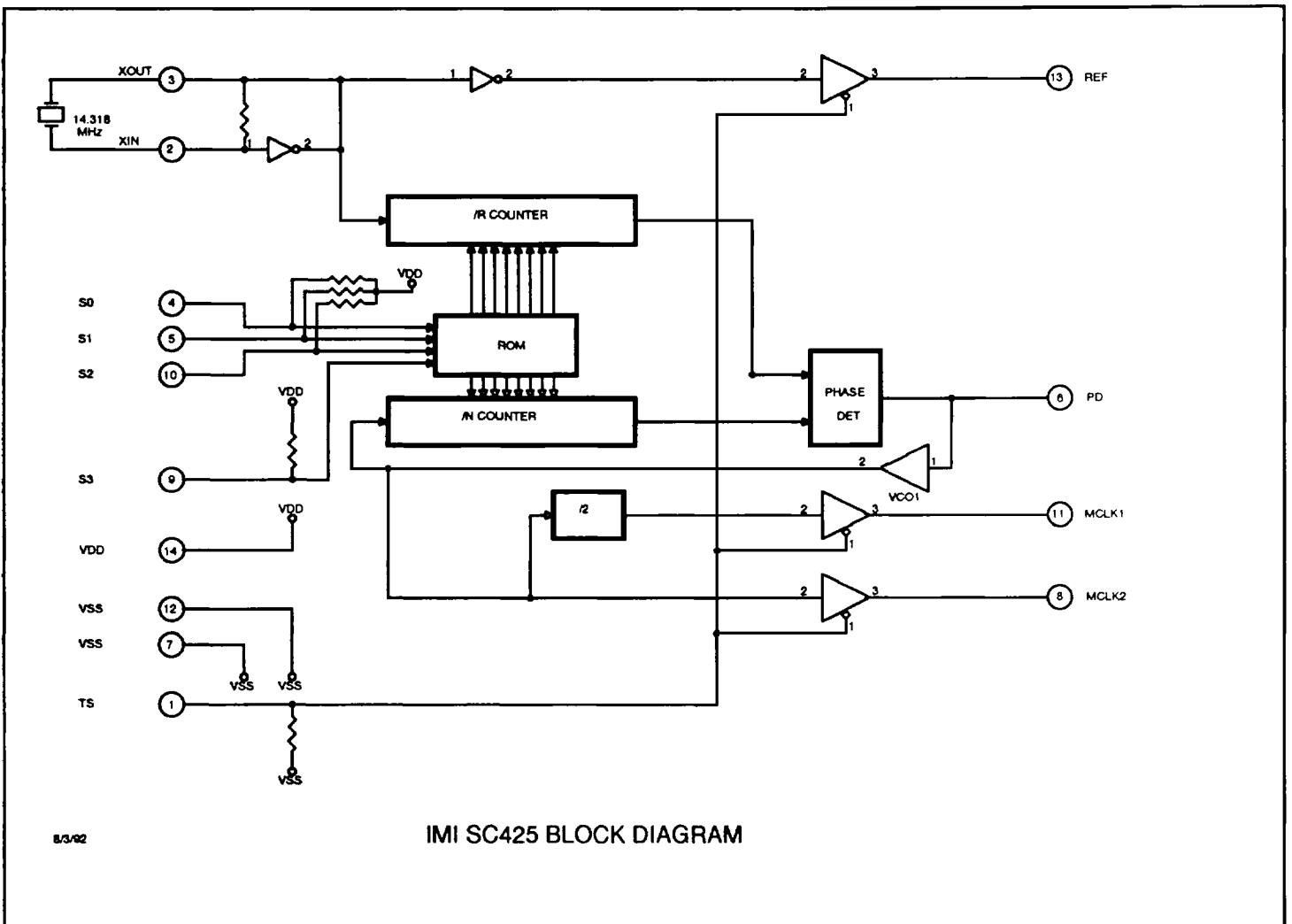
**VSS** - Circuit ground.

**VDD** - Positive power supply.

MCLK2 FREQUENCY SELECTION				
INPUTS			MCLK2 OUTPUT	
S2	S1	S0	S3=1	S3=0
0	0	0	12 MHz	24 MHz
0	0	1	16 MHz	32 MHz
0	1	0	20 MHz	40 MHz
0	1	1	25 MHz	50 MHz
1	0	0	40 MHz	80 MHz
1	0	1	50 MHz	66.6 MHz
1	1	0	33.3 MH	66.6 MHz
1	1	1	Power Down	TEST

**TABLE 1:** When Power Down address is selected, the VCO is turned off and the device goes to standby mode. All outputs except 14.318MHz output are set to low. Phase detector is in tri-state mode.

BLOCK DIAGRAM



## MAXIMUM RATINGS

Voltage Relative to VSS :	-0.3V to 7V
Voltage Relative to VDD :	0.3V
Storage Temperature :	-65°C to +150°C
Ambient Temperature:	-55°C to +125°C
Recommended Operating Range:	4V - 7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Input Low Voltage	$V_{IL}$	-	-	0.8	Vdc
Input High Voltage	$V_{IH}$	2.0	-	-	Vdc
Input Low Current With Pull-up or Pull-down	$I_{IL}$	-	-	5	uA
				$\pm 50$	
Input High Current With Pull-up or Pull-down	$I_{IH}$	-	-	5	uA
				$\pm 50$	
Output Low Voltage $I_{OL} = 12\text{mA}$	$V_{OL}$	-	-	0.4	Vdc
Output High Voltage $I_{OH} = 12\text{mA}$	$V_{OH}$	2.4	-	-	Vdc
Tri-State Leakage Current	$I_{OZ}$	-	-	10	uA
Static Supply Current	$I_{DD}$	-	-	10	uA
Dynamic Supply Current	$I_{CC}$	-	-	35	mA
Short Circuit Current	$I_{SC}$	25	-	-	mA

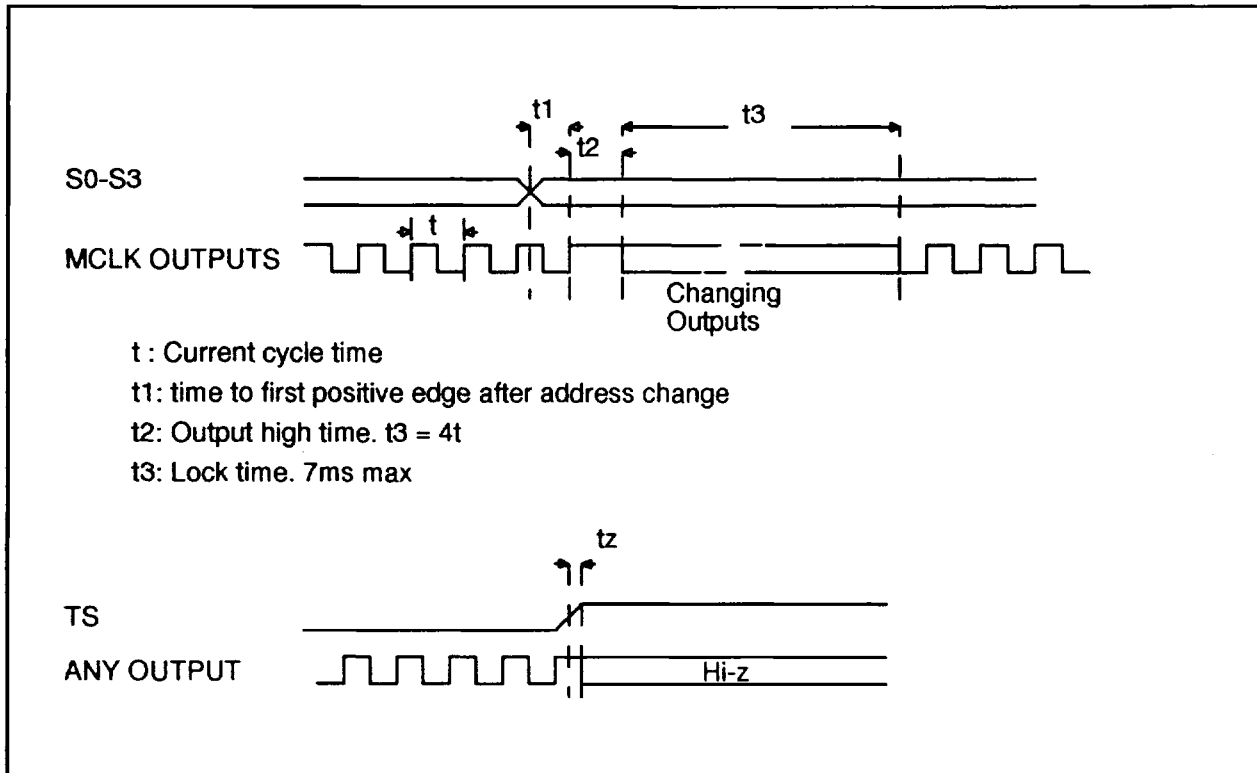
$V_{DD} = 5V \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$

## SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Output Rise (0.8V - 2.0V) and Fall Time (2.0V - 0.8V)	$t_{TLH}$ , $t_{THL}$	-		2	ns
Output Enable TS to All Outputs	$t_z$			35	ns
Duty Cycle All Outputs		45/55	50/50	45/55	%
Jitter One Sigma				300	ps
Input Rise and Fall Times OSCIN	$t_{TLH}$ , $t_{THL}$	-	3	1	us

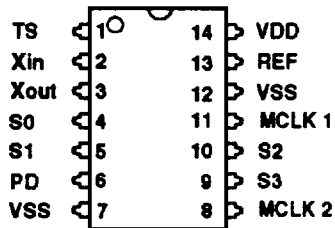
$V_{DD} = 5V \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$

TIMING DIAGRAMS

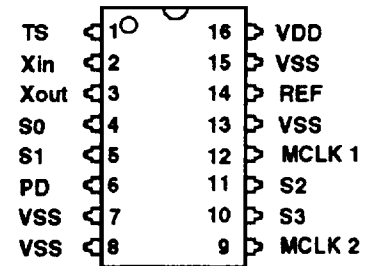


## CONNECTION DIAGRAMS

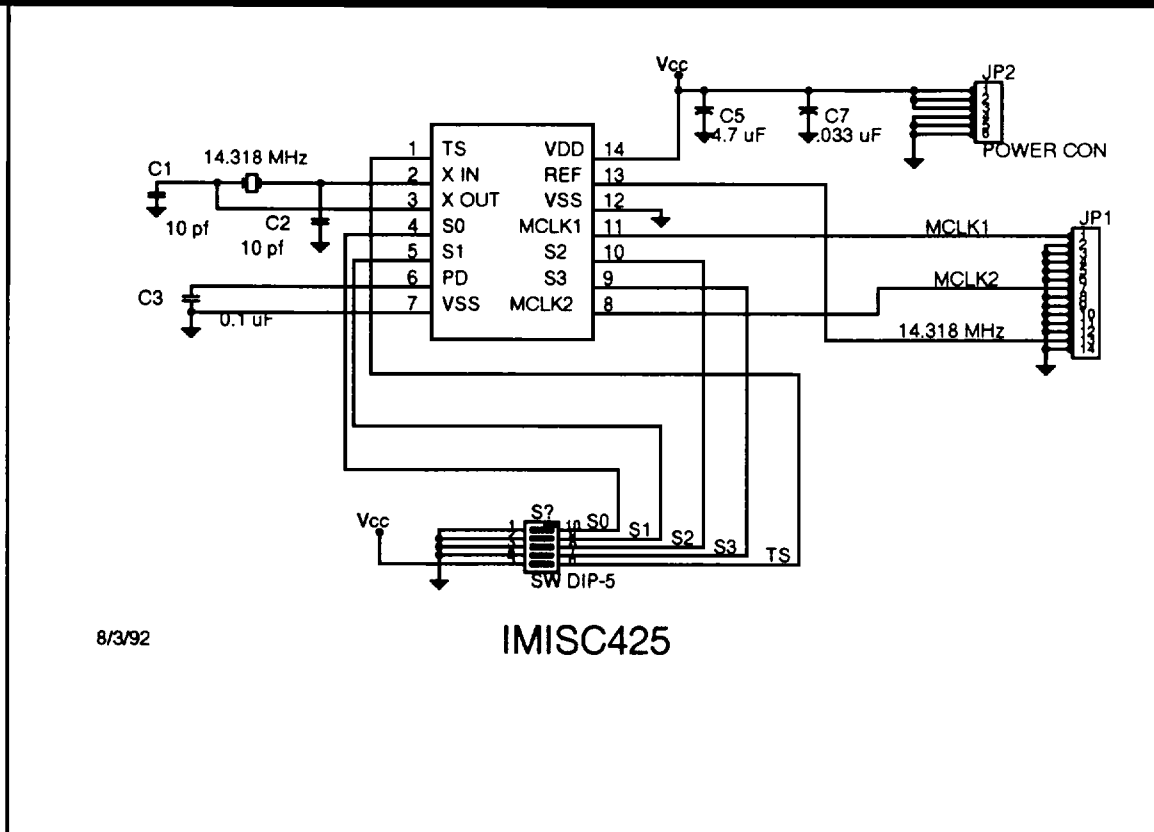
### PLASTIC DIP PACKAGE



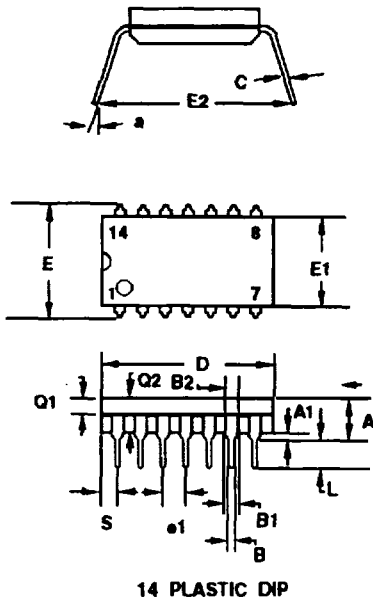
### SOIC PACKAGE



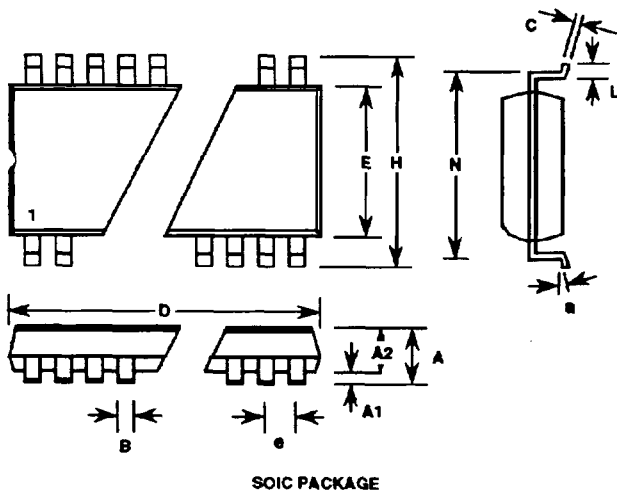
## EXTERNAL CONNECTIONS



PACKAGE DRAWINGS AND DIMENSIONS



14 PIN SKINNY PLASTIC DIP DIMENSIONS						
SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.145	-	0.155	3.68	-	3.93
A1	0.020	-	-	0.050	-	-
B	0.016	0.018	0.020	.040	.045	.050
B1	0.058	0.060	0.062	1.47	1.52	1.57
B2	0.046	0.049	0.052	1.17	1.24	1.32
C	0.008	0.010	0.012	0.20	0.25	0.30
D	0.748	0.750	0.752	19.0	19.05	19.10
E	0.298	-	0.302	7.57	-	7.67
E1	0.248	0.250	0.252	6.30	6.35	6.40
E2	0.335	0.345	0.355	8.51	8.76	9.01
e1	0.100 BSC			2.54 BSC		
L	0.128	0.130	0.132	3.25	3.30	3.35
a	0°	7°	15°	0°	7°	15°
Q1	0.059	0.060	0.061	1.50	1.53	1.55
Q2	0.128	0.130	0.132	3.25	3.30	3.35
S	0.073	0.075	0.077	1.85	1.90	1.95



16 PIN SOIC OUTLINE DIMENSIONS						
SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A1	0.0020	0.009	0.0015	0.060	0.22	0.38
A2	0.090	0.092	0.111	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	.399	.407	.412	10.13	10.34	10.46
E	0.285	0.296	0.299	7.24	7.52	7.59
e	0.050 BSC			1.27 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0°	5°	10°	0°	5°	10°
L	0.024	0.032	0.040	0.61	0.81	1.02

## ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC425xPB	Plastic Dip	Commercial, 0°C to +70°C
IMISC425xB	SOIC	Commercial, 0°C to +70°C

**Note:** The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

**Marking:** Example: IMI  
SC425xPB  
Date Code, Lot #

**IMISC425xPB**

