HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

CHIP CHIP

HC-55516/55532

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION BY DIGITAL CONTROL
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/ SURPRESSION, SPECIAL EFFECTS, ETC.

DESCRIPTION

The HC-55516 and HC-55532 are half duplex modulator/ demodulator CMOS integrated circuits used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

While signals are compatible with other CVSD circuits, internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

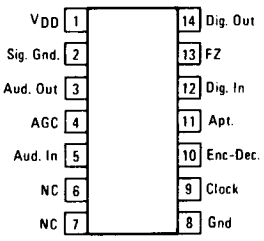
The HC-55516 has internal time constants optimized for 16K bits/sec data rate and is usable down to 9K bits/sec. The HC-55532 is optimized for 32K bits/sec and is usable beyond 64K bits/sec. Both units are available in 14 pin D.I.P. (HC1) in two temperature ranges; -55°C to +125°C (-2 or-8) and -40°C to +85°C (-9).

PINOUT

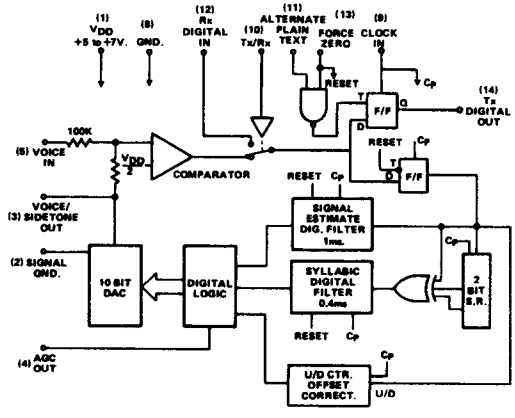
Package Code 4Q

14 PIN D.I.P.

Top View



FUNCTIONAL DIAGRAM



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PIN # 14-LEAD F.P. & D.I.P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	V_{DD}		Positive supply voltage.
2	Sig. Gnd.		Ground connection to D/A ladders and comparator; i.e. audio ground.
3	Aud. Out		Recovered audio out. May be used as side tone at the transmitter. Presents approximately 100 kilohm source. Zero signal reference is $V_{DD}/2$.
4	AGC		A logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of full scale value.
5	Aud. In		Audio input. Should be externally AC coupled. Presents approximately 100 kilohms in series with $V_{DD}/2$.
6,7			No internal connection is made to these pins.
8	Gnd.		Logic ground. Negative supply voltage.
9	Clock		Receiver clock must be phased with digital input such that data must be present at the positive clock transition.
10	Encode (Decode)	Low (High)	A single CVSD can provide half-duplex operation. The encode and decode functions are selected by the logic level applied to this input. A low level selects the encode mode, a high level, the decode mode.
11	APT.	Low	Activating this input causes an "alternate plain text" (quieting pattern) to be transmitted without affecting the internal operation of the CVSD.
12	Dig. In		Input for the received digital data.
13	FZ	Low	Activating this input forces the transmitted output, the internal logic, and the recovered audio output into the "quieting" condition.
14	Dig. Out		Output for transmitted digital data.

*Note: No active input should be left in a "floating condition".

ABSOLUTE MAXIMUM RATINGS

Voltage At Any Pin	-3.0V to V_{DD} +0.3V	Operating Temperature (-9)	-40°C to +85°C
Maximum V_{DD} Voltage	+7.0V	(-2)	-55°C to +125°C
		(-8)	-55°C to +125°C
		Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

Test Conditions V_{DD} = 6.0V, Bit Rate = 16Kb/s, (HC-55516)
Bit Rate = 32Kb/s, (HC-55532)

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Bit Rate		16/32	64	Kb/s	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+5.0		+7.0	V	
Supply Current		1.0		mA	
Digital "1" Input		4.5		V	(2)
Digital "0" Input		1.5		V	(2)
Digital "1" Output		5.5		V	(3)
Digital "0" Output		0.5		V	(3)
Audio Input Voltage		0.5	1.4	Vrms	(4)
Audio Output Voltage		0.5	1.4	Vrms	(5)
Audio Input Impedance		100		KΩ	(6)
Audio Output Impedance		100		KΩ	(7)
Transfer Gain	-0.5		+0.5	dB	(8)
Syllabic Time Constant		4.0		mS	(9)
L.P. Filter Time Constant (55516) (55532)		0.94 0.47		mS mS	(9)
Step Size Ratio (55516) (55532)		24 18		dB dB	(10)
Resolution (55516) (55532)		0.1 0.2		% %	(11)
Min. Step Size (55516) (55532)		0.2 0.4		% %	(12)
Slope Overload		Fig. 1			(13)
Signal/Noise Ratio			Tab. 1		(14)
Quieting Pattern Amplitude (55516) (55532)		12 24		mV P-P mV P-P	(15)
AGC Threshold		0.5		F.S.	(16)
Clamping Threshold		0.75		F.S.	(17)

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1. There is one NRZ (Non-Return Zero) data bit per clock period. Clock must be phased with digital data such that data must be present at the positive clock transition.

2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.

3. Logic outputs are CMOS compatible at supply voltage and withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions.

4. Recommended voice input range for best voice performance.

5. May be used for side-tone in encode mode.

6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.

7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.

8. Unloaded, for linear signals.

9. Note that filter time constants are inversely proportional to clock rate.

10. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.

11. Minimum quantization voltage level expressed as a percentage of supply voltage.

12. The minimum step size between levels is twice the resolution.

13. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels,measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Table II.

14. Table I shows the SNR under various conditions, using the output filter described in 13 (above) at a bit rate of 16Kb/s. See Table II.

15. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.

16. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative).

17. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

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TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV RMS	OUTPUT SNR dB MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

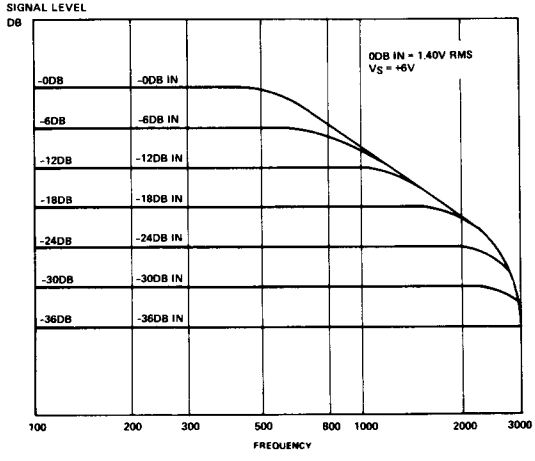

Figure 1 – Transfer Function for CVSD at 16KB

TABLE II

INPUT FILTER FREQUENCY RESPONSE		OUTPUT FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT	FREQUENCY	RELATIVE OUTPUT
100Hz	0±0.5dB	100Hz to 1500Hz	0±1.5dB
200Hz	0±0.1dB	1500Hz to 3000Hz	0±2.5dB
1000Hz	0±0.1dB	3800Hz to 100KHz	Less Than -45dB
3000Hz	-3±0.5dB		
9000Hz	-20±2.0dB		

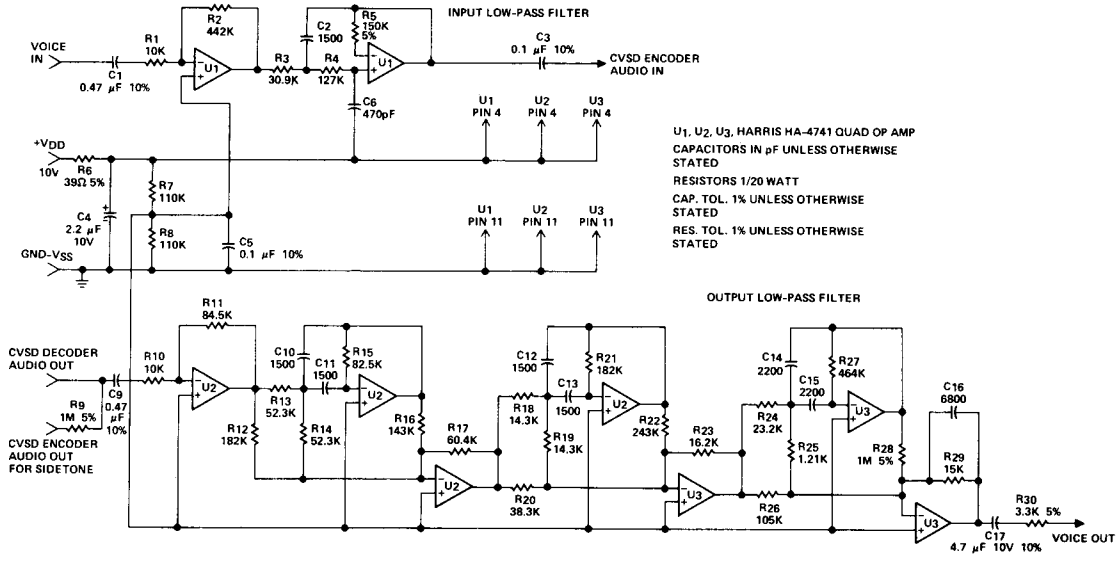

Figure 2 – Suggested Input/Output Audio Filters for SNR Measurement

NOTE: An output filter similar to the input filter section above will generally suffice for good voice intelligibility.