PRELIMINARY

Intel486™ DX2 MICROPROCESSOR

SmartDie™ Product Specification

- **SL-Technology for Energy Efficiency**
  - **—Intel's System Management Mode**
  - **—Stop Clock, Auto HALT and Auto Idle Power Down**
- **Binary-Compatible with Large Software Base**
  - **—MS-DOS*, OS/2*, Windows***
  - **—UNIX* System V/Intel386™**
  - **—iRMX® Software, iRMK Kernels**
- **High Integration Enables On-Chip**
  - **—8 Kbyte Code and Data Cache**
  - **—Floating Point Unit**
  - **—Paged, Virtual Memory Management**
- **Easy to Use**
  - **—Built-In Self Test**
  - **—Hardware Debugging Support**
- **IEEE 1149.1 Boundary Scan Compatibility**
- **High-Performance Design**
  - **—40/50 MHz Core Speed Using 20/25 MHz Bus Clock at 3.3V**
  - **—RISC Integer Core with Frequent Instructions Executing in One Core Clock**
  - **—64/80 Mbyte/sec Burst Bus @40/50 MHz**
  - **—Dynamic Bus Sizing for 8-, 16- and 32-Bit Buses**
  - **—Complete 32-Bit Architecture**
- **Multiprocessor Support**
  - **—Cache Consistency Protocols**
  - **—Support for Second-Level Cache**
- **Intel SmartDie Product**
  - **—Full AC/DC Testing at Die Level**
  - **—0°C–80°C (Junction) Temperature Range**
  - **—40 MHz and 50 MHz Core Speeds @3.3V**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice. Verify with your local Intel Sales Office that you have the latest SmartDie product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Please reference the Standard Package Data Sheet (Order No. 242202) for additional product information and specifications not found in this document.

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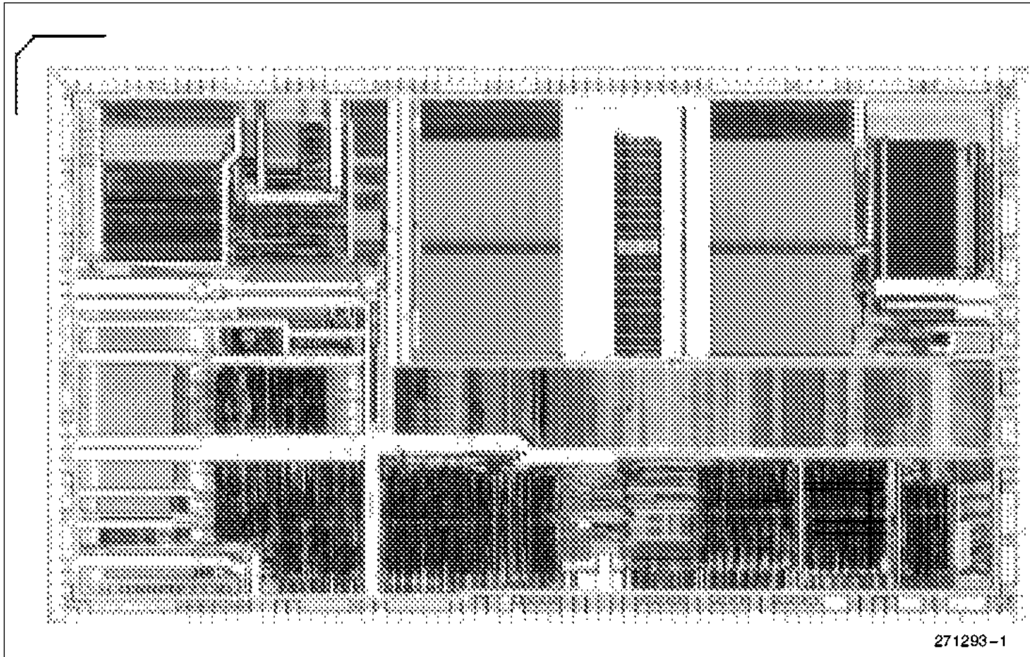
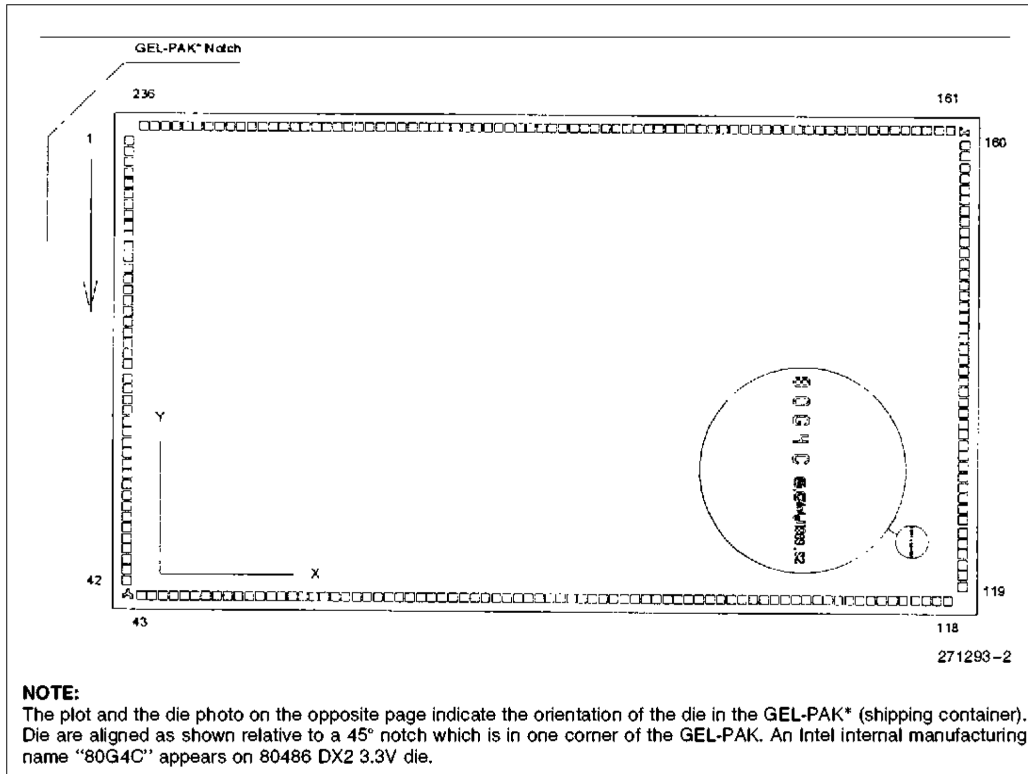
December 1994 Order Number: 271293-002



Intel486™ DX2 Microprocessor Die Photo

1.0 DIE SPECIFICATIONS



NOTE:
The plot and the die photo on the opposite page indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name "80G4C" appears on 80486 DX2 3.3V die.

Figure 1. Intel486™ DX2 Microprocessor Die/Bond Pad Layout

1.1 Pad Description

Table 1. Intel486™ DX2 Microprocessor Bond Pad Center Data

Pad	Signal	Pad Center (Mils = 0.001 in.)		Pad Center (Microns)	
		X	Y	X	Y
001	V_{CC}	−218.6	115.9	−5553	2945
002	V_{SS}	−218.6	110.3	−5553	2802
003	D21	−218.6	104.7	−5553	2660
004	D22	−218.6	99.1	−5553	2517
005	D23	−218.6	93.5	−5553	2375
006	DP3	−218.6	87.9	−5553	2232
007	V_{CC}	−218.6	82.3	−5553	2090
008	V_{SS}	−218.6	76.7	−5553	1947
009	D24	−218.6	71.1	−5553	1805
010	D25	−218.6	65.5	−5553	1662
011	D26	−218.6	59.8	−5553	1520
012	D27	−218.6	54.2	−5553	1377
013	V_{CC}	−218.6	48.6	−5553	1235
014	V_{SS}	−218.6	43.0	−5553	1092
015	V_{CC}	−218.6	37.4	−5553	950
016	V_{SS}	−218.6	31.8	−5553	807
017	V_{CC}	−218.6	26.2	−5553	665
018	V_{SS}	−218.6	20.6	−5553	522
019	D28	−218.6	15.0	−5553	380
020	D29	−218.6	9.4	−5553	237
021	D30	−218.6	3.7	−5553	95
022	D31	−218.6	−1.9	−5553	−47
023	STPCLK#	−218.6	−9.4	−5553	−237
024	IGNNE#	−218.6	−15.0	−5553	−380
025	TDO	−218.6	−20.6	−5553	−522
026	FERR#	−218.6	−26.2	−5553	−665
027	SMI#	−218.6	−31.8	−5553	−807
028	V_{CC}	−218.6	−37.4	−5553	−950
029	V_{SS}	−218.6	−43.0	−5553	−1092
030	V_{CC}	−218.6	−48.6	−5553	−1235
031	V_{SS}	−218.6	−54.2	−5553	−1377
032	V_{CC}	−218.6	−59.8	−5553	−1520
033	V_{SS}	−218.6	−65.5	−5553	−1662
034	SMIACT#	−218.6	−71.1	−5553	−1805
035	SRESET	−218.6	−76.7	−5553	−1947
036	N.C.	−218.6	−82.3	−5553	−2090

Table 1. Intel486™ DX2 Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
037	N.C.	−218.6	−87.9	−5553	−2232
038	N.C.	−218.6	−93.5	−5553	−2375
039	V_{CC}	−218.6	−99.1	−5553	−2517
040	V_{SS}	−218.6	−104.7	−5553	−2660
041	V_{SS}	−218.6	−110.3	−5553	−2802
042	V_{CC}	−218.6	−115.9	−5553	−2945
043	V_{CC}	−210.9	−123.7	−5356	−3142
044	V_{SS}	−205.2	−123.7	−5213	−3142
045	N.C.	−199.6	−123.7	−5071	−3142
046	N.C.	−194.0	−123.7	−4928	−3142
047	N.C.	−188.4	−123.7	−4786	−3142
048	N.C.	−182.8	−123.7	−4643	−3142
049	N.C.	−177.2	−123.7	−4501	−3142
050	N.C.	−171.6	−123.7	−4358	−3142
051	N.C.	−166.0	−123.7	−4216	−3142
052	NMI	−160.4	−123.7	−4073	−3142
053	INTR	−154.7	−123.7	−3931	−3142
054	FLUSH#	−149.1	−123.7	−3788	−3142
055	RESET	−143.5	−123.7	−3646	−3142
056	A20M#	−137.9	−123.7	−3503	−3142
057	EADS#	−132.3	−123.7	−3361	−3142
058	V_{SS}	−126.7	−123.7	−3218	−3142
059	V_{CC}	−121.1	−123.7	−3076	−3142
060	V_{SS}	−115.5	−123.7	−2933	−3142
061	V_{CC}	−109.9	−123.7	−2791	−3142
062	PCD	−104.3	−123.7	−2648	−3142
063	PWT	−98.6	−123.7	−2506	−3142
064	D/C#	−93.0	−123.7	−2363	−3142
065	M/IO#	−87.4	−123.7	−2221	−3142
066	V_{SS}	−81.8	−123.7	−2078	−3142
067	V_{SS}	−76.2	−123.7	−1936	−3142
068	V_{CC}	−70.6	−123.7	−1793	−3142
069	BE3#	−65.0	−123.7	−1651	−3142
070	BE2#	−59.4	−123.7	−1508	−3142
071	BE1#	−53.8	−123.7	−1366	−3142
072	BE0#	−48.2	−123.7	−1223	−3142
073	BREQ	−42.5	−123.7	−1081	−3142
074	V_{SS}	−36.9	−123.7	−938	−3142

Table 1. Intel486™ DX2 Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.)		Pad Center (Microns)	
		X	Y	X	Y
075	V_{CC}	−31.3	−123.7	−796	−3142
076	V_{SS}	−25.7	−123.7	−653	−3142
077	V_{CC}	−20.1	−123.7	−511	−3142
078	W/R#	−14.5	−123.7	−368	−3142
079	HLDA	−8.9	−123.7	−226	−3142
080	CLK	−3.3	−123.7	−83	−3142
081	N.C.	2.3	−123.7	59	−3142
082	V_{CC}	7.9	−123.7	202	−3142
083	V_{SS}	13.6	−123.7	344	−3142
084	V_{CC}	19.2	−123.7	487	−3142
085	V_{SS}	24.8	−123.7	629	−3142
086	V_{CC}	30.4	−123.7	772	−3142
087	V_{SS}	36.0	−123.7	914	−3142
088	V_{CC}	41.6	−123.7	1057	−3142
089	N.C.	47.2	−123.7	1199	−3142
090	TCK	52.8	−123.7	1342	−3142
091	AHOLD	58.4	−123.7	1484	−3142
092	HOLD	64.1	−123.7	1627	−3142
093	V_{SS}	69.7	−123.7	1769	−3142
094	V_{CC}	75.3	−123.7	1912	−3142
095	KEN#	80.9	−123.7	2054	−3142
096	RDY#	86.5	−123.7	2197	−3142
097	N.C.	92.1	−123.7	2339	−3142
098	V_{SS}	97.7	−123.7	2482	−3142
099	V_{CC}	103.3	−123.7	2624	−3142
100	BS8#	108.9	−123.7	2767	−3142
101	BS16#	114.5	−123.7	2909	−3142
102	BOFF#	120.2	−123.7	3052	−3142
103	BRDY#	125.8	−123.7	3194	−3142
104	PCHK#	131.4	−123.7	3337	−3142
105	N.C.	137.0	−123.7	3479	−3142
106	V_{SS}	142.6	−123.7	3622	−3142
107	V_{CC}	148.2	−123.7	3764	−3142
108	V_{SS}	153.8	−123.7	3907	−3142
109	V_{CC}	159.4	−123.7	4049	−3142
110	LOCK#	165.0	−123.7	4192	−3142
111	PLOCK#	170.6	−123.7	4334	−3142
112	V_{SS}	176.3	−123.7	4477	−3142

Table 1. Intel486™ DX2 Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.)		Pad Center (Microns)	
		X	Y	X	Y
113	V_{CC}	181.9	−123.7	4619	−3142
114	BLAST#	187.5	−123.7	4762	−3142
115	ADS#	194.0	−123.7	4928	−3142
116	A2	199.6	−123.7	5071	−3142
117	V_{SS}	205.2	−123.7	5213	−3142
118	V_{CC}	210.9	−123.7	5356	−3142
119	V_{CC}	218.6	−116.2	5553	−2953
120	V_{SS}	218.6	−110.3	5553	−2802
121	A3	218.6	−104.7	5553	−2660
122	A4	218.6	−99.1	5553	−2517
123	A5	218.6	−93.5	5553	−2375
124	UP#	218.6	−87.9	5553	−2232
125	A6	218.6	−81.0	5553	−2057
126	A7	218.6	−75.4	5553	−1914
127	A8	218.6	−69.8	5553	−1772
128	V_{SS}	218.6	−64.1	5553	−1629
129	V_{CC}	218.6	−58.5	5553	−1487
130	V_{SS}	218.6	−52.9	5553	−1344
131	V_{CC}	218.6	−47.3	5553	−1202
132	A9	218.6	−41.7	5553	−1059
133	A10	218.6	−36.1	5553	−917
134	V_{SS}	218.6	−30.5	5553	−774
135	V_{CC}	218.6	−24.9	5553	−632
136	V_{SS}	218.6	−19.3	5553	−489
137	V_{CC}	218.6	−13.7	5553	−347
138	V_{SS}	218.6	−8.0	5553	−204
139	V_{CC}	218.6	−2.4	5553	−62
140	A11	218.6	3.2	5553	81
141	N.C.	218.6	8.8	5553	223
142	A12	218.6	14.4	5553	366
143	V_{SS}	218.6	20.0	5553	508
144	V_{CC}	218.6	25.6	5553	651
145	A13	218.6	31.2	5553	793
146	A14	218.6	36.8	5553	936
147	V_{SS}	218.6	42.5	5553	1078
148	V_{CC}	218.6	48.1	5553	1221
149	A15	218.6	53.7	5553	1363
150	A16	218.6	59.3	5553	1506

Table 1. Intel486™ DX2 Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
151	A17	218.6	64.9	5553	1648
152	V_{SS}	218.6	70.5	5553	1791
153	V_{CC}	218.6	76.1	5553	1933
154	TDI	218.6	81.7	5553	2076
155	TMS	218.6	87.3	5553	2218
156	A18	218.6	92.9	5553	2361
157	A19	218.6	98.6	5553	2503
158	A20	218.6	104.2	5553	2646
159	V_{SS}	218.6	110.3	5553	2802
160	V_{CC}	218.6	115.9	5553	2945
161	V_{CC}	210.9	123.7	5356	3142
162	V_{SS}	204.9	123.7	5206	3142
163	A21	198.7	123.7	5047	3142
164	A22	193.1	123.7	4904	3142
165	A23	187.5	123.7	4762	3142
166	A24	181.9	123.7	4619	3142
167	V_{CC}	176.3	123.7	4477	3142
168	V_{SS}	170.6	123.7	4334	3142
169	A25	165.0	123.7	4192	3142
170	A26	159.4	123.7	4049	3142
171	A27	153.8	123.7	3907	3142
172	A28	148.2	123.7	3764	3142
173	V_{CC}	142.6	123.7	3622	3142
174	V_{SS}	137.0	123.7	3479	3142
175	A29	131.4	123.7	3337	3142
176	A30	125.8	123.7	3194	3142
177	A31	120.2	123.7	3052	3142
178	N.C.	114.5	123.7	2909	3142
179	DP0	108.9	123.7	2767	3142
180	D0	103.3	123.7	2624	3142
181	D1	97.7	123.7	2482	3142
182	D2	92.1	123.7	2339	3142
183	D3	86.5	123.7	2197	3142
184	D4	80.9	123.7	2054	3142
185	V_{CC}	75.3	123.7	1912	3142
186	V_{SS}	69.7	123.7	1769	3142
187	V_{CC}	64.1	123.7	1627	3142
188	V_{SS}	58.4	123.7	1484	3142

Table 1. Intel486™ DX2 Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
189	V_{CC}	52.8	123.7	1342	3142
190	V_{SS}	47.2	123.7	1199	3142
191	V_{SS}	41.6	123.7	1057	3142
192	V_{CC}	36.0	123.7	914	3142
193	V_{SS}	30.4	123.7	772	3142
194	V_{CC}	24.8	123.7	629	3142
195	V_{SS}	19.2	123.7	487	3142
196	V_{CC}	13.6	123.7	344	3142
197	V_{CC}	7.9	123.7	202	3142
198	V_{SS}	2.3	123.7	59	3142
199	D5	−3.3	123.7	−83	3142
200	D6	−8.9	123.7	−226	3142
201	V_{CC}	−14.5	123.7	−368	3142
202	V_{SS}	−20.1	123.7	−511	3142
203	D7	−25.7	123.7	−653	3142
204	DP1	−31.3	123.7	−796	3142
205	D8	−36.9	123.7	−938	3142
206	D9	−42.5	123.7	−1081	3142
207	V_{CC}	−48.2	123.7	−1223	3142
208	V_{SS}	−53.8	123.7	−1366	3142
209	V_{CC}	−59.4	123.7	−1508	3142
210	V_{SS}	−65.0	123.7	−1651	3142
211	V_{SS}	−70.6	123.7	−1793	3142
212	D10	−76.2	123.7	−1936	3142
213	D11	−81.8	123.7	−2078	3142
214	D12	−87.4	123.7	−2221	3142
215	D13	−93.0	123.7	−2363	3142
216	V_{CC}	−98.6	123.7	−2506	3142
217	V_{SS}	−104.3	123.7	−2648	3142
218	V_{CC}	−109.9	123.7	−2791	3142
219	V_{SS}	−115.5	123.7	−2933	3142
220	D14	−121.1	123.7	−3076	3142
221	D15	−126.7	123.7	−3218	3142
222	DP2	−132.3	123.7	−3361	3142
223	D16	−137.9	123.7	−3503	3142
224	V_{CC}	−143.5	123.7	−3646	3142
225	V_{SS}	−149.1	123.7	−3788	3142
226	V_{CC}	−154.7	123.7	−3931	3142

Table 1. Intel486™ DX2 Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.)		Pad Center (Microns)	
		X	Y	X	Y
227	V_{SS}	−160.4	123.7	−4073	3142
228	D17	−166.0	123.7	−4216	3142
229	V_{SS}	−171.6	123.7	−4358	3142
230	V_{CC}	−177.2	123.7	−4501	3142
231	V_{SS}	−182.8	123.7	−4643	3142
232	D18	−188.4	123.7	−4786	3142
233	D19	−194.0	123.7	−4928	3142
234	D20	−199.6	123.7	−5071	3142
235	V_{SS}	−205.2	123.7	−5213	3142
236	V_{CC}	−210.9	123.7	−5356	3142

Notes:

1. N.C. signifies no connect. These pads must not be connected.
2. The symbol "#" is used at the end of the signal name to denote an active low signal.
3. X-Y pad coordinates represent bond pad centers and are relative to the center of the die.

Boundary Scan (JTAG) is implemented through the following pads: 155 (TMS), 154 (TDI), 90 (TCK), 25 (TDO).

2.0 INTEL DIE PRODUCTS PROCESSING

TEST PROCEDURE

Intel has instituted full-speed functional testing at the die level for all SmartDie™ products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

WAFER PROBE

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

WAFER SAW

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

DIE INSPECTION

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

PACKING PROCEDURE

Intel will ship all Intel die products in GEL-PAKs*. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Spec
- Customer Part Number (if applicable)
- Fab Lot Number
- Quantity
- Assembly Lot Traveler Number
- Seal Date
- ROM Code (if applicable)

NOTE:
GEL-PAKs require a Vacuum Release Station. Contact Vichem Corporation for more information.

INSPECTION STEPS

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

STORAGE REQUIREMENTS

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

ESD

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Substrate Bias Condition: V_{SS}

Post-Saw Die Dimensions:
Mils: X = 451 ± 0.5 , Y = 261 ± 0.5
See associated Die/Bond Pad Layout for X, Y orientation.

Die Backside Material: (outer most layer first)
1500 (±) 500 Angstroms Gold, 200 (±) 100 Angstroms Chrome

Pad Passivation Opening Size:
Mils: 4.6 x 4.6 (single pads),
Microns: 118 x 118 (single pads)

Die Thickness: 17 ± 1 mils

Minimum Pad Pitch:
Pads may not be evenly pitched. Minimum pitch is 142.5 microns (5.6 mils).

Bond Pad Metalization (outermost layer first)
1-Micron Aluminum (0.5% Copper), 0.1 Microns Titanium

Die Revision: aC-0

Pads per Die: 236

Intel Fabrication Process: CHMOS V (min. feature size 0.8 microns)

Passivation: (outermost layer first)
5 Microns Polyimide, 0.6 Microns Nitride

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature .... 0°C to +70°C
Junction Temperature under Bias .... −65°C to +110°C
Supply Voltage with Respect to V_{SS} ...... −0.5V to +6.5V
Voltage on Other Pads .... −0.5V to V_{CC} +0.5V

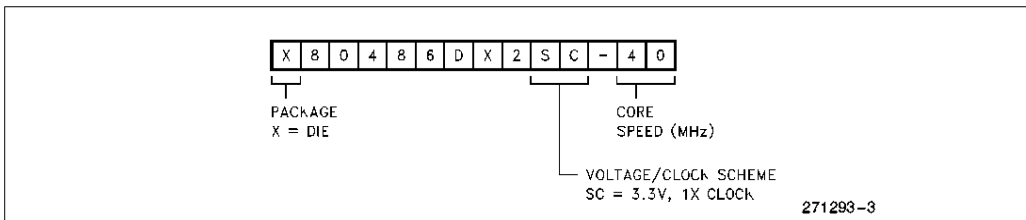
OPERATING CONDITIONS*

Digital Supply Voltage (V_{CC}) .... 3.3V ± 0.3V
Junction Temperature under Bias (T_J) .... 0°C to 80°C
Core Operating Frequency .... 40/50 MHz

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest SmartDie Product Specification before finalizing a design.

****WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



5.0 REFERENCE INFORMATION

Title	Order No.
Intel486™ Microprocessor Data Sheet	241245
SL Enhanced Intel486 Microprocessor Data Sheet Addendum	241696
Intel486 Microprocessor Family Programmer's Reference Manual	240486
Intel486 Microprocessor Hardware Reference Manual	240552

6.0 REVISION HISTORY

Rev	Date	Description
001	6/94	Initial Release
002	10/94	50 MHz Speed Added