DATA SHEET

MOS INTEGRATED CIRCUIT
μPD9318

CCD SENSOR CLOCK SIGNAL GENERATOR/DRIVER CIRCUIT

DESCRIPTION

The μPD9318 IC is used exclusively for CCD which incorporates into one package the clock generator circuit for CCD linear sensors μPD3571D, μPD3573D, μPD3574D, and μPD3575D and the interface circuit between the area sensor and the horizontal driver clock generator circuit.

It enables the select terminals to select the clock signal and driver circuit optimum for linear and area sensors to drive the CCD sensor.

This device is a 44-pin plastic QFP (Quard flat package) optimum for high-density mounting.

FEATURES

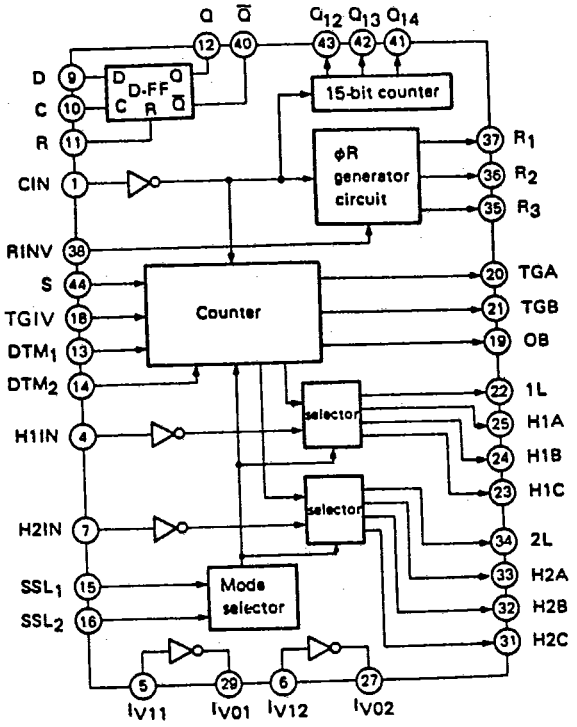
- Mode selector terminals 1 and 2 allow selection of μPD3571D, μPD3573D, μPD3574D, and μPD3575D.
- Linear sensor
  - Generates the shift register clock, reset clock, φTG, and φOB
  - Optimum for making the clock generator circuit compact and simple.
  - Enables setting the polarity of φTG or φOB with the polarity setting terminal.
  - Enables setting the φTG pulse width in four stages
- Area sensor
  - Optimum for making the driver circuit compact
  - Enables direct connection as the drive interface between area CCD sensor and the horizontal driver clock generator circuit.
  - Enables driving three CCDs simultaneously.
- Enables the 15-bit counter to divide the frequency of φM into three stages and output them.
- Incorporates the D-FF circuit.

ORDERING INFORMATION

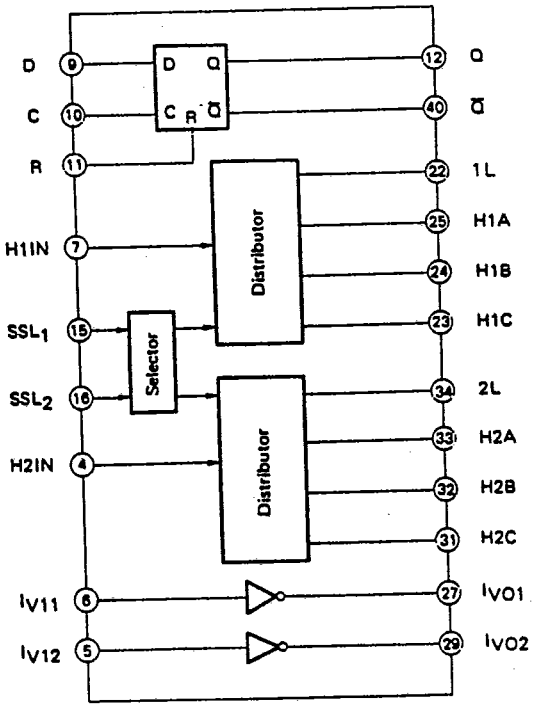
Part Number	Package
μPD9318GB	44 pin plastic QFP (□ 10)

BLOCK DIAGRAM

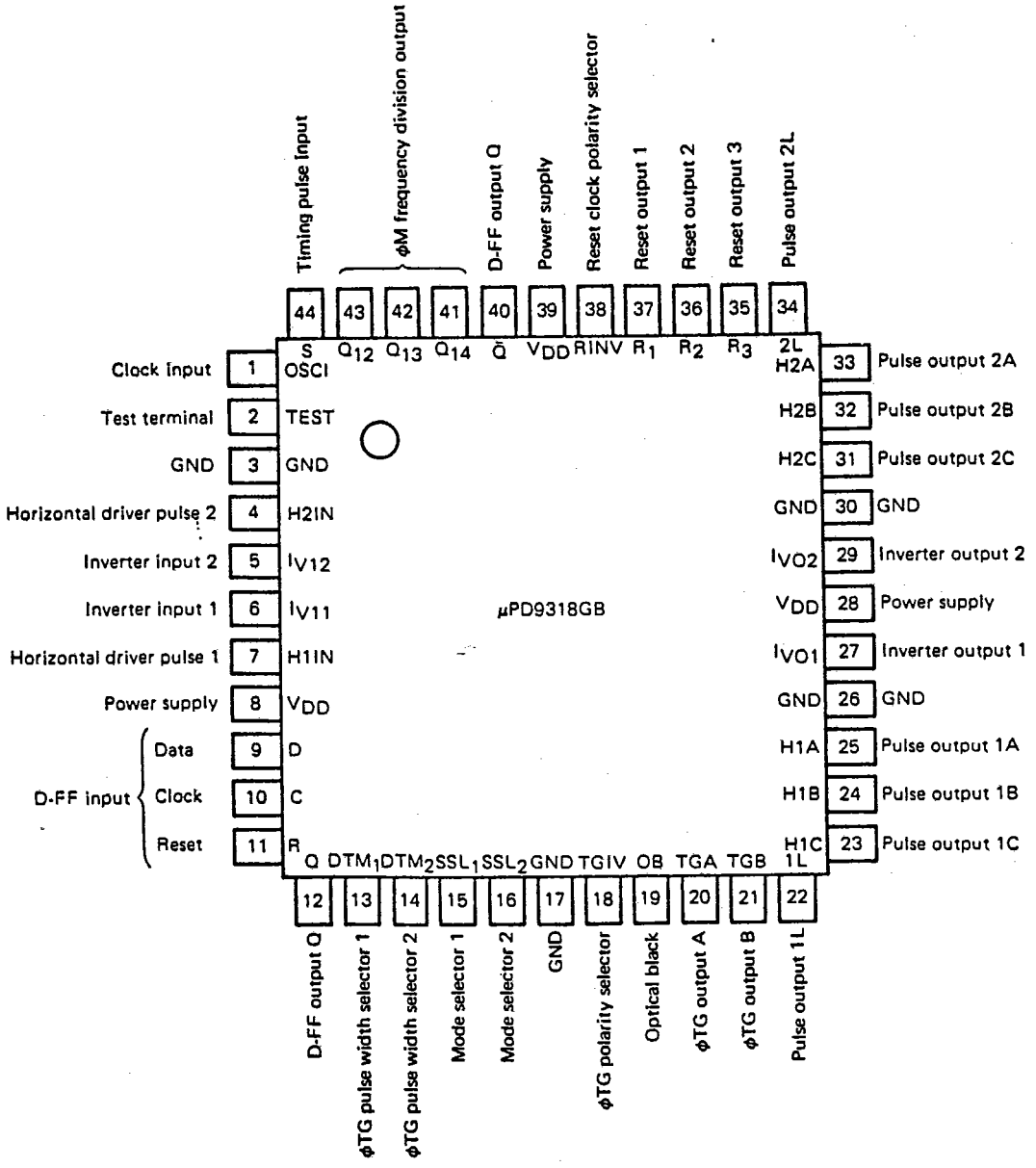
Linear sensor



Area sensor



PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply voltage	V_{DD}	−0.5 to + 7.0	V
Input voltage	V_I	−0.5 to V_{DD} + 0.5	V
Output current	V_O	40	mA
Operating temperature	T_{opt}	−10 to + 55	°C
Storage temperature	T_{stg}	−65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS (−40 to +85 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	4.5	5	5.5	V
Input voltage	V_I	0		V_{DD}	V
Low-level input voltage	V_{IL}	0		0.3 V_{DD}	V
High-level input voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V
Input rise time	t_r	0		10	μs
Input fall time	t_f	0		10	μs

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10 %, T_a = −40 to +55 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITION
Static current consumption	I_L		0.1	200	μA	V_I = V_{DD} or GND
Input current	I_I		10^{-5}	10	μA	V_I = V_{DD} or GND
Low-level output current	I_{OL}	4 12 8	11		mA mA mA	V_{OL} = 0.4 V Note 1 Note 2 Note 3
High-level output current	I_{OH}	4 12 8	8		mA mA mA	V_{OH} = V_{DD} −0.4V Note 1 Note 2 Note 3
Low-level output voltage	V_{OL}			0.1	V	I = 0 mA
High-level output voltage	V_{OH}	V_{DD} −0.1			V	I = 0 mA
Input terminal capacity	C_{IN}			10	pF	V_{DD} = 0, f = 1 MHz
Output terminal capacity	C_{out}			30	pF	V_{DD} = 0, f = 1 MHz
Output rise time	t_r		2.1		ns	C_L = 15 pF
Output fall time	t_f		2.1		ns	C_L = 15 pF
Maximum driver frequency	f_{max}			15	MHz	

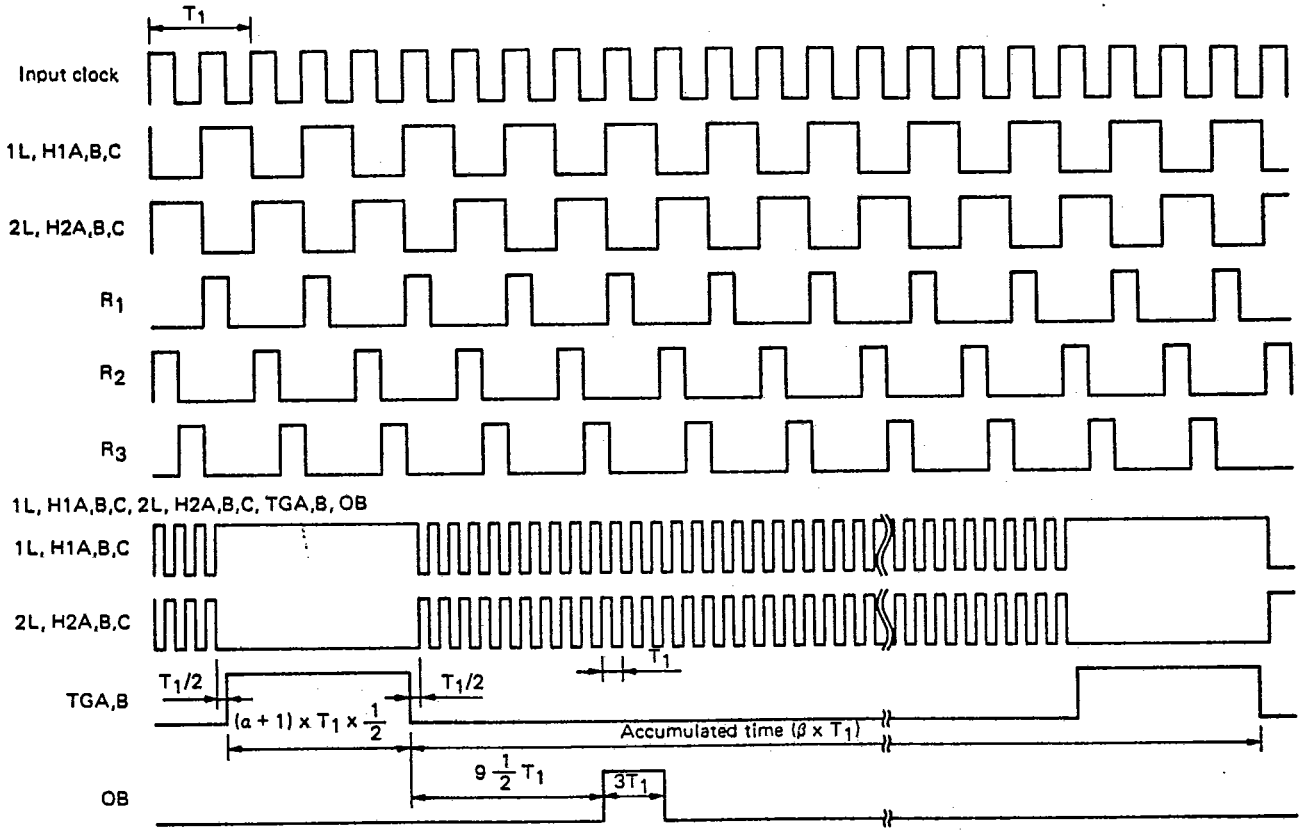
Note 1: Pins 2, 12, 19, 40, 42, and 43
Note 2: Pins 23, 24, 25, 27, 29, 31, 32, and 33
Note 3: Pins 20, 21, 22, and 34

μPD9318 PIN DESCRIPTION

PIN No.	SYMBOL	PIN NAME	PIN DESCRIPTION
1	OSCI	Clock input	Input the clock. This input clock allows the output shown in the timing chart to be obtained.
2	TEST	Test terminal	Do not connect this terminal, leave it open because this is the test terminal.
3	GND	Ground terminal	Connect this terminal to ground.
4	H2IN	Horizontal driver pulse 2	Connect this terminal to the clock generator for area sensor. When not using this terminal, tie it high or low.
5	I_{V12}	Inverter input 2	Connect this terminal to the clock generator for area sensor. When not using this terminal, tie it high or low.
6	I_{V11}	Inverter input 1	Connect this terminal to the clock generator for area sensor. When not using this terminal, tie it high or low.
7	H1IN	Horizontal driver pulse 1	Connect this terminal to the clock generator for area sensor. When not using this terminal, tie it high or low.
8	V_{DD}	Power supply terminal	Input 5 V
9	D	D-FF data input	When not using this terminal to input the D-FF clock, tie it high or low.
10	C	D-FF clock input	When not using this terminal to input the D-FF clock, tie it high or low.
11	R	D-FF reset input	When not using this terminal to input the D-FF clock, tie it high or low.
12	Q	D-FF Q output	This is the Q output terminal of D-FF.
13	DTM_1	φTG pulse width selector 1	This is the terminal to set the pulse width of φTG with the DTM1 and DTM2 terminals.
14	DTM_2	φTG pulse width selector 2	DTM_1 / DTM_2: Low/Low, Low/High, High/Low, High/High → α: 2, 4, 8, 16 Pulse width T_2 of φTG is determined by the following expression: μPD3571D $T_2 = (\alpha + 1) \times T_1 \times \frac{1}{2}$ μPD3573D, μPD3574D, μPD3575D $T_2 = (\alpha + 0.5) \times T_1$ T_1 is one cycle of the CCD driver clock.
15	SSL_1	Mode selector 1	Setting of SSL1/SSL2 allows setting of CCD exclusively used for the mode.
16	SSL_2	Mode selector 2	SSL_1 / SSL_2 / Corresponding device: Low / High / μPD3571D High / Low / μPD3573D High / Low / μPD3574D High / High / μPD3575D Low / Low / Area sensor
17	GND	Ground	Ground terminal

PIN No.	SYMBOL	PIN NAME	PIN DESCRIPTION
18	TGIV	ϕTG polarity selector	When this terminal is high, the ϕTG output terminal outputs a positive-going pulse; when low, it outputs a negative-going pulse.
19	OB	Optical black	This terminal outputs the timing pulse which times the output of the optical black pulse from CCD.
20	TGA	ϕTG output A	TGA and TGB output the same TG pulse.
21	TGB	ϕTG output B	
22	1L	Clock output 1L	H1A, H1B, H1C, and 1L output the same clock pulse for the driver (see the timing chart).
23	H1C	Clock output 1C	
24	H1B	Clock output 1B	
25	H1A	Clock output 1A	
26	GND	Ground	Ground terminal
27	I_{VO1}	Inverter output 1	Inverted output of the pulse input to pin 6.
28	V_{DD}	Power supply terminal	Input 5 V.
29	I_{VO2}	Inverter output 2	Inverter output of the pulse input to pin 4.
30	GND	Ground	Ground terminal
31	2L	Clock output 2L	H2A, H2B, H2C, and 2L output the same clock pulse for the driver (see the timing chart).
32	H2C	Clock output 2C	
33	H2B	Clock output 2B	
34	H2A	Clock output 2A	
35	R_3	Reset output R3	Each of the reset pulses shown in the timing chart is output with its own timing (see the timing chart).
36	R_2	Reset output R2	
37	R_1	Reset output R1	
38	RINV	Reset polarity selector	When this terminal is high, the reset output terminal outputs a positive-going pulse; when low, it outputs a negative-going pulse.
39	V_{DD}	Power supply terminal	Input 5 V.
40	$\overline{Q}$	D-FF $\overline{Q}$ output	D-FF $\overline{Q}$ output terminal
41	Q_{14}	ϕM frequency division output	These terminals output the frequency-divided signals of the clock input to pin 1 (OSCI). Q_{12} 1/8192 Q_{13} 1/16384 Q_{14} 1/32768
42	Q_{13}		
43	Q_{12}		
44	S	Accumulated time input	One cycle of the pulse input to this terminal becomes the CCD accumulated time.

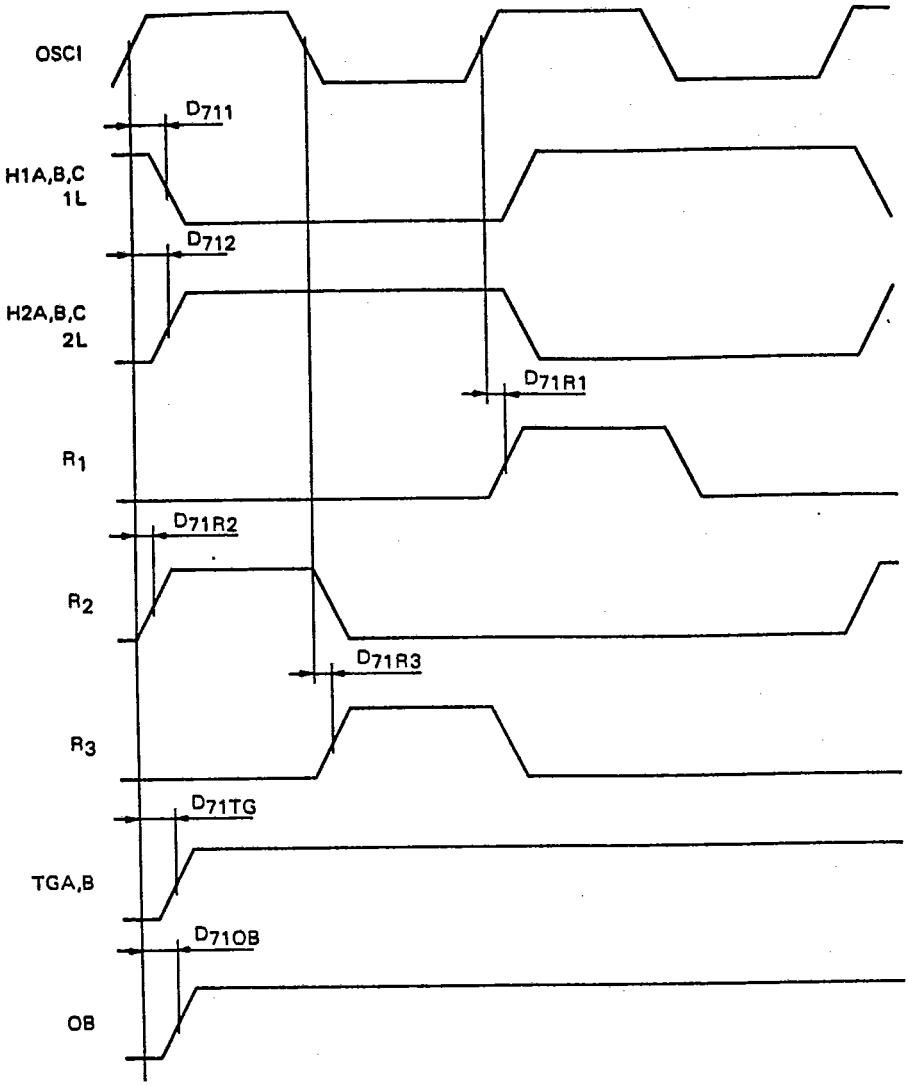
μPD3571D TIMING CHART



μPD3571D DELAY TIME CHART

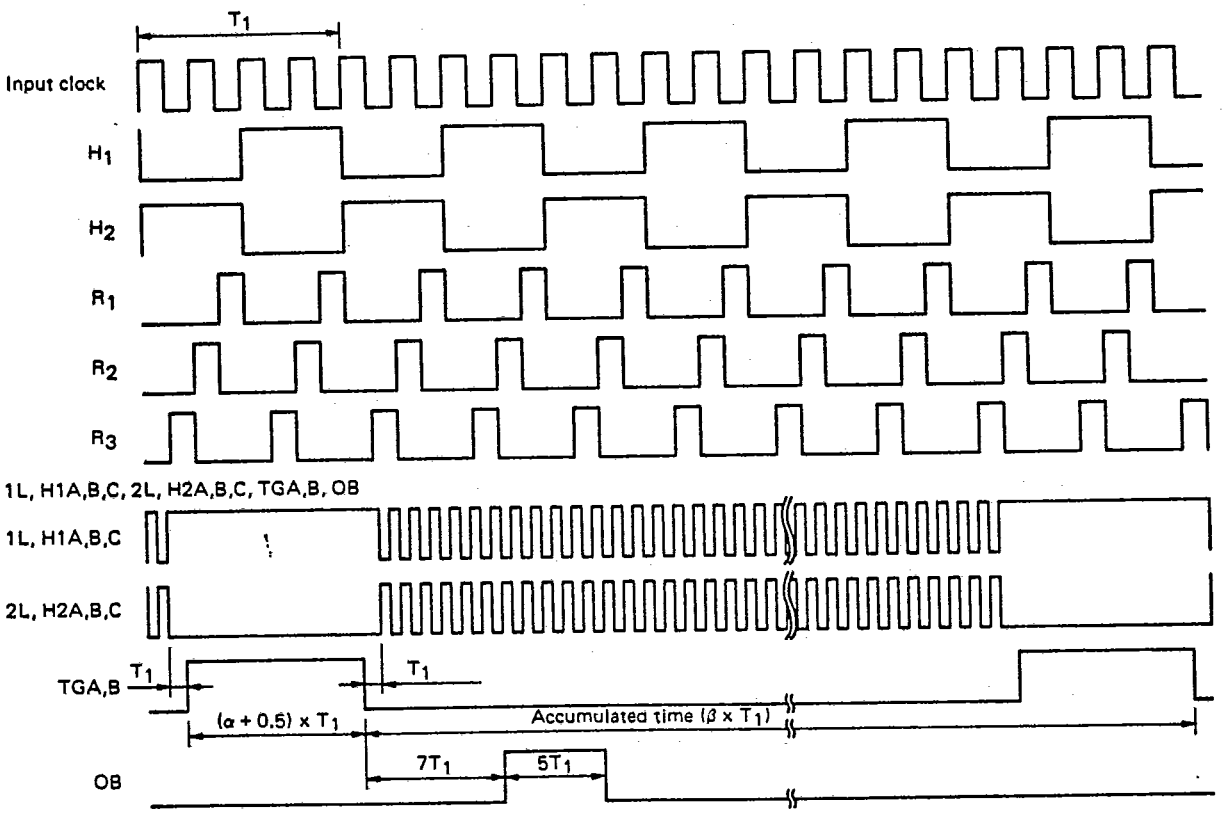
Delay time of each output for the OSCI input clock.

See the area sensor delay time chart for the $I_{VI1,2}$ input.



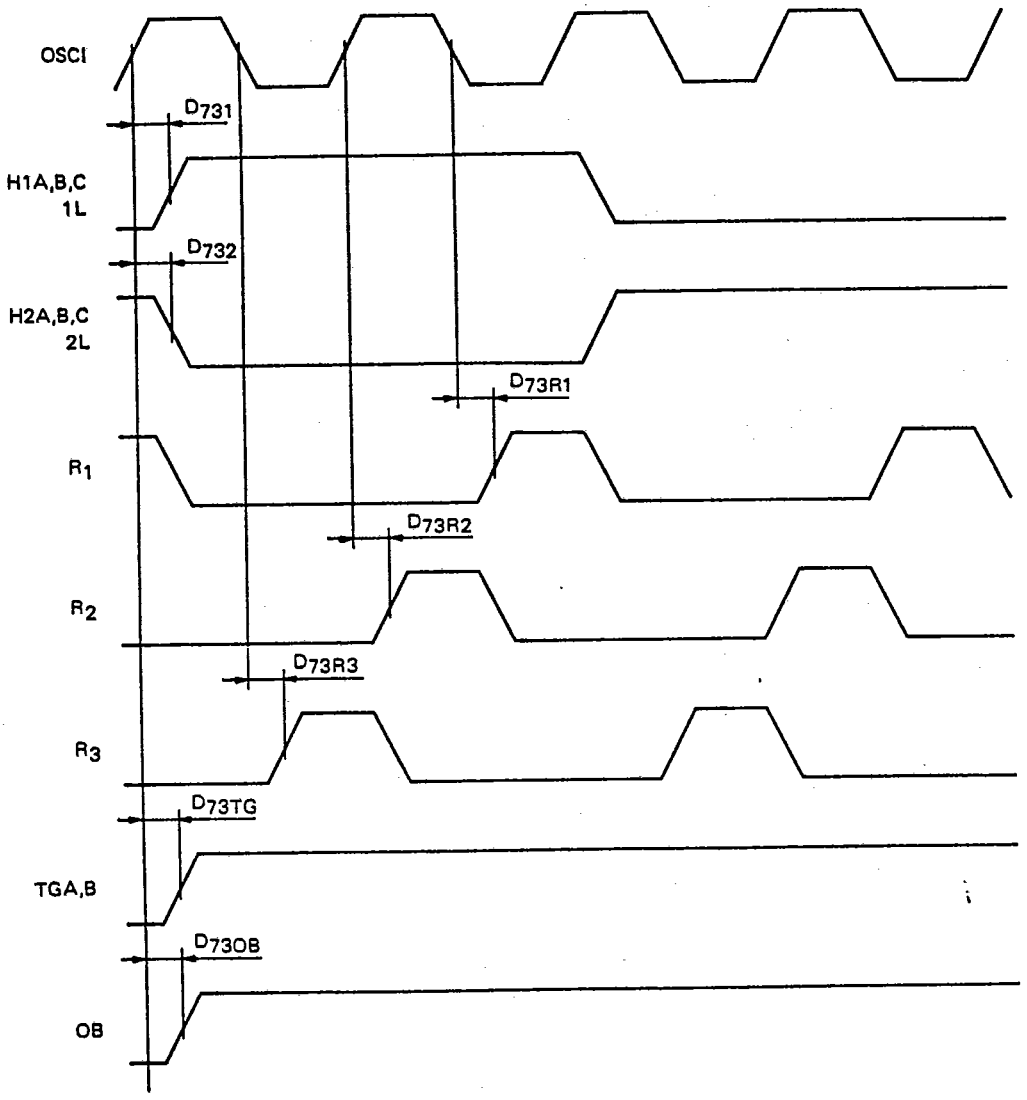
	MIN.	TYP.	MAX.	Unit
D_{711}	10	21	42	ns
D_{712}	10	21	42	
D_{71R1}	8	17	34	
D_{71R2}	8	16	32	
D_{71R3}	8	17	34	
D_{71TG}	9	19	38	
D_{71OB}	13	26	52	

μPD3573D, μPD3574D TIMING CHART



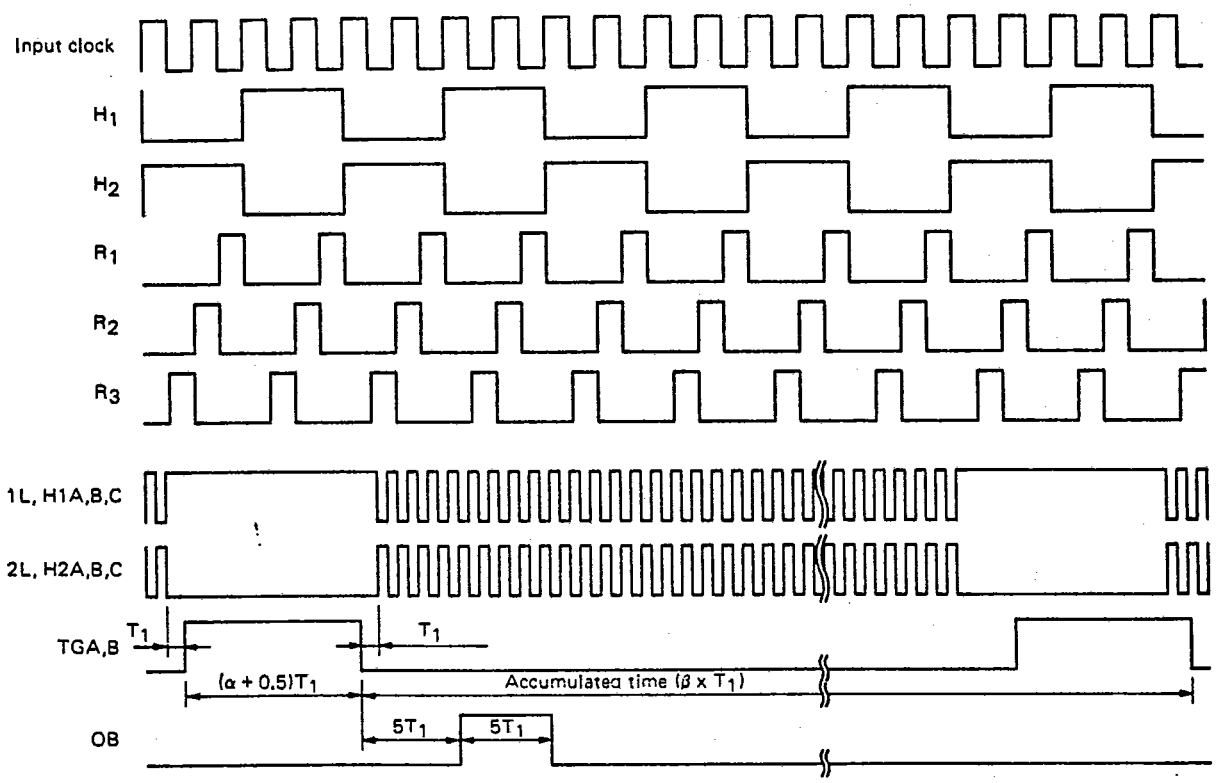
μPD3573D, μPD3574D DELAY TIME CHART

Delay time of each output for the OSCI input clock.
See the area sensor delay time chart for the $I_{VI1,2}$ input.



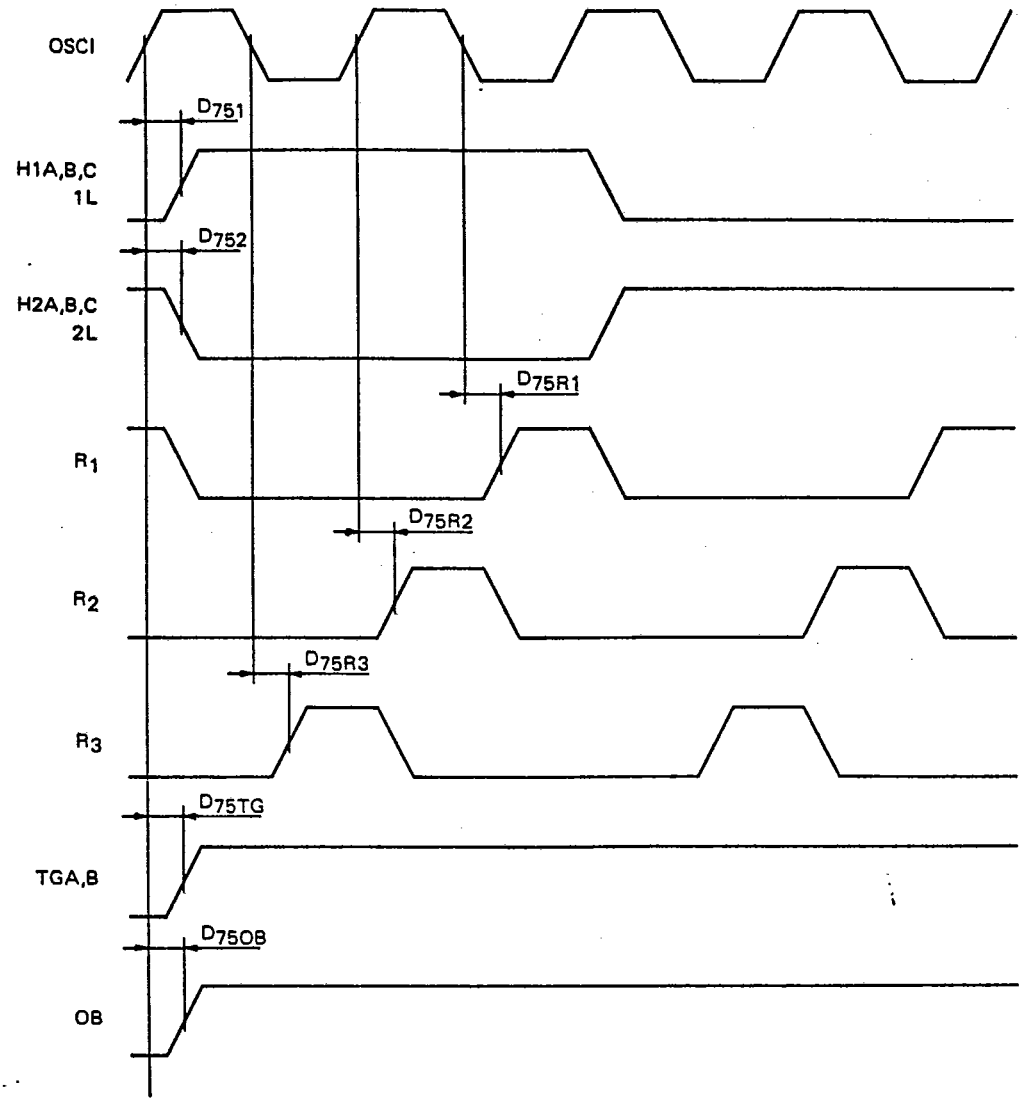
	MIN.	TYP.	MAX.	Unit
D_{731}	11	22	44	ns
D_{732}	11	22	44	
D_{73R1}	8	17	34	
D_{73R2}	8	17	34	
D_{73R3}	8	17	34	
D_{73TG}	12	24	48	
D_{73OB}	19	39	78	

μPD3575D TIMING CHART



μPD3575D DELAY TIME CHART

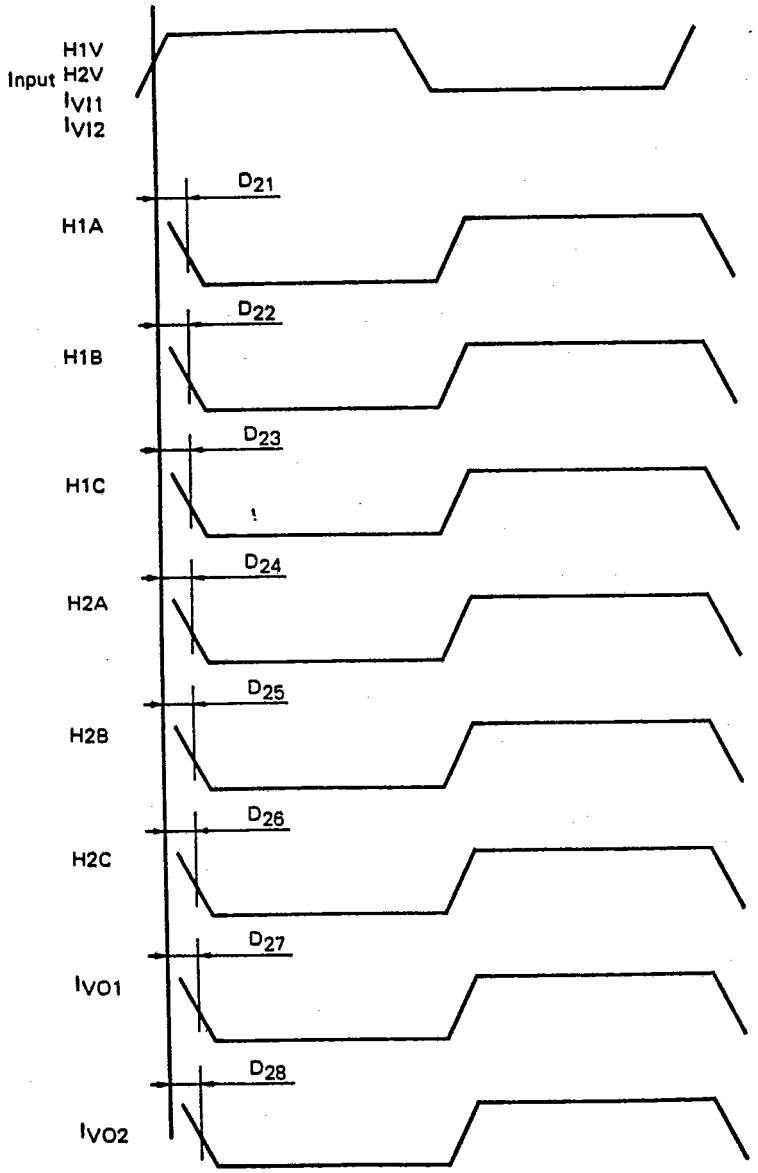
Delay time of each output for the OSCI input clock.
See the area sensor delay time chart for the $I_{V11,2}$ input.



	MIN.	TYP.	MAX.	Unit
D_{751}	11	22	44	ns
D_{752}	11	22	44	
D_{75R1}	8	17	34	
D_{75R2}	8	17	34	
D_{75R3}	8	17	34	
D_{75TG}	12	24	48	
D_{75OB}	15	31	62	

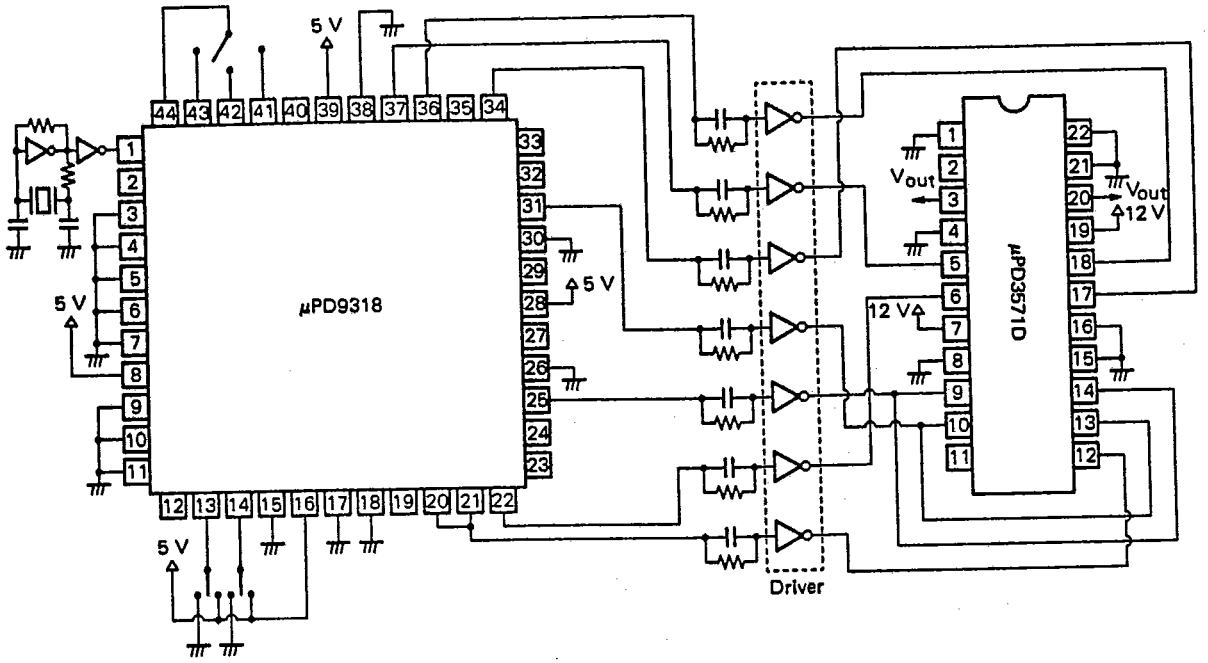
AREA SENSOR DELAY TIME CHART

Output delay time for the input clock

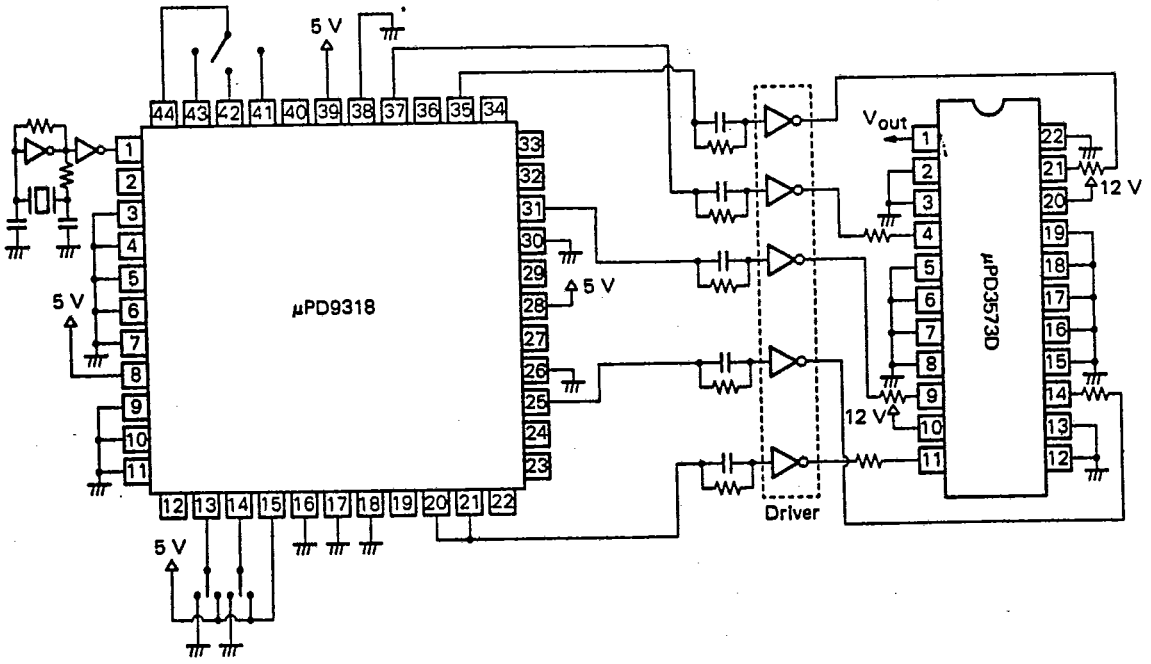


	MIN.	TYP.	MAX.	Unit
D_{21}	5	11	22	ns
D_{22}	5	11	22	
D_{23}	5	11	22	
D_{24}	5	11	22	
D_{25}	5	11	22	
D_{26}	5	11	22	
D_{27}	4	8	16	
D_{28}	4	8	16	

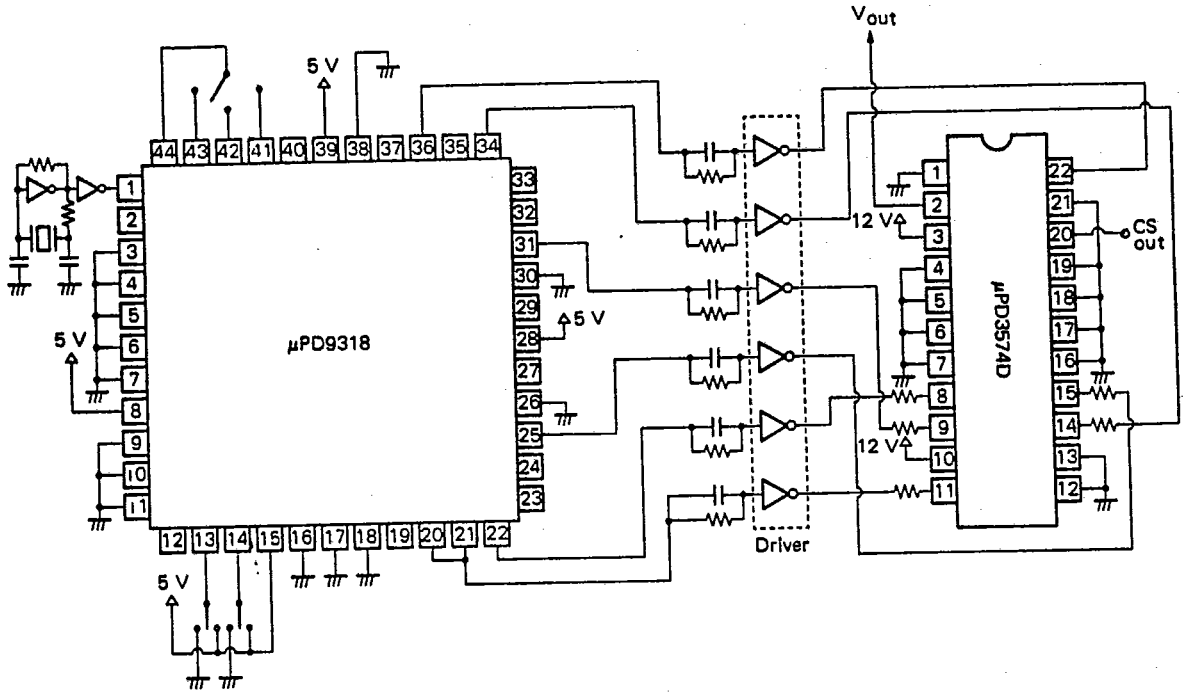
SAMPLE μPD3571D CONNECTION



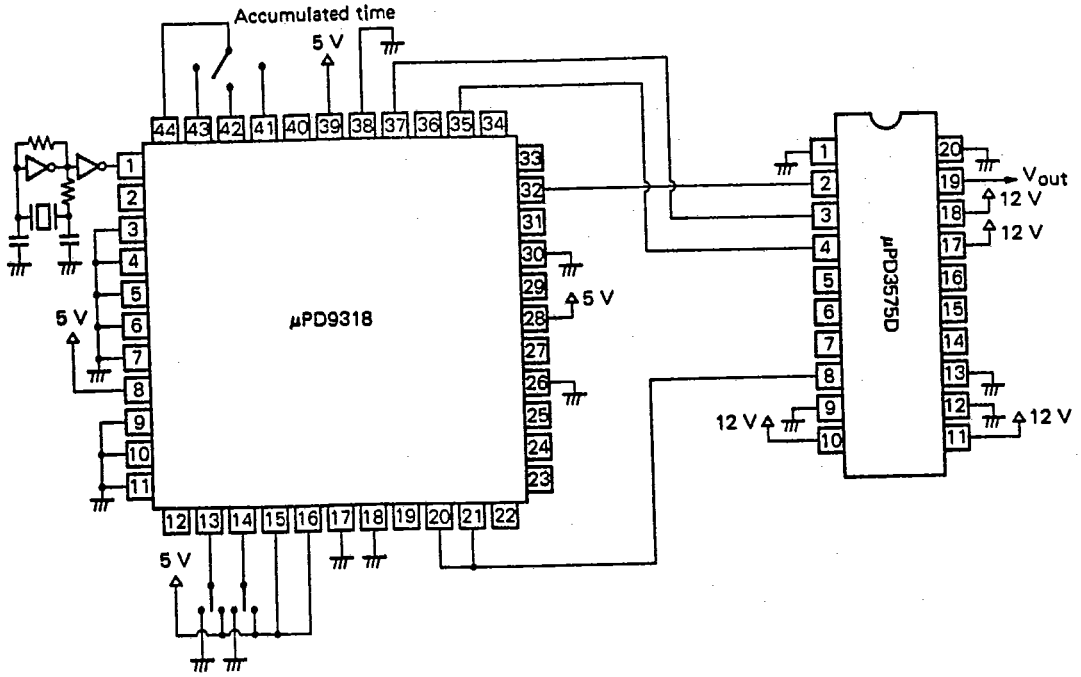
SAMPLE μPD3573D CONNECTION



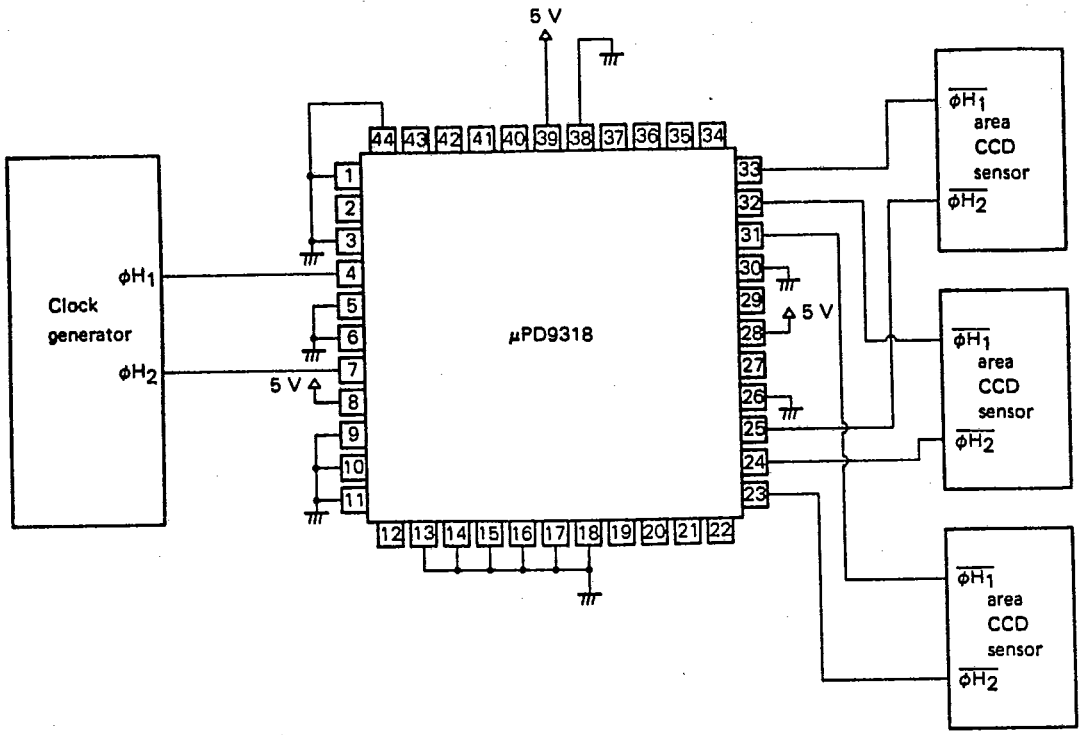
SAMPLE μPD3574D CONNECTION



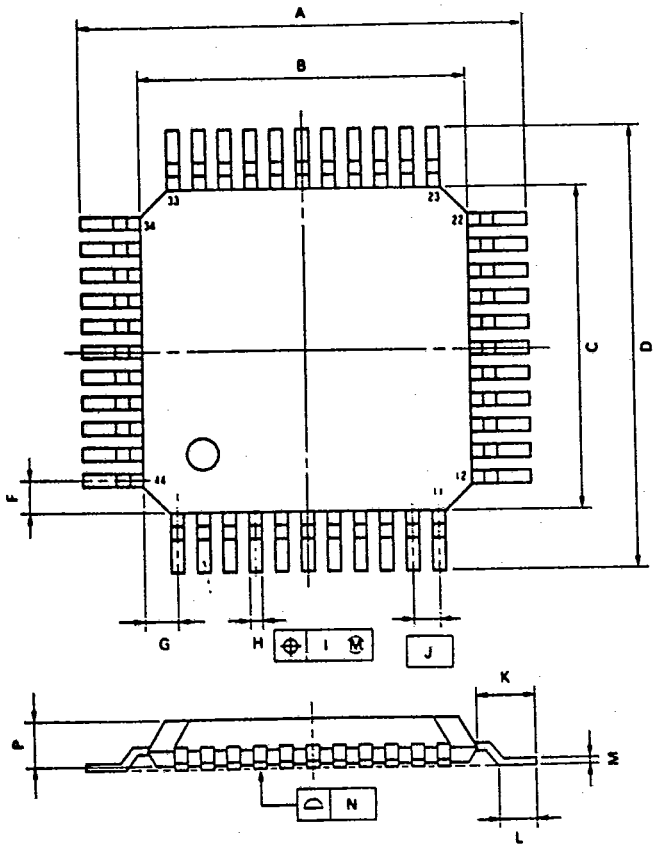
SAMPLE μPD3575D CONNECTION



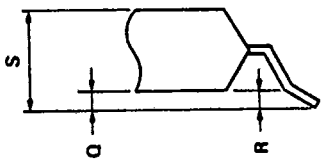
AREA CCD SENSOR CONNECTION DIAGRAM



44PIN PLASTIC QFP (□10)



detail of lead end



P44GB-80-3B4-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$13.6^{\pm 0.4}$	$0.535^{-0.017}_{-0.016}$
B	$10.0^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
C	$10.0^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
D	$13.6^{\pm 0.4}$	$0.535^{-0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.35^{\pm 0.10}$	$0.014^{-0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{-0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.