NEC
NEC Electronics Inc.

ARC Chip Set c/o MCT-ADR Address Path Controller and MCT-DP Data Path Controller

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Description

The ARC chip set operates in a high-performance computer system based on NEC's VR4000-family of 64-bit RISC microprocessors (VR4000™, VR4400™, and VR4200™). See figure 1.

The ARC chip set includes two different ASIC devices: the MCT-ADR Address Path Controller (μPD31432) and the MCT-DP Data Path Controller (μPD31431). The MCT-ADR chip contains the address paths and all of the control logic to implement the interfaces among the microprocessor, main and video memory, and the i386™-compatible bus. The MCT-DP chip contains the data path logic for the above interface and half the total of eight 32-byte data buffers for the I/O cache.

The ARC system uses one MCT-ADR and two MCT-DP chips as shown in figure 2. The MCT-DP is fully controlled by the MCT-ADR. In the ARC system design, each MCT-DP connects to half the 64-bit VR4000-family data bus and the 128-bit system memory bus and all of the i386-compatible databus.

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i386 is a trademark of Intel Corporation.
Windows NT is a trademark of Microsoft Corporation

Figure 1. VR4000-Family RISC Computer System

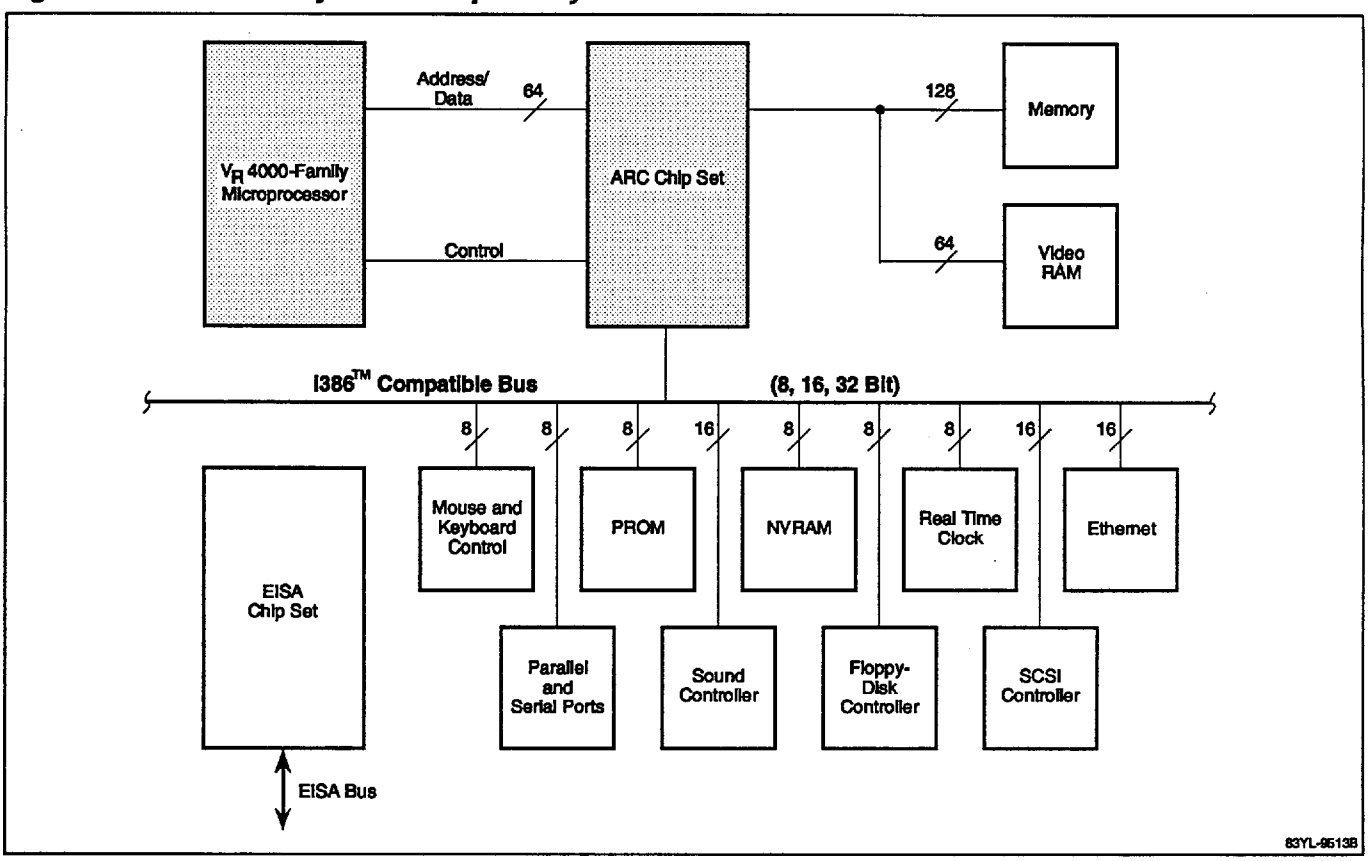
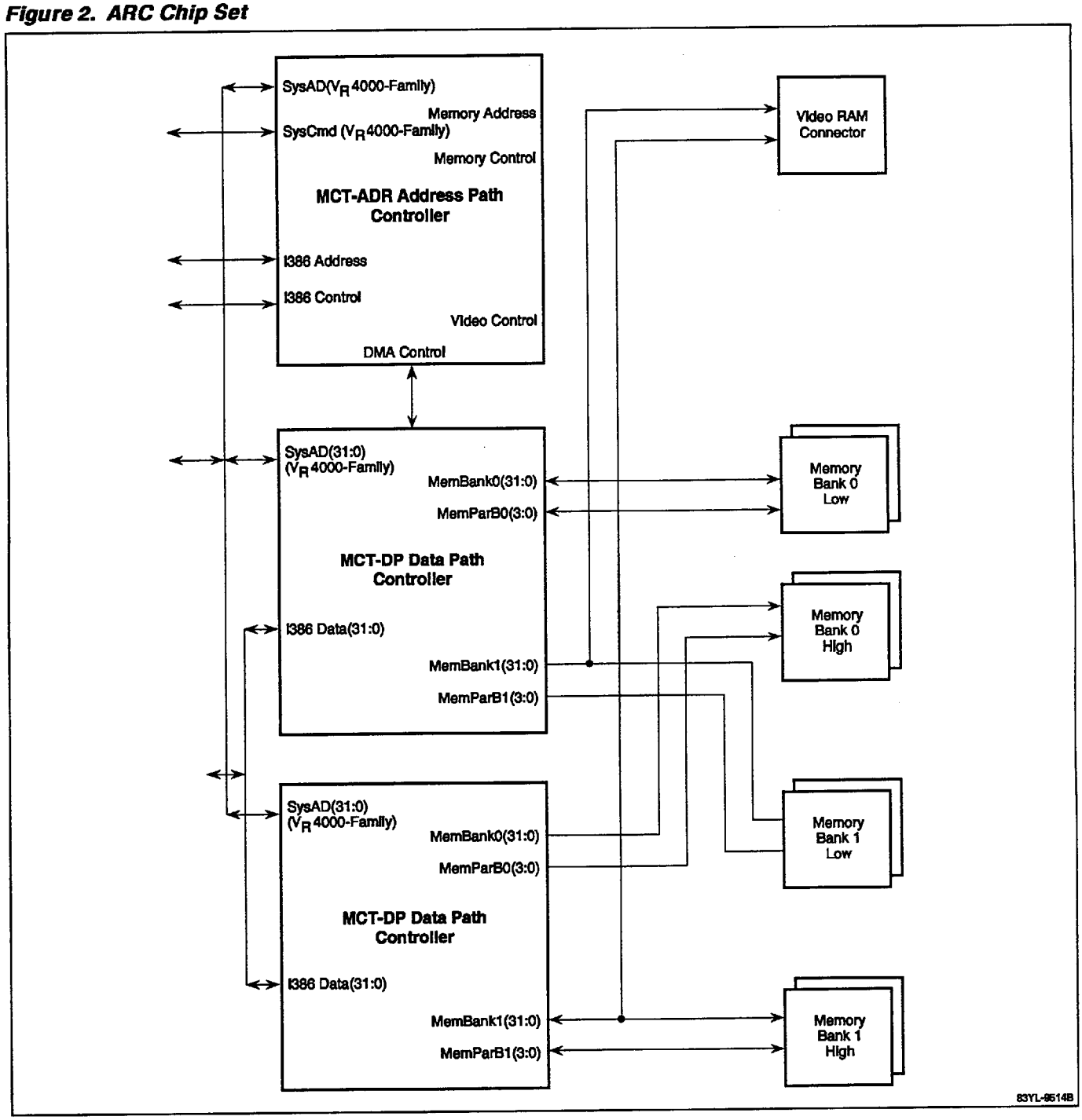


Figure 2. ARC Chip Set

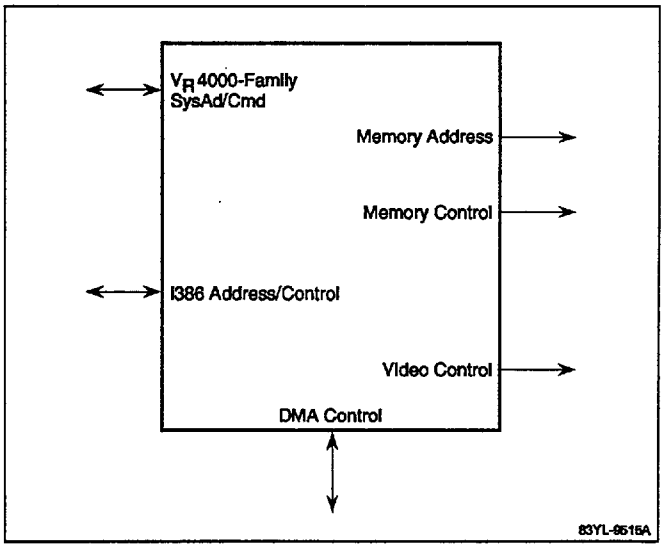


MCT-ADR ADDRESS PATH CONTROLLER (μPD31432)

The MCT-ADR chip contains all of the control logic to implement the following interfaces as shown in figure 3.

- VR4000-family microprocessor interface: Buffering address and control signals
- DRAM interface: DRAM controller for 8 to 64 Mbytes of memory
- Video memory interface: Video command generation
- I/O translation table: I/O logic to memory physical address translation
- i386-compatible master/slave interface
- Control logic for PC-style standard peripheral devices
- Eight slave DMA channels
- I/O cache controller (eight 32-byte fully associative cache blocks)
- 1 to 15 millisecond interval counter

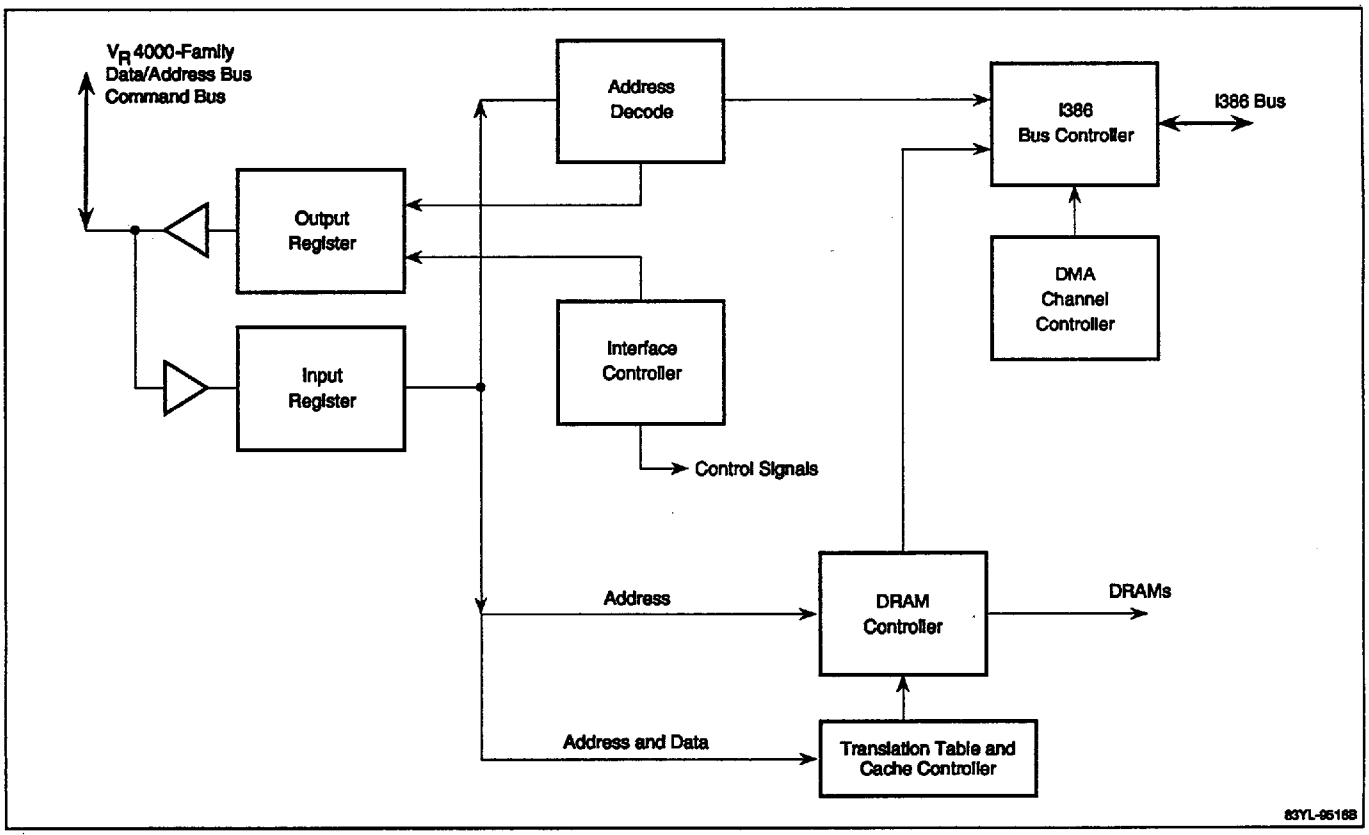
Figure 3. MCT-ADR Address Path Controller



Functional Description

A block diagram illustrating the MCT-ADR functional sections is shown in figure 4. The major blocks are described below.

Figure 4. MCT-ADR Chip, Block Diagram



Input Register

The input register captures all VR4000-family interface signals. The register uses a combination of direct control from the interface signals and the interface control block to capture VR4000-family request address and command packets or a request data packet. All lines are sampled using RCLOCK. The captured lines are then resynchronized with TCLOCK, which is the base clock for the internal logic of the MCT-ADR chip.

Output Register

The output register block contains the VR4000-family interface output registers. All interface lines driven by the MCT-ADR chip are synchronized to the TCLOCK. The output registers and drivers are controlled with a combination of direct control from the interface lines and the interface controller block.

Interface Controller

The interface controller block contains the VR4000-family slave state machine. This state machine controls the interface for both the MCT-ADR chip and the MCT-DP data path control chip. Inside the MCT-ADR chip, VR4000-family requests are directed toward the memory interface, the i386 bus interface, or an internal chip register. The interface between the state machine and the buffered i386 bus and memory interface uses synchronous signal transfers with an asynchronous protocol. Thus, the state machine initiates a request to the remote or memory interface and then waits indefinitely for a grant or ready signal response . The state machine directly sequences internal register reads and writes.

Address Decode

The address decode block receives a command and address from the input register and decodes the address according to the ARC system address map. The decoded outputs of the block are used by the VR4000-family interface to determine what kind of access to complete.

During register accesses to remote bus local devices, the address decode block also provides an encoded device chip select and if required, provides the remote bus logic with the value of the selected local device's speed register.

During internal chip set register accesses, this block provides individual chip selects and write strobes for each of the internal registers.

The block contains the following MCT-ADR internal registers.

- MCT-ADR Interrupt source register
- Global configuration
- ASIC revision number
- Invalid address register
- Remote speed registers (15:00)
- System security register
- Interrupt interval register
- Interval timer
- Interrupt enable register

Memory Controller

The memory controller block receives memory requests from the VR4000-family state machine and the I/O cache controller. The memory controller multiplexes the memory row and column addresses out on the memory address lines, and controls the memory RAS, CAS, and write lines. The memory controller sequences the memory and the MCT-DP Data Path Controller memory data path for the following accesses.

- Memory write partial (1- to 8-byte write); read-modify-write
- Memory small cache block write (16-byte memory write)
- Memory large cache block write (32-byte memory write)
- Memory read partial (1- to 8-byte read)
- Memory small cache block read (16-byte memory write)
- Memory large cache block read (32-byte memory write)
- Video read (8-byte read)
- Video write (1- to 8-byte write)
- Remote bus control block

The remote bus control block is composed of a group of state machines and responds to requests to the system memory space from devices using an i386-type protocol or EISA bus protocol. The interface fully supports both the i386 and EISA protocols for memory accesses.

DMA Channel Controller

The DMA channel contains eight separate DMA controllers. Each DMA controller is able to support a single read or write I/O data flow to and from the system

memory and an I/O device. Each DMA controller contains the following registers:

- Channel mode register
- Channel enable register
- Channel byte count register
- Channel address register

i386 Bus Controller

This block arbitrates to determine which of the various I/O controllers or the VR4000-family microprocessor is allowed to initiate an access on the i386-compatible bus. The arbiter is optimized to assure that access latency for any device is kept to a minimum and meets maximum latency requirements where specified.

Translation Table and Cache Controller

This block contains the logic to translate the 24-bit I/O virtual address into a full 26-bit system memory address. The block also contains the tags and control logic required to implement an eight-block I/O cache. Data for the cache blocks is held in the MCT-DP Data Path Controller.

Once allocated, a cache block is able to provide an intelligent buffered data path between the memory and an I/O device. Memory data is prefetched from memory or flushed to memory whenever the last byte in a cache block is accessed. The I/O cache significantly reduces average memory latency and efficiently uses memory bandwidth.

The cache is designed so that full coherency is maintained between the I/O cache and system memory as viewed from the processor or an I/O device.

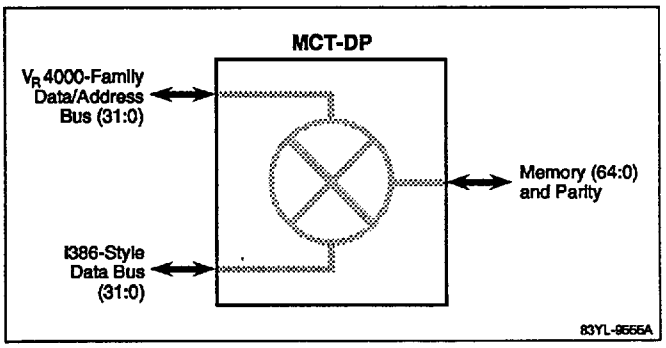
Video System Interconnect

The video system Interconnect provides a high bandwidth protocol to a video frame buffer. The interconnect shares the high bank (64 bits) of the memory data interconnect, and the memory address lines. The interconnect has its own command bus. The video system interconnect provides a peak read bandwidth of 66 Mbytes per second and a peak write bandwidth of 33 Mbytes per second. The video interface is capable of addressing an 8-Mbyte video RAM space and an 8-Mbyte control space.

Packaging and Power

The MCT-ADR is available in a 240-pin PQFP package. The average power dissipation is 1.8 watts.

Figure 5. MCT-DP Data Path Controller, Data Bus Switching



MCT-DP DATA PATH CONTROLLER (μPD31431)

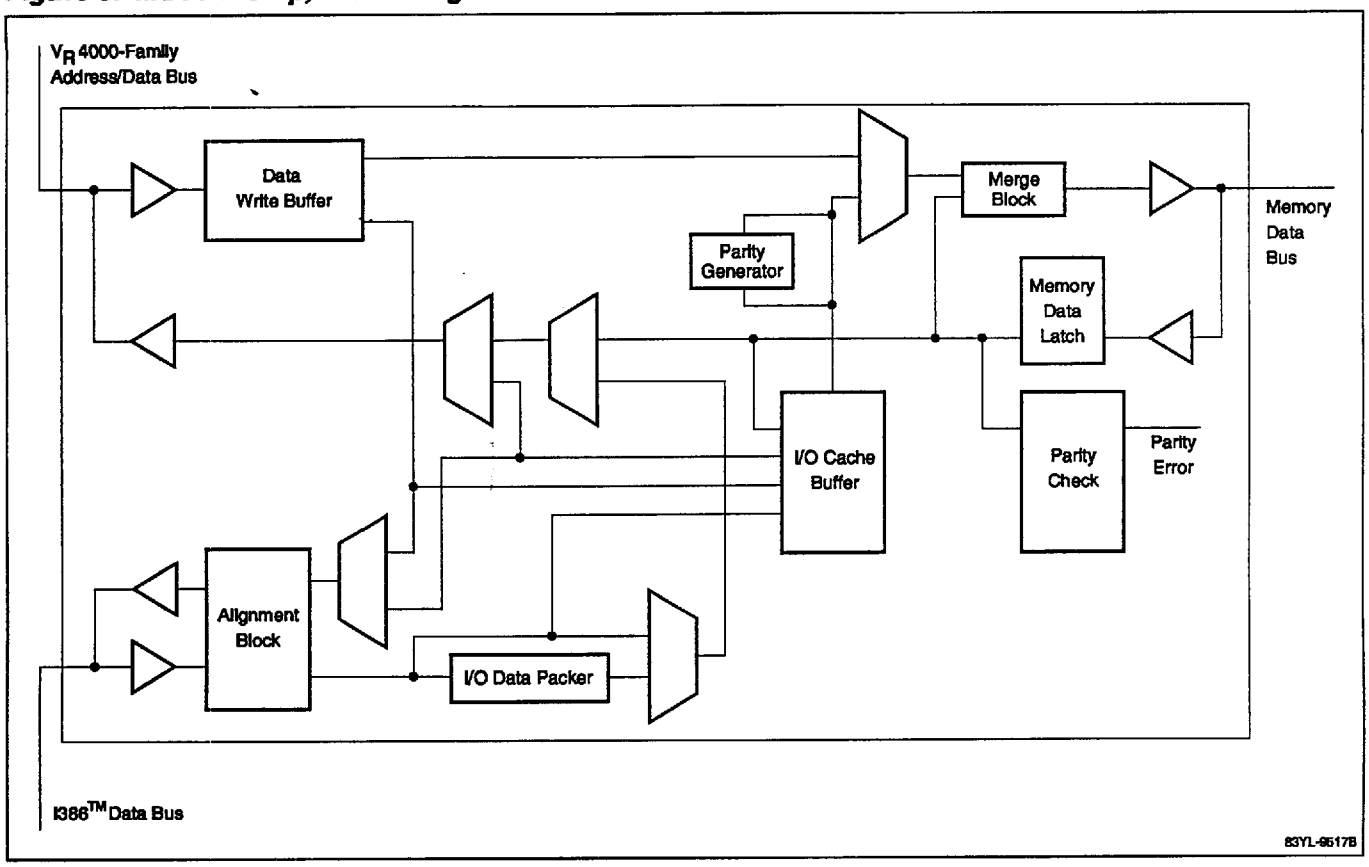
The MCT-DP chip is in effect a crossbar switch with six major connections as shown in figure 5 and listed below.

- VR4000-family data/address bus to the memory data lines (memory space store)
- Memory data lines to the VR4000-family data/address bus (memory space load)
- VR4000-family data/address bus to the i386 data bus lines (I/O register space store)
- i386-style databus to the VR4000-family data/address bus (I/O register space load)
- i386-style data bus to the memory data lines (DMA read from device)
- Memory data lines to the i386 data bus lines (DMA write to device)

The memory interface formed by the two MCT-DP chips is four words or 128 bits wide. The MCT-DP chip connected to the low word of the VR4000-family data/address bus is connected to the even words of the memory interface, while the MCT-DP chip connected to the high word is connected to the odd words of the memory interface. Both MCT-DP chips in the system connect to the i386 data bus.

The MCT-DP contains a 128-bit write buffer that is used to buffer all data from the VR4000-family to the system. The MCT-DP also contains eight 128-byte I/O data buffers, which buffer data transfers between the i386-style bus and the memory system. The write buffer and the I/O data buffer allow concurrent VR4000-family memory operations and I/O direct memory access operations.

Figure 6. MCT-DP Chip, Block Diagram



Functional Description

A block diagram illustrating the MCT-DP chip's functional sections is shown in figure 6. The major blocks are described below.

Data Write Buffers

The MCT-DP chip has four write buffers that allow it to accept its half of an entire VR4000-family large block write in four consecutive bus cycles. The MCT-DP chip relies on external control to sequence data loading into the write buffer. This control is sourced by the MCT-ADR Address Path Controller.

Because control of the write buffers comes from the MCT-ADR chip in the ARC system design, there is a delay between the receipt of a bus transfer and the propagation of the control signals caused by the transfer. Due to the delay between the time the MCT-ADR detects that the first write data packet has been sent on the VR4000-family data/address bus and the time it takes to propagate the write buffer control signals to the MCT-DP chip, a small two-state sequencer is included in the write buffer logic.

Merge Block

The merge block supports writes to memory that are smaller than the 128-bit size of the memory interface. The MCT-ADR does not have the necessary CAS lines to support byte writes into the memory arrays. Instead, a read-modify-write operation is performed on all non-cached memory writes from the VR4000-family and on all I/O cache block writes that are not aligned in 128-bit quantities. The merge block combines memory read data with write data to form a complete memory line. The block uses the memory byte masks sent by the MCT-ADR chip to specify the bytes in the memory line to be replaced by write data.

I/O Cache Buffers

The I/O cache buffers provide the data storage for eight 128-bit bidirectional data buffers. The cache buffer has a 2-bit read/write port to the i386-style bus and provides a 64-bit bidirectional port to the memory data lines. Each cache buffer has 16 "dirty" bits that are set to reflect the data in the cache buffer that has been modified by I/O remote write operations and has not been flushed to memory.

For diagnostic purposes, all cache data storage is also readable and writeable from the bus using the required cache maintenance operations. The byte mask bits are not visible to the VR4000-family processor but they are set during bus writes into the cache buffer.

Alignment Block

The alignment block is used to properly position data from the VR4000-family data/address bus onto the i386-style bus and, in reverse, position the data from the i386-style bus to the proper byte lane on the VR4000-family bus. The bus positions byte data in its eight-byte data/address bus relative to the value of the low 3 bits of the address of a transfer. The i386-style bus is 32 bits wide and the devices on this bus may have 8-, 16-, or 32-bit data interfaces. Thus, when data is moving from the VR4000-family or I/O cache to the i386-style bus, the addressed data is copied down to the lowest data lines. Data moving in the reverse direction from the remote bus to the VR4000-family or the I/O cache data is copied up so that the addressed byte lanes contain a copy of the remote data.

I/O Data Packer

The I/O data packer in the MCT-DP combines four byte-wide remote bus reads into one 32-bit data packet. During system reset, the VR4000-family initially runs out of an 8-bit PROM in the ARC system. The VR4000-family has no logic to combine the required four bytes from a PROM into a single instruction. The I/O data packer contains the storage required to pack four individual PROM fetches per MCT-DP chip into a full instruction fetch. In the system design, this logic is only used during PROM accesses.

System Clocks and Synchronous Inputs

All communication between the ARC chips and the VR4000-family, and between the MCT-ADR and MCT-DP chips, uses a two-phase clock design. Both clocks (TCLOCK and RCLOCK) have the same period and a 50-percent duty cycle. In a 50-MHz system, if TCLOCK is asserted at 0 ns then RCLOCK is asserted at 15 ns. Thus, if data is transferred synchronously to TCLOCK and received on RCLOCK, then 15 ns is allowed for bus transfer and 5 ns for bus hold time.

Loading the Write Buffer

The VR4000-family write buffer is used to buffer write data from the bus until the data is written to the receiver. The write buffer supports three types of bus write commands.

- Partial write (one data transfer)
- Small cache block write (two data transfers)
- Large cache block write (four data transfers)

Parity Control Logic

The memory, the memory data bus, and the VR4000-family data/address bus are protected with byte parity during memory operations. Parity is checked on all operations that require a read from memory. If enabled, the parity error information is saved in a diagnostic register. Parity information is passed from bus to memory, and from memory to bus. Parity is generated for data from the remote I/O bus that is to be written to memory.

Diagnostic Register

In the ARC system design, the diagnostic register is enabled to capture error information only when a memory read operation is in progress. Reads that are part of a partial write (read-modify-write) do not enable the diagnostic register.

The diagnostic register is a 32-bit read/write register used to provide the following system diagnostic functions.

- Save information from memory parity errors, allowing isolation to the offending byte lane
- Allow the inversion of the output parity lines, in effect forcing bad parity
- Reset value contains the revision level of the chip
- 32-bit read/write register that can be used for basic VR4000 diagnostics.