Signetics

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FAST Products	

FAST 74F1766 Burst Mode DRAM Controller (BMDC)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1766	150MHz	200mA

FEATURES

- Allows burst-mode access for systems using Nibble/Page/Static column mode DRAMs
- Complete control of DRAM access, acknowledge, refresh and address multiplexing functions
- True $\overline{RAS}$ interleaving for minimum refresh and $\overline{RAS}$ precharge overhead
- Asynchronous arbitration to speed up accesses
- Selectable Precharge and Acknowledge times
- Selectable Row address hold times
- Supports $\overline{CAS}$ before $\overline{RAS}$ refresh
- Allows control of dynamic RAMs with row access times down to 30ns
- Output drivers designed for incident wave switching

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1766N
44-Pin PLCC	N74F1766A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{C}_0/A_0$, $\overline{C}_1/A_1$, $\overline{C}_2/SIZ_0$, $\overline{C}_3/SIZ_1$,	$\overline{CAS}$ Enable inputs	1.0/1.0	20µA/0.6mA
PRECHRG	$\overline{RAS}$ Precharge Select input	1.0/1.0	20µA/0.6mA
$\overline{REQ}$	Memory access request input	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
RCP	Refresh clock input	1.0/1.0	20µA/0.6mA
B_0, B_1	Bank select inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Reset input	1.0/1.0	20µA/0.6mA
$\overline{BREQ}$	Burst request input	1.0/1.0	20µA/0.6mA
ACKSEL	Acknowledge select input	1.0/1.0	20µA/0.6mA
$\overline{HLDROW}$	Row address hold select input	1.0/1.0	20µA/0.6mA
$\overline{PAGE}$	Page mode select input	1.0/1.0	20µA/0.6mA
CMODE	$\overline{CAS}$ mode select input	1.0/1.0	20µA/0.6mA
CWIDTH	$\overline{CAS}$ width select input	1.0/1.0	20µA/0.6mA
$\overline{ACK}$	Acknowledge output	750/40	3.0mA/24mA
MUX	Address Multiplexer output	150/40	15.0mA/24mA
$\overline{RAS}_{0-3}$	Row address strobe outputs	750/40	15.0mA/24mA
$\overline{CAS}_{00-33}$	Column address strobe outputs	750/40	15.0mA/24mA

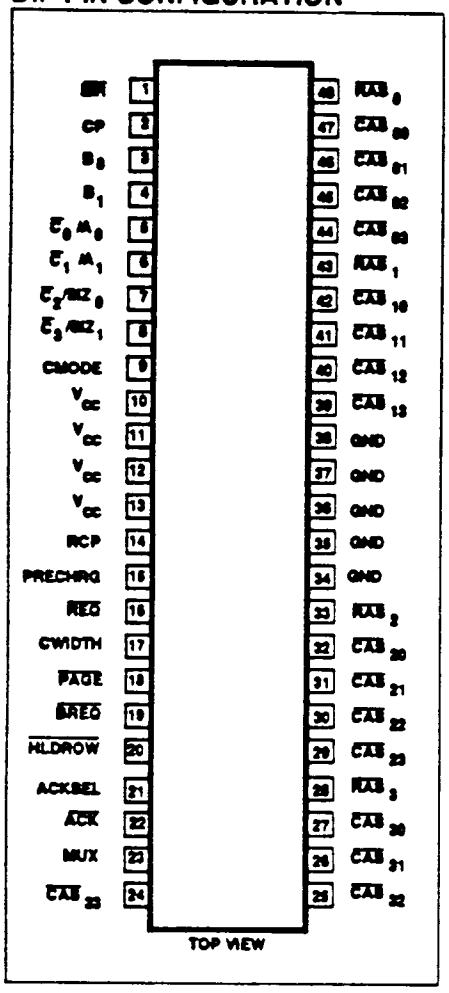
NOTE:
1.One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

DESCRIPTION

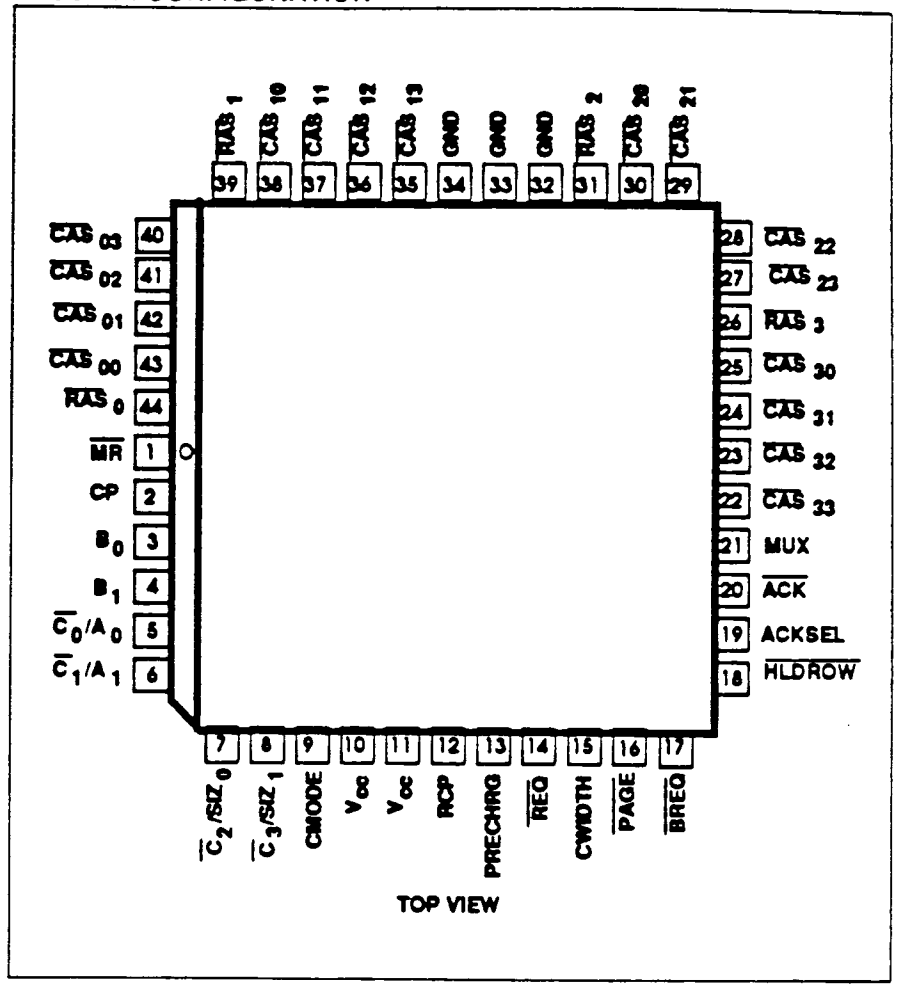
The Signetics Burst Mode DRAM Controller (BMDC) is a high performance memory timing generator designed to support Page, Nibble or Static Column modes of operation in addition to the normal DRAM access cycles. It performs memory access/refresh arbitration, refresh and memory access timing, $\overline{RAS}$ interleaving, $\overline{CAS}$ byte decoding and controls up to four banks of DRAM.

The BMDC generates DRAM timing and thus requires a companion address multiplexer like the 74F1762 Memory Address Multiplexer for row and column address generation. This provides the flexibility of using the controller with any size of DRAM array by simply using an appropriate address multiplexer. For example when used with the 74F1762, it can control 4Mbit DRAMs.

DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS DIP	PINS PLCC	TYPE	NAME AND FUNCTION
CP	2	2	Input	Clock input. Used by the controller for all timing and arbitration functions.
RCP	14	12	Input	Refresh clock input. Divided internally by 64 to produce an internal Refresh Request.
PRECHRG	15	13	Input	$\overline{RAS}$ Precharge input. A Low will program the Controller to guarantee 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
$\overline{REQ}$	16	14	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
B_0,B_1	3,4	3,4	Input	$\overline{RAS}$ Bank Select inputs.See Table1 for decoding information.
$\overline{BREQ}$	19	17	Input	Active Low Burst Request input. If active during an access cycle, the controller automatically toggles $\overline{CAS}_X$ outputs for burst access. The duration of the $\overline{CAS}_X$ outputs are controlled by the CWIDTH and $\overline{PAGE}$ inputs.
ACKSEL	21	19	Input	Acknowledge timing Select input. A Low will program the Controller to assert $\overline{ACK}$ output 2 CP clock cycles after $\overline{CAS}_X$ is asserted. When High $\overline{ACK}$ output will be asserted at the time of assertion of $\overline{CAS}_X$.
$\overline{HLDROW}$	20	18	Input	Row Address Hold input. A Low will program the Controller to assert MUX output 1/2 CP clock cycles after $\overline{RAS}_X$ is asserted. When High MUX output will be asserted at the time of assertion of $\overline{RAS}_X$.
$\overline{ACK}$	22	20	Output	Active Low, 3-state Acknowledge output. Asserted as selected by the ACKSEL input. This is asserted only once during a burst or non-burst memory access cycle, and is not asserted during a memory refresh cycle.
CMODE	9	9	Input	$\overline{CAS}$ Mode select input. When Low $\overline{CAS}_X$ outputs are enabled directly by the $\overline{C}_{0-3}$ inputs. When High $\overline{CAS}_X$ outputs are enabled by decoding the A_{0-1} and SIZ_{0-1} inputs (see Table 2).
$\overline{C}_0/A_0$	5	5	Input	$\overline{CAS}_{X0}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_1/A_1$	6	6	Input	$\overline{CAS}_{X1}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_2/SIZ_0$	7	7	Input	$\overline{CAS}_{X2}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{C}_3/SIZ_1$	8	8	Input	$\overline{CAS}_{X3}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{RAS}_{0-3}$	48,43, 33,28	44,39, 31,26	Output	Active Low Row Address Strobe outputs. Asserted as dictated by the B_{0-1} inputs. (see Table 1 for decoding information)
CWIDTH	17	15	Input	$\overline{CAS}_X$ pulse Width select input. This input selects the initial $\overline{CAS}_X$ pulse width in the burst mode. When Low the initial $\overline{CAS}_X$ pulse is selected equal to 3 CP clock cycles and when High it's selected equal to 2 CP clock cycles. This input is ignored in the non-burst mode.
MUX	23	21	Output	Row/Column address Multiplex output. Asserted as selected by the $\overline{HLDROW}$ input and is used by an external address multiplexer like the 74F1762.
$\overline{CAS}_{00-33}$	47-44, 42-39, 32-29, 27-24	43-40, 38-35, 30-27, 25-22	Output	Active Low Column Address Strobe outputs. Asserted when enabled by the $\overline{CAS}_X$ enable inputs (Table 2) and $\overline{RAS}_X$ bank circuitry.
$\overline{PAGE}$	18	16	Input	$\overline{PAGE}$ mode select input. Controls $\overline{CAS}_X$ pulse width after the initial $\overline{CAS}_X$ pulse in the burst mode. When this input is Low the $\overline{CAS}_X$ pulse is selected equal to 2 CP cycles and when High it's selected equal to 1 CP cycle. This is ignored in the non-burst mode.
$\overline{MR}$	1	1	Input	Active Low Master Reset input. The first Low to High transition on the CP clock after $\overline{RESET}$ is Low will reset the controller. After reset, the 74F1766 remains in test mode until the first rising edge of CP clock.
Vcc	10-13	10,11		Power
GND	34-38	32-34		Ground

Burst Mode DRAM Controller (BMDC)

FAST 74F1766

ARCHITECTURE

The 74F1766 Burst Mode DRAM controller is a synchronous device, with all signal generation being a function of the input clock (CP).

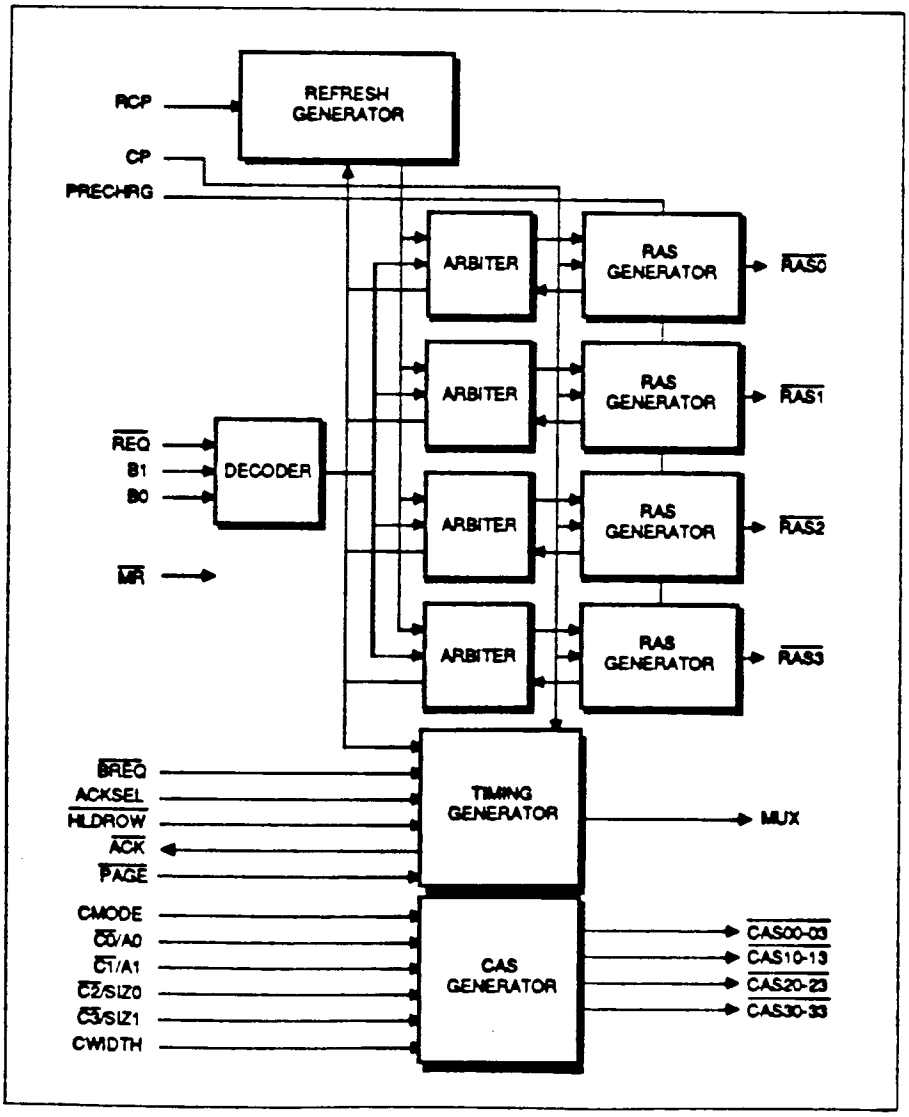
The 'F1766 Block Diagram (Figure 1) shows the overall architecture of the device. The refresh generator uses $\overline{CAS}$ before $\overline{RAS}$ refresh and produces refresh requests based upon the frequency of the refresh clock (RCP). A memory refresh request is generated for all four banks every 64 cycles of the RCP clock. This request is arbitrated individually for all banks with it's corresponding memory access request made through the $\overline{REQ}$ input. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated precharge time.

Every one of the four banks have individual refresh monitors to keep track of any missed refreshes during a long page mode access. A total of 127 missed refreshes can be stored by each bank. After the page mode access cycle the controller will burst refresh that bank until all missed refreshes have been performed. In order to limit the number of outputs switching at the same time the refresh generator will stagger the refresh cycles to individual banks, starting from Bank 0. The bank select inputs (B_{0-1}) select which $\overline{RAS}_x$ output will be enabled during the access cycle. Each $\overline{RAS}_x$ output has it's own arbiter and timing generator to allow true $\overline{RAS}$ interleaving between access cycles and refresh cycles. This also enables transparant $\overline{RAS}$ precharge between access cycles. The $\overline{RAS}$ precharge time can be selected by the PRECHRG input to be equal to either 3 or 4 CP clock cycles.

The timing generator allows burst or non-burst accesses selected by the $\overline{BREQ}$ input. If $\overline{BREQ}$ input is asserted during a memory access cycle the controller will automatically toggle $\overline{CAS}_x$ outputs for burst accesses. The duration of the first $\overline{CAS}_x$ pulse is determined by the CWIDTH input, and by the $\overline{PAGE}$ input for subsequent $\overline{CAS}_x$ pulses. This is particularly useful when block moves are made into and out of memory for cache transfers. The $\overline{CAS}_x$ outputs may be gated by the byte select inputs ($\overline{C}_{0-3}$) or by a decoding function generated by the $A_0/A_1/\overline{SIZ}_0/\overline{SIZ}_1$ using the CMODE input. Each $\overline{RAS}$ output has an associated set of $\overline{CAS}$ outputs for that bank, for example $\overline{RAS}_0$ uses $\overline{CAS}_{00-03}$ outputs. This allows simultaneous refresh of $\overline{RAS}$ banks while another bank is being accessed by the processor.

The ACKSEL input allows the assertion of Acknowledge ($\overline{ACK}$) output to be either when $\overline{CAS}_x$ is asserted or 2 CP clock cycles after that. $\overline{ACK}$ stays asserted in the burst mode until $\overline{REQ}$ is negated. The $\overline{HLDROW}$ input can be used to assert MUX output when $\overline{RAS}_x$ is asserted or one-half CP clock cycle after that.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Most DRAMs require that $\overline{RAS}$ and $\overline{CAS}$ inputs be toggled a number of times before the DRAM may be used. The BMDC has an initialization feature which allows the automatic excersizing of the DRAMs. This is done by resetting the device, which forces the refresh counter to be offset by ten, thus forcing ten refresh cycles before allowing any memory access cycles. The $\overline{REQ}$ input is sampled on the rising edge of the CP clock. If no refresh request is being serviced, one of the $\overline{RAS}_x$ outputs (depending on the B_{0-1} inputs) will be asserted immediately. Depending on the state of the $\overline{HLDROW}$ input, the MUX output will be driven High either at the assertion of $\overline{RAS}_x$ or one-half CP cycle after that. One CP cycle after the assertion of $\overline{RAS}_x$, the $\overline{CAS}_x$ outputs enabled either by the $\overline{C}_{0-3}$ inputs or the decoded function of $A_0/A_1/\overline{SIZ}_0/\overline{SIZ}_1$ (as selected by the CMODE input) will be asserted. If the ACKSEL input is High, the $\overline{ACK}$ output will be asserted at this time; otherwise it will be asserted 2 CP cycles after this time.

The $\overline{BREQ}$ input is sampled when the $\overline{CAS}_x$ outputs are initially asserted, and this determines what will take place on the $\overline{CAS}_x$ outputs after their initial assertion. If $\overline{BREQ}$ is High, the $\overline{RAS}_x$, MUX and $\overline{CAS}_x$ outputs will remain in their present state until the negation of $\overline{REQ}$, at which time all these signals are negated. Negation of $\overline{REQ}$ is asynchronous to the CP clock cycle and therefore is not sampled

by the clock. If the $\overline{BREQ}$ is Low at the assertion of $\overline{CAS}_X$, the $\overline{RAS}_X$ and MUX outputs will stay in their existing state but the $\overline{CAS}_X$ outputs after staying Low for 2 CP cycles will alternately be negated and asserted for one CP clock cycle if $\overline{PAGE}$ input is High or for two CP clock cycles if $\overline{PAGE}$ input is Low. This process will continue untill the negation of the $\overline{REQ}$ input, at which time the $\overline{RAS}_X$, MUX, $\overline{CAS}_X$ and $\overline{ACK}$ outputs will be negated.

As mentioned before, the controller guarantees a $\overline{RAS}$ precharge on all the $\overline{RAS}_X$ outputs to be either 3 or 4 CP clock cycles as selected by the PRECHRG input. This precharge function is independent among the $\overline{RAS}_X$ outputs, which means that, by connecting the appropriate low-order address lines from the processor to the B_{0-1} inputs, sequential accesses, a common occurance with microprocessors, will result in no precharge overhead.

The refresh function is also independent between the $\overline{RAS}_X$ outputs, which means that three $\overline{RAS}_X$ outputs can be performing a $\overline{CAS}$ before $\overline{RAS}$ refresh, while the fourth is in the precharge mode or is being accessed, thus reducing the overall refresh overhead.

Output driving Characteristics

Considering the transmission line characteristics of the DRAM arrays, the outputs of the DRAM controller have been designed to provide incident-edge switching (in Dual-Inline-Packaged memory arrays), needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218. The driving characteristics of the 74F1766 are the same as those of the 74F765 shown in the application note.

Testing the BMDC

Precautions have been taken in the design of the BMDC to facilitate testing of the device. After a $\overline{MR}$ is issued and the CP input is toggled from Low to High all internal flip-flops are brought into a known state, and the device goes into the test mode from the time $\overline{MR}$ is deasserted till the time the first Low to High transition occurs on the CP clock. During the test mode, bank refresh counters (that keep track of missed refreshes) are clocked by a High to Low transition on the $\overline{C}_{0-3}$ inputs and the main refresh counter is clocked on the rising RCP clock edge. The comparators that compare the contents of the main refresh counter and refresh counters of individual banks are clocked by the Low to High transition on the PRECHRG input and are gated on to $\overline{RAS}_X$ outputs by the $\overline{C}_{0-3}$ inputs. So whenever $\overline{C}_{0-3}$ are Low, $\overline{RAS}$ outputs are disabled (pulled High). If the contents of the main refresh counter and the individual bank counters are equal, the corresponding $\overline{RAS}$ output will be High, if not equal the corresponding $\overline{RAS}$ output will be Low. This allows full testing of the Counters and comparators with relatively few lines of code.

B_0	B_1	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
0	0	0	1	1	1
0	1	1	0	1	1
1	0	0	1	0	1
1	1	0	1	1	0

TABLE 1: BANK SELECT DECODE

CMODE	OPERATION	$\overline{C}_3/SIZ_1$	$\overline{C}_2/SIZ_0$	$\overline{C}_1/A_1$	$\overline{C}_0/A_0$	$\overline{CAS}_{X3}$	$\overline{CAS}_{X2}$	$\overline{CAS}_{X1}$	$\overline{CAS}_{X0}$
1	LONG WORD	0	0	0	0	0	0	0	0
1		0	0	0	1	0	0	0	1
1		0	0	1	0	0	0	1	1
1		0	0	1	1	0	1	1	1
1	BYTE	0	1	0	0	1	1	1	0
1		0	1	0	1	1	1	0	1
1		0	1	1	0	1	0	1	1
1		0	1	1	1	0	1	1	1
1	WORD	1	0	0	0	1	1	0	0
1		1	0	0	1	1	0	0	1
1		1	0	1	0	0	0	1	1
1		1	0	1	1	0	1	1	1
1	THREE BYTES	1	1	0	0	1	0	0	0
1		1	1	0	1	0	0	0	1
1		1	1	1	0	0	0	1	1
1		1	1	1	1	0	1	1	1

TABLE 2: BYTE SELECT DECODE

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	All pins except $\overline{ACK}$			-15	mA
		$\overline{ACK}$ output			-3	mA
I_{OL}	Low-level output current				24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All pins except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
V_{OH2}[3]				I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}		$\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	All pins except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{OL2}[3]				I_{OL2}[3]=60mA	±5%V_{CC}		0.45	0.80	V
V_{OL}		$\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current, High level voltage applied		V_{CC} =MAX, V_o = 2.7V					50	µA
I_{OZL}	Off-state output current, Low level voltage applied		V_{CC} =MAX, V_o = 0.5V					-50	µA
I_{OS}[4]	Short-circuit output current		V_{CC} =MAX	All pins except $\overline{ACK}$		-100		-225	mA
				$\overline{ACK}$ output		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX				185	240	mA
		I_{CCL}					200	260	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH}[3] & I_{OL}[3] are transient currents necessary to guarantee a Low to High & a High to Low transition in a 30 OHM transmission line respectively. Refer to Application note number AN218 for further explanation.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

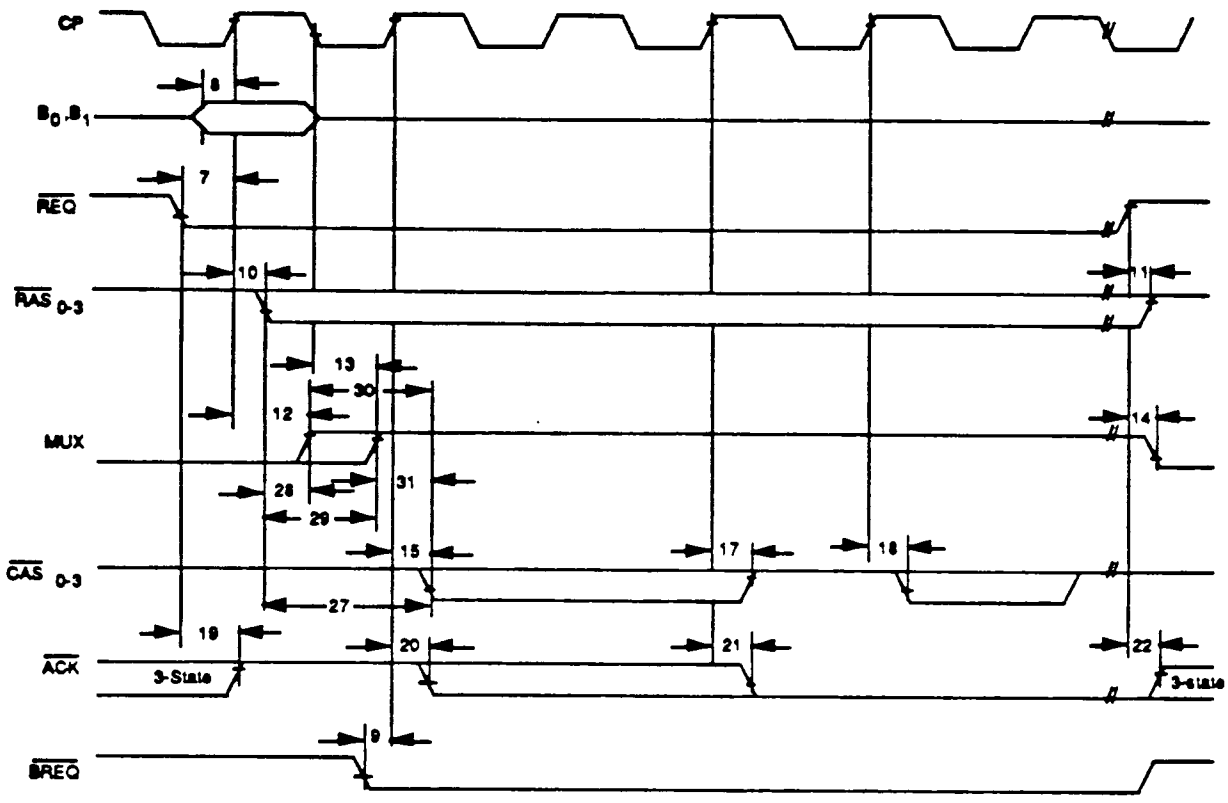
AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		4			4		ns
3	CP clock high time		6			6		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}$(↓) to CP(↑)		2.5			4		ns
8	Setup time B_0, B_1 to CP(↑)		3			4		ns
9	Setup time $\overline{BREQ}$ to CP(↑)		3			4		ns
10	Propagation delay CP(↑) to $\overline{RAS}$(↓)		3	7.5	9.5	3	10	ns
11	Propagation delay $\overline{REQ}$(↑) to $\overline{RAS}$(↑)		4	9	12	3	13	ns
12	Propagation delay CP(↑) to MUX(↑)	$\overline{HLDROW}$ = 1	3	8	10	3	11	ns
13	Propagation delay CP(↓) to MUX(↑)	$\overline{HLDROW}$ = 0	2	5.5	7.5	2	8.5	ns
14	Propagation delay $\overline{REQ}$(↑) to MUX(↓)		4	8.5	10.5	4	11.5	ns
15	Propagation delay CP(↑) to $\overline{CAS}$(↓)		3	8.5	11.5	3	12	ns
16	Propagation delay $\overline{REQ}$(↑) to $\overline{CAS}$(↑)		4	9.5	12	4	14	ns
17	Propagation delay CP(↑) to $\overline{CAS}$(↑)	$\overline{BREQ}$ = 0	3	8	10	3	11	ns
18	Propagation delay CP(↑) to $\overline{CAS}$(↓)	$\overline{BREQ}$ = 0	3	9	11	3	12	ns
19	Propagation delay $\overline{REQ}$(↓) to $\overline{ACK}$(3-state to High)		2	5	7	2	8	ns
20	Propagation delay CP(↑) to $\overline{ACK}$(↓)	ACKSEL = 1	3	7.5	9.5	3	10	ns
21	Propagation delay CP(↑) to $\overline{ACK}$(↓)	ACKSEL = 0	3	7.5	9.5	3	10	ns
22	Propagation delay $\overline{REQ}$(↑) to $\overline{ACK}$(Low to 3- state)		2	5	7	2	7.5	ns
23	Propagation delay CP(↑) to $\overline{CAS}$(↓) *	REFRESH CYCLE	4	9.5	12	4	13	ns
24	Propagation delay CP(↑) to $\overline{RAS}$(↓) *	REFRESH CYCLE	3	7.5	9.5	3	10	ns
25	Propagation delay CP(↑) to $\overline{CAS}$(↑) *	REFRESH CYCLE	4	9.5	12	4	14	ns
26	Propagation delay CP(↑) to $\overline{RAS}$(↑) *	REFRESH CYCLE	4	9	11	3	13	ns
27	Propagation delay $\overline{RAS}$(↓) to $\overline{CAS}$(↓)		1tcp-1	1tcp+1	1tcp+2.5	1tcp-1	1tcp+3	ns

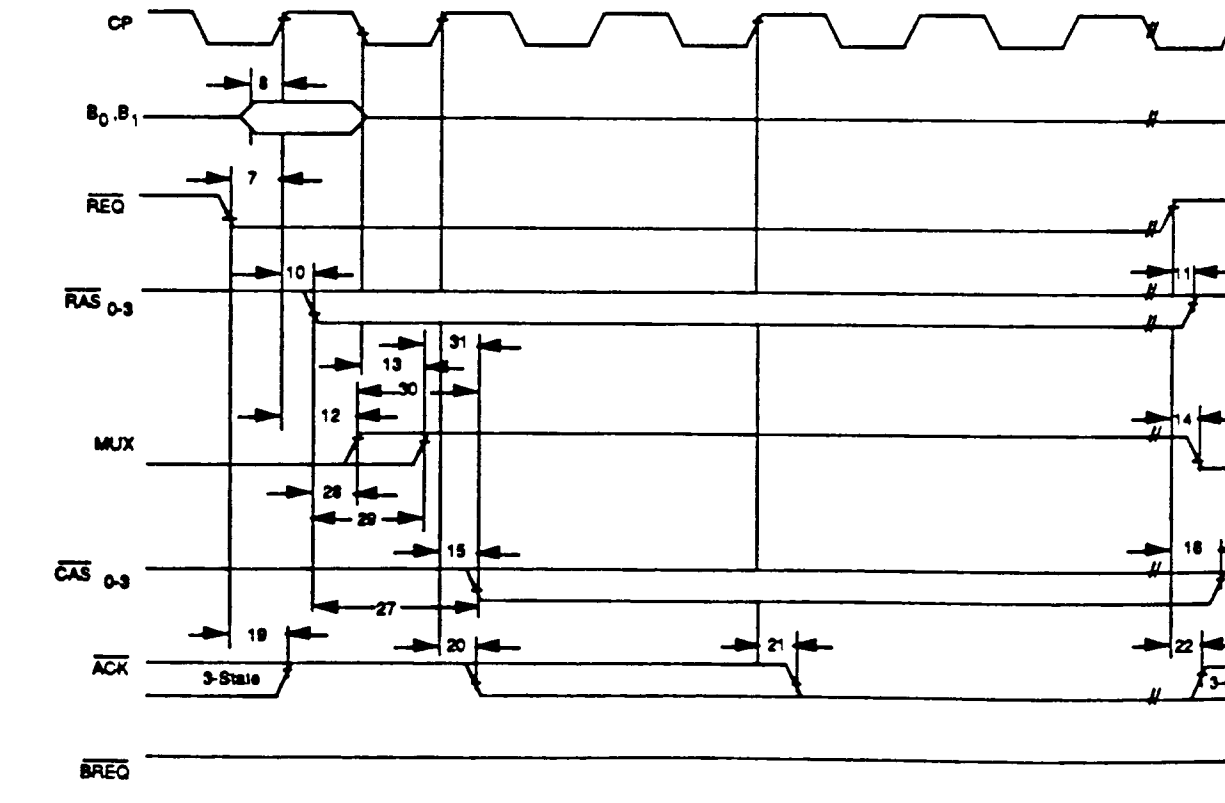
* The same parameters will hold for a refresh cycle during $\overline{RAS}_1$, $\overline{RAS}_2$ and $\overline{RAS}_3$ access cycles.

AC ELECTRICAL CHARACTERISTICS

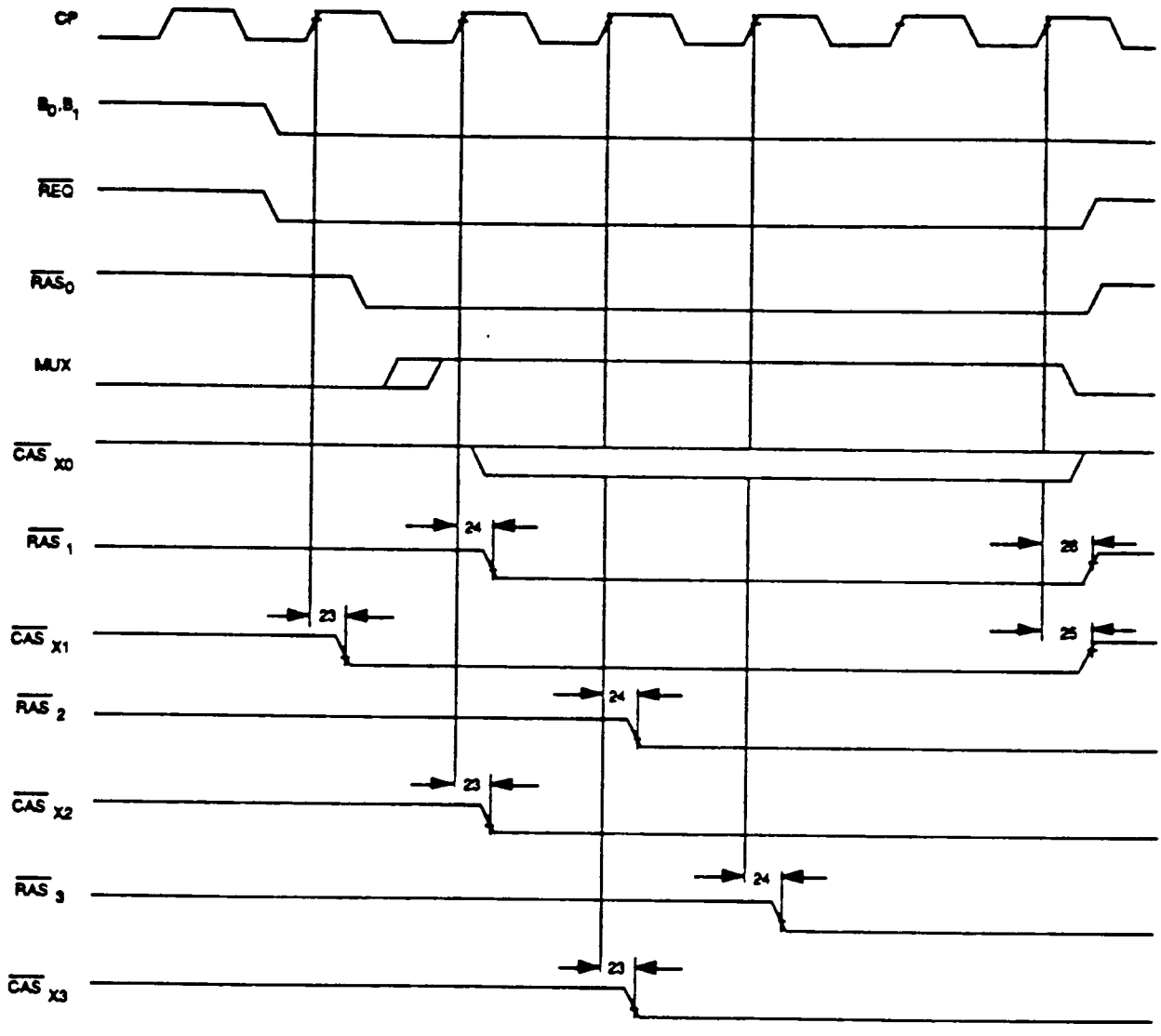
NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=25°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
28	Propagation delay $\overline{RAS}$(↓) to MUX(↑)	HLDROW = 1	-1	0.5	2	-1.5	2.5	ns
29	Propagation delay $\overline{RAS}$(↓) to MUX(↑)	HLDROW = 0	1/2tcp-3.5	1/2tcp-1.5	1/2tcp	1/2tcp-1.5	1/2tcp+2.5	ns
30	Propagation delay MUX(↑) to $\overline{CAS}$(↓)	HLDROW = 1	1tcp-1.5	1tcp+0.5	1tcp+2	1tcp-2.5	1tcp+2.5	ns
31	Propagation delay MUX(↑) to $\overline{CAS}$(↓)	HLDROW = 0	1/2tcp+0.5	1/2tcp+2	1/2tcp+4.5	1/2tcp-0.5	1/2tcp+5	ns



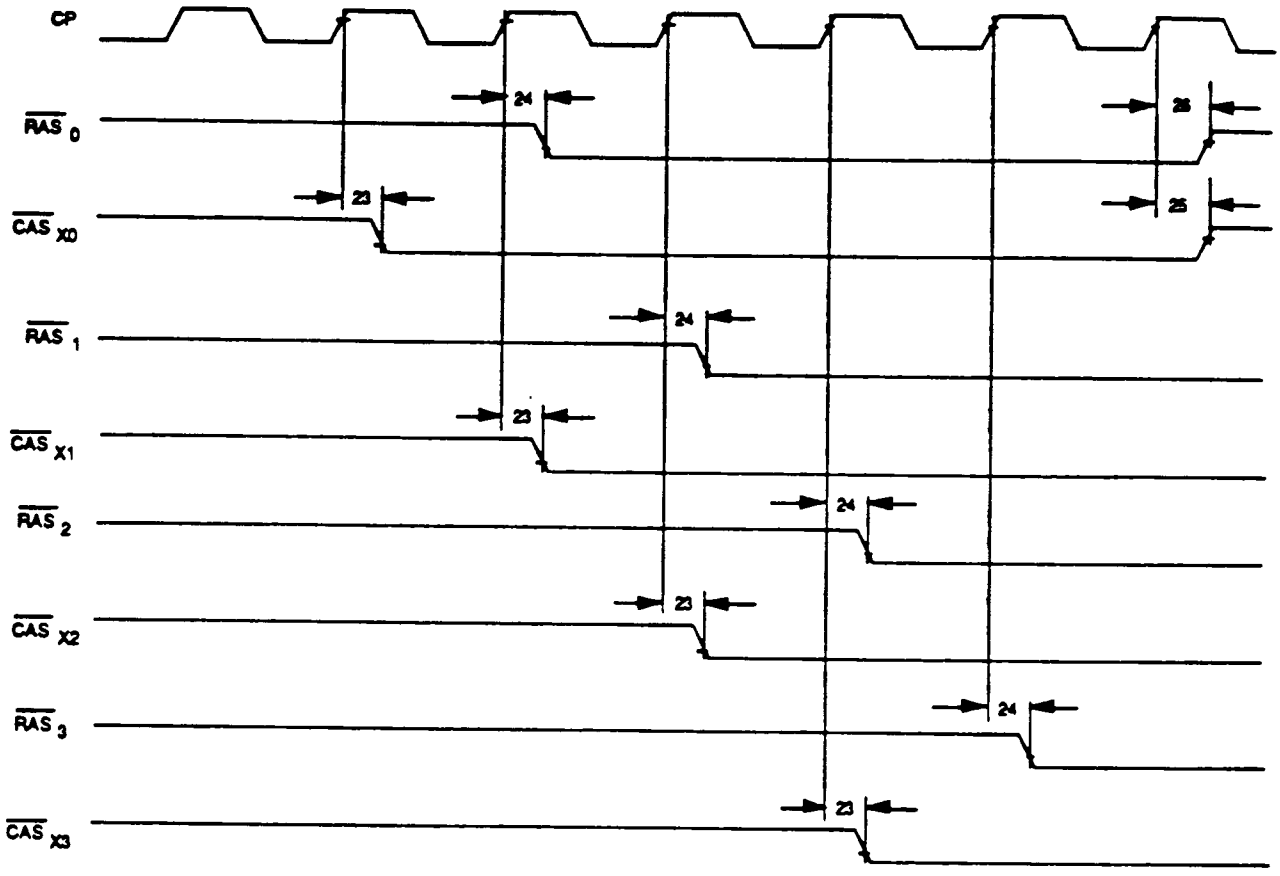
Waveform 1: Burst mode access timing



Waveform 2: Non-Burst mode access timing

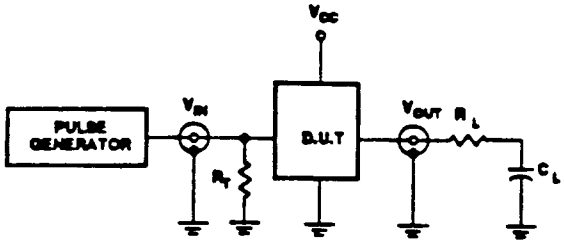


Waveform 3: Refresh cycle timing during $\overline{RAS_0}$ access

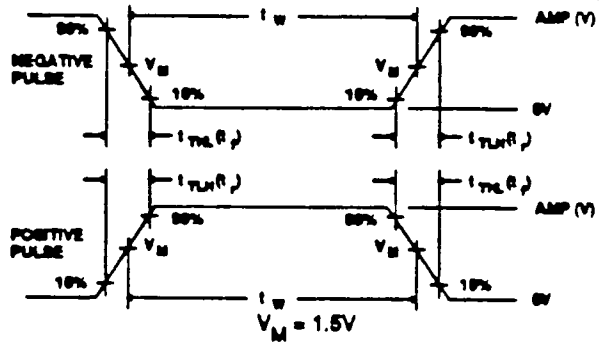


Waveform 4: Refresh cycle timing when memory is not being accessed

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns