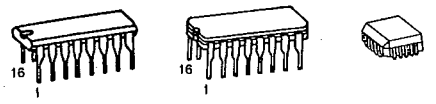
M54/M74HC4102
M54/M74HC4103

HS-C²MOS™ INTEGRATED CIRCUITS

PRELIMINARY DATA

8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS



B1 Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS: M54HCXXXX F1
M74HCXXXX B1
M74HCXXXX F1
M74HCXXXX C1

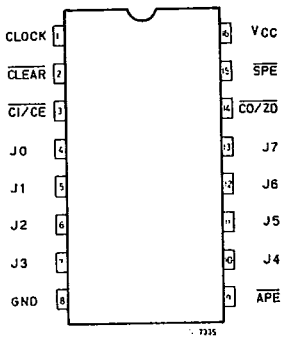
DESCRIPTION

The M54/74HC4102-4103 are high speed CMOS 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The HC4102, and HC4103 consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The HC4102 is configured as two cascaded 4-bit BCD counters, and the HC4103 contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETEC ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the J input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the J inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. J Inputs J0-J7 represent two 4-bit BCD words for the HC4102 and a single 8-bit binary word for the HC4103. When the CLEAR ($\overline{CLR}$ input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the HC4102 and 255_{10} for the HC4103 regardless of the state of any other input. The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long. The HC4102 and HC4103 may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode.

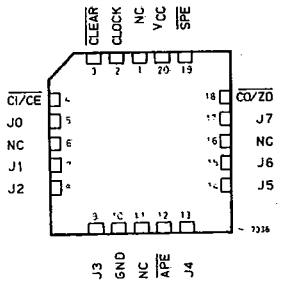
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

PIN CONNECTIONS
(top view)



Dual in line

CHIP CARRIER



NC = No Internal Connection

M54/M74HC4102
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FEATURES

- High Speed
  f_{MAX} = 47 MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible
  with 4102B 4103B

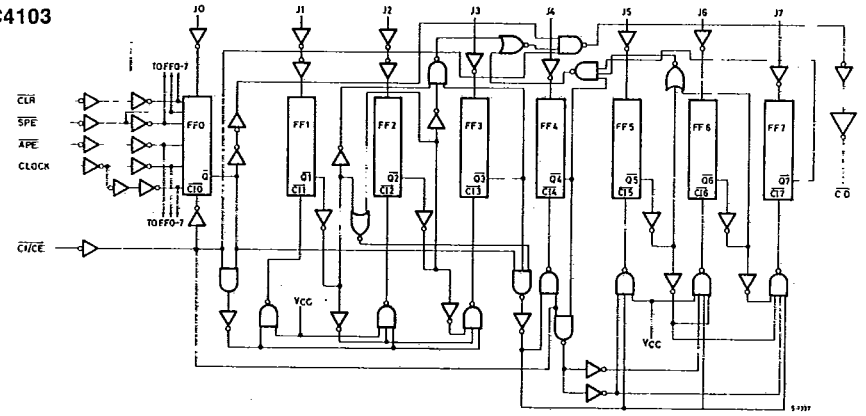
TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	CI/$\overline{CE}$		
H	H	H	H	Synchronous	Inhibit counter
H	H	H	L		Count down
H	H	L	*		Preset on next positive clock transition
H	L	*	*	Asynchronous	Preset asynchronously
L	*	*	*		Clear to maximum count

*: Don't care

LOGIC DIAGRAM

HC4103



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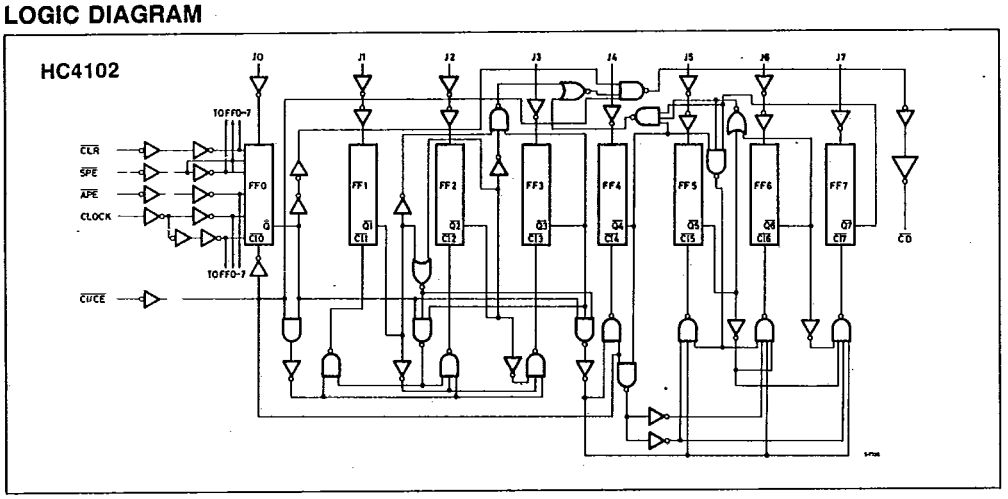
LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
Tstg	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

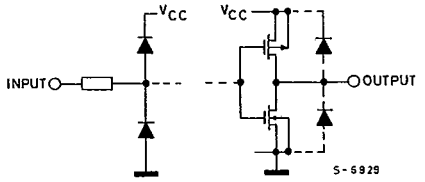
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000	ns
		4.5V	0 to 500	
		6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40		80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT



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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-$\overline{CO}$) $\overline{SPE}$ = H		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-$\overline{CO}$) $\overline{SPE}$ = L		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{APE}$-$\overline{CO}$)		31	48	ns
t_{PLH}	Propagation Delay Time ($\overline{CL}$-$\overline{CO}$)		23	36	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CI}$-$\overline{CO}$)		11	18	ns
f_{MAX}	Maximum Clock Frequency	30	47		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)		8	15	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CL}$, $\overline{APE}$)		8	15	ns
t_s	Minimum Set-up Time ($\overline{SPE}$)		8	15	ns
t_s	Minimum Set-up Time ($\overline{CI}$)		18	30	ns
t_h	Minimum Hold Time (All Inputs)		—	5	ns
t_{REM}	Minimum Removal Time ($\overline{CL}$, $\overline{APE}$)		8	15	ns
t_s	Minimum Set-up Time (J0.....J7)		8	15	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{PLH} t_{PHL}	Propagation Delay Time (CK-$\overline{CO}$) $\overline{SPE}$ = H	2.0		—	80	195	—	235			ns
		4.5		—	25	39	—	47			
		6.0		—	22	34	—	40			
t_{PLH} t_{PHL}	Progation Delay Time (CK-$\overline{CO}$) $\overline{SPE}$ = L	2.0		—	80	195	—	235			ns
		4.5		—	25	39	—	47			
		6.0		—	22	34	—	40			

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Progation Delay Time (APE - $\overline{CO}$)	2.0		—	120	280	—	340			ns
		4.5		—	36	56	—	68			
		6.0		—	31	48	—	58			
t_{PLH}	Progation Delay Time ($\overline{CL}$ - $\overline{CO}$)	2.0		—	81	210	—	255			ns
		4.5		—	27	42	—	51			
		6.0		—	23	36	—	44			
t_{PLH} t_{PHL}	Progation Delay Time ($\overline{CI}$ - $\overline{CO}$)	2.0		—	38	115	—	140			ns
		4.5		—	14	23	—	28			
		6.0		—	12	20	—	24			
f_{MAX}	Maximum Clock Frequency	2.0		5	10	—	4	—			MHz
		4.5		25	40	—	20	—			
		6.0		29	47	—	23	—			
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	23	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
$t_{W(L)}$	Minimum Pulse Width ($\overline{CL}$, APE)	2.0		—	27	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time ($\overline{SPE}$)	2.0		—	27	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time $\overline{CI}$	2.0		—	68	150	—	180			ns
		4.5		—	18	30	—	36			
		6.0		—	16	26	—	31			
t_h	Minimum Hold Time (All inputs)	2.0		—	—	5	—	6			ns
		4.5		—	—	5	—	6			
		6.0		—	—	5	—	6			
t_{REM}	Minimum Removal Time ($\overline{CL}$, APE)	2.0		—	17	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time (J0.....J7)	2.0		—	21	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance			—		—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$