SN54AS4374, SN74AS4374
8-BIT DUAL-RANK SYNCHRONIZER

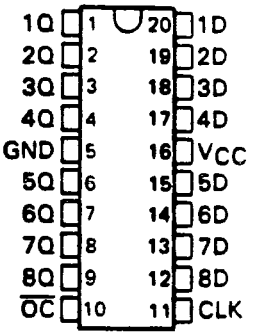
TEXAS INSTR {LOGIC} 06E D

T-52-33-90

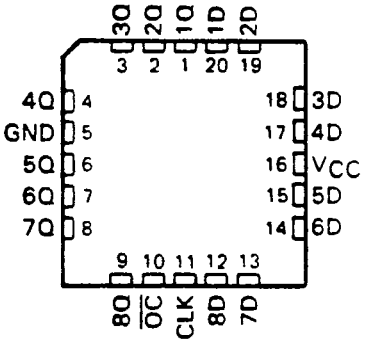
D3081, APRIL 1988

- **Specifically Designed for Data Synchronization Applications**
- **Improved Metastable Characteristics Provide Greater System Reliability**
- **3-State Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS4374 . . . JT PACKAGE
SN74AS4374 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS4374 . . . FK PACKAGE
(TOP VIEW)



description

The 'AS4374 is an eight-bit dual-rank synchronizer circuit designed specifically for data synchronization applications where the normal setup and hold time specifications are frequently violated.

Synchronization of two digital signals operating at different frequencies is a common system problem. This problem is typically solved by synchronizing one of the signals to the local clock through a flip-flop. This solution, however, causes the setup and hold time specifications associated with the flip-flop to be violated. When setup or hold time of a flip flop is violated, the output response is uncertain. A flip-flop is metastable if its output hangs up in the region between V_{IL} and V_{IH}. The metastable condition lasts until the flip-flop recovers into one of its two stable states. With conventional flip-flops, this recovery time can be longer than the specified maximum propagation delay.

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OC}$	CLK	D	Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q_0

The problem of metastability is typically solved by adding an additional layer of synchronization. This type of dual ranking is employed in the 'AS4374. The probability of the second stage entering the metastable state is exponentially reduced by this dual-ranking architecture. The 'AS4374 provides a one-chip solution for system designers in asynchronous applications.

The SN54AS4374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS4374 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

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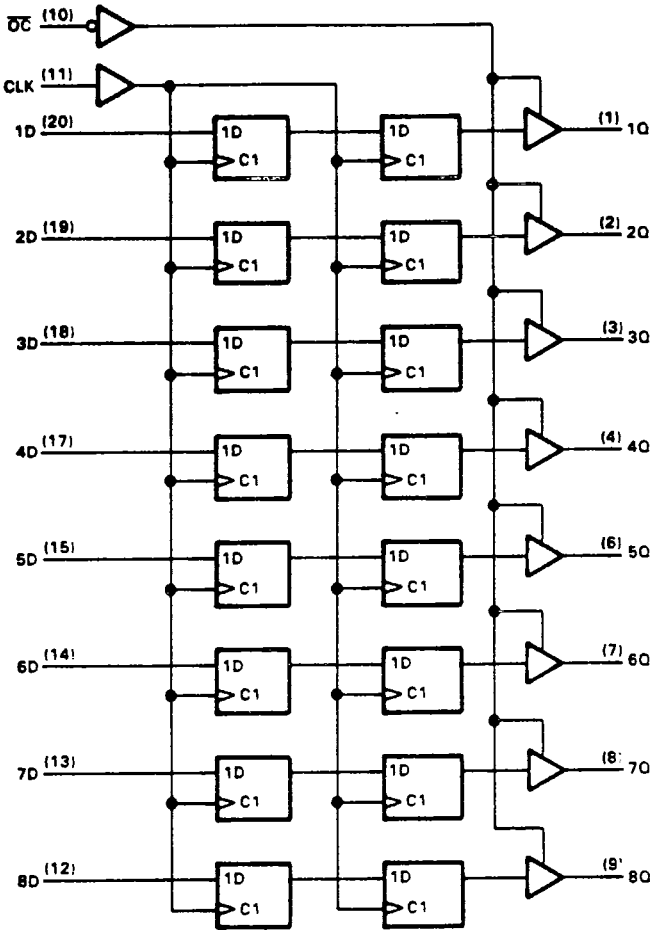
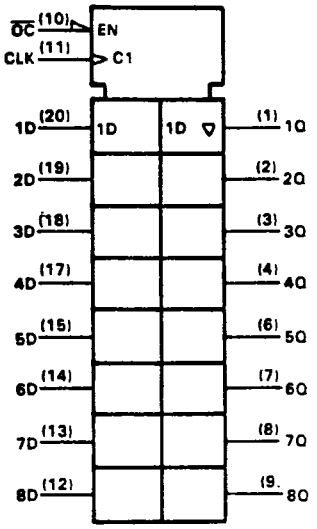
logic diagram (positive logic)



logic symbol†



† This symbol is in acordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS4374 . . . . . −55°C to 125°C
SN74AS4374 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS4374			SN74AS4374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−24	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		100	MHz
t_w	Pulse duration	CLK high	5			5			ns
		CLK low	5			5			
t_{su}	Setup time, data before CLK↑		5			5			ns
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† The data setup and hold time is specified for synchronous operation. These parameters also help guarantee overall speed characteristics of the device. Since production testing for metastibility is impossible, conformance to conventional switching characteristics verifies metastable-failure resistance.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS4374			SN74AS4374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −18 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OH} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V		−0.1	−0.2		−0.1	−0.2	mA
	$\overline{OC}$				−0.2	−0.4		−0.2	−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	$\overline{OC}$ high					105	150	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS4374		SN74AS4374		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	CLK	Q					ns
t_{PHL}							
t_{ena}	$\overline{OC}$	Q					ns
t_{dis}	$\overline{OC}$	Q					ns

Note 1: Load circuit and voltage waveforms are shown in Section 1 of the *AS/ALS Logic Data Book*, 1986.

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