CH9001
High performance PC Clock Generator

FEATURES

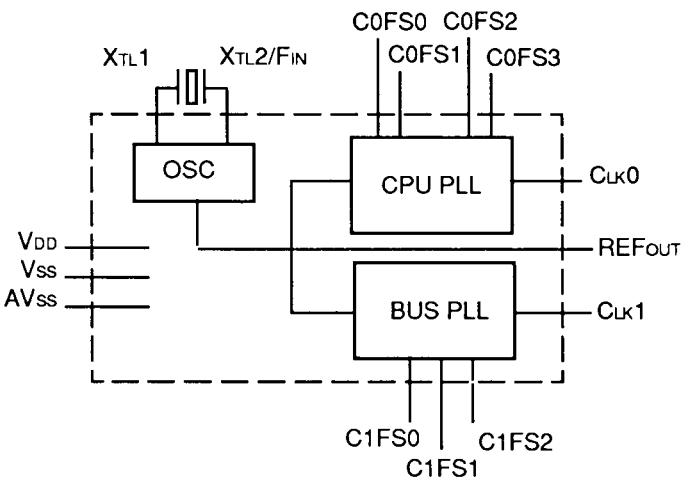
- No external loop filter components.
- Synthesizes popular P.C. frequencies from 1.8432 MHz to 80.0 MHz.
- Single 14.318MHz Source
- Supports XT, 286, 386 and 486 designs
- Designed for 0.001MHz accuracy
- TTL or CMOS output option
- High performance, low power CMOS
- Available in 16 pin plastic DIP or SOIC

DESCRIPTION

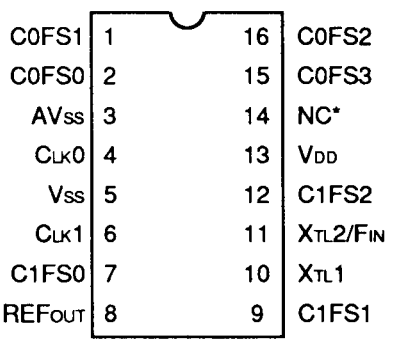
The ***Chrontel*** CH9001 is a high performance dual frequency synthesizer designed specifically for applications in personal computing (P.C.) systems. The CH9001 uses the stable 14.31818 MHz reference available on the motherboard to generate the CPU and BUS clocks used in a typical system, thereby elminating expensive clock packages. The precision frequencies are selected by externally latching the Frequency Select (FS) inputs. Output frequency accuracy has been designed for 0.001MHz plus the frequency tolerance of the crystal.

System cost reductions are achieved by eliminating expensive high frequency clocks, reducing component count to achieve the same function and reducing board layout space. These reductions result in faster manufacturing throughput, reduced logistics support and higher systems reliability.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



* Pin 14 should be left open or connected to Vss

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to Ground	-0.5 to +7.0	V
T_B	Ambient Temperature under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS (0 to +70 °C, V_{DD} = 5V ±10%)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN.	NOM.	MAX.	UNIT
V_{OH}	Output High Voltage	V_{DD}=4.5V, I_{OH}= -4.0mA	2.4			V
V_{OL}	Output Low Voltage	V_{DD}=4.5V, I_{OL}= 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{LI}	Input Leakage	GND-V_{IN}-V_{CC}	-10		10	µA
I_{OH}	Output Source	V_{OH}= 2.4V			- 4	mA
I_{OL}	Output Sink	V_{OL}= 0.4V			8	mA
I_{DD}	Operating Current	F_{OUT}= f MAX.		20		mA

AC CHARACTERISTICS (0 to +70 °C, V_{DD} = 5V ±10%)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN.	NOM.	MAX.	UNIT
F_{OSC}	Crystal Frequency	Parallel Resonant (C_L=20pF)		14.318		MHz
F_{OUT}	Output Frequency	C_{LK}0, C_{LK}1 Output			80.0	MHz
T_{OH}	Output Rise	C_{OUT}= 25pF, 0.4V-2.4V (TTL)			3	ns
T_{OL}	Output Fall	C_{OUT}= 25pF, 0.4V-2.4V (TTL)			3	ns
T_{DU}	Duty Cycle	CLK0, CLK1 Output	40	50	60	%

OPERATION

The CH9001 is a high performance dual frequency synthesizer designed to replace expensive clock oscillators in a typical PC motherboard application. The circuit has three clock outputs. REF$_{OUT}$ is generated by an on-chip oscillator and its frequency is 14.318 MHz. The Pierce oscillator causes the crystal to oscillate at its parallel resonance and the equivalent on-chip shunt capacitance presented to the crystal is 20pF. If an external TTL clock reference is available at 14.318 MHz, the oscillator can be bypassed by removing the crystal, shorting X_{TL}1 to ground, and connecting X_{TL}2/F_{IN} to the external reference source. TTL levels are recommended for the external clock if 50% duty cycle is required at FEF_{OUT}.

C_{LK}0 and C_{LK}1 are frequency programmable outputs synthesized by two monolithic phase-locked loops (PLL). Since these PLL's lock on to the 14.318 MHz reference signal, their output frequency is stable against variations in temperature and supply voltage. Frequency resolution of the two PLL's is designed at 2KHz. Frequency accuracy for the CH9001 is 1 KHz plus the frequency tolerance of the crystal. The CH9001 is especially easy to use because it requires no external loop filter, and loop stability is tested at different output frequencies during production test.

The output frequency of the CH9001 spans from 1.25 MHz to 80 MHz. To optimize performance, the voltage controlled oscillator is designed to operate within the first frequency octave only (40 MHz to 80 MHz). Lower frequency octaves are then generated by a digital divider at the VCO output. This output divider is controlled by the ROM and can divide the output frequency by 2^n.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	C0FS1	Input	Frequency Select for Clock0
2	C0FS0	Input	Frequency Select for Clock0
3	AVss		Analog Ground
4	Clk0	Output	Clock 0 Output-CPU
5	Vss		Digital Ground
6	Clk1	Output	Clock 1 Output BUS
7	C1FS0	Output	Frequency Select for Clock1
8	REFout	Output	14.318 MHz crystal reference output
9	C1FS1	Input	Frequency Select for Clock1
10	Xtl1	Input	External crystal input
11	Xtl2/Fin	Input	External crystal input/External Oscillator input
12	C1FS2	Input	Frequency Select for Clock1
13	Vdd		Power supply
14	NC		No Connection connect to ground
15	C0FS3	Input	Frequency Select for Clock0
16	C0FS2	Input	Frequency Select for Clock0

PROGRAMMING

The CH9001 has been internally programmed with precision frequencies corresponding to all of the Intel family of CPUs and the commonly used frequencies for UART, hard disk, AT-BUS or floppy controller. Non-standard CPU frequencies are also available to facilitate elevated frequency burn-in during motherboard manufacturing. Manufacturers suppling several PC product lines can reduce inventory requirements since crystal oscillators of different frequencies can now by replaced with a single part.

Control signals supplied to C0FS<3:0> are used to select one output frequency from the sixteen available for Clk0 while C1FS <2:0> selects one output frequency from the eight available for Clk1. All Frequency Select (FS) inputs have an internal pull-up resistor, therefore the desired frequency is obtained by simply externally strapping the appropriate FS input to ground or by driving the inputs with a standard TTL or CMOS signal.

CH9001CC OUTPUT FREQUENCIES (Tolerance= Crystal Tolerance ±1KHz)

CPU OUTPUTS						BUS OUTPUTS				
Pin Settings				Clk0		Pin Settings			Clk1	
C0FS3	C0FS2	C0FS1	C0FS0	Out (MHz)	Application	C1FS2	C1FS1	C1FS0	Out (MHz)	Application
0	0	0	0	16.000	XT-8	0	0	0	1.8432	UART
0	0	0	1	20.000	XT-10	0	0	1	32.000	AT bus
0	0	1	0	25.000	486-25	0	1	0	9.6000	WD37C65
0	0	1	1	28.000	486-25 Turbo	0	1	1	12.000	Modem
0	1	0	0	33.333	486-33	1	0	0	11.059	Modem
0	1	0	1	60.000	386-30, SX	1	0	1	8.000	Kbd. cntrlr
0	1	1	0	88.000	386-40 Turbo	1	1	0	24.000	Multi I/O
0	1	1	1	80.000	386-40	**1**	**1**	**1**	**16.000***	**Floppy/AT**
1	0	0	0	36.667	486-33 Turbo					
1	0	0	1	44.000	SX-20 Turbo					
1	0	1	0	73.333	Turbo 33 MHz					
1	0	1	1	55.000	Turbo 25 Mhz					
1	1	0	0	32.000	SX-16					
1	1	0	1	40.000	SX-20					
1	1	1	0	66.667	386-33, SX					
1	**1**	**1**	**1**	**50.000***	**386-25/486-50**					

* Default frequency. All frequency control pins have internal pull ups.

FREQUENCY OPTION

Under special arrangement with ***Chrontel***, the customer can specify up to twenty four (24) frequencies by mask programming the internal ROM for each loop. Sixteen (16) frequencies are available for CLK0 and eight (8) are available for CLK1. The CH9001 spans a frequency range from 1.25MHz to 80MHz.

ORDERING INFORMATION

Part Number	I/O	Package
CH9001Cx-NC	CMOS	300 mil DIP
CH9001Tx-NC	TTL	300 mil DIP
CH9001Cx-SC	CMOS	300 mil SO
CH9001Tx-SC	TTL	300 mil SO

NOTE: x = version number

LAYOUT CONSIDERATIONS

Due to the advance PLL design, no special layout consideration is required by the CH9001. Standard layout practice should be applied to the bypass capacitor and the crystal. To reduce loading capacitance and RF emission, the CH9001 should be placed near the device requiring the highest frequency.

PACKAGE DIMENSIONS

Package outlines meet JEDEC Standards

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