1. Introduction

1.1. Introduction

The MB89372A Multi-Protocol Controller (MPC) uses three serial data transfer protocols: ASYNC, Character Oriented Protocol (COP), and Bit Oriented Protocol (BOP). To enable high-speed data transfer, the MPC has a built-in DMA controller to directly read and send data from memory or transfer receive data to memory without CPU intervention. In addition, it has an interrupt controller to handle various interrupts generated from the serial interface unit (SIU) and DMA controller (DMAC) unit.

1.2. Features

■ **Two full-duplex communications channels are built in.**

(1) Up to 2Mbps transfer is possible (when operating at 8MHz). (In the loop mode, however, the maximum transfer rates are 1Mbps for NRZ/NRZI code and 666kbps for FM0/FM1/Manchester code. Note that the use of DPLL places restrictions on the maximum transfer rate.)

(2) Send data FIFO (4 bytes), receive data FIFO (8 bytes)

(3) Bit rate generator (one channel per full-duplex communications channel)

- This unit can also be used as an interval timer when it is not used as a bit rate generator.

(4) DPLL (one channel per full-duplex communications channel)

(5) ASYNC mode

- The transfer clock is selected from bit rate x1, x16, x32, and x64. (When x1 is selected, the receive data and receive clock must be synchronized.)
- The length of one character is selected from 5, 6, 7 or 8 bits.
- The stop bit length is selected from 1, 1.5 or 2 bits.
- Parity, overrun, and framing errors are detected.
- Break transmission/automatic detection

(6) COP mode

- The sync detection mode is selected from Mono SYNC, Double SYNC, or External SYNC.
- The length of one character is selected from 5, 6, 7 or 8 bits.
- CRC can be selected from LRC (exclusively used for odd numbers), non-inversion of CRC16-0, inversion of CRC16-1, non- inversion of CCITT-0, and inversion of CCITT-1. (Specification by program is required to eliminate specific data from calculations, determine transmission timing, and display check results.)
- The serial data code is selected from NRZ, NRZI, FM0, FM1, or Manchester.
- Parity, overrun, and underrun errors are detected.
- The SYNC character is automatically erased.

(7) BOP mode

- One-byte or two-byte address fields can be automatically compared.
- CRC can be selected from non-inversion of CRC16-0, inversion of CRC16-1, non- inversion of CCITT-0, and inversion of CCITT-1.
- The serial data code is selected from NRZ, NRZI, FM0, FM1 or Manchester.
- CRC, overrun, short frame errors, and underrun errors are detected.
- Idle detection.

(8) LOOP mode (This mode is for the secondary LOOP station; the primary LOOP station uses the BOP mode.)

- One-byte or two-byte address fields can be automatically compared.
- CRC can be selected from non-inversion of CRC16-0, inversion of CRC16-1, non- inversion of CCITT-0, and inversion of CCITT-1.
- The serial data code is selected from NRZ, NRZI, FM0, FM1 or Manchester.
- CRC, overrun, short frame, underrun, and loop errors are detected.
- Idle detection.

■ **Four DMA controller channels are built in.**

(1) Descriptor chain method

(2) The DMA output address is selected from 24 or 16 bits.

■ **An interrupt controller is built in.**

(1) Operate as a slave to the MB89259A.

■ **Register direct access method**

■ **CMOS process**

■ **64-pin SH-DIP, 64-pin QFP**

1.3. Block Diagram

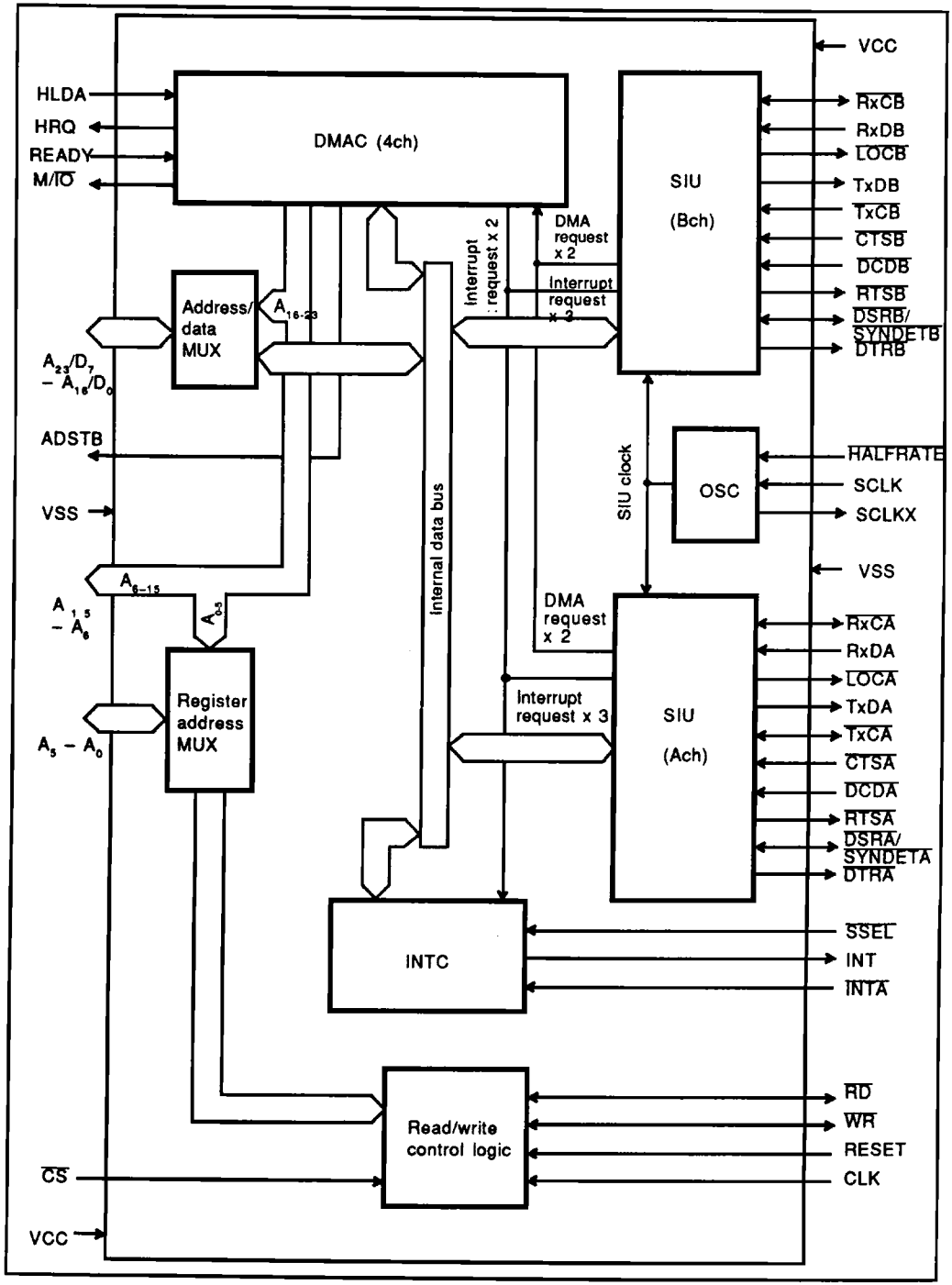


Figure 1-1. Block Diagram of MPC

1.4. Electrical Characteristics

1.4.1. Absolute Maximum Ratings

Parameter	Symbol	Rated value	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V
Ambient temperature	T_A	0 to +70	°C
Storage temperature	T_{stg}	−55 to +150	°C

1.4.2. Recommended Operating Conditions

Supply voltage V_{CC} = +5V ± 10%

V_{SS} = 0V (Voltages are referenced to V_{SS}.)

Ambient temperature T_A = 0 to 70°C

1.4.3. DC Characteristics (T_A = 0 to 70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V)

Parameter		Symbol	Test Conditions	Min.	Max.	Unit
Supply voltage	When operating	I_{CC}	Output open, input 0V or V_{CC}, when operating at 8MHz		40	mA
	When power saving	I_{CCPWS}	Output open		20	µA
Input leakage current		I_{ILK}	$0_V \le V_{IN} \le V_{CC}$		±10	µA
Output leakage current		I_{OKL}	$0_V \le V_{OUT} \le V_{CC}$		±10	µA
LOW input voltage		V_{IL}		−0.3	0.8	V
HIGH input voltage		V_{IH}		2.0	V_{CC}+0.3	V
Output voltage		V_{OL}	I_{OL} = 2.5mA		0.4	V
Output voltage		V_{OH}	I_{OH} = −2.5mA	3.0		V
			I_{OH} = −100µA	V_{CC}−0.4		
CLK pin LOW input voltage		V_{C11L}		−0.3	0.6	V
CLK pin HIGH input voltage		V_{C11H}		3.9	V_{CC}+0.3	V
SCLK pin LOW input voltage		V_{C21L}		−0.3	0.2 x V_{CC}	V
SCLK pin HIGH input voltage		V_{C21H}		0.8 x V_{CC}	V_{CC}+0.3	V

1.4.4. Pin Capacitance (T_A = 25°C; V_{CC} = 0V)

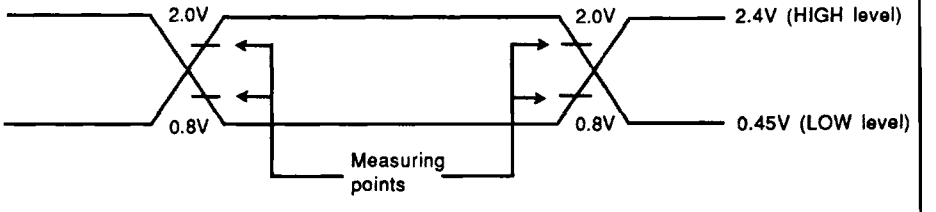
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	f_c = 1 MHz		20	pF
Output capacitance	C_{OUT}			20	pF
Input/output capacitance	$C_{I/O}$			20	pF

1.4.5. Oscillation Characteristics (T_A = 0 to 70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V)

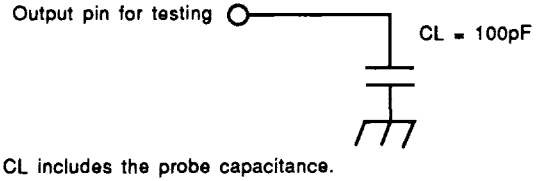
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
External clock period	t_{SCLK}	SCLKX pin output open	125		ns
External clock LOW time	t_{SCLKL}		55		
External clock HIGH time	t_{SCLKH}		50		
Quartz oscillator frequency	f_{XSCLK}	Must be within the range of duty 40-60%.	2	16	MHz
Quartz oscillator stabilizing capacitance	C_{XSCLK}		TYP. 20		pF
	C_{XSCLKX}		TYP. 20		

1.4.6. AC Characteristics (T_A = 0 to 70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V)

AC Test Waveform



AC test load circuit



CL includes the probe capacitance.

Timing Requirements

Parameter		Symbol	Min.	Max.	Unit
Clock period		t_{CK}	125	———	ns
Clock LOW time		t_{CKL}	55	———	
Clock HIGH time		t_{CKH}	50	———	
Clock rise time, fall time		t_r, t_f	———	10	
Reset pulse duration		t_{RESET}	$5t_{CK}$	———	
Read pulse duration (host read)		t_{RR}	$1t_{CK}$ +20	———	
Address setup time (relative to $\overline{RD}$ ↓)		t_{AR}	30	———	
Address hold time (relative to $\overline{RD}$ ↑)		t_{RA}	0	———	
Data delay (relative to $\overline{RD}$ ↓)		t_{DR}	———	120	
Data hold time (relative to $\overline{RD}$ ↑)		t_{RD}	10	75	
Write pulse duration (host write)		t_{WW}	$1t_{CK}$ +20	———	
Address setup time (relative to $\overline{WR}$ ↓)		t_{AW}	30	———	
Address hold time (relative to $\overline{WR}$ ↑)		t_{WA}	0	———	
Data setup time (relative to $\overline{WR}$ ↑)		t_{DW}	100	———	
Data hold time (relative to $\overline{WR}$ ↑)		t_{WD}	0	———	
Recovery time during data access	After $\overline{RD}$ ↑, $\overline{WR}$ ↑	t_{ACCS}	$3t_{CK}$ +20	———	

Timing Requirements (Continued)

Parameter	Symbol	Min.	Max.	Unit
HRQ valid delay time (relative to CLK ↓)	t_{DHRQ1}	———	100	ns
HRQ invalid delay time (relative to CLK ↓)	t_{DHRQ2}	———	100	
HLDA set time (relative to CLK ↑)	t_{DHLDA}	30	———	
STB valid delay time (relative to CLK ↑)	t_{DSTB1}	———	90	
STB invalid delay time (relative to CLK ↑)	t_{DSTB2}	———	95	
M/$\overline{IO}$ output delay time (relative to CLK ↓)	t_{DMI01}	———	100	
M/$\overline{IO}$ float delay time (relative to CLK ↓)	t_{DMI02}	———	100	
Address output delay time (relative to CLK ↓)	t_{DADD1}	———	100	
Address float delay time (relative to CLK ↓)	t_{DADD2}	———	100	
HIGH address output delay (relative to CLK ↓)	t_{DHADD1}	———	100	
HIGH address float delay (relative to CLK ↓)	t_{DHADD2}	———	100	
HIGH address setup (relative to ADSTB ↓)	t_{DHADD3}	t_{CKL} – 25	———	
HIGH address hold (relative to ADSTB ↓)	t_{DHADD4}	t_{CKH} – 15	———	
DMA data input setup (relative to CLK ↓)	t_{DDIS}	30	———	
DMA data input hold (relative to $\overline{RD}$ ↑)	t_{DDIH}	0	———	
DMA data output delay (relative to CLK ↓)	t_{DDOS}	———	100	
DMA data output hold (relative to CLK ↓)	t_{DDOH1}	———	100	
$\overline{RD}$ output delay time (relative to CLK ↓)	t_{DRD1}	———	100	
$\overline{RD}$ Hi-Z delay time (relative to CLK ↓)	t_{DRD2}	———	100	
$\overline{RD}$ valid delay time (relative to CLK ↑)	t_{DRD3}	———	75	
$\overline{RD}$ invalid delay time (relative to CLK ↑)	t_{DRD4}	———	75	
$\overline{WR}$ output delay time (relative to CLK ↓)	t_{DWR1}	———	100	
$\overline{WR}$ Hi-Z delay time (relative to CLK ↓)	t_{DWR2}	———	100	
$\overline{WR}$ valid delay time (relative to CLK ↑)	t_{DWR3}	———	100	
$\overline{WR}$ invalid delay time (relative to CLK ↑)	t_{DWR4}	———	100	
READY setting setup time (relative to CLK ↑)	t_{DRDY1}	20	———	
READY setting hold time (relative to CLK ↑)	t_{DRDY2}	40	———	

Timing Requirements (Continued)

Parameter	Symbol	Min.	Max.	Unit
M/IO setup time (relative to $\overline{RD}$ ↓)	t_{DMIO3}	t_{CKL} – 35	———	ns
M/IO hold time (relative to $\overline{RD}$ ↑)	t_{DMIO4}	t_{CKH} – 20	———	
M/IO setup time (relative to $\overline{WR}$ ↓)	t_{DMIO5}	t_{CKL} – 20	———	
M/IO hold time (relative to $\overline{WR}$ ↑)	t_{DMIO6}	t_{CKH} – 20	———	
Address setup time (relative to $\overline{RD}$ ↓)	t_{DADD3}	t_{CKL} – 35	———	
Address hold time (relative to $\overline{RD}$ ↑)	t_{DADD4}	t_{CKH} – 10	———	
Address setup time (relative to $\overline{WR}$ ↓)	t_{DADD5}	t_{CKL} – 15	———	
Address hold time (relative to $\overline{WR}$ ↑)	t_{DADD6}	t_{CKL} – 20	———	
Data setup time (relative to $\overline{WR}$ ↓)	t_{DDOS2}	t_{CKL} – 25	———	
Data hold time (relative to $\overline{WR}$ ↑)	t_{DDOH2}	t_{CKH} – 20	———	

Timing Requirements (Continued)

Parameter	Symbol	Min.	Max.	Unit
$\overline{INTA}$ pulse duration	t_{IINTA1}	$1t_{CK}$ + 20	———	ns
$\overline{INTA}$ recovery time	t_{IINTA2}	$2t_{CK}$ + 20	———	
$\overline{SSEL}$ setup time (relative to $\overline{INTA}$ ↓)	t_{ISSEL}	30	———	
Interrupt vector delay time (relative to $\overline{INTA}$ ↓)	t_{IVCT1}	———	120	
Interrupt vector delay time (relative to $\overline{INTA}$ ↑)	t_{IVCT2}	10	120	
INT mask delay (relative to $\overline{WR}$ ↓)	t_{IINTM1}	———	100	
INT mask clear delay (relative to $\overline{WR}$ ↑)	t_{IINTM2}	———	$6t_{CK}$	
INT delay time (relative to $\overline{INTA}$)	t_{IIAINT}	———	$2t_{CK}$	
INT ↑ delay (relative to CLK ↓)	t_{DDMAI}	———	100	
INT ↑ delay (relative to Port ↓↑)	t_{SPORTI}	———	$6t_{CK}$	
INT ↑ delay (relative to $\overline{TxC}$ ↓)	$t_{STXRDYI}$	———	$8t_{CK}$	
INT ↑ delay (relative to $\overline{TxC}$ ↓)	t_{STXUI}	———	$5t_{CK}$	
INT ↑ delay (relative to $\overline{TxC}$ ↓)	t_{SLATEI}	———	$6t_{CK}$	
INT ↑ delay (relative to $\overline{RxC}$ ↑) note 1)	$t_{SRXRDYI}$	———	$10t_{CK}$	
INT ↑ delay (relative to $\overline{RxC}$ ↑)	t_{SLOCI}	———	$11t_{CK}$	
INT ↑ delay (relative to $\overline{RxC}$ ↑)	t_{SLERI}	———	$5t_{CK}$	
INT ↑ delay (relative to $\overline{RxC}$ ↑)	t_{SGAPI}	———	$6t_{CK}$	
INT ↑ delay (relative to $\overline{RxC}$ ↑)	t_{SIDLI}	———	$7t_{CK}$	
INT ↑ delay (relative to $\overline{RxC}$ ↑)	t_{SSYNI}	———	$9t_{CK}$	
INT ↑ delay (relative to SCLK ↑)	t_{SBRGI}	———	$7t_{CK}$ + 250	
INT ↑ delay (relative to SCLK ↓)	t_{SDPLLI}	———	$7t_{CK}$ + 250	

Note 1: Interrupt timing due to RxRDY, receive errors (CRCER/PER, OER, SFER/FER), and frame end (EOF/EOB, ADET, BDET).

Timing Requirements (Continued)

Parameter	Symbol	Min.	Max.	Unit
INT ↓ delay (relative to $\overline{WR}$ ↑ -DCR0 to 3)	t_{DDCRI}		$4t_{CK}$	ns
INT ↓ delay (relative to $\overline{WR}$ ↑ -MCR)	t_{SMCRI}		$5t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -MSR)	t_{SMSRI}		$5t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -BPCR)	t_{SBPCRI}		$5t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -BPSR)	t_{SBPSRI}		$5t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -RxCR)	t_{SRXCRI}		$6t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -RxSR0)	$t_{SRXSR0I}$		$5t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -RxRS1)	$t_{SRXSR1I}$		$5t_{CK}$	
INT delay (relative to $\overline{WR}$ ↑ -RxIER)	$t_{SRXIERI}$		$5t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -TxSR)	t_{STXSRI}		$5t_{CK}$	
INT delay (relative to $\overline{WR}$ ↑ -TxIER)	$t_{STXIERI}$		$5t_{CK}$	
INT ↓ delay (relative to $\overline{WR}$ ↑ -SDR)	$t_{SSDRWI1}$		$6t_{CK}$	
INT ↑ delay (relative to $\overline{WR}$ ↑ -SDR)	$t_{SSDRWI2}$		$7t_{CK}$	
INT ↓ delay (relative to $\overline{RD}$ ↓ -SDR)	$t_{SSDRRI1}$		$6t_{CK}$	
INT ↑ delay (relative to $\overline{RD}$ ↑ -SDR)	$t_{SSDRRI2}$		$7t_{CK}$	

Timing Requirements (Continued)

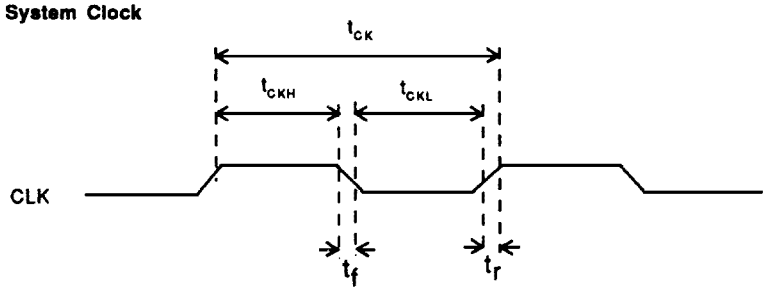
Parameter	Symbol	Min.	Max.	Unit
$\overline{\text{TxCA, B}}$ clock period	t_{STXCW}	$4t_{CK}$ note1)		ns
$\overline{\text{TxCA, B}}$ clock LOW time	t_{STXCL}	$1t_{CK}$ + 62 note2)		
$\overline{\text{TxCA, B}}$ clock HIGH time	t_{STXCH}	$1t_{CK}$ + 62 note2)		
TxDA, B delay	t_{STXDD}		100	
$\overline{\text{LOCA, B}}$ delay	t_{SLOCD}		100	
$\overline{\text{RxCA, B}}$ clock period	t_{SRXCW}	$4t_{CK}$ note1)		
$\overline{\text{RxCA, B}}$ clock LOW time	t_{SRXCL}	$1t_{CK}$ + 62 note2)		
$\overline{\text{RxCA, B}}$ clock HIGH time	t_{SRXCH}	$1t_{CK}$ + 62 note2)		
RxDA, B setup time (relative to $\overline{\text{RxCA, B}}$)	t_{SRXDS}	5		
RxDA, B hold time (relative to $\overline{\text{RxCA, B}}$)	t_{SRXDH}	160		
Port output delay (relative to $\overline{\text{WR}}$ ↑)	t_{SPORTD}		$2t_{CK}$ + 60	
Port input setting (relative to $\overline{\text{RD}}$ ↓)	t_{SPORTF}		$1t_{CK}$ + t_{CKH} + 60	
Internal sync detection delay	t_{SISYN}		$7t_{CK}$	
External sync detection setup	t_{SESYNS}		$2t_{CK}$	
External sync detection hold	t_{SESYNH}	$4t_{CK}$		

Note 1: When in the secondary LOOP station mode, if NRZ or NRZI code → 8 t_{CK}
if FM0, FM1, or Manchester code → 12 t_{CK}

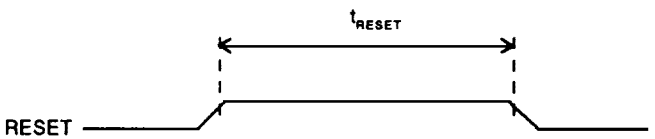
Note 2: When in the secondary LOOP station mode, if NRZ or NRZI code → 3 t_{CK} + 62
if FM0, FM1, or Manchester code → 5 t_{CK} + 62

WAVEFORMS

System Clock

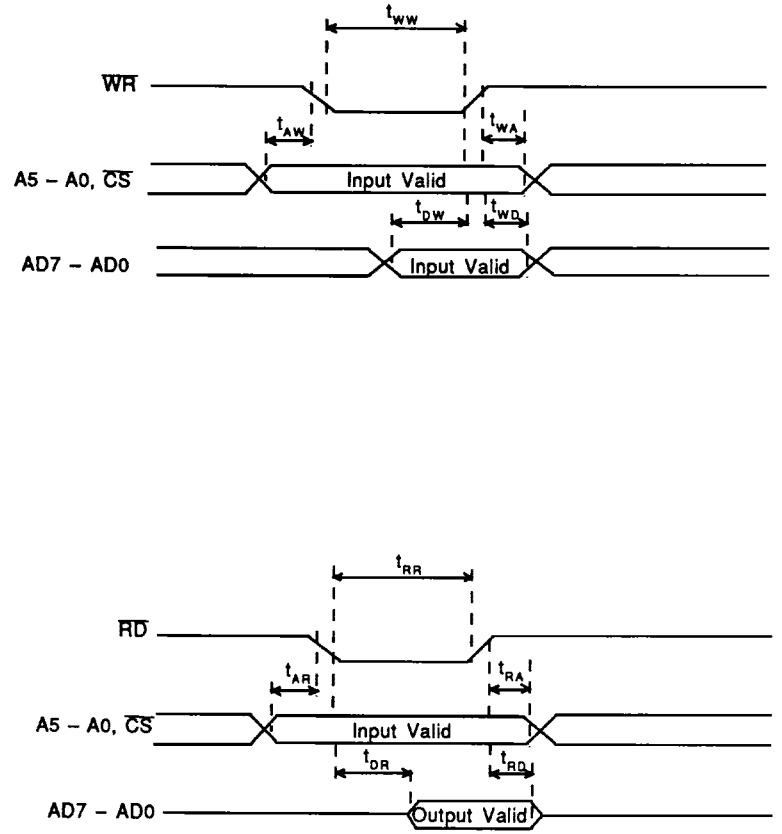


System Reset



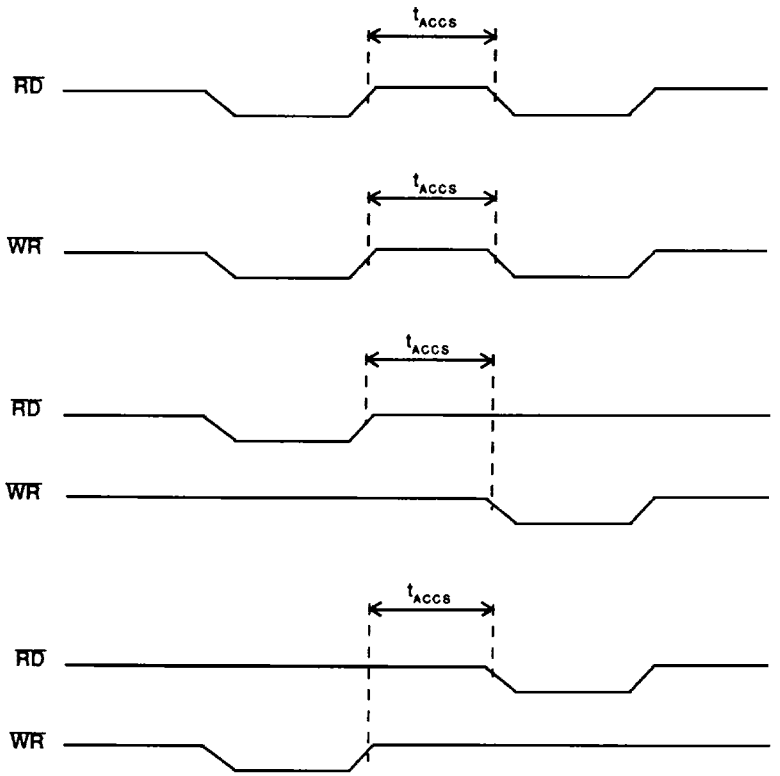
WAVEFORMS (CONTINUED)

Read/Write by Host Access



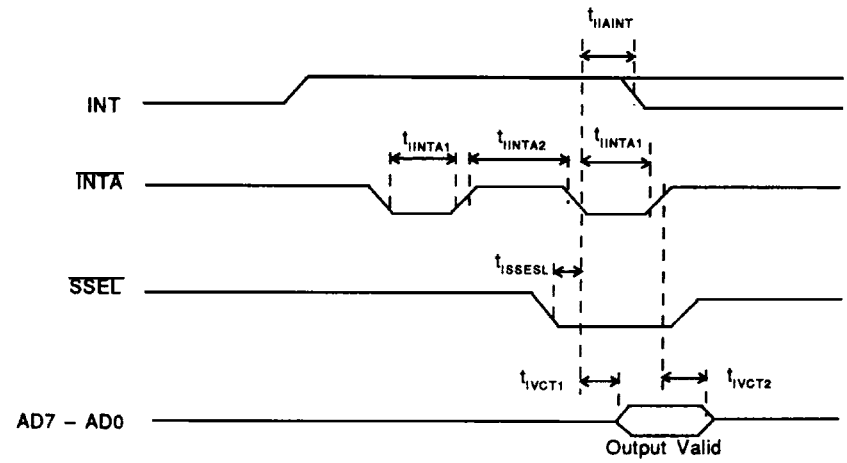
WAVEFORMS (CONTINUED)

Recovery Time during Data Access

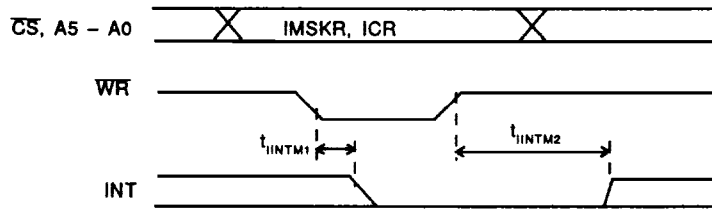


WAVEFORMS (CONTINUED)

Interrupt Acknowledge Cycle

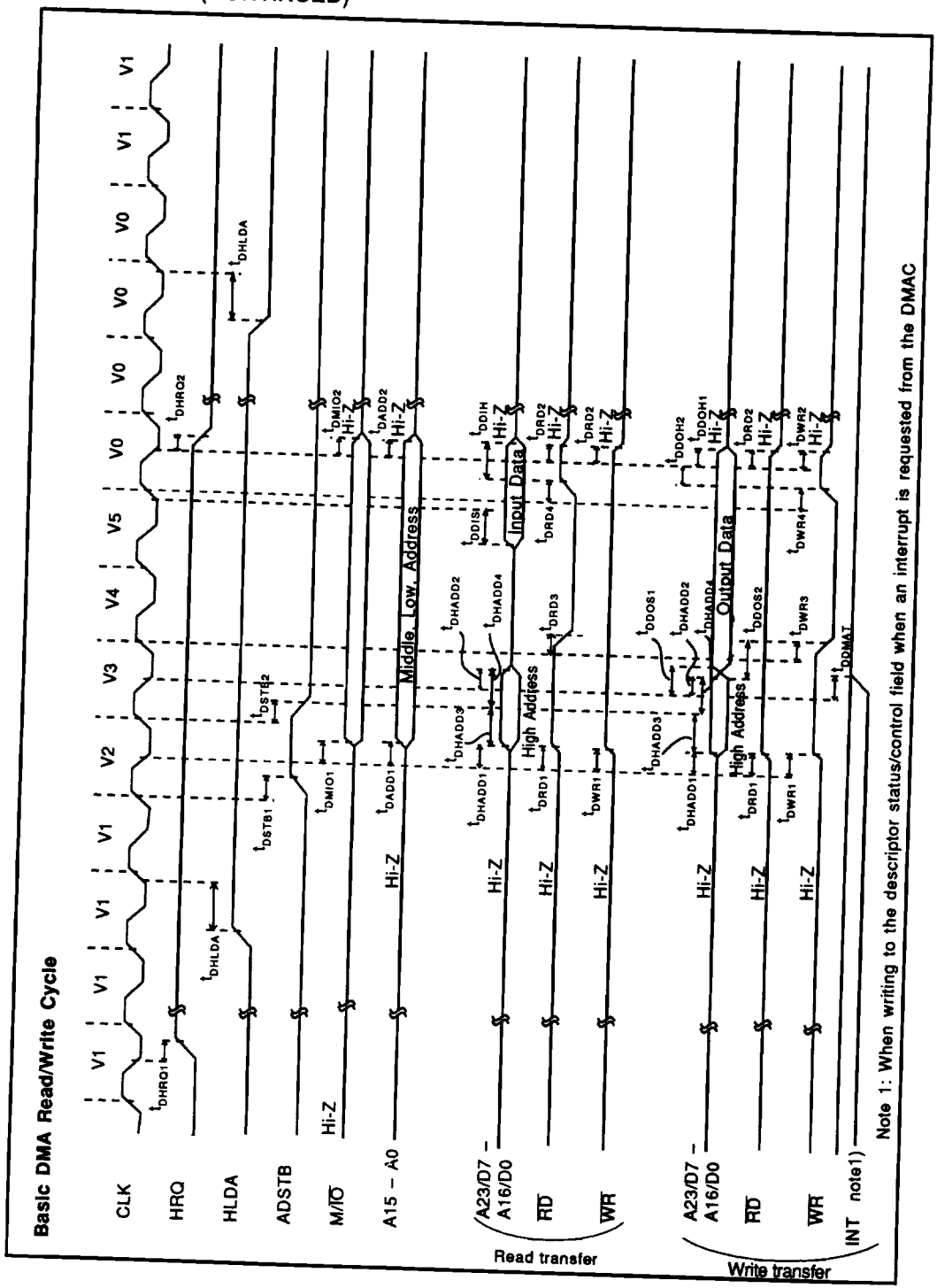


INT Pin Masking

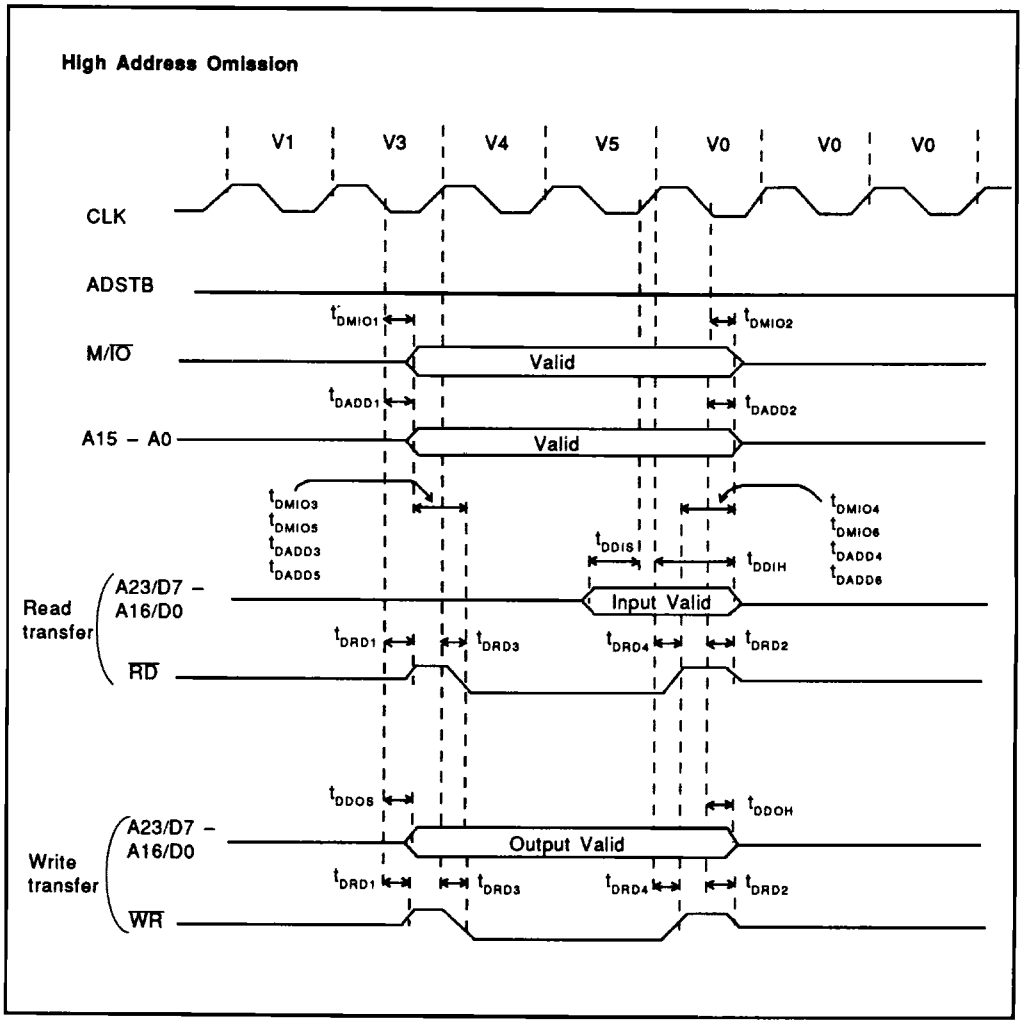


WAVEFORMS (CONTINUED)

Basic DMA Read/Write Cycle

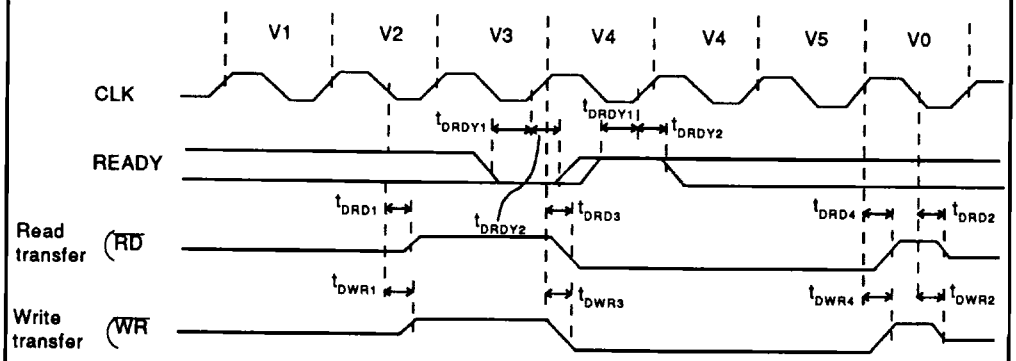


WAVEFORMS (CONTINUED)

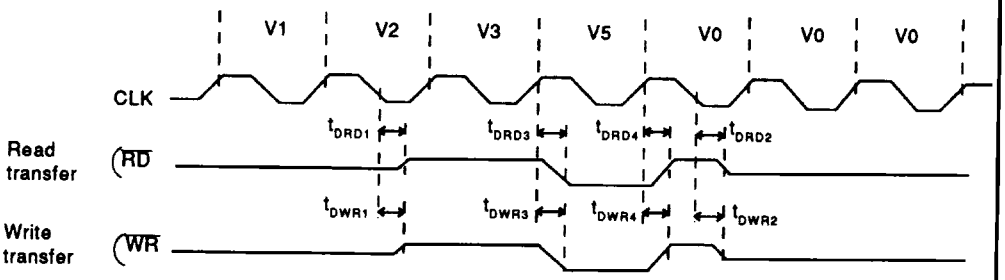


WAVEFORMS (CONTINUED)

READY Input

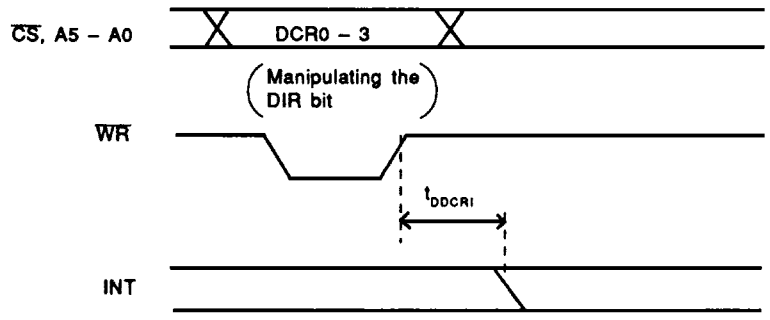


High-speed Transfer Mode

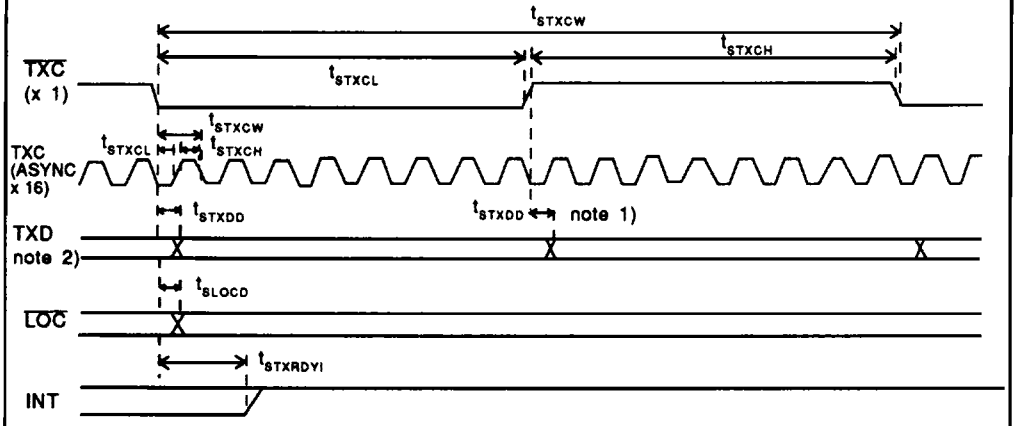


WAVEFORMS (CONTINUED)

Clearing Interrupt Causes in DMAC

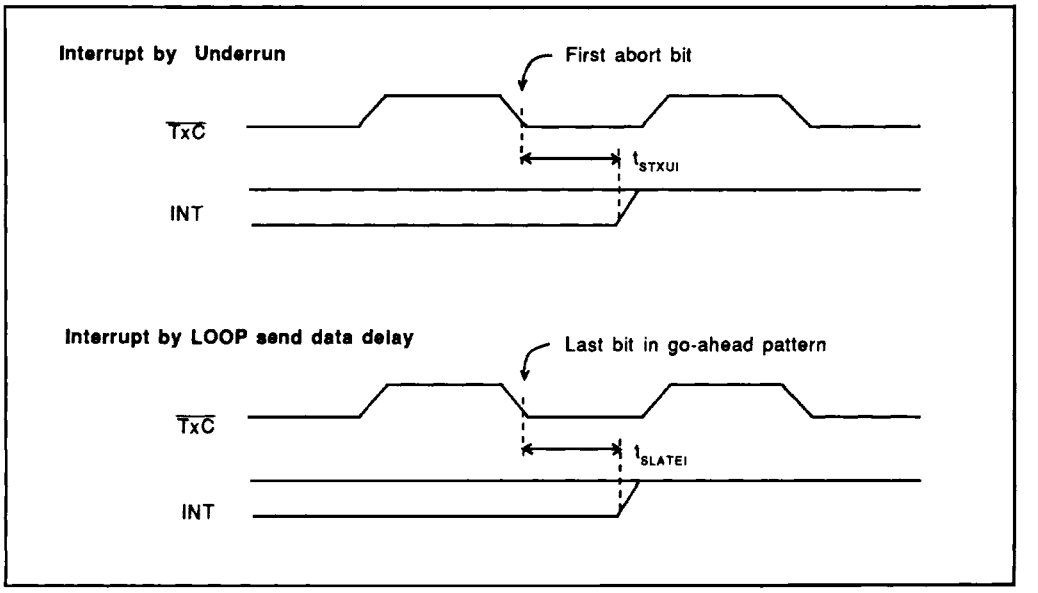


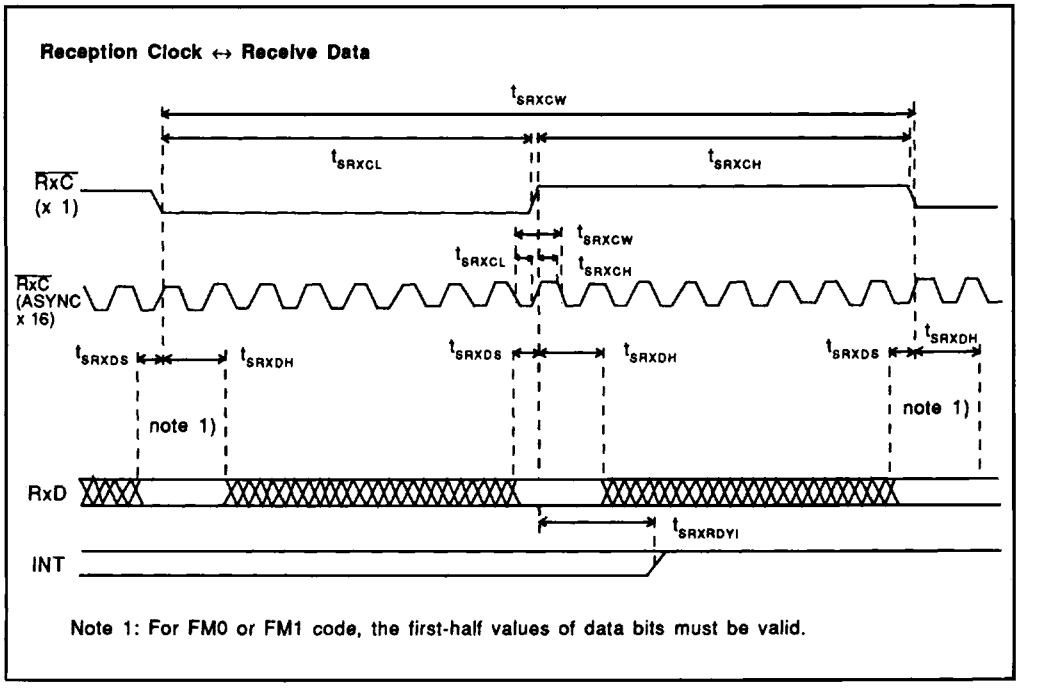
Send Clock ↔ Send Data



Note 1: For NRZ or NRZI code, this duration does not change.
Note 2: When the SH or SB bit of TxCR is manipulated, valid data is output 3_{tck} (max.) after the rising edge of WR.

WAVEFORMS (CONTINUED)

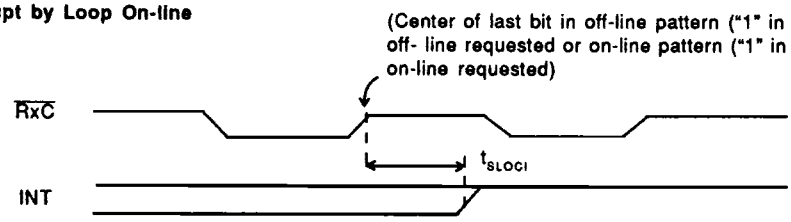




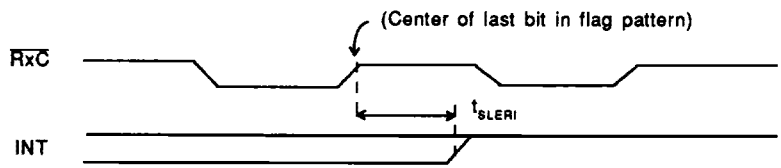
Note 1: For FM0 or FM1 code, the first-half values of data bits must be valid.

WAVEFORMS (CONTINUED)

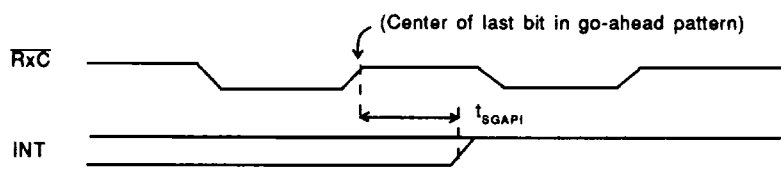
Interrupt by Loop On-line



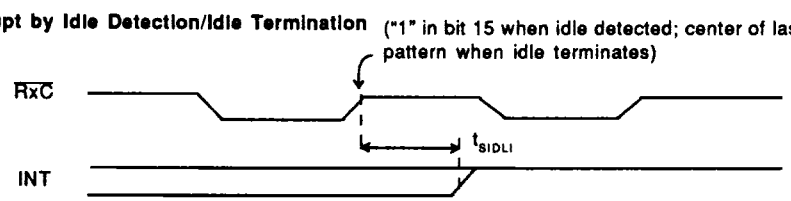
Interrupt by Loop Error



Interrupt by Detection of Go-Ahead Pattern

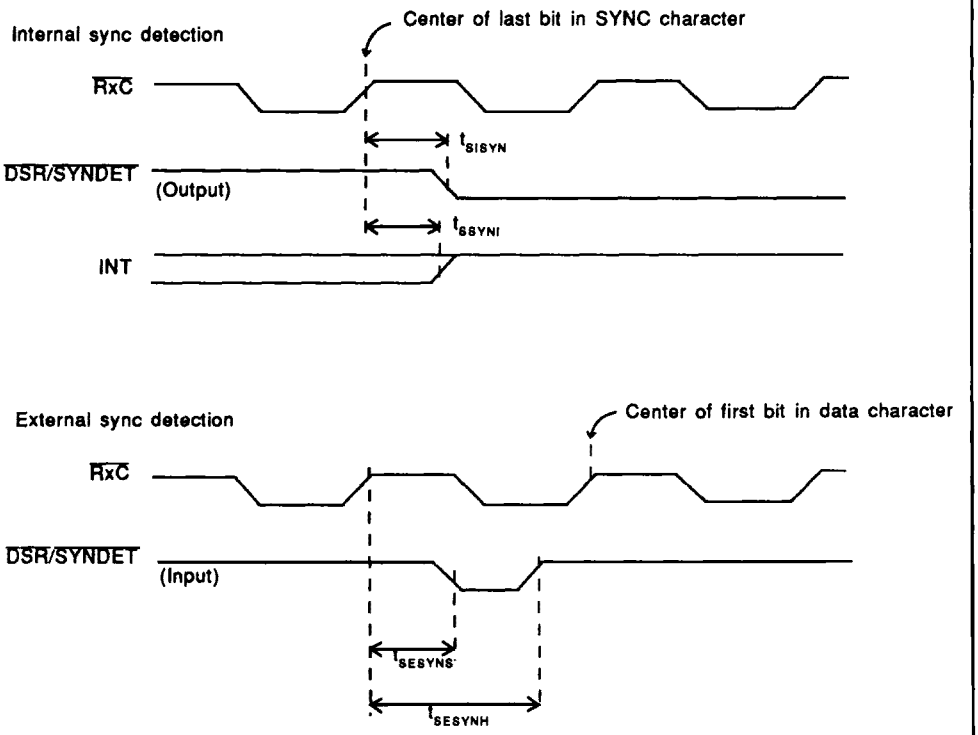


Interrupt by Idle Detection/Idle Termination



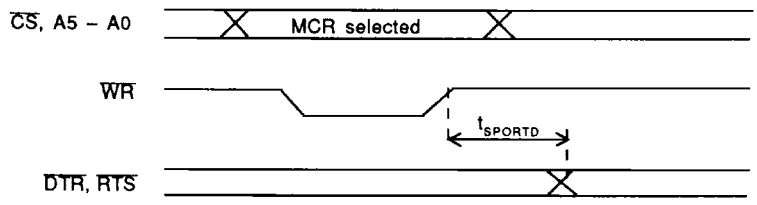
WAVEFORMS (CONTINUED)

COP Sync Detection

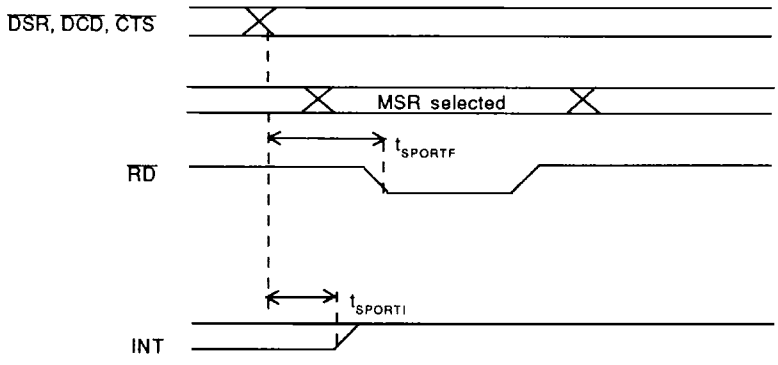


WAVEFORMS (CONTINUED)

Output Modem Control Signal

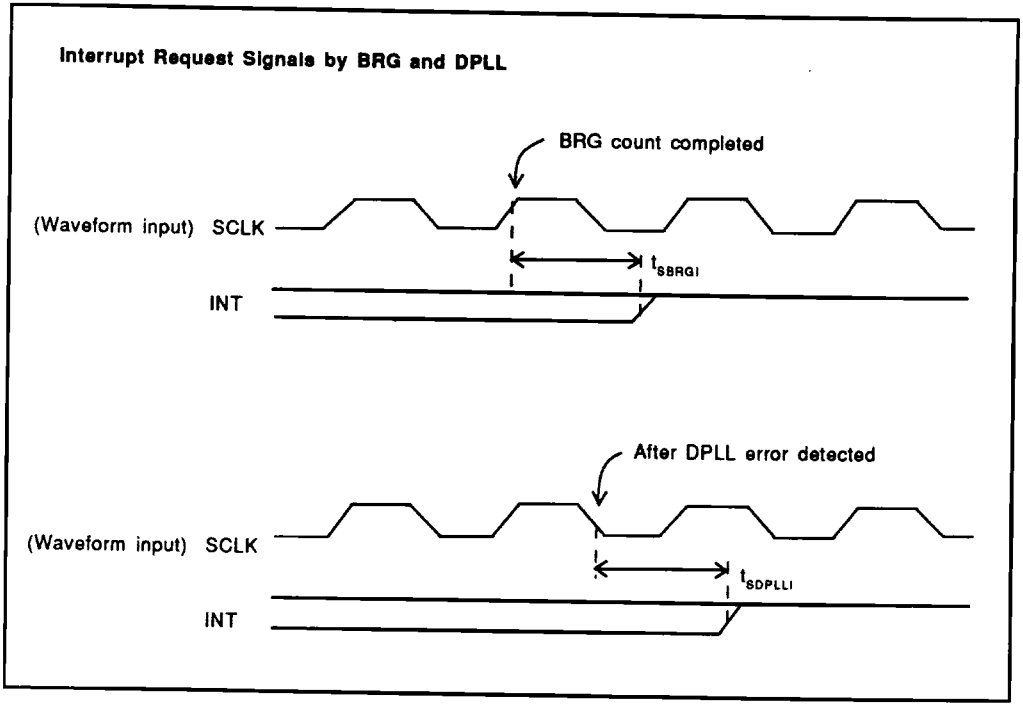


Input Modem Control Signal



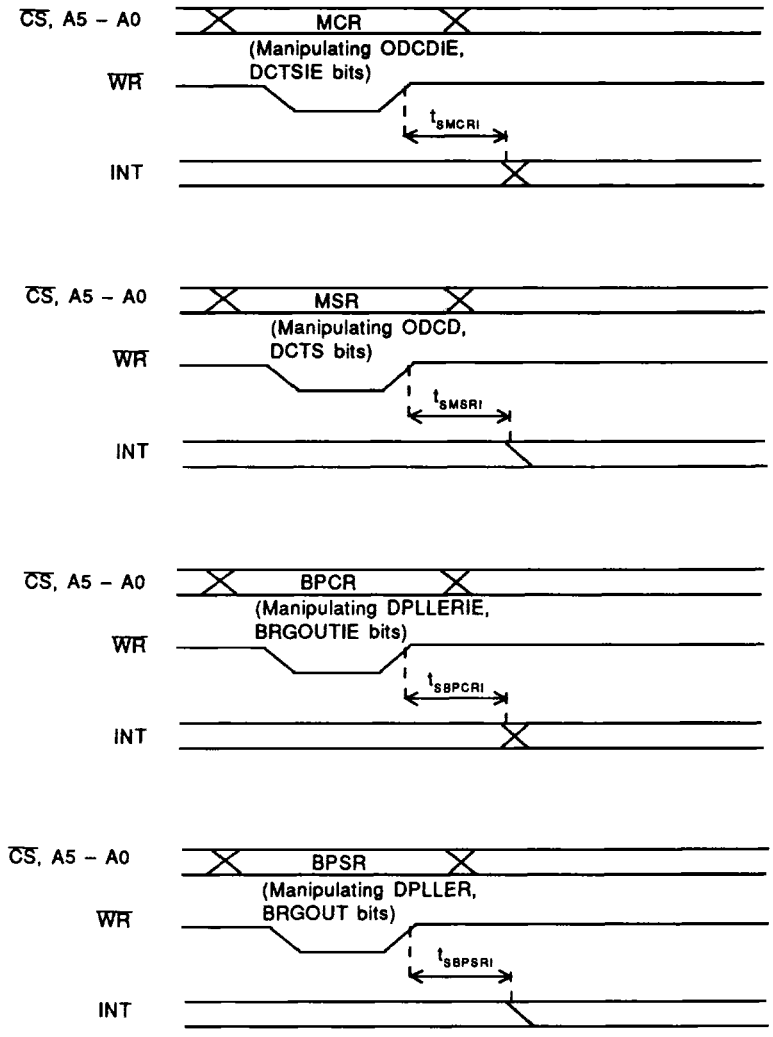
WAVEFORMS (CONTINUED)

Interrupt Request Signals by BRG and DPLL

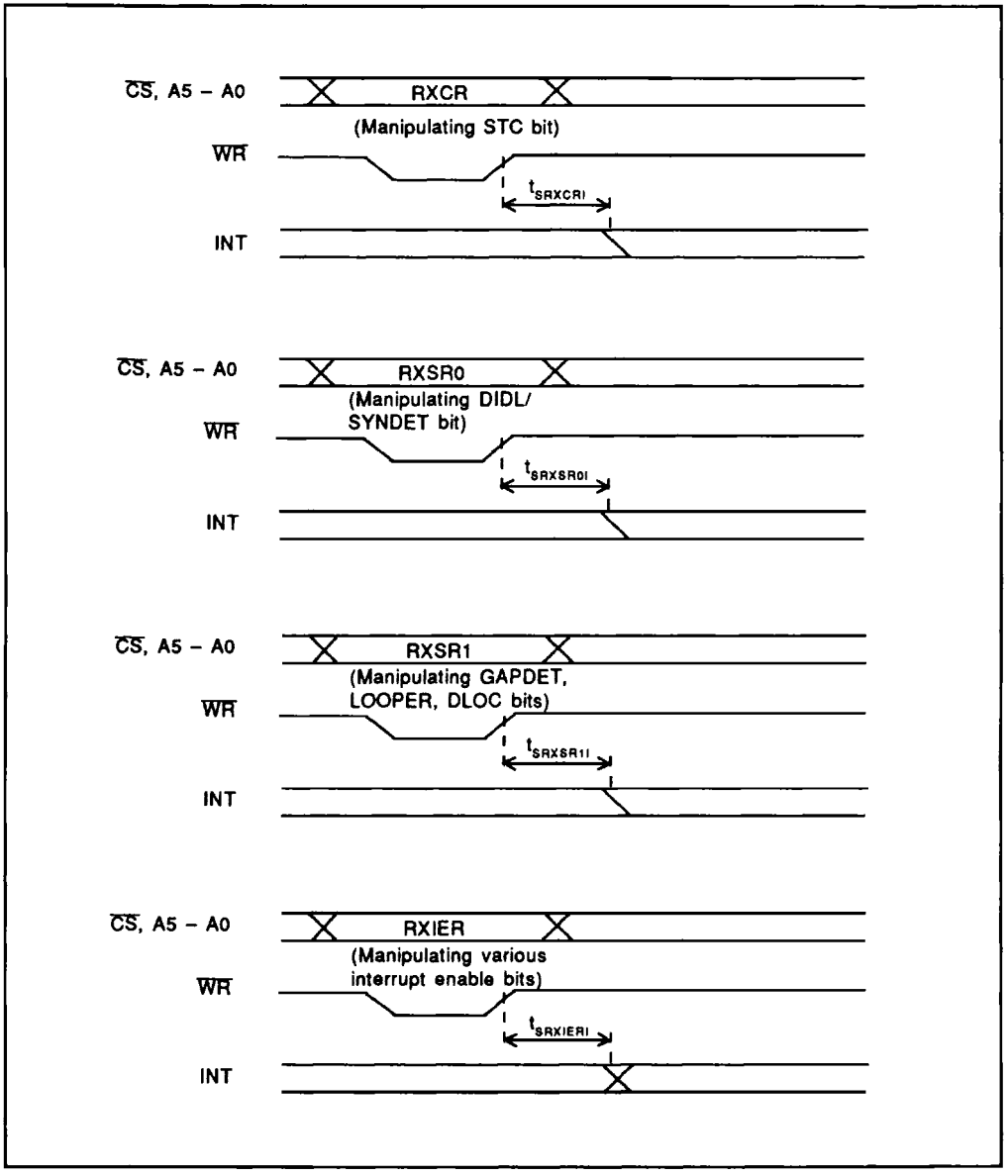


WAVEFORMS (CONTINUED)

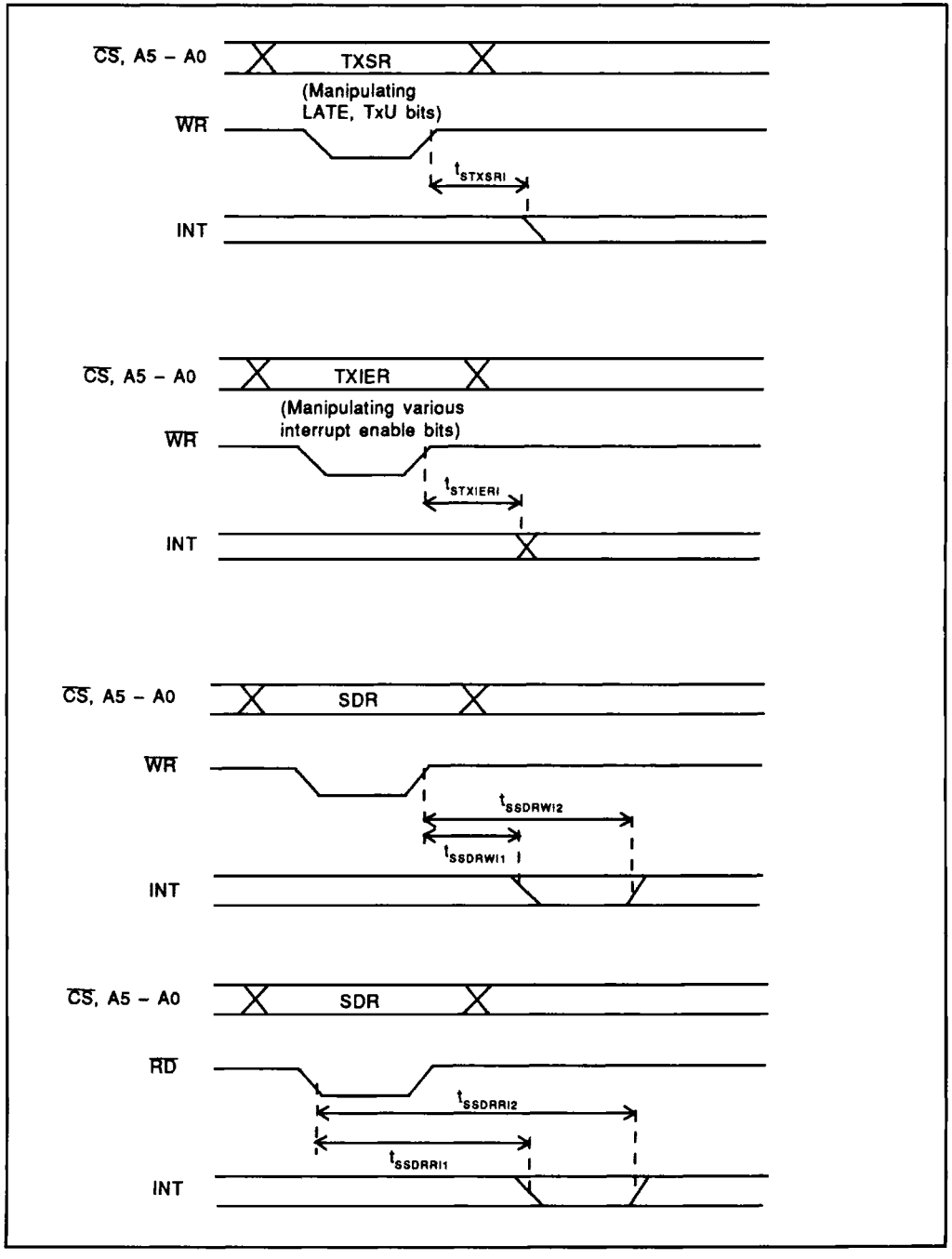
Interrupt Request Signals by Manipulation of Each Interrupt Cause



WAVEFORMS (CONTINUED)

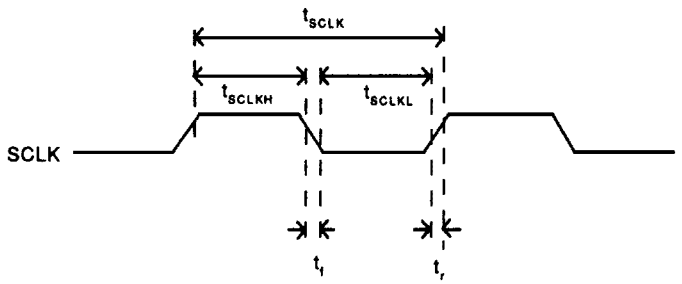


WAVEFORMS (CONTINUED)



WAVEFORMS (CONTINUED)

SCLK Waveform Input



1.5. Pin Assignment

The MPC comes in a 64-pin SH-DIP or 64-pin QFP package. The diagram below shows the pin assignment of the MPC.

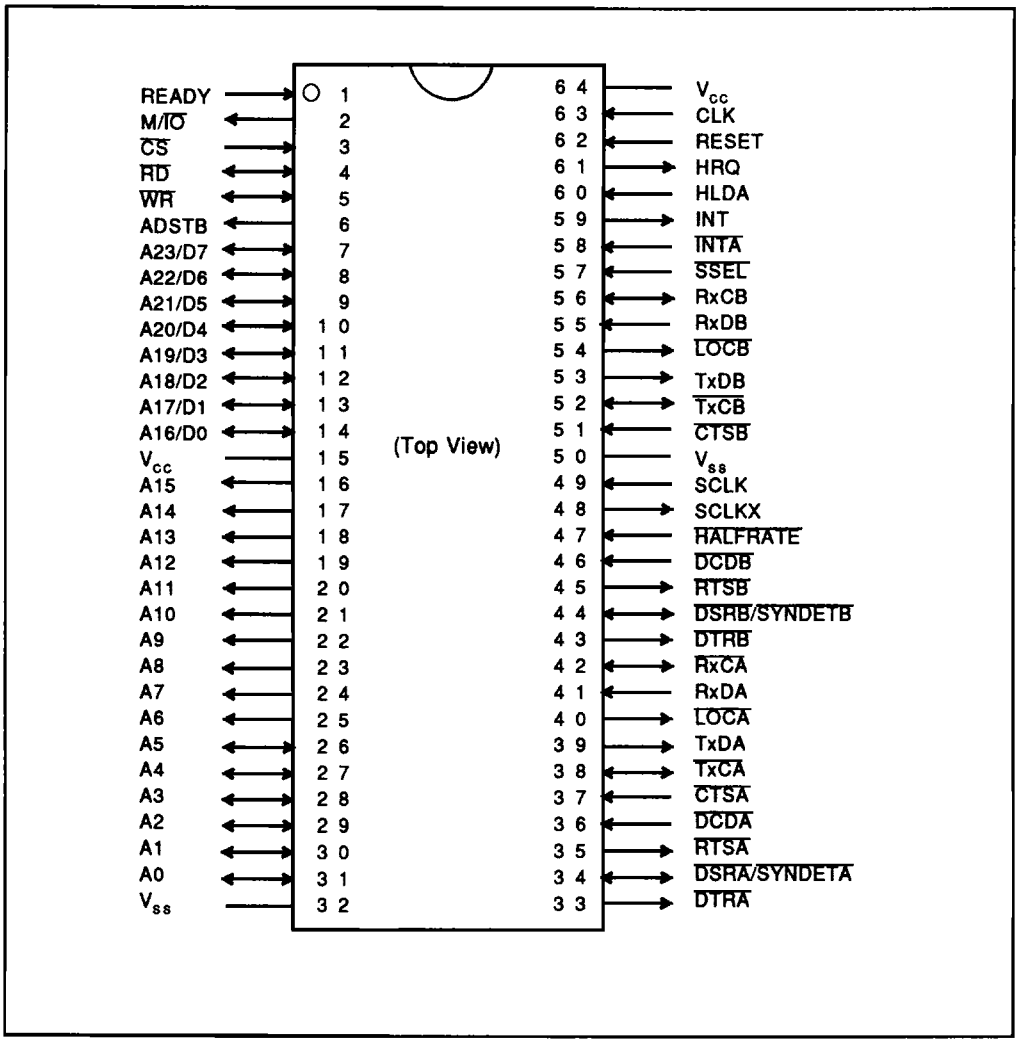


Figure 1-2. Pin Assignment (64-pin SH-DIP)

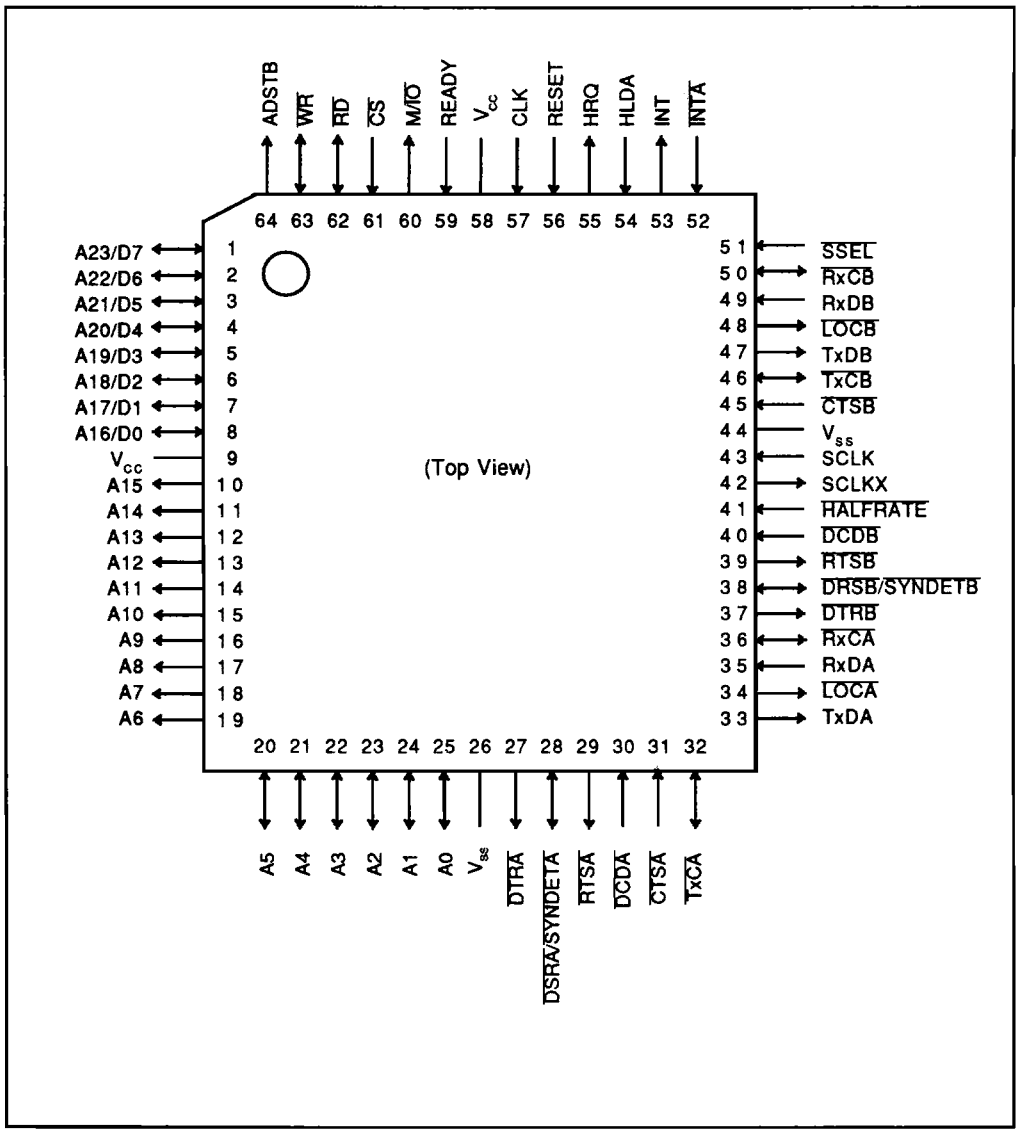


Figure 1-3. Pin Assignment (64-pin QFP)

1.6. Pin Description

Table 1-1. Pin Description

QFP pin	DIP pin	Symbol	Type	Function	When reset
57	63	CLK	I	System clock input pin: Provides the fundamental timing for the MPC internal operation; it enables input of up to 8MHz.	Input
56	62	RESET	I	Reset input pin: Applying HIGH to this pin stops the current operation. When RESET input is returned to LOW, the MPC internal logic is initialized (from which state operation can be re-started). CLK input must be on before the reset operation can be done. Use RESET to clear the power save mode.	Input
62	4	$\overline{RD}$	I/O	Read signal input/output pin: When HRQ output is LOW or HLDA input is LOW, the MPC operates as a bus slave and this pin serves as read input. When this signal goes LOW while $\overline{CS}$ input is LOW, the contents of the register selected by inputs A_5-A_0 are output to the A_{23}/D_7 - A_{16}/D_0 pins. When HRQ output is HIGH and HLDA input is HIGH, this pin enters the output state to output the read signal necessary for DMA transfer.	Input
63	5	$\overline{WR}$	I/O	Write signal input/output pin: When HRQ output is LOW or HLDA input is LOW, the MPC operates as a bus slave and this pin serves as write input. When this signal goes LOW while $\overline{CS}$ input is LOW, the contents of the A_{23}/D_7 - A_{16}/D_0 pins are written to the register selected by inputs A_5-A_0. When HRQ output is HIGH and HLDA input is HIGH, this pin enters the output state to output the write signal necessary for DMA transfer.	Input
61	3	$\overline{CS}$	I	Chip select input pin: When this pin is LOW while HRQ output is LOW or HLDA input is LOW, the internal registers can be accessed by $\overline{RD}$ input or $\overline{WR}$ input via A_{23}/D_7 - A_{16}/D_0 pins. When this pin is HIGH, the A_{23}/D_7 - A_{16}/D_0 pins are in the high impedance state. Interrupt sequences are executed without being affected by input to this pin. When HRQ output is HIGH and HLDA input is HIGH, the MPC operates as the bus master and the input to this pin becomes invalid.	Input

Table 1-1. Pin Description (Continued)

QFP pin	DIP pin	Symbol	Type	Function	When reset
20-25	26-31	A_5 - A_0	I/O	Input/output pins for lower six address bits: When HRQ output is LOW or HLDA input is LOW, the MPC operates as a bus slave and this pin serves for address input. At this time, these inputs are used with $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$ to select the register to be accessed. When HRQ output is HIGH and HLDA input is HIGH, the MPC operates as the bus master and these pins output an address.	Input
10-19	16-25	A_{15} - A_8	O	Address output pins: When HRQ output is LOW or HLDA input is LOW, the MPC operates as a bus slave and these pins are in the high impedance state. When HRQ output is HIGH and HLDA input is HIGH, the MPC operates as the bus master and these pins output an address.	Hi-Z
1 - 8	7 - 14	A_{23}/D_7 - A_{16}/D_0	I/O	Multiplex pins for 8-bit data input/output and upper-byte address output: When HRQ output is LOW or HLDA input is LOW, the MPC operates as a bus slave and these pins serve as 8-bit data input/output pins. When $\overline{CS}$ input is LOW and $\overline{RD}$ input is LOW, the contents of the register selected by inputs A_5-A_0 are output from these pins. When $\overline{CS}$ input is LOW and $\overline{WR}$ input is LOW, the contents on these pins are written to the register selected by inputs A_5-A_0. If the second $\overline{INTA}$ in an interrupt sequence is LOW and $\overline{SSEL}$ input is LOW, the interrupt vector is output from these pins. Except in these cases, the A_{23}/D_7 - A_{16}/D_0 pins remain in 3-state OFF (no outputs are made and inputs are invalid). When HRQ output is HIGH and HLDA input is HIGH, the MPC operates as the bus master and these pins serve as multiplex pins for 8- bit data input/output and upper-byte address output. When the built-in DMA controller determines that the upper-byte address be output, the upper-byte address including the address output timing is output from these pins during the DMA transfer cycle. When internal logic requires that data be read, the contents on these pins are taken into the chip at the data timing in the DMA transfer cycle. When internal logic requires that data be written, the data is output from inside the chip to these pins at the data timing in the DMA transfer cycle. If the upper-byte address is not needed for DMA transfer, the upper-byte address output timing can be omitted and the pins can be used as dedicated data input/output pins by setting the register.	Hi-Z

Table 1-1. Pin Description (Continued)

QFP pin	DIP pin	Symbol	Type	Function	When reset
64	6	ADSTB	O	This pin provides the upper-byte address latch timing during DMA operation. When HRQ output is LOW or HLDA input is LOW, the MPC operates as a bus slave and this pin outputs LOW. When HRQ output is HIGH and HLDA input is HIGH, the MPC operates as the bus master and this pin outputs a high-active strobe signal to latch the upper-byte address output from the A_{23}/D_7 - A_{16}/D_0 pins (8-bit data input/output and upper-byte address output multiplexed pins) onto an external circuit. This strobe output does not become active when the DMA controller decides that the upper-byte address need not be output or when the output of the upper-byte address is omitted by setting the register.	Low
55	61	HRQ	O	Hold request output pin: When a descriptor transfer request occurs in the DMA controller or data transfer is requested from the serial interface unit (SIU), this pin outputs HIGH to request control of the system bus. When DMA transfer is completed, it outputs LOW to relinquish control of the system bus.	Low
54	62	HLDA	I	Hold acknowledge input pin: When HIGH is input to this pin while control of the system bus is requested by HRQ output, the MPC controls the system bus as the bus master to execute DMA transfer. After HRQ output goes LOW and the MPC relinquishes control of the system bus, make the HLDA input go LOW.	Input
59	1	READY	I	READY input pin: If the $\overline{RD}$ or $\overline{WR}$ pulse duration need not be extended during DMA transfer, input HIGH to this pin. If the device to be accessed for DMA transfer operates at low speed and it is necessary to extend the $\overline{RD}$ or $\overline{WR}$ pulse duration, input LOW to this pin, then input HIGH at the timing where the required pulse duration is obtained to terminate access. Because READY input is first sampled before $\overline{RD}$ or $\overline{WR}$, this method can only be used for "normally not ready," and not for "normally ready."	Input

Table 1-1. Pin Description (Continued)

QFP pin	DIP pin	Symbol	Type	Function	When reset
60	2	M/$\overline{IO}$	O	Memory/IO device select signal output pin: When HRQ output is LOW or HLDA input is LOW, the MPC operates as a bus slave and this pin is in the high impedance state. When HRQ output is HIGH and HLDA input is HIGH, the MPC operates as the bus master and this pin outputs the M/$\overline{IO}$ signal. This output is HIGH during descriptor transfer. During data transfer, HIGH or LOW output can be specified for each data block by the TR bit in the SC field of the descriptor.	Hi-Z
53	59	INT	O	Interrupt request output pin: INT is a HIGH active interrupt request output from the MPC to the system after various interrupt requests generated by the SIU and DMA controller are prioritized by the interrupt controller.	Low
52	58	$\overline{INTA}$	I	Interrupt acknowledge input pin: The built-in interrupt controller supports the MBL8086/88 interrupt sequences. When the first interrupt acknowledge pulse (LOW active) is applied to this pin in an interrupt sequence, the A_{23}/D_7 - A_{16}/D_0 pins maintain the high impedance state; when the second interrupt acknowledge pulse is applied and $\overline{SSEL}$ input is LOW, the interrupt vector is output from the A_{23}/D_7 - A_{16}/D_0 pins. When the second interrupt acknowledge pulse is applied and $\overline{SSEL}$ input is HIGH, the A_{23}/D_7 - A_{16}/D_0 pins maintain the high impedance state. For systems in which the MBL8086/88 interrupt sequences are not executed, fix this pin to HIGH.	Input
51	57	$\overline{SSEL}$	I	Slave select input pin: The built-in interrupt controller can also be used as a slave interrupt controller when the MB89259A operates as the master. When the second interrupt acknowledge pulse is input in an interrupt sequence and $\overline{SSEL}$ input (given by decoding the C2-C0 cascaded outputs of the MB89259A) is LOW, an interrupt sequence to the MPC is assumed and the interrupt vector is output. If $\overline{SSEL}$ input is HIGH, the interrupt acknowledge pulse is ignored by assuming that it is not an interrupt sequence to the MPC. For systems in which the built-in interrupt controller is not used as a slave interrupt controller, fix this pin to LOW.	Input

Table 1-1. Pin Description (Continued)

QFP pin	DIP pin	Symbol	Type	Function	When reset
43	49	SCLK	I	Source clock input pin for serial transfer clock generated by the SIU: To use the built-in oscillation circuit, connect the quartz oscillator to this pin and SCLKX pin. It is also possible to input the clock waveform from this pin. The source clock from this pin is supplied to the built-in bit rate generator (BRG) and digital PLL (DPLL). For systems in which BRG and DPLL are not used, fix this pin to LOW or HIGH.	Input
42	48	SCLKX	O	This pin is used to connect the quartz oscillator when using the built-in oscillation circuit. If the clock waveform is input from the SCLK pin or BRG and DPLL are not operated, leave this pin open.	Inverted value of SCLK input
41	47	$\overline{\text{HALF-RATE}}$	I	The source clock signal from the SCLK pin (SCLKX pin) passes a divide-by-two circuit before being supplied to the BRG and DPLL. $\overline{\text{HALFRATE}}$ input enables the function of the divide-by-two circuit. When this pin is LOW, the function of the divide-by-two circuit is enabled and the source clock is divided by two before being supplied to the BRG and DPLL. When this pin is HIGH, the function of the divide-by-two circuit is disabled and the source clock is supplied directly to the BRG and DPLL. If the quartz oscillator is connected to the SCLK and SCLKX pins, be sure to fix this pin to LOW for reshaping the wave-form in the chip; otherwise, it may be fixed to LOW or HIGH.	Input
36	42	$\overline{\text{RxCA}}$	I/O	This is a serial receive clock input/output pin for channel-A of the SIU. After reset, this pin floats to 3-state OFF. When data is written to the SMR2A register, this pin is set for input or output depending on the setting. In the ASYNC mode, the clock input/output rate must be data rate x1, x16, x32, or x64 (as set in the SMR0A register).	Hi-Z
32	38	$\overline{\text{TxCA}}$	I/O	This is a serial send clock input/output pin for channel-A of the SIU. After reset, this pin floats to 3-state OFF. When data is written to the SMR2A register, this pin is set for input or output depending on the setting. In the ASYNC mode, the clock input/output rate must be data rate x1, x16, x32, or x64 (as set in the SMR0A register).	Hi-Z

Table 1-1. Pin Description (Continued)

QFP pin	DIP pin	Symbol	Type	Function	When reset
35	41	RxDA	I	This is a serial send data input pin for channel-A of the SIU.	Input
33	39	TxDA	O	This is a serial send data output pin for channel-A of the SIU.	High
34	40	$\overline{\text{LOCA}}$	O	This is a loop on-line control signal output pin for channel-A of the SIU. Send in the LOOP secondary station mode and logic "1" (in seven consecutive bits) is received after on-line is requested to the loop by a register specification, this pin goes LOW to indicate that the loop is in an on-line state. When logic "1" (in eight consecutive bits) is received after off-line is requested from the loop by a register specification during the on-line state, this pin goes HIGH to indicate that the loop is in an off-line state. In addition, when a forced release is requested from the loop by a register specification during the on-line state, this pin immediately goes HIGH to set the loop into the off-line state.	High
28	34	$\overline{\text{DSRA}}$/ $\overline{\text{SYNDETA}}$	I/O	This pin serves dual purposes as a general-purpose input port for channel-A of the SIU (Data Set Ready chA) and as sync detection input/output in the COP mode. In modes other than the COP mode or when the SYN bit of the SMR1A register is set to "0" for the Mono SYNC/ Double SYNC setting in the COP mode, this pin is used as a general-purpose input port. When input to this pin is HIGH, "0" is read; when LOW, "1" is read from the DSR/ SYNDET bit of the MSRA. If the SYN bit of the SMR1A register is set to "1" for the Mono SYNC/Double SYNC setting in the COP mode, this pin serves as a sync detection output pin. When sync is detected, the DIDL/SYNDET bit of the RxSR0A register is set to "1," causing output from this pin to go LOW. When the DIDL/SYNDET bit is cleared to "0," the output from this pin goes HIGH. When setting the External SYNC mode in the COP mode, the SYN bit of the SMR1A register must be set to "1." In this case, this pin becomes a sync detection input pin to enable an external character sync timing to be input to the MPC.	Input

Table 1-1. Pin Description (Continued)

QFP pin	DIP pin	Symbol	Type	Function	When reset
31	37	$\overline{CTSA}$	I	This is an interruptible input port capable of controlling channel-A transmission of the SIU (Clear To Send chA). When input to this pin is HIGH, "0" is read; when LOW, "1" is read from the CTS bit of the MSRA register. When the level of this input changes, the DCTS bit of the MSRA register (interrupt cause bit) is set. When the CTSAUTO bit of the MCRA register is "1," the transmission control function of this pin is made effective to enable serial data transmission from the TxDA pin when the TxE bit of the TxCRA register is "1" and the input to this pin is LOW. When the CTSAUTO bit of the MCRA register is "0," the transmission control function of this pin is nullified. In this case, serial data transmission from the TxDA pin can only be enabled by the TxE bit of the TxCRA register.	Input
30	36	$\overline{DCDA}$	I	This is a general-purpose interruptible input port for channel-A of the SIU (Data Carrier Detect chA). When input to this pin is HIGH, "0" is read; when LOW, "1" is read from the DCD bit of the MSRA register. When the level of this input changes, the DDCD bit of the MSRA register (interrupt cause bit) is set.	Input
29	35	$\overline{RTSA}$	O	This is a general-purpose output port for channel-A of the SIU (Request To Send chA). When the RTS bit of the MCRA register is "0," HIGH is output; when "1," LOW is output from this pin.	High
27	33	$\overline{DTRA}$	O	This is a general-purpose output port for channel-A of the SIU (Data Terminal Ready chA). When the DTR bit of the MCRA register is "0," HIGH is output; when "1," LOW is output from this pin.	High
50	56	RxCB	I/O	Used in conjunction with channel-B of the SIU, these pins have functions equivalent to those used for channel-A of the SIU. Channel-B of the SIU has registers equivalent to those of channel-A of the SIU; the channel-B registers are used for input and output to and from these pins.	Hi-Z
46	52	TxCB	I/O		Hi-Z
49	55	RxDB	I		Input
47	53	TxDB	O		High
48	54	$\overline{LOCB}$	O		High
38	44	$\overline{DSRB}$/ $\overline{SYBDETB}$	I/O		Input
45	51	$\overline{CTSB}$	I		Input
40	46	$\overline{DCDB}$	I		Input
39	45	$\overline{RTSB}$	O		High
37	43	$\overline{DTRB}$	O		High

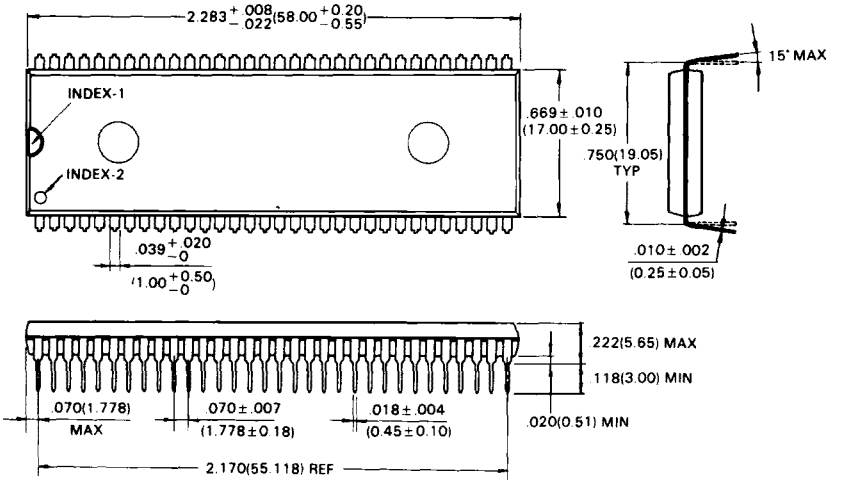
Table 1-1. Pin Description (Continued)

QFP pin	DIP pin	Symbol	Type	Function	When reset
9, 58	15, 64	V_{CC}	—	This is a +5V power supply pin.	—
26, 44	32, 50	V_{SS}	—	This is a GND pin.	—

1.7. Package Dimensions

64-LEAD PLASTIC DUAL IN-LINE PACKAGE

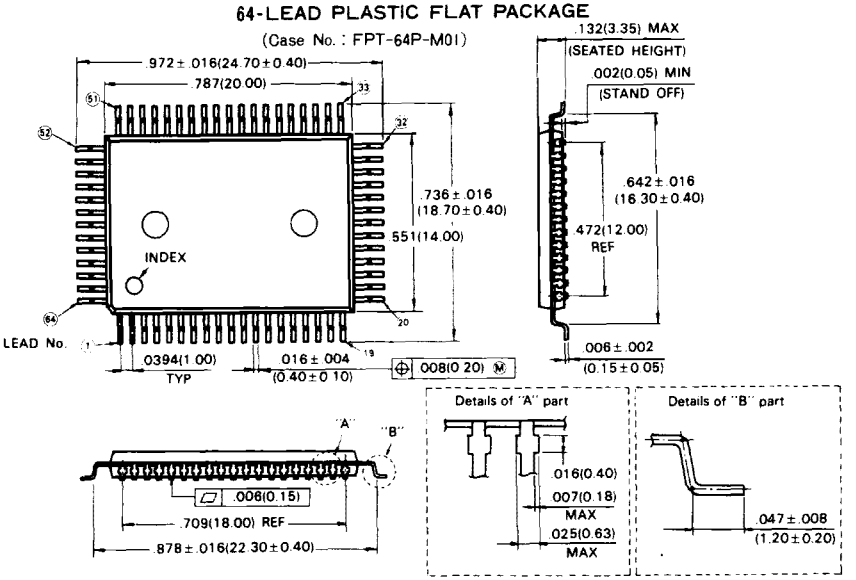
(Case No. : DIP-64P-M01)



Dimensions in inches (millimeters)

64-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-64P-M01)



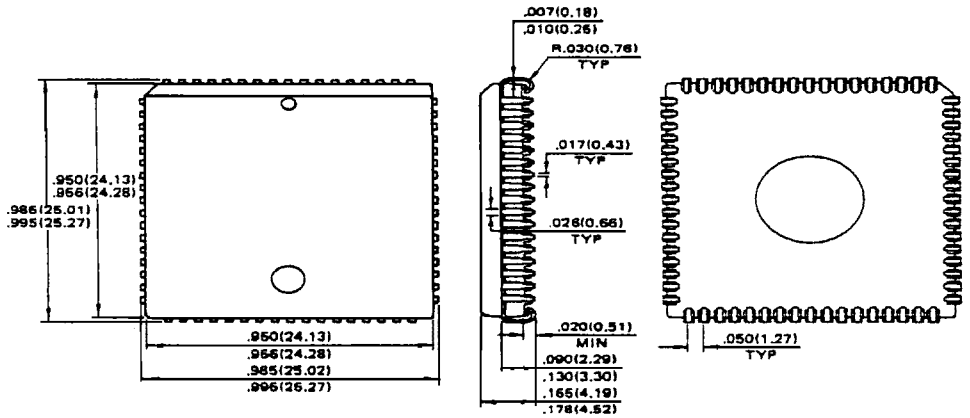
Dimensions in inches (millimeters)

FUJITSU

MB89372APD
ADDENDUM

In addition to the 64-Pin Shrink Dip and 64-Pin Quad Flat Package, the MB89372A is now available in a 68-Pin PLCC Package. The pin assignment and the mechanical dimensions are listed below.

68-LEAD PLASTIC CHIP CARRIER
(CASE No.: LCC-68P-M01)



Dimensions in inches (millimeters)

Pin No.	Description	Pin No.	Description	Pin No.	Description	Pin No.	Description
1	A15	18	/DTRA	35	N.C	52	VCC
2	A14	19	/DSRA/SYNDETA	36	VSS	53	READY
3	A13	20	/RTSA	37	N.C	54	M//IO
4	A12	21	/DCDA	38	N.C	55	/CS
5	A11	22	/CTSA	39	/CTSB	56	/RD
6	A10	23	/TXCA	40	/TXCB	57	/WR
7	A9	24	TXDA	41	TXDB	58	ADSTRB
8	A8	25	/LOCA	42	/LOCB	59	A23/D7
9	A7	26	RXDA	43	RXDB	60	A22/D6
10	A6	27	/RXCA	44	/RXCB	61	A21/D5
11	A5	28	/DTRB	45	/SSEL	62	A20/D4
12	A4	29	/DSRB/SYNDETB	46	/INTA	63	A19/D3
13	A3	30	/RTSB	47	INT	64	A18/D2
14	A2	31	/DCDB	48	HLDA	65	A17/D1
15	A1	32	/HALFRATE	49	HRQ	66	A16/D0
16	A0	33	SCLKX	50	RESET	67	VCC
17	VSS	34	SCLK	51	CLK	68	N.C

*Note: Important Errata on reverse side