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SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13
LAST REV.	A	A	A	A	A	A	A	A	A	A	A	A	A

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TITLE Specification for AY-5-9156
CMOS Loop-Disconnect Dialler

CODE INDENT. NO.

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BY	A. Long						
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SHEET 1 OF 24

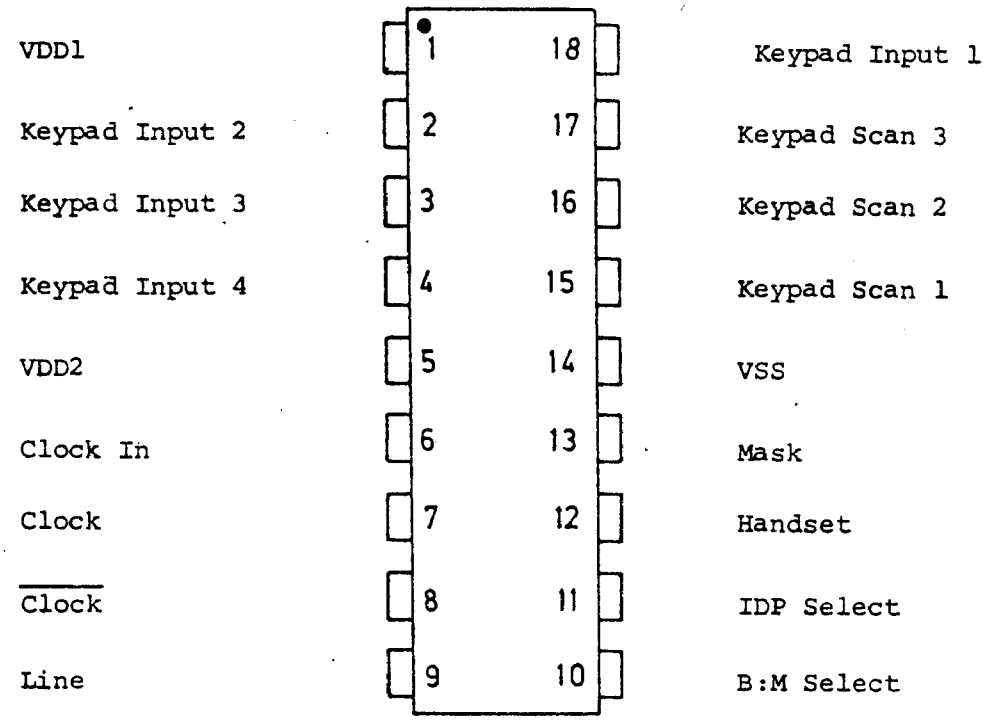
SPEC. NO.	REV.
CPSS70004	A

AY-5-9156 CMOS Loop Disconnect Dialler.

The AY-5-9156 is a CMOS loop disconnect dialler with full access pause and redial capabilities, featuring pin programmable Interdigital Pause and pin programmable Break:Make ratios. The use of a low voltage CMOS process realises well known advantages of low power and high noise immunity, particularly desirable features in a loop disconnect telephone dailler.

The main features are as follows:-

* 2.5 to 5.0V supply voltage
* Low power standby mode for redial
* On-chip clock generator
* 4 x 3 matrix single contact keypad
* Pin selectable IDP
* Pin selectable B:M
* On-chip input pull up/down devices
* Redial and access pause controlled from keypad
* 22 digit capacity including access pauses
* Dialler reset for line power breaks >200msec
* Cerdip or ceramic package



AY-5-9156
CERAMIC
and CERDIP

SECTION 1 - PIN FUNCTIONS.

Vss:

This is connected to the negative terminal of the power supply to the dialler. Voltages on all other pins of the dialler are normally referenced to this pin.

VDD1:

This is the positive supply to the RAM (or digit store). By maintaining power on this pin when the telephone handset is on-hook, the last number dialled (including access pauses) is held in the RAM so that it is subsequently available for redialling if the handset is taken off-hook. If redial is not required, this pin should be connected to VDD 2.

VDD2:

This is the positive supply to the control logic and clock generator. All outputs are connected between VDD2 and VSS and all input pull up devices are connected to VDD2.

When power is applied to VDD2, an internal Power-on reset circuit ensures that the circuit resets correctly. This is described in Section 2.

Clock Input, Clock and $\overline{\text{Clock}}$.

The Clock pulse generator consists of two inverters, the frequency of oscillation being controlled by external components connected to these three pins. The circuit is sufficiently versatile to allow the use of a variety of external component configurations. Figure 1 shows the configuration used throughout this data sheet. Details of the performance of this circuit are given in the section describing electrical characteristics.

IDP Select.

The signal applied to this pin controls the duration of the interdigital pause as follows:-

Signal on Pin	IDP
VDD2	900mS
VSS	800mS
CLOCK	500mS

The pin may also be connected to $\overline{\text{CLOCK}}$. This increases the keypad scan frequency and outdialling frequency by a factor of 15 to facilitate high speed testing of the device. The data on this pin is read during power up of VDD2 or during a reset controlled by the handset input. This pin has an on-chip pull down device to Vss.

Break:Make Select.

Four options of Break:Make ratio of the dial pulses may be selected with this pin as follows:-

Signal on Pin	B:M
VDD2	66.6 : 33.3
VSS	60:40
CLOCK	70:30
$\overline{\text{CLOCK}}$	50:50

Data on this pin is read during power-up of VDD2 or during a reset controlled by the handset input. An on-chip pull-down device to VSS is connected to this input.

Line Output.

The loop-disconnect dial pulses appear at this output. The output stage consists of an N-channel open-drain device sinking current to VSS. During a dial pulse break period the output device is switched on and during the make period and IDP the output device is switched off. The timing of this output relative to the mask output is shown in Figure 2.

Mask Output.

This is a push-pull output and is used to control the muting of the telephone speech circuit during outdialling. A logic 1 indicates that the telephone is to be muted, the transition to logic 1 occurring immediately on recognition of a key depression or on application of VDD2. See Figures 2 and 3 and Section 2.

Keypad Scans 1-3.

There are push pull outputs used to scan the keypad columns at a rate of 200Hz. Figure 4 shows how these outputs are connected to the keypad.

Keypad Inputs 1-4.

The Keypad contacts are used to connect one keypad scan output to one of the keypad inputs to enable recognition of a key depression. Each of these inputs has an on-chip pull up device to VDD2. For a description of how the keypad inputs recognise data, See Section 3.

Handset Input.

External circuitry connected to this input is used to indicate whether the telephone handset is on-hook or off-hook, these two states being represented by logic 1 and logic 0 respectively. If power is present on the dialler, this input should normally be held at logic 0. If the handset input is taken to logic 1 for a period of less than 200 msec and then returned to logic 0, no action is taken and the dialler will continue to function. If it is taken to logic 1 for a period greater than 200msec, all keypad scans go to logic '0' and any dialling sequence which is in progress will cease. All internal counters will be reset, though the contents of the RAM will be unaffected. Taking the input back to logic 0 will restart the keypad scans and the dialler will wait for a data entry. Depression of the Redial key will cause the contents of the RAM to be dialled out again. Depression of any other key will start a new dialling sequence with a potential length of 22 digits.

SECTION 2 - Power-on-Reset.

Application of power to VDD2 will cause an automatic reset of all internal counters (but will not affect the RAM conents) provided that VDD2 reaches 2.5V within 20msec. Longer risetimes may not guarantee correct initialisation of the logic.

Two conditions are possible for the power-up sequence. In both cases it is assumed that the handset input is at logic 0 as soon as power is applied.

(a) VDD2 applied with all keypad inputs open-circuit. In this case a pulse to logic 1 of 16-19 msec duration will appear on the mask output as shown in Fig. 5.

(b) VDD2 applied after one keypad scan output connected to one keypad input.

In this case the mask output goes to logic 1 immediately on application of power and remains at logic 1 provided that the keypad data is recognised within 16 msec. See figure 6.

If a faster reset than the 200msec of the handset input is required, this may be accomplished by switching off VDD2 for a short period. Interruptions in power as short as 1 msec will accomplish a reset.

SECTION 3 - Antibounce of Keypad Data Contacts.

The AY-5-9156 uses a 4 x 3 single contact keypad as shown in Figure 3. The three column contacts are connected to the Keypad Scan outputs KS1 to KS3 and the four row contacts are connected to the Keypad inputs KI1 to KI4.

The Keypad Scan signals are derived from an on-chip signal with a frequency of $\emptyset \div 30$ where $\emptyset$ is the clock frequency (nominally 18kHz). The timing relationship is shown in Figure 7.

The Keypad Inputs are normally held at logic 1 by means of on-chip pull up resistors. When a key is depressed, the dialler identifies the key by examining all four keypad inputs. Keypad Scan pulses should normally occur on one input only, hence the row may be easily identified. Identification of the key within the row is accomplished by comparing the scan pulse on the appropriate keypad input with the three keypad scans.

To prevent multiple reading of digits due to contact bounce, the dialler incorporates circuitry which delays the reading of data until certain conditions are met. This operates as follows.

All four keypad inputs are continuously examined and if any keypad input is at logic 0, an Any Key Down (AKD) signal is generated. This signal is connected to a four stage shift register as shown in Figure 8. T1 is an N-Channel MOS transistor which is switched on when $\emptyset \div 30$ is high and off when $\emptyset \div 30$ is low. When $\emptyset \div 30$ is low, capacitance at node holds the value of AKD which immediately preceded the negative transition of $\emptyset \div 30$. On each positive transition of $\emptyset \div 30$, the shift register is clocked.

In the absence of a key depression, AKD = 0 and this logic level is clocked through the shift register until $\alpha\beta\gamma\delta\varepsilon$ = 00000. Now assume that key 1 is depressed, so that KS1 appears on KI1. The relevant waveforms are shown in Figure 9. A Write Enable Pulse (WEP) is generated on the first appearance of the pattern $\alpha\beta\gamma\delta\varepsilon$ = 10010 and $\emptyset \div 30$ is low. The data on the keypad inputs must be stable for the duration of the WEP, while the data is written into the RAM.

Before another key depression may be detected, all keys must be released for a sufficient period for the shift register to fill with logic 0's, as shown in Figure 10. On the first positive transition of $\emptyset \div 30$ after $\alpha \rightarrow \varepsilon$ = 0, the WEP generator is reset and further data will then be accepted.

If at any time two keys are pressed then the logical expression $\alpha(\beta+\delta)$ will become true and the keypad scans will all go to logic 0 indicating an invalid data entry. AKD will then be permanently true and the shift register will be filled with 1's. To allow the recognition of a valid key depression, all keys must initially be released until the shift register is filled with 0's as shown in Figure 10.

The end result of this implementation of antibounce protection is that data must be stable for 5 to 10ms for a key depression to be recognised, the exact time being dependent on the relative timing of the key depression and the keypad scans. Before a further key depression may be recognised, all keypad inputs must be open circuit for 5-10mS.

SECTION 4 - Access Pause and Redial.

These two features are decoded directly from the keypad using the * and ## buttons respectively.

An Access Pause is a facility which inhibits further dialling out at some user-defined point in a dialling sequence. Such a facility is of particular use when dialling an external number from an extension telephone within a PABX. Suppose, for example that it is required to dial the national number 01-439-1891 from within a PABX. Access to the national network is gained by dialling an access digit, typically digit 9. The sequence of events is then:

1. Pick up phone
2. Wait for PABX dial tone
3. Dial digit 9
4. Wait for national network dial tone
5. Dial 01 439 1891

By using the Access Pause feature, this is reduced to:-

1. Pick up phone
2. Wait for PABX dial tone
3. Dial 9 * 01 439 1891
4. When national dial tone is heard, press ##

The dialler will dial out the digit 9 immediately and then wait. Pressing the ## key, either during or after the keying-in of 01 439 1891, will enable dialling of the national number. The timing of the line and mask outputs during this dialling sequence is shown in Figure 11.

Storage of an access pause is treated in exactly the same way as digits 1 ——— 0 so that as many access pauses as required may be entered at any point in the dialling sequence, provided that the total of access pauses and digits does not exceed 22.

The ## key is a dual function key, acting both as access pause release and redial key. If, after dialling a number, the data is stored in the RAM by maintaining VDD1 and the dialler is then reset, either by a Power on Reset or from the Handset Input, the number may be redialled in full, including access pauses, by depression of the ##.

SECTION 5 - Electrical Characteristics.

5.1 Absolute Maximum Ratings.

a) Permanent damage may result if these ratings are exceeded.

b) Functional operation is not guaranteed under these conditions. The operating ranges are specified in Section 5.2

Voltage on any pin with respect to Vss	=	+7.0 to -0.3
Storage temperature range	=	$-65^{\circ}C$ to $+150^{\circ}C$

5.2 Standard Conditions.

Unless otherwise stated, the following specification is valid for the following conditions:-

Vss	=	0.0V
Vdd1	=	2.5V to 5.0V
Vdd2	=	2.5V to 5.0V
Vdd1	=	Vdd2 $\pm$ 0.2V

Ambient temperature = $-25^{\circ}C$ to $+80^{\circ}C$

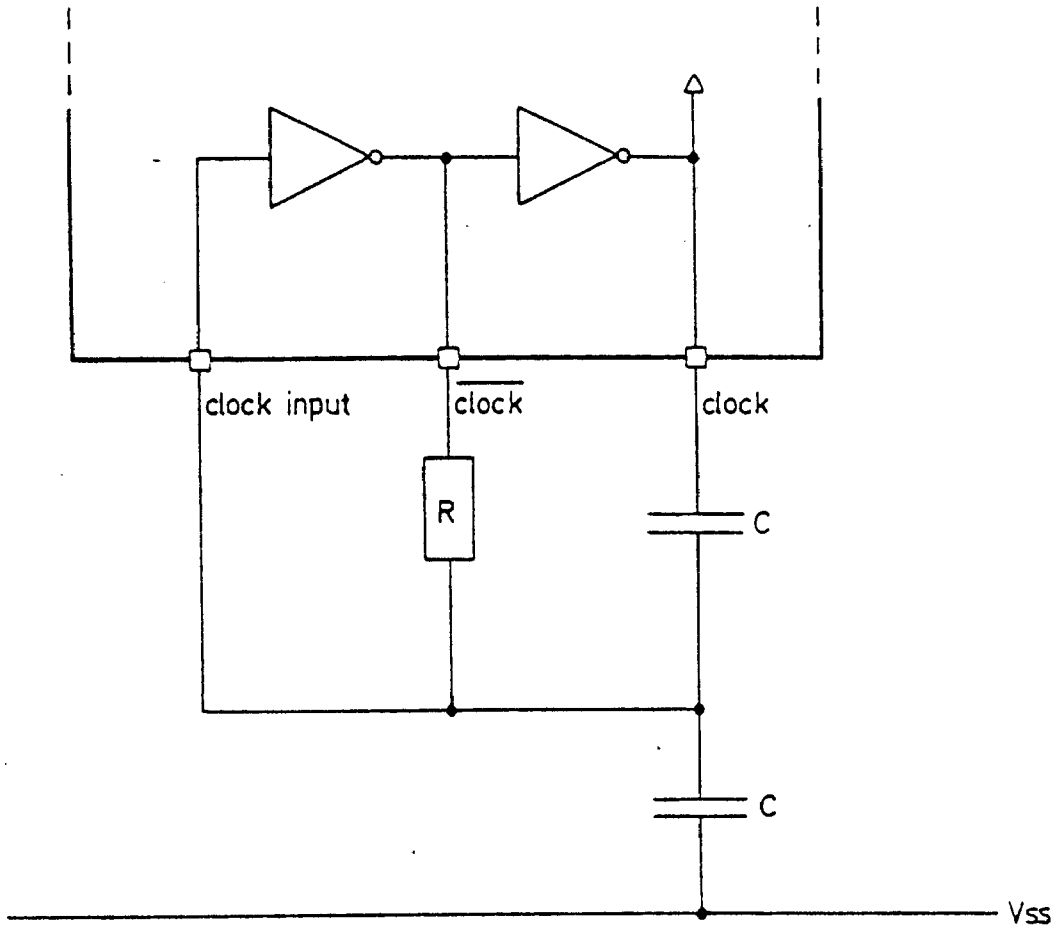
Clock frequency = 18kHz nominal
(Set by components shown in Fig. 1).

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Supply Current.					
IDD 1			7	uA	Vdd1 = 5.0, Vdd2 = 0.0
		20	40	uA	Vdd1 = Vdd2 = 5.0
IDD 2		70	200	uA	Vdd1 = Vdd2 = 5.0 Note 1.
Inputs.					
Logic 0 : IDP, B:M	-0.3		0.2	V	
All other inputs	-0.3		0.5	V	
Logic 1 : IDP, B:M	Vdd -0.2		Vdd +0.3	V	
All other inputs	Vdd2 -0.5		Vdd2 +0.3	V	
Current Source to VDD2:					
Keypad Inputs	2		60	uA	VIN = VSS
Current Sink to VSS:					
IDP, B:M	0.6		15	uA	VIN = VDD2
Clock In Leakage Current			See Note 2		VIN = VSS or VDD2
Key Depression period	10			msec	
Outputs.					
Mask.					
Logic 0 output current	1			mA	Vo = 0.5V
Logic 1 output current	1			mA	Vo = VDD2 -0.5V
Line.					
Logic 0 output current	1			mA	Vo = 0.5V
Logic 1 leakage current			1	uA	Vo = 5.0V
Keypad Scans.					
Logic 0 output current	50			uA	Vo = 0.5V
Logic 1 output current	50			uA	Vo = VDD2-0.5V
Clock Frequency	17.2		18.6	KHz	VDD1 = VDD2 = 3.75V)
	14.3			KHz	VDD1 = VDD2 = 2.5V)*
			19.5	KHz	VDD1 = VDD2 = 5.0V)
					*TA = +25°C
Clock Frequency temperature stability			±2	%	Relative to value at +25°C. VDD2 = 5.0V
			±5	%	Relative to value at +25°C. VDD2 = 2.5V

Note 1: Measured with B:M, IDP and handset inputs at VSS, keypad inputs at VDD2 and all outputs open circuit.

Note 2: Measured to maximum of 20nA on sample basis only at 25°C.

Note 3: Clock frequency specified with component values shown in Figure 1.



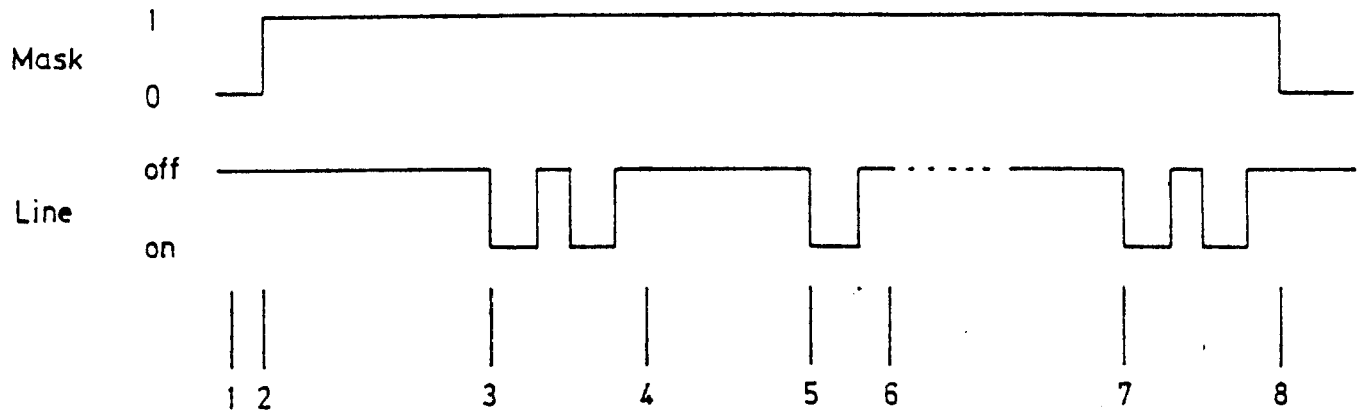
Nominal component values : R = 374 Kohm

C = 47pF

see text

Figure 1

FIGURE 2

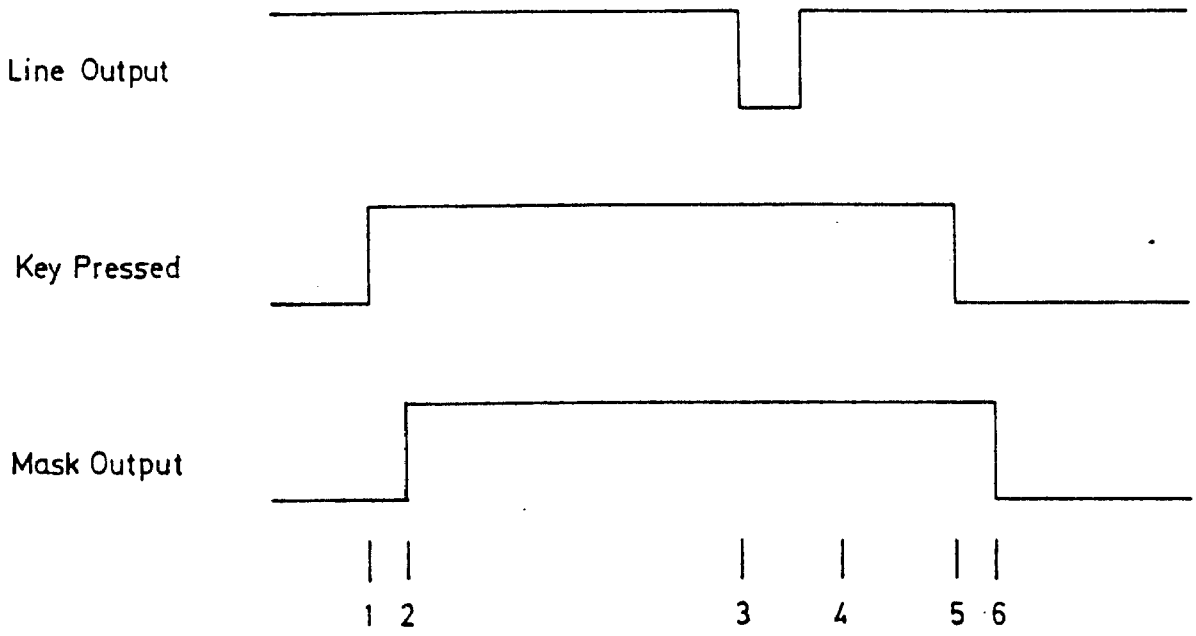


The above sequence of events is that which occurs when the digit store is initially empty. The time intervals quoted in the following explanation are valid only for a clock frequency of 18KHz. The time intervals are inversely proportional to the clock frequency.

	EVENT	TIME INTERVAL
1.	The first key is depressed and the anti-bounce timer is started.	T12 = 5-10ms after end of bounce
2.	The data from the keyboard is accepted. The mask output appears and the pre-digital pause commences. This is the same duration as the inter-digital pause and is pin selectable.	T23 = 500, 800 or 900mS
3.	Dialling of the first digit starts. The example shown is a digit 2.	T34 = n x 100ms where n = digit dialled
4.	End of 1st digit and start of inter-digital pause.	T45 = 500, 800 or 900mS
5.	Dialling of 2nd digit starts. The example shown is a digit 1.	T56 = n x 100ms where n = digit dialled
6.	End of 2nd digit and start of inter-digital pause.	T67 = 500, 800 or 900mS

Dialling of further digits continues in a similar manner until the last digit.

7.	Dialling of last digit commences, in this case a digit 2.	T78 = n x 100ms where n = digit dialled.
8.	End of last digit and end of mask signal.	



The above diagram shows the effect of depressing a key and holding it down beyond the end of dialling. All times quoted are for a clock frequency of 18kHz.

1. Digit 1 key pressed.

T12 = 5-10 msec

2. Key depression recognised after antibounce period. Mask output goes high.

T23 = IDP

3. Start of dialling for digit 1.

T34 = 100 msec

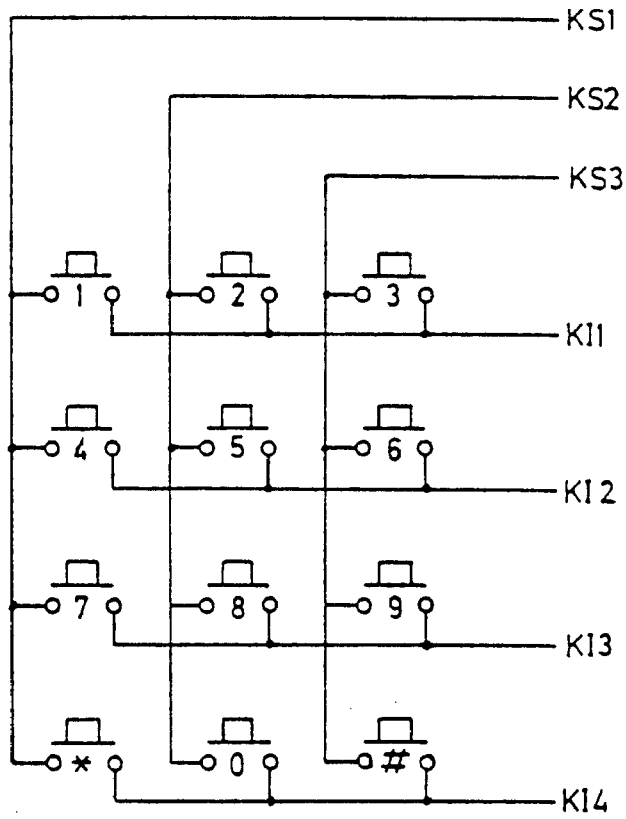
4. End of digit 1.

5. Release of key for digit 1(and any other keys which may be pressed).

T56 = 5-10 msec

6. Mask output goes low after anti-bounce period.

N.B. Although the above waveforms are shown using digit 1 as an example, similar sequences occur for all twelve keys.



Connection for 4 x 3 single contact keypad.

FIGURE 4

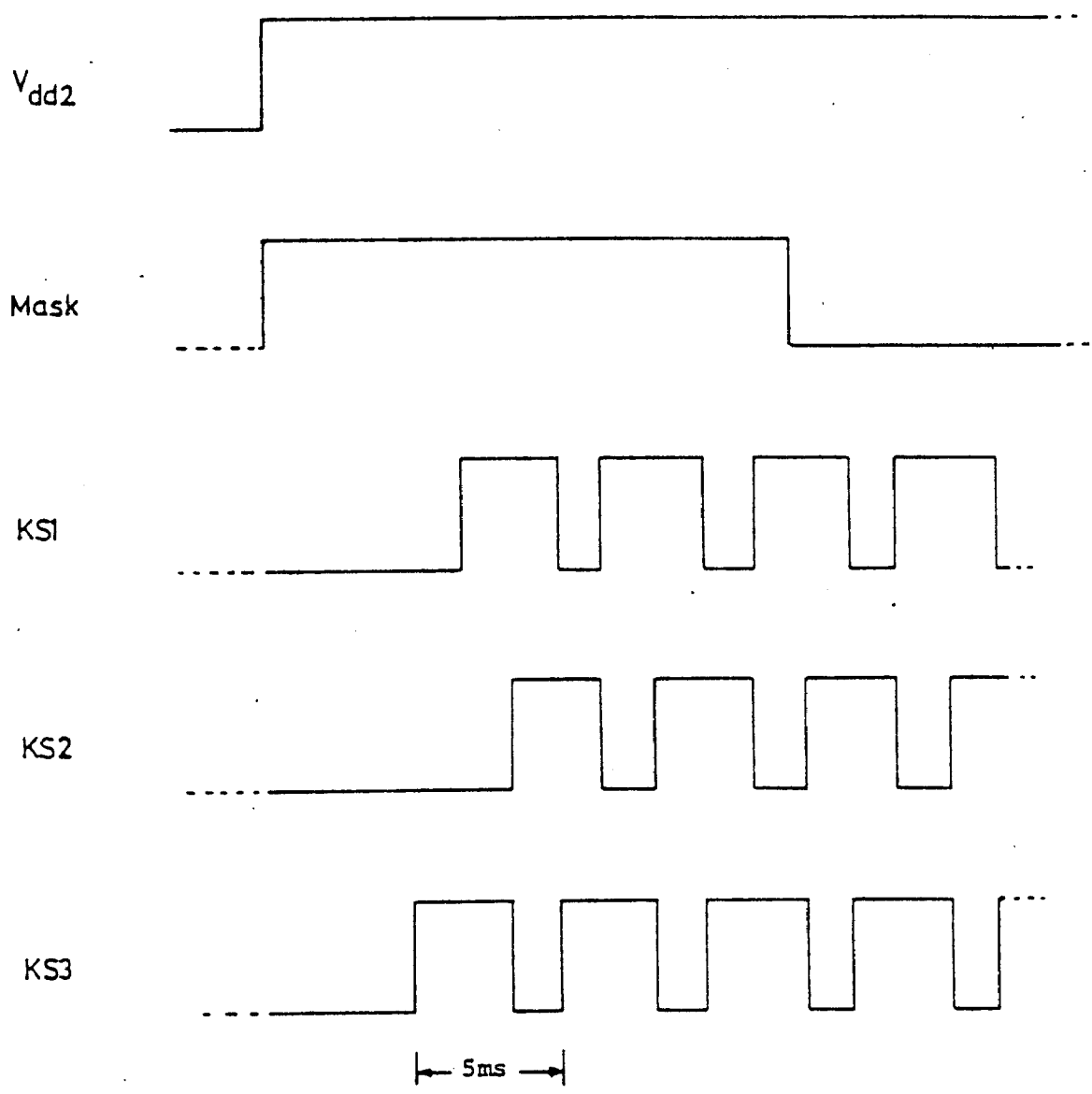


Figure 5-

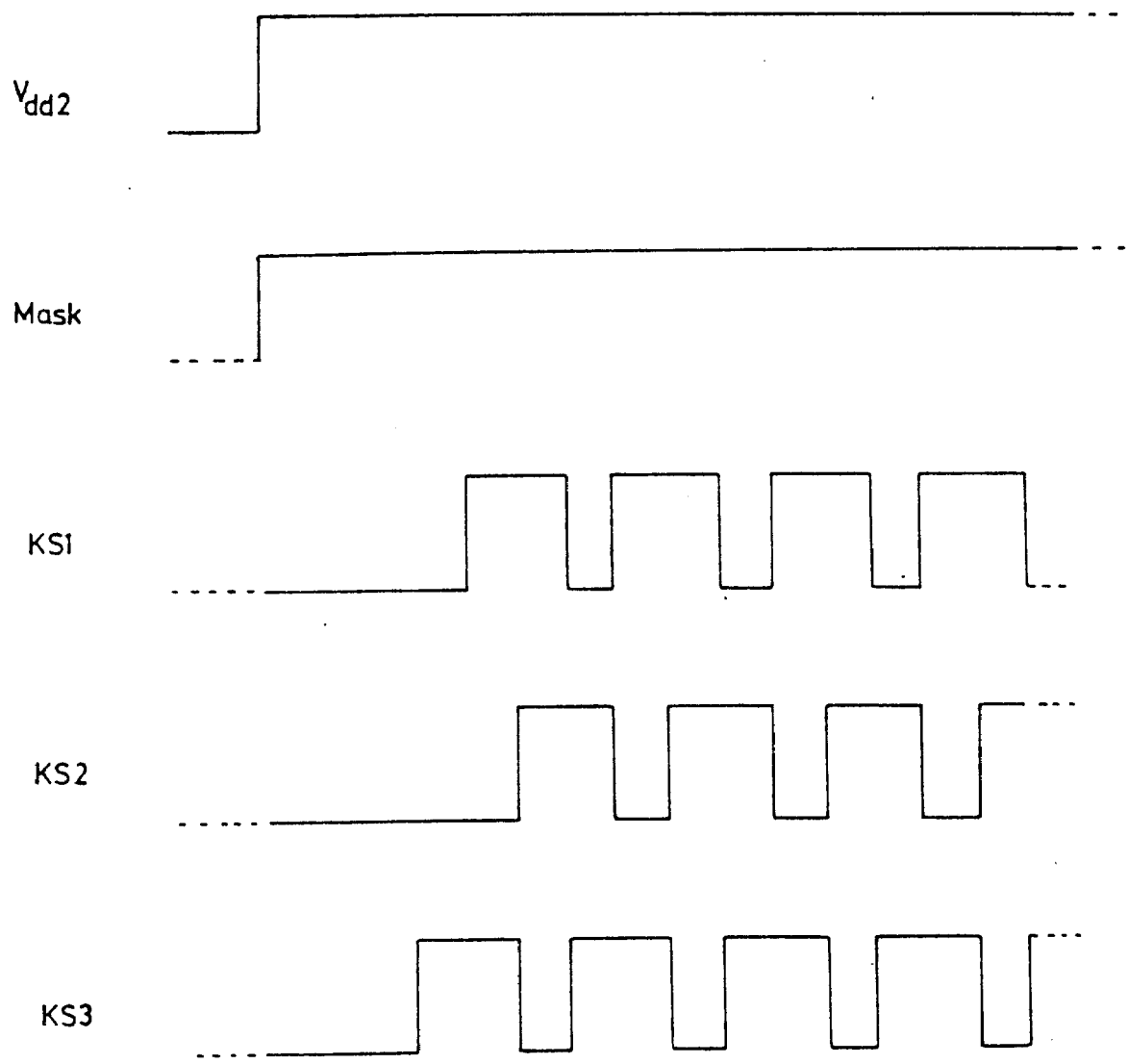
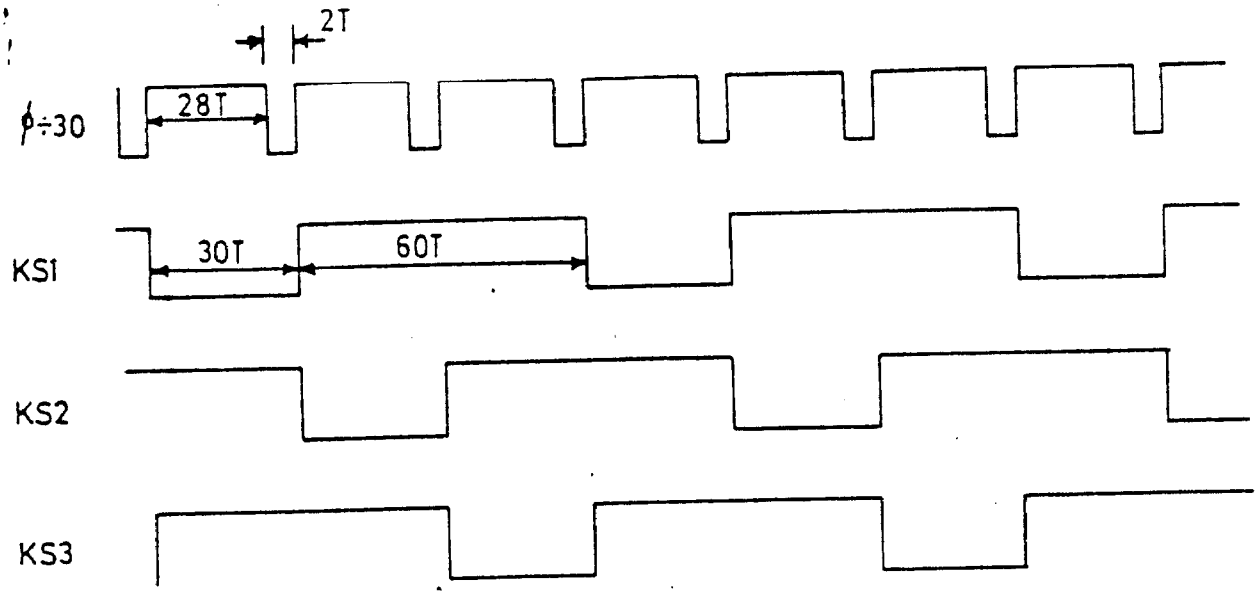


Figure 6



ϕ = clock frequency (18 kHz nominal)
T = clock period (55·55μs nominal)

Figure 7

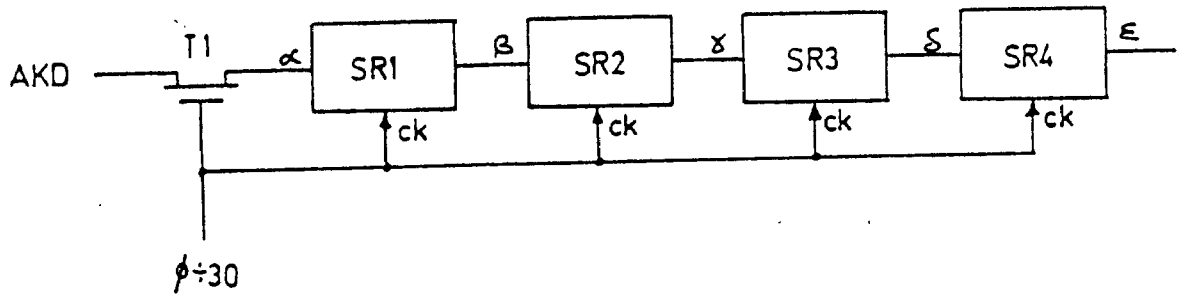
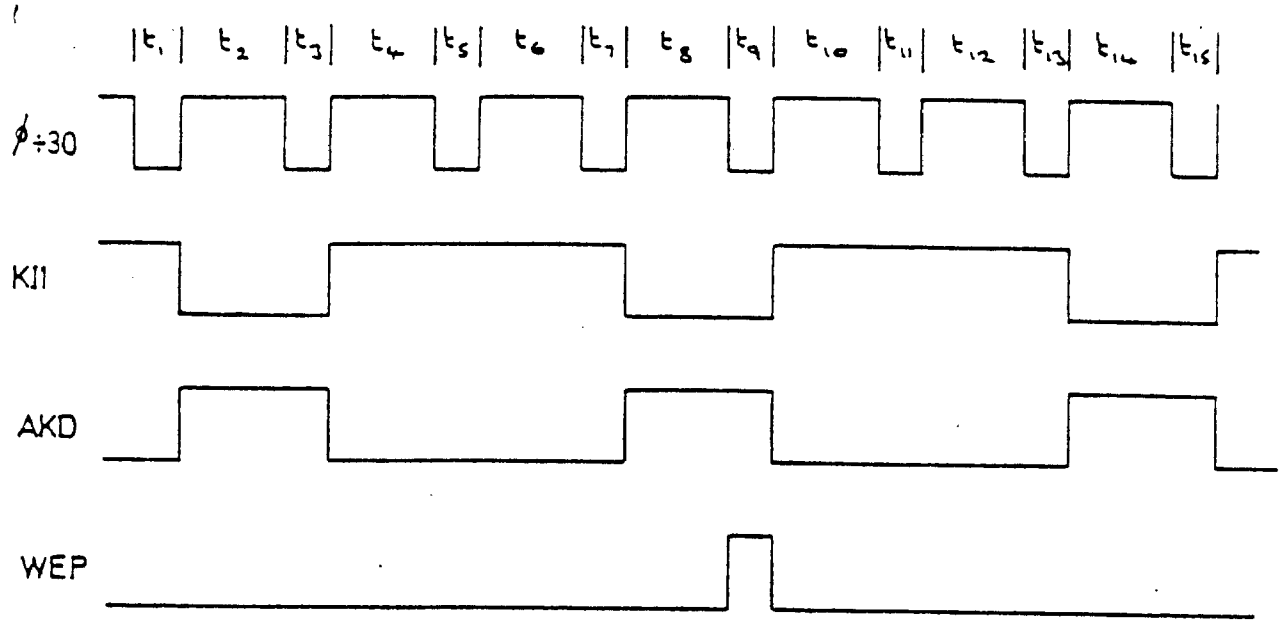


Figure 8



t	AKD	α	β	γ	δ	ϵ
1	0	0	0	0	0	0
2	1	1	0	0	0	0
3	1	1	0	0	0	0
4	0	0	1	0	0	0
5	0	0	1	0	0	0
6	0	0	0	1	0	0
7	0	0	0	1	0	0
8	1	1	0	0	1	0
9	1	1	0	0	1	0
10	0	0	1	0	0	1
11	0	0	1	0	0	1
12	0	0	0	1	0	0
13	0	0	0	1	0	0
14	1	1	0	0	1	0
15	1	1	0	0	1	0

Figure 9

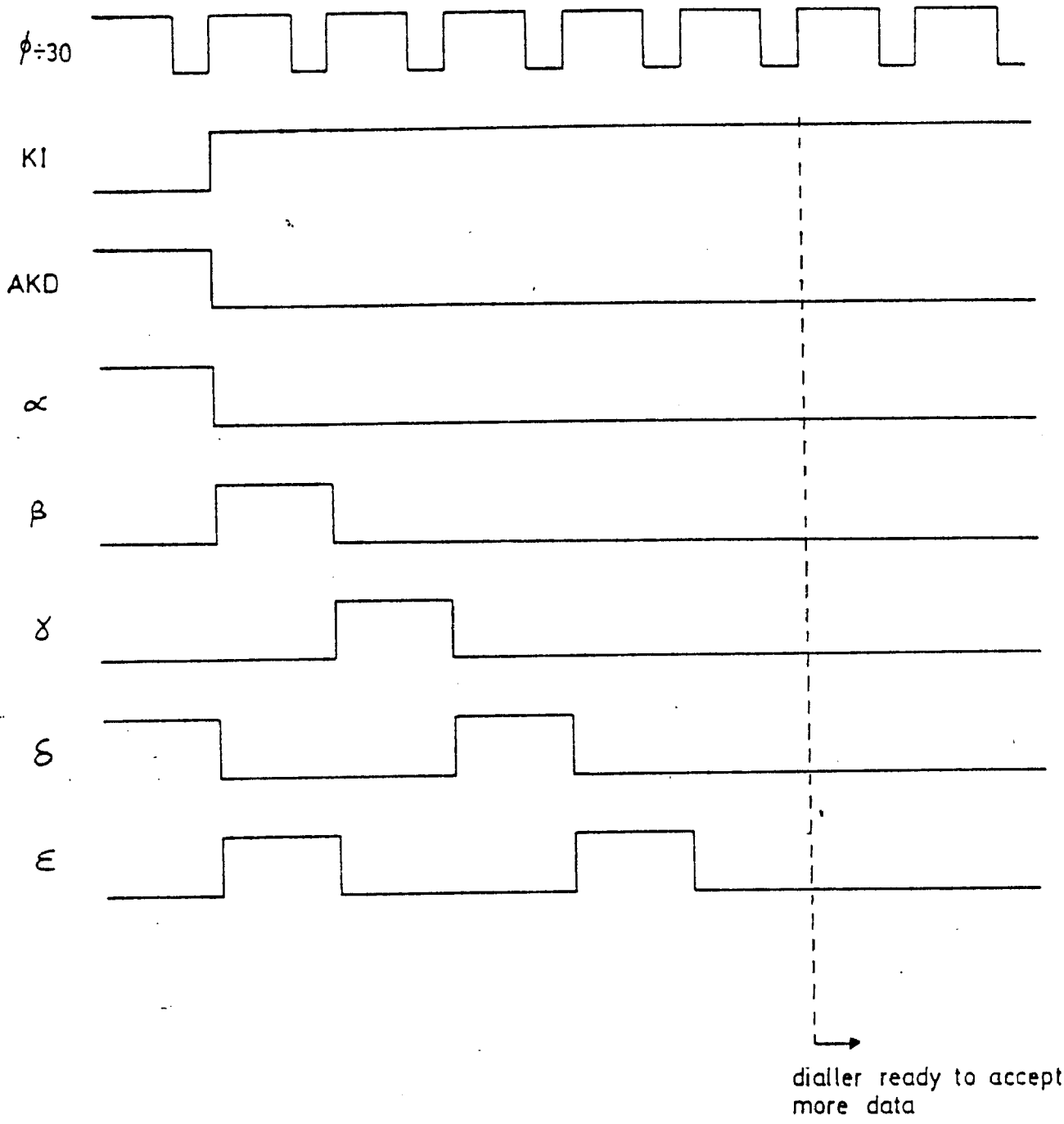
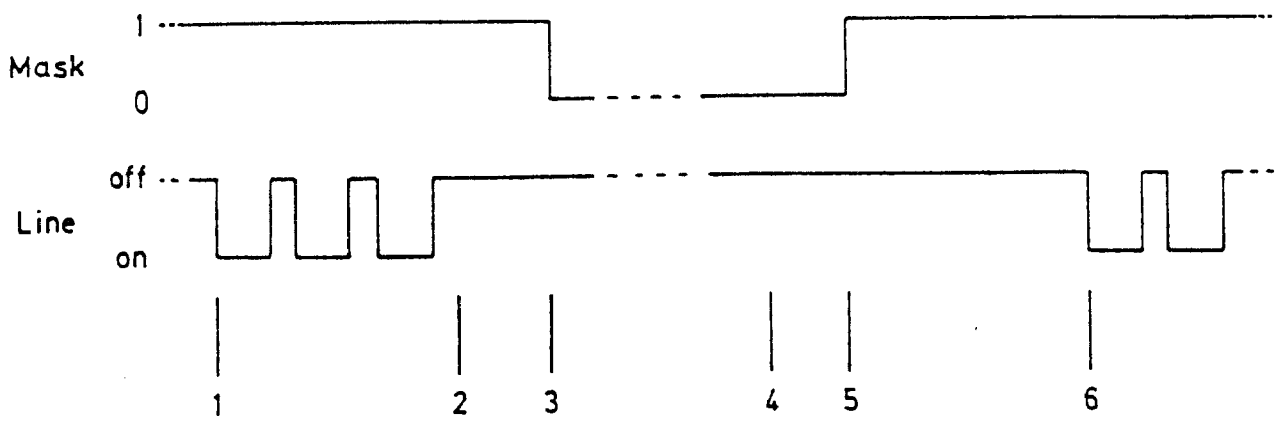


Figure 10

FIGURE 11



The following time intervals are valid only for a clock frequency of 18KHz.

EVENT	TIME INTERVAL
1. Dialling of the last digit before the access pause commences. A digit 3 is shown in this example.	T12 = n x 100ms where n = digit dialled
2. The end of the last digit before the access pause.	T23 = 500, 800 or 900mS
3. The mask signal is removed so that the telephone user can listen for the appearance of the second dial tone.	
4. The ≠ key is pressed to release the access pause. The antibounce timer is started.	T45 = 5 - 10 ms
5. The data from the ≠ key is accepted and the mask signal reappears. A pre-digital pause equal in length to an inter-digital pause starts.	T56 = 500, 800 or 900mS
6. The digit after the access pause is dialled out. Dialling then continues as normal.	

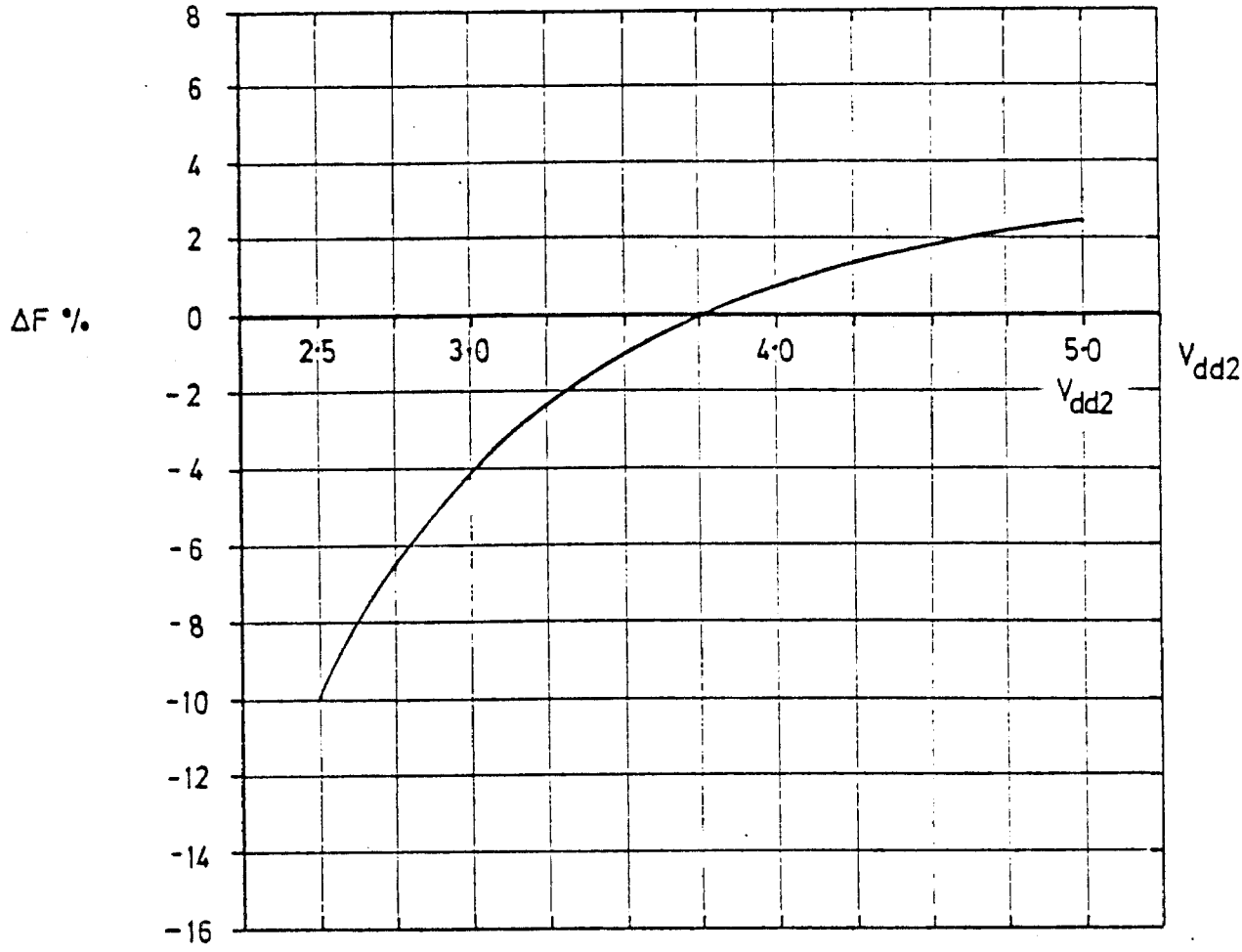


Figure 12

Typical Variation of Clock Frequency with V_{dd2}