WaveFront™ Interface

General Description

The **ICS2116** is the interface component of the WaveFront wavetable synthesis chip set. The interface chip monitors and controls the activities of the 68EC000 processor and 256K x 4 DRAM including address decoding and data buffering to and from the input source. The input can be serial, parallel, MIDI or the ISA bus emulating the MPU-401 or 6850 UART.

For systems not using the ISA bus, the WaveFront Interface can convert the serial output of the synthesizer into a form that the optional Motorola 56001 DSP can read. This option provides global digital effects like chorus and reverb to enhance the audio signal.

Features

- WaveFront interface to serial, parallel, MIDI and ISA bus
- Provides the majority of system "glue" logic, keeping parts count down and cost low
- Uses a single inexpensive 256K x 4 DRAM as system memory
- Contains small code ROM, which eliminates the code ROM in an ISA design
- Soft select of 4 different IRQs
- Part of a complete design package that includes software drivers for Windows and DOS

Applications

- ISA based sound cards
- Wavetable synthesizer daughter cards
- External sound modules that connect to a PC's serial or parallel port
- Any system requiring a self contained unit that provides high quality music synthesis of General MIDI sounds, in a low cost design

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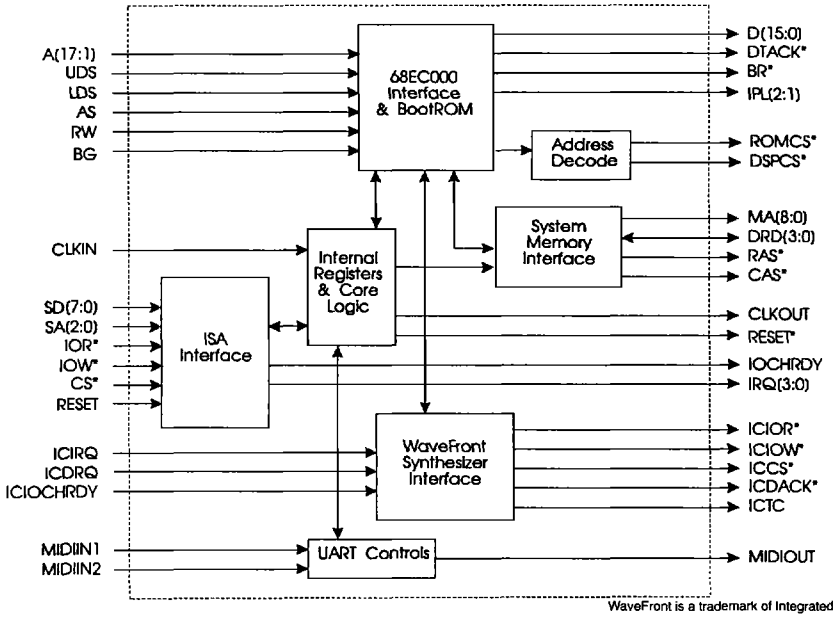
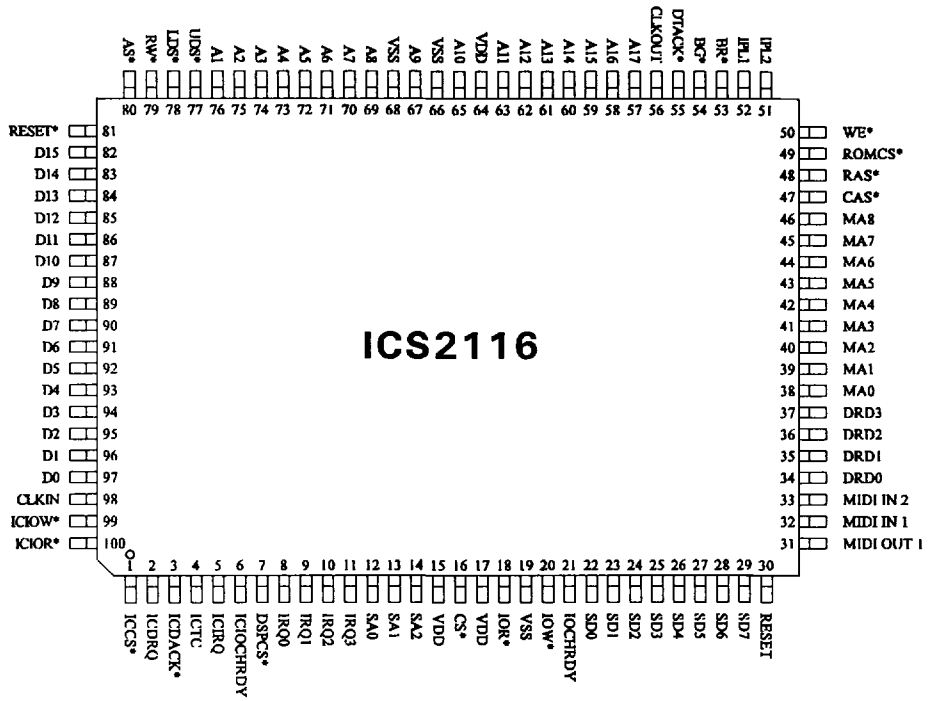
Block Diagram



Pin Configuration



100-Pin PQFP
K-11

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
12, 13, 14	SA<2:0>	I	Host Port Address Bits A2 through A0**
22-29	SD<7:0>	I/O	Host Bi-directional Data Bus
16	/CS	I	Host port Chip Select (Active Low)
18	/IOR	I	Host Read Enable (Active Low)**
20	/IOW	I	Host Write Enable (Active Low)
21	IOCHRDY	O	Host I/O Channel Ready (Active High)**
8, 9, 10, 11	IRQ<3:0>	O	Decoded Host IRQ selects. One is active, the others float in the high impedance state. (Active High)**
30	RESET	I	Master Reset (Active High)
57-63, 65, 67, 69-76	A<17:1>	I	68EC000 Address Bus
82-97	D<15:0>	I/O	68EC000 Bi-directional Data Bus
77	/UDS	I	68EC000 Upper Data Strobe (Active Low)
78	/LDS	I	68EC000 Lower Data Strobe (Active Low)
79	/RW	I	68EC000 Read/Write (Active Low)
80	/AS	I	68EC000 Address Strobe (Active Low)
55	/DTACK	O	68EC000 Data Acknowledge (Active Low)
51, 52	IPL<2:1>	O	68EC000 Interrupt Priority level (Active High)
53	/BR	O	68EC000 Bus Request (Active Low)
54	/BG	I	68EC000 Bus Grant (Active Low)
56	CLKOUT	O	CLKIN/2 for the 68EC000
81	/RESET	O	Conditioned RESET input for the 68EC000 and ICS2115 (Active Low)
1	/ICCS	O	ICS2115 Chip Select (Active Low)
100	/ICIOR	O	ICS2115 Read Enable (Active Low)
99	/ICIOW	O	ICS2115 Write Enable (Active Low)
5	ICIRQ	I	ICS2115 Interrupt Request (Active High)
6	ICIOCHRDY	I	ICS2115 I/O Channel Ready (Active High)
2	ICDRQ	I	ICS2115 DMA Request (Active High)
3	/ICDACK	O	ICS2115 DMA Acknowledge (Active Low)
4	ICTC	O	ICS2115 Terminal Count (Active High)
38-46	MA<8:0>	O	Operating System DRAM Muxed Address Bus
34-37	DRD<3:0>	I/O	Operating System DRAM Data Bus
47	/CAS	O	Operating System DRAM Column Address Strobe (Active Low)
48	/RAS	O	Operating System DRAM Row Address Strobe (Active Low)
49	/ROMCS	O	Operating System ROM Chip Select (Active Low)
7	DSPCS	O	Chip Select for a Digital Signal Processor (Active Low)
32	MIDI IN 1	I	Serial MIDI Input #1
33	MIDI IN 2	I	Serial MIDI Input #2
31	MIDI OUT 1	O	Serial MIDI Output
98	CLKIN	I	Clock Input
64, 15, 17	VDD	P	Power Supply
66, 68, 19	VSS	P	Ground

Absolute Maximum Ratings

Supply Voltage ..... -0.5 to 7.0V
Logic inputs ..... -0.5 to V_{DD}+0.5V
Ambient operating temp. ..... 0°C to 70°C
Storage temperature ..... -65°C to 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Electrical Characteristics

V_{CC}=5.0V ± 5%; GND=0V; T_A=0°C to 70°C

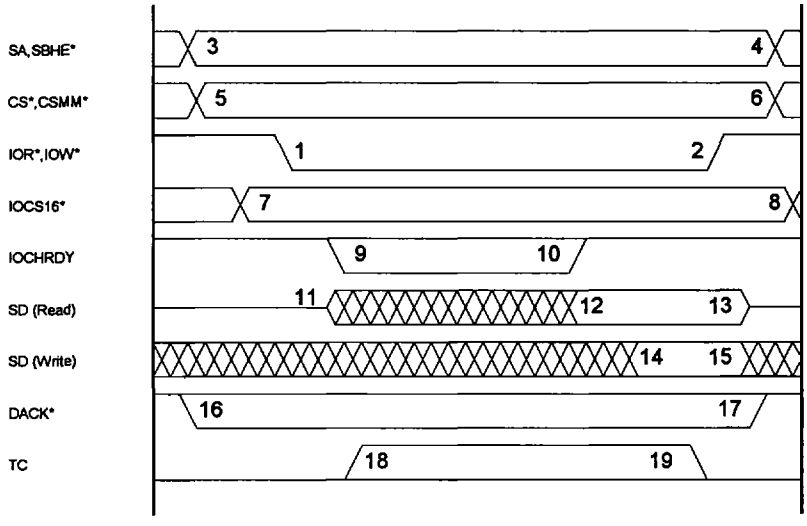
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.75	5.00	5.25	V
TTL Input Voltage Low	V_{IL}		-0.30		0.80	V
TTL Input Voltage High	V_{IH}		2.20		VDD+0.30	V
Schmidt Input Voltage Low	V_{ILS}		-0.30		1.50	V
Schmidt Input Voltage High	V_{IHS}		3.00		VDD+0.30	V
XTLI Input Voltage Low	V_{ILX}		-0.30		1.50	V
XTLI Input Voltage High	V_{IHX}		3.50		VDD+0.30	V
Output Low Current= Standard Drive	I_{OL}	V_{OL}=0.4V	4.0	6.0		mA
Output High Current Standard Drive	I_{OH}	V_{OH}=2.8V		-6.0	-4.0	mA
Output Low Current Medium Drive	I_{OL2}	V_{OH}=0.4V	6.0	9.0		mA
Output High Current Medium Drive	I_{OH2}	V_{OH}=2.8V		-9.0	-6.0	mA
Output Low Current High Drive	I_{OL3}	V_{OH}=0.4V	9.0	12.0		mA
Output High Current High Drive	I_{OH3}	V_{OH}=2.8V		-12.0	-9.0	mA
Input Leakage Current Standard Inputs	I_{IN}	VIN=V_{SS}	-1.0		1.0	uA
Pull-up Current	I_{PUP}	VIN=V_{DD}	15.0	30.0	50.0	uA
Pull-down Current	I_{PDN}		50.0	90.0	150.0	uA

Note: All pins have a maximum capacitive load of 50pf unless noted otherwise.

AC Electrical Characteristics

Please reference the timing diagram titled *Host Interface Timing*, below.

HOST INTERFACE AC TIMING PARAMETERS						
PARAMETER	SYMBOL	FROM	TO	MIN	MAX	UNITS
Address setup to command	t_{AS}	3	1	10	-	nS
Chip select setup to command	t_{CS}	5	1	10	-	nS
Address hold from command	t_{AH}	2	4	10	-	nS
Chip select hold from command	t_{CH}	2	6	10	-	nS
Command width	t_{CW}	1	2	100	-	ns
Write data setup	t_{DS}	14	2	50	-	nS
Write data hold	t_{DHW}	2	15	10	-	nS
Read data delay (ready access)	t_{DD}	1	12	0	60	nS
Read data hold	t_{DHR}	2	13	0	20	nS
DACK* setup to command	t_{DAS}	16	1	20	-	nS
DACK* hold after command	t_{DAH}	2	17	50	-	nS
TC setup to command	t_{TS}	18	2	25	-	nS
TC hold after command	t_{TH}	2	19	n/a	-	nS
TC width	t_{TW}	18	19	20	-	nS



Host Interface Timing

Miscellaneous Pins

VDD, VDDP

These are the chip power supply pins. VDD pins power the core logic, while VDDP pins power the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip by confining large switching currents to bond wires for pad supplies. These pins MUST be at the same potential externally.

VSS, VSSP

These are the chip ground pins. VSS pins ground the core logic, while VSSP pins ground the pad ring. This arrangement helps prevent switching spikes due to output transitions from disturbing the internal operation of the chip by confining large switching currents to bond wires for pad supplies. These pins MUST be at the same potential externally.

CLKIN

This input requires a 20 MHz clock source. Internally, the **ICS2116** divides this signal by two and sends it to the 68EC000 through the CLKOUT output.

ISA Host Interface

Note: This section applies to PC Mode and not Stand-Alone Mode. If /IOR is low when the /RESET input goes low, the chip enters Stand-Alone Mode, otherwise it remains in PC Mode. Stand-Alone Mode is covered in the following section. Pin descriptions for PC mode follow:

/CS

This input pin selects read/write access to emulation registers for the MIDI interface, the Media Master Interface, and the DMA transfer registers. This signal must be stable before, during, and after /IOR or /IOW strobes.

SA<2:0>

These address input pins select one of eight direct mapped registers as determined by the /CS pin. These signals must be stable before, during, and after /IOR or /IOW strobes.

SD<7:0>

This is the bi-directional data bus used for all register data transfers.

/IOR

This input pin is used to read registers when low. SA<2:0> and /CS must be stable before, during, and after the active low pulse on /IOR. If this signal is low when the /RESET input goes low, the **ICS2116** enters stand-alone mode. See the Stand-Alone Mode section for more information.

/IOW

This input pin is used to write registers when low. SA<2:0> and /CS must be stable before, during, and after the active low pulse on /IOW. SD<7:0> must be stable before, during, and after the trailing (rising) edge of /IOW.

IOCHRDY

This output pin is normally in a resistive pull-up state. During /IOR or /IOW low times, this pin can be driven low to indicate to the host that the requested data transfer is not ready, and that /IOR or /IOW should be held low until IOCHRDY goes high.

IRQ<3:0>

These outputs allow the host to choose which of four IRQs the **ICS2116** should use. Immediately following power-up, these pins are all in the high-impedance state. Software on the host side will then write to the Board Hardware Initialization Register to select one of the four IRQs. The selected IRQ will then operate as a standard TTL output, while the other IRQs remain in the high impedance-state.

RESET

This input is the active high input for the synthesizer system. When the input goes high, the /RESET output is latched low (reset state).

68EC000 Interface

The 68EC000 microprocessor communicates with the PC through the Media Master registers, located in the **ICS2116**. The **ICS2116** buffers the registers so that both the PC and the 68EC000 can access them at the same time.

To transfer blocks of data, the **ICS2116** performs a DMA-type operation. The host platform writes the desired byte or word to the Sample Transfer port, which the **ICS2116** transfers to the ICS2115 as a DMA cycle. During this operation, the **ICS2116** takes control of the data bus by requesting and receiving data from the 68EC000 (using signals /BR and /BG).

The **ICS2116** decodes the 68EC000's address lines to connect it to all of the other devices, both internal and external. Since the compact memory map is only 128K x 16, the **ICS2116** does not decode address bits 18 through 23. As a result, the map images 64 times in the 16 MB address space. The **ICS2116** does not decode A0 because address bit 0 is invalid for the 68EC000 processor in 16-bit mode.

The fixed Hardware vector, mapped in the lowest 8 bytes, points to the BootROM. This allows the 68EC000 to initialize itself with the BootROM in the **ICS2116**. Afterwards, it must load the Synthesizer operating system into OSRAM from one of three sources: the O.S. Code ROM, wavetable ROM, or from the PC via the Media Master Port.

The address space of the **ICS2116** is as follows (listed as byte addresses):

Address Definitions

Address	Size	Content
3FFFF 3FC30	488 Words	488 x 16-bit BootROM (Internal)
3FC2F 3FC20	8 Words	DSP Subsystem (Asserts /DSPCS with special timing
3FC1F 3FC18	4 Words	External I/O - /DSPCS with address timing
3FC17 3FC10	4 Words	6850 MIDI UART Configuration, Baud Rate Generator and Misc Status (Internal)
3FC0F 3FC08	4 Words	MPU-401/6850 & Media Master Interface Registers (Internal)
3FC07 3FC00	4 Words	ICS2115 Indirect Registers (Drives /ICCS, /ICIOR, & /ICIOW)
3FBFF 20000	63K Words	Optional O.S. Code ROM (Asserts /ROMCS)**
1FFFF 00008	64K Words minus 4 Words	64K x 16-bit OSRAM (Externally a 256K x 4 DRAM)
00007 00000	4 Words	Fixed H/W Vector to BootROM Address 0003FC30 (Internal)

**When disable BootROM is set, the upper 488 words of the optional external 64K OSROM replace the on chip ROM.

A<17:1>
This is the local address bus for the wavetable synthesis system.

D<15:0>
This is the local data bus for the wavetable synthesis system.

/UDS
This input connects directly to the 68EC000's Upper Data Strobe.

/LDS
This input connects directly to the 68EC000's Lower Data Strobe.

/RW
This input connects directly to the 68EC000's Read/Write Strobe.

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/AS
This input connects directly to the 68EC000's Address Strobe.

/DTACK
This output connects directly to the 68EC000's Data Acknowledge.

IPL<2:1>
These outputs connect directly to the 68EC000's Interrupt Priority Levels 2 and 1.

/BG
This output connects directly to the 68EC000's Bus Grant.

/BR
This output connects directly to the 68EC000's Bus Receive.

CLKOUT
This output provides a 10 MHz clock source for the 68EC000.

/RESET
/RESET is a conditioned version of the reset input from the host. When the RESET input goes high, the /RESET output is latched low (reset state). The host software changes the /RESET output to the non-reset state, by writing the appropriate data to the Hardware Initialization Register.

ICS2115 Interface

Based on the address decoding and the 68EC000 signals /UDS and /LDS, the **ICS2116** drives the /IOR and /IOW inputs on the ICS2115. The 68EC000 signals A1 and A2 tie directly to the ICS2115 SA0 and SA1 inputs respectively. The host interface can pass sample data to the ICS2115 through a DMA-type operation.

/ICCS
This output is the active low chip select for the ICS2115.

/ICIOR
This output is the active low read strobe for the ICS2115.

/ICIOW
This output is the active low write strobe for the ICS2115.

ICIRQ
This input accepts the hardware interrupt requests from the ICS2115.

ICIOCHRDY
This input receives the I/O Channel Ready input from the ICS2115.

ICDRQ
This input receives DMA Requests from the ICS2115.

/ICDACK & TC
These outputs operate during a DMA transfer to and from the ICS2115. /ICDACK indicates that the /ICIOR or /ICIOW is a DMA transfer. TC connects with the Terminal Count input on the ICS2115.

System DRAM Interface

The **ICS2116** interfaces with a 256K x 4 DRAM in such a way that it appears as 64K x 16 RAM to the microprocessor. The BootROM contains the code to load the synth operating system into this DRAM.

MA<8:0>
MA<8:0> are the multiplexed address lines.

DRD<3:0>
This is the four bit data bus.

/CAS
Column address Strobe for the System DRAM.

/RAS
Row address Strobe for the System DRAM.

Serial MIDI Interface

MIDI IN 1 & MIDI IN 2
These two serial MIDI inputs are switched internally, to use only one UART. The initialization register determines which MIDI input controls the synthesizer.

MIDI OUT 1
MIDI OUT 1 is a serial MIDI output.

ROM and DSP Interface

/ROMCS
This output enables the Operating System ROM. Upon initialization, the code in the BootROM transfers the operating system from the ROM to the system RAM. Afterwards, it begins execution from RAM and never accesses the Operating System ROM.

/DSPCS
This output is an address decode for a Motorola DSP.

Stand-Alone Mode

When the **ICS2116** enters Stand-Alone Mode, some of the ISA interface pins assume different functions. This is illustrated below. The chip detects this mode by checking the IOR signal when reset goes low. If IOR is low at that instant, the **ICS2116** enters "Stand-Alone Mode" and remains that way until reset or power-down occurs.

/IOR
/IOR should be tied low to signify stand-alone mode.

/BG
This input selects which baud rate the operating system will receive data on the MIDI IN 1 input. The high state indicates the standard MIDI baud rate, 31.25K. A low level indicates a rate suitable for the serial port on the PC, 38400 baud.

MIDI IN 1
This is the only usable serial input in stand-alone mode.

MIDI IN 2
MIDI IN 2 is not available in stand-alone mode.

Parallel Port Interface

/IOW
This serves as a /STROBE input for the parallel port. The **ICS2116** latches the data on SD<7:0> when the rising edge occurs.

IRQ<0>
This output serves as a Transmit Data Ready indicator for the parallel port BUSY input.

SD<7:0>
This serves a unidirectional data bus for parallel input.

/CS
This input still serves as a chip select for the parallel port. To enable the parallel interface, tie this pin low. Otherwise, tie it high.

Serial DSP Interface

SA<0>
This input receives the bit clock from the ICS2115.

SA<1>
This input receives the left/right clock from the ICS2115.

SA<2>
This input receives the serial audio data from the ICS2115.

IOCHRDY
This output is the bit clock for the serial DAC when the optional DSP is used.

IRQ<1>
This output is the bit clock for the DSP.

IRQ<2>
This output is the left/right clock for the DSP.

IRQ<3>
This output is the serial audio data for the DSP.

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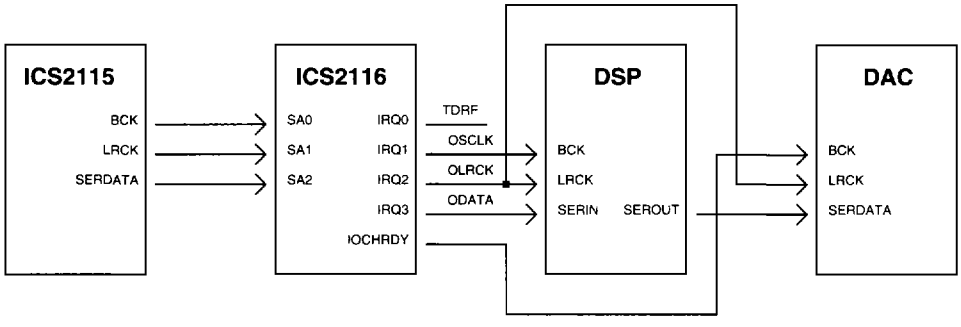


Host Interface Register Descriptions

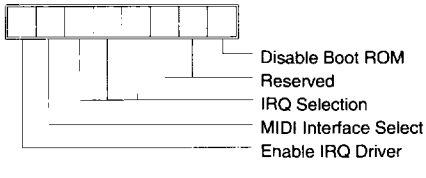
ICS provides a program named SETUPSND.EXE that initializes the **ICS2116** and downloads the Operating System to the system RAM. Using command line parameters, the user can specify the options that are contained in the Hardware Initialization Register.

The /CS input enables the Host Interface for I/O transfers. Using three address lines, the **ICS2116** has the following registers:

Base Address Offset	Function
7	Sample Data Transfer with Terminal Count (High Byte)
6	Sample Data Transfer with Terminal Count (Low Byte)
5	Sample Data Transfer (High Byte)
4	Sample Data Transfer (Low Byte)
3	Media Master Control
2	Media Master Data
1	MPU-401/6850 Port
0	MPU-401/6850 Port (Hardware Initialization Register, see below)

Hardware Initialization Register

Following power-on or a hard reboot of the host PC, the **ICS2116** resets its /RESET output which will hold the 68000 and ICS2115 in the reset state. An initialization program, running in the PC, writes to the Initialization Register. This sets the /RESET output and removes the Hardware Initialization Register from the register set. Then, the Base+0 register becomes the MPU-401/6850 Port. The format of this register is as follows:



Board H/W Initialization Register: (Base+0)

Bit 7 - Enable IRQ Driver
- 0 - Tristate the **ICS2116** IRQ outputs 3-0.
- 1 - Enable IRQ selected by bits 5:3 to be driven onto the PC Bus.

Bit 6 - MIDI Interface Select
- 0 - Use the MIDI Input 1
- 1 - Use the MIDI Input 2

Bits 5:3 - IRQ Selection
- 0 0 0 - IRQ0
- 0 0 1 - IRQ1
- 0 1 0 - IRQ2
- 0 1 1 - IRQ3
- 1 X X - All IRQs Disabled

Bits 2:1 - Reserved

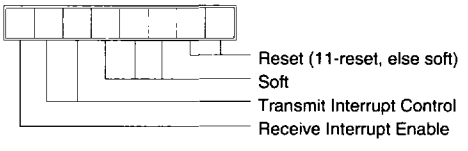
Bit 0 - Disable Boot ROM. When set to 1, the **ICS2116** selects the external ROM instead of the internal Boot ROM mapped at 03FC30-03FFFFH.

MIDI Emulation Control/Status Register

The MIDI Control Status register can be configured as either a 6850 compatible or an MPU-401 compatible sets. The MIDI Emulation Mode bit in the Media Master Emulation Mode Register will indicate which emulation mode is used. Using SETUPSND.EXE, the user can change the emulation mode.

6850 Mode Control (Base + 0) (Write Only)

The PC host application program can access this MIDI control register by writing to this address. The control register is mapped as follows.



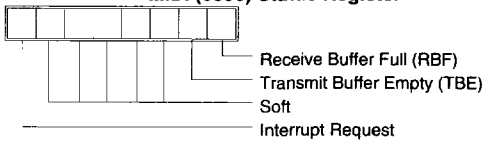
MIDI (6850) Control Register

1:0 - Reset - Resets the MIDI Port
11 = Reset (Resets Receive Buffer Full Interrupt (to the Host) and Receive Interrupt Enable)
00, 01 and 10 = No Reset
4:2 - Soft - Software controlled functions
6:5 - Transmit Buffer Empty Interrupt Control
01 = Interrupts are enabled
00, 10 and 11 = Interrupts disabled
7: - Receive Buffer Full Interrupt Enable
1 = Interrupts enabled
0 = Interrupts disabled

6850 Mode Status (Base + 0) (Read Only)

The PC host application program can access this MIDI status register by reading this address. The status register is mapped as follows.

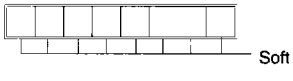
MIDI (6850) Status Register



0: - Receive Buffer Full
1 = full
0 = empty
1: - Transmit Buffer Empty
1 = empty
0 = full
6:2 - Soft
7: - Interrupt Request
1 = Interrupt pending
0 = Interrupt not pending

MPU-401 Mode Control (Base + 1) (Write Only)

The PC host application program can access this MIDI control register by writing to this address. The control register mapping is software dependent.



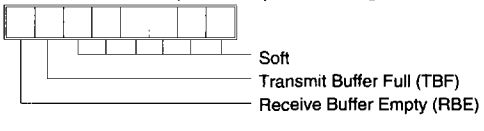
MIDI (MPU-401) Control Register

7:0 - Soft - Software controlled functions

MPU-401 Mode Status (Base + 1) (Read Only)

The PC host application program can access this MIDI status register by reading this address. The status register is mapped as follows.

MIDI (MPU-401) Status Register



5:0 - Soft
6: - Transmit Buffer Full
1 = full
0 = empty
7: - Receive Buffer Empty
1 = empty
0 = full

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MIDI Emulation Data Register

This register is the MIDI data port for writing and reading MIDI data. The PC host application program can transfer MIDI data between itself and the WaveFront Operating System via this register.

6850 Mode Data (Base + 1) (Read/Write)

Eight bit data.

MPU-401 Mode Data (Base + 0) (Read/Write)

Eight bit data.

Media Master Registers

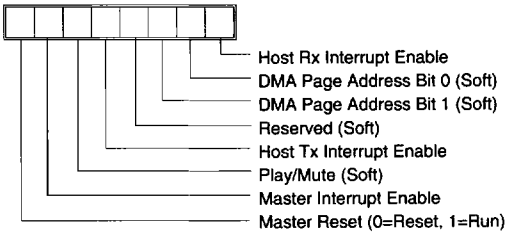
The Media Master interface provides access to the more sophisticated features of the operating system. Host programs use these registers to download wavetable data. The descriptions follow:

Host Data (Base + 2) (Read/Write)

Eight bit data register. The PC host application program can write and read this register to exchange commands and data with the WaveFront.

Host Control/*Status (Base + 3) (Write Only)*

The Host Control/Status register will have the following bit meanings when written to by the PC host application program.

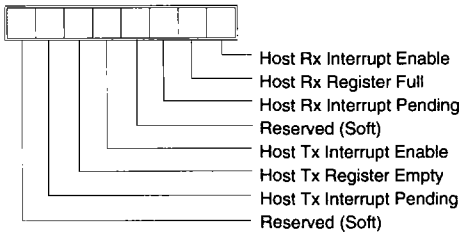


Host Control Register

0: - Host Data Receive Interrupt Enable
  1 = enable
  0 = disable
2:1 - DMA Page Address (2 bits) (Soft)
3: - Reserved (Soft)
4: - Host Data Transmit Interrupt Enable
  1 = enable
  0 = disable
5: - Play/Mute (Soft)
  1 = play
  0 = mute
6: - Host Data Master Interrupt enable
  This bit enables or disables all interrupts from the WaveFront subsystem to the PC host application program. Note that this includes the MIDI emulation mode interrupts from the MIDI Emulation Status register. It does not affect the interrupts for the WaveFront Operating System.
  1 = enable
  0 = disable
7: - Master Reset
  This bit will cause a Soft Reset to occur which resets the WaveFront chip.
  1 = run
  0 = reset (WaveFront chip soft reset)

*Host Control/*Status *(Base + 3) (Read Only)*

The Host Control/Status register will have the following bit meanings when read by the PC host.



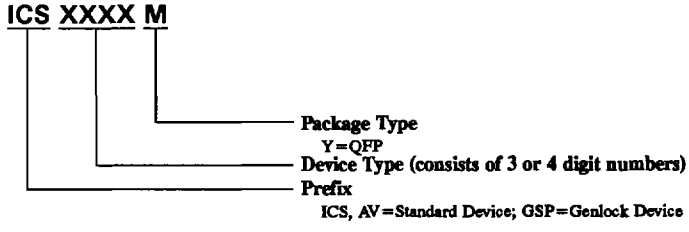
Host Status Register

0: - Host Data Receive Interrupt Enabled
  1 = enabled
  0 = disabled
1: - Host Data Receive Register Full
  1 = full
  0 = empty
2: - Host Data Receive Interrupt Pending
  1 = Pending
  0 = Not Pending
3: - Reserved (Soft)
4: - Host Data Transmit Interrupt Enabled
  1 = enabled
  0 = disabled
5: - Host Data Transmit Register Empty
  1 = empty
  0 = full
6: - Host data Transmit Interrupt Pending
  1 = Pending
  0 = Not Pending
7: - Reserved (Soft)

Ordering Information

ICS2116Y

Example:



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