MITSUBISHI MICROCOMPUTERS

M5L8048-XXXP/M5L8035LP

6249828 MITSUBISHI(MICMPTR/MIPRC) 91D 11577 D

SINGLE-CHIP 8-BIT MICROCOMPUTER

T-49-19-05

DESCRIPTION

The M5L8048-XXXP and M5L8035LP are 8-bit parallel microcomputer fabricated on a single chip using high-speed N-channel silicon-gate ED-MOS technology.

M5L8048-XXXP	Built-in ROM (1K bytes)
M5L8035LP	External ROM

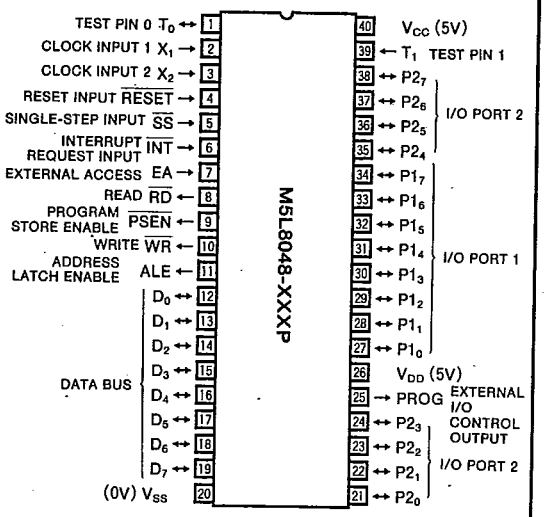
FEATURES

- Single 5V power supply
- Instruction cycle ..... 2.5μs (min)
- Basic machine instructions: 96
  - 1-byte instructions: 68
  - 2-byte instructions: 28
- Direct addressing ..... up to 4096 bytes
- Internal ROM ..... 1024 bytes (for M5L8048-XXXP only)
- Internal RAM ..... 64 bytes
- Built-in timer/event counter ..... 8 bits
- I/O Ports ..... 27 lines
- Easily expandable Memory and I/O
- Subroutine nesting ..... 8 levels
- External and timer/event counter interrupt . 1 level each
- Low power standby mode
- External RAM ..... 256 bytes
- Interchangeable with i8048 and i8035L in pin configuration and electrical characteristics

APPLICATION

- Control processor or CPU for a wide variety of applications

PIN CONFIGURATION (TOP VIEW)

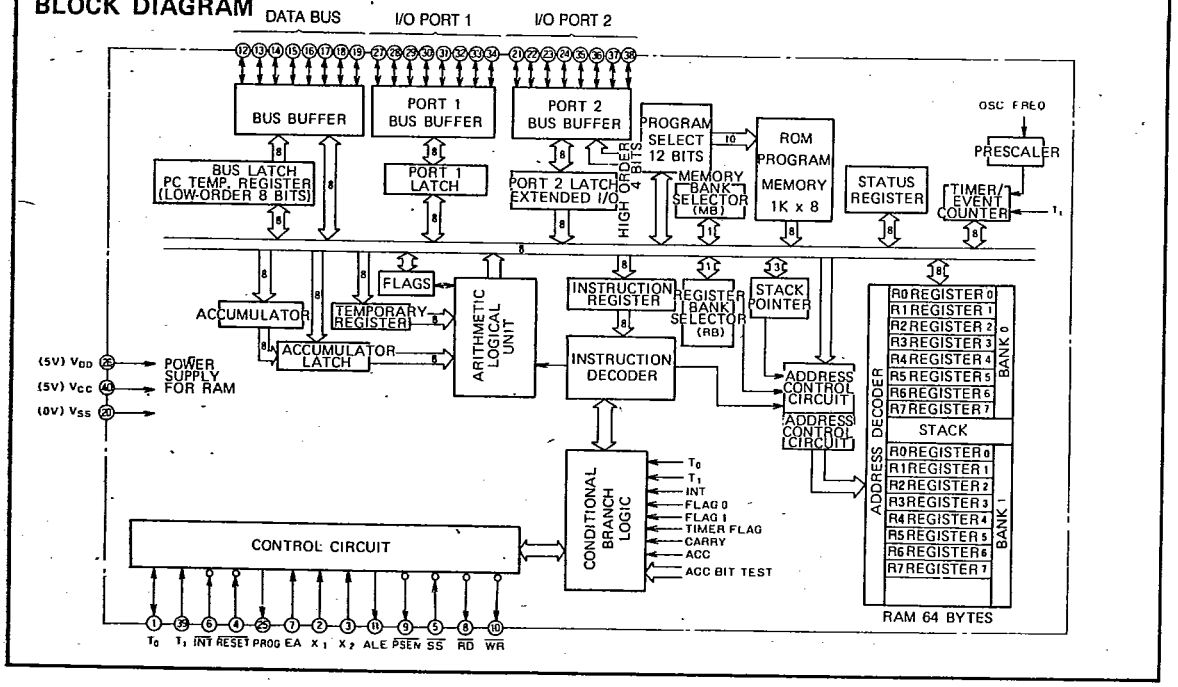


Outline 40P4

FUNCTION

The M5L8048-XXXP and M5L8035LP are integrated 8-bit CPU, with memory (ROM, RAM) and timer/event counter interrupt all contained on a single chip.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

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PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground		Normally connected to ground (0V).
V_{CC}	Main power supply		Connected to 5V power supply.
V_{DD}	Power supply		①Connected to 5V power supply. ②Used for memory hold when V_{CC} is cut.
T_0	Test pin 0	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JT0/JNT0).
		Output	②Used for outputting the internal clock signal (ENT0 CLK).
X_1, X_2	Crystal inputs	Input	External crystal oscillator or RC circuit input for generating internal clock signals. An external clock signal can be input through X_1 or X_2.
$\overline{RESET}$	Reset	Input	Control used to initialize the CPU.
$\overline{SS}$	Single step	Input	Control signal used in conjunction with ALE to stop the CPU through each instruction, in the single-step mode.
$\overline{INT}$	Interrupt	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JNI). ②Used for external interrupt to CPU.
EA	External access	Input	①Normally maintained at 0V. ②When the level is raised to 5V, external memory will be accessed even when the address is less than 400_{16} (1024). The M5L8035LP is raised to 5V.
$\overline{RD}$	Read control	Output	Read control signal used when the CPU requests data from external data memory or external device to be transferred to the data bus. (MOVX A, @R_r, and INS A, BUS)
$\overline{PSEN}$	Program store enable	Output	Strobe signal to fetch external program memory.
$\overline{WR}$	Write control	Output	Write control signal used when the CPU sends data through the data bus to external data memory or external device. (MOVX @R_r, A and OUTL BUS, A)
ALE	Address latch enable	Output	A signal used for latching the address on the data bus. An ALE signal occurs once during each cycle.
D_0~D_7	Data bus	Input/output	①Provides true bidirectional bus transfer of instructions and data between the CPU and external memory. Synchronizing is done with signals $\overline{RD}$/$\overline{WR}$. The output data is latched.
			②When using external program memory, the output of the low-order 8 bits of the program counter are synchronized with ALE. After that, the transfer of the instruction code or data from the external program memory is synchronized with $\overline{PSEN}$.
			③The output of addresses for data using the external data memory is synchronized with ALE. After that, the transfer of data with the external data memory is synchronized with $\overline{RD}$/$\overline{WR}$. (MOVX A, @R_r, and MOVX @R_r, A)
$P2_0$~$P2_7$	Port 2	Input/output	①Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After reset, when not used as an output port, nothing needs to be output.
		Output	②$P2_0$~$P2_3$ output high-order 4 bits of the program counter when using external program memory.
		Input/output	③$P2_0$~$P2_3$ serve as a 4-bit I/O expander bus for the M5L8243P.
PROG	Program	Output	Strobe signal for M5L8243P I/O expander.
$P1_0$~$P1_7$	Port 1	Input/output	Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After reset, when not used as an output port, nothing needs to be output.
T_1	Test pin 1	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JT1/JNT1). ②When enabled, event signals are transferred to the timer/event counter (STRT CNT).

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_{DD}	Supply voltage		−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
Pd	Power dissipation	Ta=25℃	1.5	W
Topr	Operating free-air temperature range		−20~75	℃
Tstg	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH1}	High-level input voltage, except X1, X2 and $\overline{RESET}$	2		V_{CC}	V
V_{IH2}	High-level input voltage, except X1, X2 and $\overline{RESET}$	3.8		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (Ta=−20~75℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL1}	Low-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	$I_{OL}=2mA$			0.45	V
V_{OL2}	Low-level output voltage, except the above and PROG	$I_{OL}=1.6mA$			0.45	V
V_{OL3}	Low-level output voltage, PROG	$I_{OL}=1mA$			0.45	V
V_{OH1}	High-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	$I_{OH}=-100\mu A$	2.4			V
V_{OH2}	High-level output voltage, except the above	$I_{OH}=-50\mu A$	2.4			V
I_I	Input leak current, T1, $\overline{INT}$	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{OZ}	Output leak current, BUS, T0 high-impedance state	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{LI1}	Input current during low-level input, port	$V_{IL}=0.8V$		−0.2		mA
I_{LI2}	Input current during low-level input, $\overline{RESET}$, $\overline{SS}$	$V_{IL}=0.8V$		−0.05		mA
I_{DD}	Supply current from V_{DD}			10	20	mA
$I_{DD}+I_{CC}$	Supply current from V_{DD} and V_{CC}			65	135	mA

TIMING REQUIREMENTS (Ta=−20~75℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Alternative symbol	t	Limits		Unit
			Min	Typ	Max	
t_C	Cycle time	t_{CY}	2.5		15.0	μs
th (PSEN-D)	Data hold time after $\overline{PSEN}$	t_{DR}	0		200	ns
th (R-D)	Data hold time after $\overline{RD}$	t_{DR}	0		200	ns
tsu (PSEN-D)	Data setup time after $\overline{PSEN}$	t_{RD}			500	ns
tsu (R-D)	Data setup time after $\overline{RD}$	t_{RD}			500	ns
tsu (A-D)	Data setup time after address	t_{AD}			950	ns
tsu (PROG-D)	Data setup time after PROG	t_{PR}			810	ns
th (PROG-D)	Data hold time before PROG	t_{PF}	0		150	ns

Note 1: The input voltage level of the input voltage is V_{IL}=0.45V and V_{IH}=2.4V.

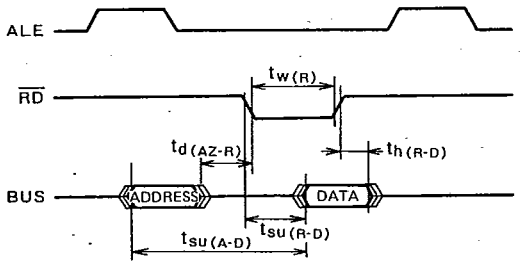
SWITCHING CHARACTERISTICS ($Ta = -20 \sim 75°C$, $V_{CC} = V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Limits			Unit
			Min	Typ	Max	
$t_{W(ALE)}$	ALE pulse width	t_{LL}	400			ns
$t_{d(A-ALE)}$	Delay time, address to ALE signal	t_{AL}	150			ns
$t_{v(ALE-A)}$	Address valid time after ALE	t_{LA}	80			ns
$t_{W(PSEN)}$	$\overline{PSEN}$ pulse width	t_{CC}	700			ns
$t_{W(R)}$	$\overline{RD}$ pulse width	t_{CC}	700			ns
$t_{W(W)}$	$\overline{WR}$ pulse width	t_{CC}	700			ns
$t_{d(Q-W)}$	Delay time, data to $\overline{WR}$ signal	t_{DW}	500			ns
$t_{v(W-Q)}$	Data valid time after $\overline{WR}$	t_{WD}	120			ns
$t_{d(A-W)}$	Delay time, address to $\overline{WR}$ signal	t_{AW}	230			ns
$t_{d(AZ-R)}$	Delay time, address disable to $\overline{RD}$ signal	t_{AFC}	0			ns
$t_{d(AZ-PSEN)}$	Delay time, address disable to $\overline{PSEN}$ signal	t_{AFC}	0			ns
$t_{d(PC-PROG)}$	Delay time, port control to PROG signal	t_{CP}	110			ns
$t_{v(PROG-PC)}$	Port control valid time after PROG	t_{PC}	130			ns
$t_{p(Q-PROG)}$	Delay time, data to PROG signal	t_{DP}	220			ns
$t_{v(PROG-Q)}$	Data valid time after PROG	t_{PD}	65			ns
$t_{W(PROGL)}$	PROG low pulse width	t_{PP}	1510			ns
$t_{d(Q-ALE)}$	Delay time, data to ALE signal	t_{PL}	400			ns
$t_{v(ALE-Q)}$	Data valid time after ALE	t_{LP}	150			ns

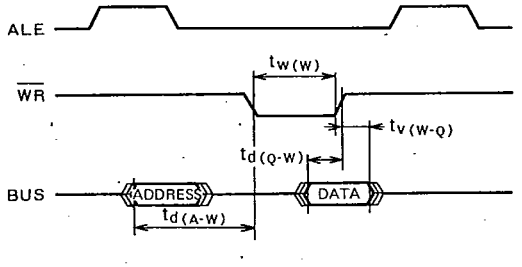
Note 2: Conditions of measurement: control output $C_L = 80pF$
data bus output, port output $C_L = 150pF$, $t_c = 2.5\mu s$
3: Reference levels for the input/output voltages are low level=0.8V and high level=2V

TIMING DIAGRAM

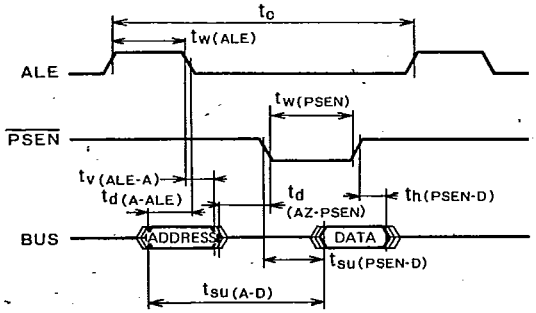
Read from External Data Memory



Write to External Data Memory



Instruction Fetch from External Program Memory



Port 2