SUPPLY VOLTAGE AND TEMPERATURE RANGE

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0V. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to 75°C.

MIL-grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range –55°C to +125°C.

TTL families may be mixed for optimum system design. The following table specify the worst case noise immunity in mixed systems.

WORST CASE TTL DC NOISE IMMUNITY/NOISE MARGINS

Electrical Characteristics											
Item	Symbol	SGS-THOMSON TTL Families	Military (– 55 to +125°C)				Commercial (0 to 75°C)				Units
			V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
6	TTL	Standard TTL (54/74)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
7	HTTL	High Speed TTL (54H/74H)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
10	LSTTL	Low Power Schottky TTL (54LS/74LS)	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate output levels. The numbers given above are guaranteed worst-case values.

LOW Level Noise Margins (Military)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	300	mV
HTTL	400	400	300	mV
LSTTL	400	400	300	mV

From "V_{OL}" to "V_{IL}"

LOW Level Noise Margins (Commercial)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	400	mV
HTTL	400	400	400	mV
LSTTL	300	300	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Military)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	400	mV
HTTL	400	400	400	mV
LSTTL	500	500	500	mV

From "V_{OH}" to "V_{IH}"

LOW Level Noise Margins (Commercial)				
From \ To	TTL	HTTL	LSTTL	Units
TTL	400	400	400	mV
HTTL	400	400	400	mV
LSTTL	700	700	700	mV

From "V_{OH}" to "V_{IH}"

FAN-IN AND FAN-OUT

In order to simplify designing with SGS-THOMSON LSTTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40μA
in the HIGH state (Logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA
in the LOW state (logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

Examples-Input Load

1. A 7400 gate, wich has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load).
2. The 74LS95 which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8mA}{1.6mA} \text{ or } 0.5 \text{ U.L.}$$

and an input HIGH load factor of

$$\frac{40\mu A}{40\mu A} \text{ or } 1 \text{U.L.}$$

3. The 74LS00 gate which has an I_{IL} of 0.36 mA and an I_{IH} of 20 μA, has input LOW load factor of

$$\frac{0.36mA}{1.6mA} \text{ or } 0.225 \text{U.L.}$$

(normally rounded to 0.25 U.L.) and an input HIGH load factor of

$$\frac{20\mu A}{40\mu A} \text{ or } 0.5 \text{ U.L.}$$

Examples-Output Drive

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16mA}{1.6mA} = 10 \text{U.L.}$$

and the output HIGH drive factor is

$$\frac{800\mu A}{40\mu A} \text{ or } 20 \text{ U.L.}$$

2. The output of the 74LS00 (Commercial Grade) will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is

$$\frac{80mA}{1.6mA} \text{ or } 5 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400\mu A}{40\mu A} \text{ or } 10 \text{ U.L.}$$

Relative load and drive factors for the basic TTL families are given in Table 1.

Table 1

Family	Input Load		Output Drive	
	High	Low	High	Low
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significant from one element to another Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS

Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie.
The pull-up resistor value is chosen from a range between a maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fanout is not exceeded when only one output is LOW).

Minimum and Maximum Pull-Up Resistor Values

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_{2(LOW)} \cdot 1.6mA}$$

$$R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \cdot I_{OH} + N_{2(HIGH)} \cdot 40\mu A}$$

where

R_X = External Pull-up Resistor

N_1 = Number of Wired-OR Outputs

N_2 = Number of Input Unit Loads being Driven

$I_{OH}=I_{CEX}$ = Output HIGH Leakage Current

I_{OL} = LOW Level Fan-out Current of Driving Element

V_{OL} = Output LOW Voltage Level (0.5V)

V_{OH} = Output HIGH Voltage Level (2.4V)

V_{CC} = Power Supply Current

Example: Four 74LS03 gate outputs driving four other 74LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25V - 0.5V}{8mA - 1.6mA} = \frac{4.75V}{6.4mA} = 742\ \Omega$$

$$R_{X(MIN)} = \frac{4.75V - 2.4V}{4 \cdot 100\mu A + 2 \cdot 40\mu A} = \frac{2.35V}{0.48mA} = 4.9K\Omega$$

where

$N_1 = 4$

$N_{2(HIGH)} = 4 \cdot 0.5$ U.L. $= 2$ U.L.

$N_{2(LOW)} = 4 \cdot 0.25$ U.L. $= 1$ U.L.

$I_{OH} = 100\ \mu A$

$I_{OL} = 8$ mA

$V_{OL} = 0.5V$

$V_{OH} = 2.4V$

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS

For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4V and the absolute maximum input voltage.

Two possible ways of handing unused inputs are:

1. Connect unused input to V_{CC}. Most 74LS inputs have a breakdown voltage >15V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1 to 10kΩ current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5V.

2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: *Do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.*

INTERCONNECTION DELAYS

For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in system using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit.

When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 150Ω to 200Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treal the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL has to do with its output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection. a situation that exists any time a transmission line is terminated by an impedance lower than its characteristics impedance. This means that when the reflection from the (essentially) open end of the interconnection arrives back at the driver it will be re-reflected with the opposite polarity. The result is a sequence of reflected signal which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

The output impedance of LSTTL, on the other hand, is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

METASTABLE CHARACTERISTIC

When a setup, hold or recovery time is violated, the response of a flip-flop is uncertain. Reliable operation under this condition cannot be guaranteed, since there is the probability that the output locks in the metastable region for a certain period.
The metastable state is defined as that time period in which the output level is not at logic "0" nor at logic "1", but stays in the region between 0.8 and 2V.